Design and Implementation of Shunt Active Power Line Conditioner using Novel Control Strategies

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Design and Implementation of Shunt Active Power Line Conditioner using Novel Control Strategies

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CERTIFICATE

This is to certify that the thesis entitled "Design and Implementation of Shunt Active Power Line Conditioner using Novel Control Strategies", submitted to the National Institute of Technology, Rourkela by **Mr.P. Karuppanan, Roll No**. **508EC103** for the award of the degree of Doctor of Philosophy in Department of Electronics and Communication Engineering, is a bonafide record of research work carried out by him under my supervision and guidance.

The candidate has fulfilled all the prescribed requirements.

The Thesis is based on candidate's own work, has not submitted elsewhere for the award of degree/diploma.

In my opinion, the thesis is in standard fulfilling all the requirements for the award of the degree of Doctor of Philosophy in Electronics and Communication Engineering.

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Dedicated to

my Nation

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ABSTRACT

Shunt Active Power Filter (APF) or Active Power Line Conditioner (APLC) is designed and implemented for power quality improvements in terms of current harmonics and reactive-power compensation. The widespread use of non-linear loads in industrial, commercial and domestic facilities cause harmonic problems. Harmonics induce malfunctions in sensitive equipment, overvoltage by resonance, increase heat in the conductors, harmonic voltage drop across the network impedance and affects other customer loads connected at the Point of Common Coupling (PCC). Active power line conditioner is implemented for compensating the harmonics and reactive-power simultaneously in the distribution system. The performance of the active power line conditioner depends on the design and characteristics of the controller adopted for APLC. The objective of this research is to find a suitable control strategy for reference current extraction as well as PWM-VSI current controller. PI / PID / FLC / PI-FLC, Fryze power theory, proposed instantaneous real-power theory, proposed sinusoidal extraction controller and modified-synchronous reference frame theory methods are utilized for extracting reference current. Furthermore, indirect PWM-current control (triangular-carrier / triangular-periodical current controller, space vector modulation controller, fixed-Hysteresis Current Controller (HCC), adaptive-HCC and adaptive-fuzzy-HCC) approach is applied to generate switching pulses of the PWM-inverter. Each reference current extraction method in conjunction with various PWM-current control techniques (or vice-versa) are simulated and investigated for the active power line conditioner. For experimental validation, the modified-synchronous reference frame with adaptive-fuzzy-HCC technique is adopted. This control algorithm is demonstrated through the TMS320F240 Digital Signal Processor for shunt APLC system.

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ABBREVIATION

AC	-	Alternating Current
AMP	-	Amplitude
APF	-	Active Power Filter
APLC	-	Active Power-Line Conditioner
ASD	-	Adjustable Speed Drive
ASIC	-	Application Specific Integrated Circuits
CENELEC	-	Comite Europeen de Normalisation Electrotechnique
CLB	-	Configurable Logic Block
CMOS	-	Complementary Metal Oxide Semiconductor
CSI	-	Current Source Inverter
DC	-	Direct Current
DSP	-	Digital Signal Processor
EDA	-	Electronic Design Automation
EPQ	-	Electric Power Quality
FBD	-	Fryze-Buchholz-Dpenbrock
FFT	-	Fast Fourier Transformation
FLC	-	Fuzzy Logic Controller
FPGA	-	Field Programmable Gate Array
HB	-	Hysteresis Band
HCC	-	Hysteresis Current Controller
HDL	-	Hardware Description Language
HVDC	-	High Voltage Direct Current
IEC	-	International Electro-technical Commission
IEEE	-	Institute of Electrical and Electronics Engineers
IGBT	-	Insulated Gate Bibolar Transistor
IOB	-	Input Output Blocks
LOM	-	Largest of Maximum
LPF	-	Low Pass Filter
LUT	-	Look Up Table
MOM	-	Middle of Maximum
NB	-	Negative Big
NM	-	Negative Medium
NS	-	Negative Small
PB	-	Positive Big
PCC	-	Point of Common Coupling
PI	-	Proportional Integral
PID	-	Proportional Integral and Derivative

PLB	-	Programmable Logic block
PLL	-	Phase locked loop
PVS	-	Positive Very Small
PS	-	Positive Small
PM	-	Positive Medium
PB	-	Positive Big
PVB	-	Positive Very Big
PWM	-	Pulse Width Modulation
RAF	-	Ripple Attenuation Factor
RTL	-	Registor Transistor Logic
rms	-	root mean square
SFU	-	Switch Fuse Unit
SMPs	-	Switched Mode Power Supply
SMPS	-	Switched Mode Power Supplies
SOM	-	Smallest of Maximum
SRF	-	Synchronous Reference Frame
SVC	-	static VAR compensators
SVM	-	Space Vector Modulation
TCCC	-	Triangular-Carrier Current Controller
THD	-	Total Harmonic distortion
TPCC	-	Triangular-Periodical Current Controller
TTL	-	Transistor-Transistor Logic
TV	-	Television
UPS	-	Uninterruptable Power Supply
VA	-	Volt Ampere
VAR	-	Volt Ampere Reactor
VCR	-	Video Cassette Recorder
VHDL	-	Very high speed integrated circuit Hardware Description Language
VLSI	-	Very Large Scale Integration
VSI	-	Voltage Source Inverter
ZE	-	Zero

LIST OF SYMBOLS

$f(t)$	-	periodic function of frequency
T_k	-	time duration of k^{th} active state vector
T_{k+1}	-	time duration of $(k+1)^{th}$ active state vector
T_s	-	sampling period
T_o	-	time duration of null vector
I_h	-	h^{th} harmonic peak current
ϕ_h	-	h^{th} harmonic current phase
V_h	-	h^{th} harmonic peak voltage
θ_h	-	h^{th} harmonic voltage phase
ω	-	angular frequency
f	-	fundamental frequency
V_s or v_s	-	supply voltage
I_s or i_s	-	source current
I_L or i_L	-	load current
I_c or i_c	-	compensation filter current
I_{sm}	-	peak value of the source current
V_{sm} or v_{sm}	-	peak magnitude value of the source voltage
I_{sp}	-	peak value of the extracted reference current
$I_{\max}$	-	magnitude of peak reference current
I_{rms}	-	rms line current
I_{sl}	-	switching loss current
m_a	-	modulation factor
V_{c1}	-	fundamendal components at ac-side of PWM-inverter
I_{c1}	-	fundamental compensation current
I_{s1}	-	fundamental supply current
m_f	-	frequency modulation ratio of the PWM-VSI.
I_{ch}	-	harmonic content of the compensation current

V_{ch}	-	harmonic content of the compensation voltage
Q_{c1}	-	reactive power factor
R_c	-	interface resistor
L_c	-	interface inductor
C_{dc}	-	dc-link capacitor
$V_{dc,ref}$	-	reference of the dc-link capacitor voltage
V_{dc}	-	dc-link capacitor voltage
$\Delta I_{c(p-p)\max}$	-	peak compensation current
ΔV	-	difference between the source voltage and the inverter voltage
$I_{c1,rated}$	-	active power line conditioner current
$V_{dr,(p-p)\max}$	-	peak to peak voltage ripple
$E_{\max}$	-	maximum energy
v_{sa}, v_{sb}, v_{sc}	-	supply voltages a-phase, b-phase, c-phase
u_{sa}, u_{sb}, u_{sc}	-	unit sine vector templates of a-phase, b-phase, c-phase
v_{ca}, v_{cb} *and* v_{cc}	-	inverter voltages a-phase, b-phase, c-phase
i_{sa}, i_{sb}, i_{sc}	-	source currents a-phase, b-phase, c-phase
$i_{sa}^*, i_{sb}^*, i_{sc}^*$	-	Reference currents a-phase, b-phase, c-phase
i_{ca}, i_{cb}, i_{cc}	-	compensation filter currents a-phase, b-phase, c-phase
i_{La}, i_{Lb}, i_{Lc}	-	load currents a-phase, b-phase, c-phase
S_A, S_B, S_C	-	switching signals a-phase, b-phase, c-phase
$e(v)$	-	error voltage
$P_L(t)$	-	load power contains
$P_f(t)$	-	fundamental or active power
$P_r(t)$	-	reactive power
$P_h(t)$	-	harmonic power
ζ	-	damping ratio
ω_{nv}	-	natural frequency
$H(s)$	-	transfer function
K_P	-	proportional gain

K_I	-	integral gain
K_D	-	derivative gain
$e(n)$	-	error signal
$ec(n)$	-	change of error signal
$a-b-c$	-	three-phase coordinate voltage /current signal
$\alpha-\beta$	-	two-phase coordinate voltage/current signal
p_{ac}	-	real power
$\overline{p_{ac}}$	-	real power losses
p	-	instantaneous real-power
i_α' and i_β'	-	auxiliary currents
p' and q'	-	auxiliary powers
$p_{3\varphi}$	-	three-phase instantaneous active power
G_e	-	conductance or admittance
$i_d - i_q$	-	direct axis (d) – quadratic axis (q) rotating coordinates currents
$\vec{V}$	-	magnitude of the space vector
i_{dc}	-	dc-current component
v_{ref}	-	reference voltage vector
L	-	phase inductance
$i_{sa}+$	-	rising current segment
$i_{sa}-$	-	falling current segment
t_1 and t_2	-	switching intervals of time t_1 and t_2
f_c	-	modulation frequency
m	-	slope of the reference current
Hz	-	Hertz
µF	-	Micro Farad
mH	-	milli Hentry
kW	-	Kilo Watts
mV/div milli	-	Volt per division
Ω	-	Ohm
s	-	time periods in seconds
%	-	percentage

CHAPTER 1

INTRODUCTION

1.1. Introduction

Generally, electrical engineers are focused on the subject of generation, transmission, distribution and utilization of electric energy. The distribution system is a vital connection between the generation and utilization of electrical power at rated amplitude and frequency, which indicates the Electric Power Quality (EPQ) [1]. EPQ is often used to express voltage as well as current quality, reliability of service, and quality of power supply, etc. Poor power quality sources are raised from two categories: (i) Non-linear loads, electrical components and equipments (ii) Subsystems of transmission and distribution systems. Quality degradation of electric power mainly occurs due to power line disturbances such as impulses, notches, voltage sags / swell, voltage and current unbalance, interruption and harmonic distortions [2]. The electric power quality has become an important part of the distribution power system. Harmonics are the primary cause for the poor power quality of the distribution system.

Harmonics are qualitatively defined as sinusoidal waveforms having frequencies that are integral multiples of the power line frequency. In power system engineering, the term harmonic is widely used to describe the distortion for voltage or current waveforms [3]. The power line frequency (fundamental) is 50 Hz or 60 Hz. In case the fundamental frequency is 50 Hz, then 5^{th} harmonic is 250 Hz, and 7^{th} harmonics is 350 Hz, etc. Nonlinear loads are the main source of harmonic related problems. All electronic loads are mostly non-linear and generate harmonics in the power system. These non-linear loads draw only short pulses of current from supply network and combine with the source impedance resulting in distortion of the supply voltage [4]. The modern power electronics provide suitable topology to mitigate the power quality problems [5]. This chapter discusses the harmonic distortion and its solutions based on shunt active power line conditioner.

1.2. Research motivation

AC power supply feeds different kind of linear and non-linear loads. The non-linear loads like power converters and solid state drives that use high speed switches are the main sources of harmonics in the power system [6]. The harmonics in the system induce several undesirable issues; such as increased heating in transformers, low power factor, torque pulsation in motors, overvoltage by resonance, harmonic voltage drop across the network impedance, poor utilization of distribution plant and also affects other loads connected at the same Point of Common Coupling (PCC). Traditionally, passive filters have been used to compensate the harmonic distortion in the distribution system. Passive filters consist of inductive and capacitive elements and are tuned to control harmonics. The passive filter is connected in shunt with the distribution system and is tuned to present low impedance to a particular harmonic current. However, it is found that the passive filter is not commonly used for low-voltage or medium-voltage applications since the complexity and reliability factors are matters of concern. It also inherits several shortcomings such as ageing and tuning problems, resonance that affects the stability of the power distribution systems, bulky in size and also fixed compensation [7]. To solve these problems, different configurations of Static VAR Compensators (SVCs) have been proposed. Unfortunately some SVC generates lower-order harmonics themselves and the response time of the SVC system may be too long to be acceptable for fast-fluctuating loads. Recently, Active Power Filter (APFs) or Active Power-Line Conditioners (APLCs) are developed for compensating the harmonics and reactive-power simultaneously [8]. The APLC topology can be connected in series or shunt and combinations of both (unified power quality conditioners) as well as hybrid configurations [9-11]. The shunt active power line conditioner is most commonly used than the series active power line conditioner, because most of the industrial, commercial and domestic applications need current harmonic compensation.

1.3. Harmonics in the power system

Harmonic related problems are not new in the electric power system. From the early 1920's harmonics are observed in power equipment because of telephone line interference. The proliferation of power converter equipment connected to the

distribution power system which limits harmonic current injection maintains good power quality [12]. The various standards and guidelines have been established that specify limits on the magnitudes of harmonic currents and voltages. The Comite Europeen de Normalisation Electrotechnique (CENELEC), International Electro-technical Commission (IEC), and Institute of Electrical and Electronics Engineers (IEEE) specify the limits on the voltages at various harmonic frequencies of the utility frequency [13]. In 1983, IEEE Working Group made a reference about harmonic sources and effects on the electric power system. There is significant activity in the IEEE-Power Engineering Society and IEEE-Industry Applications Society to detect harmonic effects. These societies and institutes define standards for harmonics [14]. T.C.Shuter surveyed and reported the harmonic levels (three classes of distribution circuits; residential, commercial and industrial) in the American Electric Power Distribution System [15]. Christopher reported the statement "The Static Power Converter Committee of the Industry Applications Society recognized the harmonic related problems and started work on a standard that would give guidelines to users and engineer-architects in the application of static power converter drives and other uses on electric power systems that contained capacitors. The result was IEEE 519-1981, IEEE Guide for Harmonic Control and Reactive Compensation of Static Power Converters" [16]. Joseph mentioned about harmonics-causes, effects, measurements, and analysis with Specific system in the cement, steel and carbon industries [17]. Alexander E. Emanuel surveyed the harmonic voltages and currents at the customer point of industrial, commercial and residential applications [18]. In 1996, IEEE working group proposed definitions for power terms that are practical and effective when voltage and/or currents are distorted and/or unbalanced. It also suggests definitions for measurable values that may be used to indicate the level of distortion and unbalance [19]. Eric J. Davis reported the harmonic pollution metering as a theoretical consideration. He advocated "Toll Road" concept: this method requires each consumer to pay according to the amount of stress (usage) his equipment causes to the mitigation equipment [20]. Jacques discussed the concept of apparent power in single-phase sinusoidal and unbalanced three-phase situations under IEEE Standard 1459-2000. Here power factor is defined as the ratio of the actual active power to the apparent power in the power system [21]. Salvador noticed about IEEE Standard 1459. It includes new definitions for the measurement of electric power quantities

under sinusoidal, non-sinusoidal and balanced or unbalanced conditions [22]. Predrag reported about power components estimation according to IEEE Standard 1459–2010 under wide-range frequency deviations. This statement clarifies using adaptive phase shifter, cascaded integrator–comb filter, finite-impulse-response comb filter, algorithm [23]. Yao Xiao described the harmonic summation method for the standard IEC / TR 61000-3-6 in the power system [24]. The IEEE standard 1459 is intended to evaluate the performance of modern equipment or to design and build the new generation of instrumentation for energy and power quantification.

1.3.1. Harmonic sources [13-154]

- *Modern power electronic devices* such as fluorescent lamp, static power converter, arc furnace, Adjustable Speed Drives (ASDs), electronic control and Switched Mode Power Supplies (SMPS) are drawing non-sinusoidal current which contain harmonics.
- *Switching of power electronic devices* which includes power electric converter, controlled rectifiers, uncontrolled rectifiers, inverter, static VAR compensator, cycloconverters and High Voltage Direct Current (HVDC) transmission
- *Single-phase power supplies* including personal computers, fax machines, photocopier, Uninterruptable Power Supplies (UPSs), Televisions (TVs), Video Cassette Recorders (VCRs), microwave ovens, air conditioners, electronic ballasts for high efficiency lighting and single phase ac and dc drives

1.3.2. Harmonic problems [15-17]

- Amplification of harmonic levels resulting from series and parallel resonance.
- Plant mal-operation.
- Malfunctioning and failure of electronic components.
- Overheating and failure of electric motors.
- Overloading, overheating and failure of power factor correction capacitors.
- Overloading and overheating of distribution transformers and neutral conductors.
- Excessive measurement errors in metering equipments.
- Spurious operation of fuses, circuit breakers and other protective equipments.

- Voltage glitches in computer systems results in loss of data.
- Electromagnetic interference in HF communication systems such as television, radio, communication and telephone systems and similar signal conditioning devices.

1.3.3. End effects of harmonics [18-20]

- Higher power cost
- Premature office equipment failure and data corruption or loss
- Computer and system lockups
- Loss of productivity and higher cost of products and/or services
- Reduced product or service quality and reduced quality assurance
- Loss of Customer Confidence and revenue

1.3.4. Mitigation of harmonics

The harmonic related problem is mitigated by using active power quality conditioner. The active power quality conditioner can be connected in series or parallel and combinations of both (unified power quality conditioners) as well as hybrid configurations [9-12]. The series APLC operates as a voltage regulator and harmonic isolator between the nonlinear load and distribution system. The series active filter injects voltage component in series with the supply voltage and therefore can be regarded as controlled voltage source, compensating voltage sags and swells on the load side. The injected harmonic voltages are added or subtracted, to / from the source voltage to maintain pure sinusoidal voltage across the load. Hybrid APLC is a combination of passive and active power line conditioner. The hybrid series APLC is controlled to act as harmonic isolator between the source and non-linear load by injection of controlled harmonic voltage source. Unified power quality conditioner is the integration of the series and shunt APLC. The series active power filter has the capability of voltage regulation and harmonic compensation at the utility-consumer point of common coupling. The shunt active power filter absorbs current harmonics, compensate for reactive-power and negative-sequence current, and regulate the dc-link voltage between both active power line conditioners. Power system current harmonics are the major problems in the distribution system, due to widespread use of non-linear loads. From the literature, the shunt active power line conditioner is an

attractive choice to solve the current harmonic as well as reactive-power problems. The shunt APLC is compensating harmonic currents drawn by the non-linear loads besides power factor correction.

1.4. Shunt active power line conditioner

Shunt active power line conditioner uses power electronics to produce complementary harmonic components that compensates the harmonic components produced by the non-linear load. This harmonic filter consists of a power converter unit and control unit, which controls the harmonic injection of the filter into the ac network based on the measured load harmonics. Therefore, this device senses voltage and current harmonics and generates offsetting harmonics to cancel out the superfluous harmonics in the source. There obviously exists a feedback mechanism by virtue of which the source provides clean waveforms for the load. Voltage regulation and power factor control are also normal byproducts of this filter operation. Some of the merits of using active power line conditioner are [25]

- Harmonic reduction
- Reduction of three-phase neutral return current
- Impact minimization upon the distribution transformer
- Power factor improvement
- Voltage regulation
- Automatically adapts to changes in the ac network and load fluctuation
- Eliminating risk of resonance between filters and network impedance

1.4.1. Approach used in the thesis

In this thesis, the parallel or shunt active power line conditioner configuration is chosen. The active power line conditioner is connected in parallel with the load being compensated at Point of Common Coupling (PCC). For this power circuit, a Pulse Width Modulation (PWM) based two-level voltage source inverter is in use, which operates in a current control mode. The current compensation is performed in time domain approach (specification) for faster response. The purpose is to inject the compensating current at the parallel point such that the source current becomes

sinusoidal, since this shunt active power line conditioner is used for cancelling the current harmonics [26].

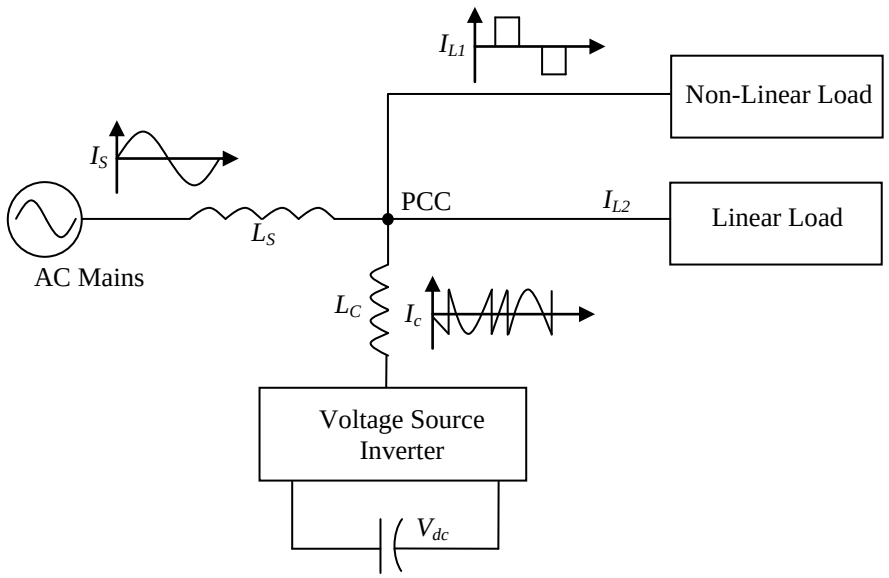


Fig.1.1 Schematic diagram of shunt active power line conditioner

Fig.1.1 shows the schematic diagram of shunt active power line conditioner. The dc-side of the voltage source inverter (also called shunt active power inverter) is connected to an energy storing capacitor and the ac-side of the inverter is connected to the ac-bus through the interface inductor. The ac-bus can supply industrial, commercial and domestic loads including the non-linear loads. The active power line conditioner is controlled in a closed loop manner, the inverter switches are controlled to actively shape the current through the coupling (interface) inductor *(L_C)* following a reference current such that the input current from the source is in-phase and of the same shape as the input sinusoidal voltage. Thus, the active power line conditioner supplies reactive and harmonic components of the load current and hence the source will be required to supply only the in-phase fundamental component of the load current.

The current waveform for cancelling harmonics is achieved with the help of active power inverter and an interfacing inductor. This interfacing inductor or filter provides isolation inductance to convert the voltage signal created by the inverter to a current signal for cancelling harmonics. The compensation filter current waveform is

obtained by accurately controlling the switches in the active power inverter. Control of current wave shape is limited by the switching frequency of the inverter and by the available voltage across the interfacing inductor. The voltage across the interfacing inductance determines the maximum *di/dt* that can be achieved by the active power inverter. This is important in the sense that relatively high values of *di/dt* may be required to compensate the higher order harmonic components. Therefore the choice of the inductor is essential. A large inductor would be better for isolation from the power system and protection from transient disturbances. However, the large size of the inductor would limit the ability of the compensator to compensate the higher order harmonics [27].

In this configuration, it is important to know the active power line conditioner is required to supply the compensating filter current at PCC. In an ideal situation, the active power line conditioner is required only to supply the reactive power of the load and hence the average dc-link capacitor voltage should remain constant. In practice, this however is not true as the losses of the inverter and interface inductor will make the dc charge stored in the capacitor to fall. However, it is important to keep the dc charge or voltage of the dc storage capacitor nearly constant so that the functioning of the system remains unaffected. This can only be done by drawing active current from the source to replenish the losses through a feedback mechanism. Therefore to put the active power line conditioner in use it is significant to discuss the following concerns

- The efficient reference current extraction method to extract the required reference current
- The control strategy, taking into account transient and steady state
- The high efficiency large capacity converter used as the power circuit
- The indirect PWM-current control scheme of the converter

1.5. Literature reviews

The controller is the most significant part of the active power line conditioner system and currently various control strategies are reported in the literature. There are essentially two types of controllers requirement in an active power line conditioner: (i) Reference current extraction method to generate the reference current from the

distorted line current (ii) PWM-VSI current control technique to generate the switching pulses to drive the inverter.

1.5.1. Reference current extraction method

Many control methods are proposed in the literature to extract the reference currents from the distorted line currents. Classification according to reference current extraction techniques can be computed as time domain and frequency domain method [28-29]. Control strategy in the frequency domain is based on the Fourier analysis of the distorted current signals to extract the compensating reference current. Frequency domain approaches are suitable for both single and three-phase systems. The frequency-domain based Fast Fourier Transformation (FFT) algorithms, sine multiplication technique and modified Fourier series technique provides accurate individual and multiple harmonic load current detection. Control strategy in the time domain is based on the instantaneous derivation of compensating commands in the form of current signals from distorted or harmonic polluted current signals. Time domain approaches are mainly used for three-phase systems. The merit of time-domain method is its fast response compared to frequency-domain [30-31]. S. Fryze developed a new control method based on rms value of voltage and current known as fryze power theory. M. Depenbrock promoted the power analysis method based on the fryze power theory and it was further modified by F. Buchholz, this improved method is now known as FBD (Fryze-Buchholz-Dpenbrock) method and the required reference currents calculated from the active component currents [32-33]. Hirofumi Akagi developed three-phase, three-wire shunt active power line conditioner system with a proposed instantaneous reactive power theory. It is possible to extend the instantaneous reactive power theory developed in this paper to the three-phase circuit including zero-phase sequence components. The reference currents are calculated instantaneously without any time delay by using the instantaneous voltages and currents on the load side. The control circuit consists of several analog multipliers, dividers, and operational amplifiers [34]. Bhattacharya proposed the calculation of the *d-q* components (direct and quadratic) of the instantaneous three-phase currents. This method creates a synchronous reference frame concept and is used to generate the reference currents from the load currents [35]. Watanabe reported the conventional active and reactive power theory, valid for the steady-state analysis and the

instantaneous power theory. This instantaneous theory is valid for steady-state / transient-state, generic voltage and current waveforms [36]. A generalized instantaneous reactive power theory which is valid for sinusoidal or non-sinusoidal, balanced or unbalanced three phase power systems with or without zero-sequence currents was later proposed by Peng and Lai [37]. Nassar Mendalek developed a nonlinear decoupling control method of a three-phase three-wire voltage source shunt active power line conditioner. The reference currents are extracted from the sensed non-linear load currents by applying the synchronous reference frame method [38]. Reyes S conducted a study experiment of the *p - q* original theory, *d - q* transformation, modified or cross-product formulation, *p - q- r* reference frame, and vectorial-theory. All these methods achieve the targets, if the supply voltage is balanced and sinusoidal. None of them is achieved, in their original development, a zero distortion index value if the supply voltage is non-sinusoidal [39]. Salem Rahmani demonstrated the nonlinear control technique to extract reference currents for a three-phase shunt active power line conditioner. The method provides compensation for reactive, unbalanced, and harmonic load current components [40]. Rondineli described new strategies to improve the transient response time of harmonic detection using adaptive filters applied to shunt active power line conditioners [41]. Ricardo introduced a robust adaptive control strategy of active power line conditioners for power-factor correction, harmonic compensation, and balancing of non-linear loads. The reference currents are generated by the dc-link voltage controller based on the active power balance of the system. They are aligned to the phase angle of the power mains voltage vector, by using a *d-q* phase-locked loop system [42]. The conventional PI and PID controllers are also used to estimate the required magnitude of reference current by controlling the dc-link capacitor voltage of the PWM-inverter [43]. However, these controllers require a precise linear mathematical calculation of the system, which is difficult to obtain under parametric variations and load disturbances. In recent years, many artificial intelligence (fuzzy logic, Artificial Neuro-fuzzy and genetic algorithm, etc.) control methods are proposed to extract the reference current from the distorted line current [44-47]. The fuzzy logic controller is used to estimate the magnitude of reference current and maintain the dc-voltage of the PWM-inverter nearly constant. This method doesn't

require an accurate numerical calculation; it can work with imprecise inputs and can handle nonlinearity [48-50].

1.5.2. PWM-current control technique

Various PWM-VSI current control techniques are proposed for active filter applications. David Brod reported a general overview of the behavior and inherent limitations of PWM-current controllers when commanding currents in a three-phase load. The predictive controller is the most complex and extensive hardware which may limit the dynamic response of the controller. The ramp comparison controller has the advantage of limiting the maximum PWM-inverter switching frequency and producing well defined harmonics, but the controller requires a large gain and has lower bandwidth. The hysteresis controller with three independent controls works very well, except when the voltage source inverter switching frequency is higher than required and when there is low counter EMF due to limited cycles. The switching frequency can be reduced by introducing zero voltages at the appropriate times [51]. Akira Nabae proposed a novel control scheme which is not a predictive control but a feedback control. It is able to suppress higher harmonic current in steady state and also solve the quick current response problem in transient state [52]. Bimal K Bose, proposed an adaptive hysteresis-band current control technique of a voltage-fed PWM inverter for the machine drive system. It maintains the modulation frequency to be nearly constant. Although the technique is applicable to general AC drives and other types of load, an interior permanent magnet synchronous machine load is considered [53]. Marian presented two-novel simple control strategies for PWM-VSI current-controller. Both methods are based on the three-level hysteresis comparators which select appropriate voltage source inverter output voltage vectors via switching electrically programmable read-only memory table. The first controller works with current components represented in a stationary AC components system, and the second one with a rotated (field-oriented) dc components system. The theoretical principle of these methods are discussed and compared with three independent two-level hysteresis controller [54]. Dixon modeled different current modulation techniques for voltage source inverter and evaluated them practically. He used periodical-sampling controller, triangular-carrier controller and hysteresis current controller. The triangular-carrier controller claimed best harmonic distortion and the

current ripple lower than other methods. However, this method with proportional gain introduced overshoot problems. The periodical-sampling controller improves with moderate time delays and displayed better performance when slow power switches are used. The hysteresis-band instantaneous current control PWM technique is popularly used because of its simplicity in implementation [55]. Bong-Hwan Kwon reported a novel space-vector-modulation (SVM)-based hysteresis current controller. This technique utilizes all advantages of the hysteresis controller and SVM technique. The controller determines a set of space vectors from a region detector and applies a space vector selected according to the main hysteresis controller. A set of space vectors including the zero vector to reduce the number of switchings are determined from the sign of the output frequency and output signals of the three-comparators with a little larger hysteresis band than that of the main hysteresis controller [56]. G.H. Bode implemented a three-level hysteresis current controller for single phase inverter. This achieves substantial reduction in the magnitude and variation of the switching frequency and improves efficiency compared to two-level hysteresis current controller [57]. Murat Kale used an adaptive hysteresis band current controller for active power line conditioner to eliminate harmonics and to compensate the reactive power of three-phase rectifier. The adaptive hysteresis band current controller changes the hysteresis bandwidth according to modulation frequency, supply voltage, dc-link capacitor voltage and slope of the reference compensator current [58]. However, this adaptive-hysteresis current controller ensures more switching power losses due to high frequency, which is solved by adaptive-fuzzy-hysteresis current controller. B.Mazari used fuzzy hysteresis control and parametric optimization of a shunt active power line conditioner. The adaptive-fuzzy hysteresis band technique is used to derive the switching signals and also to choose the optimal value of the decoupling inductance. This approach permits to define a systematic hysteresis band for designing a look-up control using the instantaneous supply voltage and mains current as input variables; and the hysteresis band as an output variable to maintain the modulation frequency quasi constant [59]. In recent years, the control algorithms are coded in high level language and implemented in DSP / FPGA processor for efficient performance of the active power line conditioner [60-61]. The PWM-switching pulses applied to PWM-inverter should meet the requirements of harmonics of the load and

maintains the dc-voltage constant. Therefore, the APLC with non-linear load should draw only sinusoidal unity power-factor balanced currents from the AC mains.

1.6. Objective of the thesis

The main objective of this research is to design and develop a suitable control strategy (ies) for shunt active power line conditioner to reduce the harmonic currents. Increased use of non-linear loads results in current harmonics in the distribution system. The shunt active power line conditioner provides current harmonic as well as reactive-power compensation. Many techniques have been suggested in the literature for current harmonics compensation. However, all these schemes indicate one or more drawbacks such as load impedance, large system in size, inadequate current regulator bandwidth, poor system efficiency and complexity of control methods and difficulty in hardware implementation. Keeping in view the above considerations, the objectives of the thesis can be defined as follows

- To implement a voltage source inverter based shunt active power line conditioner, which provides adequate current regulator bandwidth, achieve high efficiency, and fast transient response.

- To determine a suitable control strategy for the extraction of reference current from the distorted line currents.

- To determine a suitable PWM-current controller technique for switching pulse generation to drive the voltage source inverter

- To evaluate the performance of the active power line conditioner in terms of harmonic and reactive-power compensation through simulations.

- To develop an experimental setup to validate the active power line conditioner system in real-time.

1.7. Scopes and contributions

Thesis contribution is the design and implementation of suitable control strategy for shunt active power line conditioner. The main scopes of works can be outlined as follows

- The power circuit for the shunt active power line conditioner is constructed using force commutated two-level PWM-voltage source inverter. The appropriate PWM-VSI current control strategy is proposed in order to turn-ON and OFF power circuit for active power line conditioner.

- The practical implementation uses simple and cost effective TMS320F240 DSP controller.

- Control algorithm is partially executed and tested with Xilinx / Spatran3E FPGA (field programmable gate array) target device.

- To test the harmonic compensation, a diode / thyristor rectifier load is used.

The specific contributions are as follows

- Suitable control techniques are developed to generate the reference currents from the distorted line current. The following harmonic extraction controllers are designed for active power line conditioner
  - Study of PI / PID / Fuzzy and PI-Fuzzy Controller
  - Study of fryze power theory
  - Proposed instantaneous real-power theory
  - Proposed sinusoidal extraction control strategy
  - Proposed modified-SRF

- The projected indirect PWM-VSI current control techniques reduce the switching power losses. The following techniques are developed to generate the switching pulses for the inverter
  - Triangular-carrier current controller

- Triangular-periodical current controller
- Space Vector Modulation Controller
- Fixed-HCC
- Adaptive-HCC
- Adaptive-fuzzy-HCC

- The THD of the source current is reduced to less than 5 %, which complies with IEC 61000-3 and IEEE 519 harmonic standards.

1.8. Organization of the thesis

Chapter 1 introduces the concept of active power line conditioner. The basis for this problem along with detailed literature review is presented. The objective of the thesis and outline of the thesis is also presented.

Chapter 2 describes the shunt active power line conditioner topology, system configuration, characteristics of harmonics as well as compensation principle and the filter design. The active power line conditioner topologies are developed with voltage source inverter. The active power line conditioner configuration is categorized into single and three phase system to meet the requirements of various types of nonlinear loads. It is explained in detail in this chapter.

Chapter 3 describes the reference current extraction methods. PI, PID, FLC and PI-FLC, Fryze power theory, proposed instantaneous real-power theory and sinusoidal extraction controller, and also modified-SRF methods are developed to extract the required reference currents from the distorted line currents. The proposed instantaneous real-power theory is derived from the conventional $p-q$ theory. The algorithm is developed from sensing dc-link capacitor voltage, three-phase source voltages and currents (no need to sense load current and compensation filter current). It reduces the number of sensors and hence decreasing the complexity of the controller. The instantaneous $\alpha-\beta$ current components are calculated from $v_\alpha - v_\beta$ with instantaneous real power losses, and the reactive-power are considered as zero. This approach reduces the calculations and provides better performance than the conventional methods. The modified-SRF method is incorporated with a simplified unit vector generation for vector orientation that is discussed in this chapter.

Chapter 4 describes the various indirect PWM-VSI current control techniques for active power line conditioner. The TCCC, TPCC, SVM, fixed-HCC, adaptive-HCC and adaptive-fuzzy-HCC techniques are derived to generate the required switching pulses of the PWM-inverter. A novel fuzzy-adaptive-HCC technique comprising better features of adaptive and fuzzy techniques is presented that facilitates reduction of switching losses. These techniques are discussed in this chapter in detail.

Chapter 5 investigates the performance of the shunt active power line conditioner by employing different methods of active power line conditioner control techniques. Each reference current extraction method with various PWM-current control techniques (or vice-versa) is validated through extensive simulation using Matlab / Simpower tools. The active power line conditioner system is tested under diode / thyristor-rectifier load in both steady-state and transient conditions. Various performance metrics are evaluated and the indication of THD establishes the superiority of the proposed techniques. Comparisons between different control techniques on the same simulation platform are conducted.

Chapter 6 focuses on the hardware set-up and experimental verification of the three-phase shunt active power line conditioner. For hardware implementation, the modified-SRF control method and adaptive-fuzzy-HCC is adopted. This control algorithm is executed through TMS320F240DSP for active power line conditioner system. Furthermore, we take up the study of the FPGA controller for three-phase active power line conditioner using Matlab / system generator and ISE-Xilinx. The objective is to demonstrate how the control circuit could be simplified by the use of FPGAs. The controller is validated for proposed instantaneous real-power theory and adaptive-fuzzy-HCC.

In chapter 7 general conclusions are derived from the thesis. This chapter also presents some future directions for research in the area of active power line conditioner.

CHAPTER 2

STUDY OF SHUNT APLC SYSTEM

2.1. Introduction

This chapter presents shunt active power line conditioner topology, system configuration, characteristics of harmonics as well as compensation principle and the system design. The shunt active power line conditioner is normally designed for current harmonic compensations in the ac power distribution system. It is used in low power (<100 kVA), medium power (100 kVA-10 MVA) and high power (>10 MVA) applications [62]. The active power line conditioner system consists of power circuit and the control unit. The power circuits are usually developed with PWM-converters and the topologies can be classified as [63]

- Current Source Inverter (CSI)
- Voltage Source Inverter (VSI)

The active power line conditioner system categorized into following two types of configurations to meet out the requirements of the various types of nonlinear loads.

- Single-phase system
- Three-phase system
    - Three-phase three-wire system
    - Three-phase four-wire system

The design of shunt active power line conditioner comprises the device (power transistor), dc- link capacitor, interface inductor parameters and control unit [64]. The control unit is implemented through the reference current extraction method with PWM-current control technique. In recent years, the digital controllers for APLC are implemented using Microprocessor / DSP / FPGA for real time operations.

2.2. APLC topologies

The active power line conditioner has been developed for harmonic compensation, reactive power, and voltage balance in ac power networks. The APLC is developed

with PWM based current source inverter or voltage source inverter. The current source inverter behaves as non-sinusoidal current source to meet out the harmonic current requirement of the nonlinear load. The voltage source inverter is more convenient for active power line conditioner implementation when it is operated as current-controlled voltage source [65]. CSI and VSI are well known terminologies, however we mention about these configurations for continuity purpose.

2.2.1. Current source inverter

The structure of the current source inverter is shown in Fig.2.1 (a). It is built with six-controllable unidirectional switches. It has to carry the entire current as demanded by the load. The current source active power line conditioner is connected with PCC through the series transformers, which filters the carrier frequency components from the inverter currents [66]. The dc-current supply is implemented using large dc-inductor in series. The inductor dc-current should be at least as high as the peak value of the compensating current. The current source inverter provides distinct advantages such as direct output current control, high converter reliability due to the unidirectional nature of the switches and the inbuilt short-circuit protection. However, it has a self-supported dc-reactor ensures the continuous circulation of the dc-current. Again, it requires high values of parallel capacitor filters at the ac-terminals to remove unwanted current harmonics, bulky in size and more expensive than VSI. This configuration cannot be used in multilevel or cascaded configurations to allow harmonic compensation in higher power ratings [25].

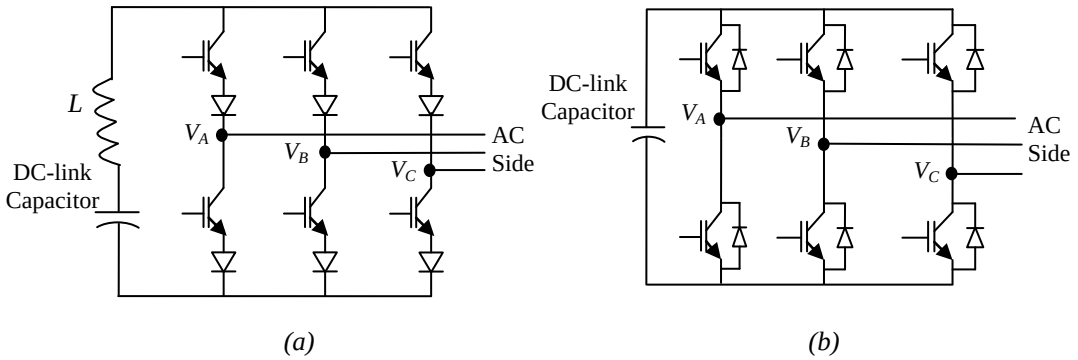


Fig. 2.1 (a) Current source inverter and (b) Voltage source inverter

2.2.2. Voltage source inverter

The PWM-voltage source inverter is more convenient for shunt active power line conditioner applications, because of light-weight, cheaper, and expandable to multilevel topologies to improve its performance for higher power rating compensation with lower switching frequencies [67]. The structure of the voltage source inverter is shown in Fig.2.1 (b). It is built by using six-controllable power transistors with anti parallel diodes. The voltage source inverter operates as current-controlled voltage source. Conventionally, two-level voltage source inverter has been used to connect the system to the ac mains through an interface inductor (transformer). An electrolytic capacitor maintains the dc-voltage constant and ripple free. This type of configuration is aimed to compensate non-linear load rated in the medium power range (100 kVA) due to semiconductors rated value limitations. However, the multilevel or cascaded PWM-VSI have been developed to active power line conditioner for medium voltage and higher rated power applications [68].

2.3. Shunt APLC configurations

APLC is basically categorized into single-phase system and three-phase system configurations to meet out the requirements for the various types of nonlinear loads in supply systems.

2.3.1. Single-phase system

Harmonics in single-phase customer equipment make the use of active power line conditioner to improve the performance of the distributed power systems. The widespread use of computers, printers and electronic equipments, in offices and household appliances create harmonic related problems and it can be solved by single-phase active power line conditioner [63]. The single-phase shunt APLC is implemented using voltage source inverter which consists of two-leg, four-switching power transistor with a DC - link capacitor as shown in Fig.2.2. The inverter is connected in parallel with loads to PCC through interface inductor. The single-phase shunt APLC compensates current harmonics by injecting equal but opposite harmonic compensation current. As a result, the compensated current becomes sinusoidal and it is in phase with the voltage.

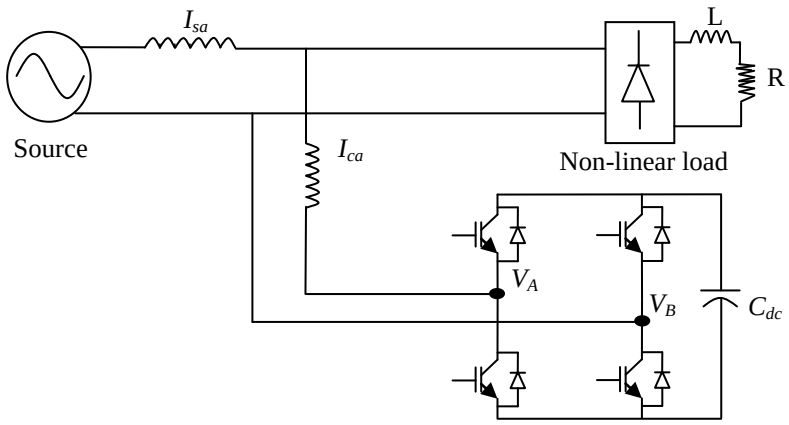


Fig.2.2 Single-phase shunt active power line conditioner system

2.3.2. Three-phase three-wire system

Fig.2.3 shows the two-level PWM-voltage source inverter includes three-phase, three-wire shunt active power line conditioner system. The PWM-VSI consists of six-power transistors with dc - link capacitor and it is connected with the PCC through interface inductor. The interface inductor does the function of suppressing the higher order harmonic components caused by the switching operation of the power transistors. Reduction of current harmonics is achieved by injecting equal but opposite current harmonic components with the PCC, thereby canceling the original distortion and improving the power quality of the connected power system [63-65].

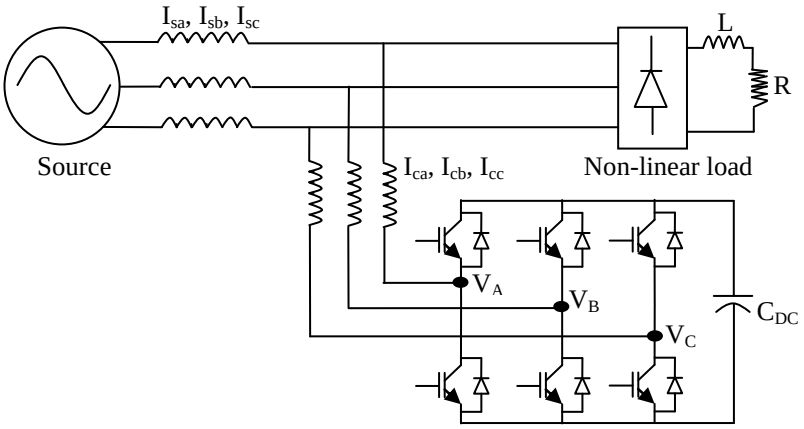


Fig.2.3 Three-phase three-wire shunt active power line conditioner system

2.3.3. Three-phase four-wire system

PWM-voltage source inverter with three-phase four-wire active power line conditioner is configured by two-different approaches [63]: (i) Four-leg inverter, in which the ac neutral is provided through the fourth leg of the inverter (ii) Three-leg inverter and the ac neutral wire are connected directly to the midpoint of the dc-bus [25]. Fig 2.4 (a) consists of four-leg voltage source inverter, three-legs are needed to compensate the three-phase currents and fourth-leg compensates the neutral current. The four-leg voltage source inverter has eight power transistors and an energy storage capacitor. The second approach is cost effective and it is simple in design. It utilizes standard three-leg inverter where the dc-link capacitor is split and the midpoint of the capacitor is connected to the fourth wire, to provide the return path for the neutral current as shown in Fig.2.4 (b). These type three-phase four-wire APLC system is used in many industries to compensates current harmonics by injecting an equal but opposite harmonic compensating current [69].

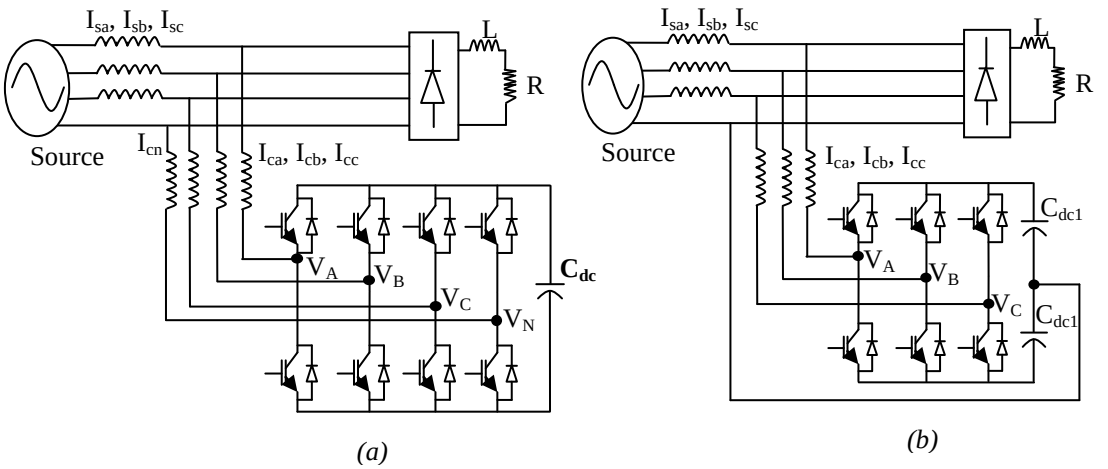
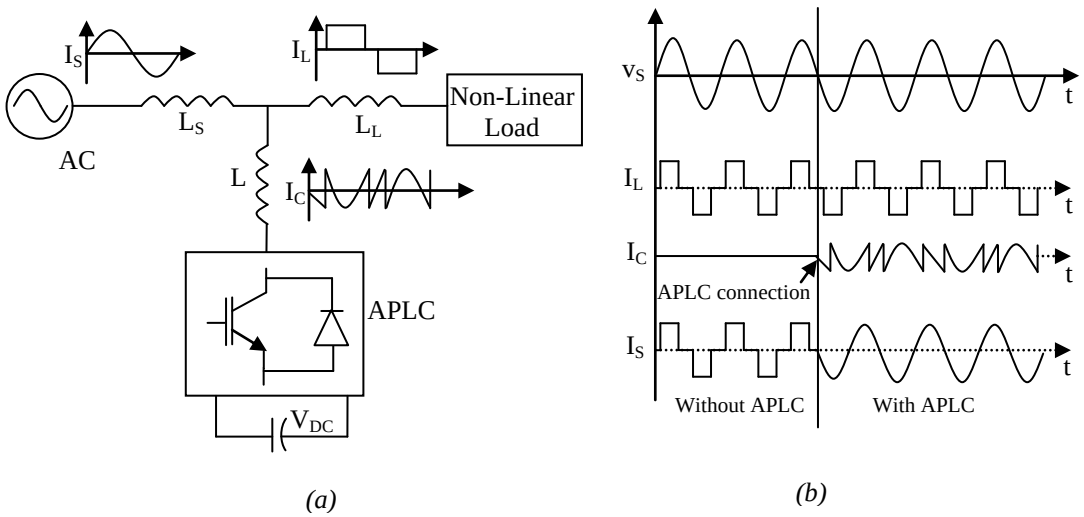


Fig.2.4 Three-phase 4-wire shunt APLC system (a) 4-leg inverter (b) 3-leg inverter

2.4. Principle of the shunt APLC system

The basic principle of active power line conditioner was proposed during 1970s. However, the actual design of active power line conditioner was proposed by Gyugyi and Strycula in 1976 [70]. The shunt APLC often refers to the compensation in the current harmonics and reactive-power. Fig.2.5 (a) shows the schematic diagram of the

shunt active power line conditioner and Fig.2.5 (b) presents the corresponding waveforms of the system. The shunt active power line conditioner compensates current harmonics by injecting equal-but-opposite harmonic components. It operates as current source injecting the harmonic components generated by the load but phase shifted by 180^0. As a result, components of harmonic currents in the load current are cancelled by the effect of the shunt APLC and the source current remains sinusoidal and in phase with the respective voltage [71]. This principle is applicable to any type of non-linear load that creates harmonics.



(a) *(b)*

Fig.2.5 (a) Schematic diagram of shunt APLC system and (b) Schematic waveforms

2.4.1. Characteristics of harmonics

Harmonic distortion is noticed in both the voltage and current waveform. Most of the current distortion is generated by electronic loads or non-linear loads. These non-linear loads might be single phase or three-phase. The electronic loads generate positive and negative sequence as well as zero sequence harmonic currents. The Fourier series represents an effective way to study and analyze the harmonic distortion [72]. We are presenting the following discussion for continuation and gaining insight for our research perspective.

$$f(t) = a_0 + \sum_{h=1}^{\infty} [a_h \cos(h\omega t) + b_h \sin(h\omega t)]$$
$$= a_0 + \sum_{h=1}^{\infty} c_h \sin(h\omega t) + \psi_h \tag{2.1}$$

where,

$f(t)$ - periodic function of frequency f

$\omega = 2\pi f$ - angular frequency period

$T = 1/f = 2\pi/\omega$ - time period

c_h - h^{th} harmonic of amplitude

hf - harmonic frequency and ψ_h - phase

The Fourier series coefficients are given by

$$a_0 = \frac{1}{T}\int_0^T f(t)\,dt = \frac{1}{2\pi}\int_0^{2\pi} f(t)\,dx, \quad where\, x = \omega t \tag{2.2}$$

$$a_h = \frac{2}{T}\int_0^T f(t)\cos(h\omega t)dt = \frac{1}{\pi}\int_0^{2\pi} f(t)\cos(hx)dx \tag{2.3}$$

$$b_h = \frac{2}{T}\int_0^T f(t)\sin(h\omega t)dt = \frac{1}{\pi}\int_0^{2\pi} f(t)\sin(hx)dx \tag{2.4}$$

$$c_h = \sqrt{a_h{}^2 + b_h{}^2} \qquad and \qquad \psi_h = \tan^{-1}\left(\frac{a_h}{b_h}\right) \tag{2.5}$$

The distorted periodic current or voltage waveform expanded into a Fourier series is expressed as follows

$$I(t) = \sum_{h=1}^{\infty} I_h \cos(h\omega t + \varphi_h) \tag{2.6}$$

$$V(t) = \sum_{h=1}^{\infty} V_h \cos(h\omega t + \theta_h) \tag{2.7}$$

where,

I_h - h^{th} harmonic peak current, ϕ_h is the h^{th} harmonic current phase

V_h - h^{th} harmonic peak voltage, θ_h is the h^{th} harmonic voltage phase

ω -angular frequency $\omega = 2\pi f$, f is the fundamental frequency

2.4.2. Characteristics of harmonic compensation

From the grid, the instantaneous supply voltage V_s is written as

$$V_s(t) = V_{sm} \sin \omega t \tag{2.8}$$

The instantaneous source current I_s is represented as

$$I_s(t) = I_L(t) - I_c(t) \tag{2.9}$$

The non-linear load current I_L comprises the fundamental and harmonic current components, which is represented as [73]

$$\begin{aligned} I_L(t) &= \sum_{h=1}^{\infty} I_h \sin(n\omega t + \Phi_h) \\ &= I_1 \sin(\omega t + \Phi_1) + \left(\sum_{h=2}^{\infty} I_h \sin(n\omega t + \Phi_h) \right) \end{aligned} \tag{2.10}$$

In equation (2.10), there are three terms

$$I_L(t) = \underbrace{I_1 \sin(\omega t)}_{active} + \underbrace{I_1 \cos(\omega t)}_{reactive} + \sum_{n=2}^{\infty} \underbrace{I_h \sin(n\omega t + \Phi_h)}_{harmonics} \tag{2.11}$$

The instantaneous load power is computed from the supply voltage and the load current. The load power calculation is given as

$$\begin{aligned} P_L(t) &= I_L(t) * V_s(t) \\ &= \left[V_{sm} I_1 \sin^2 \omega t * \cos \varphi_1 \right] + V_{sm} I_1 \sin \omega t * \cos \omega t * \sin \varphi_1 + \\ &\qquad \left[V_{sm} \sin \omega t * \left(\sum_{h=2}^{\infty} I_h \sin(n\omega t + \Phi_h) \right) \right] \\ &= P_f(t) + P_r(t) + P_h(t) \end{aligned} \tag{2.12}$$

From the above equation, the load power has fundamental or active power $P_f(t)$, reactive power $P_r(t)$ and harmonic power $P_h(t)$.

The real (fundamental) power is extracted from the total load power and it is given as

$$P_f(t) = V_{sm} I_1 \sin^2 \omega t * \cos \varphi_1 = V_s(t) * I_s(t) \tag{2.13}$$

If the active power line conditioner provides the total reactive and harmonic power, the source current $I_s(t)$ will be in phase with the supply voltage and should be sinusoidal. The source currents after compensation can be expressed as

$$I_s(t) = P_f(t) / V_s(t) = I_1 \cos\varphi_1 \sin\omega t = I_{sm} \sin\omega t \quad (2.14)$$

where,

$I_{sm} = I_1 \cos\varphi_1 \sin\omega t$ - peak value of the source current

There are also some switching losses in the voltage source inverter, and hence the utility must supply small overhead for the capacitor leakage and inverter switching losses in addition to the real power of the load. The total peak current supplied by the source is therefore

$$I_{sp} = I_{sm} + I_{sl} \quad (2.15)$$

where,

$I_{sp} = I_1 \cos\varphi_1 + I_{sl}$ - peak value of the extracted reference current,

I_{sl} - switching loss current.

If the active power line conditioner provides the total reactive and harmonic power; then $I_s(t)$ will be in phase with supply voltage and close to sinusoidal waveform. In this case, the active power line conditioner must provide the following compensation current

$$I_c(t) = I_L(t) - I_s(t) \quad (2.16)$$

Hence, for accurate and instantaneous compensation of reactive and harmonic currents, it is necessary to estimate the fundamental component of the load current.

2.5. Design of the shunt APLC system

Several methods are reported for designing the APLC system parameters. This section presents an overview of common methods and their obtained values for the system specifications [74]. To design the active power line conditioner system, the following components are used

a) Device selection

b) Reference capacitor voltage selection

c) Interface inductor selection

d) dc-link capacitor selection

e) Control unit

The design of these components is based on the following assumptions [75]

- The AC source voltage is sinusoidal
- To design the interface inductor, AC side line current distortion is assumed to be 5%
- There is fixed capability of reactive power compensation of the active power line conditioner
- The PWM-VSI is assumed to operate in the linear modulation mode
- The switching frequency selected is a function of the highest order of harmonics to be compensated

a) Device selection:

The voltage and current rating of the device selection is based on the following factors:

- Maximum current flow through the device
- Maximum voltage stress on the device during the OFF period
- Switching frequency

Maximum current flow: Considering one leg of the inverter, the maximum current flow through the switch S_A when S_A is closed (and S_A' is open) and it is equal to the maximum line current [76]. The maximum line current is same as the per phase current in a three-phase system. The maximum current flow is same for all the devices.

Maximum Voltage stress: Considering the same situation of S_A being closed and S_A' being open, the maximum voltage is blocked by the switch S_A' which is V_{dc}. Generally the blocking voltage is chosen slightly higher than V_{dc} so as to avoid device failure.

Switching frequency required: For a composite compensation of both reactive and harmonic currents, the switching frequency should be as large as possible. Usually PWM frequency used is ten times the harmonic frequency to be compensated [27].

For reactive power compensation, 500 Hz would be good enough as we want to compensate only 50 Hz component. However, for harmonic compensation when we want to compensate a 13th harmonic we should use 6.5 kHz to compensate that 650 Hz component and so on. However, the switching losses increase as the device is operating at high switching frequency.

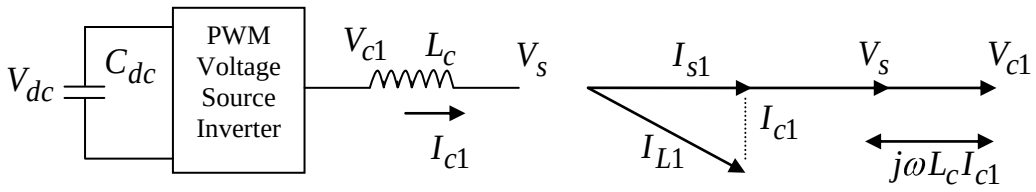


Fig.2.6 Vector diagram

b) Reference capacitor voltage selection:

The PWM-VSI is assumed to operate in the linear modulation mode $(0 \le m_a \le 1)$, and then the amplitude modulation factor m_a is calculated as [77]

$$m_a = \frac{V_m}{V_{dc}/2} \tag{2.17}$$

where $V_m = \sqrt{2}V_{c1}$

Hence,

$$V_{dc} = 2\sqrt{2}V_{c1} \text{ for } m_a = 1 \tag{2.18}$$

where,

V_{c1} - fundamental components in the ac-side of PWM-inverter.

According to the compensation principle, the APLC compensate the current I_{c1} (means fundamental) to the reactive power of the load. The supply current I_{s1} should be in phase with the supply voltage V_s and the compensation current I_{c1} should be orthogonal to V_s as shown in Fig.2.6. Based on the circuit theory,

$$V_{c1} = V_s + j\omega L_c I_{c1} \tag{2.19}$$

The exact range of V_{c1} must be set according to the capacity requirement of the system. However, based on the above analysis, the allowable V_{c1} should be in the range

$$V_s < V_{c1} \leq 2V_s \tag{2.20}$$

$V_{c1} > 2V_s$ is not necessary, since the maximum capacity produced is less than the case $V_{c1} = 2V_s$. In addition, larger V_{c1} means higher V_{dc}, and thus higher voltage stress are caused to the switches. Once V_{c1} is determined, the required V_{dc} is calculated with the equation (2.18) by substituting $m_a = 1$.

However, for a known specific non-linear load (for example three phase rectifier), the reference voltage selected is a function of the peak value of supply voltage and the maximum harmonic order to be compensated. Therefore,

$$V_{dc} = 2\sqrt{2}V_{(ch)\max} \tag{2.20}$$

where, $V_{(ch)\max}$ - maximum voltage value of $V_c(t)$ which includes harmonic compensation

$$V_c(t) = V_s + \frac{6}{\pi} L_c.\omega.I_c(-\cos 5\omega t - \cos 7\omega t + \cos 11\omega t + ...) \tag{2.21}$$

If the inductor output filter is small due to high switching frequency, the voltage V_{c1} is approximately equal to the source voltage, and then the equation (2.18) will be

$$V_{dc} = 2\sqrt{2}V_s \tag{2.22}$$

Assuming a value of $1.1.V_{dc}$, the dc-voltage is regulated to be *10%* above the peak input voltage. However, the required V_{dc} is reduced due to the sine reference for PWM is modulated with third and ninth harmonics. The minimum required voltage is expressed in terms of the source voltage as follows

$$V_{dc} = \frac{2\sqrt{2}}{1.155}V_s \tag{2.23}$$

c) Interface inductor selection:

The interface inductors should be at lower flux density with enough ventilation between the conductor and core of the inductor. The following necessities can be enforced on the estimation of interface inductor value [74].

- Provide path for compensation currents (also the rate of change of current) for harmonics and reactive power
- Ensure filtering to a certain quality level of PWM-inverter output current and voltage source ripples

First approach: The design of interface inductor L_c is based on considering the capability of reactive power compensation and harmonics current reduction. The inductor is also used to filter the ripples of the compensation current caused by the switching of the inverter. For the sinusoidal PWM-VSI is assumed to operate in the linear modulation mode, the maximum harmonic voltage occurs at the frequency $m_f \omega$ [75]. Considering this harmonic content, the ripple current of the APLC compensation current is given as

$$I_{ch} = I_{ch}(m_f \omega) = \frac{V_{ch}(m_f \omega)}{L_c(m_f \omega)} \tag{2.24}$$

where, the subscript h is used for representing the harmonics m_f is the frequency modulation ratio of the PWM-VSI. For the quantitative representation, Ripple Attenuation Factor (RAF) is defined as

$$RAF = \frac{I_{ch}}{I_{c1,rated}} \tag{2.25}$$

The three-phase reactive power Q_{c1} delivered from the active power line conditioner to the system is calculated from the vector diagram, shown in Fig. 2.6

$$Q_{c1} = 3V_s I_{c1} = 3V_s \frac{V_{c1}}{\omega L_c}\left(1 - \frac{V_s}{V_{c1}}\right) \tag{2.26}$$

By solving equations (2.24) and (2.26) simultaneously the value of L_c and V_{c1} is calculated.

Second approach: The peak ripple current is the chosen criterion for designing the interface inductor. For calculating the ripple current, no-load condition is considered and the effect of inductor resistance is supposed to be negligible. Under this condition, the reference voltage of the inverter is equal to the supply voltage [64]. Thus the required inductor is given by

$$L_C = \frac{V_S}{2\sqrt{6}\, f_S\, \Delta I_{c(p-p)\max}} \tag{2.27}$$

where, $\Delta I_{c(p-p)\max}$ - 15% of peak compensation current

Third approach: The inductor value is considered as the maximum current I_{max} that the filter must supply in order to compensate a totally inductive load [80], is as follows

$$L_{c\min} = \frac{\Delta V}{\omega I_{max}} \tag{2.28}$$

where,

ΔV -the difference between the source voltage and the inverter voltage, which depends on the values of the dc-voltage and the modulation index

ω -value of the fundamental frequency.

In order to keep the ripple current at reduced level, the used inductor value should not be less than this. As an active power line conditioner, the inductor value is decreased to be capable of higher surge and harmonic currents. In this condition, other criteria can be evaluated. Imposing a fixed switching frequency f_S the maximum di/dt of the current to be compensated, and the ripple current ΔI_C inductance value is given by

$$L_{c\max} = \frac{\Delta V_{\max}}{4\, f_S\, \Delta I_{c(p-p)}} \tag{2.29}$$

If the ripple is reduced by increasing in the switching frequency or by controlling dynamics, the design of inductor will not influence the global filter performance. The connecting inductances also decouple the output inverter voltage from the ac source voltage. Taking into account all these referred factors, the value of the inductor between two extremes of the minimum and maximum current is considered as,

$$\frac{\Delta V}{\omega I_{max}} \le L_C \le \frac{\Delta V_{\max}}{4\, f_S\, \Delta I_{c(p-p)}} \tag{2.30}$$

Fourth approach: The inductor required in the active power line conditioner for current control is determined from the constraint on the maximum ripple current, $\Delta I_{(p-p)\max}$ [74]. In a six switching power transistor, the maximum ripple current occurs at the zero-crossings of the fundamental frequency component of the output voltage [81]; the inductor value is computed as

$$L_c = \frac{V_{dc}}{6\, f_c\, \Delta I_{(p-p)\max}} \tag{2.31}$$

The first approach is commonly used in many APLC applications for designing the interface inductor. The interface inductor suppresses the harmonics caused by the switching operation of the power transistors. The inductor provides smoothing as well as isolation for high frequency components and the voltage source inverter. Control of the current wave shape is limited by the switching frequency of the inverter and by the available driving voltage across the interface inductor.

d) dc-link capacitor selection:

The dc-link capacitor of the voltage source inverter performs two significant functions: (i) maintains the dc-voltage nearly constant with small ripples in steady state (ii) serves as an energy storage element to supply real power difference between load and source during the transient period. In steady state, the real power supplied by the source should be equal to the real power required by the load with small power to compensate the losses in the active power line conditioner. However, when the load condition changes, the real power balance between the mains and the load will be disturbed. This real power difference needs to be compensated by the dc-link capacitor. In order to operate satisfactorily of the active power line conditioner, the peak value of the reference current must be adjusted proportionally to change the real power drawn from the source. This real power charged / discharged by the capacitor compensates the real-power consumed by the load. The determination of dc-link capacitor is made either by the stored capacitor energy released instantaneously to support the step increase or decrease in the power consumed by the linear or non-linear load.

First approach: The design of the dc-link capacitor is based on the principle of instantaneous power flow on the dc and ac side of the PWM-inverter [75]. The selection of C_{dc} is governed by reducing the voltage ripple. The dc-link capacitor C_{dc} is found from rated active power line conditioner current $I_{c1,rated}$ and peak to peak voltage ripple $V_{dr,(p-p)\max}$. It is defined as

$$C_{dc} = \frac{\pi * I_{c1,rated}}{\sqrt{3}\,\omega V_{dr,(p-p)\max}} \tag{2.32}$$

Second approach: The capacitor has to supply the real power demand of the load for one cycle of the supply voltage during the transient condition. Hence, the capacitor value equation based on the principle is as follows [74]

$$C_{dc} = \frac{2E_{\max}}{{V_{dc}}^2 - {V_{dc\min}}^2} \tag{2.33}$$

where,

$E_{\max}$ - maximum energy that the capacitor has to supply during the transient condition.

Third approach: The dc-link capacitor deals with ripple power at 2ω due to the negative-sequence load current. The minimum capacitor value is calculated as

$$C_{dc} = \frac{S}{2.\omega.V_{dc}.\Delta V_{dc}} \tag{2.34}$$

Fourth approach: The first approach is based on the measurement of the lowest rank harmonic current I_h. The capacitor value is determined by [74]

$$C_{dc} = \frac{I_h}{\varepsilon.V_{dc}.\omega} \tag{2.35}$$

The second approach is based on calculation of the energy provided by the active power line conditioner for a half-cycle period of the power pulsation related to the first two harmonics (5^{th} and 7^{th} for a three phase rectifier). By choosing an acceptable rate ripple (example $\varepsilon = 5\%$) the capacitor C_{dc} is calculated as follows

$$C_{dc} = \frac{V_s\sqrt{{I_5}^2 + {I_7}^2 - 2I_5I_7\cos(5\alpha - 7\alpha)}}{2.\omega.{V_{dc}}^2.\varepsilon} \tag{2.36}$$

where,

α - firing angle delay.

e) Control unit: The control unit consists of the reference current extraction method and the PWM-current control technique [82-83].

Reference current extraction method: Many control methods are proposed in the literature to extract the reference currents from the distorted load currents. Some of the reference current extraction methods are PI, PID, FLC and PI-FLC, Fryze power theory, proposed instantaneous real-power theory, sinusoidal extraction controller, and modified-SRF theory. These methods are derived and explained in chapter 3.

PWM-current control technique: Various current control techniques are proposed for active power line conditioner applications, such as triangular-carrier / triangular-periodical current controller, space vector modulation, fixed-HCC, adaptive-HCC, adaptive-fuzzy-HCC techniques. These methods are explained in chapter 4.

2.6. Conclusions

The active power line conditioner can be implemented with current source inverter or voltage source inverter. The PWM-voltage source inverter is more convenient for shunt active power line conditioner applications, due to light-weight, cheaper, and expandable to multilevel configuration to improve its performance for higher power rating compensation. The single-phase and three-phase active power line conditioner system is configured to meet out the requirements for the various types of nonlinear loads. The single-phase active power line conditioner is mostly used in home applications, whereas the three-phase active power line conditioner is used in industrial applications. The concept of shunt active power line conditioner system and the characteristics of harmonic components as well as compensation principles are discussed. The design of various components in shunt active power line conditioner has been studied in this chapter.

CHAPTER 3

REFERENCE CURRENT EXTRACTION METHODS

3.1. Introduction

The reference current extraction method is classified into time-domain and frequency-domain. The time-domain method is used to extract the reference current from the harmonic line current with simple algebraic computation. The frequency-domain based on Fast Fourier Transformation (FFT) method provides accurate individual and multiple harmonic load current detection. The merit of time-domain method has fast response compared to frequency-domain [29-31]. The following time-domain methods are carried out for the active power line conditioner. Several techniques are available in the literature as discussed in Chapter-1; we have carried out a comprehensive investigation including our proposed methods for the sake of comparison.

- Study of PI, PID, FLC and PI-FLC
- Study of fryze power theory
- Proposed instantaneous real-power theory
- Proposed sinusoidal extraction control strategy
- Synchronous reference frame theory
    - Conventional-SRF,
    - Proposed modified-SRF

This chapter describes different control strategies for active power line conditioner applications to extract the required reference or fundamental current components.

3.2. PI-controller

Active power line conditioner controller consists of reference current extraction method and PWM-VSI current control technique. The required reference current is extracted from the distorted line-current using the unit sine vector along with the PI-controller. The conventional PI-controller is used to estimate the required magnitude

of reference current, and to control the dc-link capacitor voltage of the inverter [43]. When the source supplies a non-linear or reactive load, it is expected to supply only the active fundamental component of the load current and the compensator supplies the harmonic / reactive component. Moreover, the compensator supplies the harmonic power, which manifests itself only on the reactive component of power. During transient conditions, the load changes are reflected in the dc-link capacitor voltage as an increase (or decrease) as capacitor absorbs (or delivers) the excess (or deficit) power [84]. This conservation of energy philosophy is used to obtain the reference current for compensator in this method. The perturbations in the capacitor voltage are related to the perturbations in the average power drawn by the non-linear load. This property is utilized which facilitates extracting compensator reference and maintains capacitor voltage.

The PI-control algorithm is computed based on sensing dc-link voltage, three-phase supply voltages and currents (neglecting sense load and compensation currents). The voltage source inverter switching pulses are generated through indirect PWM-current control technique that reduces sensors and complexity of the controller [85].

3.2.1. Unit sine vector

To generate the unit sine vector templates, the instantaneous supply voltages are sensed and given as

$$\begin{aligned} V_{sa} &= V_{sm}\sin(\omega t) \\ V_{sb} &= V_{sm}\sin(\omega t - 120^{o}) \\ V_{sc} &= V_{sm}\sin(\omega t + 120^{o}) \end{aligned} \tag{3.1}$$

where,

V_{sm} - peak value of the source voltage,

$\omega = 2\pi f$ -fundamental angular frequency.

For harmonic free unity power factor, three-phase supply currents are estimated using the unit sine vector templates, which are in phase with the supply voltages and its peak value. The unit sine vector templates are derived as [73]

$$\begin{aligned} u_{sa} &= V_{sa}/V_{sm} = \sin\omega t, \\ u_{sb} &= V_{sb}/V_{sm} = \sin(\omega t - 120^{0}) \ \ and \\ u_{sc} &= V_{sc}/V_{sm} = \sin(\omega t + 120^{0}) \end{aligned} \tag{3.2}$$

The amplitude of the unit sine vector template is unity in steady-state. In the transient condition, it will vary according to the load variation. The unit sine vector templates are multiplied with the peak-amplitude of the estimated reference current which is used to generate the required reference currents.

3.2.2. Reference current generation

The PI - controller is used to estimate the peak value of the reference current and to regulate the dc-link capacitor voltage. The output of the PI-controller is considered as the peak value of the estimated source or reference current. The estimated reference current is composed of two components; (i) fundamental active power component of the load current, (ii) loss component of the active power line conditioner (power loss due to switching losses in the VSI is also supplied by the source) [86-88]. Fig.3.1 shows the block diagram of PI-controller to estimate the required reference currents. To implement the PI-controller, the dc-link capacitor voltage is sensed and compared with the reference voltage. The comparison result of the voltage error $e(v) = V_{dc-ref} - V_{dc}$ at the sampling instant is used as input to the PI-controller.

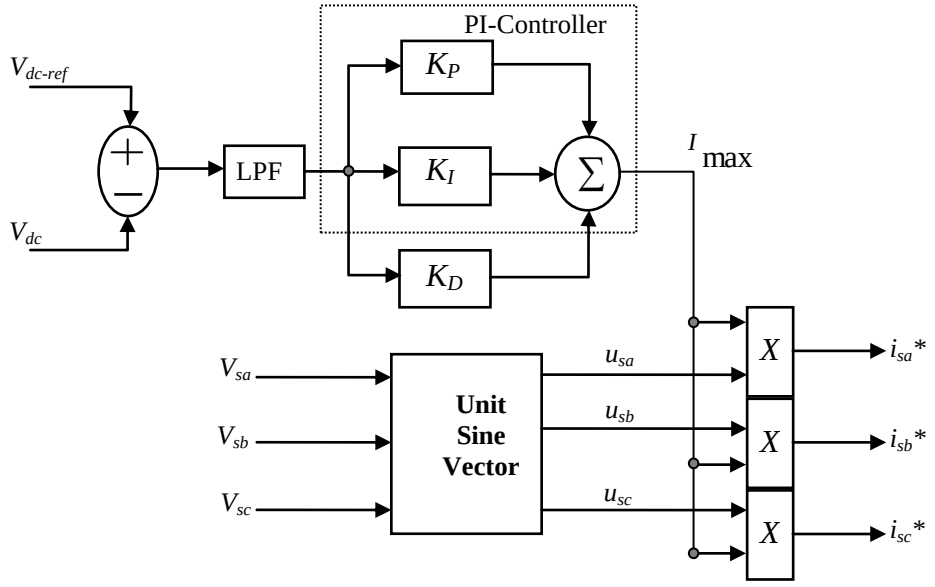


Fig.3.1 Block diagram of the PI / PID - controller

Low Pass Filter (LPF) is introduced to filter out higher order ripples as well as harmonic components and allows the fundamental components. The voltage error

signal passes through LPF which passes the fundamental signal. The PI-controller of the transfer function is defined as,

$$H(s) = K_P + K_I / s \tag{3.3}$$

where, the proportional and integral gains are chosen either heuristically or mathematically. The proportional gain determines the dynamic response of the dc-link capacitor voltage. The gain value is derived using the mathematical formula $K_P = 2\zeta\omega_{nv}C$. where, $\zeta = \sqrt{2}/2$ - damping factor, C - dc-link capacitor value, ω_{nv} - natural frequency, chosen as the supply fundamental frequency.

Similarly, the integral gain is derived using $K_I = C\omega_{nv}{}^2$ that determines settling time and eliminates steady state error in the DC- capacitor voltage.

This controller estimates the magnitude of peak reference current $I_{\max}$ by controlling the dc-link capacitor. This estimated magnitude of peak current multiplies with an output of unit sine vector templates, which generates the required reference currents.

$$\begin{aligned} i_{sa}{}^* &= I_{max} * u_{sa} = I_{max} \sin \omega t, \\ i_{sb}{}^* &= I_{max} * u_{sb} = I_{max} \sin(\omega t - 120^0) \ \ and \\ i_{sc}{}^* &= I_{max} * u_{sc} = I_{max} \sin(\omega t + 120^0) \end{aligned} \tag{3.4}$$

The reference current compared with the sensed actual current generate the VSI-switching pulses using indirect PWM-current controller.

3.3. PID-controller

Fig.3.1 shows the block diagram of the PID-control scheme of an active power line conditioner. The error $e(v) = V_{dc-ref} - V_{dc}$ in the n^{th} sampling instant is used as input to PID controller. The error signal passes through first order Butterworth design based LPF that suppresses high frequency components and allows only the fundamental component. The PID-controller is a linear combination of the Proportional (P) Integral (I) and Derivative (D) gains of the numerical values [84-88]. Its transfer function can be represented as

$$H(s) = K_P + \frac{K_I}{s} + K_D(s) \tag{3.5}$$

where,

K_P -proportional constant that determines the dynamic response of the dc-link voltage control

K_I -integration constant that determines the settling time

K_D -derivative of the error representing the trends

The controller is tuned with proper gain parameters to estimate the magnitude of peak reference current $I_{\max}$ and to control dc-link capacitor voltage of the inverter. This peak reference current $I_{\max}$ is multiplied with the unit-sine vector output and determines the required reference current.

Remarks: The PI and PID controller require a precise linear mathematical calculation of the system, which is difficult to obtain under parametric variations, non-linearity and load disturbances. Another drawback of the system is that the proportional, integral and derivative gains are chosen by heuristic or mathematical method which is difficult in optimizing the APLC performance. This drawback is overcome by using fuzzy logic controller.

3.4. Fuzzy logic controller

Fuzzy logic control is deduced from fuzzy set theory; which was introduced by Zadeh in 1965. In the fuzzy set theory concept, the transition is between membership and non-membership function. Therefore, limits or boundaries of fuzzy sets are undefined and ambiguous but useful in approximating systems design [89-94]. In order to implement the fuzzy logic control algorithm of an active power line conditioner in a closed loop, the dc-link capacitor voltage is sensed and compared with the desired reference value. The error signal $(e(v) = V_{dc-ref} - V_{dc})$ passes through a Butterworth low pass filter that allows only the fundamental component. The voltage error signal $e(n)$ and change of error signal $ce(n)$ are used as inputs for fuzzy processing as shown in Fig.3. 2. The output of the fuzzy logic controller estimates the magnitude of peak reference current $I_{\max}$.

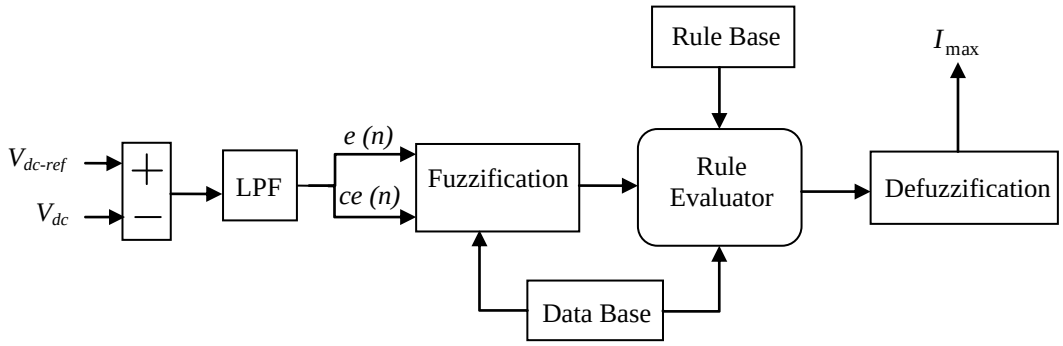


Fig.3.2 Schematic diagram of the fuzzy logic controller

The fuzzy logic controller is characterized as follows

- Seven fuzzy sets (NB, NM, NS, ZE, PS, PM, PB) for each input and output variables.
- Triangular membership function is used for the simplicity
- Implication using Mamdani-type min-operator
- Defuzzification using the centroid method.

Fuzzification: Fuzzy logic uses linguistic variables instead of numerical variables. In a closed loop control system, the error signal $e(n)$, change of error signal $ce(n)$ and output of peak reference current $I_{\max}$ are considered as membership functions. It can be labeled as Negative Big (NB), Negative Medium (NM), Negative Small (NS), Zero (ZE), Positive Small (PS), Positive Medium (PM), Positive Big (PB) as shown in Fig.3.3. Converting numerical variable (real number) into a linguistic variable (fuzzy number) is the process of fuzzification.

Rule Elevator: The fuzzy logic rules are linguistic variables in nature and a typical rule can be written as $R_k : If\ e(n)\ is\ A_i\ and\ ce(n)\ is\ B_i\ then\ I_{\max}\ is\ C_i$

where, $A_i, B_i\ and\ C_i$ are linguistic variables of $e(n), ce(n) and\ I_{\max}$ and it represents the degree of membership function. Let X be a collection of objects denoted generically by $\{x\}$; this could be discrete or continuous and X is defined as the universe. If an element in the universe, say x, is a member of fuzzy set A then the

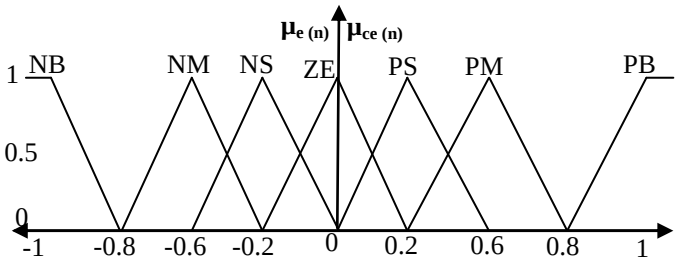
mapping is given as $A=[x,\mu(x)|x\in X]$. The basic fuzzy set operations required for evaluation of fuzzy rules are $AND(\cap)$, $OR\ \cup$ and $NOT(-)$.

The membership function $\mu_{A\cap B}$ of the intersection $A\cap B$ is point-wise defined for all $x\in X$ by $\mu_{A\cap B}=\min[\mu_A(X),\mu_B(x)]$

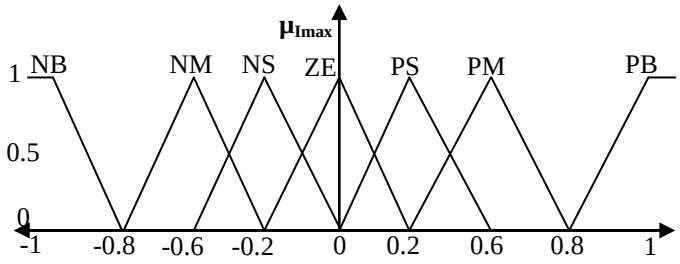
The membership function $\mu_{A\cup B}$ of the union $A\cup B$ is point-wise defined for all $x\in X$ by $\mu_{A\cup B}=\max[\mu_A(X),\mu_B(x)]$

The membership function μ_A of the complement of a fuzzy set A is point-wise defined for all $x\in X$ by $\mu_A=1-\mu_A(x)$

By definition of AND, evaluation of rule R_k results in a minimum of $\mu_{Ai(x)},\mu_{Bi(x)}$ allocated to $\mu_{Ci(x)}$.



(a) Input variables "*e (n)* and *ce (n)*"



(b) Output variable "I_{max}"

Fig.3.3 Membership functions (a) the input variables e (n), ce (n) and (b) output variable I_{max}

Defuzzification: The rules of fuzzy logic produce the set of modified control output in a linguistic variable. The defuzzification module converts these linguistic variables into a crisp value (real number) according to real time applications. The different

methods of defuzzification available are Bisector, Centroid, Middle of Maximum (MOM), Smallest of Maximum (SOM) and Largest of Maximum (LOM), etc., however, the selection of method is a compromise between accuracy and computational intensity (that influences hardware requirement for real time application) . The centroid (or center of gravity) method is used for simplicity and accuracy. The linguistic output variable from the rule evaluator and definition of output membership are used to calculate the hidden area. Finally, crisp output is obtained by using $output = \sum A_i * x_i / \sum A_i$

Database: Database stores the definition of the membership function required by fuzzifier and defuzzifier. Storage format is a compromise between available memory and processor of the digital controller chip.

Rule Base: The Rule base stores the linguistic (fuzzy) control rules required by the rule evaluator (decision making logic), the 49-rules used are presented in Table 3.1.

Table 3.1Rule base table using 49-rules

e(n) / *ce(n)*	*NB*	*NM*	*NS*	*ZE*	*PS*	*PM*	*PB*
NB	NB	NB	NB	NB	NM	NS	ZE
NM	NB	NB	NB	NM	NS	ZE	PS
NS	NB	NB	NM	NS	ZE	PS	PM
ZE	NB	NM	NS	ZE	PS	PM	PB
PS	NM	NS	ZE	PS	PM	PB	PB
PM	NS	ZE	PS	PM	PB	PB	PB
PB	ZE	PS	PM	PB	PB	PB	PB

The output of the fuzzy controller estimates the magnitude of peak reference current $I_{\max}$. These estimated magnitude of peak-current multiplied with an output of unit sine vector determines the reference currents.

Remark: Recently, fuzzy logic controller is used in active power line conditioner application. The advantages of fuzzy logic controller over the conventional controllers are: (i) does not require an accurate numerical calculation, (ii) work with imprecise inputs, (iii) handle nonlinearity, (iv) more robust than conventional PI and PID controllers. To improve the performance of PI-controller, it is combined with the FLC and applied in the active power line conditioner system.

3.5. PI-fuzzy logic controller

Fig.3.4 shows the block diagram of the PI-controller in conjunction with the fuzzy logic controller scheme for active power line conditioner. The PI-controller output contains certain ripples, so it needs another processing unit to reduce this ripple. The fuzzy logic controller is connected together with the PI-controller for reducing these ripples [95]. The PI controller output error is used as inputs to the fuzzy processing and output $I_{\max}$ is derived.

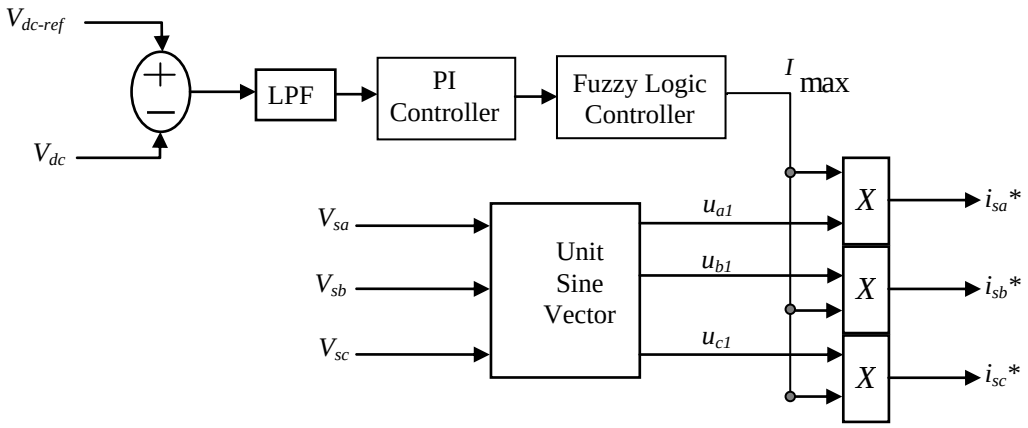


Fig.3.4 Block diagram of the PI with fuzzy logic Controller

The rule base stores the linguistic control rules required by the rule evaluator (decision making logic). The 25-rules used in this controller are given in Table 3.2. Our observation says that using 25 rules we are able to simplify the design further without sacrificing much accuracy.

Table 3.2 Rule base table using 25-rules

e(n) / *ce(n)*	*NM*	*NS*	*ZE*	*PS*	*PM*
NM	NM	NM	NM	NS	ZE
NS	NM	NM	NS	ZE	PS
ZE	NM	NS	ZE	PS	PM
PS	NS	ZE	PS	PM	PM
PM	ZE	PS	PM	PM	PM

This estimated magnitude of peak-current multiplied with an output of unit sine vector determines the reference currents. The reference currents are compared with actual source currents to generate VSI-switching pulses using PWM-current controller.

Remarks: PI / PID / FLC with indirect PWM-current control algorithm are developed by sensing dc-voltage, three-phase source voltages and currents (neglecting to sense load currents and compensation currents). It reduces the sensors and complexity of the control algorithm. The PI and FLC method is combined for efficient active power line conditioning. This controller handles nonlinearity, and it is more robust. The PI-FLC facilitates reduction of ripples in dc-link capacitor of the PWM-inverter.

3.6. Fryze power theory

Fryze power theory method presents a minimum rms value to draw the same three phase average active power from the source as the original load current. The fryze power theory guarantees linearity between the supply voltage and compensated current [32-33] [96-99]. Fig.3.5 shows the block diagram of the control circuit for implementation of the generalized fryze current control strategy.

The instantaneous equivalent conductance (G_e) is calculated from the three phase instantaneous active power theory $(p_{3\varphi})$

$$\begin{aligned} p_{3\varphi}(t) &= v_{sa}(t)i_{sa}(t) + v_{sb}(t)i_{sb}(t) + v_{sc}(t)i_{sc}(t) \\ &= p_{sa}(t) + p_{sb}(t) + p_{sc}(t) \end{aligned} \tag{3.6}$$

Moreover the root mean square aggregate voltage is derived from the instantaneous value of phase voltages, this is written as

$$V = \sqrt{v_{sa}^{2}(t) + v_{sb}^{2}(t) + v_{sc}^{2}(t)} \tag{3.7}$$

The instantaneous conductance or admittance (G_e) is calculated from the three phase instantaneous phase voltages v_{sa}, v_{sb} *and* v_{sc} and load currents i_{La}, i_{Lb} *and* i_{Lc}. It is derived by the following equation

$$G_e = \frac{v_{sa} i_{La} + v_{sb} i_{Lb} + v_{sc} i_{Lc}}{v_{sa}^{2} + v_{sb}^{2} + v_{sc}^{2}} \tag{3.8}$$

The conductance (G_e) passes through the Butterworth design based low pass filter to calculate the average conductance $(\overline{G_e})$. The LPF cutoff frequency is 50 Hz which allows only the fundamental component for the active current calculation. The instantaneous active components of the load currents are directly obtained by multiplying $\overline{G_e} + G_{loss}$ by the phase voltages.

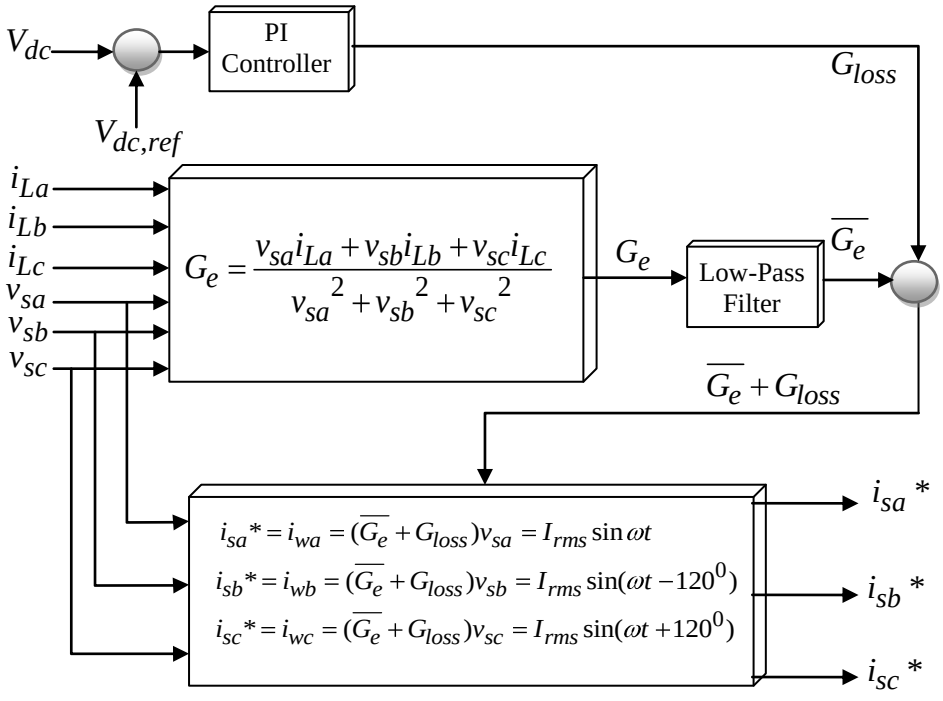


Fig.3.5 Block diagram of the generalized fryze power theory algorithm

The control strategy follows the convention of current direction assuming shunt active power line conditioner draws the inverse of the non-active current of the load.

An extra active component of current is added, in order to draw a small amount of active power to compensate for switching loss and conducting loss in the shunt active power line conditioner, which tends to discharge the dc-link capacitor voltage. This is realized by the addition of the signal G_{loss} and the average conductance $\overline{G_e}$. The desired reference source currents are calculated from the active component currents, are written as

$$\begin{aligned} i_{sa}{}^* &= i_{wa} = (\overline{G_e} + G_{loss})v_{sa} = I_{rms}\sin\omega t \\ i_{sb}{}^* &= i_{wb} = (\overline{G_e} + G_{loss})v_{sb} = I_{rms}\sin(\omega t - 120^0) \\ i_{sc}{}^* &= i_{wc} = (\overline{G_e} + G_{loss})v_{sc} = I_{rms}\sin(\omega t + 120^0) \end{aligned} \quad (3.9)$$

where,

I_{rms} - rms line current.

The reference current is compared with actual source current and generates PWM-VSI gate drive switching pulses. The control strategy indicates the shunt active power line conditioner should draw the inverse of the non-active current of the load. The results indicate the compensated currents are proportional to the corresponding phase voltage.

Remarks: The generalized fryze power theory method reduces the reference current calculation, since it works directly with the *abc*-phase voltage and line currents. The elimination of the Clarke transformation makes control strategy relatively simple to implement. However, this theory has no consistent expression to calculate the three-phase instantaneous reactive-power to compensate for the reactive-power of the load.

3.7. Proposed instantaneous real-power theory

The proposed instantaneous real-power (p) theory is derived from the conventional $p-q$ theory or instantaneous reactive power theory concept [32] [34]. It operates in steady-state or transient-state as well as in generic voltage and current power systems which control the active power line conditioners in real-time. Fig.3.6 shows the block diagram of the reference current extraction scheme using instantaneous real-power theory.

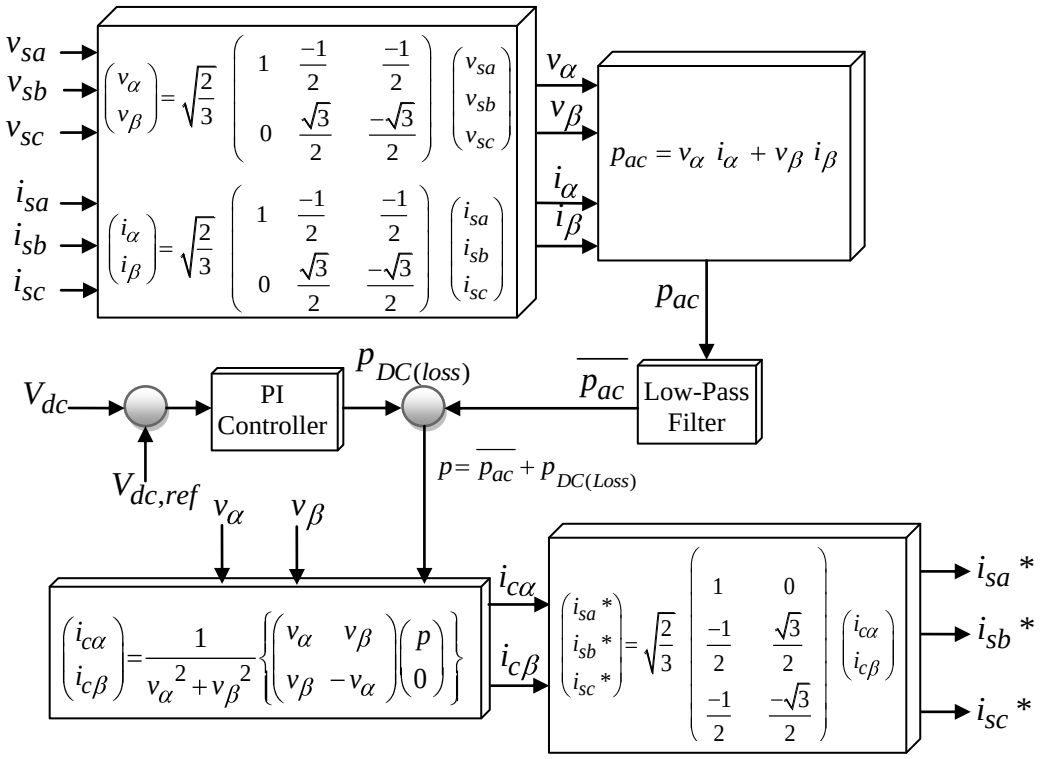


Fig.3.6 Block diagram of the instantaneous real-power theory

The $p-q$ theory performs a Clarke transformation of a stationary system of coordinates $a-b-c$ to an orthogonal reference system of coordinates $\alpha-\beta$. The $a-b-c$ coordinate axis are fixed on the same plane, phase shifted by 120^0. The instantaneous space vectors voltage v_{sa} and current i_{sa} set on a-axis, v_{sb} *and* i_{sb} on b-axis, and v_{sc} *and* i_{sc} on c-axis. The instantaneous space vector voltage(s) is transformed into the $\alpha-\beta$ coordinate voltage(s) by the Clarke transformation as follows

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} \tag{3.10}$$

Similarly, the instantaneous space vector current(s) is transformed into the $\alpha-\beta$ coordinate current(s) by Clarke transformation that is given as

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} \tag{3.11}$$

The orthogonal coordinates of voltage v_α and current i_α on α-axis, and v_β *and* i_β on β-axis respectively. Let the instantaneous real-power be calculated from the α-axis and β-axis of the current and voltage. These are given by the conventional definition of real power as follows [100-104]

$$p_{ac} = v_\alpha \, i_\alpha + v_\beta \, i_\beta \tag{3.12}$$

This instantaneous real power p_{ac} passes through Butterworth design based 50 Hz low pass filter for eliminating the higher order harmonic components, and it allows passing the fundamental components only. The output of the LPF component is considered as real power losses and it is denoted as $\overline{p_{ac}}$. The dc-power loss is calculated from the dc-capacitance voltage of the voltage source inverter using the PI-controller. The PI-controller determines the dynamic response and settling time in the dc-link capacitor voltage and dc-power losses. The dc-power losses are written as

$$p_{dc(loss)} = \left[V_{dc,ref} - V_{dc} \right] \left[K_P + \frac{K_I}{s} \right] \tag{3.13}$$

The instantaneous real-power p is calculated from the real power loss $\overline{p_{ac}}$ and the dc power loss $p_{dc(Loss)}$, it is calculated as

$$p = \overline{p_{ac}} + p_{dc(Loss)} \tag{3.14}$$

The instantaneous current on the $\alpha - \beta$ coordinates of $i_{c\alpha}$ *and* $i_{c\beta}$ are divided into two kinds of instantaneous current components; one is real-power losses and the other is reactive-power losses, but this controller computes only the real-power losses. The $\alpha - \beta$ coordinate currents $i_{c\alpha}$ *and* $i_{c\beta}$ are calculated from v_α *and* v_β voltages with instantaneous real power p, and the reactive power q is considered as zero. In case of $p - q$ theory, it uses both real-power and reactive-power to estimate the $\alpha - \beta$ current components. However, the reactive-power does not contribute to energy transfer between the source and the load at any time. This proposed approach reduces the

calculations and provides better performance than conventional methods [105]; the $\alpha-\beta$ coordinate currents are calculated as

$$\begin{bmatrix} i_{c\alpha} \\ i_{c\beta} \end{bmatrix} = \frac{1}{v_\alpha{}^2 + v_\beta{}^2} \left\{ \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} p \\ 0 \end{bmatrix} \right\} \tag{3.15}$$

From the above equation, we calculate the orthogonal coordinate active power currents. The α -axis of the instantaneous active current is written as

$$i_{c\alpha p} = \frac{v_\alpha p}{v_\alpha{}^2 + v_\beta{}^2} \tag{3.16}$$

The β -axis of the instantaneous active current is written as

$$i_{c\beta p} = \frac{v_\beta p}{v_\alpha{}^2 + v_\beta{}^2} \tag{3.17}$$

Let the instantaneous powers in the α -axis and the β -axis is represented as $p_\alpha \; and \; p_\beta$ respectively. They are given by the definition of real-power as follows

$$p(t) = v_{\alpha p}(t)\; i_{\alpha p}(t) + v_{\beta p}(t)\; i_{\beta p}(t) \tag{3.18}$$

From the above equation (3.18), substituting the orthogonal coordinates α -axis active power and β -axis active power, calculate the real-power as follows

$$p(t) = v_\alpha(t) \left[\frac{v_\alpha p}{v_\alpha{}^2 + v_\beta{}^2} \right] + v_\beta(t) \left[\frac{v_\beta p}{v_\alpha{}^2 + v_\beta{}^2} \right] \tag{3.19}$$

The ac component of the instantaneous power $p(t)$ is related to the harmonic currents. The instantaneous real-power extract the reference current required to compensate the current harmonics and reactive-power. The references of the compensating currents $i_{sa}{}^*, i_{sb}{}^* \; and \; i_{sc}{}^*$ are calculated instantaneously without any time delay by using the instantaneous $\alpha-\beta$ coordinate currents.

$$\begin{bmatrix} i_{sa}{}^* \\ i_{sb}{}^* \\ i_{sc}{}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ \frac{-1}{2} & \frac{\sqrt{3}}{2} \\ \frac{-1}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{c\alpha} \\ i_{c\beta} \end{bmatrix} \tag{3.20}$$

The small amount of real power is taken care of through the controller by modulating fundamental component of reference current. The objective of this algorithm is to compensate all undesirable power components. When the power

system voltages are balanced and sinusoidal, it results simultaneously in constant instantaneous power and balanced sinusoidal currents in the ac-power supply.

Remarks: The proposed instantaneous real-power theory is derived from the conventional $p-q$ theory concept. The $\alpha-\beta$ coordinate currents are calculated from v_α *and* v_β with instantaneous real power p, and the reactive power q is considered as zero. This approach reduces the calculations compared to conventional methods.

3.8. Proposed sinusoidal extraction control strategy

The proposed sinusoidal extraction control strategy is used to extract the reference current from the distorted line current.

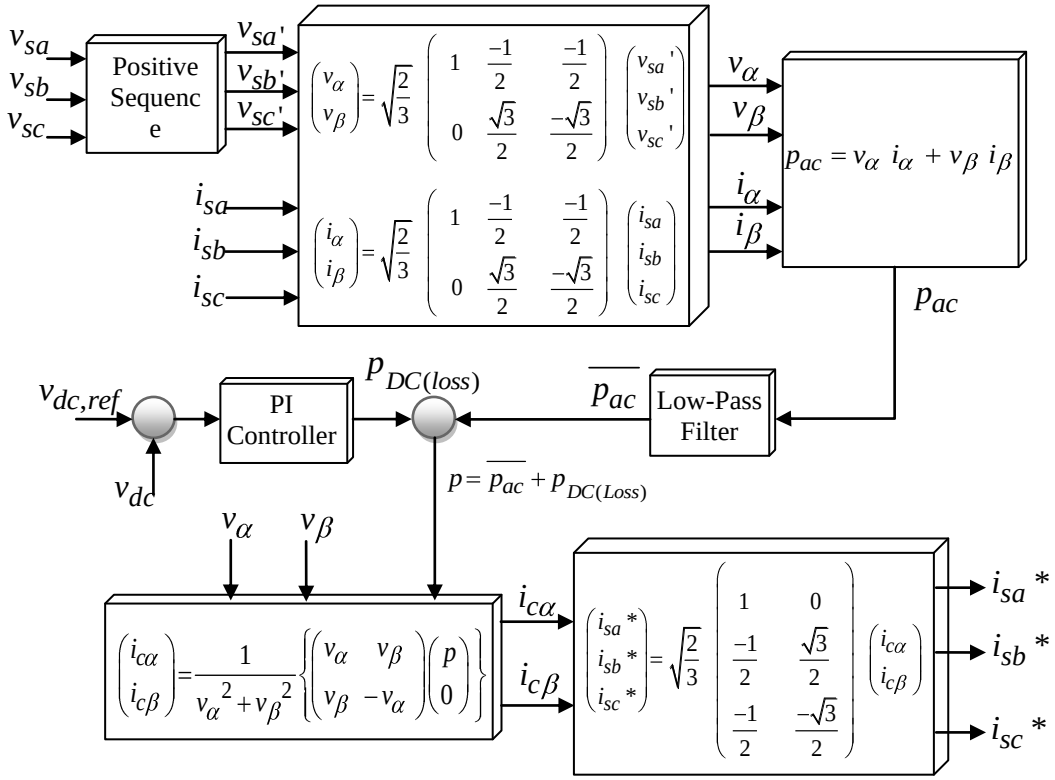


Fig.3.7 Block diagram of the sinusoidal extraction controller

Fig.3.7 shows the block diagram of the sinusoidal extraction control strategy. It has two important parts; (i) Positive sequence voltage detector to generate the balanced

sinusoidal voltages v_{sa}', v_{sb}' *and* v_{sc}' from the unbalanced or unregulated supply voltages v_{sa}, v_{sb} *and* v_{sc} (ii) Instantaneous real-power theory to extract the reference currents from the distorted line currents [106].

3.8.1. Positive sequence voltage detector

Fig.3.8 shows the block diagram of the positive-sequence voltage detector. The unbalanced voltages v_{sa}, v_{sb} *and* v_{sc} are transformed into the $\alpha - \beta$ coordinates to determine v_α *and* v_β using Clarke transformation, using equation (3.10).

The v_α *and* v_β components are used to meet with auxiliary currents i_α' *and* i_β' (produced from the PLL-synchronizing circuit) to calculate the auxiliary powers p' *and* q'. The auxiliary real and reactive power is computed as follows [32]

$$\begin{aligned} p' &= v_\alpha\ i_\alpha' + v_\beta\ i_\beta' \\ q' &= v_\beta\ i_\alpha' + v_\alpha\ i_\beta' \end{aligned} \tag{3.21}$$

The auxiliary powers p' *and* q' passed through first order Butterworth design based 50 Hz low pass filter for eliminating the higher order components and passes the fundamental components. The LPF is obtained from the average real and reactive power $\bar{p}'$ *and* $\bar{q}'$. The instantaneous voltages v_α' *and* v_β' which correspond to time functions of the fundamental positive sequence voltage detector of the system is derived as

$$\begin{bmatrix} v_\alpha' \\ v_\beta' \end{bmatrix} = \frac{1}{{i_\alpha'}^2 + {i_\beta'}^2} \left\{ \begin{bmatrix} i_\alpha' & i_\beta' \\ i_\beta' & -i_\alpha' \end{bmatrix} \begin{bmatrix} \bar{p}' \\ \bar{q}' \end{bmatrix} \right\} \tag{3.22}$$

The instantaneous voltages v_{sa}', v_{sb}' *and* v_{sc}' is calculated from the $\alpha - \beta$ coordinate voltages v_α' *and* v_β' by applying the inverse Clarke transformation; this is derived as

$$\begin{bmatrix} v_{sa}' \\ v_{sb}' \\ v_{sc}' \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ \frac{-1}{2} & \frac{\sqrt{3}}{2} \\ \frac{-1}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_\alpha' \\ v_\beta' \end{bmatrix} \tag{3.23}$$

The positive sequence voltage detector provides good dynamic response and accuracy even under distorted or unbalanced conditions. This controller makes the shunt active power line conditioner to compensate load currents, so that the active

portion of the fundamental positive sequence component produces average real-power, which is supplied by the source. The PLL-circuit must provide auxiliary currents to sinusoidal functions at the fundamental frequency. The next section describes the function of the PLL - circuit.

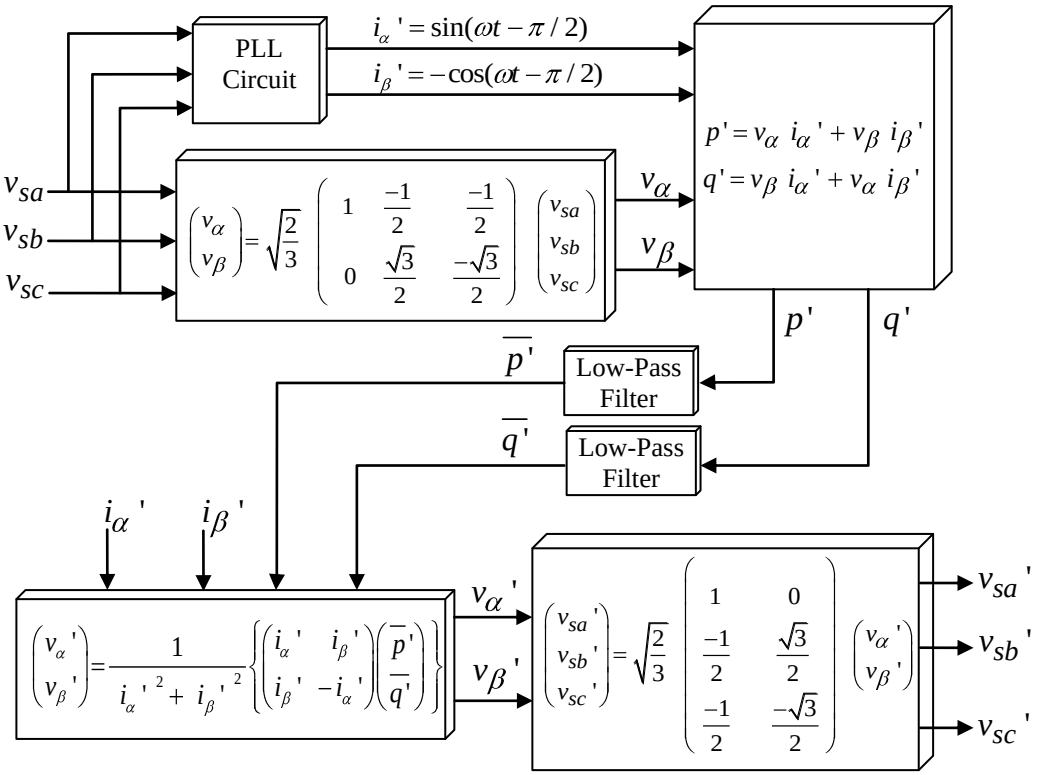


Fig.3.8 Block diagram of the positive sequence voltage detector

3.8.1.1. Phase locked loop circuit

The PLL-circuit work properly under distorted and unbalanced supply voltage. The block diagram of the PLL-circuit is shown in Fig.3.9. The inputs are $v_{ab} = v_a - v_b; v_{bc} = v_b - v_c$. The outputs of the PLL circuit are i_α' *and* i_β'. The algorithm is based on the three-phase instantaneous active power expression $p_{3\varphi} = v_a i_a + v_b i_b + v_c i_c$. The current feedback signals, $i_a(\omega t) = \sin(\omega t)$ and $i_c(\omega t) = \sin(\omega t + 2\pi/3)$ are developed by the PLL-circuit, using the time integral of output ω of the PI-Controller [107]. The PLL-synchronizing circuit reaches stable point of operation when the input $p_{3\varphi}$ of the PI-controller has a zero average value

($p_{3\varphi} = 0$). It minimizes the low-frequency oscillating portions in three phase voltages. Once the circuit is stabilized, the average value of $p_{3\varphi}$ is zero and the phase angle of the system voltage reaches the fundamental frequency. Under this condition, the auxiliary currents become orthogonal to the fundamental phase voltage component. The PLL synchronizing output currents are defined as

$$\begin{aligned} i_\alpha' &= \sin(\omega t - \pi/2) \\ i_\beta' &= -\cos(\omega t - \pi/2) \end{aligned} \tag{3.24}$$

The PLL synchronizing output currents are used to determine the instantaneous auxiliary power, thus p' *and* q' are calculated.

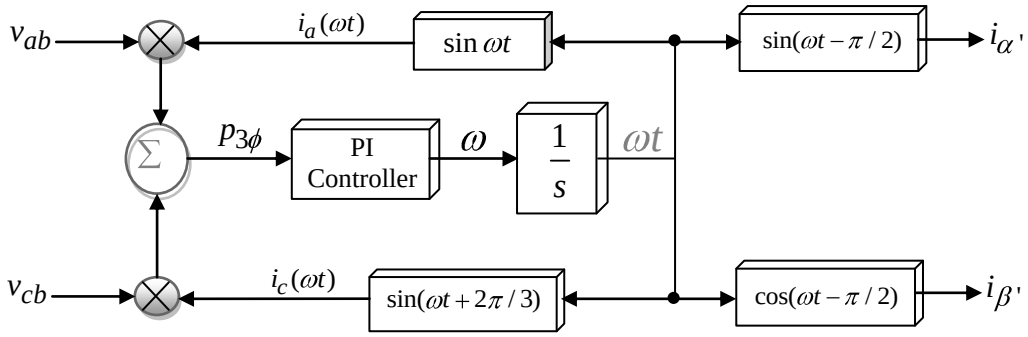


Fig.3.9 PLL-circuit

3.8.2. Instantaneous real-power theory

The instantaneous $a-b-c$ coordinate sinusoidal voltage v_a', v_b' *and* v_c' are transformed into the $\alpha-\beta$ coordinate voltages by using the Clarke transformation equation (3.10)

Similarly, the instantaneous source current i_{sa}, i_{sb} *and* i_{sc} transformed into the $\alpha-\beta$ coordinate current i_α *and* i_β by using Clarke transformation equation (3.11)

The voltage v_α and current i_α are on the α -axis and v_β *and* i_β are on the β -axis. The instantaneous $i_{c\alpha}$ *and* $i_{c\beta}$ currents are calculated from the v_α *and* v_β voltages with instantaneous real-power p , assuming the reactive power q as a zero. This approach

reduces the calculations [105], the $\alpha-\beta$ coordinate currents can be calculated using equation (3.15).

The references of the compensating currents are calculated instantaneously without any time delay by using the instantaneous $\alpha-\beta$ coordinate currents. The desired reference current is derived from the inverse Clarke transformation equation (3.20).

The control strategy indicates that shunt APLC will ensure that the source current sinusoidal.

Remarks: The proposed sinusoidal extraction controller works under unbalanced or distorted supply voltages. This control strategy makes the active power line conditioner compensate the current of nonlinear load and force the compensated source current to become sinusoidal as well as balanced. However, this controller requires large computation time to compare constant instantaneous power control strategy.

3.9. Synchronous reference frame theory

The time domain based synchronous reference frame theory is utilized to extract the reference current from the distorted line current. The SRF control strategy operates in steady-state as well as in dynamic-state perfectly to control the active power line conditioner in real-time application. Another important characteristic of SRF theory is the simplicity of the calculations, which involves only algebraic calculation [108-118]. There are two-types of SRF control methods derived; (i) conventional-SRF and (ii) proposed modified-SRF

3.9.1. Conventional-SRF

The basic structure of SRF method consists of PLL-circuit for vector orientation and PI-controller for dc-link capacitor voltage regulator. Fig.3.10 shows the block diagram of the conventional-SRF method. The three-phase load currents i_{La}, i_{Lb}, i_{Lc} in stationary coordinates are converted into the two-phase direct axis (d) and quadratic axis (q) rotating coordinates currents $i_d - i_q$ as

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \sin\theta & \sin(\theta-\frac{2\pi}{3}) & \sin(\theta+\frac{2\pi}{3}) \\ \cos\theta & \cos(\theta-\frac{2\pi}{3}) & \cos(\theta+\frac{2\pi}{3}) \end{bmatrix}\begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{3.25}$$

The reference frame is rotating synchronously with fundamental currents. Therefore, time variant currents with fundamental frequencies are constant after transformation. Thus, currents are separating simultaneously (to dc and ac components). The d -axis current components are used for harmonic eliminations and reactive-power compensations. The $d-q$ transformation output signals depend on the load current and the performance of the phase locked loop [110-111].

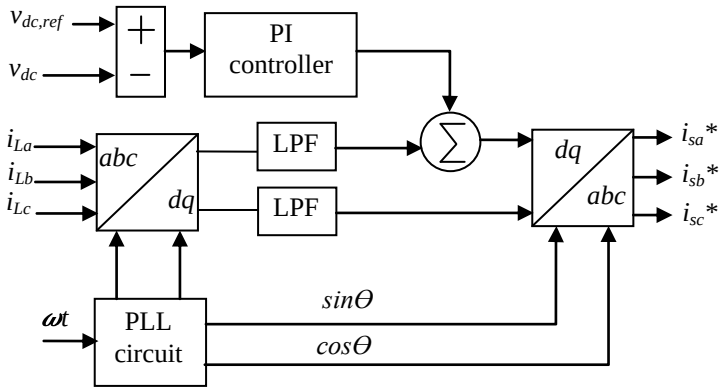


Fig.3.10 Block diagram of the conventional-SRF method

The PLL-circuit is providing the vectorized fundamental frequency ($\sin\theta$ and $\cos\theta$) for synchronization. The $i_d - i_q$ currents are passed through a low pass filter to filter the higher order harmonic components and permit fundamental frequency components. The PI-controller is used to eliminate the steady state error of the dc-component and maintains the dc-capacitance voltage of the inverter. The proportional and integral gains determine the dynamic response and settling time of the dc-voltage respectively [113]. To minimize the inverter losses by maintaining the dc-voltage constant or within limits, the required current is added to the positive sequence fundamental frequency active component of the $d-q$ current. The desired reference current ($a-b-c$ stationary frame) is calculated from $i_d - i_q$ rotating frame using inverse transformation,

$$\begin{bmatrix} i_{sa}* \\ i_{sb}* \\ i_{sc}* \end{bmatrix} = \begin{bmatrix} \sin\theta & \cos\theta \\ \sin(\theta - 2\pi/3) & \cos(\theta - 2\pi/3) \\ \sin(\theta + 2\pi/3) & \cos(\theta + 2\pi/3) \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \quad (3.26)$$

The extracted reference current is compared with actual currents and hence generates the required switching pulses for the inverter using indirect PWM-current controller. However, the conventional-SRF control strategy requires a PLL-circuit based on the supply voltage for vector orientation. But the design of a high performance PLL-circuit is difficult, when various non-idealities like multiple zero crossing are occurring in the supply voltage. A simple and efficient method is used to calculate the unit vector, which is incorporated with the modified- SRF method.

3.9.2. Proposed modified-SRF

The block diagram of modified-SRF structure is shown in Fig.3.11. The modified-SRF method consist of simplified unit vector generation for vector orientation, dc-link capacitor voltage regulator and stationary-rotating synchronous frames to extract the reference current.

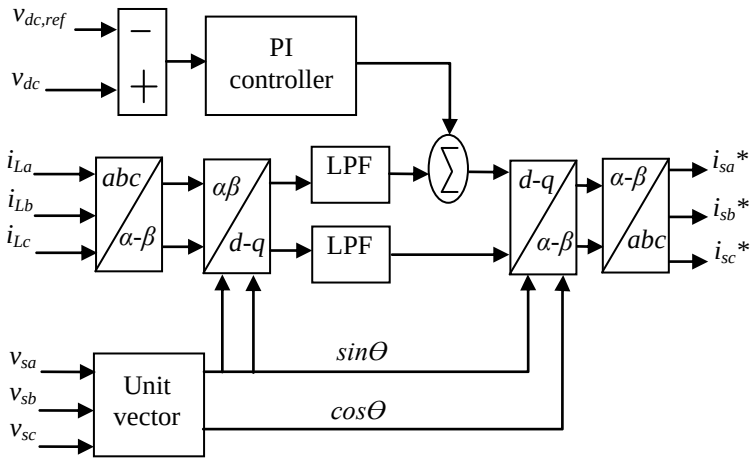


Fig.3.11 Block diagram of the modified - SRF method

3.9.2.1. Unit vector generation

The simple and efficient unit vector generator is used for vector orientation. Fig.3.12 shows the block diagram of a unit vector generation method. To generate the synchronization vector the instantaneous supply voltages are sensed and computed.

The instantaneous three-phase source voltages are transformed into the two-phase stationary $\alpha-\beta$ voltages using Clarke transformation given in equation (3.10).

Transforming equation (3.1) to $\alpha-\beta$ plane using equation (3.10) and simplifying,

$$\begin{aligned} v_{s\alpha} &= \frac{3}{2} v_m \sin(\omega t) \\ v_{s\beta} &= -\frac{3}{2} v_m \cos(\omega t) \end{aligned} \tag{3.27}$$

The $\alpha-\beta$ voltages are filtered using first order digital low pass filter whose frequency is ω (at fundamental frequency). After filtering, the percentage of h^{th} order harmonics of the sensed supply voltage are reduced by a factor of $\sqrt{2/(h^2+1)}$. It cancels the higher order harmonics, notches and high frequency noise. The estimated magnitude of the space vector generated is as follows [115]

$$\vec{V} = \overrightarrow{V_{\alpha\beta}} = v_{s\alpha} + j v_{s\beta} = \sqrt{{v_{s\alpha}}^2 + {v_{s\beta}}^2} \tag{3.28}$$

From the derivation in equation (3.28), it is evident that the unit vectors can be generated by transforming the supply voltage to $\alpha-\beta$ plane and dividing the $\alpha-\beta$ components by the magnitude of the space vector. Hence, the unit vector generation is defined as

$$\begin{aligned} \cos\theta &= \frac{v_\alpha}{\sqrt{{v_{s\alpha}}^2 + {v_{s\beta}}^2}} = \frac{(3/2) v_m \sin(\omega t)}{(3/2) v_m} = \sin(\omega t) \\ \sin\theta &= \frac{v_\beta}{\sqrt{{v_{s\alpha}}^2 + {v_{s\beta}}^2}} = \frac{-(3/2) v_m \cos(\omega t)}{(3/2) v_m} = -\cos(\omega t) \end{aligned} \tag{3.29}$$

This unit vector generation method results in elimination of supply harmonics, high frequency noise and notches in the distribution of supply voltages.

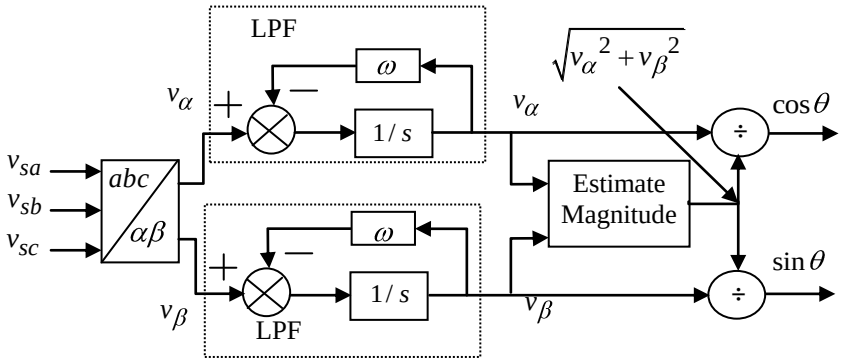


Fig.3.12 Block diagram of the unit vector generation

3.9.2.2. dc-voltage regulator

The PI-regulator is used to eliminate the steady state error of the dc-component and maintains the dc-link capacitor voltage constant. The dc-current component is derived as

$$i_{dc} = C\frac{dv_{dc}}{dt} \tag{3.30}$$

In order to regulate the dc-voltage v_{dc} at a fixed value, the error $\overline{v_{dc}} = v_{dc}{}^{*} - v_{dc}$ is passed through the PI-regulator [38]

$$i_{dc} = K_P\overline{v_{dc}} + K_I\int\overline{v_{dc}}dt \tag{3.31}$$

The $d-q$ co-ordinates provide $v_d = \sqrt{(3/2)}\ V$ *and* $v_q = 0$. From these statements, the dc-component of the reference current is approximated by

$$i_{dc} = \sqrt{\frac{2}{3}}\frac{v_{dc}}{V}i_{dc} \tag{3.32}$$

In order to maintain the dc-voltage, the d-axis harmonic current $(i_d{}^{*} = i_d{}^{*} + i_{dc})$ is added with the dc-component of the reference current, since the q-axis component current does not contribute to the active power for maintaining the dc-voltage.

3.9.2.3. Reference current extraction

The instantaneous three-phase load currents i_{La}, i_{Lb}, i_{Lc} are transformed into the stationary coordinate currents $i_\alpha - i_\beta$ by using Clarke transformation equation (3.11).

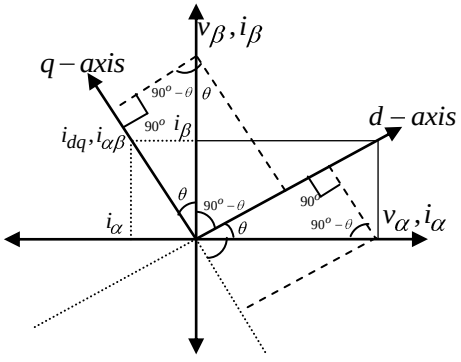


Fig.3.13 Voltage and current components in stationary and rotating d-q frame

Fig.3.13 shows the current components in stationary and rotating synchronous reference frames. The $\alpha-\beta$ components of the current quantities are transformed to the rotating synchronous $d-q$ reference frame by park equations

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} \tag{3.33}$$

The $d-q$ transformed output signals depend on the load current and the performance of the unit vector generation. The $i_d - i_q$ harmonic currents are passed through the LPF to eliminate the higher order ripples. The LPF passes the active current of fundamental frequency component $i_d{}^*$ and reactive-power component $i_q{}^*$ required by the load [118]. The algorithm is further developed to calculate the desired reference current signals; hence, the $d-q$ rotating frame is converted back into $\alpha-\beta$ stationary frame.

$$\begin{bmatrix} i_\alpha{}^* \\ i_\beta{}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_d{}^* \\ i_q{}^* \end{bmatrix} \tag{3.34}$$

The inverse transformation from $d-q$ rotating frame into $a-b-c$–stationary frame is achieved by the following equation

$$\begin{bmatrix} i_{sa}{}^* \\ i_{sb}{}^* \\ i_{sc}{}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_\alpha{}^* \\ i_\beta{}^* \end{bmatrix} \tag{3.35}$$

The extracted reference currents are compared with actual currents and generate switching pulses to drive the voltage source inverter by using PWM-current controller.

Remarks: The conventional-SRF controller requires PLL-circuit for vector orientation. But the design of a high performance PLL-circuit is difficult and this drawback is rectified by the proposed modified-SRF method. It uses a simple unit vector for vector orientation and $\alpha-\beta$ stationery frame transformation for high performance control strategy. The modified-SRF provides better performance than conventional method in terms of dc-voltage regulation, harmonic current elimination and reactive-power compensation.

3.10. Conclusions

The time-domain based reference current extraction methods are explained and derived for active power line conditioner. The PI / PID / Fuzzy / PI-Fuzzy logic control methods have been used to estimate the required reference current by controlling the dc-voltage of the PWM-inverter. PI / PID / FLC with indirect PWM-current control algorithms are constructed based on sensing dc-voltage, three-phase source voltages and current. The PI and FLC method is combined for efficient active power line conditioning. This controller handles nonlinearity, and is more robust than other methods.

The proposed instantaneous real-power theory is derived from the conventional $p-q$ theory. The algorithm is developed from sensing dc-voltage, three-phase source voltages and currents (no need to sense load current and compensation filter current). It reduces the number of sensors and hence decreasing the complexity of the controller. The instantaneous $\alpha-\beta$ current components are calculated from the $v_\alpha - v_\beta$ with instantaneous real power losses, and the reactive-power is considered as zero. This approach reduces the calculations and provides better performance than conventional methods. It operates in steady-state / transient-state as well as for generic voltage and current power systems which control the active power line conditioner in real-time.

The proposed sinusoidal extraction controller works under unbalanced or distorted supply voltages. This control strategy makes the active power line conditioner compensate the current of a nonlinear load to force the compensated source current to become sinusoidal and balanced. However, this controller requires large computation time compared to instantaneous power control strategy.

The fryze power theory does not use the Clarke transformation, which makes the control strategy very simple with less computation time. However, this theory has no consistent expression to calculate the three-phase instantaneous reactive-power, to compensate for the reactive-power of the load.

The conventional and proposed modified-synchronous reference frame method has facilitated in extracting the required reference currents. The modified-SRF uses a simple and efficient unit vector generator instead of PLL-circuit for vector orientation

The various reference current extraction methods (PI / PID / FLC / PI-FLC, fryze power theory, proposed instantaneous real-power theory, proposed sinusoidal extraction controller, and proposed modified-SRF) are investigated using Matlab tool.

CHAPTER 4

PWM-VSI CURRENT CONTROL TECHNIQUES

4.1. Introduction

Most of the current control techniques are used in active power line conditioner based on PWM- current control strategy. Various PWM-current control strategies are applied for active power line conditioner applications [51-59]. However, the high performance of the current-control is a difficult task in most practical cases, the inverter load is unidentified and changeable [119-120]. It is already explained that APLC must supply the anti-harmonics as per the load requirement. We are using a VSI with current control within the inverter. It is important that this system supplies current in response to the reference current and the tracking must be as clean and as close as possible. Therefore, current control techniques should follow the below mentioned properties for efficient performance of the active power line conditioner.

- Better utilization of the voltage source inverter, for producing high current in a given non-linear load.
- Low static and dynamic current-control errors (difference between the reference current and actual currents is less).
- Wide linear modulation range.
- Low amplitudes of lower order harmonics in output voltage to minimize the harmonics in output current.
- Lower switching losses in the power transistor (voltage source inverter) switches
- Easy implementation and less computation time.

In this chapter, the following indirect PWM-current control techniques are derived and implemented for active power line conditioner.

- Triangular Carrier Current Controller (TCCC)
- Triangular Periodical Current Controller (TPCC)
- Space Vector Modulation (SVM) Controller
- Fixed-HCC

    - Two-level HCC
    - Three-level HCC
- Adaptive-HCC and
- Adaptive-fuzzy-HCC

4.2. Current control technique

In the PWM-current control technique, the three-phase error signals obtained from the comparison of reference currents and sensed actual currents generate the required PWM-switching pulses for the devices used in the active power line conditioner. There are two types of current control techniques that can be designed by the regulated variables with the source current I_s or active power line conditioner current I_c [121]. They are

- Direct current controller
- Indirect current controller

The purpose is that AC mains should supply fundamental active power to a non-linear load and losses in the system. The active power line conditioner system should supply the harmonics of the load locally; hence the supply currents must be close to sinusoidal and locked in phase with the supply voltages. It is necessary to supply an additional active power to meet the losses of the active power line conditioner system, and to regulate the dc-voltage of the inverter. The regulation of dc-voltage ensures an effective current control at the input of the active power line conditioner. Since the regulation of dc-voltage imparts a proper current control of the active power line conditioner, the control scheme works with the dc-voltage as a feedback signal in both the techniques (direct and indirect) of current control. The current controls are aimed to get the sinusoidal shape of supply currents which are locked in phase with the voltages. However, these techniques differ in the methodology adopted for obtaining the switching pulses to drive the active power line conditioner.

4.2.1. Direct current control technique

To implement the direct current control technique, the seven analog signals $(v_{sa}, v_{sb}, v_{sc}, V_{dc}, i_{la}, i_{lb}, i_{lc})$ and three compensation currents (i_{ca}, i_{cb}, i_{cc}) are

sensed and computed. The three output reference signals $(i_{ca}^*, i_{cb}^*, i_{cc}^*)$ are generated using reference current extraction control method [58]. Fig.4.1 (a) shows the block diagram of the direct current control technique. The PWM switching pulses are obtained by comparing the sensed three-phase active power line conditioner currents (i_{ca}, i_{cb}, i_{cc}) with their reference counterpart's $(i_{ca}^*, i_{cb}^*, i_{cc}^*)$ currents.

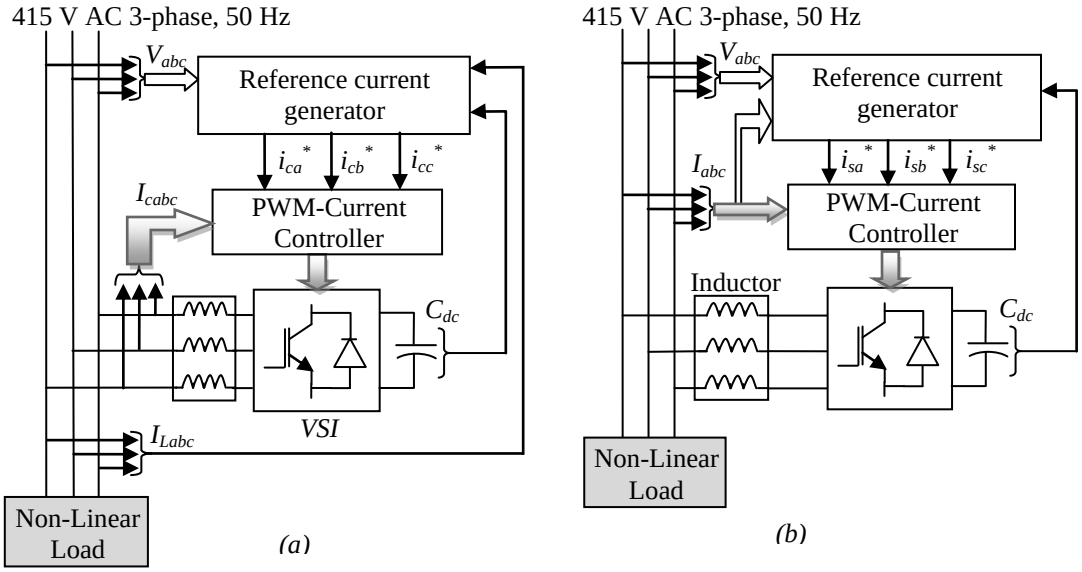


Fig.4.1 Block diagram of (a) Direct current controller and (b) Indirect current controller

4.2.2. Indirect current control technique

To implement the indirect current control technique, the four analog signals $(v_{sa}, v_{sb}, v_{sc}, V_{dc})$ and three actual source currents (i_{sa}, i_{sb}, i_{sc}) are sensed and computed [77]. Fig.4.1 (b) shows the block diagram of the indirect current control technique. In this technique, the PWM-switching pulses are obtained by comparing the sensed three-phase actual currents (i_{sa}, i_{sb}, i_{sc}) with their reference counterparts $(i_{sa}^*, i_{sb}^*, i_{sc}^*)$ which are generated by the reference current extraction methods. In chapter 3, the reference current extraction methods are discussed.

The PWM-switching pulses are processed in gate driver circuit for optical isolation and amplification. The gate driver circuit provides gate control switching pulses for the power transistor of the active power line conditioner. In response to these

switching pulses to power transistors of the inverter; APLC should meet the requirements of harmonics of the load while maintaining the dc capacitor voltage nearly constant. Therefore, the active power line conditioner system with nonlinear load should draw only sinusoidal unity power-factor balanced currents from the ac mains.

The response of the active power line conditioner system, during the steady state condition, illustrated that the direct control technique offers a slow response with a delay. The indirect current control technique offers instantaneous response without any delay. Therefore, the indirect current control technique is relatively free from the problem of switching ripples and actively eliminates the harmonics in the supply current for a given THD in the load current. The summary of the difference between both direct and indirect techniques of current control is given in Table 4.1 [121].

Table 4.1 Relative comparison of direct and indirect current control techniques

Type of technique	% THD in supply current	Load perturbation response	DSP computation time	Power consumed by AF	Number of current sensors	Requirement of ripple filter for improved performance	Commend generated from DSP / FPGA	Response of the AF
Direct current control	More	Poor	More	More	Six (more hardware)	Yes	AF current	With delay
Indirect current control	Less	Better	Less	Less	Three (less hardware)	No	Supply current	Instantaneous without delay

4.3. Modeling of PWM-VSI

The PWM-voltage source inverter has been modeled which comprises a three-phase ac-voltage applied through interface impedance on its input, and dc-link capacitor on its output. The three-phase voltages v_{ca}, v_{cb} *and* v_{cc} and reflected on the input side can be expressed in terms of the dc-link capacitor voltage V_{dc} and switching functions states the ON / OFF status of the devices of each leg S_A, S_B *and* S_C as [73]

$$v_{ca} = \frac{V_{dc}}{3}(2S_A - S_B - S_C)$$
$$v_{cb} = \frac{V_{dc}}{3}(-S_A + 2S_B - S_C) \quad (4.1)$$
$$v_{cc} = \frac{V_{dc}}{3}(-S_A - S_B + 2S_C)$$

The three-phase currents $i_{ca}, i_{cb}\ and\ i_{cc}$ flowing through the filter impedance (R_c, L_c) are obtained by solving the following equations

$$i_{ca} = -(R_c / L_c)i_{ca} + (v_{sa} - v_{ca}) / L_c$$
$$i_{cb} = -(R_c / L_c)i_{cb} + (v_{sb} - v_{cb}) / L_c \quad (4.2)$$
$$i_{cc} = -(R_c / L_c)i_{cc} + (v_{sc} - v_{cc}) / L_c$$

The dc-link capacitor current can be obtained in terms of phase currents $i_{ca}, i_{cb}\ and\ i_{cc}$ and the switching status (1 for ON-state and 0 for OFF-state) of the devices $S_A, S_B\ and\ S_C$

$$I_{dc} = i_{ca}S_A + i_{cb}S_B + i_{cc}S_C \quad (4.3)$$

From this, the model equation of the dc-link capacitor voltage can be written as

$$V_{dc} = \frac{1}{C_{dc}}(i_{ca}S_A + i_{cb}S_B + i_{cc}S_C) \quad (4.4)$$

The dc-link capacitor voltage serves as the energy storage element to supply real-power (to the inverter) difference between load and source during the transient period. In the steady state, the real power supplied by the source should be equal to the real-power demand of the load plus small power to compensate the losses in the active power line conditioner. If the active power line conditioner provides the total reactive and harmonic current, then the source current will be in phase with the supply voltage and sinusoidal in nature.

4.4. Triangular-carrier current controller

The triangular-carrier current controller is one of the familiar methods for active power line conditioner applications to generate gate control switching pulses of the PWM-inverter. The PWM based TCCC is utilized independently for each phase. It directly generates the VSI-switching pulses of the three (A, B, C) phase system [51]. In case of A-phase, the actual source current is represented as i_{sa} and reference

current is represented as $i_{sa}*$. Similarly, B-phase and C-phase currents are represented as $i_{sb}\ and\ i_{sb}*$ and $i_{sc}\ and\ i_{sc}*$ respectively. Fig.4.2 shows the block diagram of the A-phase followed triangular-carrier current controller.

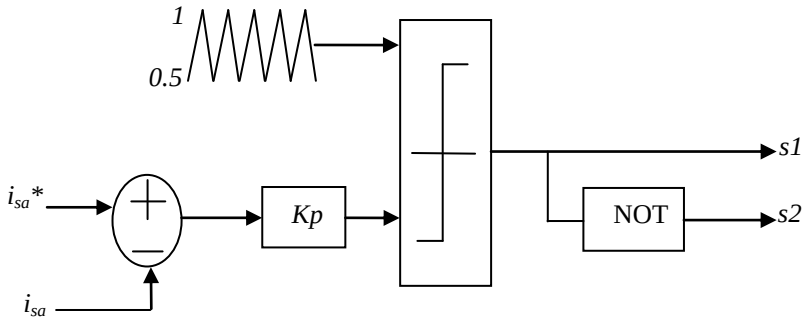


Fig.4.2 Block diagram of triangular-carrier current controller

To determine the switching transitions by means of the error current (reference current $i_{sa}*$ compared with the actual source current i_{sa}) is amplified with proportional gain. The output error signal is compared with triangular carrier signal to generate the required switching pulses. In A-phase, if the current error signal is greater than the triangular carrier signal, the upper inverter switch is ON. However, if the current error signal is smaller than the triangular signal, the lower inverter switch is ON. Similarly, the switching performance of phase-B and phase-B devices can be derived comparing with triangular signals. Thus the switching frequency of the power transistor is equal to the frequency of the triangular carrier signal. The triangular-carrier controller provides best harmonic distortion and the current ripple lower than other methods. However, this controller with proportional gain introduced overshoot problems and it has lower bandwidth.

4.5. Triangular periodical current controller

The triangular-periodical current controller is used to generate the switching pulses of the PWM-voltage source inverter. This technique switches the power transistor of the inverter during the transitions of a fixed clock frequency [55].

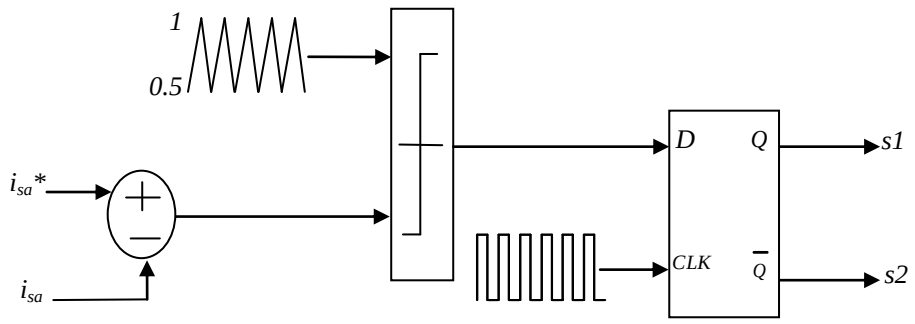


Fig.4.3 Block diagram of triangular-periodical current controller

The triangular-periodical current controller is utilized independently for each (A, B, C) phase of the inverter. Fig.4.3 shows the block diagram of the triangular-periodical current controller. The reference current $i_{sa}*$ is directly compared with the actual current i_{sa} to determine the error signal. The error current is compared with the triangular carrier signal and held D-Latch. The D-Latch maintain at a regular interval Ts synchronized with the clock of frequency equal to $1/Ts$. Thus the switching frequency of the power transistor is equal to the clock frequency. The merits of this technique are that the minimum time between switching transitions is limited to the period of the sampling clock. However, the actual switching frequency is not clearly defined and it has fixed bandwidth.

4.6. Space vector modulation control

Three phase modulating signal can be represented as a vector of fixed magnitude and rotating at constant angular velocity $'\omega'$ in the complex plane, which is called a sparse vector. Let the supply voltage $v_a, v_b \, and \, v_c$ be three phase variables that add up to zero in the stationary $a, b \, and \, c$ reference frame. The corresponding state space vector is defined as,

$$v = v_\alpha + jv_\beta = \frac{2}{3}\left(v_a + v_b e^{-j\frac{2\pi}{3}} + v_c e^{-\frac{4\pi}{3}} \right) \tag{4.5}$$

where,

α -voltage quantity is oriented in the same direction of the phase

β -voltage quantity is displaced 90^o lag from the α quantity.

$$v_\alpha = \frac{2}{3}\left(v_a - \frac{1}{2}v_b - \frac{1}{2}v_c \right) \tag{4.6}$$

$$v_\beta = \frac{2}{3}\left(\frac{\sqrt{3}}{2}v_b - \frac{\sqrt{3}}{2}v_c \right) \tag{4.7}$$

A voltage source inverter can assume eight distinct switching states as shown in Fig.4.4. Six out of these eight topologies produce a nonzero output voltage, known as active switching states and the rest two produce zero output voltage, known as zero switching or null state vectors.

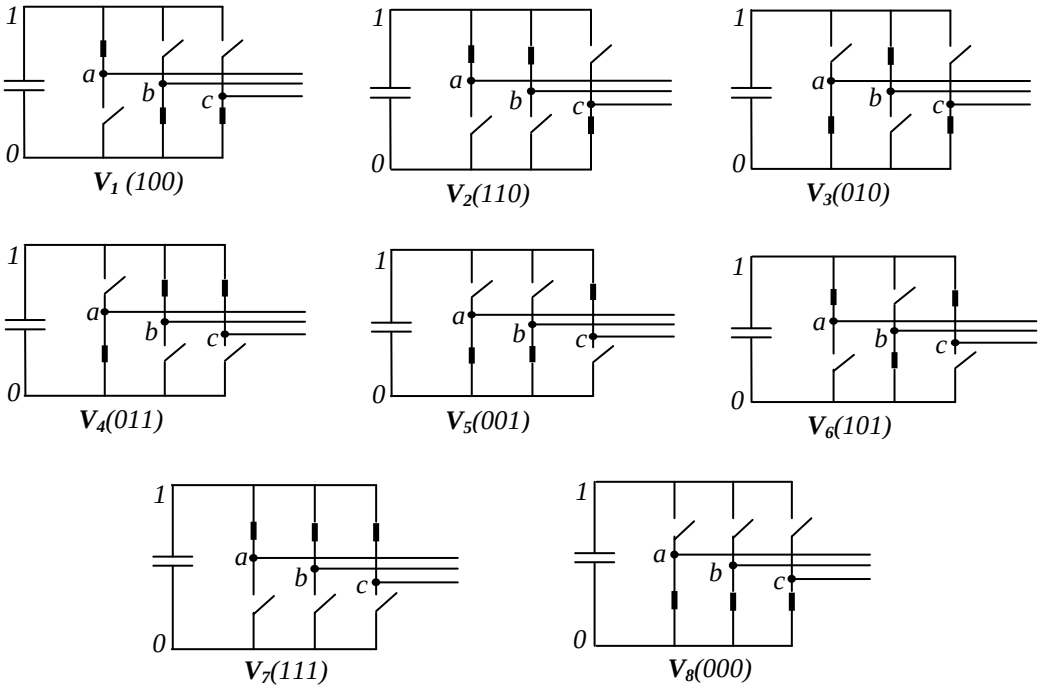


Fig.4.4 Eight switching state topologies of the VSI

Let $v_{ao} - v_{bo} - v_{co}$ be the three phase pole voltages of the VSI in the stationary $a-b-c$ reference frame taken with respect to the midpoint of the dc-capacitor voltage [54] [122].

$$v_{no} = \begin{cases} v_{dc} & if\ 'top'\ switch\ is\ closed \\ -v_{dc} & if\ 'bottom'\ switch\ is\ closed \end{cases}$$

$$where, n = \{a, b, c\} \tag{4.8}$$

For the first converter state, $v_1(100)$ shown in Fig.4.4, $v_{ao} = v_{dc}$, $v_{bo} = -(v_{dc})$, $v_{co} = -(v_{dc})$. Then the components of the corresponding state space vector are found from equations (4.6) and (4.7) as shown below,

$$v_\alpha = \frac{2}{3}\left(v_{dc} - \frac{1}{2} \times -v_{dc} - \frac{1}{2} \times -v_{dc} \right) = \frac{4}{3} v_{dc}$$

$$v_\beta = \frac{2}{3}\left(\frac{\sqrt{3}}{2} \times -v_{dc} - \frac{\sqrt{3}}{2} \times -v_{dc} \right) = 0 \tag{4.9}$$

Table 4.2 shows the components of the state space vector corresponding to each of the eight possible converter states.

Table 4.2 Space vector components for VSI switching states

Converter states	Three phase pole voltages			Components of space vector	
	v_{ao}	v_{bo}	v_{co}	v_α	v_β
$v_1(100)$	v_{dc}	$-(v_{dc})$	$-(v_{dc})$	$(4/3)v_{dc}$	0
$v_2(110)$	v_{dc}	v_{dc}	$-(v_{dc})$	$(2/3)v_{dc}$	$(2/\sqrt{3})v_{dc}$
$v_3(010)$	$-(v_{dc})$	v_{dc}	$-(v_{dc}/2)$	$-(2/3)v_{dc}$	$(2/\sqrt{3})v_{dc}$
$v_4(011)$	$-(v_{dc})$	v_{dc}	v_{dc}	$-(4/3)v_{dc}$	0
$v_5(001)$	$-(v_{dc})$	$-(v_{dc})$	v_{dc}	$-(2/3)v_{dc}$	$-(2/\sqrt{3})v_{dc}$
$v_6(101)$	v_{dc}	$-(v_{dc})$	v_{dc}	$(2/3)v_{dc}$	$-(2/\sqrt{3})v_{dc}$
$v_7(111)$	v_{dc}	v_{dc}	v_{dc}	0	0
$v_8(000)$	$-(v_{dc})$	$-(v_{dc})$	$-(v_{dc}$	0	0

It is observed in the state vector plane, indicating each of the eight converter state maps to a stationary vector with constant magnitude and direction. Space vector diagram of converter states and modulating signal are shown in Fig.4.5. From the diagram, it is observed the entire state space is divided into six equal sectors by the active state vectors and each sector space in 60^0.

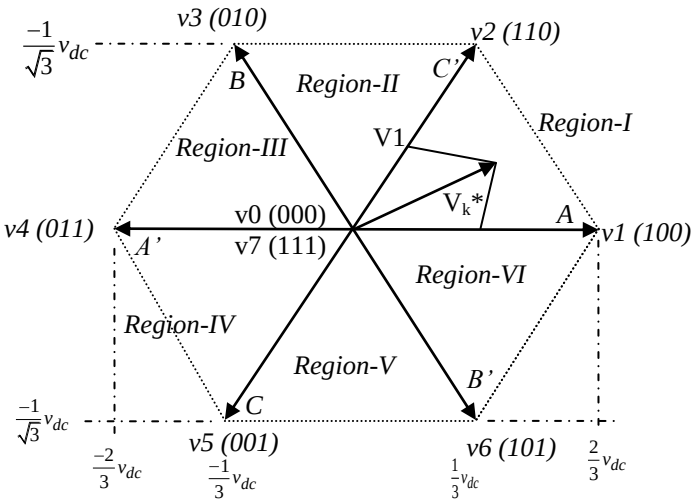


Fig.4.5 Space vector diagram of the converter states and modulating signal

The objective of the space vector PWM technique is to approximate the continuously rotating reference voltage vector v_{ref} using the eight stationary converter voltage vectors. For this purpose reference voltage vector v_{ref} is sampled at a sampling frequency f_s, which is much higher than the frequency of the reference signal. Reference vector during each sampling period can be assumed to be constant. It can be approximated by applying suitable converter voltage vectors for specified time durations within that sampling period. Nearest three vectors switching method are the most popular technique used for synthesizing the reference voltage vector. In this method, the reference vector in each sampling period is expressed as a weighted average combination of the adjacent active state vectors and the null state vectors. Let us assume the reference vector v_{ref}, in a particular sampling period lies in sector 1. It is synthesized by time averaging of the nearest vectors v_1, v_2 and the null vector

during that sampling period. In general, if v_{ref} is laying in the sector 'k', adjacent active vectors are v_k and v_{k+1}. From this the v_{ref} can be synthesized as follows.

$$v_{ref} = v_k \frac{T_k}{T_s} + v_{k+1} \frac{T_{k+1}}{T_s} \tag{4.10}$$

where,

T_k *and* T_{k+1} - Time duration of k^{th} *and* $(k+1)^{th}$ active state vectors respectively.

T_s - Sampling period.

Time duration of null vector is given by,

$$T_o = T_s - (T_k + T_{k+1}) \tag{4.11}$$

The zero switching states are equally distributed around the active switching states and switching sequence is arranged so that transition from one state to the next is performed by switching only one inverter leg. The technique provides high performance in terms of harmonic minimization.

4.7. Fixed-hysteresis current controller

The conventional or fixed-hysteresis current control method for active power line conditioner line currents can be carried out to generate the switching pattern of the inverter. The hysteresis current controller can be classified as two-level and three-level hysteresis current controller.

4.7. 1. Two-level hysteresis current controller

Conventional hysteresis current control operates the voltage source inverter by comparing the current error $e(t)$ against the fixed-hysteresis bands. This block diagram of the two-level hysteresis current controller is shown in Fig.4.6 (a). The current error is the difference between the reference current and the actual current. If the error current exceeds the upper limit of the hysteresis band, the upper switch of the inverter arm is turned OFF and the lower switch is turned ON. As a result, the current starts to decay [51-52]. Fig.4.6 (b) shows the ON and OFF switching pulses to drive the active power inverter. If the error current crosses the lower limit of the band, the lower switch is turned OFF and the upper switch is turned ON. As a result, the

current gets back into the hysteresis band. Hence, the actual current is forced to track the reference current within the hysteresis band.

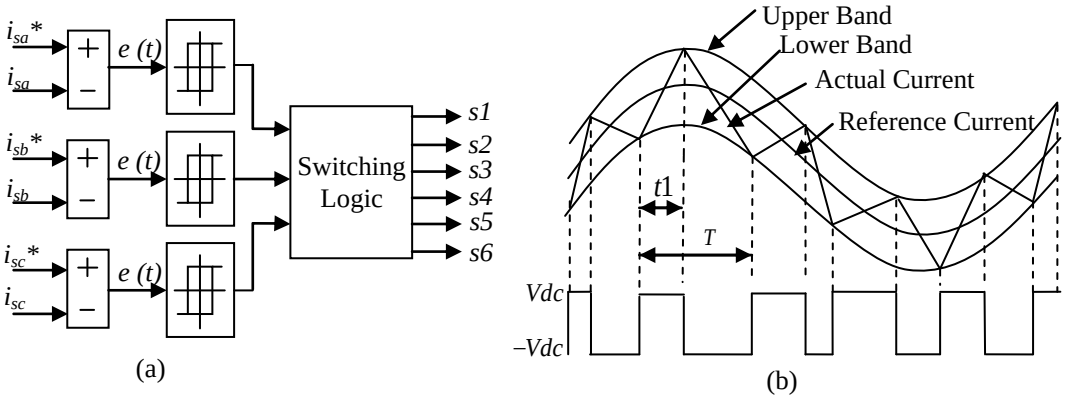


Fig.4.6 Block diagram of (a) two-level HCC and (b) two-level switching pattern

The phase-A switching performance is defined as

$$S = \begin{cases} OFF & if \;\; i_{sa}(t) > i_{sa}^{*}(t) + hb \\ ON & if \;\; i_{sa}(t) < i_{sa}^{*}(t) - hb \end{cases} \tag{4.12}$$

Similarly, the switching performance of phase-B and phase-C devices can be derived using hysteresis- bandwidth hb. The two-level hysteresis controllers are widely used for active power line conditioner applications, because the circuit is very simple [123]. However, it does not use zero voltage from the inverter dc-side; only positive and negative dc supply voltages are used to generate the required switching pulses. It is well known that the harmonic performance of two-level modulation is inferior to three-level modulation. The two-level modulation generates significant sideband harmonics around the switching frequency. To overcome the problems, the three-level hysteresis modulation is implemented with three-level switching process. The three-level hysteresis current control approach provides superior performance on harmonic perspective.

4.7.2. Three-level hysteresis current controller

The implementation of three-level modulation hysteresis controller are set as upper and lower band overlap boundaries and displacement of small offset current. Whenever the current error $e(t)$ crosses an outer hysteresis boundary, the inverter

output is set to an active positive or negative output to force a reversal of the current error. Similarly, whenever the current error reaches an inner hysteresis boundary, the inverter output is set to zero condition and the current error will be forced to reverse direction without reaching the next outer boundary. If the selection of zero output does not reverse the current trajectory, it will continue through the inner hysteresis boundary to the next outer boundary, where an opposite polarity active inverter output will be controlled and the current will reverse in any direction [57]. The three-level HCC based switching process is shown in Fig.4.7. The current error is bounded between the upper-inner and lower-outer hysteresis boundaries for a positive inverter output. Similarly, the current error is bounded between the lower-inner and upper-outer hysteresis boundaries for a negative inverter output.

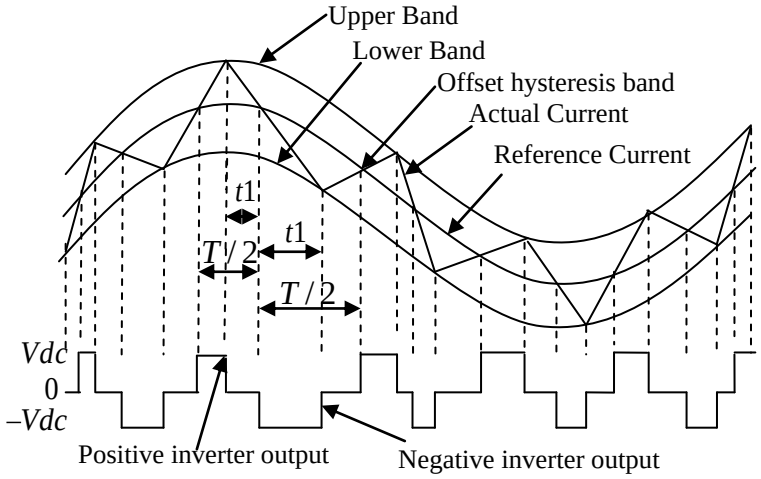


Fig.4.7 switching patterns of the three-level HCC

A complete switching cycle of the two-level HCC goes from $0 \rightarrow t_1 \rightarrow T$; whereas the three-level HCC switching cycle goes from $0 \rightarrow t_1 \rightarrow T/2$. The switching process introduces a positive or negative dc-offset error in the average output current, depending on the polarity of the active output voltage. However, this error can be corrected by adding a compensation factor of half the hysteresis band offset magnitude to the phase current reference. The polarity of this compensation factor is determined by the polarity of the most recent inverter active output. In other words, it

is positive when positive inverter output is in use and vice-versa. The MATLAB program for A-phase switching operation of the inverter is given as [124]

```
if error (i_a)>0
    if error (i_a)>= (hb)
    swa=0;
    end
    if error (i_a) <=del
    swa=1;
end
if error (i_a) <0
    if error (i_a) <= (-hb)
    swa=2;
    end
    if error (i_a)>= (-del)
    swa=1;
end
```

In case of A-phase, if swa=0 implies the switch state is positive V_{dc}, elsif swa=1 implies the switch state is zero, elsif swa=2 implies the switch state is negative V_{dc}. Similarly, the B-phase and C-phase switching function is carried out in the three phase voltage source inverter. Therefore, it reduces switching hence minimizes switching losses compared to the two-level hysteresis controller. Moreover, there is improvement in harmonic compensation.

The advantages of fixed-HCC are simple design, unconditioned stability and accuracy. However, current control with a fixed hysteresis-band has the unsatisfactory feature of variable switching frequency. The slope of current waveform may vary widely and the peak amplitude of current waveform may exceed the hysteresis-band. Consequently, inverter switches will be operated at high switching frequency in order to track reference current. Moreover, the variable switching frequency makes it difficult for the design of interface inductor and the selection of dc-link capacitor voltage value. This unpredictable switching function affects the active power line conditioner efficiency and reliability. Adaptive-hysteresis current controller overcomes the fixed-HCC demerits [58]. This adaptive-HCC changes the bandwidth according to instantaneous current variation.

4.8. Adaptive-hysteresis current controller

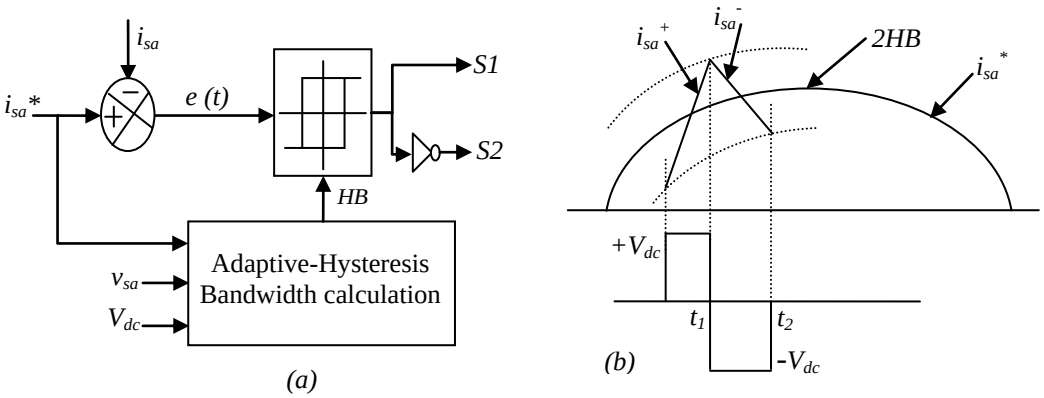


Fig.4.8 (a) Block diagram of an adaptive-HCC and (b) Single line switching function

Fig.4.8 (a) shows the block diagram of adaptive-HCC based switching pulse generator for PWM-voltage source inverter. The adaptive- hysteresis band controller proposed by Bose for the machine drive system is adopted here for three-phase three-wire active power line conditioner system based on indirect current control theory. When the current error $e(t)$ exceeds the upper limit of the adaptive-hysteresis band, the lower switch is turned ON. If the error current crosses the lower limit of the adaptive-hysteresis band, the upper switch is turned ON. Hence, the actual current is forced to track the reference current within the hysteresis-band. Fig.4.8 (b) shows the single line switching representation of ac-side power flow of shunt active power line conditioner. The following equations can be written for the switching interval t_1 and t_2 [59-60]

$$\frac{di_{sa}^{+}}{dt} = \frac{1}{L}(V_{dc} - v_s) \tag{4.13}$$

$$\frac{di_{sa}^{-}}{dt} = -\frac{1}{L}(V_{dc} + v_s) \tag{4.14}$$

where, $L =$ phase inductance, $(i_{sa}+)$ and $(i_{sa}-)$ are the respective rising and falling current segments.

[Notes: The current control method may be a design based on source currents (indirect-current control) or active power line conditioner currents (direct current control). Both methods are equivalent]

From the geometry of Fig.4.8 (b), the following equations can be written in the hysteresis-band curvature with respective switching intervals

$$\frac{di_{sa}^{+}}{dt}t_1 - \frac{di_{sa}^{*}}{dt}t_1 = 2HB \tag{4.15}$$

$$\frac{di_{sa}^{-}}{dt}t_2 - \frac{di_{sa}^{*}}{dt}t_2 = -2HB \tag{4.16}$$

$$t_1 + t_2 = T_c = 1/\ f_c \tag{4.17}$$

where t_1 and t_2 are the respective switching intervals, and f_c is the modulation frequency. Adding equation $(4.15)\ and\ (4.16)$

$$\frac{di_{sa}^{+}}{dt}t_1 + \frac{di_{sa}^{-}}{dt}t_2 - \frac{di_{sa}^{*}}{dt}(t_1 + t_2) = 0 \tag{4.18}$$

Substituting $di_{sa}^{+}/dt\ and\ di_{sa}^{-}/dt\ values$ in the equation (4.18)

$$\frac{(V_{dc} - v_s)}{L}t_1 - \frac{(V_{dc} + v_s)}{L}t_2 - \frac{di_{sa}^{*}}{dt}(t_1 + t_2) = 0 \tag{4.19}$$

Simplify and substituting $(t_1 + t_2) = 1/\ f_c$ in the equation (4.19)

$$\frac{V_{dc}}{L}(t_1 - t_2) - \frac{v_s}{L}(t_1 + t_2) - \frac{1}{f_c}\frac{di_{sa}^{*}}{dt} = 0 \tag{4.20}$$

Simplify the equation (4.20)

$$(t_1 - t_2) = \frac{L}{V_{dc} f_c}\left(\frac{v_s}{L} + \frac{di_{sa}^{*}}{dt}\right) \tag{4.21}$$

Subtracting $(4.16)\ from\ (4.15)$, we get

$$\frac{di_{a}^{+}}{dt}t_1 - \frac{di_{a}^{-}}{dt}t_2 - \frac{di_{sa}^{*}}{dt}(t_1 - t_2) = 4HB \tag{4.22}$$

Substituting $di_{sa}^{+}/dt\ and\ di_{sa}^{-}/dt\ values$ in the equation (4.22)

$$\frac{(V_{dc} - v_s)}{L}t_1 + \frac{(V_{dc} + v_s)}{L}t_2 - \frac{di_{sa}^{*}}{dt}(t_1 - t_2) = 4HB \tag{4.23}$$

Simplify this equation (4.23)

$$\frac{V_{dc}}{L}(t_1 + t_2) - \frac{v_s}{L}(t_1 - t_2) - \frac{di_{sa}^{*}}{dt}(t_1 - t_2) = 4HB \tag{4.24}$$

Further simplify and substituting $(t_1 + t_2) = 1/\ f_c$ in the equation (4.24)

$$\frac{V_{dc}}{f_c L} - (t_1 - t_2)\left(\frac{v_s}{L} + \frac{di_{sa}{}^*}{dt}\right) = 4HB \tag{4.25}$$

Here substituting $(t_1 - t_2)$ value in the equation (4.25)

$$\frac{V_{dc}}{f_c L} - \frac{L}{V_{dc} f_c}\left(\frac{v_s}{L} + \frac{di_{sa}{}^*}{dt}\right)^2 = 4HB \tag{4.26}$$

Simplify this equation (4.26)

$$HB = \frac{1}{4}\left[\frac{V_{dc}}{f_c L} - \frac{L}{V_{dc} f_c}\left(\frac{v_s}{L} + \frac{di_{sa}{}^*}{dt}\right)^2\right] \tag{4.27}$$

Further simplify the equation (4.27)

$$HB = \frac{0.25 V_{dc}}{f_c L}\left[1 - \frac{L^2}{V_{dc}{}^2}\left(\frac{v_s}{L} + m\right)^2\right] \tag{4.28}$$

Here, v_s is the supply voltage, V_{dc} is the dc-link capacitor voltage, L is the coupling inductor, $m = di_a{}^*/dt$ and is the slope of the reference current signals. The hysteresis band HB can be modulated at different points of fundamental frequency to control the switching pulses of the inverter. The calculated hysteresis bandwidth HB is applied to the switching operation of HCC. The switching operation is created by S-functions in MATLAB and is adopted in the Simulink model to produce gate control-switching pulses to drive the inverter.

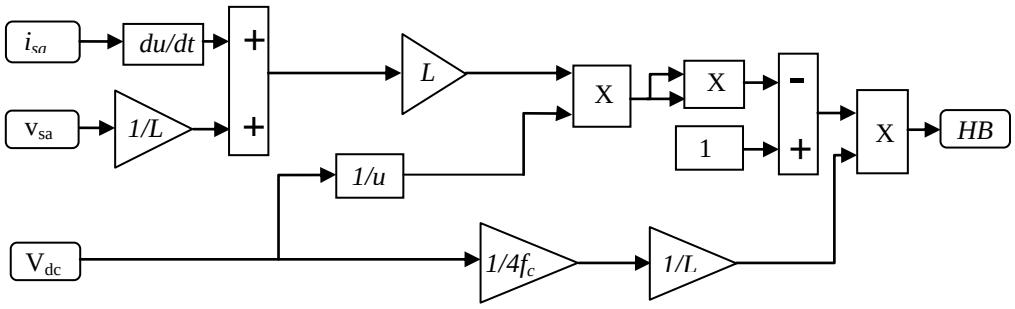


Fig.4.9 Block diagram of an adaptive-hysteresis bandwidth calculation

The switching frequency of the inverter depends on the dc-link capacitor voltage and coupling inductor of the active power line conditioner configuration. The block

diagram of the adaptive-hysteresis bandwidth calculation is shown in Fig.4.9. This adaptive-HCC ensures more switching power losses due to high frequency, which is solved by the proposed adaptive-fuzzy-HCC. The Adaptive-Fuzzy-HCC calculates the hysteresis bandwidth effectively with the help of fuzzy logic and reduces the switching power losses.

4.9. Adaptive-fuzzy hysteresis current controller

To improve the active power line conditioner performance without precise knowledge of the active power line conditioner parameters (interface inductor and dc-link capacitor voltage), the hysteresis band value can be implemented with a fuzzy logic controller [59] [125-127]. The block diagram of adaptive-fuzzy-HCC is shown in Fig.4.10 (a). The adaptive-fuzzy-hysteresis bandwidth is modulated as a function of slope reference current and supply voltage. The slope of the reference current $di_{sa}*/dt$ and supply voltage v_s are used as inputs for fuzzy processing as shown in Fig.4.10 (b). The adaptive-fuzzy hysteresis band HB is the output of the fuzzy controller.

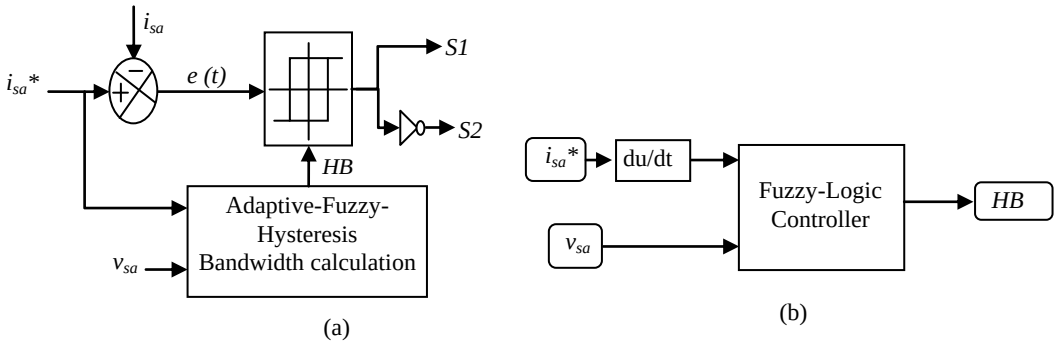


Fig.4.10 Block diagram of (a) Adaptive-fuzzy-HCC and (b) Fuzzy processing

The fuzzy logic is characterized by

- Five-fuzzy sets (NB, NM, ZE, PM and PB) for each input (slope of the reference current $di_{sa}*/dt$ and supply voltage v_s) and output variable (Positive Very Small (PVS), Positive Small (PS), Positive Medium (PM), Positive Big (PB) and Positive Very Big (PVB)) of adaptive-fuzzy hysteresis band HB as shown in Fig.4.11.

- Triangular membership function is used for the simplicity.
- Implication using Mamdani-type min-operator.
- Defuzzification using the centroid method.

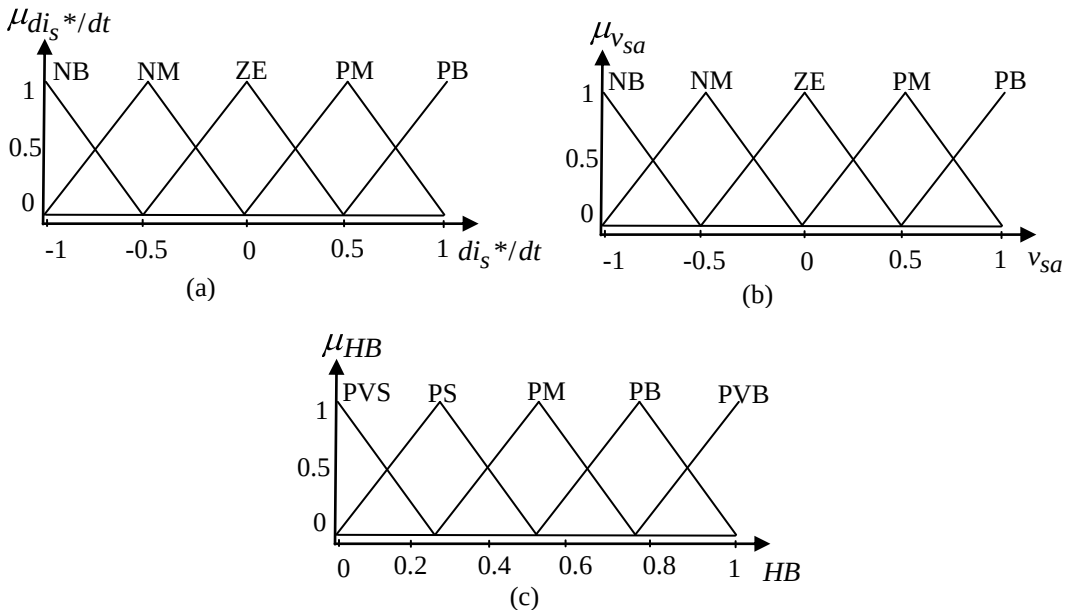


Fig.4.11 Membership functions for the input and variables di_{sa}/dt, v_{sa} *and HB*

The fuzzy logic rules are stored as linguistic variables required by rule evaluator. The 25-rules are used in this adaptive-fuzzy-hysteresis current controller that is given in Table 4.3.

Table 4.3 Fuzzy logic rules

$di_{sa}*/dt$ / V_{sa}	*NB*	*NM*	*ZE*	*PM*	*PB*
NB	PB	PM	PM	PM	PB
NM	PB	PM	PS	PM	PB
ZE	PVB	PM	PVS	PM	PVB
PM	PB	PM	PS	PM	PB
PB	PB	PM	PM	PM	PB

The output of fuzzy logic controller *HB* (hysteresis bandwidth) is modulated at different points of the fundamental frequency cycle to control the switching pulses of the voltage source inverter. For symmetrical operation of all three-phases, the hysteresis bandwidth *HB* is denoted as HB_a, HB_b *and* HB_c of the same value, but

having 120^0 phase difference. The Adaptive-Fuzzy HCC based hysteresis bandwidth HB should maintain the modulation frequency f_c quasi constant. This controller reduces the switching power losses and improves the PWM-VSI performances for active power line conditioner substantially.

4.10. Conclusions

The PWM-current control techniques are used to generate the required switching pulses for voltage source inverter. The triangular-carrier current controller, triangular-periodical current controller, space vector modulation controller, fixed-HCC, adaptive-HCC and proposed adaptive-fuzzy-HCC techniques are discussed.

The TCCC technique is very simple to implement; only a fixed amplitude and frequency triangular-carrier signal is compared with the error current (difference between reference current and actual current). The TPCC uses a triangular-carrier signal comparator and a D flip-flop per phase. The SVM technique confines space vector to be applied according to the region where the output voltage vector is located. However, the TCCC, TPCC and SVM techniques are claiming more switching power losses due to fixed frequency that reduces the active power line conditioner performance.

The fixed-HCC is simple in design, unconditioned in stability and easy to implement. However, this control scheme exhibits several unsatisfactory features such as the uneven switching frequency where the switching frequency varies within a particular band limit. Adaptive-HCC overcomes these fixed-HCC demerits. The adaptive-HCC changes the bandwidth according to instantaneous current variation. However, the adaptive-HCC is having more switching power losses due to high frequency switching. The problems discussed in the chapter can be solved by the Adaptive-Fuzzy-HCC.

The adaptive-fuzzy-HCC method calculates the bandwidth using the fuzzy logic controller without precise knowledge of the active power line conditioner parameters (interface inductor and dc-link capacitor voltage). The proposed adaptive-fuzzy-HCC method have reduced the switching power losses and improves the performance of the active power line conditioner compared to other techniques.

The various current control techniques are investigated using Matlab tool.

CHAPTER 5

SIMULATION RESULTS AND ANALYSIS

5.1. Introduction

This chapter investigates the performance of the shunt active power line conditioner by employing different methods of APLC control techniques. Fig.5.1 illustrates the various types of active power line conditioner controllers that have been investigated, which can be applied in the active power line conditioner system. The active power line conditioner controller consists of reference current extraction and PWM-VSI current controller. In chapter 3, reference current extraction methods are discussed. In chapter 4, indirect PWM-VSI current control techniques are discussed. This section is focused on simulation studies and analysis of the three-phase active power line conditioner system.

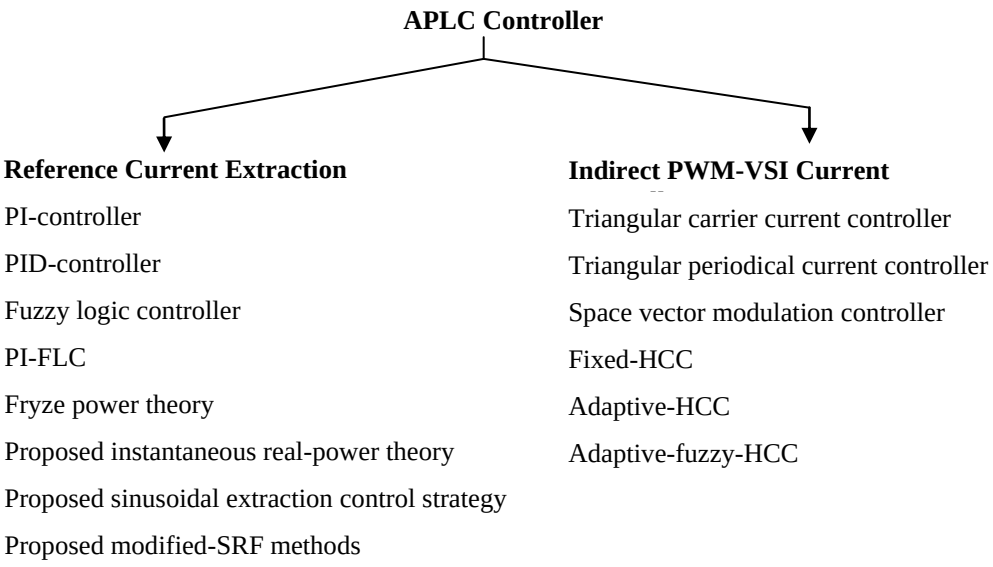


Fig.5.1 Subdivision of an APLC controller

To model the active power line conditioner system, the computer aided simulation is carried out in the MATLAB / SIMULINK environment using Simpower tools [128-

129]. For simulation, the system parameter values are given in Appendix-B, which is considered for three-phase active power line conditioner system. The voltage source inverter based APLC consists of six-power transistors with dc-link capacitor and connected to the PCC through interface inductor. The interface inductor has the function of suppressing higher order harmonic components caused by the switching operation of the power transistors. The active power line conditioner system uses the same platform with the similar simulation parameters for all the different control methods of active power line conditioner controller. Each reference current extraction method is in conjunction with various PWM-current control techniques (or vice-versa) is investigated separately. The active power line conditioner system is tested under diode / thyristor-rectifier load in both steady-state and transient-state conditions.

5.2. PI / PID / FLC and PI-FLC

The performance of the PI / PID / FLC / PI-FLC based shunt active power line conditioner system is evaluated through Matlab / Simpower tools. Fig.5.2 shows the block diagram of the three-phase shunt active power line conditioner system using above mentioned method(s). The ac-main supply feeds diode or thyristor rectifier load. The supply current draws non-sinusoidal waveform due to the rectifier load. It indicates the source current contains fundamental and harmonic current components. To compensate the current harmonics, shunt APLC is connected in parallel to the load at PCC that injects the anti-harmonics and make the supply current as sinusoidal. The active power line conditioner comprises six-IGBTs, dc-link capacitor, interface-filter, reference current extraction controller and switching pulse generator. The reference current extraction process is developed from unit current vector along with PI / PID / FLC / PI-FLC for extracting the reference currents from the distorted line currents. The PI / PID / FLC / PI-FLC are used to estimate the required amplitude of peak current using dc-link capacitor voltage of the inverter. The peak amplitude is multiplied with the unit current templates to generate the required reference current. The reference current is compared with actual current to generate the gate control switching pulses using TCCC / TPCC / SVM / fixed-HCC / adaptive-HCC / adaptive-fuzzy-HCC techniques.

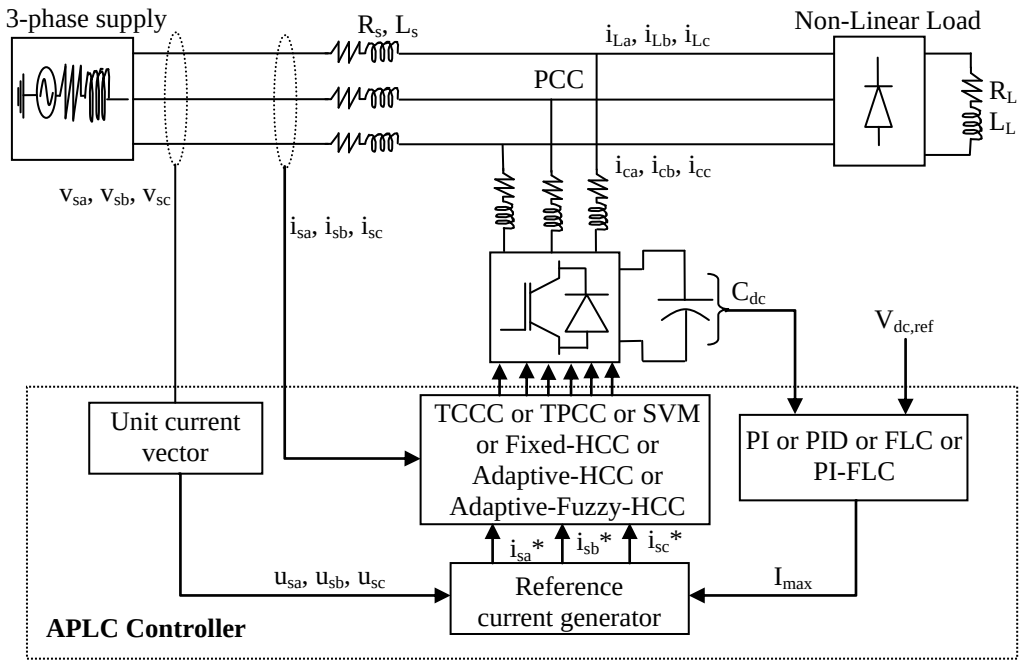


Fig.5.2 PI / PID / FLC / PI-FLC based *active power line conditioner system*

The effectiveness of an active power line conditioner basically depends on the design and characteristics of TCCC / TPCC / SVM / fixed-HCC / adaptive-HCC / adaptive-fuzzy-HCC techniques. The switching losses are increased in the TCCC, TPCC, SVM and fixed-HCC due to high frequency operation. These techniques add high frequency ripples in the generated current. The current controller performance is improved by using the adaptive-HCC technique. This adaptive-HCC changes the bandwidth according to instantaneous current variation. A novel adaptive-fuzzy-HCC based on the adaptive control concept is used where the bandwidth computation is done using fuzzy logic; this approach optimizes the PWM performance. Fig.5.3 illustrates the switching patterns of the various PWM-current controllers. The ripples in the currents are reduced even if the switching frequency is increased; the adaptive-fuzzy-HCC provides additional cushion for increase in switching frequency as per the system requirements. It reduces the arbitrary switching losses and current ripples, which improves the APLC performance.

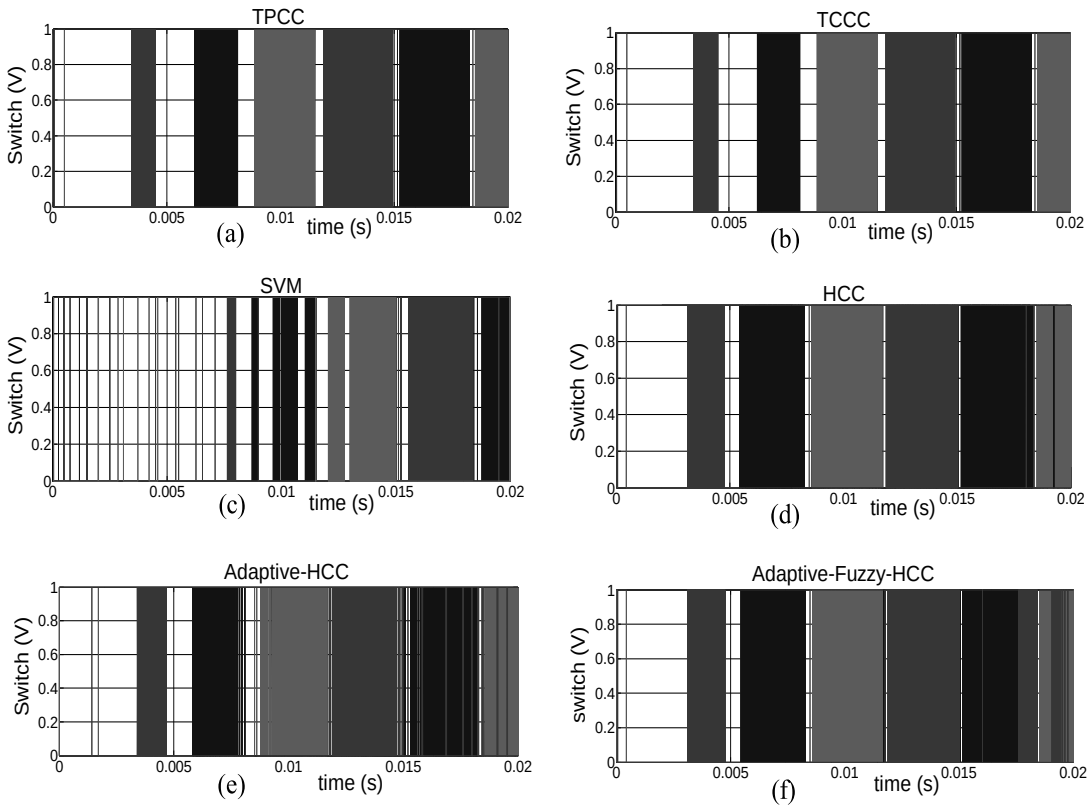


Fig.5.3 switching patterns of (a) TCCC, (b) TPCC, (c) SVM, (d) Fixed-HCC, (e) Adaptive-HCC and (f) Adaptive-fuzzy-HCC techniques

5.2.1. Case-1 PI-Controller

PI-controller with various PWM-current controllers based active power line conditioner system is simulated under balanced diode / thyristor-rectifier load conditions. The simulation in Fig.5.4 is focused on PI with TCCC, TPCC and SVM technique respectively. Fig.5.4 (a) shows the source current before compensation. It indicates that the source current contains fundamental as well as harmonic components due to the non-linear load. The TCCC / TPCC / SVM are used to generate the gate control switching pulses to drive the active power inverter. The inverter provides the required compensating current to compensate the harmonic current at PCC as shown in Fig.5.4 (b). The harmonic compensation is achieved by injecting equal but opposite harmonic components. Fig.5.4 (c) shows the source current after compensation. These waveforms are obtained under diode- rectifier load with the steady-state conditions. It is presented for A-phase only; the other phase (B-phase and C-phase) are phase shifted by 120^0

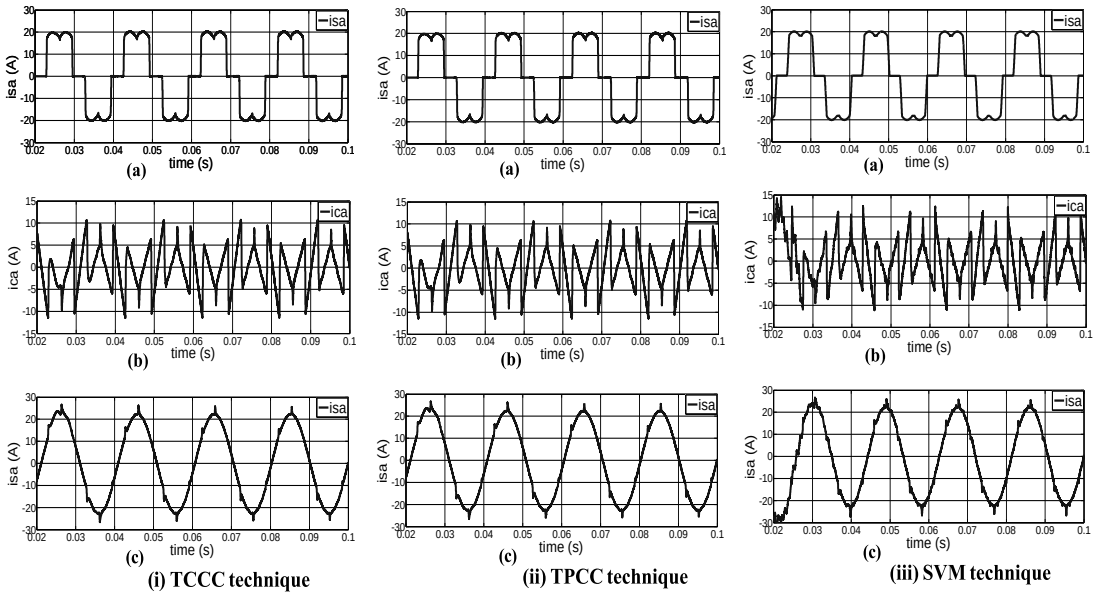


Fig.5.4 Simulation waveforms of (a) Source current before compensation, (b) Compensation current and (c) Source current after compensation

5.2.2. Case-2 PID-Controller

PID-controller with various PWM-current controller based active power line conditioner system is simulated under diode / thyristor-rectifier load conditions. However, the simulation in Fig.5.5 (i) and (ii) is obtained using PID with fixed-HCC and adaptive-HCC technique respectively. For transient-state condition, the step-time is applied between 0.06 s to 0.12 s (total simulation time is 0.14 s). Fig.5.5 (a) shows the source current before compensation under diode-rectifier load. It indicates that the source current contains fundamental and harmonic components due to the non-linear load. The fixed-HCC / adaptive-HCC is used to generate the switching pulses to drive the active power inverter. The inverter provides the required compensating current to compensate the harmonic current as shown in Fig.5.5 (b). The harmonic compensation is achieved by injecting equal but opposite harmonic components. Fig.5.5 (c) shows the source current after compensation that contains small frequency ripples and indicates the source current after compensation is sinusoidal.

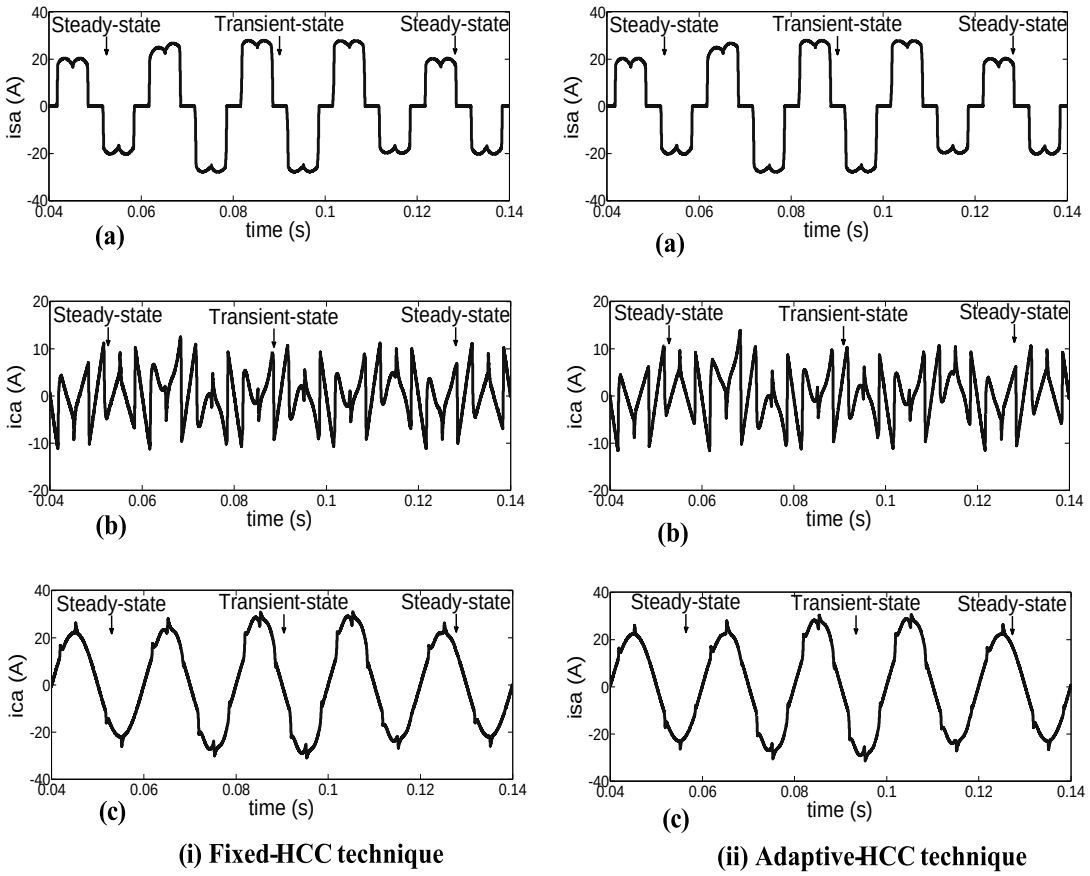


Fig.5.5 Simulation waveforms of (a) Source current before APLC compensation, (b) Compensation current and (c) Source current after APLC compensation

5.2.3. Case-3 Fuzzy logic controller

Fuzzy logic controller with TCCC / TPCC / SVM / fixed-HCC / adaptive-HCC / adaptive-fuzzy-HCC are simulated and investigated under diode / thyristor-rectifier load. Fig.5.6 is obtained using adaptive-fuzzy-HCC under thyristor-rectifier load with steady-state. Fig.5.6 (a) shows the instantaneous supply voltage and indicates the three-phase voltages are balanced. Fig.5.6 (b) shows the source currents before compensation which consist of fundamental as well as harmonic components due to the non-linear load. To compensate the harmonic currents, the active power line conditioner (when it is ON) should provide the required compensating currents as shown in Fig.5.6 (c). The source currents after compensation are presented in Fig.5.6 (d), which indicates when the APLC is ON, the source currents become sinusoidal.

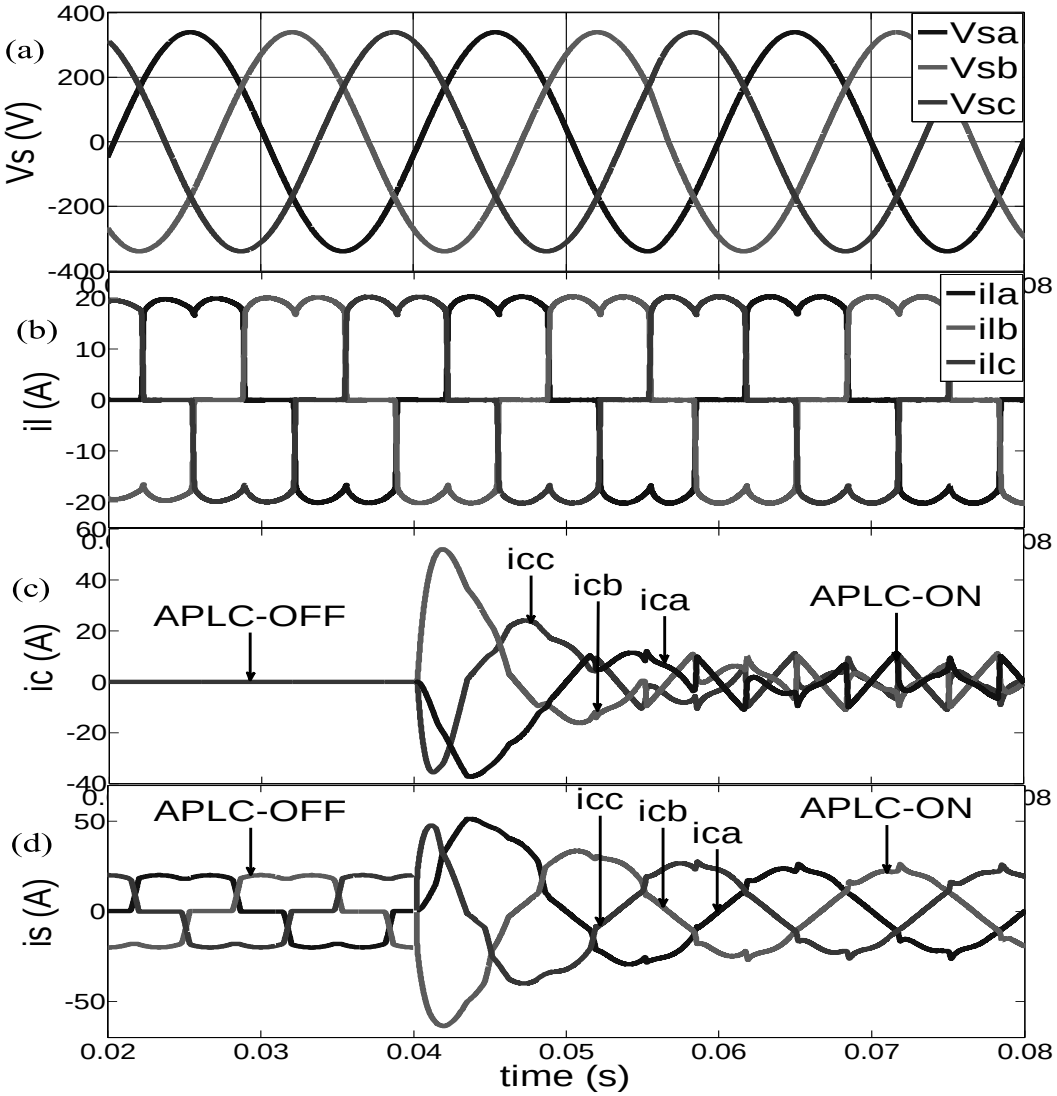


Fig.5.6 (a) Supply voltages, (b) Source currents before compensation, (c) Compensation currents (when APLC is OFF / ON) and (d) Source currents after compensation (when APLC is OFF / ON)

5.2.4. Case-4 PI with FLC

PI-Fuzzy logic controller with various PWM-current control techniques are simulated and investigated under diode / thyristor-rectifier load. The simulation in Fig.5.7 is obtained using PI-FLC with adaptive-fuzzy-HCC under thyristor-rectifier load. For transient-state (sudden change in load from R_L=50 Ω, L_L=40 mH to R_L=30 Ω, L_L=30 mH) condition, the step-time is applied between 0.06 s to 0.12 s. This simulation indicates how the APLC is also adapting to load changes and this sudden changes in load are termed as transients. Fig.5.7 (a) shows the instantaneous supply voltages and indicates that the three-phase voltages are balanced.

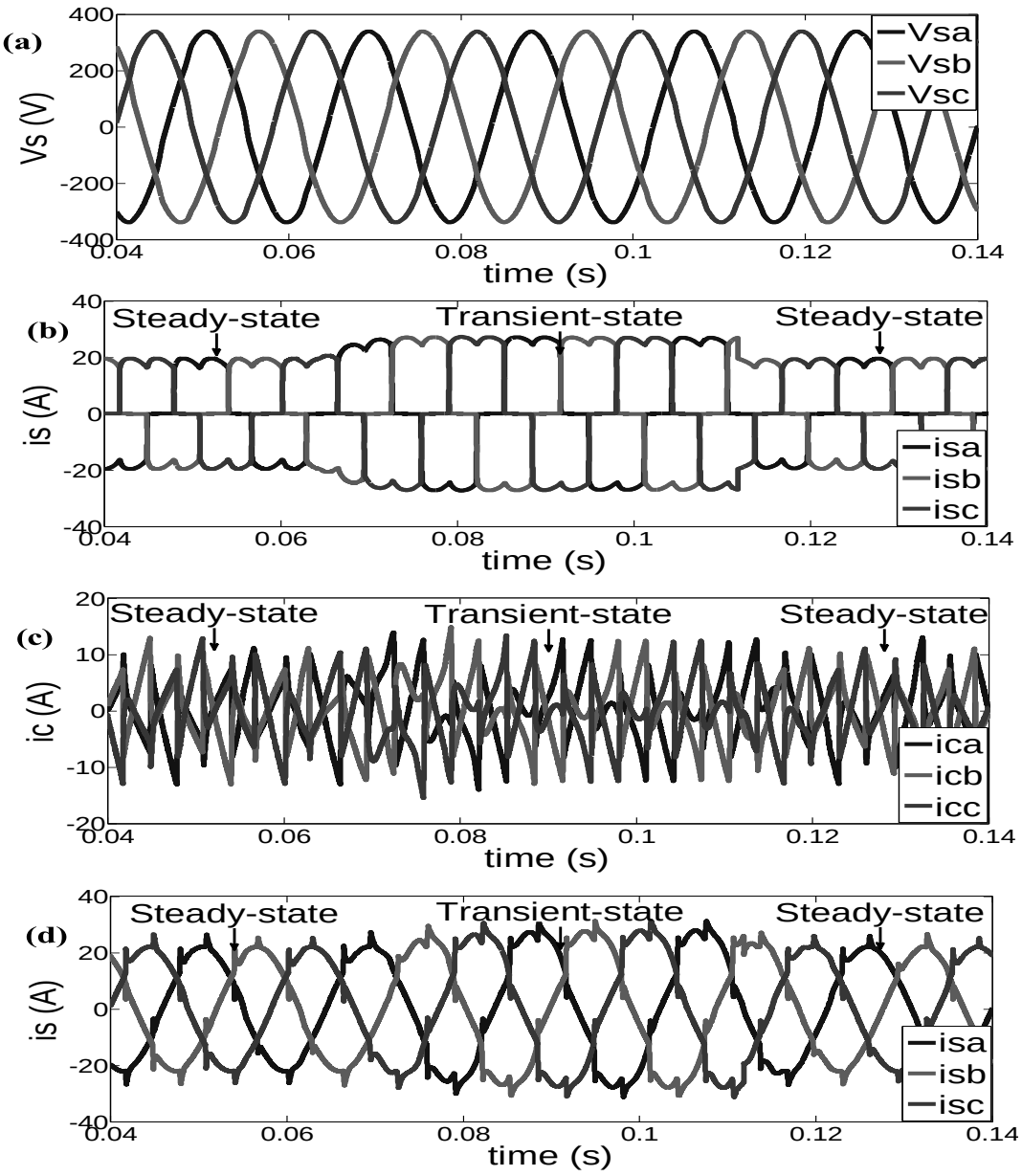


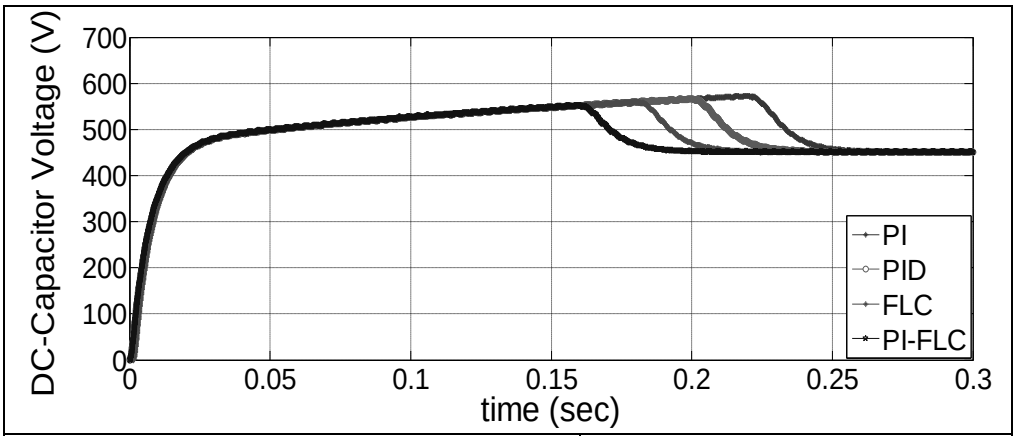
Fig.5.7 Simulations of (a) Supply voltages, (b) Source currents before APLC, (c) Compensation currents and (d) Source currents after APLC

Fig.5.7 (b) shows the instantaneous source currents before APLC compensation that contains fundamental as well as harmonic components. To compensate harmonic components, the active power line conditioner provides the required compensating currents as shown in Fig.5.7 (c). The harmonic compensation is achieved by injecting equal but opposite harmonic components. Fig.5.7 (d) shows the source currents after APPLC compensation and indicates that the source currents after compensation are sinusoidal and in-phase with the respective voltages.

5.2.5. Case-5 APLC system analysis

The active power line conditioner system is analyzed in terms of V_{dc} settling time, order of harmonics, real and reactive-power calculation.

V_{dc}-settling time: The dc-link capacitor voltage is controlled by PI or PID or FLC or PI-FLC. The proportional, integral and derivative (K_P=0.97; K_I=217 and K_D=0.01) gains are chosen mathematically. This controller reduces the ripples in the capacitor voltage to a certain level and makes settling time to low value, which is plotted in Fig.5.8. It indicates that PI-FLC facilitates settling time to reduce compared to the PI or PID or FLC methods.



Controller	V_{dc} settling time
PI	0.26s
PID	0.24s
Fuzzy	0.21s
PI-Fuzzy	0.18s

Fig.5.8 dc-link capacitor voltage settling time

THD analysis: The order of harmonics versus magnitude of the source current is plotted without / with-APLC under diode and thyristor-rectifier load. The simulation in Fig.5.9 (a)-(b) is for PI-FLC and adaptive-fuzzy-HCC based active power line conditioner for steady-state and transient-state condition (sudden load change) under diode-rectifier load. From the harmonic spectrum, it is observed that the supply current without-APLC is containing harmonic components. With-APLC the harmonic level of the THD is reduced from 26.66 % to 3.47 % in steady-state and 24.87 % to 4.25 % in transient-state respectively.

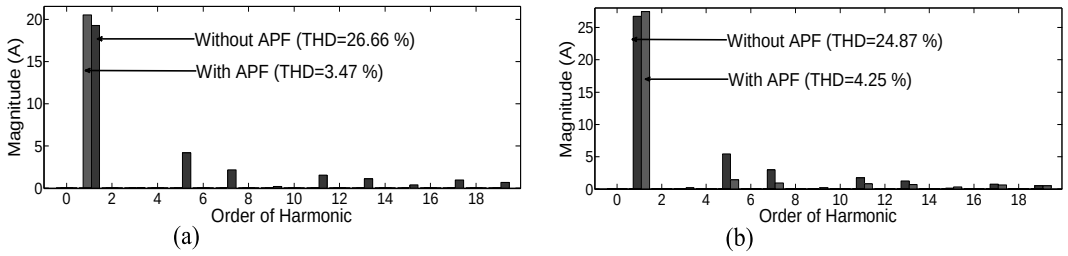


Fig.5.9 Order of harmonics (a) Steady-state and (b) Transient-state

The Fast Fourier Transform (FFT) is used to measure the order of harmonics in the source current. Total harmonic distortion of the source current is measured without-APLC and with-APLC using PI, PID, FLC and PI-FLC along with different PWM-current controllers. The THD measurement is compared under diode and thyristor-rectifier load in both steady-state and transient conditions that is presented in Table 5.1.

Real and Reactive power analysis: The active and reactive power block (in Simulink) measure the active power P and reactive power Q associated with a periodic voltage-current pair which comprises harmonics. With a sinusoidal voltage, current harmonics do not lead to average power. However, current harmonics do increase the rms current, and hence they decrease the power factor. The shunt APLC improves the power factor in the power system. Fig.5.10 shows the power factor correction, it indicates the a-phase voltage and current are in phase.

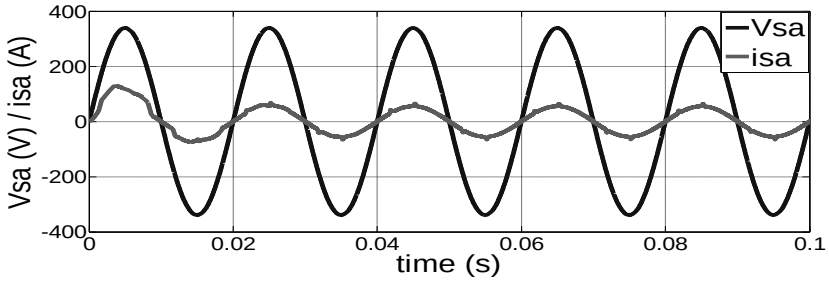


Fig.5.10 Source voltage per current for unity power factor

The real and reactive power is calculated by averaging the voltage and current product (magnitude and phase) with a running average window over one cycle of the fundamental frequency, so that the real and reactive power is evaluated at the fundamental frequency.

$$P = \frac{1}{T} \int_{(t-T)}^{t} V(\omega t) \times I(\omega t) dt \tag{5.1}$$

$$Q = \frac{1}{T} \int_{(t-T)}^{t} V(\omega t) \times I(\omega t - \pi / 2) dt \tag{5.2}$$

where $T = 1/f$ fundamental frequency).

For the first cycle of simulation the outputs are held constant using the values specified by the initial input parameters. The Real (P) and Reactive (Q) power is calculated and it is given in Table 5.2. This result indicates the shunt active power line conditioner is suppressing reactive power and hence improving the power factor in particular and power quality in general. Since the load is a power electronic load the power factor dexterities in the absence of APLC and hence a reactive power component arises. When we use APLC, power factor approaches almost unity and hence this reactive power reduces.

Table 5.1 THD measurements

Rectifier RL loads	Condition	Controller	Without APLC	With APLC					
				TCCC	TPCC	SVM	HCC	A-HCC	A-F-HCC
Diode	Steady state	PI	26.66 %	3.89 %	3.81 %	3.82 %	3.86 %	3.76 %	3.62 %
		PID		3.88 %	3.81 %	3.80 %	3.83 %	3.71 %	3.65 %
		Fuzzy		3.81 %	3.79 %	3.79 %	3.82 %	3.62 %	3.52 %
		PI-Fuzzy		3.76 %	3.69 %	3.63 %	3.64 %	3.58 %	3.47 %
	Transient	PI	24.87 %	4.87 %	4.77 %	4.76 %	4.79 %	4.53 %	4.38 %
		PID		4.86 %	4.78 %	4.79 %	4.77 %	4.53 %	4.36 %
		Fuzzy		4.86 %	4.75 %	4.77 %	4.76 %	4.59 %	4.30 %
		PI-Fuzzy		4.82%	4.75 %	4.76%	4.74%	4.48 %	4.25 %
Thyristor	Steady state	PI	26.79 %	3.85 %	3.79 %	3.78 %	3.81 %	3.75 %	3.62 %
		PID		3.83 %	3.80 %	3.81 %	3.80 %	3.73 %	3.57 %
		Fuzzy		3.84 %	3.76 %	3.79 %	3.82 %	3.66 %	3.49 %
		PI-Fuzzy		3.76 %	3.71 %	3.67 %	3.64 %	3.59 %	3.48 %
	Transient	PI	25.06 %	4.92 %	4.85 %	4.87 %	4.85 %	4.63 %	4.43 %
		PID		4.92 %	4.81 %	4.81 %	4.83 %	4.63 %	4.41 %
		Fuzzy		4.87 %	4.79 %	4.82 %	4.84 %	4.67 %	4.32 %
		PI-Fuzzy		4.82%	4.77 %	4.80%	4.81%	4.55 %	4.25 %

Table 5.2 Real (P) and Reactive (Q) power measurements

Rectifier RL loads	Controllers	Without APLC	With APLC		
			HCC	Adaptive-HCC	Adaptive-Fuzzy-HCC
Diode	PI	P=8.99 kW Q=239 VAR	P=9.45 kW Q=53 VAR	P=9.44 kW Q=48 VAR	P=9.74 kW Q=22VAR
	PID		P=9.45 kW Q=53VAR	P=9.44 kW Q=48 VAR	P=9.81 kW Q=15 VAR
	Fuzzy		P=9.45 kW Q=53VAR	P=9.44 kW Q=48 VAR	P=9.81 kW Q=15 VAR
	PI-Fuzzy		P=9.45 kW Q=53VAR	P=9.44 kW Q=48 VAR	P=9.81 kW Q=15 VAR
Thyristor	PI	P=8.74 kW Q=250 VAR	P=9.36 kW Q=26 VAR	P=9.42kW Q=63 VAR	P=9.86 kW Q=11 VAR
	PID		P=9.45 kW Q=53 VAR	P=9.47 kW Q=48 VAR	P=9.81 kW Q=15 VAR
	Fuzzy		P=9.45 kW Q=53 VAR	P=9.47 kW Q=48 VAR	P=9.81 kW Q=15 VAR
	PI-Fuzzy		P=9.45 kW Q=53 VAR	P=9.47 kW Q=48 VAR	P=9.81 kW Q=15 VAR

Remarks: The PI, PID, FLC and PI-FLC conjunction with the various PWM-current controller based active power line conditioner system has been simulated and performance is evaluated. The adaptive-fuzzy-HCC reduces the switching power losses and improves the active power line conditioner performance in comparison with the TCCC, TPCC, SVM, fixed-HCC and the adaptive-HCC. Similarly PI-FLC is giving better performance than conventional PI or PID or FLC in terms of V_{dc}-settling time, harmonic current and reactive-power compensation. The FFT analysis of the active power line conditioner validates the THD of the source current to be less than 5% of all the cases.

5.3. Fryze power theory

The performance of the fryze power theory with various PWM-current controller based shunt active power line conditioner system is evaluated through Matlab / Simulink tools. The model system consists of three-phase voltage source inverter, interface-inductor, reference current extraction controller (fryze power theory) and PWM-switching pulse generator as shown in Fig.5.11. The fryze power theory is used to extract the required reference current from the distorted load current. The reference current is compared with actual current to generate the switching pulses using TCCC / TPCC / SVM / fixed-HCC / adaptive-HCC / adaptive-fuzzy-HCC techniques to drive the active power inverter. The APLC supplies the compensating current to compensate current harmonics and reactive-power in the distributed system. The system performance is demonstrated under diode and thyristor-rectifier load with steady-state and transient conditions.

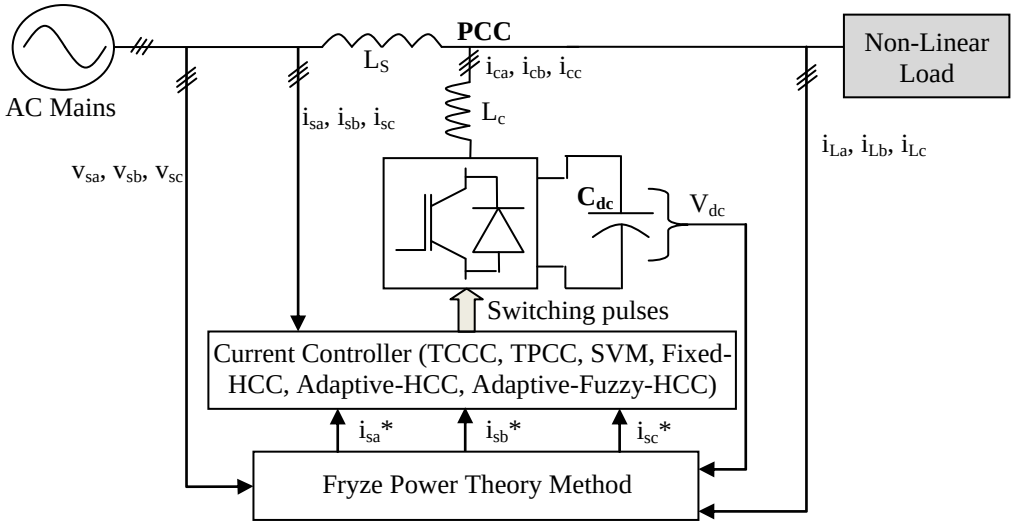


Fig.5.11 Fryze power theory based shunt APLC implemented with VSI

5.3.1. Case-1 Fixed-HCC and adaptive-HCC

Fig.5.12 shows the fixed-HCC / adaptive-HCC based active power line conditioner under steady-state with the diode-rectifier load. Fig.5.12 (a) shows the compensation current when APLC is OFF and ON. Fig.5.12 (b) shows the instantaneous source current before and after compensation (while APLC is OFF and ON) using fixed-HCC. Similarly, Fig.5.12 (c) and (d) indicates the compensation current and source current before and after shunt APLC compensation (while APLC is OFF and ON).

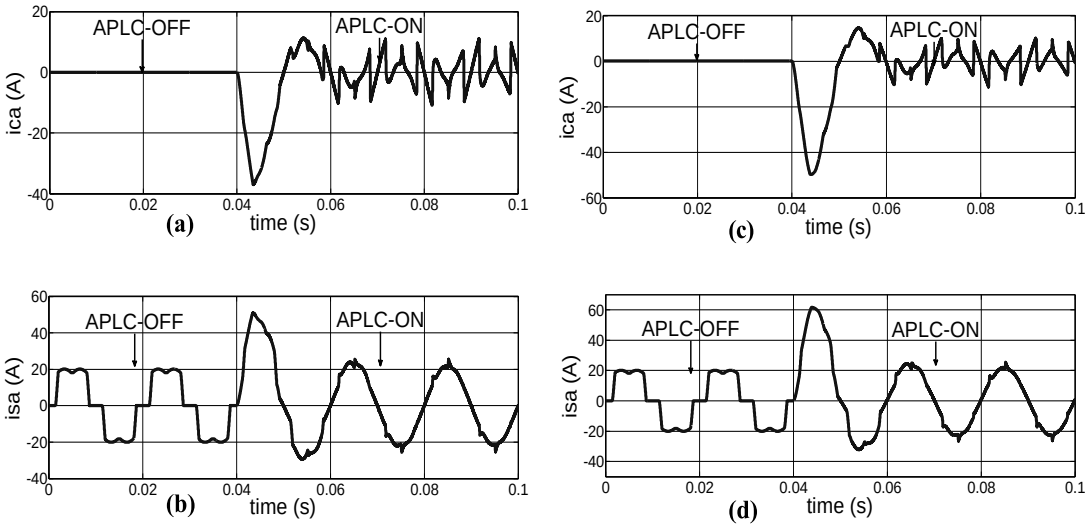


Fig.5.12 (a) Compensation current under APLC is OFF / ON, (b) source current under APLC is OFF / ON using fixed-HCC, and (c-d) compensation current and source current under APLC is OFF / ON using adaptive-HCC

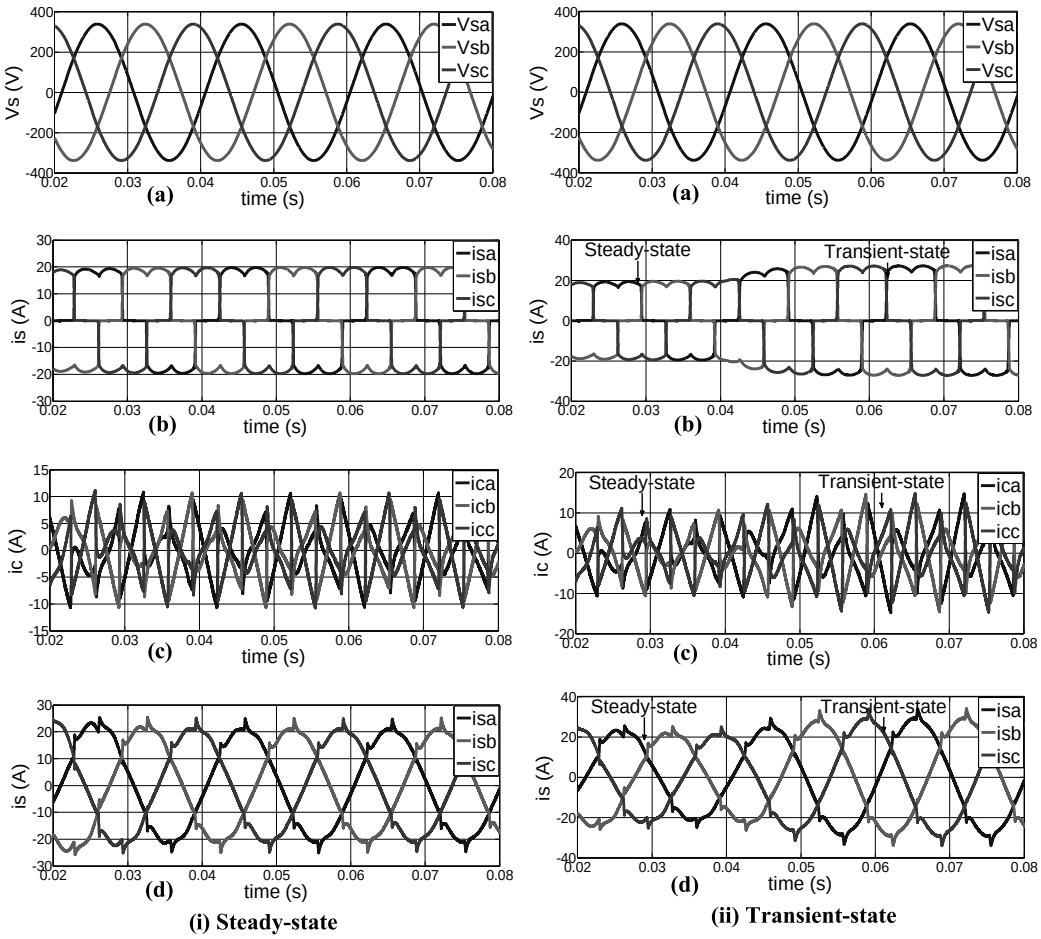


Fig.5.13 Simulation waveforms of (a) Steady-state (b) Transient-state

5.3.2. Case-2 Adaptive-fuzzy-HCC

Fig.5.13 (i) and (ii) are obtained using fryze power theory with adaptive-fuzzy-HCC based active power line conditioner system under steady-state and transient-state respectively. Fig.5.13 (a) shows the instantaneous supply voltages and indicates the three-phase voltages are balanced. Fig.5.13 (b) shows the instantaneous source currents before compensation, which comprises fundamental as well as harmonic components due to thyristor-rectifier load. To compensate harmonic components, the active power line conditioner supplies the necessary compensating currents as shown in Fig.5.13 (c). The active power line conditioner compensates harmonic current components by injecting equal-but-opposite harmonic current components. As a result, components of harmonic currents contained in the load current are cancelled by the effect of the active power line conditioner. Fig.5.13 (d) shows the source currents after compensation and indicates the source currents after compensation are sinusoidal and in-phase with the respective voltages.

5.3.3. Case-3 APLC system analysis

The active power line conditioner is analyzed in terms of settling time of the dc-voltage inverter, order of harmonics, real and reactive power calculation.

dc-link capacitor voltage: The dc-link capacitor voltage of the voltage source inverter is controlled by proportional and integral gain. Fig.5.14 shows the waveform of the dc-link capacitor voltage and ensures that it is nearly constant.

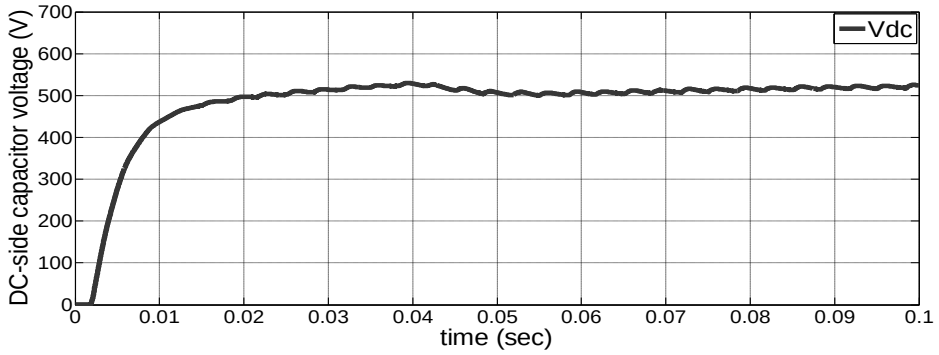


Fig.5.14 dc-link capacitor voltage settling time

THD analysis: The fryze power theory with adaptive-fuzzy-HCC based active power line conditioner system is compensating harmonic current components at the PCC.

Fig.5.15 (a) and (b) are plotted with the order of the harmonics versus magnitude of the source current. These figures are captured without-APLC and with-APLC under thyristor-rectifier load with steady-state and transient conditions. Without-APLC the supply current is distorted due to the harmonic spectral components and with-APLC the THD is reduced to a value which is less than 5%.

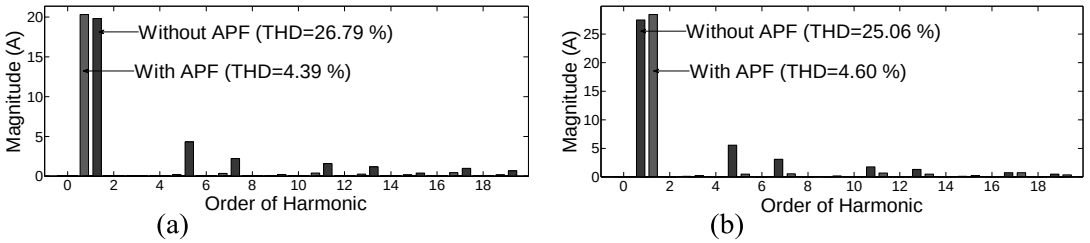


Fig.5.15 Order of harmonics (a) Steady-state and (b) Transient-state

The THD of the source current is measured without-APLC and with-APLC using fryze power theory along with different PWM-current controllers that are presented in Table 5.3.

Table 5.3 THD measurements

Rectifier RL Loads	Condition	Without APLC	With APLC					
			TCCC	TPCC	SVM	F-HCC	A-HCC	A-F-HCC
Diode	Steady state	26.66 %	4.73 %	4.64 %	4.66 %	4.81 %	4.62 %	4.47 %
	Transient	24.87 %	4.82 %	4.74 %	4.76 %	4.87 %	4.71 %	4.52 %
Thyristor	Steady state	26.79 %	4.83 %	4.68 %	4.82 %	4.86 %	4.66 %	4.39 %
	Transient	25.06 %	4.94 %	4.73 %	4.88 %	4.91 %	4.74 %	4.60 %

Real and Reactive power analysis: The shunt APLC improves the power factor in the considered power system. Fig.5.16 shows the power factor correction, it indicates that A-phase voltage and current are in phase.

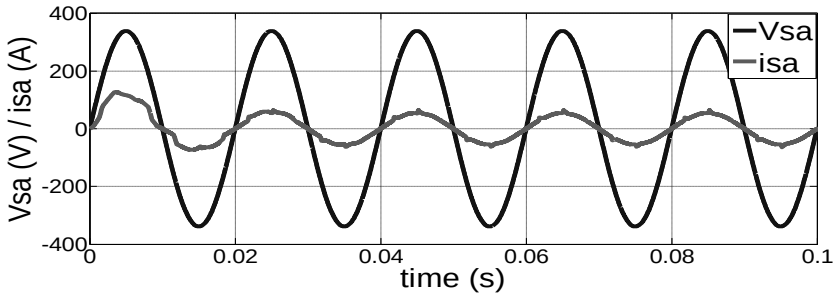


Fig.5.16 Unity power factor

The real and reactive power is calculated under diode / thruster-rectifier load and it is given in Table 5.4. This result indicates fryze power theory with TCCC / TPCC / SVM / fixed-HCC / adaptive-HCC / adaptive-fuzzy-HCC based active power line conditioner is suppressing reactive power and hence improving the power factor in particular and power quality in general.

Table 5.4 Real (P) and Reactive (Q) power measurements

Rectifier RL Loads	Without APLC	With APLC				
		TPCC	SVM	F-HCC	A-HCC	A-F-HCC
Diode	P=8.99 kW Q=239 VAR	P=9.31 kW Q=76 VAR	P=9.37 kW Q=56 VAR	P=9.29 kW Q=78 VAR	P=9.31 kW Q=78 VAR	P=9.53 kW Q=35 VAR
Thyristor	P=8.74 kW Q=250 VAR	P=9.02 kW Q=87 VAR	P=9.07 kW Q=127 VAR	P=8.99 kW Q=56 VAR	P=9.12 kW Q=67 VAR	P=9.25 kW Q=53VAR

Remarks: The fryze power theory with various PWM-current controller based active power line conditioner system is simulated and compensation principle is confirmed. The adaptive-fuzzy-HCC reduces the switching power losses and improves the active power line conditioner performance compared to other techniques. From these results, it is evident that the THD of the source current is in compliance with harmonic current standards.

5.4. Proposed instantaneous real-power theory

The performance of the conventional p-q theory and proposed instantaneous real-power theory with various PWM-current controller based shunt APLC system is evaluated through Matlab / Simpower tools. The APLC consists of power inverter, interface-filter, a reference current extraction controller (instantaneous real-power theory) and switching pulse generator as shown in Fig.5.17. The instantaneous real-power theory is used to extract the required reference current from the distorted load current. The reference current is compared with actual current to generate the switching pulses using TCCC / TPCC / SVM / fixed-HCC / adaptive-HCC / adaptive-fuzzy-HCC techniques to drive the active power inverter. The active power line conditioner provides the required compensating current to compensate current harmonics and reactive-power in the distributed system. This system is tested under diode and thyristor-rectifier load with steady-state and transient conditions.

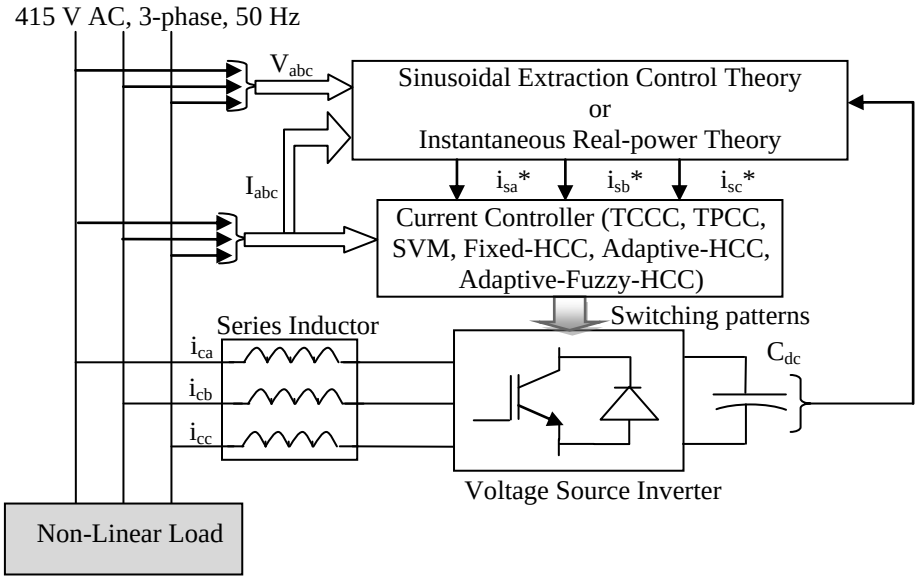


Fig.5.17 Instantaneous real-power theory / Sinusoidal extraction controller based shunt APLC system

5.4.1. Case 1 TCCC, TPCC and SVM

Conventional p-q theory with TCCC / TPCC / SVM current controller based active power line conditioner system is simulated and investigated under diode / thyristor-rectifier load. The simulation is conducted under diode-rectifier load with the steady-state condition. Fig.5.18 (a) shows the source current before compensation. It

comprises fundamental current components and harmonic current components. To compensate harmonic current components, the active power line conditioner provides the required compensating current as shown in Fig.5.18 (b). Consequently, the harmonic current compensation is achieved by injecting equal but opposite harmonic components. Fig.5.18 (c) shows the source current after APLC compensation which is sinusoidal in nature.

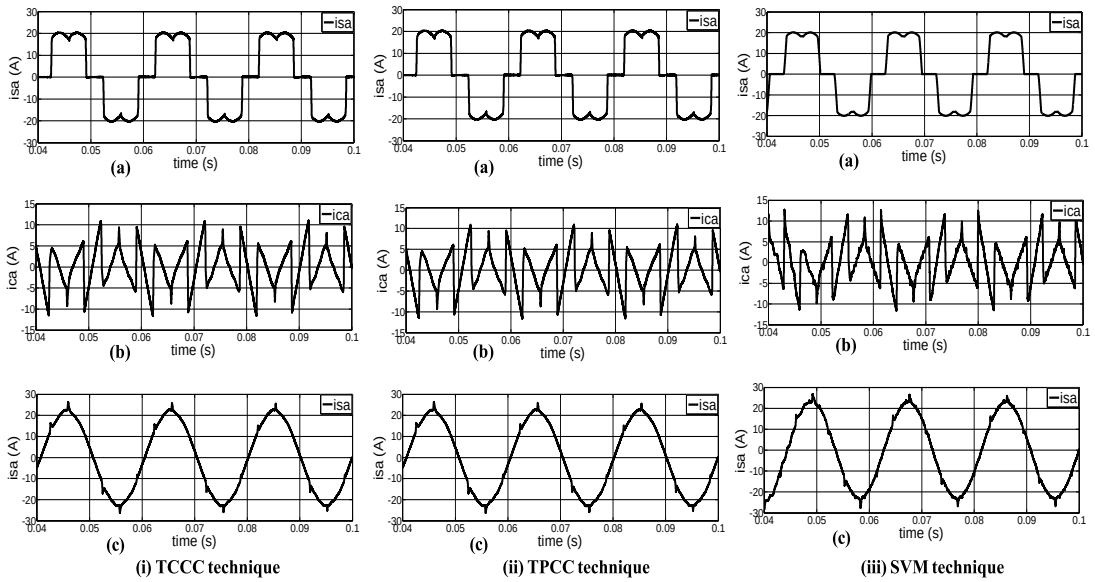


Fig.5.18 Simulation waveforms of (a) Source current before compensation, (b) Compensation current and (c) Source current after compensation

5.4.2. Case 2 Fixed-HCC and adaptive-HCC

Fig.5.19 (i) and (ii) is obtained using instantaneous real-power theory with fixed-HCC and adaptive-HCC respectively. To study transient-state behavior, the load is suddenly changed at 0.06 s. Fig.5.19 (a) shows the source current before compensation under diode-rectifier load. It contains fundamental and harmonic components due to the non-linear load. The fixed / adaptive-HCC is used to generate the switching pulses to drive the PWM-inverter. The inverter provides the compensating current as shown in Fig.5.19 (b) to compensate the harmonic components. The harmonic compensation is achieved by injecting equal but opposite harmonic components. Fig.5.19 (c) shows the source current after compensation and is sinusoidal in nature.

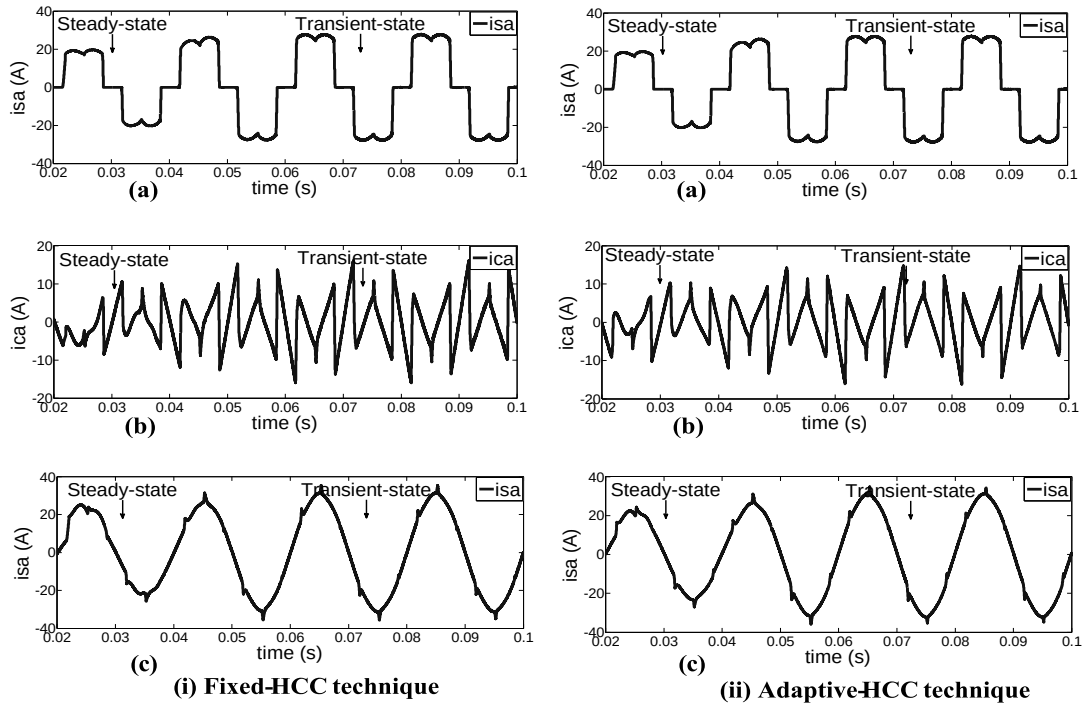


Fig.5.19 Simulation waveforms of (a) Source current before APLC compensation, (b) Compensation current and (c) Source current after APLC compensation

5.4.3. Case-3 Adaptive-fuzzy-HCC

Fig.5.20 (i) and (ii) show instantaneous real-power theory with adaptive-fuzzy-HCC based active power line conditioner system under steady-state and transient-state. Fig.5.20 (a) shows the instantaneous supply voltages which indicate the three-phase voltages are balanced. Fig.5.20 (b) shows the instantaneous source currents before compensation that contains fundamental as well as harmonic components due to thyristor-rectifier load. Fig.5.20 (c) shows the reference currents, which is generated from the distorted line currents using the proposed instantaneous real-power theory. The reference currents compared with actual currents and generate switching pulses using adaptive-fuzzy-HCC to operate the active power line conditioner. The APLC provides the required compensation current as shown in Fig.5.20 (d). The APLC compensates harmonic current components by injecting equal-but-opposite harmonic current components. It operates as current source injecting the harmonic current components generated by the thyristor-rectifier load but phase shifted by 180^0. As a result, components of harmonic currents contained in the load currents are cancelled by the effect of the active power line conditioner.

Fig.5.20 (e) shows the source currents after compensation and indicates that the source currents after compensation is sinusoidal and in phase with the supply voltages.

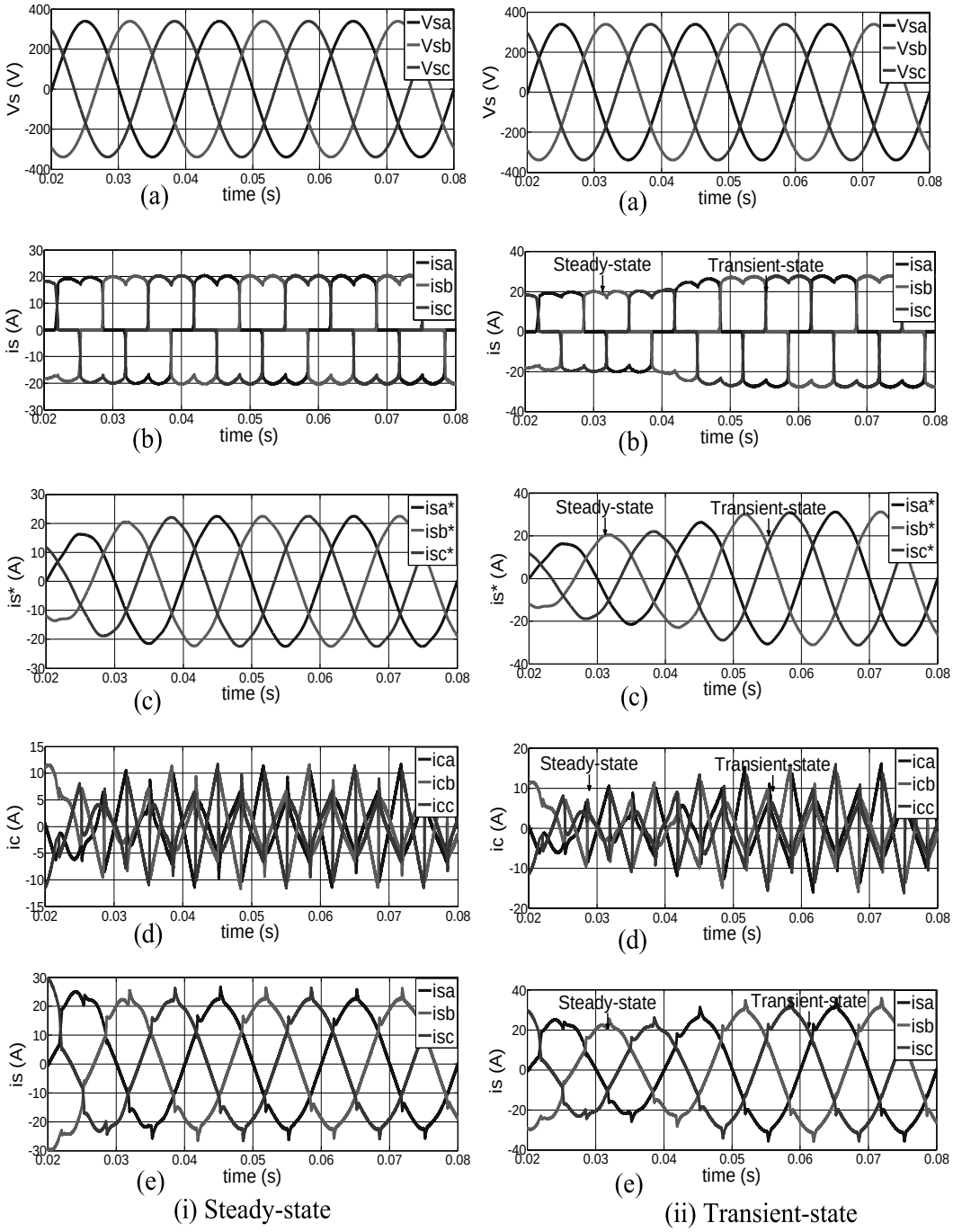


Fig.5.20 Simulation waveforms of (a) Supply voltages, (b) Source currents before compensation, (c) Reference currents, (d) Compensation currents and (e) Source currents after compensation

5.4.4. Case 4 APLC system analysis

dc-link capacitor voltage: The dc-link capacitor voltage of the voltage source inverter is controlled by the PI - controller. Fig.5.21 shows the waveform of the dc-link voltage and ensures it is nearly constant, which is required to supply the voltage source inverter.

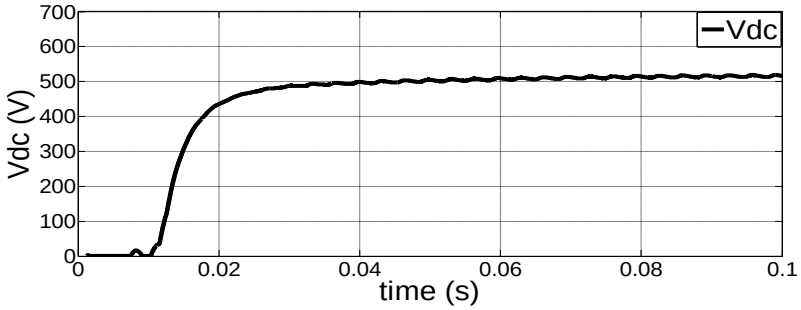


Fig.5.21 dc-link capacitor voltage settling time

THD analysis: The order of the harmonics versus magnitude in source current is plotted without / with APLC under diode / thyristor-rectifier load. Fig.5.22 (a) and (b) is obtained using instantaneous real-power theory with adaptive-fuzzy-HCC based active power line conditioner under diode-rectifier load. Without-APLC the supply current is distorted due to the presence of fifth, seventh, eleventh and higher order of harmonic spectral components. The measurement of THD is 26.66 % and 24.87 % under steady state and transient respectively. With-APLC the order of harmonics is reduced to less than 5% (THD=3.98 % in steady-state and 3.56 % in transient).

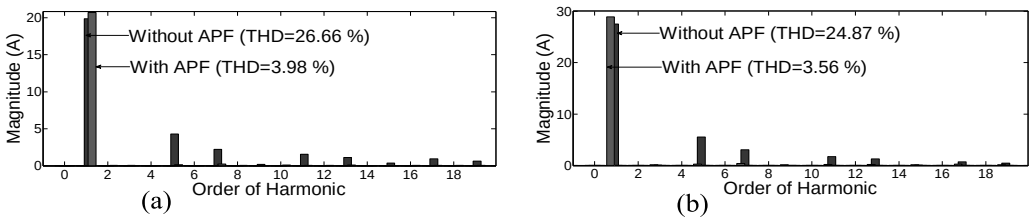


Fig.5.22 Order of harmonics (a) Steady-state and (b) Transient-state

The FFT is used to measure the order of harmonics in the source current. The THD of the source current is measured without and with active power line conditioner using conventional *p-q* theory and instantaneous real-power *(p-theory)* theory along with different PWM-current controllers that is presented in Table 5.5.

Table 5.5 THD measurements

Rectifier Load	Condition	Harmonic controller	Without APLC	With APLC					
				TCCC	TPCC	SVM	F-HCC	A-HCC	A-F-HCC
Diode	Steady	p-q theory	26.66 %	4.42 %	4.38 %	4.25 %	4.24 %	4.18 %	4.11 %
		p-theory		4.36 %	4.30 %	4.10 %	4.13 %	4.08 %	3.98 %
	Transient	p-q theory	24.87 %	4.43 %	4.32%	4.37 %	4.14 %	3.95 %	3.81 %
		p-theory		4.25 %	4.14 %	4.22 %	3.97 %	3.74 %	3.56 %
Thyristor	Steady	p-q theory	26.79 %	4.69 %	4.55 %	4.32%	4.23 %	4.14 %	4.08 %
		p-theory		4.57 %	4.22 %	4.02 %	4.11 %	4.06 %	3.94 %
	Transient	p-q theory	25.06 %	4.46 %	4.29%	4.34 %	4.23 %	4.10 %	3.82 %
		p-theory		4.34 %	4.06 %	4.29 %	4.14 %	3.97 %	3.66 %

The shunt APLC improves the power factor in the connected power system. Fig.5.23 shows the power factor correction, it indicates that A-phase voltage and current are in phase.

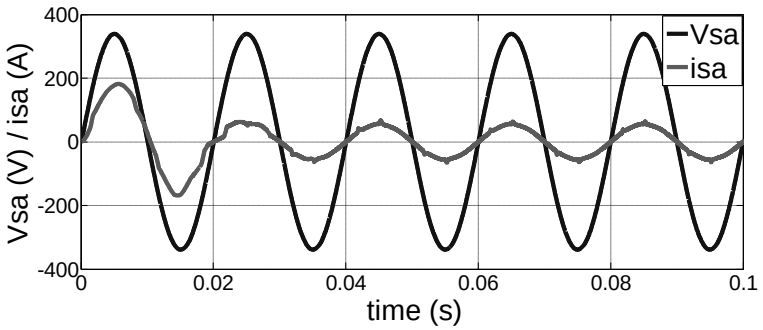


Fig.5.23 Unit power factor

The real and reactive power is measured and shown in Table 5.6. This result indicates that the instantaneous real-power theory with various PWM-current controllers based active power line conditioner is suppressing reactive power and hence improving the power quality.

Table 5.6 Real (P) and Reactive (Q) power measurements

Rectifier RL Load	Harmonic controller	Without APLC	With APLC			
			SVM	F-HCC	Adaptive-HCC	Adaptive-Fuzzy-HCC
Diode	p-q theory	P=8.99 kW Q=239 VAR	P=9.45 kW Q=69 VAR	P=9.27 kW Q=93 VAR	P=9.41 kW Q=80 VAR	P=9.48 kW Q=76 VAR
	p-theory		P=9.68 kW Q=10 VAR	P=9.45 kW Q=33 VAR	P=9.61kW Q=38 VAR	P=9.79 kW Q=30 VAR
Thyristor	p-q theory	P=8.74 kW Q=250 VAR	P=8.97 kW Q=98 VAR	P=9.08 kW Q=89 VAR	P=9.11 kW Q=83 VAR	P=9.31 kW Q=103 VAR
	p-theory		P=9.18 kW Q=29 VAR	P=9.15 kW Q=66 VAR	P=9.37 kW Q=19 VAR	P=9.49 kW Q=76 VAR

Remarks: The instantaneous reactive-power theory with various PWM-current control techniques based active power line conditioner system is simulated and compensation principle is validated under diode / thyristor rectifier load. The result indicates the projected controller based active power line conditioner performs quite well and compensates for both harmonic currents as well as reactive-power. The FFT analysis of the active power line conditioner confirms the THD of the source current is less than 5 %.

5.5. Proposed sinusoidal extraction control strategy

The performance of the sinusoidal extraction control with various PWM-current control techniques based shunt APLC system is evaluated through Matlab / Simulink power tools. The system is simulated in a similar way as the instantaneous real-power theory based APLC system under distorted supply voltage. Fig.5.24 is obtained using the sinusoidal extraction control with adaptive-fuzzy-HCC based active power line conditioner system under steady-state. Fig.5.24 (a) shows the instantaneous supply voltages and indicated the supply voltages are distorted. The proposed sinusoidal extraction control strategy consists of a positive sequence voltage detector to generate the balanced sinusoidal voltages from the unbalanced or distorted supply voltages, and the instantaneous real-power theory to extract the reference currents.

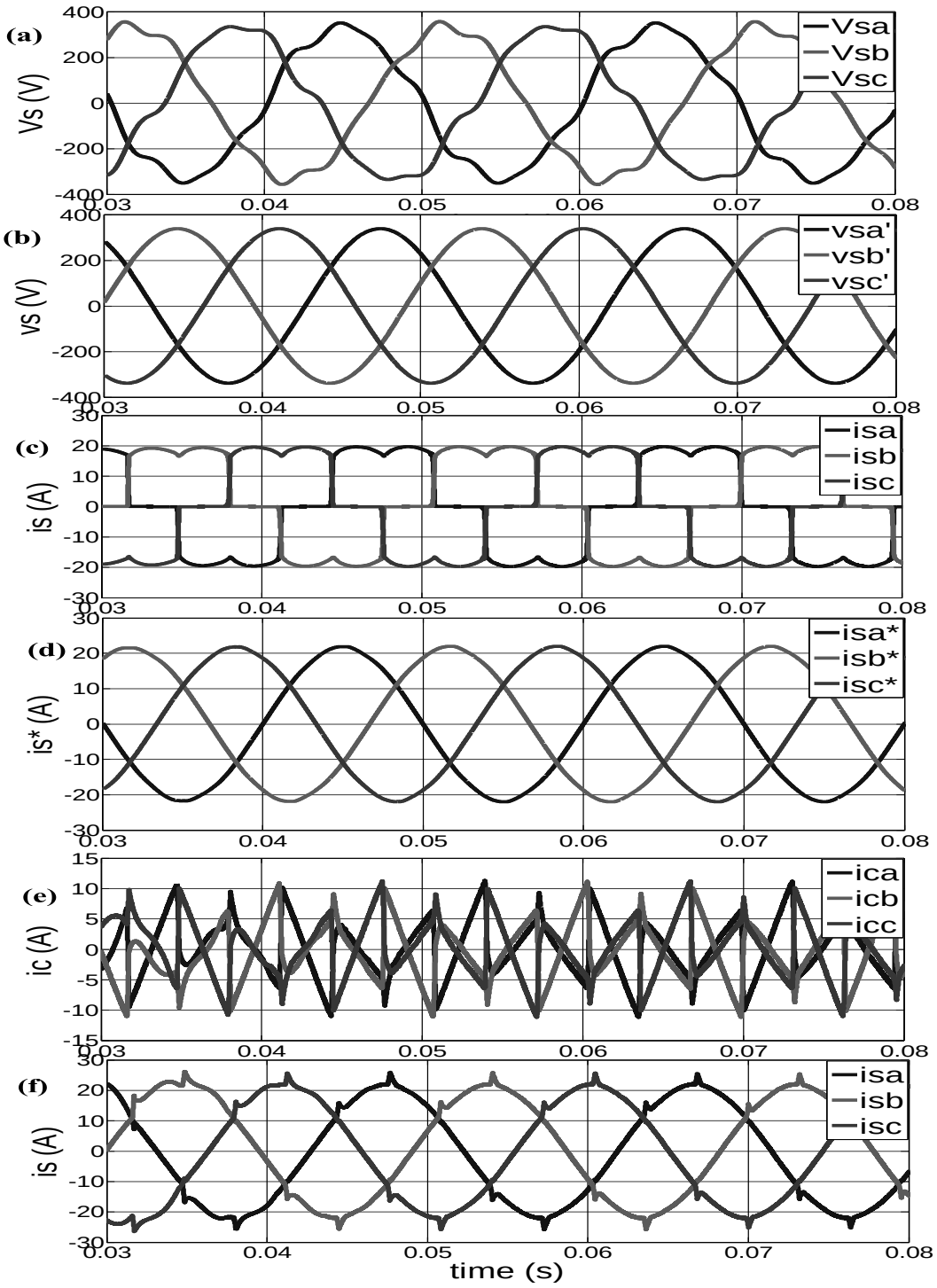


Fig.5.24 (a) Distorted supply voltages, (b) Balanced supply voltages, (c) Source currents before APLC, (d) Reference currents, (e) Compensation currents and (f) Source currents after APLC

Fig.5.24 (b) shows the balanced sinusoidal voltages that are generated from the distorted supply voltages by using the positive sequence voltage detector. Fig.5.24 (c) shows the instantaneous source currents before compensation that contains

fundamental as well as harmonic components due to thyristor-rectifier load. The reference currents are extracted from the distorted line currents using the sinusoidal extraction control method as shown in Fig.5.24 (d). The reference currents compared with actual currents and generate switching pulses using adaptive-fuzzy-HCC (or TCCC / TPCC / SVM / fixed-HCC / adaptive-HCC) to operate the active power line conditioner. The APLC provides the compensation currents as shown in Fig.5.24 (e). The APLC compensates harmonic current components by injecting equal-but-opposite harmonic current components. It operates as current source injecting the harmonic current components generated by the load but phase shifted by 180^0. As a result, components of harmonic currents in the load current are cancelled by the effect of the APLC. Fig.5.24 (f) shows the source currents after compensation and indicates the source currents after compensation are sinusoidal and it is in phase with the respective phase voltages.

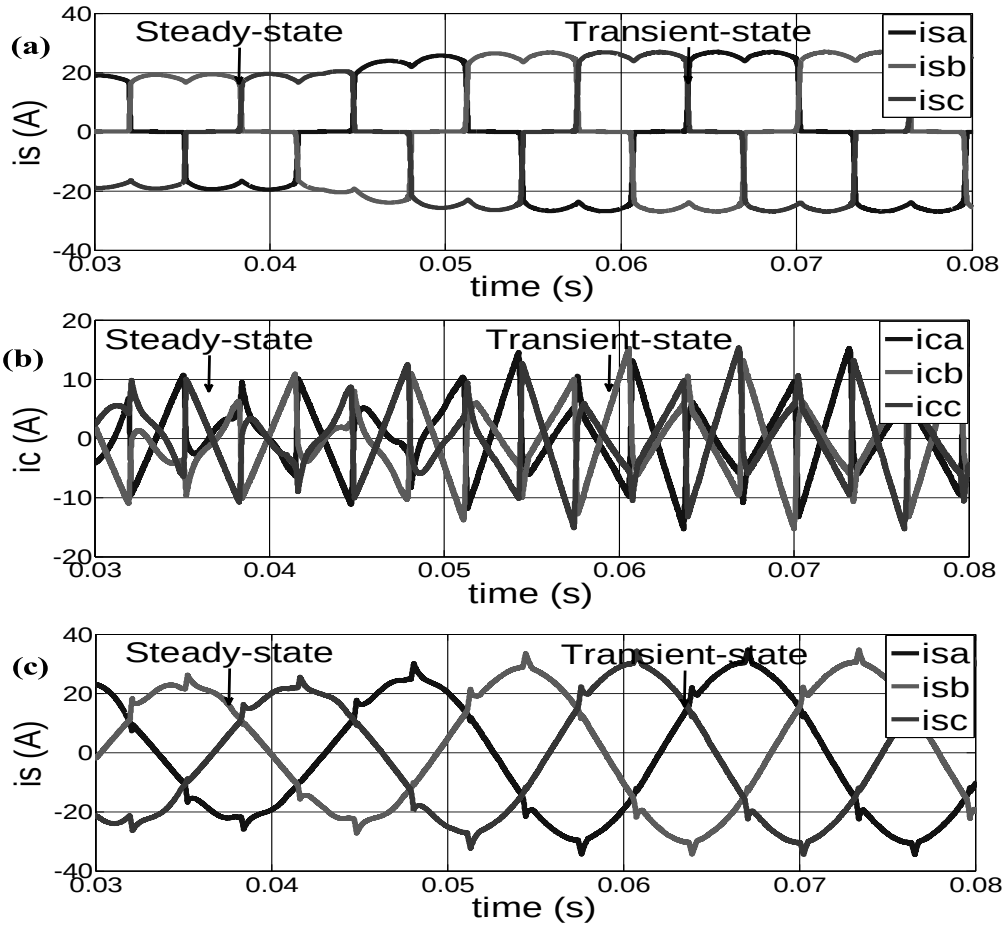


Fig.5.25 Simulation waveforms of (a) Source currents before compensation, (b) Compensation currents and (c) Source currents after compensation

Fig.5.25 is obtained using the sinusoidal extraction control with adaptive-fuzzy-HCC based APLC system under transient-state. Fig.5.25 (a) shows the instantaneous source currents before compensation, which consist fundamental as well as harmonic components due to thyristor-rectifier load. To compensate harmonic components, the APLC provides the compensating currents as shown in Fig.5.25 (b). The APLC compensates harmonic current components by injecting equal-but-opposite harmonic current components. As a result, components of harmonic currents contained in the load current are cancelled by the effect of the active power line conditioner. Fig.5.25 (c) shows the source currents after compensation and indicates the source currents after compensation are sinusoidal and is in phase with the respective voltages.

5.5.1. APLC system analysis

The sinusoidal extraction controller with different PWM-current controller based APLC system measures the order of the harmonics at the source current for diode / thyristor-rectifier load. Without-APLC the supply current is distorted due to the harmonic spectral components and with-APLC the THD is reduced to a value which is less than 5 %. The THD measurement is compared with TCCC, TPCC, SVM, fixed-HCC, adaptive-HCC and adaptive-fuzzy-HCC that is presented in Table 5.7.

Table 5.7 THD measurements

Rectifier RL Loads	Condition	Without APLC	With APLC					
			TCCC	TPCC	SVM	HCC	A-HCC	A-F-HCC
Diode	Steady state	26.66 %	4.29 %	4.26 %	3.92 %	3.97 %	3.85 %	3.81 %
	Transient	24.87 %	4. 25%	3.86 %	3.93 %	3.96 %	3.76 %	3.69 %
Thyristor	Steady state	26.79 %	4.38 %	4.21 %	3.98 %	4.07 %	3.94 %	3.83 %
	Transient	25.06 %	4. 23%	3.95 %	4.08 %	4.11 %	3.81 %	3.77 %

Remarks: The sinusoidal extraction controller with TCCC / TPCC / SVM / fixed-HCC / adaptive-HCC / adaptive-fuzzy-HCC based active power line conditioner system is simulated. The sinusoidal extraction controller with adaptive-fuzzy-HCC

performs better compared to other current control techniques. From the results, the active power line conditioner ensured that the current harmonics and reactive-power has been compensated.

5.6. Synchronous reference frame theory

The conventional and proposed modified-SRF based shunt active power line conditioner system is modeled and evaluated through Matlab / Simpower tools. The model system consists of three-phase voltage source inverter and connected through the interface inductor in parallel with rectifier load as shown in Fig.5.26. The APLC controller uses the conventional / modified-SRF with various PWM-current control techniques. The conventional or modified-SRF is used to extract the required reference currents from the distorted load currents. The reference currents are compared with actual currents to generate the switching pulses using PWM-current controller (TCCC / TPCC / SVM / fixed-HCC / adaptive-HCC / adaptive-fuzzy-HCC techniques) to drive the active power line conditioner. The APLC provides the essential compensating current to compensate current harmonics and reactive-power in the connected system. This system is demonstrated under diode and thyristor-rectifier load with steady-state and transient conditions.

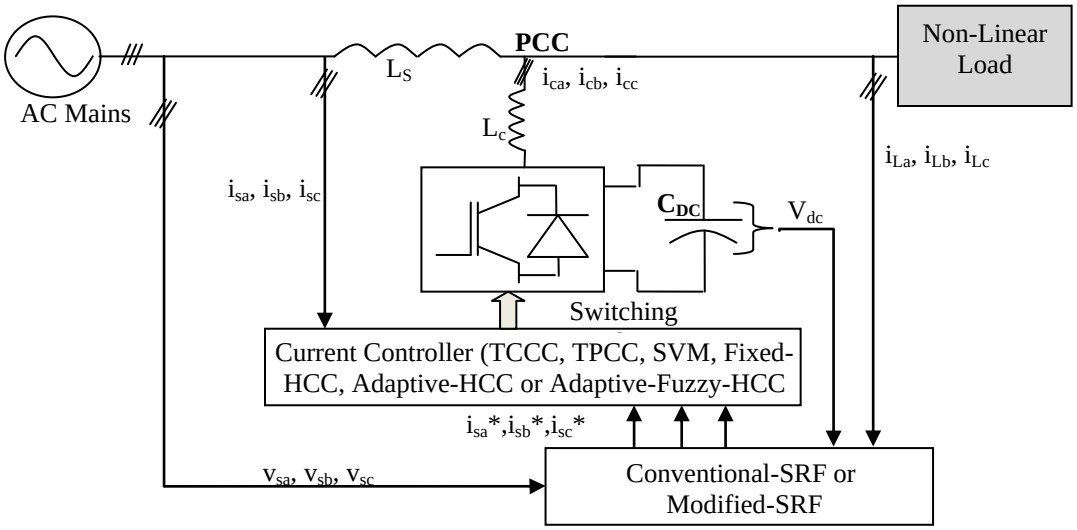


Fig.5.26 Conventional / Modified-SRF controller based shunt APLC system

5.6.1. Case-1 conventional-SRF

Fig.5.27 shows the TCCC / TPCC / SVM techniques under diode-rectifier load with the steady-state condition. Fig.5.27 (a) shows the source current before compensation. It indicates the source current contains fundamental and harmonic current components. To compensate harmonic current components, the APLC supplies the compensating current as shown in Fig.5.27 (b). Consequently, the harmonic current compensation is achieved by injecting equal but opposite harmonic components. Fig.5.27 (c) shows the source current after compensation. It indicates the source current after the compensation becomes sinusoidal.

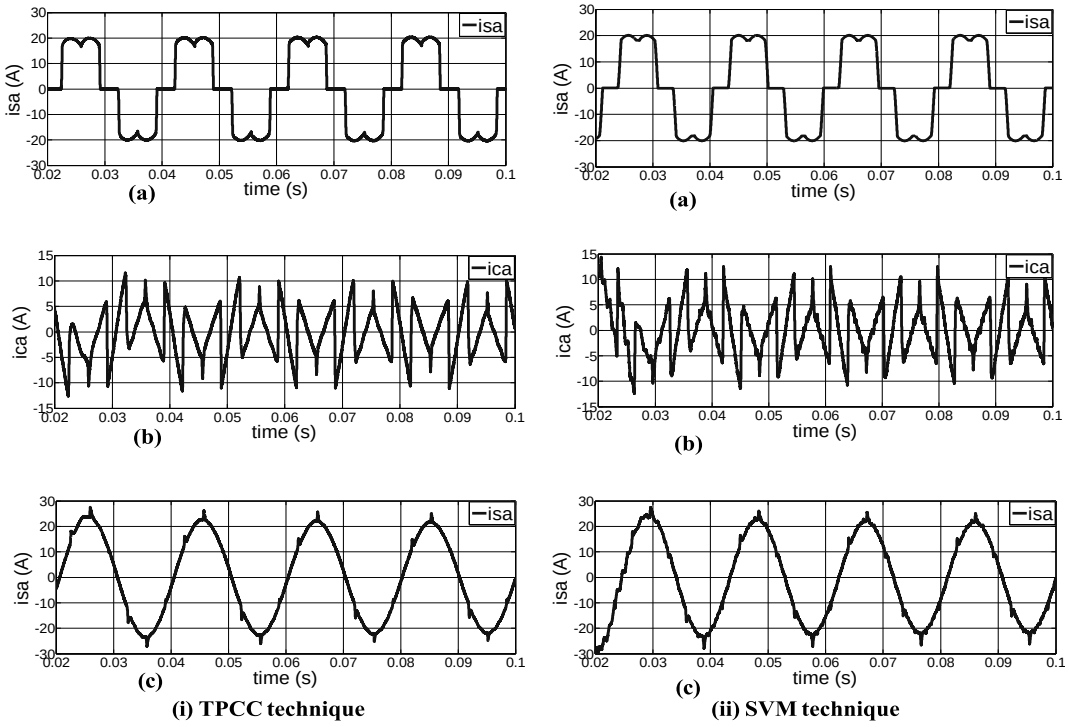


Fig.5.27 Simulations waveforms of (a) Source current before compensation, (b) Compensation current (c) Source current after compensation using TPCC, SVM and adaptive-HCC respectively

5.6.2. Case-2 proposed modified-SRF

Fig.5.28 (i) and (ii) are obtained using proposed modified-SRF with adaptive-fuzzy-HCC based shunt APLC system under steady-state and transient-state respectively. Fig.5.28 (a) shows the instantaneous supply voltages and indicates the three-phase voltages are balanced. Fig.5.28 (b) shows the source currents before compensation that contains fundamental and harmonic components due to thyristor-rectifier load.

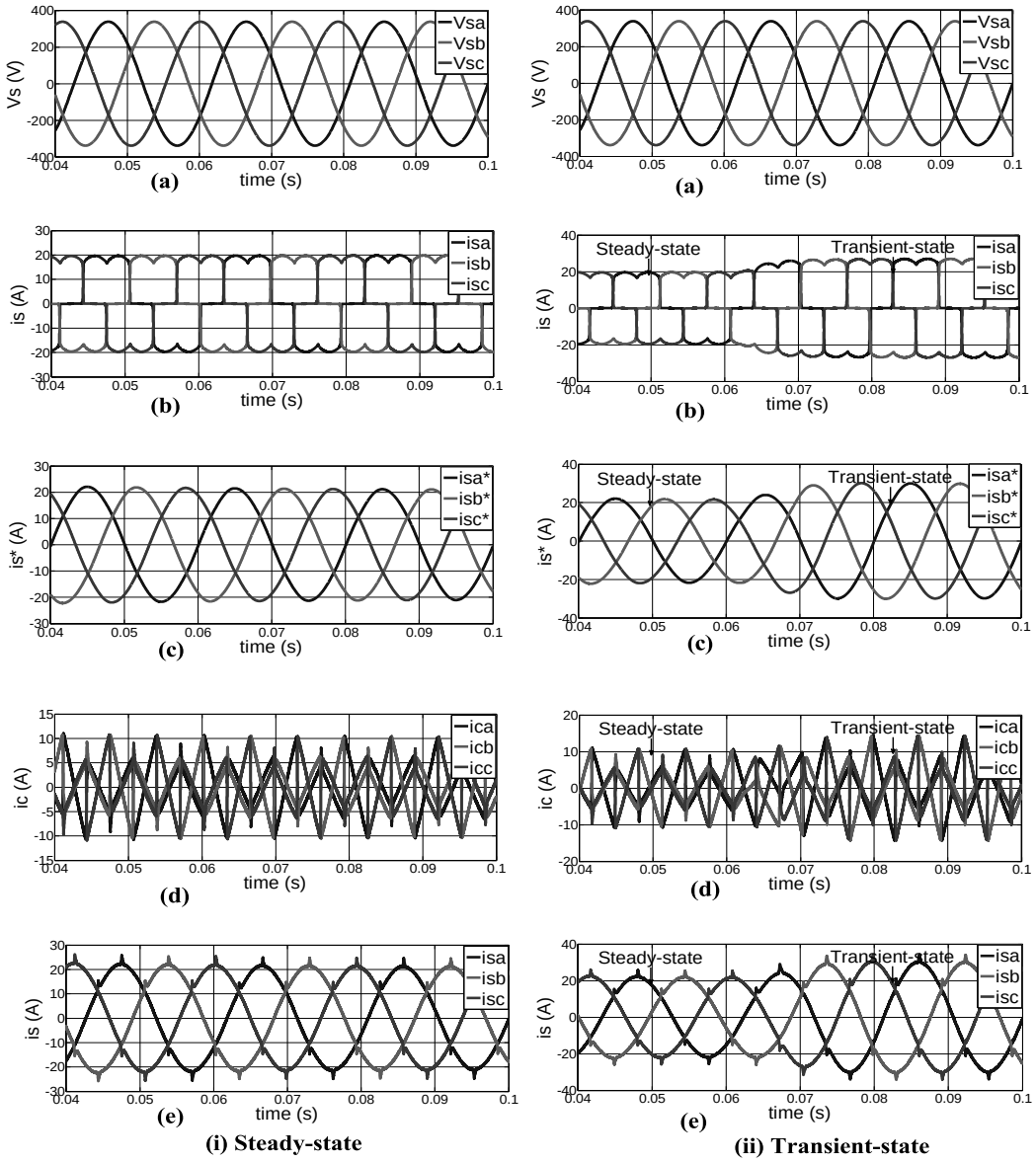


Fig.5.28 Simulation waveforms of (a) Steady-state (b) Transient-state

Fig.5.28 (c) shows the reference currents, which is extracted from the distorted load current using the modified-SRF method. The reference currents compared with actual currents and generate switching pulses using adaptive-fuzzy-HCC (or various current control methods) to operate the APLC. The APLC provides the necessary compensating currents as shown in Fig.5.28 (d), it compensates harmonic current components by injecting equal-but-opposite harmonic components. The APLC operates as current source injecting the harmonic current components generated by the load but phase shifted by 180^0. As a result, components of harmonic currents in the load currents are cancelled by the effect of the APLC. Fig.5.28 (e) shows the

source currents after compensation and indicates the source currents after compensation are sinusoidal and in-phase with the supply voltages.

5.6.3. Case-3 APLC system analysis

The active power line conditioner is analyzed in terms of V_{dc} settling time, order of harmonic compensation, real and reactive power calculation.

dc-link capacitor voltage: The APLC, during normal operation draws only a small amount of active power from grid to maintain the dc-link capacitor voltage at the required level, and to supply for the switching loss as well as conduction loss. The dc-voltage of the inverter is controlled and maintained constant by propositional and integral gains. Fig.5.29 shows the waveform of the dc-voltage and ensures it is nearly constant, which is essential in order to supply the PWM-inverter.

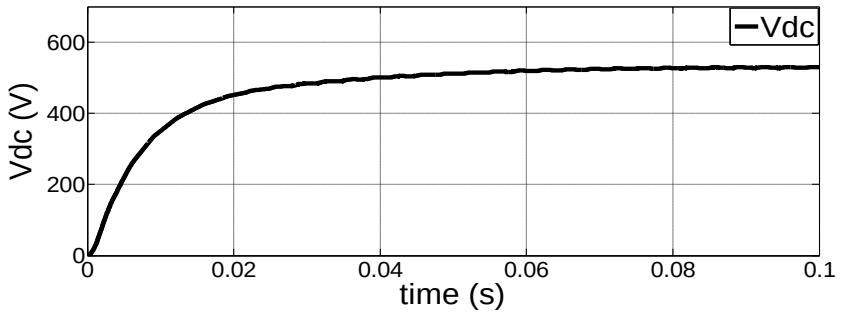


Fig.5.29 dc-link capacitor voltage

THD analysis: The modified-SRF with adaptive-fuzzy-HCC based active power line conditioner has facilitated the harmonic current compensation at the PCC. Fig.5.30 (a) and (b) illustrate plots of the order of harmonics versus magnitude in source current without and with APLC. Without-APLC the THD is 26.79 % and 25.06 % under the thyristor-rectifier load in both steady-state and transient respectively. With-APLC the order of harmonics is reduced to less than 5% (THD=3.54 % in steady-state and 3.37 % in transient).

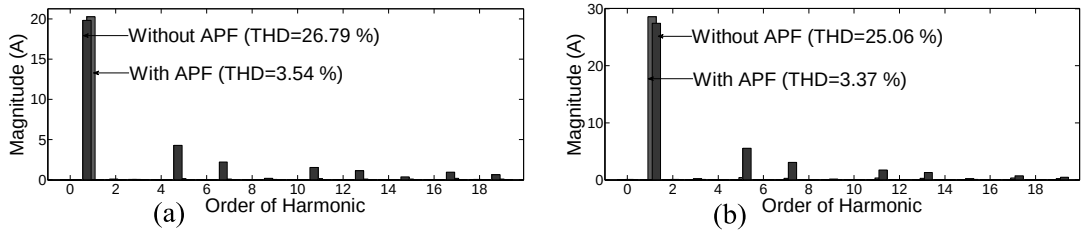


Fig.5.30 Order of harmonics (a) Steady-state and (b) Transient-state

The FFT is used to measure the order of harmonics. The THD of the source current is measured without-APLC and with-APLC using conventional and modified-SRF method along with different PWM-current controllers that is presented in Table 5.8.

Table 5.8 THD measurements

Rectifier Load	Condition	controller	Without APLC	With APLC					
				TCCC	TPCC	SVM	F-HCC	A-HCC	A-F-HCC
Diode	Steady	SRF	26.66 %	4.34 %	4.11 %	4.25 %	4.54 %	3.92 %	3.87 %
		M-SRF		4.25 %	3.96 %	4.15 %	4.37 %	3.74 %	3.58 %
	Transient	SRF	24.87 %	3.98 %	3.72 %	3.80 %	3.84 %	3.75 %	3.61 %
		M-SRF		3.77 %	3.53 %	3.62 %	3.78 %	3.44 %	3.26 %
Thyristor	Steady	SRF	26.79 %	4.69 %	4.55 %	4.62%	4.73 %	4.54 %	3.73 %
		M-SRF		4.51 %	4.32 %	4.38 %	4.61 %	4.26 %	3.54 %
	Transient	SRF	25.06 %	4.66 %	4. 49%	4.64 %	4.53 %	4.40 %	3.62 %
		M-SRF		4.43 %	4. 20%	4.39 %	4.35 %	4.28 %	3.37 %

Real and reactive Power: The shunt APLC improves the power factor in the connected power system. Fig.5.31 shows the power factor correction, it indicates the A-phase voltage and current are in phase.

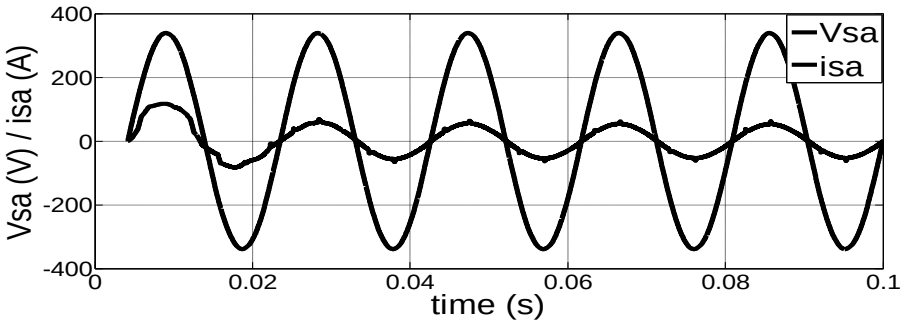


Fig.5.31 Unit power factor

The real and reactive-power is measured under diode / thyristor-rectifier load and is given in Table 5.9. This result indicates conventional and modified-SRF with various PWM-current controller based active power line conditioner is suppressing reactive-power and improving the power quality.

Table 5.9 Real (P) and Reactive (Q) power measurements

Rectifier RL Load	controller	Without APLC	With APLC			
			SVM	F-HCC	Adaptive-HCC	Adaptive-Fuzzy-HCC
Diode	SRF	P=8.99 kW Q=239 VAR	P=9.11 kW Q=132 VAR	P=9.14 kW Q=126 VAR	P=9.22 kW Q=104 VAR	P=9.33 kW Q=86 VAR
	M-SRF		P=9.25 kW Q=106 VAR	P=9.21 kW Q=112 VAR	P=9.32 kW Q=102 VAR	P=9.54 kW Q=58 VAR
Thyristor	SRF	P=8.74 kW Q=250 VAR	P=8.98 kW Q=116 VAR	P=8.86 kW Q=152 VAR	P=9.11 kW Q=108 VAR	P=9.43 kW Q=77 VAR
	M-SRF		P=9.07 kW Q=106 VAR	P=8.97 kW Q=116 VAR	P=9.37 kW Q=89 VAR	P=9.82 kW Q=31 VAR

Remarks: The conventional / modified-SRF with various PWM-current control techniques based active power line conditioner system is simulated and validated. From the results, the modified-SRF is giving better performance than conventional-SRF method in terms of V_{dc}-settling time, harmonic current as well as reactive-power compensation.

5.7. Conclusions

The shunt active power line conditioner system is modeled and evaluated through Matlab / Simpower tools. PI / PID / FLC / PI-FLC, fryze power theory, instantaneous real-power theory, sinusoidal extraction controller conventional-SRF and modified-

SRF methods have been applied to extract the reference currents. Similarly, TCCC, TPCC, SVM, fixed-HCC, adaptive-HCC and adaptive-fuzzy-HCC techniques are computed to generate the switching pulses of the inverter. These simulation results reveal that the active power line conditioner is compensating current harmonics as well as reactive-power. The comparison results of the THD and real and reactive-power measurements are presented in the tabular form. From the simulation, the instantaneous real-power and modified-SRF methods with adaptive-fuzzy-HCC provides better performance. The measured THD of the source currents is less than 5 % which is in compliance with IEEE 519 and IEC 61000-3 harmonic standards.

CHAPTER 6

EXPERIMENTAL RESULTS AND ANALYSIS

6.1. Introduction

This chapter presents the hardware set-up and experimental verification of three-phase shunt active power line conditioner system. The main objective is to demonstrate the arrangement of two-level voltage source inverter based active power line conditioner for harmonic and reactive-power compensation. The performance of the active power line conditioner depends on (i) reference current extraction method and (ii) PWM-VSI current controller. In chapter 3, some of the reference current extraction methods are discussed. In chapter 4, different PWM-current control methods to generate the switching pulses of the inverter are presented. In chapter 5, the simulation results and analysis of the various active power line conditioner controllers under diode / thyristor-rectifier loads has been discussed. From the simulation results, it has been demonstrated that instantaneous real-power theory and modified-SRF with adaptive-fuzzy-HCC method provides better performance in terms of compensation of harmonics as well as reactive-power while using simple algebraic calculation. For experimental verification we conducted the performance of APLC for the following control strategies.

- Modified-SRF with SVM technique
- Modified-SRF with adaptive-fuzzy-HCC technique

Modified-SRF control method is used for reference current extraction from the distorted load current. The modified-SRF uses simple and efficient method to calculate the unit vector for vector orientation. The SVM technique and adaptive-fuzzy-HCC is applied to generate the required switching pulses to drive the PWM-inverter. The control algorithm is implemented through TMS320F240DSP for active power line conditioner system.

Furthermore, we also take up the study of the FPGA controller for three-phase active power line conditioner using Matlab / system generator and ISE-Xilinx. The objective is to demonstrate how the control circuit could be simplified by the use of

FPGAs. The FPGA controller is validated for proposed instantaneous real-power theory with adaptive-fuzzy-HCC.

6.2. Experimental setup

In chapter 2, the design of the active power line conditioner (power devices, capacitor and interface inductor selection) has been discussed. This section proceeds the implementation of the active power line conditioner for compensating harmonics and reactive-power at PCC. The modified-SRF method with SVM technique and adaptive-fuzzy-HCC is validated using this experimental setup. The SVM technique is used as direct current control approach, whereas the adaptive-fuzzy-HCC is used as an indirect current control approach for generating the PWM-switching pulses. For the prototype model of the active power line conditioner system, the following components and devices are used. The exact specifications as well as the values of the components used in the simulation and experiment are mentioned in Appendix-A.

6.2.1. Thyristor-rectifier load

The three-phase variable transformer is used to set the voltage level according to the load condition. For experimental verification, the line-to-line voltage 360 V / 50 Hz is considered for three-phase shunt active power line conditioner. A three-phase thyristor-rectifier load is connected to the power system for harmonic testing. The thyristor rectifier load is constructed using SKKT57B16E device. The thyristor turns ON using micro controller based synchronized pulse generator circuit.

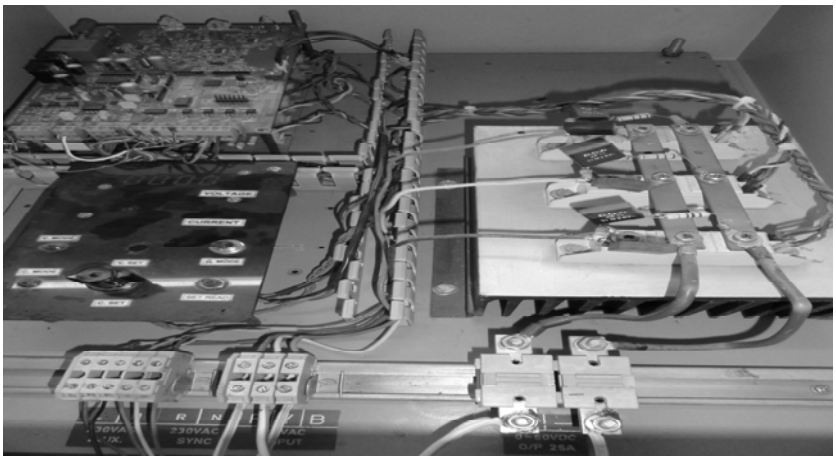


Fig.6.1 Photograph of thyristor-rectifier load

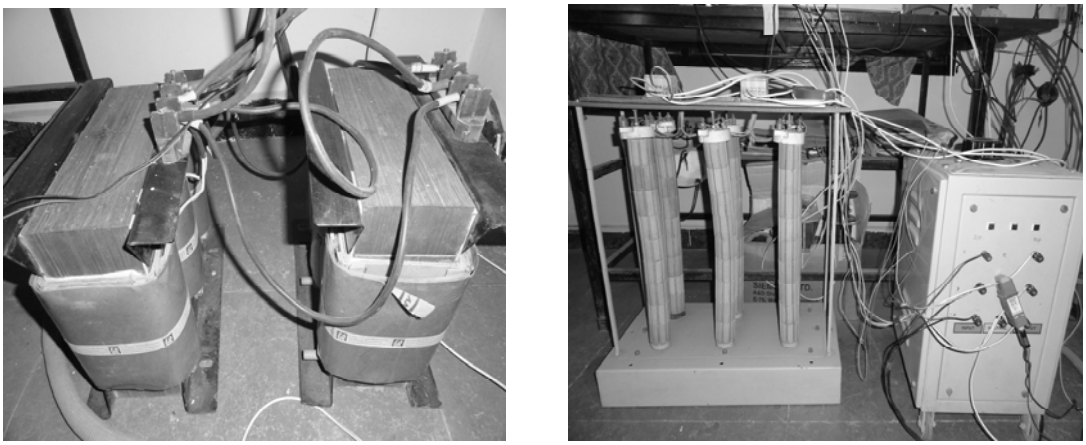


Fig.6.2 Photograph of inductor and resistor load

Fig.6.1 shows the photograph of the thyristor-rectifier circuit along with synchronized pulse generator circuit. The thyristor-rectifier load is connected with 10 Ω resistors for harmonic testing. The thyristor generates six-pulse rectifier load, which contains 5^{th}, 7^{th} and higher order harmonic current components. To test the reactive-power compensation, inductor (10 mH) load is used which is connected in parallel with active power line conditioner at PCC. Fig.6.2 shows the photograph of the inductor and resistor load.

6.2.2. Voltage source inverter

The selection of IGBT (switching power transistor) is based on the supply voltage as well as the maximum dc-link capacitor voltage and peak value of rated current which it is supposed to carry during ON state. The power circuit comprises with IGBTs of power rating of 1200 V / 200 Amp and switching frequency (maximum) of 10 kHz. According to this requirement FF200R12KE3 power component is selected, which is dual IGBT with anti-parallel diode package. The device is mounted on the heat sink compound, which provides thermal conduction between the IGBT device and the heat sink. Fig.6.3 (a) shows the photograph of the two-level voltage source inverter with the gate driver circuit. The interface inductors should be selected at a lower flux density. It provides enough ventilation between the conductor and core of the inductor. This is derived using the voltage drop across the inductor and expected the current to flow at required angular frequency. This interface inductor is calculated

to be L=1.8 mH. Fig.6.3 (b) shows the photograph of the interface-inductor and pre-charger, which is used to charge the dc-link capacitor of the voltage source inverter.

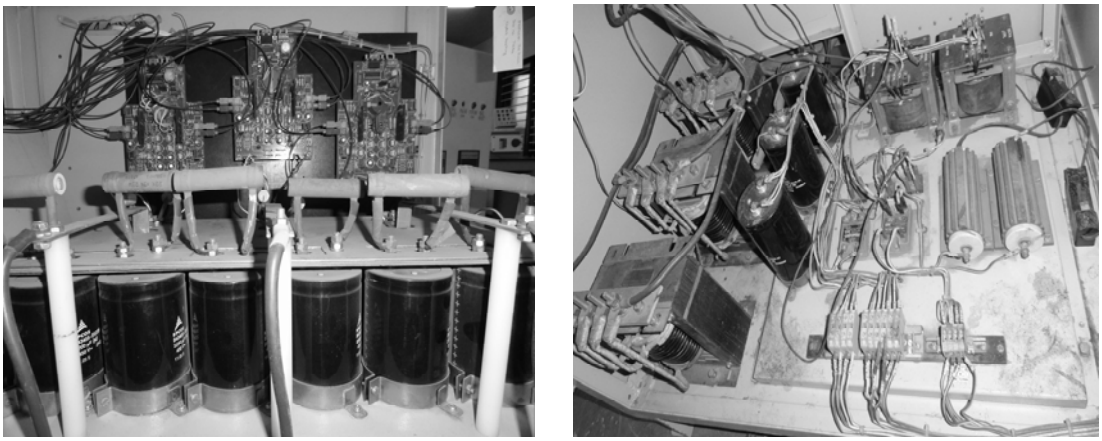


Fig.6.3 Photograph of (a) Three-phase VSI with gate-driver circuit (b) Interface-inductor and pre-charger

The voltage rating of dc-link capacitor is decided by the supply voltage as well as the voltage drop across the inductor and VSI switching technique. The dc-voltage is required to produce at maximum modulation index according to the theoretical calculation [supply voltage + voltage drop across the inductor]. But in practical cases, due to the introduction of dead-band and device transition times from ON-state to OFF-state and vice-versa, the supply voltage attainable will be less than the estimated voltage. Considering all these factors, the dc operating voltage is chosen at 750 V. The allowable ripple component of the dc-voltage decides the required capacitor value. The capacitor must have a ripple current capability, since the maximum value of ripple current of 2200 μF / 450V capacitor is 16 Amp. It provides required dc-voltage (around 750 V) at the voltage source inverter.

6.2.3. DSP Processor

The performance of the active power line conditioner is demonstrated experimentally using 16-bit fixed point TMS320F240 Texas DSP. It combines the features of TMS320 architectural design of the C2xLP core for low-cost, high performance capabilities and advanced peripherals, which are optimized for power

electronic applications. These peripherals include the event manager module, which provides general-purpose timers and registers to generate up to 12-PWM outputs [130]. Fig.6.4 shows the block diagram of the TMS320F240 digital signal processor control device.

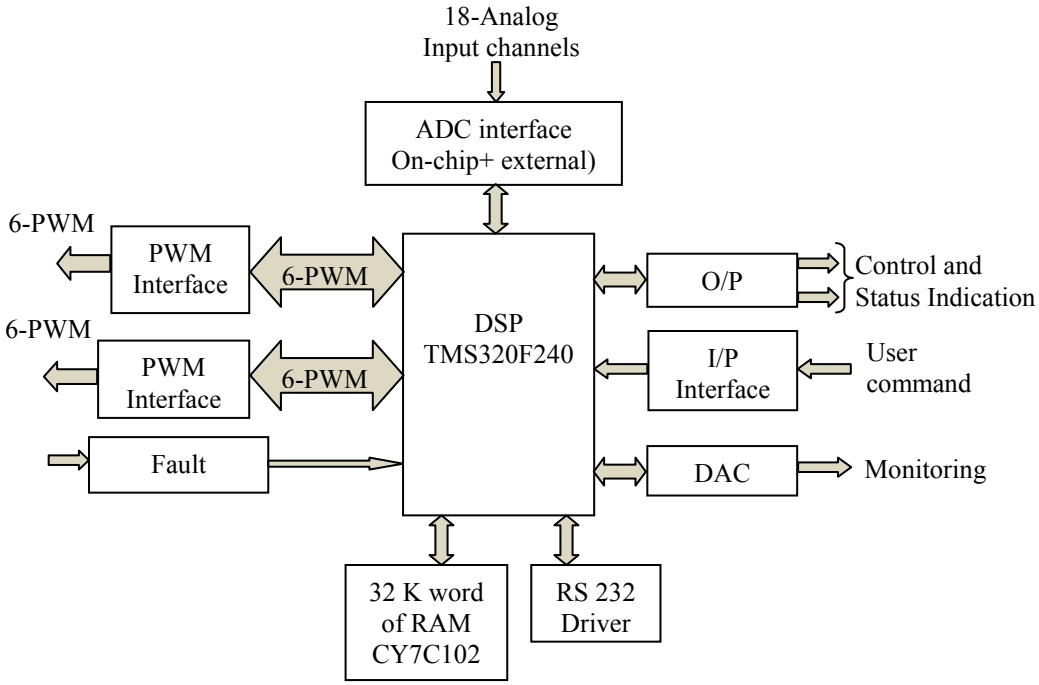


Fig.6.4 Block diagram of TMS320F240 DSP controller

Fig.6.5 shows the photograph of the TMS320F240 DSP and SMPS for powering the DSP. The F240 microprocessor implements a comprehensive instruction set that supports both numeric-intensive signal-processing operations and general-purpose applications, such as multiprocessing and high-speed control. For maximum throughput, the next instruction is pre-fetched while the current one is being executed. Because the same data lines are used to communicate with external data, program, or I/O space, the number of cycles an instruction requires to execute varies, depending upon whether the next data operand fetch is from internal or external memory. The memory is used as 16k words of on-chip flash EEPROM, 544 words of on-chip data / program DRAM and 32k words of external RAM of speed 10 ns for debugging. The details regarding this DSP processor is mentioned in Appendix-B in the thesis.

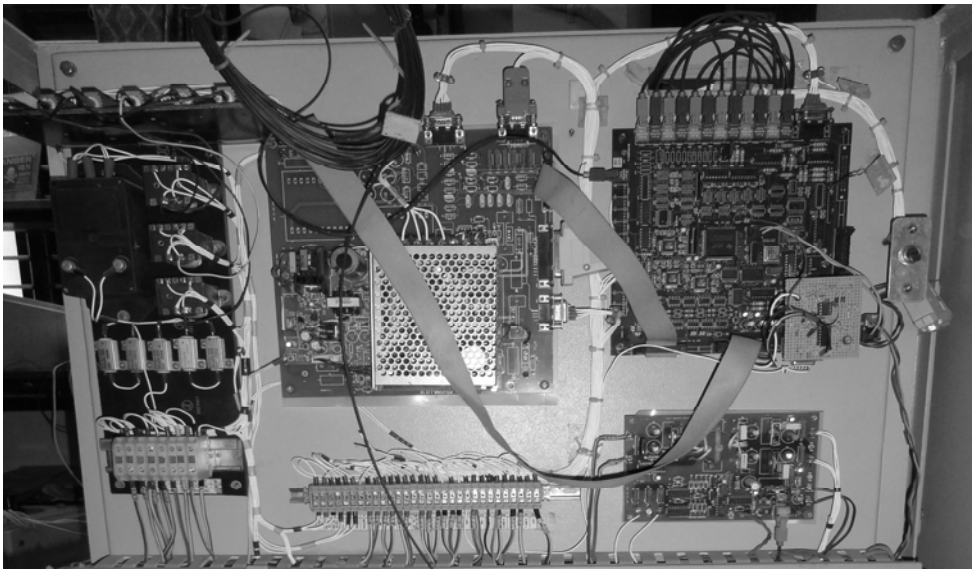


Fig.6.5 Photograph of TMS320F240 DSP and SMPS for powering the DSP

6.2.4. Hall effect sensors

The power quantities are sensed and transformed into low-level signals using the Hall Effect voltage and current sensors (transducers). The Hall Effect sensors also provide isolation between the primary circuit (power network) and the electronic circuits (signal level circuit). The three-phase voltages, load currents, source currents and dc-link capacitor voltage signals are sensed and computed for proposed active power line conditioner controller. The sensor should be selected with the consideration of the desired measuring range, accuracy, linearity, bandwidth and faster response. The phase voltages are sensed using LEM-LV20P (Hall Effect sensor), the source currents (or compensation currents in case of direct current control approach) and load currents are sensed by LEM-LA100P current transducer. The active power line conditioner controller has an external dc-voltage regulation loop in the control strategy. This loop requires dc-voltage feedback as precise as possible. The high performance dc sensing circuit is preferred and the dc-link capacitor voltage is sensed by LEM LV100 voltage transducer. Fig.6.6 shows the photograph of the voltage and current transducer. These transducers convert the power level voltage and current quantities to low level analog signals in the range of $\pm 5V$

Fig.6.6 Photograph of voltage sensor and current sensor

6.2.5. Signal conditioning card

The low-level bipolar voltage and current from the Hall Effect sensors are in the range $\pm 5\ V$. These are converted to 0-3 V range to be compatible with the analog channels of the DSP through the signal conditioning card. The digital controller has simultaneous sampling, analog to digital converter (ADC) with a maximum conversion time of 6.6 μs. It is also equipped with a supervisory controller realized with Intel 80188 microprocessor and general purpose peripherals. These digitized sampling signals are computed using proposed control algorithm to extract the fundamental components and harmonic components.

6.2.6. Code composer studio

The control algorithm is coded in assembly language for digital control design and implementation. XDS510PP JTAG Emulator with Code Composer Studio (CCS) is used to implement the proposed control algorithm in real-time target processor (TMS320F240) on the host computer. The Emulator operates through parallel port on personal computer and no adapter card is required.

6.2.7. Gate driver circuits

The primary function of the gate driver circuit is to switch device from the OFF state to the ON state and vice versa. The gate driver circuit amplifies the switching pulse to levels required to drive the device and provides an electrical isolation

(interface) between the control circuit and the power device. This gate driver will work with gate pulses transmitted either electrically or optically. Single card is used to control complementary switches of one arm of the two-level inverter, so totally three gate driver cards are required for two-level active power inverter. The driver circuit is constructed with the M57962AL which is a hybrid driver circuit supplied by Mitsubishi. The direct SVM technique and indirect adaptive-fuzzy-HCC techniques generate the switching pulses. These generated switching pulses are provided to the voltage source inverter via PWM-port of the DSP processor through proper interfacing circuits (protection circuits and gate driver circuits). The protection scheme is based on the fact that the drain-source voltage of IGBT increases with drain current for given gate-source voltage. As long as the drain current is within the normal limit, the driver signal (switching pulse) is transmitted to the gate. When the current exceeds its limit, the protection logic inhibits the drive signal from reaching the gate and fault indication is given. The fault indication persists as long as the turn-on process is present. An indication is also given in case of a turn-on failure. The gate driver uses fiber optic interface which enhances the noise immunity, and also isolates the DSP processor and power device.

6.2.8. Complete hardware setup:

The experimental setup is designed such that all the auxiliary circuits including the digital controller, two-level inverter, interface inductor and the thyristor-rectifier load are present. Fig.6.7 shows the photograph of the complete hardware setup for active power line conditioner system. The experimental set-up has the following circuits and components

- Contactor for main source and switch Fuse Unit (SFU)

  The function of contactor is to connect or disconnect the active power line conditioner with the PCC, which can be controlled by the digital controller. The control is achieved through the closing and opening of a Solid State Relay (SSR) with the ON / OFF signal from an output port of the digital controller. An isolator is provided to isolate the active power line conditioner from the PCC if any maintenance work has to be carried out. Semiconductor Fuses of suitable rating shall be provided at the entry point of the converter panel.

- Two-level voltage source inverter set-up
- Main SMPS for powering the DSP
- Gate driver SMPS for powering the gate driver circuitry
- Hall effect transducers for the supply voltage sensor
- Hall effect transducers for the load currents and the source currents (and compensation currents) measurement
- DC-voltage sensing circuit
- Pre-charger circuit to charge the dc-link capacitor voltage
- Miscellaneous arrangements like connectors to transfer PWM-pulses from the digital controller to the voltage source inverter, connectors to transfer sensed currents and voltages to the digital controller, transistor based pull-up circuits, power supply connectors, etc.

Fig.6.7 Photograph of complete hardware setup for APLC system

6.3. Modified-SRF with SVM technique

Modified-SRF with direct current control SVM method is validated for three-phase active power line conditioner system. To implement the direct current control based

SVM technique, the three-phase supply voltages, load currents, compensation currents and dc-voltage are sensed and computed. The reference signals are generated through modified-SRF method. The required PWM-switching pulses are obtained by comparing the compensation current (supplied by APLC) with the reference currents. These switching pulses drive the active power inverter and make sinusoidal unity power-factor currents in the AC mains.

6.3.1. Simulation Results

For simulation, the system parameters are considered as line-to-line voltage of 360 V / 50 Hz, interface inductance of 1.8 mH and dc-capacitance of 2200 μF. This simulation is conducted with the same parameter values as in the experiment for the purpose of verification. The simulation waveform of the instantaneous three-phase balanced supply voltages is shown in Fig.6.8 (a). The source current draws non-sinusoidal current due to the thyristor-rectifier load that is shown in Fig.6.8 (b). It indicates that the source current contains fundamental as well as harmonic components. The active power line conditioner provides the required harmonic compensation current to inject / draw the harmonic current as shown in Fig.6.8 (c). The source current after compensation is presented in Fig.6.8 (d) that indicates current is sinusoidal.

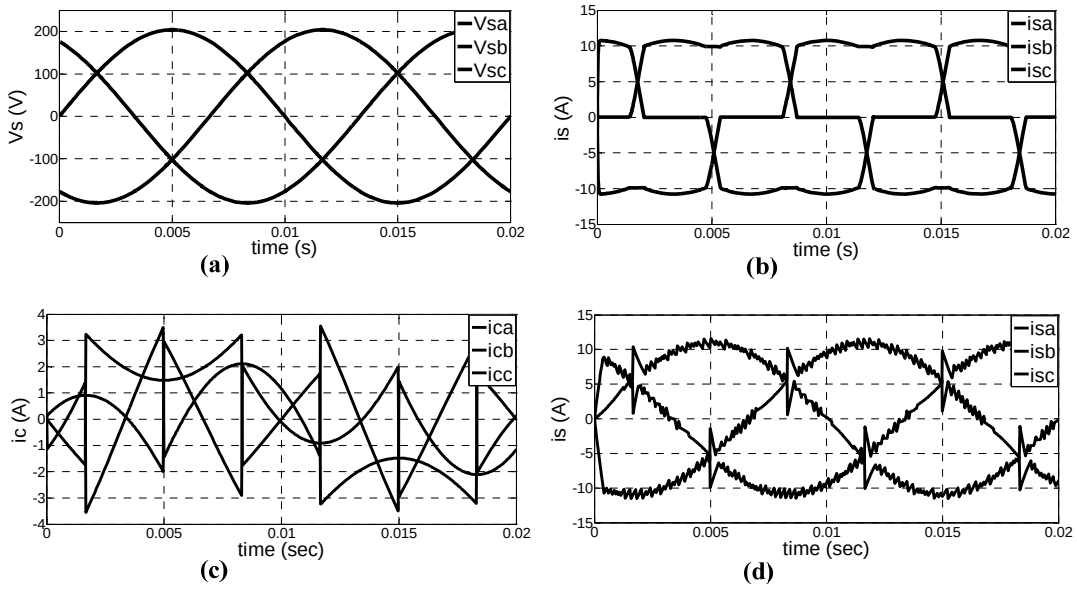


Fig.6.8 Simulation waveforms of (a) Supply voltages, (b) Source currents before APLC compensation, (c) Compensation currents and (d) Source currents after APLC compensation.

The FFT is employed to investigate the presence of harmonics. The spectral response of the source current without APLC compensation is shown in Fig. 6.8 (e). It indicates that the supply current is distorted due to the presence of fifth, seventh, eleventh and higher order of harmonic spectral components. In this case THD is found to be 23.41 %. Fig. 6.8 (f) shows the spectral response with APLC and it is observed that THD is 4.51 %

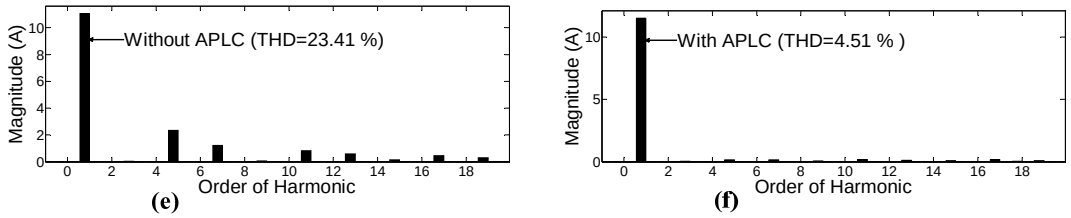


Fig.6.8 Simulations of order of harmonics (a) Without-APLC and (f) With-APLC

6.3.2. Experimental results

For the experimental validation of the three-phase active power line conditioner system, the modified-SRF with direct current control SVM technique is adopted. The prototype active power line conditioner consists of six-IGBT-FF200R12KE3 (two-level voltage source inverter), dc-link capacitor 2200 μF (for 750 V_{dc} supply) and three-interface inductor (1.8 mH). The performance of the controller is verified through 16-bit fixed point TMS320F240 digital signal processor. The three-phase supply voltages, load currents, compensation currents and dc-voltage signals are sensed and computed, which are the main inputs of the controller. Fig. 6.9 shows the schematic diagram of the shunt active power line conditioner system using modified-SRF with direct current control SVM-technique. These sensed signals are applied to the analog to digital converter of the processor through the signal conditioning card. This active power line conditioner control algorithm is coded in assembly language for digital control design and implementation. Code Composer Studio (CCS) is used to implement the proposed control algorithm in real-time target TMS320F240 processor on the host computer. The adaptive-fuzzy-HCC technique is used to generate the switching pulses of the voltage source inverter. These required switching pulses are provided to the IGBT inverter via PWM-port of the DSP processor through

gate driver circuits. The performance of the active power line conditioner system has been experimented under the thyristor-rectifier load. This experiment has been tested separately, with the switch-ON and switch-OFF response of the active power line conditioner. Initially voltage source inverter acts as rectifier to charge the dc-link capacitor voltage through pre-charger circuit. When the dc-voltage is equal to the supply voltage that is considered as a floating mode, the inverter will be in the ON-state. When the supply voltage is less than or greater than the dc-voltage, the inverter injects or draws the required compensation power at PCC in the power system, respectively.

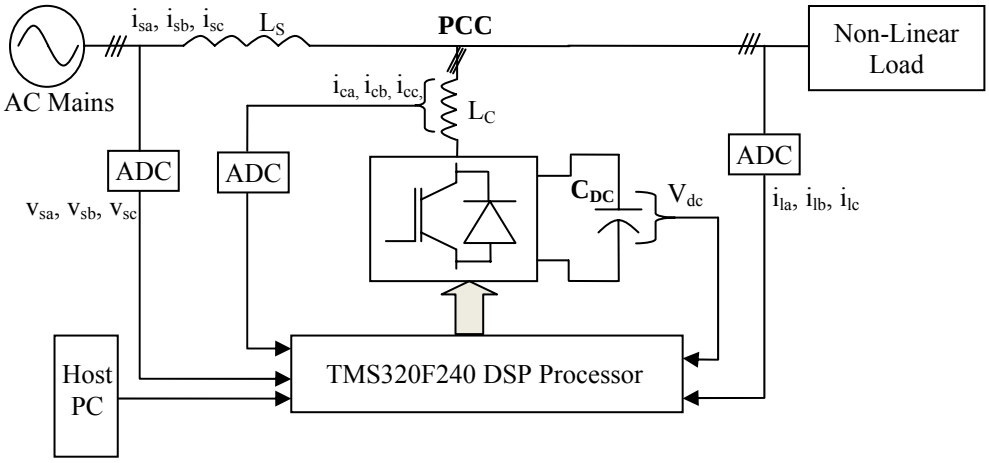


Fig. 6.9 Block diagram of the shunt APLC using modified-SRF with direct SVM-technique

Fig. 6.10 (a) shows the experimental waveform of three-phase supply voltages of the power line conditioner system. These waveforms indicate that the supply voltages (V_{sa}*=210 V,* V_{sb}*=204 V and* V_{sc}*= 205 V*) are almost balanced and sinusoidal. The source current draws non-sinusoidal or harmonic-current due to the thyristor-rectifier load. Fig. 6.10 (b) shows the source currents before APLC compensation currents *(*i_{La}*=10.3 A,* i_{Lb}*=10.3 A and* i_{Lc}*=10.1 A)*. From this waveform, it is observed that the current contains fundamental and harmonic components. The direct current control SVM technique is employed for generating gate control switching pulses to drive the active power inverter. The inverter draws / injects the required compensating currents *(*i_{ca}*=1.7 A,* i_{cb}*=1.6 A and* i_{cc}*=1.8 A)* as shown in Fig. 6.10 (c). Consequently the

current harmonic compensation is achieved by injecting equal but opposite current harmonic components at PCC by canceling the original distortion. The waveform of source current *(i_{sa}=10.8 A, i_{sb}=10.6 A and i_{sc}=10.3 A)* after APLC compensation is presented in Fig. 6.10 (d) that indicates the currents are sinusoidal and it is in phase with the respective phase-voltages. It may be noted that these values of source, load and compensation current(s) refer to a specific instant when waveforms are captured.

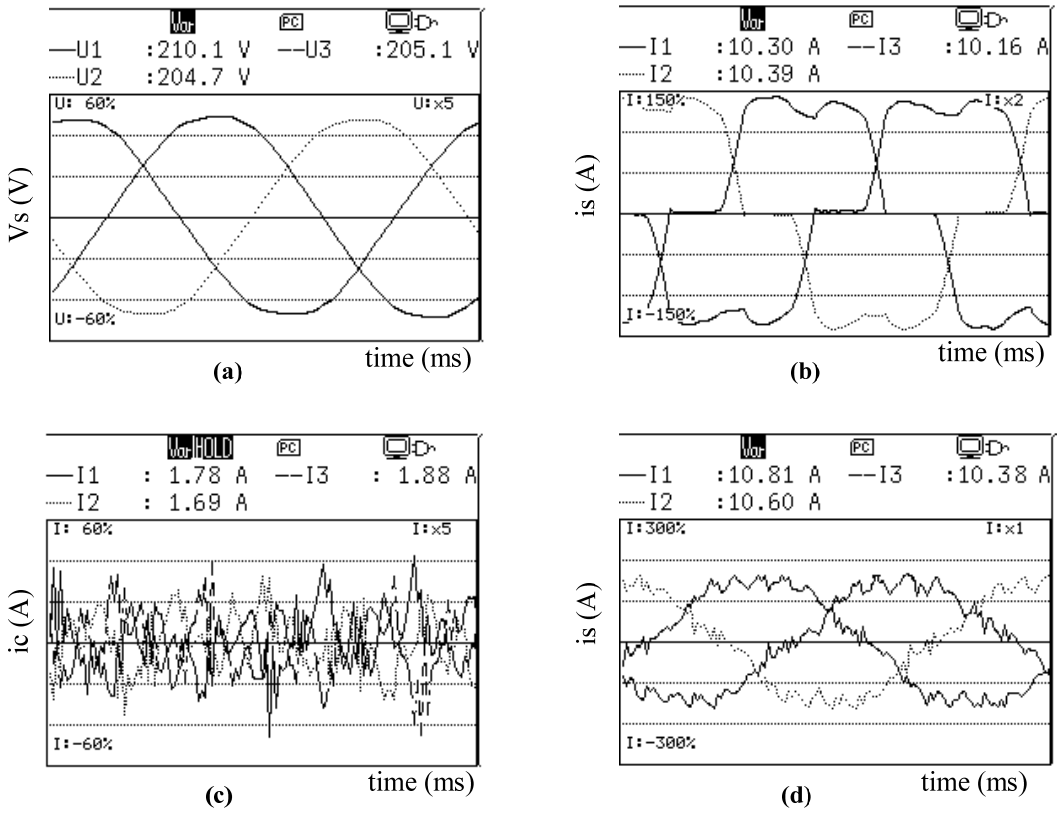


Fig.6.10 Experimental waveforms of (a) Supply voltages, (b) Source currents before APLC compensation, (c) Compensation currents and (d) Source currents after APLC compensation

The total harmonic distortion for source current is measured. Before connection of the active power line conditioner, the THD is 22.5% and after connecting active power line conditioner, this value is reduced to 4.6 %. The THD waveforms are presented in Fig. 6.11 (a) without APLC and in Fig. 6.11 (b) with APLC. These figures demonstrate that proposed active power line conditioner is capable of compensating load current harmonics.

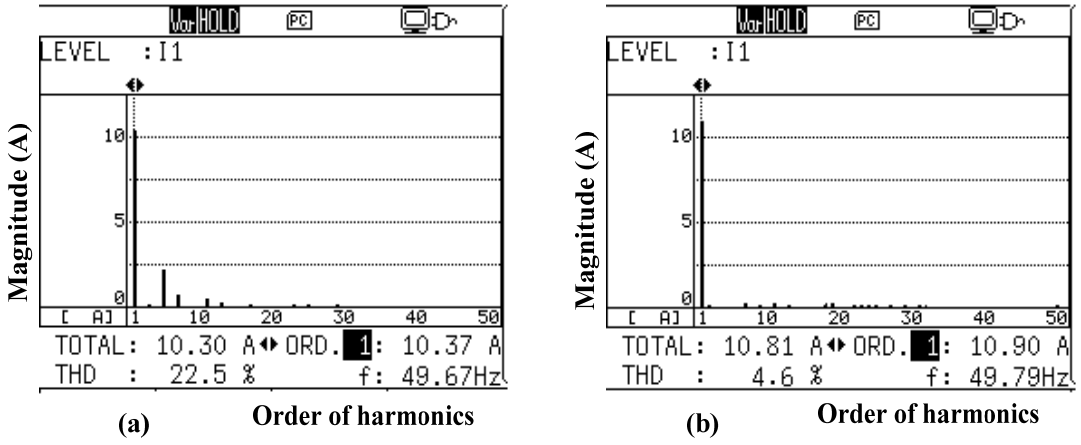


Fig.6.11 Order of harmonics (a) Without APLC and (b) With APLC

Remarks: Total harmonic distortion of the source current is measured without and with active power line conditioner using modified-SRF with direct current control SVM technique. The simulation (THD=4. 51 %) and the experiment (THD=4. 6 %) results ensure that THD is almost same with the active power line conditioner.

6.4. Modified-SRF with adaptive-fuzzy-HCC

The performance of the modified-SRF with indirect current control using adaptive-fuzzy-HCC method is adopted for active power line conditioner system. To implement the indirect current control approach based adaptive-fuzzy-HCC technique, the three-phase voltages, actual source currents, load currents and dc-link capacitor voltage are sensed. In this technique, the PWM-switching pulses are obtained by comparing the actual currents with the reference current which are generated by the modified-SRF methods. The control algorithm is validated through MATLAB program and coded in assembly language for digital hardware implementation. Fig.6.12 shows the flowchart of the APLC controller, which is used with modified-SRF and adaptive-fuzzy-HCC technique. The modified-SRF method consists of simplified unit vector generation for vector orientation, PI-controller for dc-link capacitor voltage regulator and stationary-rotating synchronous frames for extracting the reference current. The extracted fundamental reference currents are compared with actual currents and generates the required switching pulses by using adaptive-fuzzy-HCC to drive the inverter. The adaptive-fuzzy-hysteresis bandwidth

HB is modulated as a function of slope reference current di_s*/dt and supply voltage v_s. For symmetrical operation of three-phase, the bandwidth is denoted as HB_A, HB_B *and* HB_C of the same value, but having 120^0 phase difference. The HB is applied to the switching function of the hysteresis current controller to produce the gate control switching pulses *(S1, S2, S3, S4, S5, S6)* of the PWM-inverter.

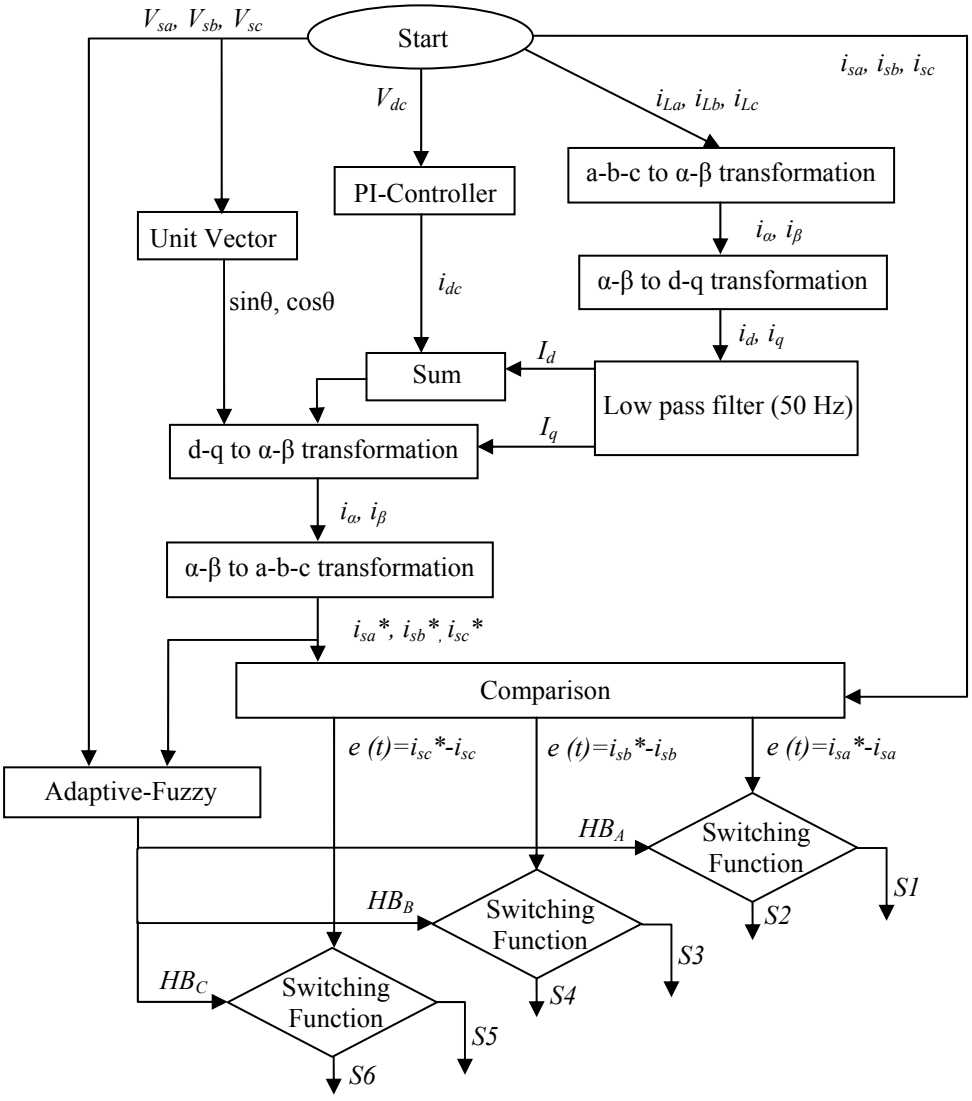


Fig.6.12 Flow chart of the modified-SRF with indirect current control adaptive-fuzzy-HCC

6.4.1. Simulation results

The modified-SRF with indirect current control adaptive-fuzzy-HCC algorithm is verified using MATLAB program and coded in assembly language for hardware implementation. The simulation result for a particular phase(phase a in this case) of the instantaneous three-phase supply voltage is shown in Fig.6.13 (a). It indicates the supply voltage is sinusoidal. The source current draws non-sinusoidal current due to non-linear characteristics of the thyristor-rectifier load, which generate six-pulse rectifier waveform. The source current before compensation is shown in Fig.6.13 (b). It indicates the source current contains fundamental component as well as harmonic components. The active power line conditioner provides the required harmonic compensation current to inject / draw the harmonic current as shown in Fig.6.13 (c). The source current after compensation is presented in Fig.6.13 (d), which indicates current is sinusoidal. These simulation results are plotted for a-phase; the other phases (b-phase and c-phase) are considered to be phase shifted by 120^0.

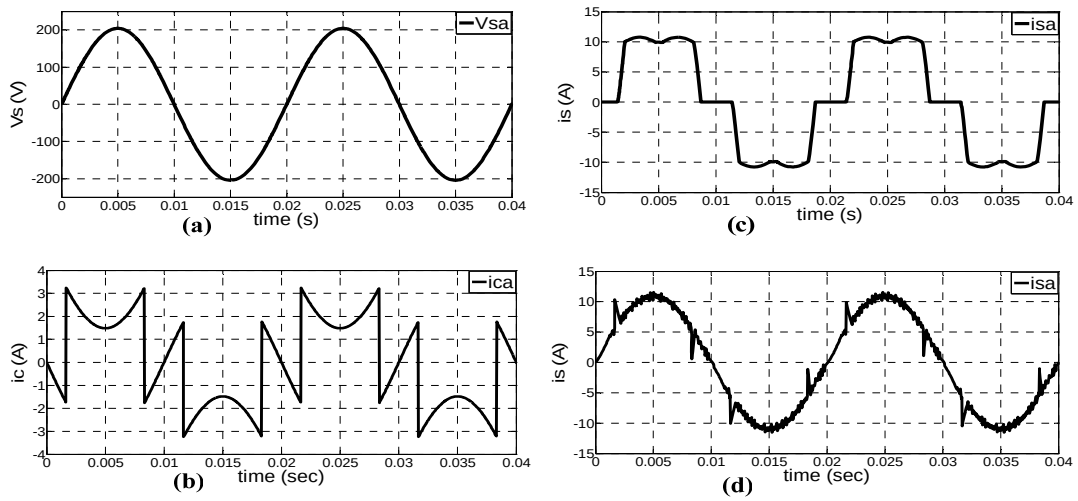


Fig.6.13 Simulation waveforms of (a) Supply voltage, (b) Source current before APLC compensation, (c) Compensation current and (d) Source current after APLC compensation

The FFT method computes the order of harmonics. The total harmonic distortion in the source current without active power line conditioner compensation is computed using the plot which is shown in Fig.6.13 (e). It indicates the supply current is distorted due to the dominance of fifth, seventh and eleventh order of harmonic spectral components. The measurement of THD is 23.41 %. Fig.6.13 (f) shows a

plot(order of harmonics vs magnitude) with active power line conditioner and ensures that THD is less than 5 % (THD=3. 65 %).

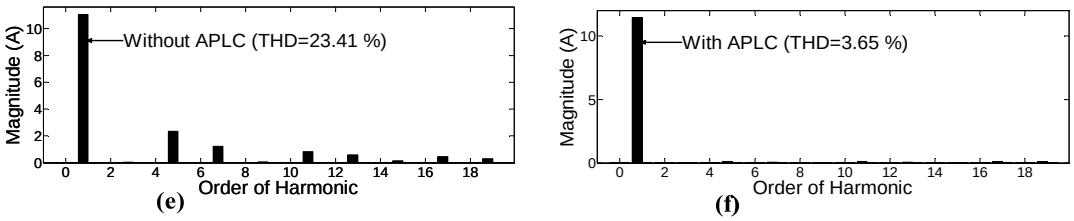


Fig.6.13 (e) Order of harmonics of source current Without-APLC and (f) With-APLC

dc-link capacitor voltage: The dc-link capacitor voltage of the PWM-inverter is controlled by the modified-SRF controller. Fig.6.14 shows the waveform of the dc-link capacitor voltage and ensures it is nearly constant, which is required to supply the voltage source inverter.

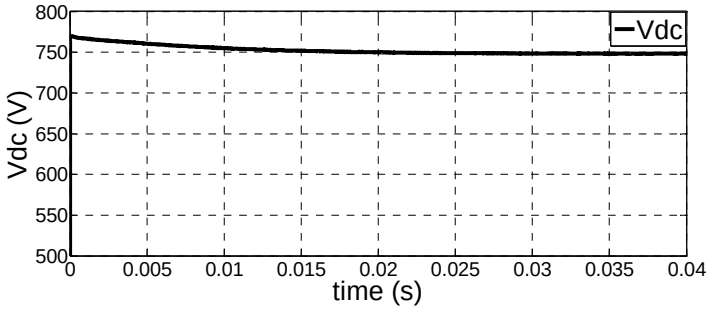


Fig.6.14 dc-link capacitor voltage

6.4.2. Experimental results

The modified-SRF with adaptive-fuzzy-HCC (using the indirect current control approach) is adopted for the experimental validation of the three-phase active power line conditioner system. Fig.6.15 (a) shows the experimental waveform of the supply voltage (x-axis 5 ms/div, y-axis 200 V/div) in the power distribution system, which indicates the supply voltage is nearly balanced and sinusoidal. The source current draws non-sinusoidal current due to the nonlinear characteristics of the thyristor-rectifier load. Fig.6.15 (b) shows the source currents (50 mV/div) before active power line conditioner compensation. It indicates that the source current comprises of fundamental components as well as higher order harmonic components.

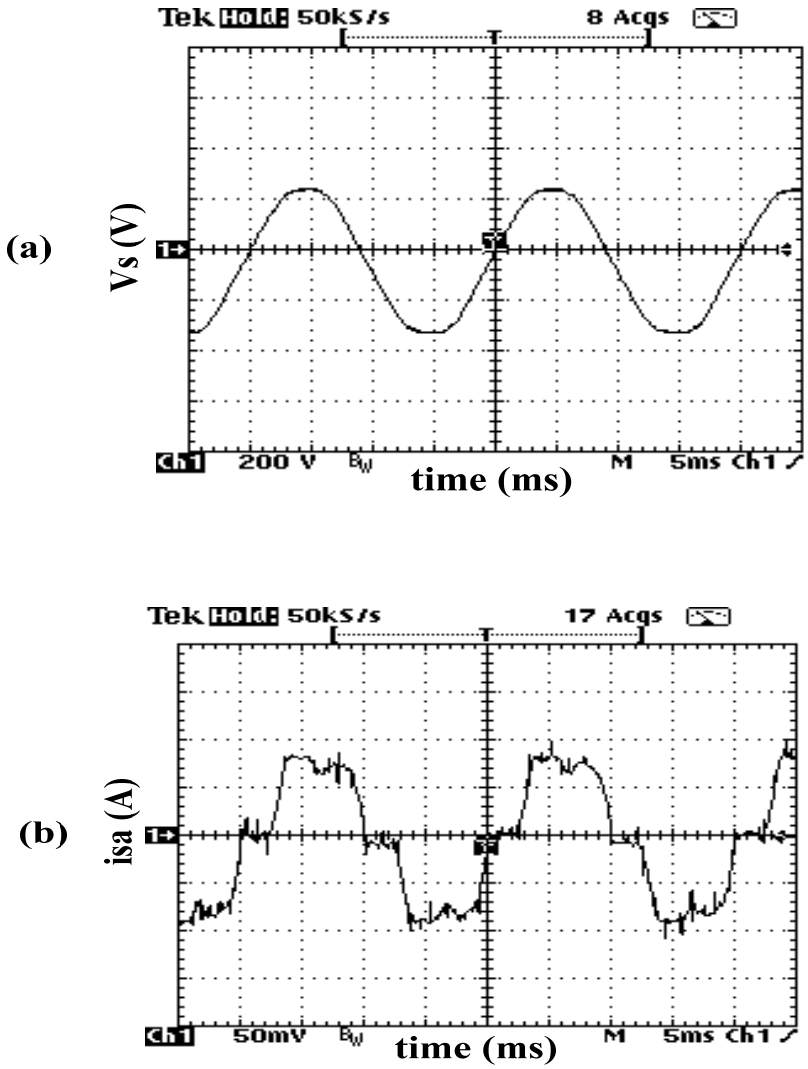
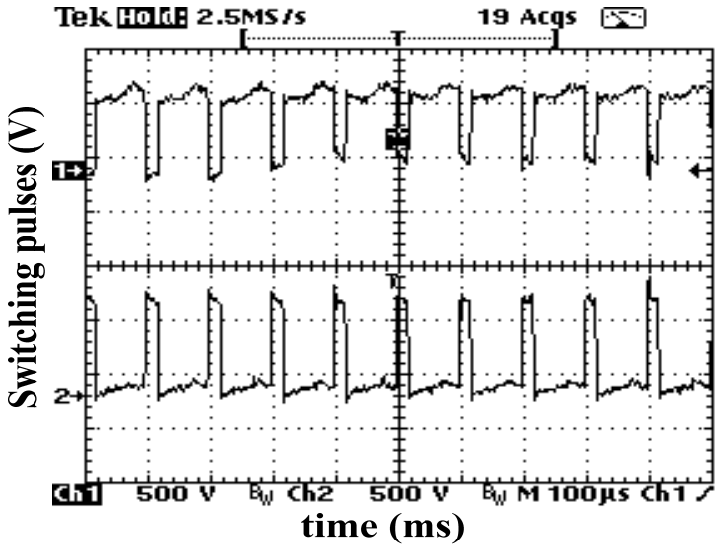


Fig.6.15 Experimental waveforms of (a) Supply voltage and (b) Source current before APLC compensation

The modified-SRF method is used to extract the reference current components. The reference current compared with actual source current generates the gate control switching pulses (channel 1-pulse ON and channel 2-pulse OFF (inverse signal); 500 V/div) using adaptive-fuzzy-HCC-technique to drive the active power inverter as shown in Fig.6.15 (c). The active power line conditioner injects harmonics demanded by the thyristor-rectifier load, so that the power system needs to supply active component of the fundamental current required by the load. The amount of current injected by the active power line conditioner to PCC is $(V_{inv} - V_g)/X_L$; thereby APLC cancels the original distortion and improves the power quality of the connected power system. The harmonic compensation current (500 mV/div) is shown in Fig.6.15 (d).

(c)



(d)

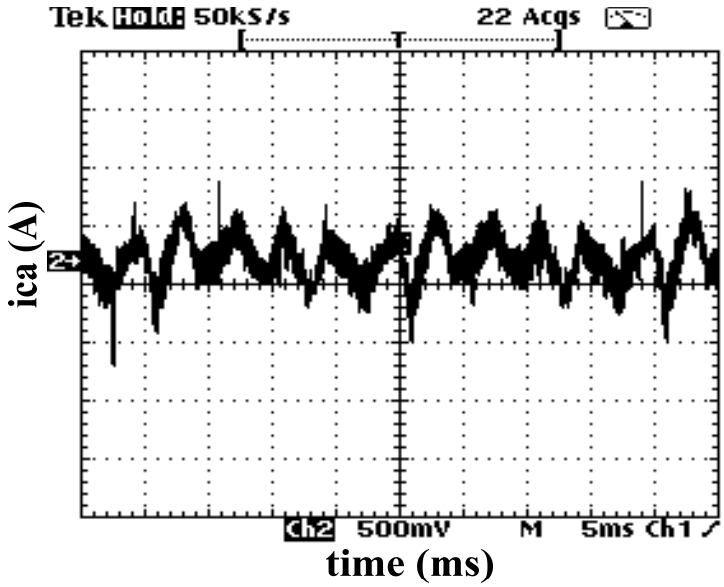
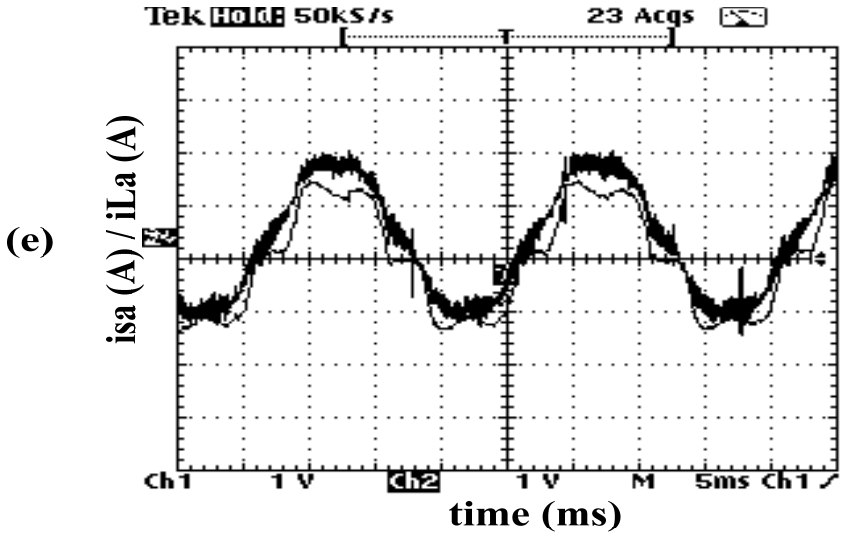


Fig.6.15 (c) Switching pulses and (d) Compensation current

Consequently the current harmonics is achieved by injecting equal but opposite current harmonic components. The waveform of source current after active power line conditioner compensation current (1 V/div) is presented in Fig.6.15 (e). It indicates the current is sinusoidal and in phase with the respective phase-voltages. Fig.6.15 (f) represents the comparison of the load current and the source current (channel 1-load current and channel 2-compensation current; 1 V/div) after active power line conditioner compensation. These experimental waveforms are measured in a-phase; the other b-phase and c-phase are phase shifted by 120^0 each other.



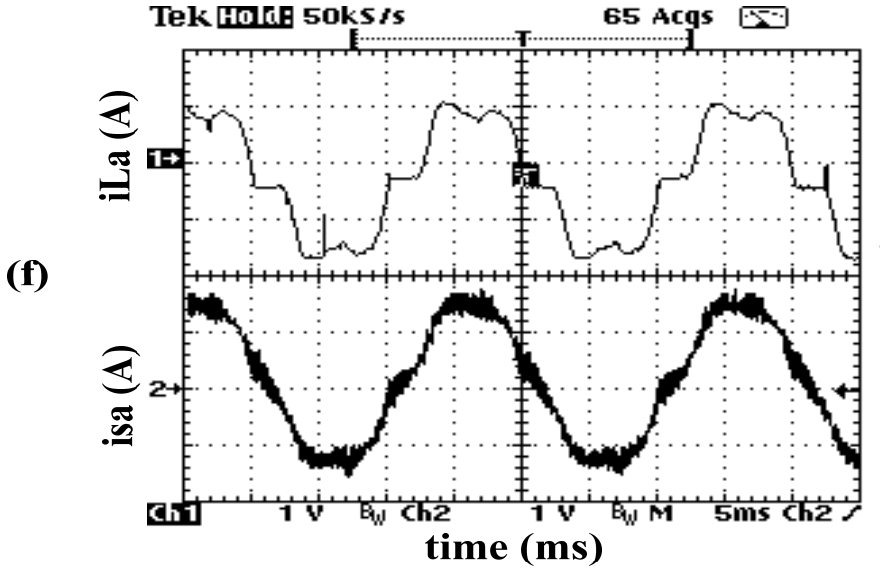


Fig.6.15 (e) Source current after compensation and (f) Load current and Source current

Fig.6.16 (a) shows the experimental waveform of supply voltages of the power line conditioner system. These waveforms indicate the supply voltages (v_{sa}=210 V, v_{sb}=208 V, v_{sc}=212 V) are almost balanced and sinusoidal. The source current draws non-sinusoidal current due to the thyristor-rectifier load. Fig.6.16 (b) shows the source currents before active power line conditioner compensation. From this waveform, it is observed that the source current contains fundamental components and harmonic components.

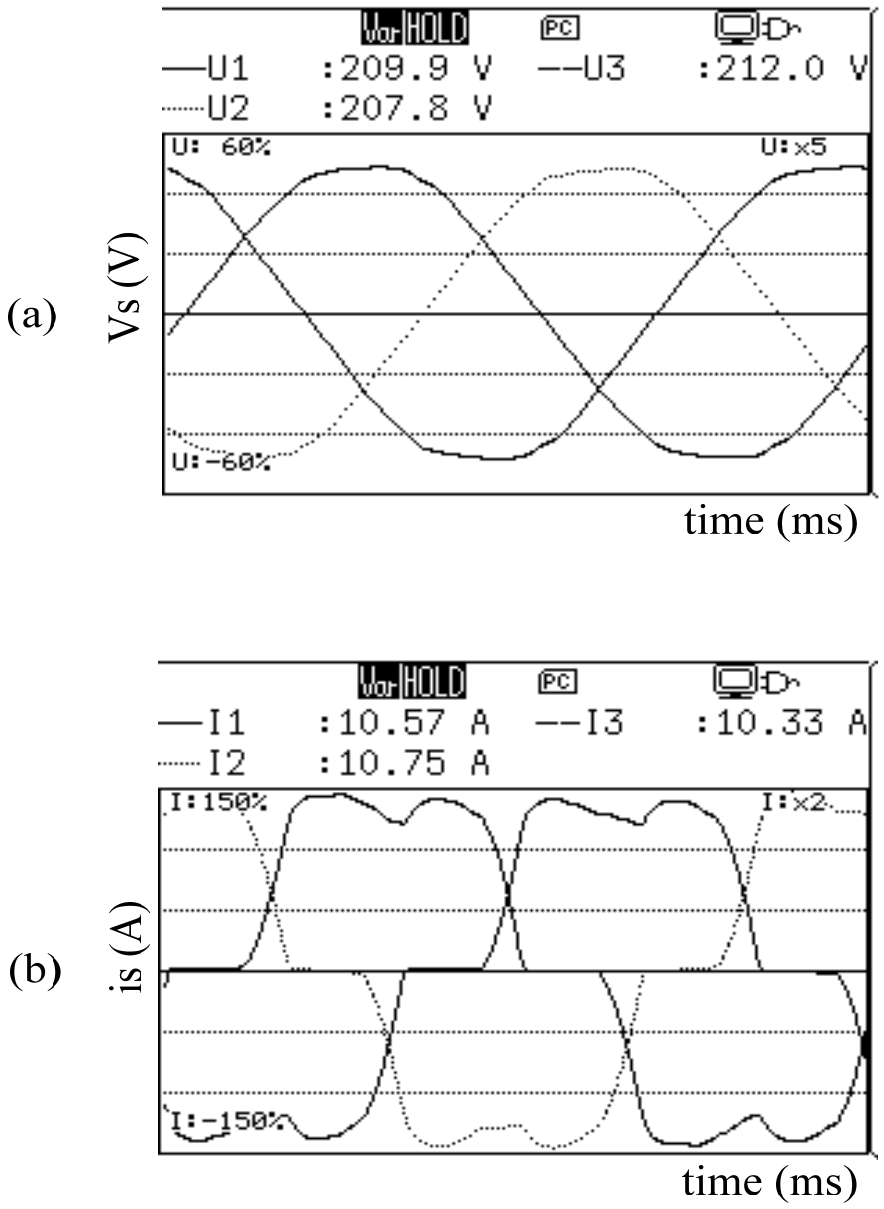
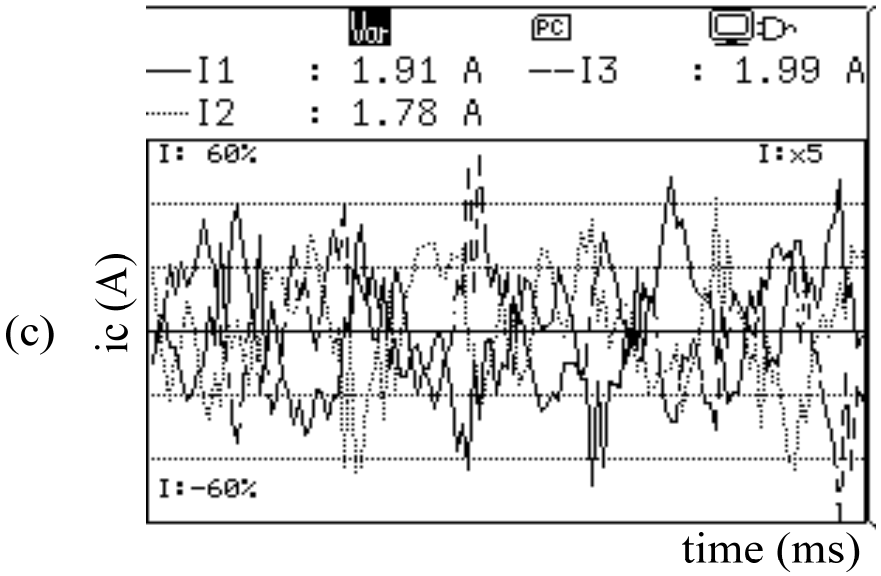


Fig.6.16 Experiment waveforms of (a) Supply voltages and (b) Source currents before APLC compensation

The shunt active power line conditioner injects / draws the required compensating currents as shown in Fig.6.16 (c). Consequently the current harmonic compensation is achieved by injecting equal but opposite current harmonic components at PCC by canceling the original distortion. The waveform of source current after active power line conditioner compensation is presented in Fig.6.16 (d) which indicates the currents are sinusoidal.



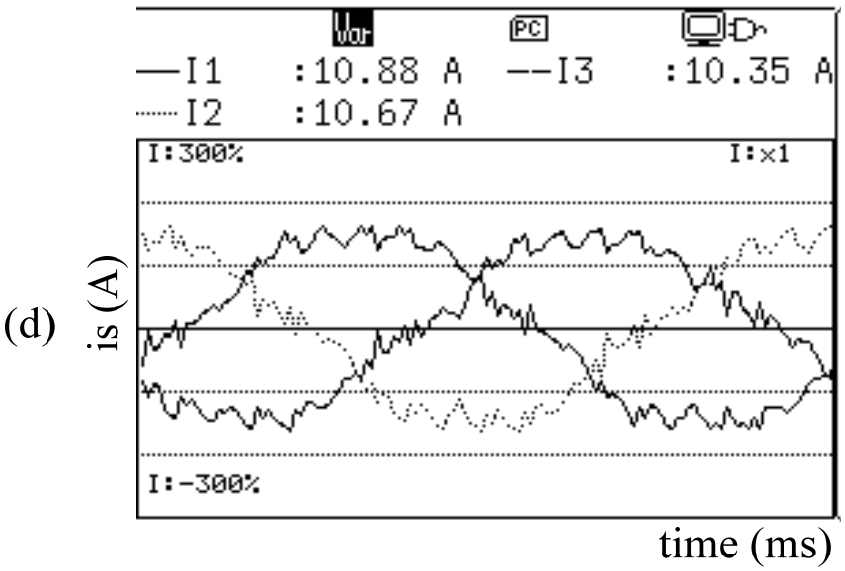


Fig.6.16 (c) Compensation currents and (d) Source currents after APLC compensation

THD Analysis: The total harmonic distortion in the source current is measured. Before connecting the active power line conditioner, the THD is 22.5 % and after connecting the active power line conditioner, the value is reduced to 3.7 %. The THD waveform is presented in Fig.6.17 (a) without active power line conditioner and Fig.6.17 (b) indicate the individual order of harmonics in the source current. Similarly, THD waveform is presented in Fig.6.17 (c) with active power line conditioner and Fig.6.17

(d) indicates the individual order of harmonic components in the source current. These figures demonstrate the proposed controller based active power line conditioner is capable of compensating load current harmonics. These waveforms are measured using the Yokogawa CW240 Clamp-on Power Meter.

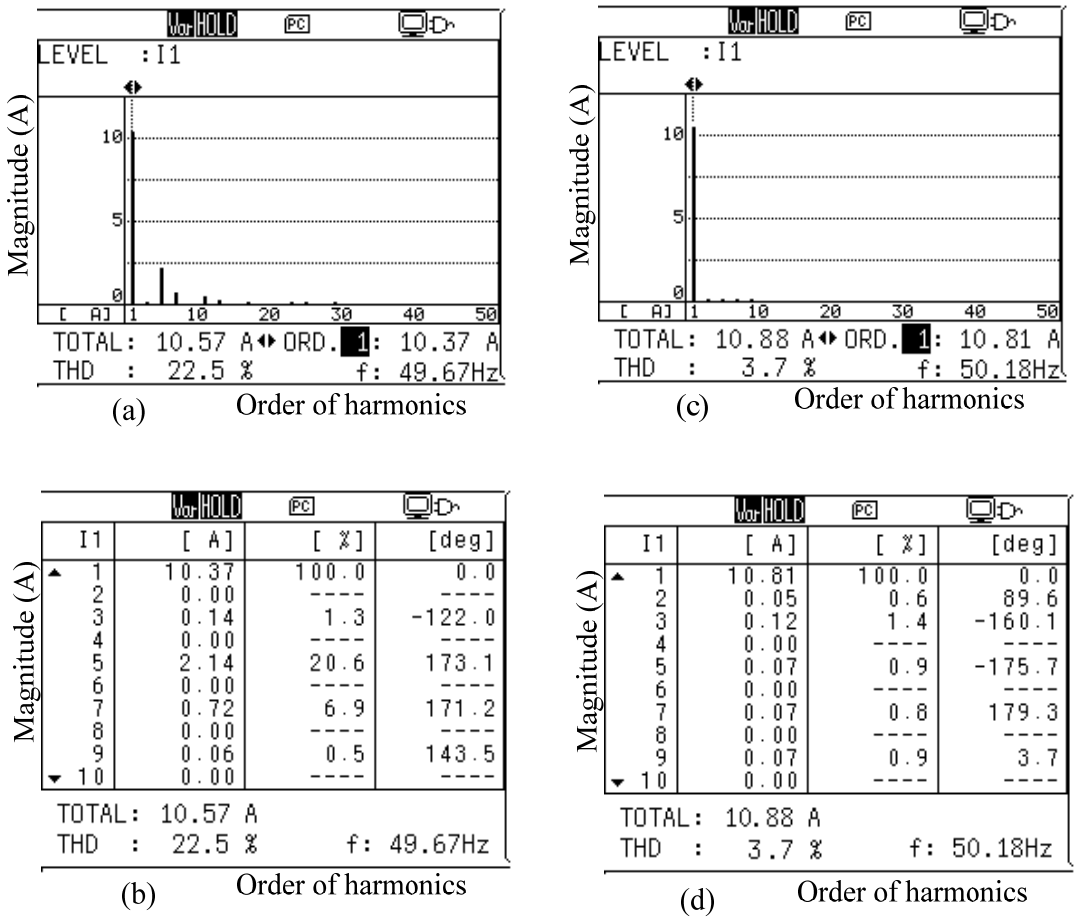


Fig.6.17 Order of harmonics (a) Without-APLC (THD=22.5 %) and (b) With-APLC (THD=3.7 %)

dc-link capacitor voltage: The active power line conditioner, during normal operation draw small amount of the active power from supply to maintain the dc-link capacitor voltage at the required level and supply for the inverter losses (switching loss and conduction loss). The dc-link capacitor voltage is controlled by the PI - controller. Fig.6.18 shows the waveform (500 V/div) of the dc-voltage and ensures that it is constant, which is required to supply the voltage source inverter.

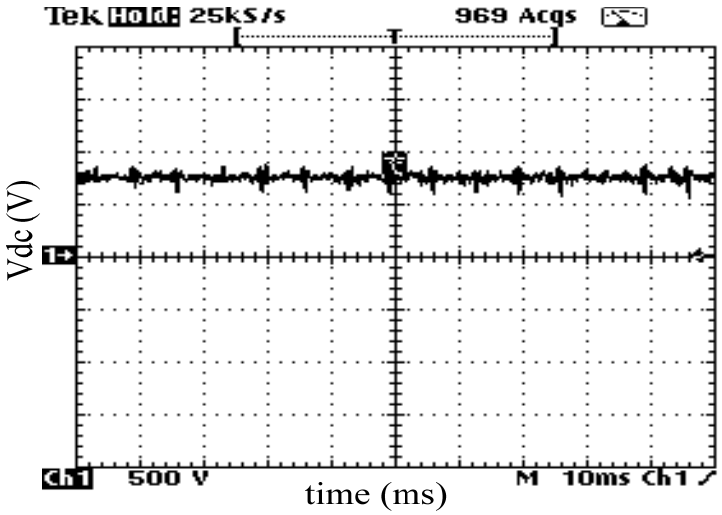


Fig.6.18 dc-link capacitor voltage

Reactive-power compensation: The fully digital controlled active power line conditioner operates as source of reactive power (leading or lagging power factor) and obtained unity power factor. Fig.6.19 (a) waveform is measured from resistor load and indicate the source current is in phase with the supply voltage (channel 1-Voltage 100 V/div and channel 2-Current 1 V/div). Fig.6.19 (b) waveform (channel 1-Voltage 100 V/div and channel 2-Current 1 V/div) is measured with a pure inductor load, which confirms the supply current is almost 90º delayed (phase-shift) with respect to the phase voltage (or source current is lagging with respect to the supply voltage). The shunt active power line conditioner provides the compensation current (channel 1-Voltage 200 V/div and channel 2-Current 1 V/div) as shown in Fig.6.19 (c) to compensate the reactive-power at PCC. Fig.6.19 (d) waveform (channel 1-Voltage 100 V/Div and channel 2-Current 1 V/div) is measured after active power line conditioner compensation under the inductor load, which obtains the current in phase with the supply voltage. In other words, the shunt active power line conditioner compensates the load power factor and almost instantaneously. These waveforms are measured by Tektronix THS720P scope. The obtained waveforms indicate that the active power line conditioner is a superior solution to compensate reactive-power in the power system. The experimental results are more or less similar to the theoretical waveforms.

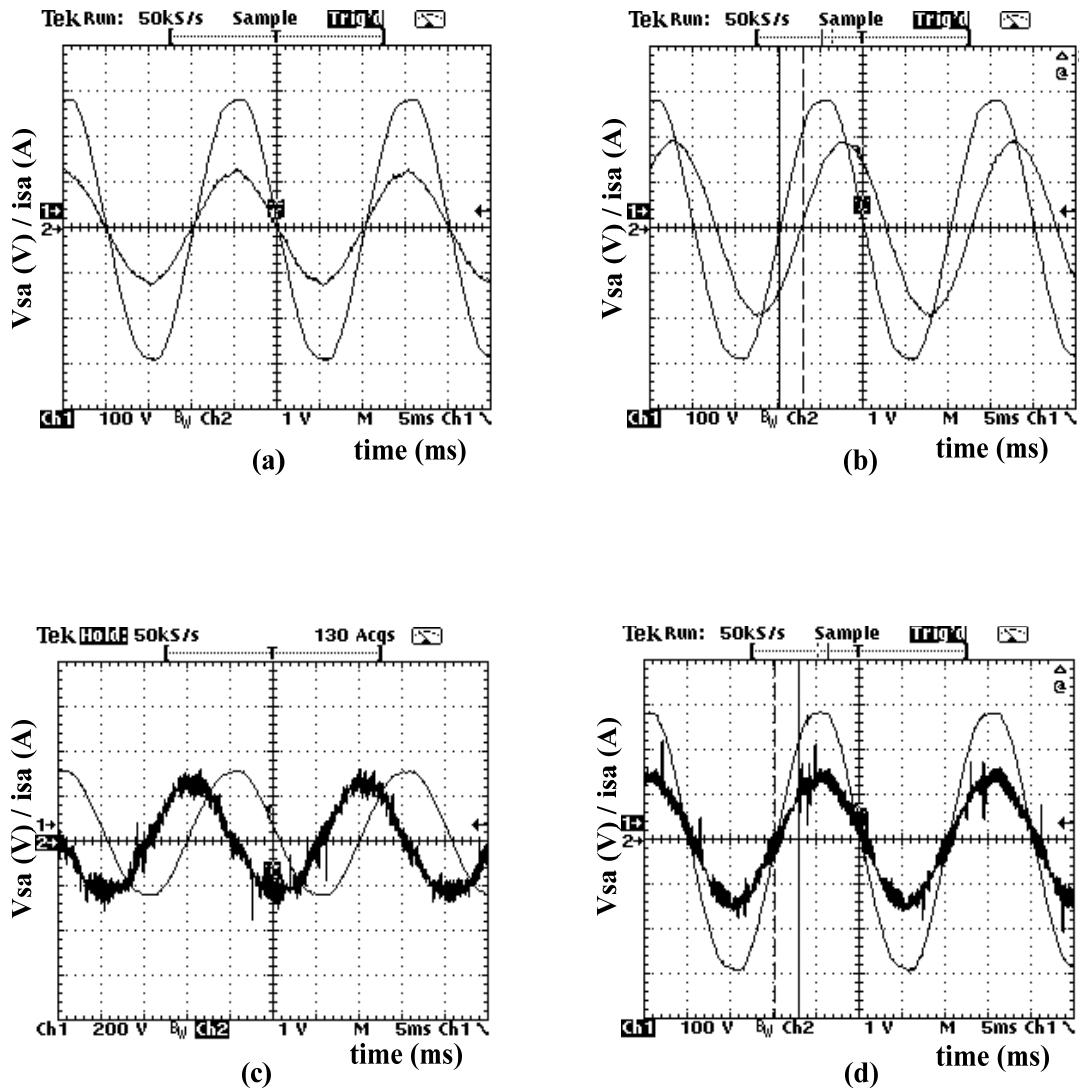


Fig.6.19 Experimental waveforms of supply voltage versus current (a) Resistor-load (b) Inductor-load, (c) Compensation current and (d) After APLC compensation under inductor-load

Table 6.1 THD measurements

Control method	THD in simulation studies		THD in experimental setup	
	Without AHCC	With AHCC	Without AHCC	With AHCC
Modified-SRF with SVM technique	23.41 %	4.51 %	22.5 %	4.6 %
Modified-SRF with adaptive-fuzzy-HCC	23.41 %	3.65 %	22.5 %	3.7 %

Remarks: Total harmonic distortion of the source current is measured without and with APLC using modified-SRF and direct current control SVM technique / indirect current control adaptive-fuzzy-HCC technique. The THD measurement with simulation and experimental results are compared and these results are tabulated in Table 6.1. It is observed that the experimental results are in agreement with the simulation results. This clearly validates our proposed modified SRF theory.

6.5. Study of FPGA Controller

In recent years digital control techniques are becoming the widespread revolution in modern power electronics and active power line conditioner application [131-137]. The microprocessors, DSP processor and Application Specific Integrated Circuits (ASICs) are responsible for better performance of the active power line conditioner system. The design of digitally controlled active power inverter (power converter) is affected by several problems, such as sampling rate, software portability, re-usability, peripheral devices, complicate design and specific register settings for each microprocessor. Change of microprocessor or need of better performance requires huge revision of the design to fit with the new system. These problems is mitigated by designing the controller in Field Programmable Gate Array (FPGA) [138-139]. Very Large Scale Integration (VLSI) technology and Electronic Design Automation (EDA) techniques created an opportunity for the development of complex and compact high-performance controllers. An FPGA is a Programmable Device, comprising thousands of logic gates on a single chip and some of them can be combined to form a Configurable Logic Block (CLB). The FPGA benefits of using portable high level Hardware Description Languages (HDLs) is to encompass the holistic modeling of industrial FPGA design environment [140]. It allows concurrent operation, reduced desining time, easy and fast circuit modification and low cost even for complex circuits. It also maximizes operational performance to achieve high efficiency and power quality while simultaneously allowing the rapid prototyping of digital controllers in ASICs. This section investigates a study of FPGA controller based APLC to compensate harmonic related problems. The instantaneous real-power theory with adaptive-fuzzy-hysteresis current controller is adopted for the active

power line conditioner system. The projected digital controller part is tested and implemented in FPGA device using Xilinx ISE-iMPACT.

6.5.1. FPGA Architecture

The FPGA consists of configurable logic blocks along with configurable interconnection resources. The input / output blocks provide the interface between the FPGA processor and the real time application [138]. The general schematic structure of an FPGA is shown in Fig.6.20.

Programmable Logic block (PLB): The programmable (configurable) logic block consists of configurable logic blocks and is used to implement custom combinational or sequential logic. It is composed of Look Up Table (LUT) controlled by 4-inputs to implement combinational logic and D-Flip-Flop for sequential logic. A MUX is used to select between using the output of the combinational logic directly and using the output of the Flip-Flop. One CLB is programmed by implementing the truth table of the logical function to the LUT (16-bit) and the control bit of the MUX (1-bit). The users can also configure the LUT in the CLB as read / write RAM locations. Some FPGA allows configuration of their LUTs as Dual port RAMs; with one write and two read inputs. By using multiple copies of the CLB structure any combinational and sequential logic circuit can be implemented.

Interconnect: The interconnection resources allow the implementation of an entire digital system by connecting various individual circuits (subsystems) that have been implemented on different CLBs in an FPGA. The interconnect resources in a typical FPGA can be classified as (1) *General Purpose Interconnects:* Signal between CLBs and input output blocks can be routed through switch matrices as they travel along the horizontal and vertical interconnect lines. (2) *Direct Interconnects*: Adjacent CLBs are interconnected directly. (3) *Long Lines*: Long lines provide for high fan out, low-skew distribution of signals that must travel relatively long distances. They span the entire length or width of the interconnect area. FPGA interconnects are normally un-segmented (each wiring segment spans only one logic block before it terminates in a switch box). A switch box is a switching matrix that contains programmable interconnections to all the wiring segments that terminate inside it. By turning on some of the programmable switches within a switch box, longer paths can be constructed.

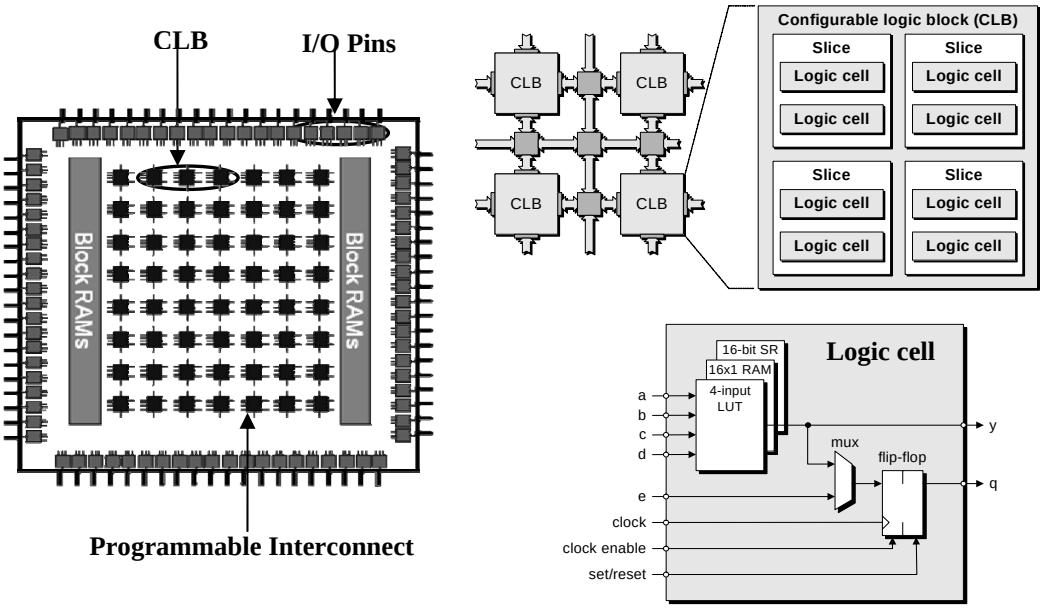


Fig.6.20 Structure of FPGA

Input Output Blocks (IOB): The IOB provides the interface between the FPGA and the real world signals. The IOB pads connect to one of the pins on the IC package so that the external signals can be input to or output from the array of logic cells. It also consists of tri-state buffers, which enable the signals to be input or output from the logic array. Flip flops are provided so that the input and the output values can be stored within the IOB. Each IOB has also got variety of other features like re programmability of the input threshold to respond to either TTL or CMOS logic levels. It also incorporates slew rate control of the output signal and includes an internal pull up resistors to avoid floating inputs.

6.5.2. Configuring FPGAs

FPGAs are not programmed directly. Synthesis tools translate the code into bit stream, which is downloaded to the configuration memory of the FPGA. Commonly, hardware description languages are used to configure the device. However, recent trends also offer the possibility using high level languages. Furthermore, there are library and graphical tool based solution which is optimized for a specific device. This reduces the development time for the designer.

Hardware description language: Using HDL programming is the most common approach to configure an FPGA. There are two dominating languages, VHDL and

Verilog. VHDL was developed in the 1980s by the Department of Defense and is essentially as a subset of the ADA with extensions for describing hardware. Verilog was originally C-like programming language to model hardware and later became an IEEE standard like VHDL.

High level language: There are also approaches using high level languages that make designing FPGA application more like software development. *System C* is a C++ library that allows specifying and simulating hardware processes using C++ syntax. *Handel-C* is an extended subset of ANSI C that allows developers to specify their designs with C. It can be synthesized directly for implementation on FPGAs. With Accelchip it is possible to generate VHDL or Verilog code block for common MATLAB DSP functions.

Library-based solutions: Recently, the Library-based functions are used for rapid implementation in many FPGA designs. Therefore the FPGA manufacturer Xilinx and Altera offer parameterized macros to generate code for common blocks such as arithmetic functions or specialized memories. The output of the macros is HDL code that can be included in the developer synthesis process.

Graphical tool based design: The MATLAB / Xilinx tool and LABVIEW are providing high-level logical blocks for designing high-performance digital control system. These tools provide automatic synthesis and translate the code into bit stream, which is implemented to the configuration memory of the FPGA board.

6.5.3. FPGA controller design

The performance of the FPGA controller based active power line conditioner is verified through system generator / Xilinx platform. The Xilinx System Generator is a tool that allows high-level tool for designing high-performance systems to implement on FPGA processor. A close interconnection with the MATLAB / Simulink software makes the implementation of complex hardware designs an easy task. All of the down-stream FPGA implementation steps including synthesis and place and route are automatically performed to generate an FPGA programming file. To design and dump on FPGA using the Simulink / Xilinx simulation model, the Gateway In and Gateway Out define the boundary of the FPGA. Instantaneous real-power theory with adaptive-fuzzy-HCC technique is designed and implemented in the FPGA-kit using a Xilinx system generator [141-143]. Fig.6.21 shows the block diagram of the instantaneous

real-power theory with adaptive-fuzzy-HCC Controller design using Xilinx blockset / Matlab. The following steps are carried out to design the FPGA controller.

Gateway-In: The instantaneous real-power theory and adaptive-fuzzy-HCC technique is designed using the Simulink / Xilinx Blockset. The three-phase supply voltages, source currents and the dc-link capacitor voltage are sensed, which are the inputs of the controller. These sensed signals are sent through the Xilinx gateway-in, which converts integer, double and fixed-point to Xilinx fixed-point.

Instantaneous real-power theory: The Xilinx block-set is used to compute the design of the controller. The 10-bit fixed-point source voltages and currents are transformed into the $\alpha-\beta$ coordinate voltage by Clarke transformation. Let the instantaneous real-power be calculated from the $\alpha \; and \; \beta$ in terms of current and voltage. This instantaneous real power(p_{ac}) passes through a digital filter for eliminating the higher order components and calculates the real power losses $\overline{p_{ac}}$. The dc power loss $p_{dc(Loss)})$ is calculated from dc-voltage of the inverter using the PI-Controller. The instantaneous real-power(p) is calculated from the real power loss and the dc power loss. The instantaneous current on the $\alpha-\beta$ coordinates of $i_{c\alpha} \; and \; i_{c\beta}$ are divided into two kinds of instantaneous current components; first is real-power losses and second is reactive-power losses, but this controller computes only the real-power losses. This approach reduces the calculations and is better in performance than the conventional methods. The instantaneous real-power generates the 10-bit reference currents $i_{sa}^*, i_{sb}^* \; and \; i_{sc}^*$ required to compensate the load current harmonics and reactive power without any time delay.

Adaptive-Fuzzy-HCC: The 10-bit reference currents are compared with the 10-bit digitized actual currents$(i_{sa}, i_{sb} \; and \; i_{sc})$ to generate switching pulses using the adaptive-fuzzy-HCC. The adaptive-fuzzy-hysteresis bandwidth can be modulated as a function of slope reference di_{sa}^*/dt current and supply voltage v_s which are used as inputs for fuzzy processing. The adaptive-fuzzy hysteresis band HB is the output of the fuzzy controller. This fuzzy logic controller is programmed in the S-function code and can be made as an adaptive-fuzzy block using the Mcode block. Similarly, the variable HCC is created by S-functions in MATLAB to produce gate control-pulses to drive the VSI.

Gateway-Out: The adaptive-fuzzy-HCC generates switching pulses as a fixed point that converts into Simulink fixed point through Gateway-out. The entire controller is computed and design using Xilinx block-set for FPGA implementation.

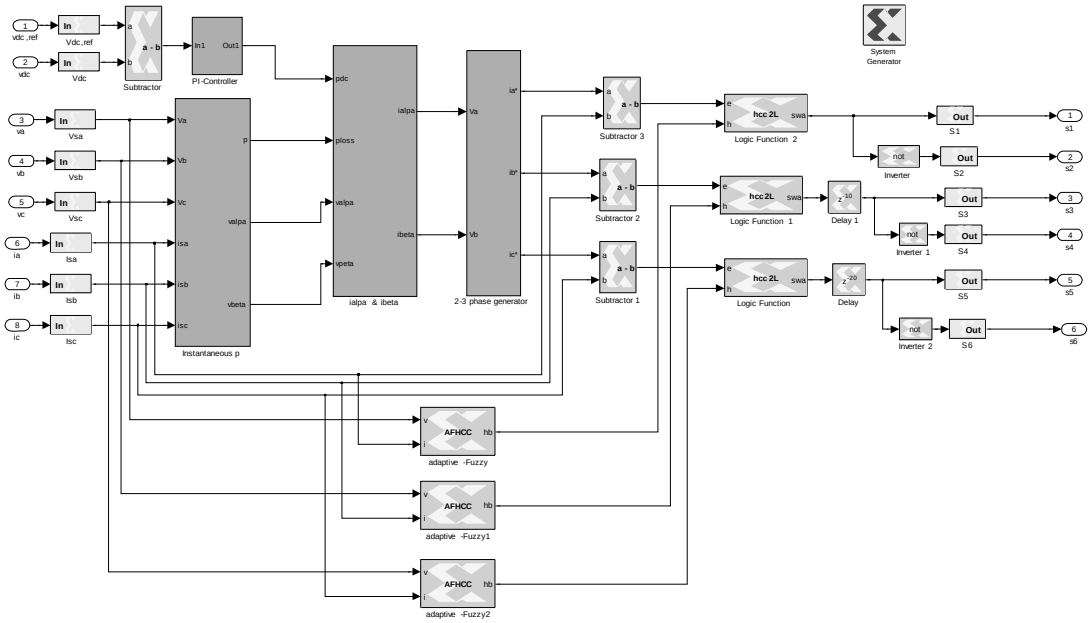


Fig.6.21 Controller design using Xilinx blockset / Matlab

System Generator: Once the controller design is completed, the hardware implementation files is generated using System Generator token properties editor. One option is to select HDL Netlist which allows the FPGA implementation steps of RTL synthesis and place and route to be performed interactively using tool specific user interfaces. Alternatively, you can select Bit-stream as the Compilation target and System Generator will automatically perform all implementations. The generated VHDL code is implemented in the FPGA kit. The FPGA processor provides the switching pulses to drive the voltage source inverter through proper interfacing circuits (protection circuits and gate driver circuits).

6.5.4. FPGA implementation

The projected digital controller is tested and implemented in FPGA hardware by using the following two methods; (1) Hardware-co-Simulation and (2) Xilinx ISE-iMPACT

6.5.4.1. Hardware-co-simulation

The system generator allows for hardware-co-simulation interfaces that make it possible to integrate an FPGA processor directly into a Simulink simulation. The system generator is a system level modeling tool that facilitates digital hardware design and provides high-level abstractions that are automatically compiled into an FPGA board. This tool provides access to underlying FPGA resources through lower level abstractions, allowing the user to implement highly efficient designs. Programming an FPGA board using the system generator the following steps are followed

- Design the suitable control method using Xilinx block-set as a Simulink model. The Xilinx block-set allows constructing bit-accuracy and cycle-accurate models of an FPGA circuit.
- The code generator has 'hardware-co-simulation' compilation targets (HDL Netlist target) that automatically create a bit-stream file.
- After creating the bit-stream, the system generator automatically integrates an FPGA hardware platform configured with this bit-stream back into Simulink as a run-time block.

The digital control method is simulated with hardware-co-simulation; results for the compiled digital control part is executed and implemented in the FPGA target device. This performs the compiled part to be tested in actual hardware and can speed up simulation dramatically.

6.5.4.2. Xilinx ISE-iMPACT

The VHDL program code is generated by the system generator after the verification and simulation of the controller design. The VHDL program is synthesized using Xilinx-ISE 10.1 software. The ISE™ (Integrated Software Environment) based FPGA design flow comprises the following steps:

- Design entry,
- Design synthesis,
- Design implementation,
- Design verification,
- Xilinx® device programming.

The Xilinx device programming uses iMPACT to create a BIT file for debugging and

downloads it into the target device XILINX / SPARTAN-3E FPGA.

Once the program is dumped to FPGA kit, it acts as an adaptive-fuzzy-HCC based FPGA controller and generates gate control switching pulses. These pulses are connected to Opto-isolator circuit for preventing the ground sharing between the FPGA-processor and power converter. The output of the Opto - isolator is connected through the driver circuit to each switching device for controlling the active power inverter.

6.5.5. Results and analysis

The input signals $(i_{sa}, i_{sb}, i_{sc}, v_{dc}, v_{sa}, v_{sb}, v_{sc})$ are converted to fixed point for digital-design. The required switching pulses $(s_1, s_2, s_3, s_4, s_5, s_6)$ are generated from the digitized adaptive-fuzzy-HCC technique. The entire control algorithm is designed using Xilinx-block set and VHDL code is generated using system generator. The VHDL code is tested and Compiled in the Xilinx-ISE 10.1 project navigator. The HDL code of analysis, synthesis and RTL schematic view is executed as shown in Fig.6.22.

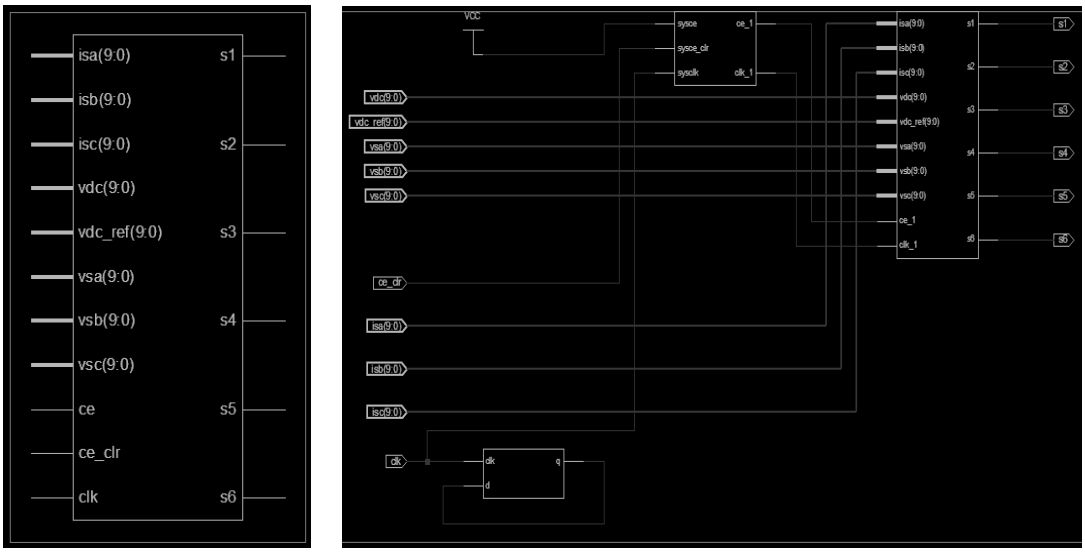


Fig.6.22 View of the RTL schematic

The three-phase supply voltages $(v_{sa}, v_{sb}\ and\ v_{sc})$, source currents $(i_{sa}, i_{sb}\ and\ i_{sc})$ and the dc-link capacitor voltage (V_{dc}) are sensed, which are the main inputs of the digital controller. These sensed analog signals are converted to fixed-point using

Xilinx gateway in. Fig.6.23 shows the input signals, which are converted to fixed point for digital-design.

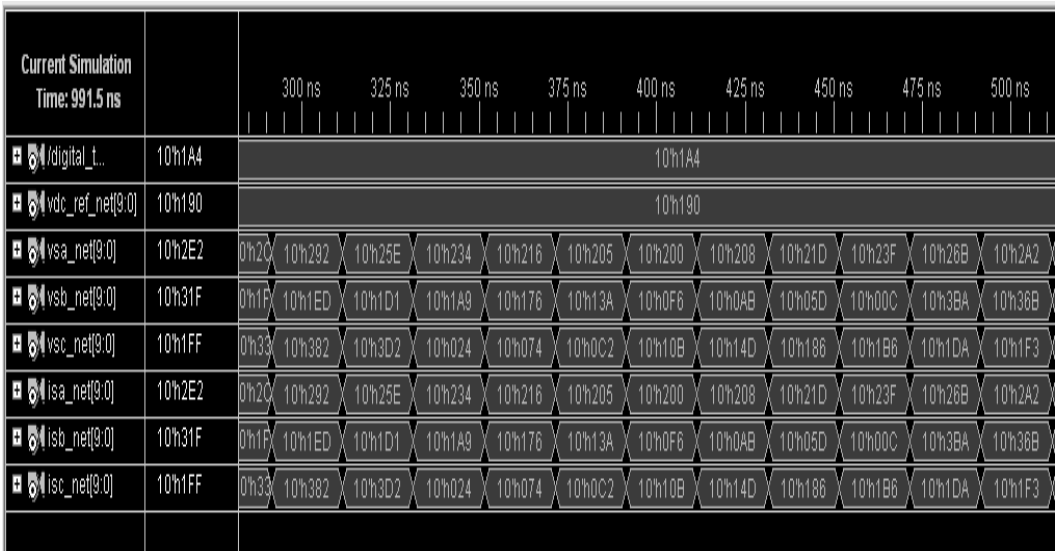


Fig.6.23 VHDL simulation result (input signals)

The six-channel gate control switching pulses are generated using adaptive-fuzzy-HCC. The VHDL program is generated by the system generator using Simulink platform. Fig.6.24 shows, six-gate switching pulses and clock signals to drive the active power inverter.

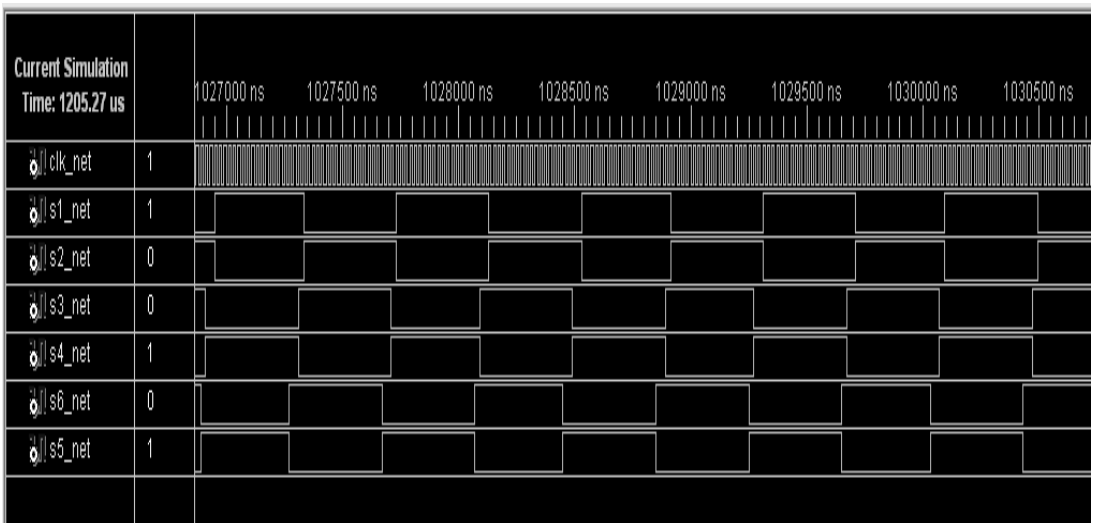


Fig.6.24 Six-channel gate driver switching pulses using VHDL code

The Matlab / Simulink based system generator provides the interface with Xilinx-Spartan3E board in Xilinx-iMPACT interface through USB cable. The USB cable is able to program the FPGA with 12-MHz speed. The compilation target automatically creates a bit-stream file and dumps it to FPGA board. This system clock frequency is set at 50 MHz at pin location C9 of the internal FPGA board. Fig.6.25 shows the photograph of Xilinx / Spatran3e FPGA implementation using Xilinx ISE tool. The proposed controller design is simulated and compilation portion is tested successfully through the FPGA kit in real time environment.

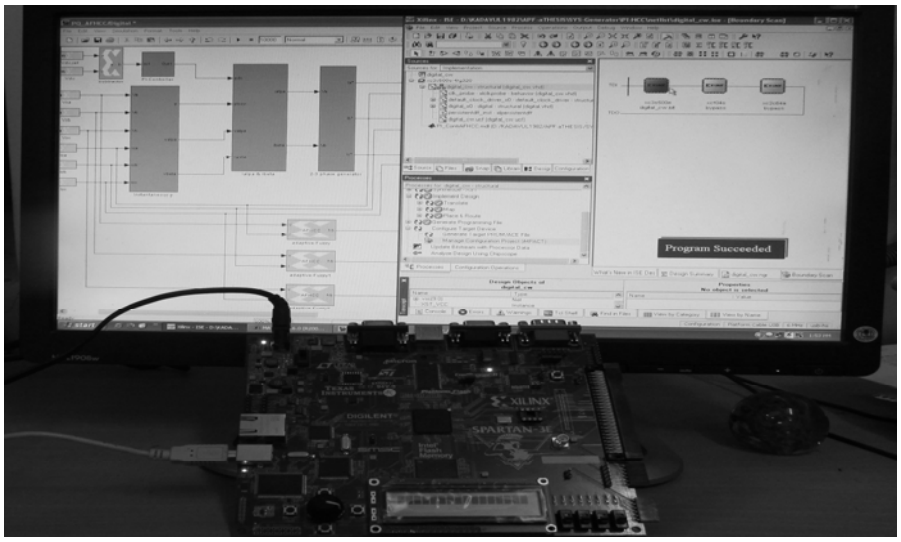


Fig.6.25 Photograph of Xilinx / Spatran3E FPGA implementation

Remarks: The instantaneous real-power theory with adaptive-fuzzy-HCC control algorithm is designed and implemented in the FPGA-kit using Xilinx ISE. The controller is modeled using the Xilinx Blockset and tested through the Matlab / Simulink environment. The Matlab / Xilinx tool lead in high-level logical blocks for designing high-performance digital systems. From the Simulink, VHDL code is generated for this particular controller using System Generator. The VHDL code is verified and synthesized in the Xilinx ISE 10.1 Platform. After synthesizing the code, the programming bit file is generated and configured on the target FPGA device. The FPGA provides the switching pulses to drive the PWM-voltage source inverter through gate driver circuits.

6.6. Conclusions

The experimental setup has been prepared and validated for three-phase shunt active power line conditioner system. The APLC is facilitated for current harmonic compensation under thyristor-rectifier load and reactive-power compensation under inductor load. For hardware implementation, the modified-SRF with space vector modulation and adaptive-fuzzy-HCC techniques are worked out. The modified-SRF method is used to extract the reference currents from the distorted load currents. This method is incorporated with a simplified unit vector generation for vector orientation instead of the PLL - circuit. The direct current control approach based SVM technique uses the space vectors, according to the region where the output voltage vector is located. However, this technique indicates more switching power losses due to fixed frequency that degrades APLC performance to some extent. The indirect current control adaptive-fuzzy-HCC calculates the hysteresis bandwidth using fuzzy logic controller without precise knowledge of the APLC parameters (interface inductor and dc-link capacitor voltage). This controller reduces the switching power losses and improves the active power line conditioner performances. The control algorithms are demonstrated through the TMS320F240 Digital Signal Processor for active power line conditioner system. The experimental results reveal that the active power line conditioner is compensating current harmonics as well as the reactive-power in the power system. The comparison of the modified-SRF with space vector modulation (THD=4. 6 %) and adaptive-fuzzy-HCC (THD=3. 7 %) techniques are investigated. The results indicate the modified-SRF with adaptive-fuzzy-HCC is providing better performance than SVM technique. These techniques are showing the measurement of the THD is less than 5% that is in compliance with IEEE-519 and IEC 61000-3 harmonic standards.

The study of the FPGA controller is discussed for three-phase active power line conditioner using Matlab / system generator and ISE-Xilinx. The objective is to demonstrate how the control circuit could be simplified by the use of FPGAs. The controller is validated for proposed instantaneous real-power theory with adaptive-fuzzy-HCC. The FPGA based APLC controller is verified and the complete active power line conditioner system can be proceeded to experiment that would be attempted as a future work.

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

7.1. General Conclusions

The three-phase shunt active power line conditioner facilitates reduction of current harmonics and reactive power compensation in the distribution system. The compensation process uses suitable control method to extract the reference-current while controlling dc-link capacitor voltage of the inverter. The active power line conditioner is implemented with PWM-current controlled voltage source inverter and the switching patterns are generated from the various techniques like TCCC, TPCC, SVM, fixed-HCC, adaptive-HCC and adaptive-fuzzy-HCC. The different methods of reference current extraction and current control techniques are executed and investigated for active power line conditioner system, thus obtaining the following conclusions:

- PI / PID / FLC / PI-FLC with indirect PWM-current controller methods are simulated from sensing dc-voltage, supply voltages and currents (neglecting to sense load currents and compensation currents). It reduces the number of sensors and hence decreases the complexity of the controller. The PI / PID / FLC / PI-FLC methods have been used to estimate the peak amplitude of reference current by controlling the dc-voltage of the inverter. The PI / PID / Fuzzy / PI-FLC methods along with various PWM-current control techniques are validated for diode / thyristor-rectifier load. However, the PI and PID controller requires precise linear mathematical calculation of the system, which is difficult to obtain under parametric variations, non-linearity and load disturbances. Hence, it is difficult to optimize APLC performance. This drawback is rectified by using fuzzy logic controller. It does not require an accurate numerical calculation; it can work with imprecise inputs. To improve the PI-controller, it is combined with the FLC and is applied in the active power line conditioner. The PI and FLC method is combined for efficient

active power line conditioning. This controller handle nonlinearity, and more robust than other methods. The PI-FLC facilitates reduction of ripples in the dc-link capacitor of the PWM-inverter.

- The proposed instantaneous real-power theory is derived from the conventional $p-q$ theory. The algorithm is developed from sensing dc-voltage, three-phase source voltages and currents only. The instantaneous $\alpha-\beta$ current components are calculated from the $v_\alpha - v_\beta$ with instantaneous real power losses, and the reactive-power is considered as zero. However, the reactive-power does not contribute to energy transfer between the source and the load. This method is simple in computation and different from conventional methods. The instantaneous real-power theory with various indirect PWM-current control techniques based active power line conditioner system is validated under diode / thyristor-rectifier load. It is observed that it is possible to extract reference current. This method is found to be a better technique at a lower hardware use.

- The sinusoidal extraction controller consists of a positive sequence voltage detector as well as an instantaneous real-power concept. The sinusoidal extraction controller with various indirect PWM-current control techniques based active power line conditioner system is validated under diode / thyristor-rectifier load. This control strategy makes the active power line conditioner compensate the current of nonlinear load to force the compensated source current to become sinusoidal and balanced. However, this controller requires large computation time compared to instantaneous power control strategy.

- The fryze power theory method reduces the reference current calculation, since it works directly with *abc*-phase voltage and line currents. The elimination of the Clarke transformation makes this control strategy simple to implement. However, this theory has no consistent expression to calculate the three-phase instantaneous reactive-power, to compensate for the reactive-power to the

load. The Fryze power theory along with various PWM-current control techniques based active power line conditioner system is validated under different non-linear load conditions.

- The conventional and modified-SRF along with various current control techniques based active power line conditioner system is executed and verified under diode / thyristor-rectifier load . The modified-SRF used simple and efficient unit vector generator for vector orientation without using PLL circuit. The modified-SRF gives better performance than conventional-SRF method in terms of V_{dc}-settling time and harmonics as well as reactive-power compensation.

- The experimental set-up is prepared and validated for three-phase shunt active power line conditioner system. For hardware implementation, the modified-SRF with adaptive-fuzzy-hysteresis current controller is demonstrated. The adaptive-fuzzy-HCC calculates the hysteresis bandwidth effectively with the help of fuzzy logic and reduces the switching power losses. The projected control algorithm is demonstrated through the TMS320F240 Digital Signal Processor for active power line conditioner system.

- The instantaneous real-power theory and adaptive-fuzzy-HCC control algorithm is designed and implemented in the FPGA-kit using Xilinx ISE. Initially, the controller is modeled using the Xilinx Blockset and tested through the Matlab / Simulink. From the Simulink, VHDL code is generated for this particular controller using System Generator. The generated VHDL code is verified and synthesized in the Xilinx ISE 10.1. After synthesizing the code, the programming bit file is generated and configured on the target FPGA-device. The FPGA provides the switching pulses to drive the PWM-inverter through gate driver circuits. The FPGA active power line conditioner controller is verified and the complete active power line conditioner system can be proceeded to experiment that would be attempted as a future work.

These obtained results reveal that the active power line conditioner is compensating current harmonics as well as reactive-power. The adaptive-fuzzy-HCC technique reduces the switching power losses and improves the active power line conditioner performance in comparison with the TCCC, TPCC, SVM, fixed-HCC and the adaptive-HCC. The measured total harmonic distortion of the source currents is in compliance with IEEE 519 and IEC 61000-3 harmonic standards.

7.2. Scope for future work

The following can be taken up as future work.

- A complete FPGA based controller for APLC can be developed that would add flexibility for controller design. This would significantly reduce hardware requirement and it can further be extended to ASIC development.
- Recently non-renewable energy (NRE) sources are getting lot of attention and in many cases these power sources are feeding a grid which could support non-linear loads as well. Such systems would require an integrated APLC. A comprehensive model including NRE sources, APLC and grid can be taken up as a further investigation.
- To meet higher power requirements multi-level inverter would be used, an APLC using such inverter and control strategies suitable for such inverter should be taken up.
- Reactive power compensation and harmonic compensation are essentially two different requirements from the frequency of operation of inverter perspective. Harmonic compensation requires a high frequency low power inverter where as reactive power requires low frequency high power operation. Therefore, it is important to develop a suitable methodology such that these tasks are decoupled and compensation can be done by two different inverters.

REFERENCES

[1] Arindam Ghosh, Gerard Ledwich *"Power Quality enhancement using Custom Power Devices"* Springer, First Indian reprint-2009

[2] E.Wald F.Fuchs, Mohammad A.S.Masoum *"Power Quality in Power Systems and Electrical Machines"* Academic press is an imprint of Elsevier, 2008

[3] Nitin Gupta, S. P. Singh and R. C. Bansal "A Digital Signal Processor Based Performance Evaluation of Three phase Four-wire Shunt Active Filter for Harmonic Elimination, Reactive Power Compensation, and Balancing of Nonlinear Loads under Non-ideal Mains Voltages" *Electric Power Components and Systems*, Vol. 40, No. 10, pp. 1119–1148, July-2012

[4] Naimish Zaveri and Ajitsinh Chudasama "Control strategies for harmonic mitigation and power factor correction using shunt active filter under various source voltage conditions" *Electrical Power and Energy Systems*, Vol. 42, No. 1, pp. 661–671, Nov-2012

[5] Ray Arnold "Solutions to the power quality problem" *Power Engineering Journal*, Vol.15, No.2, pp.65-73, April-2001

[6] Hirofumi Akagi "Active Harmonic Filters" *Proceedings of the IEEE*, Vol. 93, No. 12, pp.2128-2141, Dec-2005.

[7] F.Z.Peng, H.Akagi, A.Nabae "A Novel Harmonic Power Filter" *PESC*, pp. 1151-1158, April-1988.

[8] Karuppanan P and Kamala Kanta Mahapatra "PI, PID and Fuzzy Logic Controlled Cascaded Voltage Source Inverter based Active Filter for Power Line Conditioners" *WSEAS Transaction on Power Systems*, Vol.6, No.4, pp.100-109, Oct-2011

[9] Yi Tang, Poh Chiang Loh, Peng Wang, Fook Hoong Choo, Feng Gao, and Frede Blaabjerg "Generalized Design of High Performance Shunt Active Power Filter With Output LCL Filter" *IEEE Trans on Industrial Electronics*, Vol. 59, No. 3, pp. 1443-1452, March-2012.

[10] M.A.Hannan and Azah Mohamed "PSCAD/EMTDC Simulation of Unified Series-Shunt Compensator for Power Quality Improvement" *IEEE Trans on Power Delivery*, Vol. 20, No. 2, pp.1650-1656, April-2005

[11] W.M.Grady, M.J.Samotyj and A.H.Noyola "Survey of Active Power Line Conditioning Methodologies" *IEEE Trans on Power Delivery*, Vol.5, No.3, pp. 1536-1542, July-1990.

[12] S. Bhattacharyya, S. Cobben, P. Ribeiro and W. Kling "Harmonic emission limits and responsibilities at a point of connection" *IET Gener. Transm. Distrib.*, Vol. 6, No. 3, pp. 256–264, March-2012

[13] Francisco C.De La Rosa *"Harmonics and Power Systems"* CRC press, First Indian reprint-2010

[14] IEEE Working Group on Power System Harmonics "Power System Harmonics: An Overview" *IEEE Power Engineering Review*, Vol.3, No.8, pp. 27-28, Aug-1983

[15] T.C.Shuter, H.T.Vollkommer, Jr.T.L.Kirkpatrick "Survey of Harmonic Levels on the American Electric Power Distribution System" *IEEE Trans on Power Delivery*, Vol. 4, No. 4, pp.2204-2213, Oct-1989.

[16] Christopher K. Duffey and Ray. P. Stratford "Update of Harmonic Standard IEEE-519: IEEE Recommended Practices and Requirements for Harmonic Control in Electric Power Systems" *IEEE Trans on Industrial Applications*, Vol.25, No.6, pp.1025-1034, Nov/Dec-1989.

[17] Joseph S. Subjak., JR and John S. Mcquilkin "Harmonics - Causes, Effects, Measurements, and Analysis: An Update" *IEEE Trans on Industrial Applications*, Vol.26, No.6, pp.1034-1042, Nov/Dec-1990.

[18] Alexander E. Emanuel, John A. Orr, David Cyganski and Edward M. Gulachenski, "A Survey of Harmonic Voltages and Currents at the Customer's Bus" *IEEE Transactions on Power Delivery*, Vol. 8, No. 1, pp.411-421, Jan-1993.

[19] IEEE Working group on Non-sinusoidal Situations "Practical Definitions for Powers in Systems with Non sinusoidal Waveforms and Unbalanced Loads: A Discussion" *IEEE Transactions on Power Delivery*, Vol. 11, No. 1, pp.79-87, Jan-1996

[20] Eric J. Davis, Alexander E. Emanuel, and David J. Pileggi "Harmonic Pollution Metering: Theoretical Considerations" *IEEE Trans on Power Delivery*, Vol. 15, No. 1, pp.19-23, Jan-2000

[21] Jacques L. Willems, Jozef A. Ghijselen, and Alexander E. Emanuel "The Apparent Power Concept and the IEEE Standard 1459-2000" *IEEE Trans on Power Delivery*, Vol. 20, No. 2, pp.876-884, April-2005

[22] Salvador Orts-Grau, Jose Carlos Alfonso-Gil, Francisco J. Gimeno-Sales, and Salvador Segui-Chilet "New Resolution of the Unbalance Power According to Std. 1459" *IEEE Trans on Power Delivery*, Vol.25, No.1, pp. 341-350, Jan-2010.

[23] Predrag D. Poljak, Miodrag D. Kusljevic and Josif J. Tomic "Power Components Estimation According to IEEE Standard 1459–2010 Under Wide-Range Frequency Deviations" *IEEE Trans on Instrumentation and Measurement*, Vol. 61, No. 3, pp.636-644, Mar-2012

[24] Yao Xiao and Xavier Yang "Harmonic Summation and Assessment Based on Probability Distribution" *IEEE Trans on Power Delivery*, Vol. 27, No. 2, pp.1030-1032, April-2012

[25] Muhammad H. Rashid "*Power Electronics Handbook*" Academic Press, An imprint of Elsevier (ISBN: 0-12-581650-2), 2001.

[26] Karuppanan P and Kamala Kanta Mahapatra "A Novel Control Strategy based Shunt APLC for Power Quality Improvements" *IEEE International Conference on Power, Control and Embedded Systems (ICPCES)* -2010

[27] Kamala Kanta Mahapatra "*Active Harmonic current compensation using Hard and soft-switched Inverters*" Thesis for the degree of Doctor of Philosophy, Indian Institute of Technology-Kanpur, June-1999

[28] Zainal Salam, Tan Perng Cheng and Awang Jusoh "Harmonics Mitigation Using Active Power Filter: A Technological Review" *ELEKTRIKA*, Vol. 8, No. 2, pp. 17-26, 2006.

[29] Donghua Chen and Shaojun Xie "Review of the control strategies applied to active power filters" *IEEE International Conference on Electric Utility Deregulation, Restructuring and Power Technologies*, pp. 666-670, April-2004

[30] Maria Isabel Milanes Montero Enrique Romero Cadaval and Fermin Barrero Gonzalez "Comparison of Control Strategies for Shunt Active Power Filters in Three-Phase Four-Wire Systems" *IEEE Trans on Power Electronics*, Vol. 22, No. 1, pp.299-236, Jan-2007

[31] Tzung-Lin Lee and Shang-Hung Hu "Discrete Frequency-Tuning Active Filter to Suppress Harmonic Resonances of Closed-Loop Distribution Power Systems" *IEEE Trans on Power Electronics*, Vol. 26, No. 1, pp.137-148, Jan-2011

[32] Hirofumi Akagi, Edson hirokazu watanabe and Mauricio Aredes "*Instantaneius power theory and applications to power conditioning*" IEEE-press, 2007

[33] M. Depenbrock "The FBD method a generally applicable tool for analyzing power relations" *IEEE Transactions on Power Systems*, Vol. 8, No. 2. May-1993

[34] Hirofimi Akagi, Yoshihira Kanazawa and Akira Nabae “Instantaneous Reactive Power Compensators Comprising Switching Devices without Energy Storage Components” *IEEE Trans on Industry Applications*, Vol.I1-20, No.3, pp. 625-630, May/June-1984

[35] S. Bhattacharya, D.M. Divan, B. Banerjee, "Synchronous Reference Frame Harmonic Isolator Using Series Active Filter", *Proc. 4th EPE, Florence*, Vol. 3, pp 030-035, 1991.

[36] Edson H. Watanabe, Richard M. Stephan and Mauricio Aredes “New Concepts of Instantaneous Active and Reactive Powers in Electrical Systems with Generic Loads”- *IEEE Trans on Power Delivery*, Vol.8, No.2, pp.697-703, April-1993

[37] Fang Zheng Peng and Jih-Sheng Lai “Generalized Instantaneous Reactive Power Theory for Three-phase Power Systems” *IEEE Trans on Instrumentation and measurement*, Vol.45, No.1, pp. 293-297, Feb-1996

[38] Nassar Mendalek, Kamal Al-Haddad, Louis A.Dessaint and Farhat Fnaiech “Nonlinear Control Strategy Applied to A Shunt Active Power Filter” *proceedings on IEEE conference*, pp.1877-1882, 2001

[39] Reyes S. Herrera, Patricio Salmeron and Hyosung Kim “Instantaneous reactive power theory applied to active power filter compensation: Different approaches, assessment, and experimental results” *IEEE Trans on Industrial Electronics*, Vol. 55, No. 1, pp. 184–196, Jan-2008

[40] Salem Rahmani, Nassar Mendalek and Kamal Al-Haddad “Experimental Design of a Nonlinear Control Technique for Three-Phase Shunt Active Power Filter” *IEEE Transactions on Industrial Electronics*, Vol. 57, No. 10, pp. 3364-3375, Oct-2010.

[41] Rondineli Rodrigues Pereira, Carlos Henrique da Silva, Luiz Eduardo Borges da Silva, Germano Lambert-Torres and Joao O. P. Pinto “New Strategies for Application of Adaptive Filters in Active Power Filters” *IEEE Trans on Industry Applications*, Vol. 47, No. 3, pp.1136-1141, May/June-2011

[42] Ricardo Lucio de Araujo Ribeiro, Christian Cesar de Azevedo, and Raphaell Maciel de Sousa “A Robust Adaptive Control Strategy of Active Power Filters for Power-Factor Correction, Harmonic Compensation, and Balancing of Nonlinear Loads” *IEEE Trans on Power Electronics*, Vol. 27, No. 2, pp. 718-730, Feb-2012

[43] Abdelmadjid Chaoui, Jean Paul Gaubert, Fateh Krim, Gerard Champenois “PI Controlled Three-phase Shunt Active Power Filter for Power Quality Improvement” *Electric Power Components and Systems,* Vol.35,No.12, pp. 1331–1344, Sep-2007

[44] R.D. Patidar and S. P. Singh "Digital Signal Processor Based Shunt Active Filter Controller for Customer-generated Harmonics and Reactive Power Compensation" *Electric Power Components and Systems*, Vol.38,No.8, pp.937–959, May-2010

[45] Avik Bhattacharya, and Chandan Chakraborty "A Shunt Active Power Filter With Enhanced Performance Using ANN-Based Predictive and Adaptive Controllers" *IEEE Trans on Industrial Electronics*, Vol. 58, No. 2, pp.421-428, Feb-2011.

[46] Zhongfu Zhou and Yanzhen Liu "Pre-sampled data based prediction control for active power filters" *Electrical Power and Energy Systems*, 37, pp.13–22, 2012

[47] Maria Marinelli and Antonio Dell Aquila "Improved Current Control of Active Power Filters Using Genetic Algorithms" *IEEE Symposium on Industrial electronics*, May-2004.

[48] R. Belaidi,A. Haddouche, and H. Guendouz "Fuzzy Logic Controller Based Three-Phase Shunt Active Power Filter for Compensating Harmonics and Reactive Power under Unbalanced Mains Voltages" *Energy Procedia*, 18, pp. 560 – 570, 2012

[49] S. Saad and L. Zellouma "Fuzzy logic controller for three-level shunt active filter compensating harmonics and reactive power" *Electric Power Systems Research*, Vol.79, No.10, pp.1337–1341, 2009

[50] Karuppanan P and Kamala Kanta Mahapatra "PI and fuzzy logic controllers for shunt active power filter-A report" *ISA Transactions* Vo.51, No.1, pp.163–169, 2012

[51] Brod D.M, Novotny D.M "Current control of VSI-PWM Inverter" *IEEE Trans on Industry Applications*, Vol.IA-21 No.3, pp.562-570, May-1985

[52] Akira Nabae, Satoshi Ogasawara, and Hirofumi Akagi, "A Novel Control Scheme for Current-Controlled PWM Inverters" *IEEE Trans on Industry Applications*,Vol 1A-22, No.4, pp.562-570, July-1986

[53] Bimal K Bose "An Adaptive Hysteresis-Band Current Control Technique of a Voltage-Fed PWM Inverter for Machine Drive System" *IEEE Trans on Industrial Electronics*, Vol.31, No.5, pp. 402-408, Oct-1990.

[54] Marian P. Kaimierkowski, Maciej A. Dzieniakowski, and Waldemar Sulkowski "Novel Space Vector Based Current Controllers for PWM-Inverters" *IEEE Trans on Power Electronics*, Vol. *6.* No. 1. pp.158-166, Jan-1991

[55] J.Dixon, S.Tepper and L.Moran "Practical Evaluation of Different Modulation Techniquies for Current-Controlled Voltage Source Inverters" *IEE Proc. Electr Power Appl.,* Vol.143, No.4, pp.301-306, 1996.

[56] Bong-Hwan Kwon, Tae-Woo Kim, and Jang-Hyoun Youm "A Novel SVM-Based Hysteresis Current Controller" *IEEE Trans on Power Electronics,* Vol. 13, No. 2, pp.297-307, March-1998.

[57] G.H. Bode and D.G. Holmes "Implementation of Three Level Hysteresis Current Control for a Single Phase Voltage Source Inverter" *IEEE Proceedings on Power Electronics Specialists Conference,* 2000

[58] Murat Kale and Engin Ozdemir "An adaptive hysteresis band current controller for shunt active power filter" *Electric Power Systems Research,* Vol.73, No.2, pp.113–119, 2005

[59] B. Mazari and F. Mekri "Fuzzy Hysteresis Control and Parameter Optimization of a Shunt Active Power Filter" *Journal of Information Science and Engineering,* 21, pp.1139-1156, 2005

[60] N. Gupta, S. P. Singh, S. P. Dubey "DSP based adaptive hysteresis-band current controlled active filter for power quality conditioning under non-sinusoidal supply voltages" *International Journal of Engineering, Science and Technology,* Vol. 3, No. 4, pp. 236-252, 2011

[61] S. Karimi, P. Poure, S. Saadate and E. Gholipour "FPGA-based fully digital controller for three-phase shunt active filters" *International Journal of Electronics*, Vol. 95, No. 8, pp.805–818, Aug-2008

[62] M.El. Habrouk, M.K. Darwish and P.Mehta "Active power filters: A review" I*EE Proc.-Elertr. Power Appl.,* Vol. 147, No. 5, pp. 403-413, Sept-2000.

[63] Bhim Singh, Kamal Al-Haddad & Ambrish Chandra, "A Review of Active Filter for Power Quality Improvements" *IEEE Trans on Industrial Electronics,* Vol.46, No.5, pp. 960-970, Oct-1999.

[64] Srinivas Ponnaluri and Axel Brickwedde, "Generalized System Design of Active filters," *IEEE Conference on PESC,* June-2001

[65] N. Mohan, T. M. Undeland and W. P. Robbins, "*Power electronics: converters, applications and design*," John Wiley and Sons, 1995

[66] Alper Terciyanli, Muammer Ermis and Isik Cadirci *"*A Selective Harmonic Amplification Method for Reduction of kVA Rating of Current Source Converters in Shunt Active Power Filters" *IEEE Trans on Power Delivery,* Vol. 26, No. 1, pp. 65-78, Jan-2011.

[67] Xiong Du, Luowei Zhou, Hao Lu, and Heng-Ming Tai "DC Link Active Power Filter for Three-Phase Diode Rectifier" *IEEE Trans on Industrial Electronics*, Vol. 59, No. 3, pp. 1430-1442, March-2012.

[68] Ravindra Kumar Singh "Multiphase Inverter Topology and its Modulation Technique for Optimal Harmonic Output" *International conference on Power Electronics, Drives and Energy Systems (PEDES),* Dec-2006

[69] V.Khadkikar, A. Chandra, B. Singh "Digital signal processor implementation and performance evaluation of split capacitor, four-leg and three H-bridge-based three-phase four-wire shunt active filters" *IET Power Electronics,* Vol. 4, No. 4, pp. 463–470, 2011.

[70] L.Gyugyi, E.C.Strycula "Active AC Power Filters" *Proc of IEEE/IAS Annu. Meeting*, Vol.19-C, pp. 529-535, 1976.

[71] Hirofumi Akagi "Trends in Active Power Line Conditioners" *IEEE Trans on Power Electronics*, Vol.9, No.3, pp. 263-268, May-1994.

[72] George J.Wakileh *"Power System Harmonics: Fundamentals, Analysis and Filter Design"* Springer, First Indian reprint-2007

[73] S. K. Jain, P. Agrawal, H.O. Gupta, "Fuzzy logic controlled shunt active power filter for power quality improvement," *IEE Proc. Electr.Power Appl*., Vol.149, No.5, pp.317-328, Sept-2002

[74] Abdelmadjid Chaoui, Jean-Paul Gaubert, Fateh Krim and Laurent Rambault "On the Design of Shunt Active Filter for Improving Power Quality" *IEEE International symposium on Industrial Electronics*, pp.31-37, July-2008

[75] S. J. Chiang, J.M. Chang, "Design and Implementation of the parallelable active power filtre," *Proc. 30th Annual IEEE Power Electr. Specialists Conference (PESC-99),* Vol.1, pp. 406-411, June/July-1999.

[76] Arun karuppaswamy.B *"Synchronous Reference Frame Strategy based STATCOM for Reactive and Harmonic Current Compensation"* Thesis for the degree of Master of Technology, National Institute of Technology-calicut, June-2007

[77] Shailendra Kumar Jain and Pramod Agarwal, "Design Simulation and Experimental investigation, on a shunt active power filter for harmonics, and reactive power compensation," *Electric Power Components and Systems*, Vol.31, No.7, pp. 671-692, July-2003.

[78] G.K. Singh, A.K. Singh, R.Mitra, "A simple fuzzy logic based robust active power filter for harmonics minimization under random load variation," *Electric Power Systems Research*, Vol.77, No.8, pp.1101-1111, June-2007, 2007.

[79] M. Rastogi, R. Naik, N. Mohan, "A comparative evaluation of harmonic reduction techniques in three-phase utility interface of power electronic loads," *IEEE Trans on Industry Applications*, Vol. 30, No. 5, pp.1149-1155, Sept/Oct-1994.

[80] Helder J. Azevedo, Jose M. Ferreira, Antonio P. Martins and Adriano S. Carvalho "Direct current control of an active power filter for harmonic elimination, power factor correction and load unbalancing compensation" *EPE, power electronics in generation, transmission and distribution of electrical energy*,Toulouse,2003

[81] Luis A. Moran, Juan W. Dixon, and Rogel R. Wallace "A three-Phase active power filter operating wth fixed switching frequency for reactive power and current harmonic compensation" I*EEE Transaction on Industrial Electronics*, Vol. 42, No. 4, pp.402-408, Aug-1995

[82] A.M.Massoud, S.J.Finney, and B.W.Williams "Review of Harmonic Current Extraction Techniques for an Active Power Filter" *International Conference on Harmonies and Quality of Power*, pp. 145-159, 2004.

[83] Sergio Alejandro Gonzalez, Rogelio Garcia-Retegui and Mario Benedetti "Harmonic computation technique suitable for active power filters" *IEEE Trans on Industrial Electronics*, Vol. 54, No. 5, pp. 2791–2796, Oct-2007

[84] Bhim Singh, Ambrish Chandra, Kamal Al-Haddad "Computer-Aided Modeling and Simulation of Active Power Filters" *Electric Machines & Power Systems*, Vol.27, No.11, pp.1227–1241,1999

[85] Karuppanan P and Kamala kanta Mahapatra "PLL with PI, PID and Fuzzy Logic Controllers based Shunt Active Power Line Conditioners" IEEE *International Conference on Power Electronics, Drives and Energy Systems* (*PEDES)* -2010

[86] Abdelmadjid Chaoui, Jean-Paul Gaubert and Fateh Krim "Power quality improvement using DPC controlled three-phase shunt active filter" *Electric Power Systems Research* 80, pp.657–666, 2010.

[87] G. N. Pillai, Arindam Ghosh and Avinash Joshi "Torsional Interaction Studies on a Power System Compensated by SSSC and Fixed Capacitor" *IEEE Transactions on Power Delivery*, Vol. 18, No. 3, pp.988-994, July-2003

[88] J. C. Basilio and S. R. Matos "Design of PI and PID Controllers With Transient Performance Specification" *IEEE Trans on Education*, Vol. 45, No. 4, pp.364-370, Nov-2002

[89] Hocine Benalla and Hind Djeghloud "Shunt Active Filter Controlled by Fuzzy Logic" *J. King Saud Univ., Eng. Sci.*, Vol. 18, No.2, pp. 231-247,2005

[90] V. S. C. Raviraj and P. C. Sen "Comparative Study of Proportional–Integral, Sliding Mode, and Fuzzy Logic Controllers for Power Converters" *IEEE Tran on Industry Applications,* Vol 33, No. 2, pp. 518-524, Mar/April-1997

[91] C. N. Bhende, S. Mishra, and S. K. Jain "TS-Fuzzy-Controlled Active Power Filter for Load Compensation" *IEEE Trans on Power Delivery,* Vol. 21, No. 3, pp.1459-1465, July-2006

[92] Maged F. Naguib and Luiz A. C. Lopes "Harmonics Reduction in Current Source Converters Using Fuzzy Logic" *IEEE Trans on Power Electronics*, Vol. 25, No. 1, pp.158-167, Jan-2010

[93] Chuen Chien Lee "Fuzzy Logic in control systems: Fuzzy Logic Controller-Part I" I*EEE Trans on Systems, Man and Cybernetics*, Vol.20, No.2, pp.404-418, March/April-1990

[94] Chuen Chien Lee "Fuzzy Logic in control systems: Fuzzy Logic Controller-Part II" *IEEE Trans on Systems, Man and Cybernetics*, Vol.20, No.2, pp.419-435, March/April-1990

[95] Karuppanan P and Kamala Kanta Mahapatra "PI with Fuzzy Logic Controller based Active Power Line Conditioners" *Asian Power Electronics Journal*, Vol.5, No.1, pp.13-18, Aug-2011

[96] Cheng Qiong and Zheng Jianyong "The Application of FBD Current Examination Method in the Three-phase Power System" *Proceedings of the 27th Chinese Control Conference*, pp. 232-235, July-2008.

[97] M. Depenbrock and V.Staudt "The FBD-Method as Tool for Compensating Total Non-Active Currents" *International Conference on Harmonics and Quality of Power ICHQP*, pp.320-324, Oct-1998

[98] Luis F.C. Monteiro, Mauricio Aredes and Joao A. Moor Neto "A Control Strategy for Unified Power Quality Conditioner" *IEEE International Symposium on Industrial Electronics*, Vol.1, pp. 391-396, 2003.

[99] Karuppanan P, Kamala Kanta Mahapatra, Jeyaraman.K and Jeraldine Viji "Fryze Power Theory with Adaptive-HCC based Active Power Line Conditioners", *IEEE International Conference on Power and Energy Systems (ICPS),*2011

[100] Leszek S. Czarnecki "Instantaneous Reactive Power p-q Theory and Power Properties of Three-Phase Systems" *IEEE Trans on Power Delivery*, Vol. 21, No. 1, pp 362-367, Jan-2006.

[101] Radu Iustin Bojoi, Leonardo Rodrigues Limongi, Daniel Roiu and Alberto Tenconi "Enhanced Power Quality Control Strategy for Single-Phase Inverters

in Distributed Generation Systems" *IEEE Trans on Power Electronics*, Vol. 26, No. 3, pp.798-806, March-2011.

[102] Rahmat Allah Hooshmand and Mahdi Torabian Esfahani "A new combined method in active filter design for power quality improvement in power systems" *ISA Transactions*, Vol.50, No.2, pp.150–158, 2011

[103] Joao Afonso, Carlos Couto, Julio Martins "Active Filters with Control Based on the p-q Theory" *IEEE Industrial Electronics Society Newsletter*, Vol. 47, No.3, pp.5-10, Sept-2000

[104] E. H. Watanabe, H. Akagi and M. Aredes "Instantaneous p-q Power Theory for Compensating Nonsinusoidal Systems" IEEE *International School on Nonsinllsoidal Currents and Compensation*, 2008

[105] Karuppanan P and Kamala Kanta Mahapatra "Shunt Active Power Line Conditioners for Compensating Harmonics and Reactive Power" *IEEE International Conference on Environment and Electrical Engineering (EEEIC)*-Poland, pp.273-276, 2010

[106] Karuppanan P, Kamala Kanta Mahapatra, Jeraldine Viji and Bhuyan Kanhu Charan "Sinusoidal Extraction Control Strategy based Shunt Active Power Line Conditioners for Enhancing Power Quality" *Journal of Electrical and Electronics Engineering*, Vol.4, No.2, pp.83-88, Oct-2011

[107] Karuppanan P, Rajesh Kumar Patjoshi, Kamalakanta Mahapatra and Ajay-D-Vimalraj "Sinusoidal Extraction Controller based on Cascaded VSI for Active Power Filter" *IEEE-INDICON*-2011

[108] Alberto Pigazo, Victor M. Moreno and Emilio J. Estebanez "A Recursive Park Transformation to Improve the Performance of Synchronous Reference Frame Controllers in Shunt Active Power Filters" *IEEE Trans on Power Electronics*, Vol.24, No.9, pp.2065-2075, Sept-2009.

[109] Bhim Singh and Vishal Verma "Selective Compensation of Power-Quality Problems through Active Power Filter by Current Decomposition" *IEEE Trans on Power Delivery*, Vol.23, No.2, pp. 792-799, Aprl-2008

[110] S.Bhattacharya, T.M.Frank, D.M.Divan and B.Banerjee "Parallel Active Filter System Implementation and Design Issuses for Utility Interface of adjustable speed drive systems" *IEEE Conference*, pp.1032-1039, 1996

[111] Subhashish Bhattacharya Deepak Divan "synchronous reference frame based controller for a hybrid series active filter system" *Industry appl. Conference, IAS-Annual meetings*, Vol.3, pp. 2531 – 2540, 1995

[112] F.Profumo, M.Bilewski, M.Pastorelli, A.Boglietti and G.Franceschini "Current Controller in Synchronous Reference Frame for High Performance AC Drives" *IEEE conference on Electrical Machines and Drives*, 1991

[113] Karuppanan P and Kamala kanta Mahapatra “A Novel SRF Based Cascaded Multilevel Active Filter for Power Line Conditioners” *IEEE*-INDICON-2010

[114] Carlos Henrique da Silva, Rondineli R. Pereira, Luiz Eduardo Borges da Silva, Germano Lambert-Torres, Joao Onofre Pereira Pinto and Edson Hideki Takauti “Modified Synchronous Reference Frame Strategy for Single Phase Hybrid Active Power Filter” *IEEE Conference on Harmonics and Quality of Power*, 2008

[115] Subhash Joshi T.G., Aby Joseph and Gautam Poddar "Active Power Factor Correction For Highly Fluctuating Industrial Load" *National Power Electronics Conference (NEPC)*, Oct-2003.

[116] Wang Xuedan, Jiang Jianguo and Gao Baichen “Lag compensation errors in active power filters based on DSP controllers” *Mining Science and Technology*, Vol.20, No.2, pp.312–316, 2010.

[117] L.R.Limongi, M.C.Cavalcanti, F.A.S.Neves and G.M.S.Azevedo “Implementation of a Digital Signal processor-Controlled Shunt Active Filter” *Electrical Power Quality and Utilization Journal*,Vol.12, No.2, pp.5-14, 2006

[118] Edris Pouresmaeil, Daniel Montesinos-Miracle, Oriol Gomis-Bellmunt and Joan Bergas-Jane “A multi-objective control strategy for grid connection of DG (distributed generation) resources” *Energy*, Vol. 35, No.12, pp.5022-5030, 2010

[119] Rajesh Gupta “Generalized Frequency Domain Formulation of the Switching Frequency for Hysteresis Current Controlled VSI Used for Load Compensation” *IEEE Trans on Power Electronics*, Vol. 27, No. 5, May-2012

[120] R.K. Behera and S.P. Das “Analysis and experimental investigation for switching frequency characterisation of a three-level ac–dc converter using frequency domain approach” *IET Power Electronics*, Vol. 4, No. 8, pp. 936–942, 2011

[121] B.N. Singh, Ambrish Chandra and Kamal AI-Haddad “Performance Comparison of Two Current Control Techniques Applied to an Active Filter” *International Conference on Harmonics and Quality of Power ICHQP*, Vol.1, pp.133-138, 1998

[122] Ali Mehrizi-Sani and Shaahin Filizadeh “An Optimized Space Vector Modulation Sequence for Improved Harmonic Performance” *IEEE Trans on Industrial Electronics*, Vol. 56, No. 8, pp.2894-2903, Aug-2009.

[123] Jiang Zeng, Chang Yu, Qingru Qi, Zheng Yan, Yixin Ni, B.L. Zhang, Shousun Chen and Felix F. Wu “A novel hysteresis current control for active

power filter with constant frequency" *Electric Power Systems Research*, Vol.68, No.1, pp. 75-82, 2004

[124] Karuppanan P, Saswat Kumar Ram and Kamala Kanta Mahapatra "Three level hysteresis current controller based active power filter for harmonic compensation" *IEEE Emerging Trends in Electrical and Computer Technology (ICETECT),* pp.407-412, 2011

[125] P. Karuppanan and Kamala Kanta Mahapatra "Erratum to ''PI and fuzzy logic controllers for shunt active power filter—A report'' [ISA Transactions 51, 163–169]" *ISA Transactions*, Vol.51, No.5, pp.667-671, Sept-2012

[126] P. Rathika and Dr. D. Devaraj "Fuzzy Logic – Based Approach for Adaptive Hysteresis Band and Dc Voltage Control in Shunt Active Filter" *International Journal of Computer and Electrical Engineering*, Vol. 2, No. 3, pp.404-412, June-2010.

[127] Karuppanan P and Kamala Kanta Mahapatra "Adaptive-Fuzzy Controller Based Shunt Active Filter for Power Line Conditioners" *TELKOMNIKA Journal of Electrical Engineering*, Vol. 9, No.2, pp. 201-208, Aug-2011

[128] Gianluca Fabbri, Eleonora Nistico and Ezio Santini "Building Simulation Modeling Environments" *WSEAS Transactions on Circuits and Systems*, Vol.4, No.9, Sept-2005

[129] www.mathworks.com

[130] TMS320F/C24x DSP Controllers Reference Guide, *Texas Instruments*,1999

[131] Zeliang Shu, Yuhua Guo and Jisan Lian "Steady-State and Dynamic Study of Active Power Filter With Efficient FPGA-Based Control Algorithm" *IEEE Trans on Industrial Electronics*, Vol. 55, No. 4, pp.1527-1536, April-2008.

[132] J. Acosta, A. Gonzalez and Z.R.Martfnez "FPGA Based Control Scheme for Active Power Filter" *IEEE Conference*, 2006.

[133] Ning-Yi Dai, Man-Chung Wong, Fan Ng and Ying-Duo Han *"*A FPGA-Based Generalized Pulse Width Modulator for Three-Leg Center-Split and Four-Leg Voltage Source Inverters" *IEEE Trans on Power Electronics*, Vol. 23, No. 3, pp.1472-1484, May-2008.

[134] David M.E. Ingram and Simon D. Round "A Novel Digital Hysteresis Current Controller for an Active Power Filter" *IEEE Conference Proceedings on Power Electronics and Drive Systems*, 1997

[135] Stephen brown "FPGA Architectural Research: A Survey" *IEEE conderence on Design & Test of Computers, Winter* 1996.

[136] Eric Monmasson and Marcian N. Cirstea “FPGA Design Methodology for Industrial Control Systems-A Review” *IEEE Trans on Industrial Electronics*, Vol. 54, No. 4, pp.1824-1842, Aug-2007

[137] Mohamed-Wissem Naouar, Eric Monmasson, Ahmad Ammar Naassani, Ilhem Slama-Belkhodja, and Nicolas Patin “FPGA-Based Current Controllers for AC Machine Drives-A Review” *IEEE Trans on Industrial Electronics*, Vol. 54, No. 4, pp.1907-1925, Aug-2007

[138] Clive Max Maxfield “The Design Warrior’s Guide to FPGAs” *Newnes is an imprint of Elsevie,* 2004.

[139] Karuppanan P, Ayas Kanta Swain, Kamala Kanta Mahapatra “FPGA based Single-phase Cascaded Multilevel Voltage Source Inverter Fed ASD Applications” *Journal of Electrical Engineering*, Vol.11, No.3, pp.102-107, Oct-2011

[140] J.Bhasker “VHDL Primer” *Pearson Education*, 2000

[141] www.xilinx.com

[142] Spartan-3E Starter Kit Board User Guide, *Xilinx*, 2006

[143] System Generator for DSP Performing Hardware-in-the-Loop With the Spartan-3E Starter Kit, *Xilinx*, 2006

List of Publications

International journals

1. Karuppanan P and Kamala Kanta Mahapatra "PI and fuzzy logic controllers for shunt active power filter — A report" *ISA Transactions* Vo.51, No.1, pp.163–169, Jan-2012

2. Karuppanan P, Kamala Kanta Mahapatra, Jeraldine Viji and Bhuyan Kanhu Charan "Sinusoidal Extraction Control Strategy based Shunt Active Power Line Conditioners for Enhancing Power Quality" *Journal of Electrical and Electronics Engineering*, Vol.4, No.2, pp.83-88, Oct-2011.

3. Karuppanan P and Kamala Kanta Mahapatra "Adaptive-Fuzzy Controller Based Shunt Active Filter for Power Line Conditioners" *TELKOMNIKA Journal of Electrical Engineering*, Vol. 9, No.2, pp. 201-208, Aug-2011.

4. Karuppanan P and Kamala Kanta Mahapatra "PI with Fuzzy Logic Controller based Active Power Line Conditioners" *Asian Power Electronics Journal*, Vol.5, No.1, pp.13-18, Aug-2011.

5. Karuppanan P and Kamala Kanta Mahapatra "PLL Synchronization with PID Controller Based Shunt Active Power Line Conditioners" *International Journal of Computer and Electrical Engineering*, Vol.3, No.1, pp.42-47, Feb-2011.

6. PitchaiVijaya Karuppanan, Mahapatra Kamala Kanta "A Novel PLL with Fuzzy Logic Controller based Shunt Active Power Line Conditioners" *Journal of Electrical and Electronics Engineering*, Vol.3, No.2, pp. 153-158.Oct-2010.

7. Karuppanan P, Sushant Kumar Pattnaik and Kamala Kanta Mahapatra "Fuzzy Logic Controller based Active Power Line Conditioners for Compensating Reactive Power and Harmonics" *ICTACT-Journal on Soft Computing*,Vol.1, No.1 pp.49-53 July-2010.

8. Karuppanan P and Kamala Kanta Mahapatra "PI, PID and Fuzzy logic controller for Reactive Power and Harmonic Compensation" *International Journal of Recent Trends in Engineering***,** Vol. 3, No. 3, pp.88-92, May-2010

International conference

1. Karuppanan P, Kamala Kanta Mahapatra, Jeyaraman.K and Jeraldine Viji "Fryze Power Theory with Adaptive-HCC based Active Power Line Conditioners" *IEEE International Conference on Power and Energy Systems (ICPS)*,2011

2. Karuppanan P, Smrtuti Ranjan Prusty and Kamala Kanta Mahapatra "Adaptive-Hysteresis Current Controller based Active Power Filter for Power Quality Enhancement" *IET International Conference on Sustainable Energy and Intelligent System(SEISCON)* -2011

3. Karuppanan P and Kamala kanta Mahapatra "PLL with Fuzzy Logic Controller based Shunt Active Power Filter for Harmonic and Reactive power Compensation*"* IEEE *India International Conference on Power Electronics (IICPE)*- 2011

4. Karuppanan P and Kamala kanta Mahapatra "PLL with PI, PID and Fuzzy Logic Controllers based Shunt Active Power Line Conditioners" *IEEE* International Conference on Power Electronics, Drives and Energy Systems *(PEDES)* - 2010

5. Karuppanan P and Kamala Kanta Mahapatra "A Novel Control Strategy based Shunt APLC for Power Quality Improvements" *IEEE International Conference on Power, Control and Embedded Systems (ICPCES)* - 2010

6. Karuppanan P and Kamala Kanta Mahapatra "Shunt Active Power Line Conditioners for Compensating Harmonics and Reactive Power" *IEEE International Conference on Environment and Electrical Engineering (EEEIC)*- Poland, pp.273-276, 2010

National conference

1. Karuppanan P and Kamala Kanta Mahapatra "PID with PLL Synchronization Controlled Shunt APLC under Non-Sinusoidal and Unbalanced Conditions" *National Conference on Power Electronics (NPEC)*-2010

2. Karuppanan P and Kamala Kanta Mahapatra "A Control Strategy for Shunt Active Power Line Conditioners" *National Conference on Power Electronics (NPEC)*-2010

The following publications related to the topic, but are not included in the thesis

International journals

1. Karuppanan P and Kamala Kanta Mahapatra "PI, PID and Fuzzy Logic Controlled Cascaded Voltage Source Inverter based Active Filter for Power Line Conditioners" *WSEAS Transaction on Power Systems*, Vol.6, No.4, pp.100-109, Oct-2011

2. Karuppanan P, Ayas Kanta Swain, Kamala Kanta Mahapatra "FPGA based Single-phase Cascaded Multilevel Voltage Source Inverter Fed ASD Applications" *Journal of Electrical Engineering*, Vol.11, No.3, pp.102-107, Oct-2011.

3. Karuppanan P, Rajasekar S and Kamala Kanta Mahapatra "Cascaded Multilevel Voltage Source Inverter based active power filter for Harmonics and Reactive power compensation" *International Journal of Applied Engineering Research*, Vol. 1, No 4, pp.661-674, June-2011.

International conference

1. Karuppanan P, Rajesh Kumar Patjoshi, Kamalakanta Mahapatra and Ajay-D-Vimalraj 'Sinusoidal Extraction Controller based on Cascaded VSI for Active Power Filter' IEEE-**INDICON**-2011

2. Karuppanan P, Saswat Kumar Ram and Kamala Kanta Mahapatra "Three level hysteresis current controller based active power filter for harmonic compensation" *IEEE Emerging Trends in Electrical and Computer Technology (ICETECT),* pp.407-412, 2011

3. Karuppanan P and Kamala kanta Mahapatra "Cascaded Multilevel Inverter based Active Filter for Power Line Conditioners using Instantaneous Real-Power Theory" *IEEE* India International Conference on Power Electronics *(IICPE)*-2011

4. Karuppanan P and Kamala kanta Mahapatra "A Novel SRF Based Cascaded Multilevel Active Filter for Power Line Conditioners" *IEEE-INDICON* 2010

5. Karuppanan P, Rajasekar S and Kamala Kanta Mahapatra "Five-Level Cascaded Active Filter for Power Line Conditioners" *IEEE International Conference on Power, Control and Embedded Systems (ICPCES)* - 2010

6. Karuppanan P and Kamala Kanta Mahapatra "FPGA based Cascaded Multilevel Pulse Width Modulation for Single Phase Inverter" *IEEE International Conference on Environment and Electrical Engineering (EEEIC)*-Poland, pp.273-276, 2010

National conference

1. Karuppanan P, Kamala kanta Mahapatra, Kanhu Charan Bhuyan and Rajesh Kumar Patjoshi "Cascaded Voltage Source Inverter based Active Power Line Conditioners" *National Systems Conference (NSC)* 2011

APPENDIX-A

System parameters

The performance of the shunt active power line conditioner system is evaluated through MATLAB / SIMULINK environment using Simpower tools. For simulation, the system parameter values used are given in Table A.1, which is considered for three-phase active power line conditioner system.

Table A.1 System parameters (For Matlab/Simulink Simulation)

Parameters	Values
Supply voltage/frequency	415 V / 50 Hz
Smoothing inductor (R_s , L_S)	1 Ω, 0.1 mH
Diode / Thyristor- rectifier Load resistor (R_L), Load inductor (L_L)	6-diode / Thyristor 50 Ω, 40 mH
Interface Inductor (R_c , L_c)	1 mH, 1 Ω
DC-side capacitance (C_{dc})	2200 μF
Reference voltage ($V_{dc, ref}$)	500 V
Voltage source inverter	6-IGBTs/diodes

For Hardware implementation, Modified-SRF with direct PWM-SVM and indirect PWM-adaptive-fuzzy-HCC technique is adopted. The modified-SRF control method is used for reference current extraction from the distorted load current. The direct SVM technique and indirect adaptive-fuzzy-HCC is applied to generate the required switching pulses to drive the PWM-inverter. The entire control algorithm is validated through MATLAB program and coded in assembly language for digital hardware implementation. For simulation and hardware implementation, the system parameter

values used are given in Table A.2, which is considered for three-phase active power line conditioner system.

Table A.2 List of parameters used in simulation and experimentation

Parameters	Simulated Values	Experimental Values
Supply voltage/frequency	360 V / 50 Hz	360 V / 50 Hz
Thyristor- rectifier Load Resistor (R_L) and Inductor (L_L)	-- 50 Ω and 20 mH	SKKT57B16E device 10 Ω
Interface inductor (R_c, L_c)	1 Ω and 1.8 mH	1.8 mH
Dc-link capacitance (C_{dc})	2200 μF	2200 μF
Reference voltage ($V_{dc, ref}$)	750 V	750 V
Voltage source inverter	--	FF200R12KE3 IGBT module, M57962AL for Gate driver circuit, Amplifier circuit, Power supply for DSP processor and driver circuit.
Sensors	--	LEM make LV20P for phase voltage, LA100P for current transducer and LV100 for dc-link voltage sensor
Processor	--	Texas TMS320F240
CCS for PC interface	--	XDS510PP JTAG Emulator

APPENDIX-B

TMS320F240 Controller

TMS320F240 device is DSP controller based on the TMS320C2xx generation of 16-bit fixed-point digital signal processors. It combines the features of TMS320 architectural design of the C2xLP core for low-cost, high performance capabilities and advanced peripherals, which are optimized for power electronic applications. Fig.B.1 shows the Pin Configuration and schematic diagram of the TMS320F240 devices. The main features of the TMS320F240 DSP controller as follows

- Memory
  - 16k words of on chip Flash EEPROM
  - 544 words of ON-Chip Data/Program DRAM
  - 32k words of external RAM of speed 10 ns for debugging and development
- Analog interface
  - 12-channel of 12-bit, simultaneous sampling bipolar external ADC with maximum conversion time of 6.6 μs (AD7864)
  - Two numbers of dual channel 8-bit DACs for software debugging (AD7628)
- PWM outputs
  - 6-PWM ports with programmable deadband
  - Fiber optic transmitters for fiber optic link based PWM pulse transmission
- I/O ports
  - Three-electrically isolated and four non-isolated input ports
  - Seven buffered output ports
  - LEDs for status indications (8 Nos)
- Communication interface
  - RS232 interface for serial data communication

PC Interface Card

XDS510PP PLUS parallel port JTAG emulator is designed to use with digital signal processors (DSPs), which is designed by Texas Instruments. The XDS510PP PLUS

parallel port JTAG emulator is table top module connected with personal computer or laptop to allow hardware engineers and software programmers to develop applications with DSPs and microcontrollers.

Key Features:

- Supports Texas Instrument's Digital Signal Processors with JTAG interface (IEEE 1149.1)
- Advanced emulation controller provides high performance.
- Supports standard parallel communication interface with host PC. No adapter required.
- Supports JTAG interfaces from +3.3 V to 5 volts.
- One status LED for operational status.
- Compatible with Texas Instruments Code Composer Studio

The XDS510PP JTAG Emulator with Code Composer Studio (CCS) is used to implement the control algorithm in real-time target processor (TMS320F240) on the host computer.

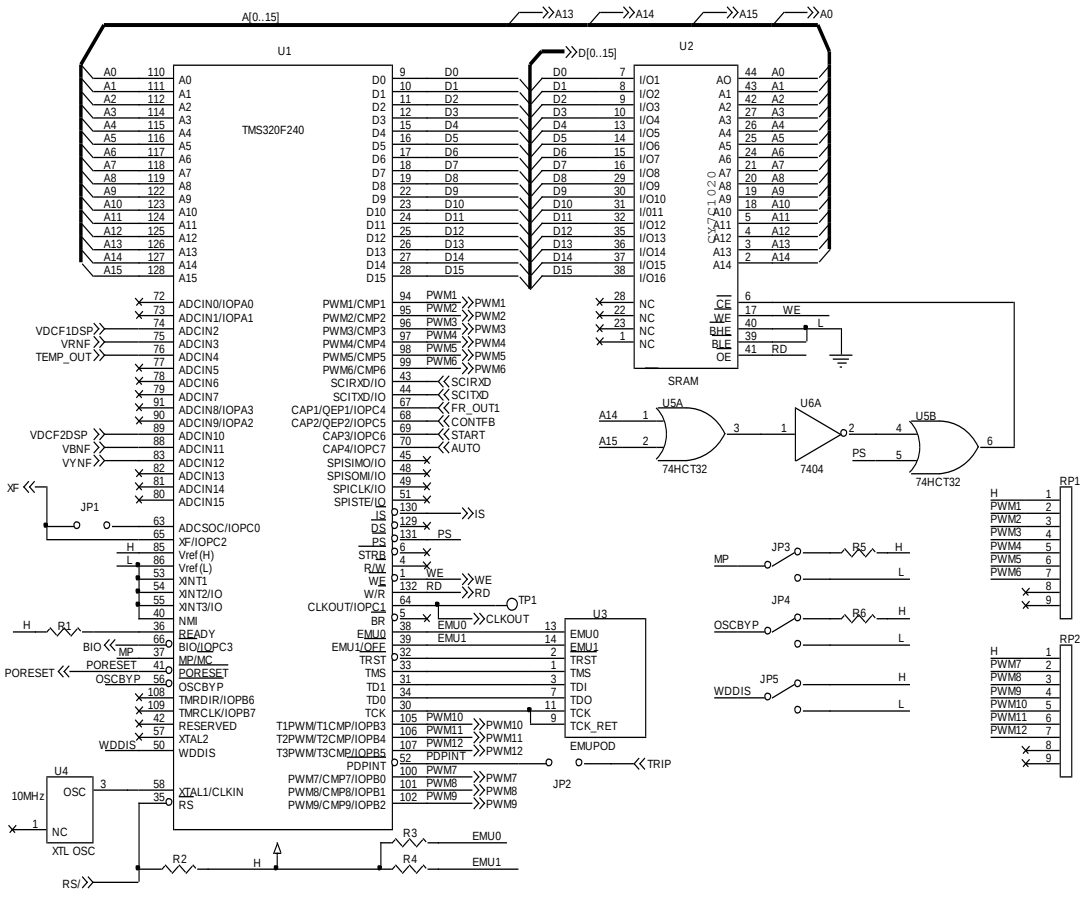


Fig. B.1 Pin configuration of the TMS320F240 devices