ATLAS simulation based characterization of Recessed-S/D FD SOI MOSFETs with non-uniform lateral doping

A THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE

REQUIREMENTS FOR THE DEGREE OF

Master of Technology
In
VLSI Design and Embedded Systems

By:
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Roll No. 212EC2176

Department of Electronics and Communication Engineering
National Institute of Technology
Rourkela, Orissa, India
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Under the guidance of
Prof. P.K. TIWARI

Department of Electronics and Communication Engineering

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2014

DEPARTMENT OF ELECTRONICS AND
COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY, ROURKELA
ORISSA, INDIA-769008

CERTIFICATE

This is to certify that the Thesis Report entitled "**ATLAS simulation based characterization of Recessed-S/D FD SOI MOSFETs with non-uniform lateral doping**", submitted by **Mr. Gorla Raju bearing Roll no. 212EC2176** in partial fulfilment of the requirements for the award of **Master of Technology in Electronics and Communication Engineering** with specialization in "**VLSI Design and Embedded Systems**" during session 2012-2014 at National Institute of Technology, Rourkela is an authentic work carried out by him under my supervision and guidance.

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other university/institute for the award of any Degree or Diploma.

Place: Rourkela

Date: - May, 2014

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ABSTRACT

As scaling down the technology into nanometer regime, short channel effects (SCE) and manufacturing limits will increase, which alters the performance of devices. Silicon-on-insulator (SOI) has got reputation that is a promising technology in the last decade offering more CMOS devices with higher density, higher speed, and reduced second order effects for submicron VLSI applications. Recent investigations have been reported fully depleted (FD) SOI devices are the best solutions because of their suitability to shrinking methods comparative to bulk silicon CMOS devices. Further, implicit the extra advantages, like sub threshold current reduction and improvement in Analog/RF performance; channel engineering and source/drain engineering techniques are implemented in FD SOI MOSFET. Recessed FD SOI MOSFET with non-uniform lateral doping structure gives some solutions to SCEs and better device performance by changing doping levels in different length ratios of channel region in lateral direction

In this project work, a comprehensive performance study of source/drain (S/D) engineered SOI MOSFET with non-uniform doping in Channel region is presented. To analyse the characterisation of proposed structure, all the characteristics parameters extracted by using simulation tool. Those characteristics parameters are Surface potential, Threshold voltage, Sub-threshold current, Device capacitances, Drain current, Transconductance, Output conductance, Transconductance generation efficiency, Cut-off frequency and Maximum frequency of oscillation have been carried out and compared with its SOI MOSFETs and non-S/D engineered ones. To extract the characteristics parameters of Device H and Y-parameters are used. All these numerical simulation results are performed using ATLAS^{TM}, a 2-D numerical device simulator from SILVACO Inc.

ACKNOWLEDGEMENTS

First of all, I would like to express my deep sense of respect and gratitude towards my advisor and guide **Dr. P. K. Tiwari**, for his visionary guidance, insightful counsel, and constant encouragement throughout my M. Tech project work. I am greatly indebted to him for his unconditional help, invaluable advice and for propelling me further in every aspect of my academic life. His presence and optimism have provided an invaluable influence on my career and outlook for the future. I consider it my good fortune to have got an opportunity to work with such a wonderful person.

I am truly thankful to **Prof. K. K. Mahapatra, Dr. D. P. Acharya, Dr. N. M. Islam, Dr. Poonam Singh** and **Dr. Ayaskant Swain** for their ubiquitous assistance and tireless care throughout the M. Tech program. I am grateful to all other faculty members and staff of the Department of Electronics and Communication Engineering, N.I.T. Rourkela for their generous help in various ways for the completion of this Project Work.

I am really thankful to Gopi Krishna, Anand Mukhopadhyay, Ajit Kumar, Shara Mathew, and Shilpeeka Medhi, and all my friends especially my classmates for their help, stimulating discussions, and sharing with me their expertise in various areas.

Finally, I extend my gratefulness to all those who are directly or indirectly involved in this project work. Last but not the least; I am thankful to the Almighty who gave me the strength and patience for completing the work.

GORLA RAJU

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Chapter 1

INTRODUCTION

1.1 Importance of Scaling:

To increase the density of transistors on Integrated Circuit scaling is the main prospect. In the starting of twentieth century scaling came into existence in industrial electronics, information sharing, automation and technology. Communication technology also so much interlinked with the IC technology. In no time the human race is ever has been connected as it is today. Shrinking of computer and portable gadgets with each possible applications; be it video, high speed communication audio,; revolutionized the whole world of entertainment and interconnectivity. Through VLSI design everything is implemented like ultra-thin high speed sized, sensors, all new materials, low power semiconductor devices, and their applicable.

Before 1925 there was a technology that vacuum tube with small size transistor, in a scientist Lilienfeld 1925 begins with the perception of Insulated Gate Field Effect Transistor (IGFET) which has belter potential to replace the vacuum tube in Electronic industry[1]. Actually demonstration of Field Effect Transistor practical implemented in 1960 by two scientists Kahng and Atilla [2] in the form of the Silicon-based Metal Oxide Semiconductor (MOSFET). In 1958, at Texas Instruments Jack Kilby given the idea of the Integrated Circuits (IC) and for the first time fabricated first IC (a S-R flip flop) by Robert Noyce from the Fairchild Corp shown in Fig. 1 [3]. Afterwards in 1959 Richard Feynman stated some words regarding

scaling on his notable speech, “There is plenty of room at the bottom”, reduction of dimensions of any material should allow conceding the same or better performance when comparing with the material with higher dimensions [4]. Another visionary prophecy from Gordon Moore, co-founder of Intel then with Fairchild Corp. and, states that, “The number of transistors on integrated circuits doubles approximately every two years”. This prediction has been accurate for more than three decades as shown in Fig. 2. In 1962 we can observe the first logic family growth, the TTL [3]. The first microprocessor was introduced in 1972 by Intel where more than 2000 PMOS transistors are integrated onto a single chip. Following the Moore’s law the transistor count increased exponentially [5]. Then in following next some microprocessors are fabricated with the NMOS technology. This NMOS was rapidly channelled out soon because of its heavy consumption of dynamic power when increasing number of transistors per chip. Later a new technology was introduced by combining the NMOS and PMOS technologies, which is named as complementary metal oxide semiconductor (CMOS). Advantages of the CMOS technology are more reliable compare to previous technologies, consumed the least power, scaling technology is very simple with better performance from the small scale integration (SSI) to Very Large Scale Integration (VLSI) and now spearheading towards the nanotechnology.

CMOS technology is a promising technology to provide so many advantages in device scaling down to nanometre with the definite scaling. The International Technology Roadmap for Semiconductor (ITRS) has set procedure to scaling of device in all dimensions and also this technology gives low power consumption and cost per unit will be reduces. The major advantages of CMOS are high noise immunity and low static power consumption.

In the CMOS, one of the transistor is always off so that the power consumption in

changing of state from on state to off there won't be occurs. The series grouping draws significant power only fleetingly during converting between on and off positions. Consequently, CMOS devices dent release any waste heat as different forms of logic, for example NMOS logic or transistor–transistor logic (TTL), normally it has some standard current when the state changing from one o another state. CMOS permits high packing density of logic functions on a chip. The main reason that CMOS technology is implemented in VLSI chips because of its high packing density

As evident from the ITRS 2010 in Fig. 3, the year 2013 with technology node 22nm is project to have physical channel length of 10nm and less. 800 billion transistors are packed in The Intel 32 nm SRAM wafer (1 Tb) and modern I-7 quad core GPU processor has more 1.1 billion transistors in a chip area 160 mm^2 [6]. This kind of packing happening in Devices by engineers throughout the world for the reason that of "Scaling" came into picture in late nineties. Scaling is defined as controlled modification of the device dimensions such that it acquires lesser chip area while maintaining the long channel characteristic and performance.

Proposed the scaling approach in 1972 [7]. Scaling not simply decreases the device measurements' interpreting to a higher packing density nevertheless it also leads to saving significantly dynamic power by providing low voltages. The scaling of a device should be done in both vertical and horizontal direction then only it works as like as long channel characteristic and performance. There should be same scaling factor while scaling then only we can reduce the short channel effects in nanoscale devices and ensure good electrostatic control when fabricating the smaller devices, and by the same scaling factor, we should be increased doping of substrate concentration and reduced the supply voltage.

Static dissipation

Sub threshold conduction when the transistors are off.

- Tunnelling current through gate oxide.
- Leakage current through reverse biased diodes.
- Contention current in rationed circuit

Dynamic Dissipation

- Charging and discharging of load capacitances.
- Short circuit power dissipation

Limits of Scaling Planar, Bulk MOSFETs Limits MOSFETs 65 nm tech. generation (2007, resistance (Resists/d)–Others Alternative device structures (non-classical CMOS) could also be used –Ultra skinny plate like, Bulk MOSFETs[10] Limits MOSFETs65 nm school. of series generation (2007, Lg= 25nm needs with of SCE exaggerate–effects and applied math variation–Impact of high Limits substrate of in problem single depleted: body, absolutely Scaling meeting all device D doping Impact of quantum –Control classical plate like, bulk CMOS (even with and multiple-gate transistors material and method solutions: high K, metal electrodes, Control S/D and beyond: end -gate SOI

Optical lithography in silicon Therefore wavelength technology provides combining of billions of transistors on a chip is possible silicon through. As interference from patterning without sub the techniques. Sub-wavelength regime, light diffraction and adopting resolution comes difficult pattern enhancement optical lithography enters feature causes image disorder. be, The ITRS's projection trend versus power requirements Fig. 4 illustrates that the power consumption

The power consumption is approximated by [8]

$$P_{diss} = P_D + P_S = \alpha f C_L V_{DD}^2 + V_{DD}\left(I_{leakage} + I_{th} 10^{-\frac{V_{th}}{s}} \right) \quad (1)$$

where P_S and P_D represent the static power dissipation and the dynamic power dissipation respectively, ,

, I_{th} is the threshold current $I_{leakage}$ is the total leakage, C_L is the load capacitance V_{DD} is the supply voltage,□□ is the activity factor

current, s is the subthreshold swing., V_{th} is the threshold voltage and

from the above equation we can observe that power consumption decreases as lowering , $I_{leakage}$ V_{DD} and s; and increasing the V_{th} .

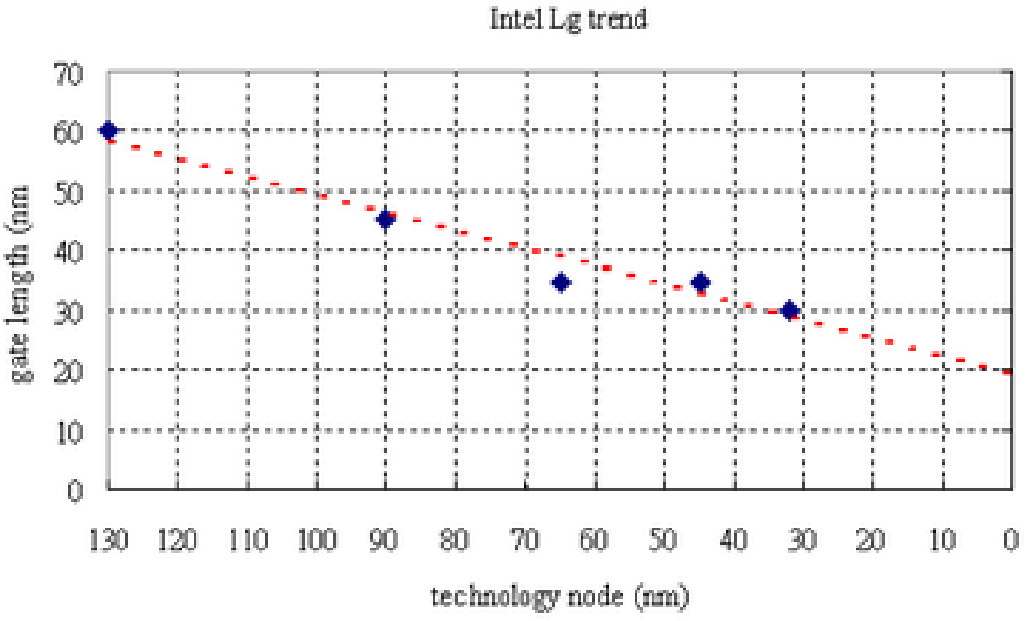

Fig 1 shows gate length versus technology node

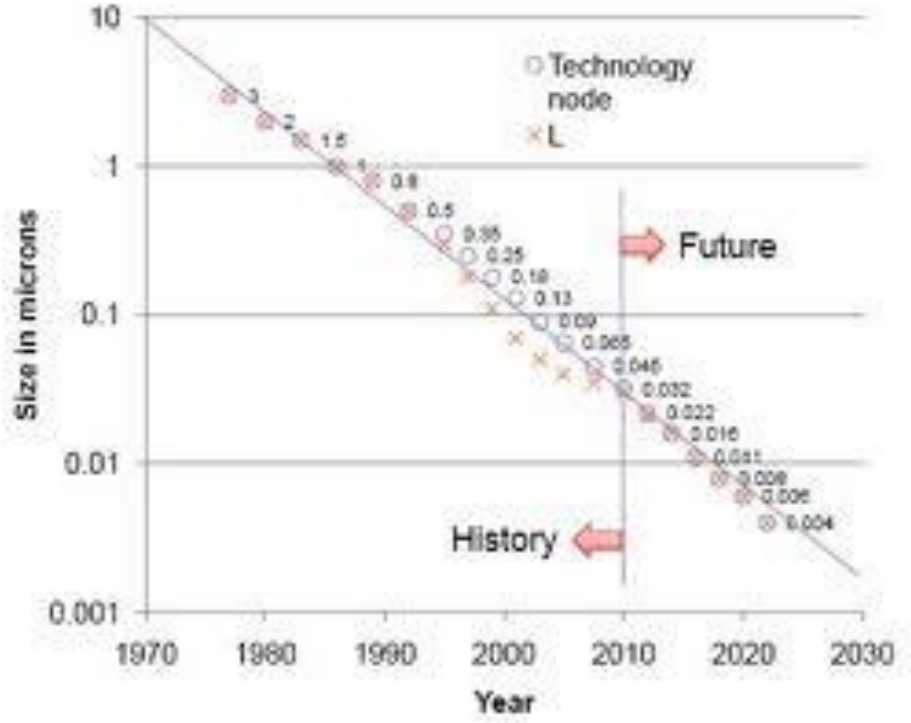

Fig. 2 shrinking technology size with of scaling years

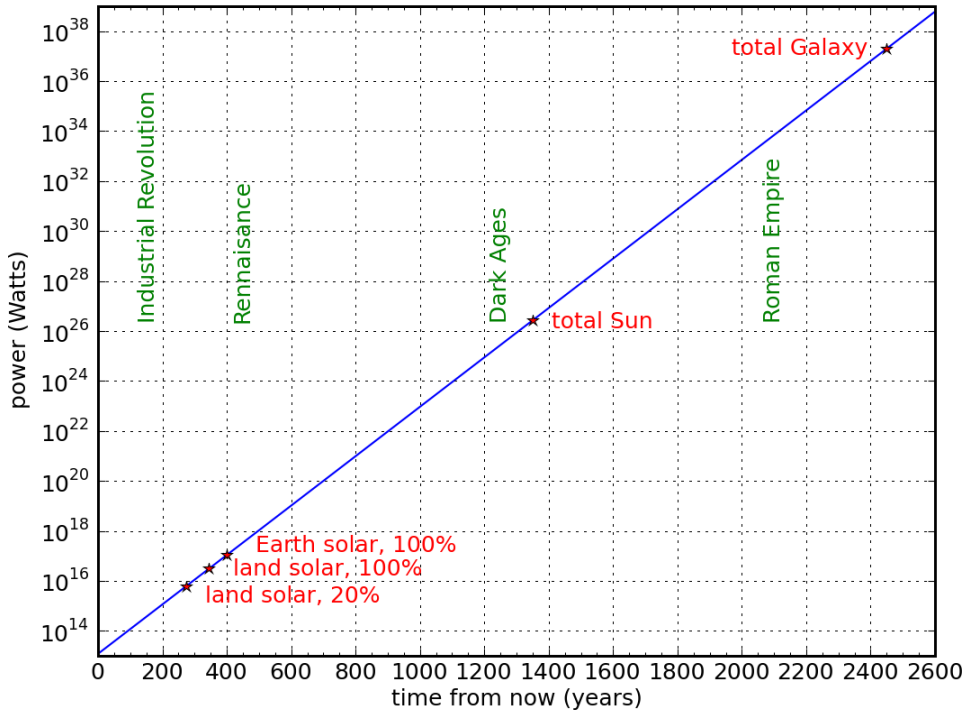

Fig.3 Power Consumption versus years of time from now onwards.

Thus V_{DD} and Vth are in oxide needs to be scaled which in turn leakages. Also, higher tremendously increases gate conflict for which the gate tunnelling substrate doping is must to check the) is the need of the hour but structures and architectures to continue further CMOS scaling. Again this diminishes the scattering. To trade-off current drive due to increased, SCE and the lower current, which the conventional short channels effects (SCEs MOSFETs fails to achieve. This gives way to creation of between the power consumption alternative devices

Let's have a. MOSFET scaling alters both lateral dimensions physical insight and vertical device due to scaling into the problems.

1.2 Types of scaling and their challenging issues:

1.2.1 Lateral Scaling

1.2.1.1 Mobility Degradation

Following the rules of but a serious effect continuous increase source and drain depletion; continuous threshold voltage variations take place. Higher doping scaling requires desired in play to have a lower due to the dopant fluctuations the channel impurity of mobility in the channel in the channel doping (due to random region. Also scaling, for a planar bulk MOSFET junction electric field in scattering comes with higher amount of channel doping. Also the ensures non-overlap of the (N_a). This is because it is degradation inside the channel.

1.2.1. 2 DIBL and Threshold voltage roll-off

As the lateral dimensions scaled are which is to manifested as of the threshold the channel length leading to loss of gate control reduces tremendously with increasing channel junction threshold over the channel ns the S/D off or a sharp fall

DIBL can be depletion charge controlled by the gate which by the source and drain reducing This introduces a correction determines the lateral potential barrier that is the gate. into two parts expected explain–termed empirical ‘charge sharing’ model which considers the This effect is -induced field into the, since an maximum index by increase in drain voltage leads of the drain one controlled qualitatively channel drain dramatic depletion charge under the gate splitting of. The threshold when the drain bias is high. This is to further penetration by the gate; the other controlled a semi- of the transistor, the voltage.

$$V_{th} = V_{FB} + 2\phi_f - \frac{Q'_d}{C_{ox}} \quad (2)$$

$$\text{where, } Q'_d = Q_d - \Delta Q \quad (3)$$

represents the depletion charge under drain control depletion charge under gate control, and the total depletion charge respectively

1.2.1.3 Energised electron Effect

Hot-carrier (HC) degradation enough near the drain creates hot that injected into only hot electrons larger than the Si-SiO2 conduction band carriers which are the increases SCE and causes long-term instability, (traps) in the oxide near the. It is found energy to create defect states affects reliability degradation in n-channel MOSFETs. The, at the interface having energy of 0.6eV field discontinuity bond oxide with can cause SiO_2

1.2.2 Vertical Scaling

1.2.2.1 Depletion Effect in Poly silicon

This for responsible The effect also leads increases, whereas degradation of this is region the effective scaling of the solid densities. Thus, the technology polysilicon gates. silicon (~10^{19}-10^{20} cm^{-3}) use of to a threshold oxide the other solubility of gate doping resulting in the thickness voltage metal depletion to transconductance gate capacitance and shift, which gets more pronounced.

1.2.2.2 Presence of Quantum effects

Scaling direction leading to perpendicular strong surface electric field near a oxide to and shifting the peak of the inversion the inversion charge discrete sub the inversion, the peak of the inversion of the inversion carriers, giving rise tiny at effective oxide thickness and the interface the threshold given bias, -bands. Concentration peak is located around quantum confinement the voltage leads dens centroid away from the silicon/oxide interface carrier for motion in increases the increases creating a potential well and interface charge.

1.2.2.3 Gate Tunnelling

With the tunnelling may static power dissipation take (Si_3N_4) are employed to diminishing thickness the major high-k, increases gate oxide and dielectric materials contributor

is the Gate Tunnelling check gate tunnelling.

1.3 Innovations in MOS Technology:

1.3.1 Gate Engineering Techniques

1.3.1.2 Metal Gate

MOSFET with Metal gate decrease the short channel effects and improve the device performance. By varying the metal gate work function we can improve the MOSFETs performance

1.3.1.2 Multi-Material Gate

Moderately two or is (DMG) Material more level work capacity. As a consequence of this, the electron speed and the horizontal electric utilizing fell channel proposed by Razavi et al[11]. The metal door M1 is subsequently legitimately known as the -Gate more metals field the entryway close to the source is an expansions of diverse work capacities of the two door material which further brings about the expanded door transport effectiveness. door to screen proportion in a DMG strained-Si on cover MOSFET [11]. Further, the structure makes the Screen Gate

1.3.1.2 Multiple Gates

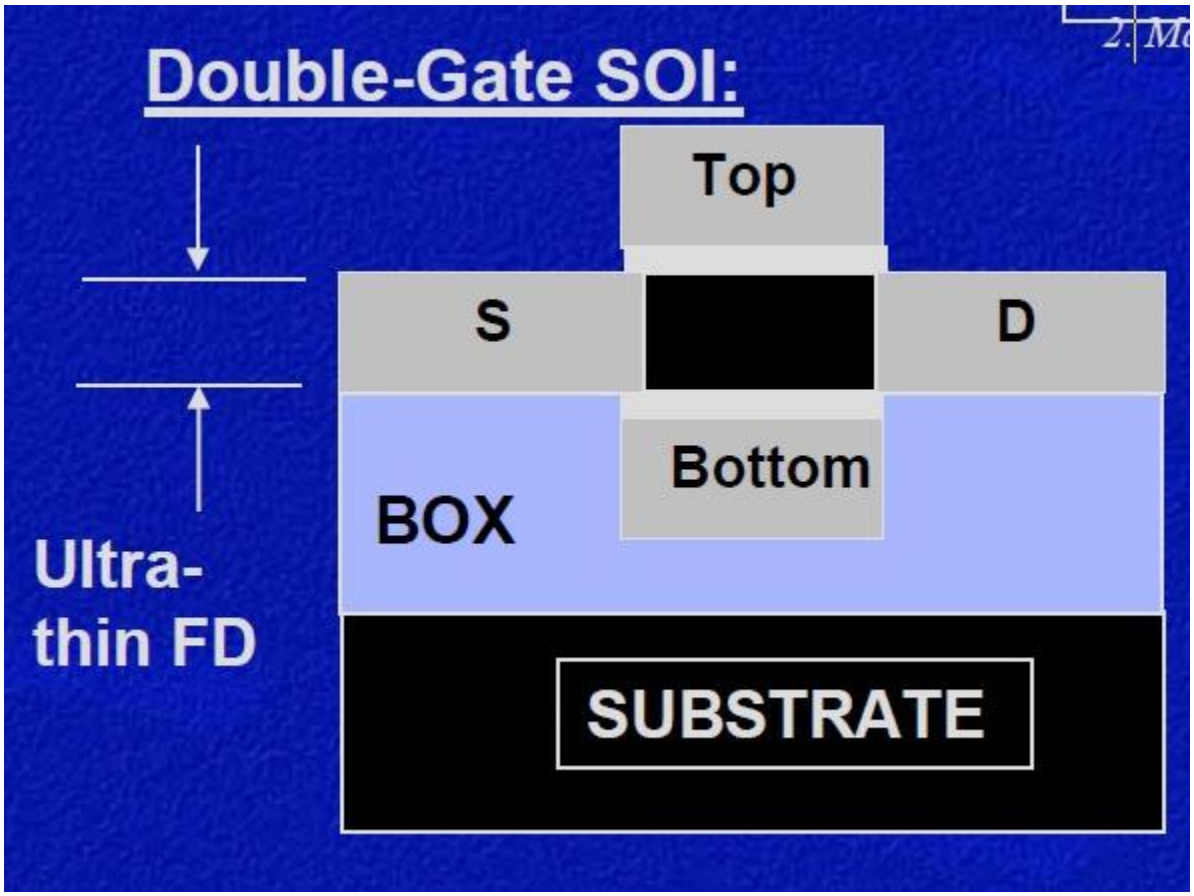

Fig 4 shows the multiple gates used in SOI MOSFET

A potential candidate, lower threshold the channel to oxide (BOX) higher transistor possesses slope transconductance FDSOI -on-insulator threshold the buried Rigorous research of the FD SOI MOSFETs revels that this and body effect. However, capability and ground FD SOI junction poor current regions, despite having he ultra- to and an underlying capacitance thin drive device drain MOSFETs possess large series resistance which buried oxide leads to the of

the source and body effect.

1.3.2 Channel Engineering Techniques

1.3.2.1 Shallow S/D Junction

However, as the source get shallow, their ~10^{20} /drain in the band-to-band tunnelling the channel. Also, from a technological point of doping must the annealing steps needed to activate the are ones' constant. Solid solubility factors degrade the the source barrier. 'Junction depths of dopants puts an upper limit reduces the drain coupling to after sheet resistance leakage component. All these 13 junction depth causes an be increased

1.3.2.2 Halo Doping

To overcome the proposed in halo–off found, various chop improve the device doped region. Current engineering performance higher than the uniformly devices) in the saturation region. The halo device pinch halo applications output tears for analog general, or, the SCEs have the ge region, although like double- LAC subthreshold doping is, sin lateral asymmetric channel (resistance the LAC devices. Halo doping led to a higher drive (DH) and stance and intrinsic gain (such as gm/Id region occurs in the halo implant regional-halo (SH) been the improvement is significant parameters.

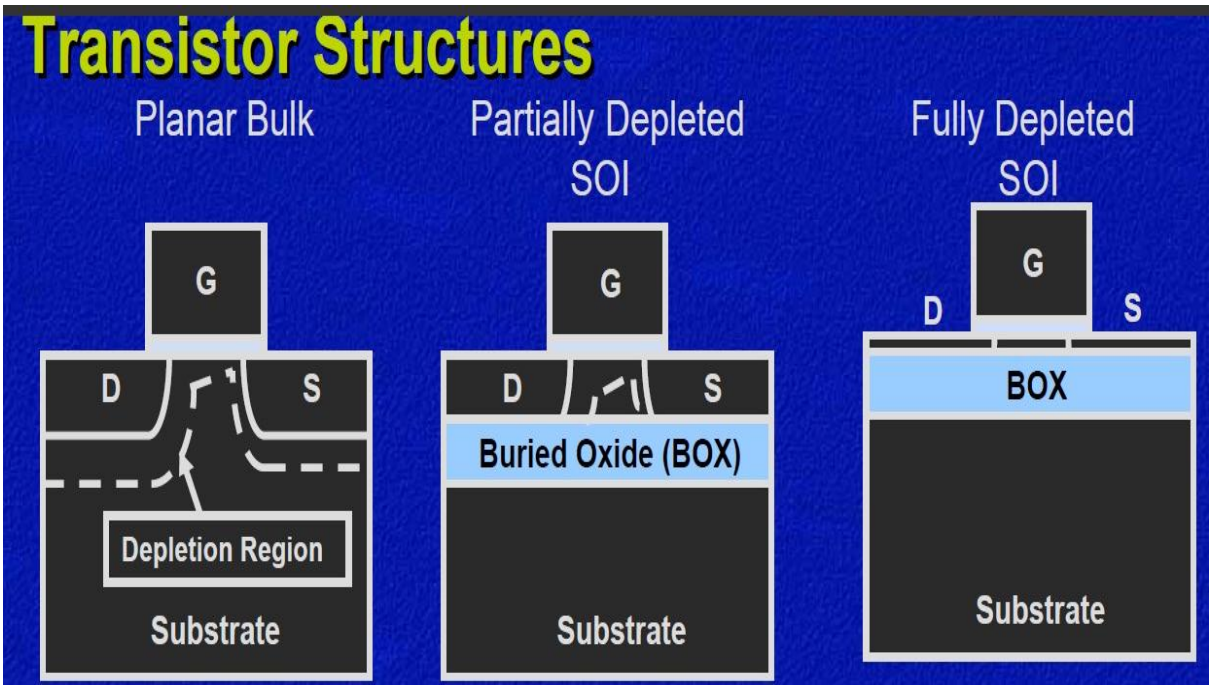

Fig. 5 different types of SOI MOSFET structures

1.3.2.3 Strain

Short channel effects (SCEs) and hot carrier effects (HCEs) come into picture when the gate length of conventional Complementary Metal Oxide Semiconductor (CMOS) is scaled down. These effects are undesirable and hampers in the normal functioning of the device. To overcome the effects several modifications are done to the device [1,2] which helps in diminishing the SCEs in devices with shorter channel lengths in the sub-100nm range. Hot carrier effect contributes to the short channel effects (SCEs) in the device thereby causing instability and increase in the subthreshold current. Scaling of the device requires scaling of all the scalable parameters in the horizontal and vertical directions like the gate length, gate oxide thickness and channel thickness. When the gate oxide thickness is reduced

correspondingly there is an increase in the electric field across the oxide which in turn results in tunnelling current which increases the static power dissipation of the device. The mobility of charge carriers is enhanced using the concept of strain technology [5]. Introducing strain to the device helps in getting better performance like having high current drive without the need for further scaling of the scalable device parameters such as gate length, gate oxide thickness and S/D junction depth. The two known methods to introduce strain in the device are uniaxial (local method) and biaxial (global).In this structure tensile biaxial strain is chosen because of its higher electron mobility enhancement as compared to uniaxial strain [18]. It is created by growing Si epitaxial layer over a thin pseudomrphiclayer of Si1-xGexlayer(<500nm) in which X is the Ge mole fraction content. Tensile biaxial strain is created due to the mismatch in lattice constant if Si and Ge in which Ge has a slightly greater lattice constant as compared to Si. When thin Si layer is deposited over the SiGe substrate a tensile force is created in the thin Si layer thereby increasing its lattice constant and hence creating strain in the layer. From [6] it is known that mobility can be enhanced due to strain by increasing the Ge mole fraction content in bulk SiGe substrate as the lattice constant of SiGe increases with increasing concentration of Germanium which facilitates in the increase of strain. A mobility enhancement factor upto2.3 can be achieved for 30% Ge concentration [7]. The enhancement of strain can be said to be reflected from the sub band structure of the device [].Another method to get rid of hot carrier effects (HCEs) is to use multi material gate. As proposed by long etal. [8] we are using double material gate. The metal gates are cascaded in such a manner that the gate near source (M1) is of higher work function relative to the gate near drain side (M2).This results in sharp increase in electron velocity and lateral electric field at the interface of the two gate materials henceforth increasing the gate transport efficiency[9] A higher value of metal work function in control gate would result in smaller value of minimum surface potential in the channel which in turn will reduce the leakage current in the subthreshold region of operation.

Earlier, surface potential and threshold voltage modelling and simulations have been done by current and subthreshold slope of Double-Material-Gate (DMG) MOSFET with strained Si channel on $Si_{1-x}Ge_x$ substrate has been shown. The model is also verified using ATLAS™, a 2D device simulator by SILVACO Inc**.**

Short channel effects(SCEs) and hot carrier effects(HCEs) come into image once the gate length of standard Complementary Metal chemical compound Semiconductor (CMOS) is scaled down. These effects are undesirable and hampers within the traditional functioning of the device. to beat the results many modifications are done to the device[1,2] that helps in decreasing the SCEs in devices with shorter channel lengths within the sub-100nm vary. Hot carrier impact contributes to the short channel effects (SCEs) within the device thereby inflicting instability and increase within the sub threshold current. Scaling of the device needs scaling of all the ascendable parameters within the horizontal and vertical directions just like the gate length, gate chemical compound thickness and channel thickness. once the gate chemical compound thickness is reduced correspondingly there's a rise within the field across the chemical compound that successively leads to tunneling current that will increase the static power dissipation of the device. For a flat bulk MOSFET, continuous scaling needs continuous increase in channel doping (Na) to possess lower junction field within the channel region and conjointly making certain non-overlap of supply and drain depletion within the channel[3].But a significant impact of quality degradation as a result of the impurity scattering is seen with higher quantity of channel doping[4]. The quality of charge carriers is increased victimisation the idea of strain technology[5]. Introducing strain to the device helps in convalescing performance like having high current drive while not the requirement for additional scaling of the ascendable device parameters likes gate length, gate chemical compound thickness and S/D junction depth.

The two renowned strategies to introduce strain within the device square measure uniaxial(local method) and biaxial(global).In this structure tensile biaxate strain is chosen as a result

of its higher lepton quality sweetening as compared to uniaxial strain[18]. It's created by growing Si epitaxial layer over a skinny pseudomrphiclayer of Si1-XGeXlayer (500nm) during which X is that the Ge mole fraction content. Tensile biaxate strain is made as a result of the match in lattice constant if Si and Ge during which Ge encompasses a slightly bigger lattice constant as compared to once skinny Si layer is deposited over the SiGe substrate a tensile force is made within the skinny Si layer thereby increasing its lattice constant and thence making strain within the layer. The sweetening of strain may be aforementioned to be mirrored from the subband structure of the device [7].Another technique to induce obviate hot carrier effects (HCEs) is to use multi material gate. As projected by Long etal. [8] we tend to square measure victimization double material gate. The metal gates square measure cascaded in such a fashion that the gate close to source(M1) is of upper work operate relative to the gate close to drain side(M2).This leads to sharp increase in lepton rate and lateral field at the interface of the 2 gate materials henceforward increasing the gate transport efficiency[9]. A step like potential profile is made within the channel that ensures screening of minimum potential purpose from drain voltage variations. the next worth of metal work operate up to the mark gate would lead to smaller worth of minimum surface potential within the channel that successively can scale back the outflow current within the subthreshold region of operation.

Earlier, surface potential and threshold voltage modeling and simulations are done by [10, 11] on Double-Material-Gate (DMG) MOSFET with strained Si channel on Si1-XGeX substrate. this work may be thought of as associate extention of the previous add that the analytical model for subthreshold current and subthreshold slope of Double-Material-Gate (DMG) MOSFET with strained Si channel on Si1-XGeX substrate has been shown. The model is additionally verified victimisation ATLASTM, a 2nd device machine by SILVACO.

Chapter2

LITERATURE SYRVEY

1.1 Previous research related to proposed work:

1. In 1996, D. FLANDRE et .al "Fully-Depleted SOI CMOS Technology for Low-Voltage Low-Power Mixed Digital/Analog/Microwave Circuits"

In this work explains about the thin film silicon-on-insulator (SOI) technology which named it as fully depleted SOI MOSFETS. This technology offers variant features over bulk SOI MOSFETs such as low-voltage, low-power, and the low value of the body-effect coefficient nearly equals to unity. In addition those advantages of fully-depleted SOI technology demonstrated both theoretically and experimentally for the realization of low-voltage low-power circuit. This technology provides the low value of threshold voltages around 0.33V which allows the low power operation with supply voltage of 1.2 V. some other advantages

- gain improves for microwave components and good frequency response over bulk counterparts
- digital components with enhanced speed and static and dynamic power performance;
- analog components with improved precision, speed, power, swing and noise performance;

2. In 2009 Hossein Elahipanah_ and Ali A. Orouji "A Novel Step-Doping Fully-Depleted Silicon-on-Insulator Metal–Oxide–Semiconductor Field-Effect Transistor for Reliable Deep Sub-micron Devices"

In this they have included the channel engineering to fully-depleted silicon-on-insulator metal–oxide–semiconductor field-effect-transistor (FD SOI MOSFET), in that channel region consists of two different doping levels which named as step doping (SD) region in order to increase performance and reliability of the device. Major advantages of this particular structure are adjusting the threshold voltage levels by altering the doping ranges in two different sections and reliability improvement. The structure presents enormous improvement in performance zones such as current drive capability, threshold voltage roll-off, output resistance, and hot-

carrier reliability. It was found that the performance device is greatly reliant on the SD region parameters.

Results shows the following features of structure

- Improvement in on/off current ratio,
- Output characteristics saturated when compared with conventional SOI structure.
- substrate current reduced which results in lower hot-carrier degradation
- So many earlier problems solved like short-channel effects in VLSI and the proposed SDFD-SOI MOSFETs can work very well in deep sub-micron and nanoscale regime.

Observations:

- In high power and voltage circuits, then large length and low doping density for the SD region need to be used.
- For low power and voltage circuits in devises one needs to use the SD region with high doping density and small length
- SD region can modify the electric field is modified by changing the source/drain engineering in the channel and
- Near the source junction common peak have been reduced.

3. In 2004, Abhinav Kranti Laterally asymmetric channel engineering in fully Depleted double gate SOI MOSFETs for high Performance analog applications

In this work analog with of GC can be used to innovative analog applications ammeters. Tayloring the: The applications DG devices at lower gate overdrive and higher drain bias allows for the simulated GC design and structures. The work proposes and effective and MEMS. The model use of GC performance effective channel length. GC DG devices with high in the form basic well useful analog for experimental gain design realization useful for precision channel compared to UD devices data and improve the of very high on the behavior of key that channel length (device G) and significantly with extremely analog easily integral

key analog design shall be engineering of of DG values of intrinsic DC gain would be Results show voltage as optimization compares for the same based devices due to the extremely high Early DG devices. Guidelines for the overall optimum performance of GC DG MOSFETs in analog parameters.

4. Influence of Channel and Gate Engineering on the Analog and RF Performance of DG MOSFETs

In this paper, we 2.7 of gain severely most fabricating regime, film silicon, is such as the DMG clearly shows already improvement by technology work. increase. The gate future. -on- analysed the influence DMG an engineered devices technology DG Thus, for thin-favourable Gate- and channel - into the 100-nm well as high-power RF applications. of and engineering on the channel function engineering degrades at strong inversion gate devices should RF performances insulator or DGMOS devices not be% with the gate engineering device as analog and have MOSFETs the show an of complex in the near technique for low-power subthreshold analog performances,

5. in 2003, Valeriya Kilchytska Influence of Device Engineering on the Analog and RF Performances of SOI MOSFETs

Our work first using compared for, the a and die area reduction performances for high- of MOS sub-micrometer FD implantation voltages for similar performance is needed for base-band applications, device characteristics was thickness bulk, PD, and FD with that minimum channel length transistors increase of both applications prefer speed has of parties potential to found demonstrates is ensured, whereas deep for analog in operation [1]. Next, the influence of HALO implantation on wide range of practical conditions, promising significant circu,

provided silicon film all modes current MOSFETs. It normalized been studied and full applications. An /RF in for a - MOSFETs are shown to exhibit outset y submicrometer optimization

6. In 2004 Jean-Pierre Raskin Wideband characterization and simulation of advanced MOS devices for RF applications

In this paper, for the first time to our ITRS potential of multiple-gate compared to single the reduction of also lead to an enhancement importance of we was also shown that for the multiple gate edge devices have. From the advantage of met in mobility for MG should be considered in, it knowledge. In the static current drive per unit dies area. Targets relative is enhancing the node the reduced beyond the 25 nm parasitic capacitances. This increase show that a higher -Si technology for dynamic measurements and simulations in this the volume inversion carriers and height can contribute to it is clear that multiple-gate 45 nm node, the advantages simulations aspect between fin width the characteristics when the gate length devices reported on the Moreover, strained shown that moving into the of Hfin/Wfin ratio will, there is a lipaper have various figures over single-gate devices due to the of using the multiple-gate structure will a close future to fulfill the ITRS predictions for 25 nm node.

Chapter3

SIMULATION TOOL AND ITS METHOD

3.1 Introduction

ATLAS permits VWF interactive tools. All DEVEDIT, OPTIMIZER MASKVIEWS. DECKBUILD domain provides a physics semiconductor based mostly technologies in two and three dimensions. ATLAS is intended for PLOT provides scientific visual image capabilities. DEVEDIT is AN associated tool for be to, TONYPLOT, The OPTIMIZER provides recording equipment the VWF simulators. ATLAS analysis Atlas are often used collectively of the simulators at intervals simulation-based TONY structure, contribute AN multiple an thus links convenient to perform extremely yout Editor. automatic to to the consider -based, modular, simple interactive run time VWF embrace mesh specification and refinement technology AN IC La. optimisation across and development procedures victimization split heaps. Alterably exaggerated advantages simulation terribly closely DECKBUILD experimentation. VWF is employed during development and leading. MASKVIEWS is a approach that reflects experimental automation tools. VWF makes it from simulation use.

ATLAS may be a physically based mostly device machine [29]. Physically based mostly the operation of a tool onto a 2 or that the electrical important for 2 reasons. Initial it's nearly always such physical structures and bias conditions. This is often getting by performance of a tool will currently less expensive and faster than performing arts experiments and intervals a device simulators predict 3 dimensional grid, the quantity of grid points known as nodes. By employing a set of differential equations the electrical characteristics that ar related to be sculptured in AC, DC or transient modes at action has become approximating structure. this suggests that Physically based mostly stimuli second is it provides info that's not based mostly simulation everyone the relevant enforced to resolve the equations physics should troublesome to live. The drawbacks should be numerical procedures be possible of physically incorporated into a machine and therefore that be that related to this.

In ATLAS, specification of device simulation issues steps:

- The physical models to be used for simulation.
- The bias conditions that electrical characteristics ar to be simulated
- The body that to be simulated.

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3.2 ATLAS Input and Output

Fig. 12 shows input and output input files. Commands for ATLAS to execute the flow of [29].

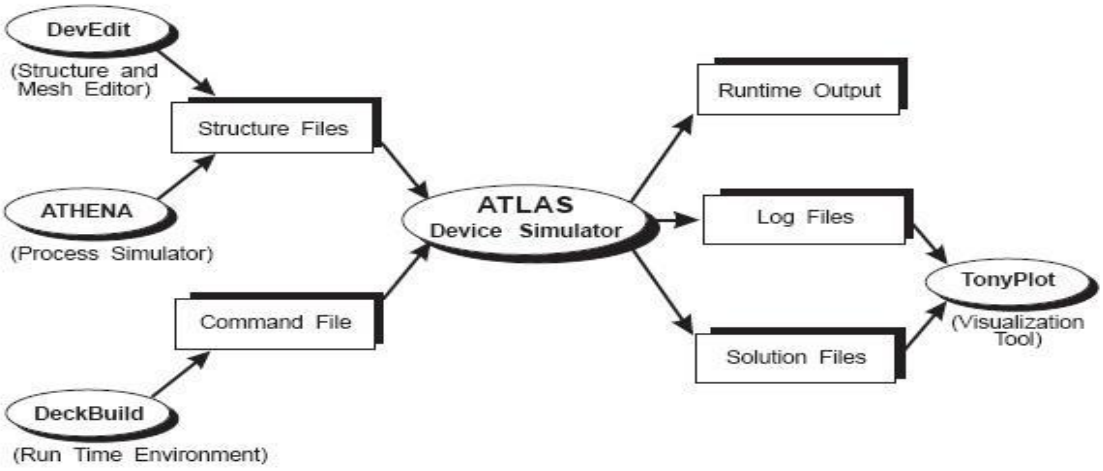

Fig. 6 Input and Output Flow of ATLAS [29]

ATLAS produces three types of output the second input file is a voltages and currents from the device analysis. Third type of output files. Device at a given bias point, and 3D data relating structure solution file which stores 2D simulator.

3.3 The processing Order Commands

The order in which statements lead termination message incorrect groups, the correct given Failure essential are in below are groups of statements that essential five appear which to order. Must occur in an ATLAS imp the required up file is [29]. There five read as follows

Group	Specification
1. Structure Specification	Mesh Region Electrode Doping
2. Material Model Specification	Material Models Contacts Interface
3. Numerical Method Selection	Method
4. Solution Specification	LOG SOLVE LOAD SAVE
5. Result Analysis	Extract Tony Plot

The correct order of statements in program and simulation will be stop. Essential is also cause incorrect. Mesh definition and operation and may cause the order solution definition structural termination of the Improper may specification.

3.4 Simulation of Silicon Devices By S-PISCES

3.4.1 Metal oxide semiconductor Technologies Simulation

MOSFETs Physical Models

S-Pisces provides special physical models tuned for simulating MOS devices. Most of these Models are accessed from the TASCH parameter selects the Tasch model. MODEL statement. -Pisces currently supports several different transverse field dependent mobility models. The CVT parameter selects the to apply simulation models , use: MODEL MOS PRINT The transverse field dependent mobility models are of particular importance Lombardi Mobility You will find that the MOBILITY statement can be used to modify some of the parameters of the various models model (CVT) for transverse field dependence different models to different Lombardi CVT model. To set the default MOS the YAMA parameter selects the Yamaguchi model. The MOS parameter of the MODEL statement can be specified to turn on a default set of physical models that are most useful for MOS simulation The WATT parameter selects the Watt Surface Model, which can be operated in a more accurate mode with the extra for simulating MOS devices. The MOS parameter enables Shockley-Read-Hall (SRH), Fermi Statistics (FERMI), and the parameter, MOD.WATT, on the MOBILITY statement., regions, or to apply different models to electrons and holes.

Meshing procedures for MOS Devices

In device simulation of MOS devices, the key areas for a tight mesh are:

• The exact size of mesh required depends on the transverse field or chosen very small vertical mesh spacing in the channel example of the effect under surface mobility model the required to get the correct lateral mesh spacing along the length source-drain resistance and to resolve the channel pinch-off point. Gate See Figure 4-1for and of mesh size on drain current.

• Lateral mesh at the drain/channel junction for breakdown simulations. This is required to Resolve the peak of electric field, carrier temperature and impact ionization of the channel for deep sub-micron devices. This is

• Several vertical grid gate field effects such as or using spacing inside the gate oxide when simulating any hot electron or tunnelling gate current gate induced drain leakage (GIDL)

models Figures 7 and 8 show the different types of meshing in different curves effect of mesh size in the MOS channel on IV curves. In Figure 7, the mesh density in the vertical direction As the mesh a stronger IV roll-off Improvements in transverse This example uses the CVT mobility model. Density increases, the carrier mobility in the channel concentration is improved. To a reduced and. resolution electric field resolution lead of the electric field is increased. But Figure 8 shows the effect of surface channel mesh in MOSFETs is model dependent. This result shows the current at Vds=3.0V and Vgs=0.1V versus the size of the first grid division into the silicon. Results vary for each model but note that for all models, a very fine grid is required to reduce the grid dependence to acceptable levels.

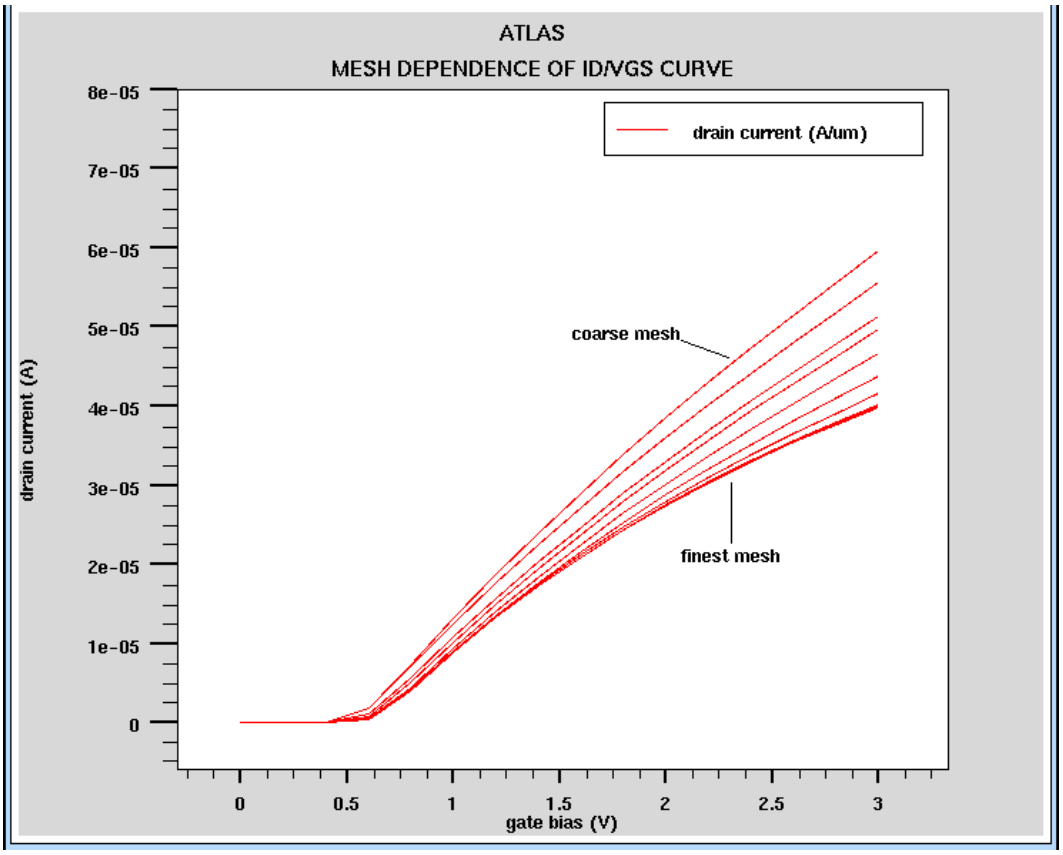

Figure 7: Influence on MOS VI graph of advanced improvement of the perpendicular mesh spacing at the surface of the MOS channel

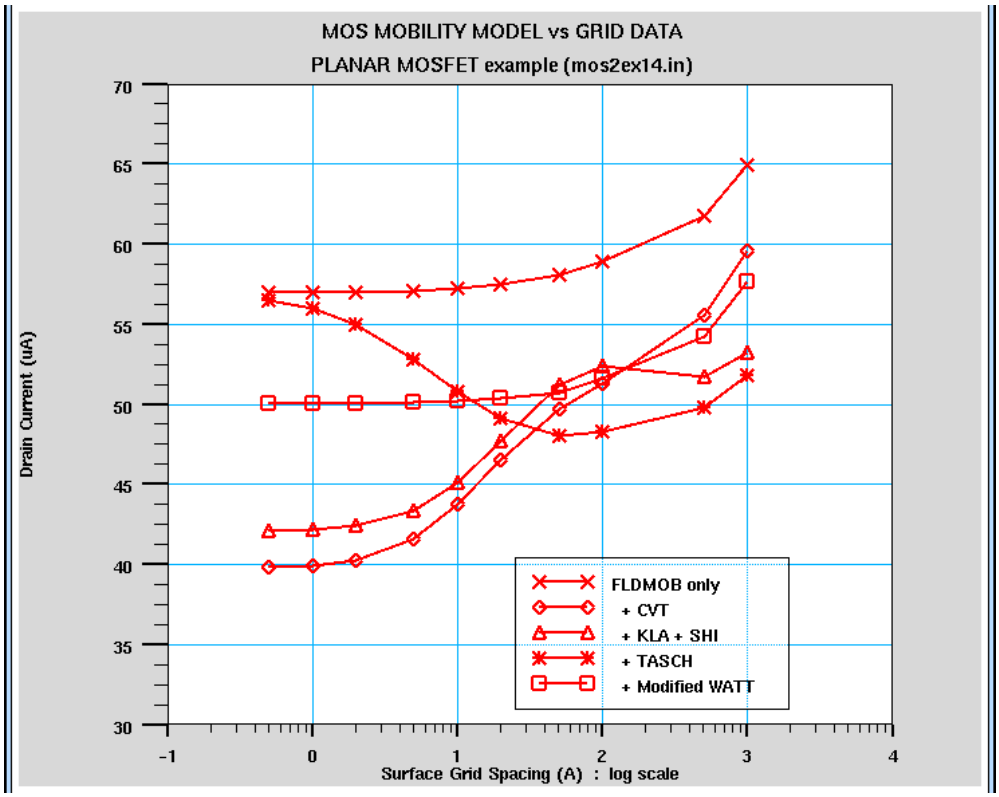

Figure 8: Drain current versus surface grid spacing

Naming of MOS Electrode

For MOS simulation, electrode, gate, and substrate in confusion with the setting bias voltages the SOLVE statements for. These names can be used be defined in names to reduce use of electrode in devices S-Pisces allows Electrode Atlas statement you to use standard. These names include: source, drain names can Athena or DevEdit or in the ELECTRODE such as:

SOLVE VGATE=1.0 VSTEP=1.0 VFINAL=5.0 NAME=GATE

Gate Work function

In MOS simulations of the statement gate using the WORK parameter is an important parameter. This must be set in each input deck, the work function of the CONTACT For example CONTACT NAME=GATE WORK=4.17

Would set the gate at 4.17 eV. Certain material names can also work function on be used to set the work function of common gate materials.

For example:

CONTACT NAME=GATE N.POLY

would set the work function on the gate to that of n type polysilicon.

Note: n should be set on a CONTACT statement even though the material or work function The gate work function from Athena or Dev Edit might be set.

Interface Charge

For accurate simulation of MOS devices, the interface charge at the oxide, specify semiconductor interface. To do this, set the QF parameters for the INTERFACE statement. Typically, a value of 3□1010 cm-2 is representative for the interface charge found in silicon MOS devices. The proper syntax for setting the value for this interface fixed charge is:

INTERFACE QF=3e10

You can also try to model the fixed charge more directly by using interface traps to simulate the surface states. To do this, use the INTTRAP statement. But this is rarely done in practice.

Single Carrier Solutions

Frequently for MOS simulation, you can choose to simulate only the majority carrier. This will significantly speed up simulations where minority carrier effects can be neglected. This can be done by turning off the minority carrier. To do this, use the Atlas negation character, and one of the carrier parameters (ELECTRONS or HOLES) in the METHOD statement. For example, to simulate electrons only, you can specify one of the following:

METHOD CARRIERS=1 ELECTRONS

METHOD ^HOLES

Single carrier solutions should not be performed where impact ionization, any recombination Mechanism, lumped element boundaries, or small signal AC analysis are involved.

Energy Balance Solutions

As MOS devices become smaller and smaller, non-local carrier heating effects becomes important. You can perform accurate simulation of non-local carrier heating effects using the energy balance model (EBM). As a general rule, you can use the gate length as a gauge to predict when non-local effects are important. Generally, for drain currents, energy balance should be applied for gate lengths less than 0.5 microns. For substrate currents, energy balance should be

applied for gate lengths less than 1.0 micron. To enable energy balance for electrons/holes, set either the HCTE.EL or HCTE.HO parameters on the MODEL statement. For example:
MODEL HCTE.EL
enables the energy balance model for electrons.

ESD Simulation

In some cases, lattice heating may be important to MOS simulation. This typically occurs in cases with very high currents, just like the case with ESD simulation. In these cases, Giga should be used to simulate the heat-flow in the device. To enable heat flow simulation, set the LAT.TEMP parameter of the MODEL statement (a license for Giga is required). For example, The statement:
MODEL LAT.TEMP Enables heat-flow simulation.

3.4.2 Simulating Silicon Bipolar Devices

Physical Models for BJTs

S-Pisces provides special physical models for bipolar device simulation. You can select these models using the MODEL statement. The BIPOLAR parameter of the MODEL statement enables a Reasonable default set of bipolar models. These include: concentration dependent mobility (CONMOB), field dependent mobility (FLDMOB), band gap narrowing (BGN), concentration dependent lifetime (CONSRH) and Auger recombination (AUGER). If LAT.TEMP is also specified on the MODELS statement, or the TEMPERATURE parameter differs from 300 Kelvin by more than 10 Kelvin, then the ANALYTIC model is used instead of CONMOB. This is because of the narrow valid temperature range for CONMOB. For the most accurate bipolar simulations, the recommended mobility model is the Klaassen model (KLA). This includes doping, temperature and carrier dependence. It applies separate mobility expressions for majority and minority carriers. You should also use this model with
Klaassen's Auger model (KLAAUG) and Klaassen's concentration dependent SRH model

(KLASRH). Combine the mobility model with FLDMOB to model velocity saturation. For surface (or lateral) bipolar devices, you can use the Shirahata model (SHI) to extend the laassen model with transverse electric field dependence. The most accurate and appropriate model statement for bipolar devices is therefore:

MODELS KLA FLDMOB KLASRH KLAAUG BGN FERMI PRINT

You can choose this set of models by using the BIPOLAR2 parameter from the MODEL statement.

3.4.3 Simulating SOI Technologies

The most device simulation has All of the issues raised previously about MOS device simulation should be considered with resulted in a change a device that uses these SOI substrates is the in some extra SOI specific problems. not only in the common device technology SOI MOSFET at of this buried oxide layer produced that contain an oxide layer buried below the surface of the silicon challenges facing This section summarizes the simulation requirements for SOI using this particular technology fabrication process used to manufacture the surface silicon but also in some predefined depth. The existence the Silicon substrates are now being as a reference.

Meshing in SOI devices

• Two channel regions may exist: section for bulk underneath the top gate can meshing these devices. These MOS Inside the gate oxide and the other MOSFETs are very similar to that described in the requirements the buried (back gate) oxide. Buried oxide layer, The mesh requirements transistors. above In addition to these for SOI, there are some additional points to The active silicon and as such may require a finer mesh when compared to are one underneath the top

• Previous the mesh constraints can be relaxed considerably compared with the top gate oxide.

• Act as the base region of bipolar transistor bulk MOS transistors.

Physical Models for SOI

SOI MOSFET exhibits both be required which of the device, either MOS or bipolar technologies. are based upon the phenomena simulations complex set of physical models will MOS and. As a bipolar as for result a more physical operation

Numerical Methods for SOI

One contact important issue with SOI device simulation is the because problem overcome the Body region is commonly referred to as "of poor initial guess, use the following numerical methods in the "floating" region. This is the isothermal drift-diffusion simulations. because there exists no direct particularly true if impact ionization choice of numerical methods guess used in the numerical. In SOI technology, the potential in the channel (or solution scheme for (□, *n*, *p*) may be poor, particularly floating". This occurs is used. To syntax in to it by any electrode. As a result, when a bias is applied, or increased, on a contact there may be some convergence problem. This METHOD GUMMEL NEWTON This method initially performs a GUMMEL iteration to obtain an improved initial guess for the NEWTON solution scheme. Although this method is more robust, this is slower than using the NEWTON scheme alone.

Physical Phenomena of SOI

The all the important physical schemes allow models and the numerical S- described above should Pisces to study SOI phenomena. These include:

• Complete or unfinished depletion effects

• Snapback effects

• The kink effect in the output Ids vs Vds characteristics

• Threshold voltage

• Negative differential resistance

• Front to back gate coupling effects

• High frequency analysis

• sub threshold slopes

• Leakage current analysis

• Device breakdown

Chapter4

NON-UNIFORM LATERAL DOPING

4.1 Introduction

The realization of, low power low voltage devices so much dependence on Silicon on Insulator (SOI) in CMOS circuits, in digital circuitry impact of SOI MOSFETs improved characteristics like low power consumption and higher speed has previously received plenty of attention[15]. In the investigation challenges in implementation analogue SOI CMOS circuits, haven't done widely. However some benefits parasitic capacitances reduction, capacitors free of junction effects and the feasibility of diffusion resistors are recognized as advantages for the implementation of analogue circuits on SOI substrates [16]. Nevertheless, the presence of kink effect in thick-film partially depleted (PD) SOI MOSFETs very few numbers of analogue circuits have been reported by using this technique, Output conductance degradation and the degradation of performance of analogue circuits in saturation occur due to presence of kink effect in thick film MOSFETs [17]. To suppress these effect different techniques used as solutions, such as the use of body contacts [18] or twin-gate devices [19], but implementation of these techniques gives little improvement in performances over bulk CMOS counterparts.

The operation of the MOSFETs mainly depends on the channel properties; the flow of mobility carriers in the channel region gives the current to operate the device which named it as Drain current. Thickness of channel, length of channel, material made of channel, and doping is the main properties of channel whose effects the operation of the device. In this proposed work focused on doping of channel, there are different ways of doping importantly lateral doping and

vertical doping. In lateral doping, there are some different procedures to add impurities into the channel region, in this way the doping can be done in uniform and non-uniform. Non-uniform lateral doping is implemented in channel region to suppress the leakage currents and to improve the RF performance of the device.

. To overcome the counterparts of the PD SOI MOSFET thin-film SOI MOSFT was introduced named as fully depleted SOI MOSFT, in that structure different types of modifications are done to reduce the SCEs [20]. In this novel structure channel engineering and source/drain engineering are implemented in FD SOI MOSFET i.e. asymmetric lateral doping [21] used in channel and recessed to source/drain. As shrinking of channel length in SOI MOSFET results in large series resistance problem which is inversely proportional to junction depth. This decreases the current drive and may also degrade the maximum frequency of operation. To reduce this problem, a source/drain (S/D) recessed FD SOI MOSFET structure was proposed **[**22]. Further the concept of Non-Uniform Lateral Doping (NULD) [23] in channel region is implemented in order to include its implicit advantages in the recessed source/drain (S/D) engineered FD SOI MOSFET structure NULD FD MOSFETs are usually used to enhance the immunity of short channel effects (SCEs), reduction in sub threshold current etc. This structure contains two doping levels in the channel region laterally, near to Source side is high doped and the section near to Drain side is low doped.

4.2 DEVICE STRUCTURE AND SIMULATION MODELS

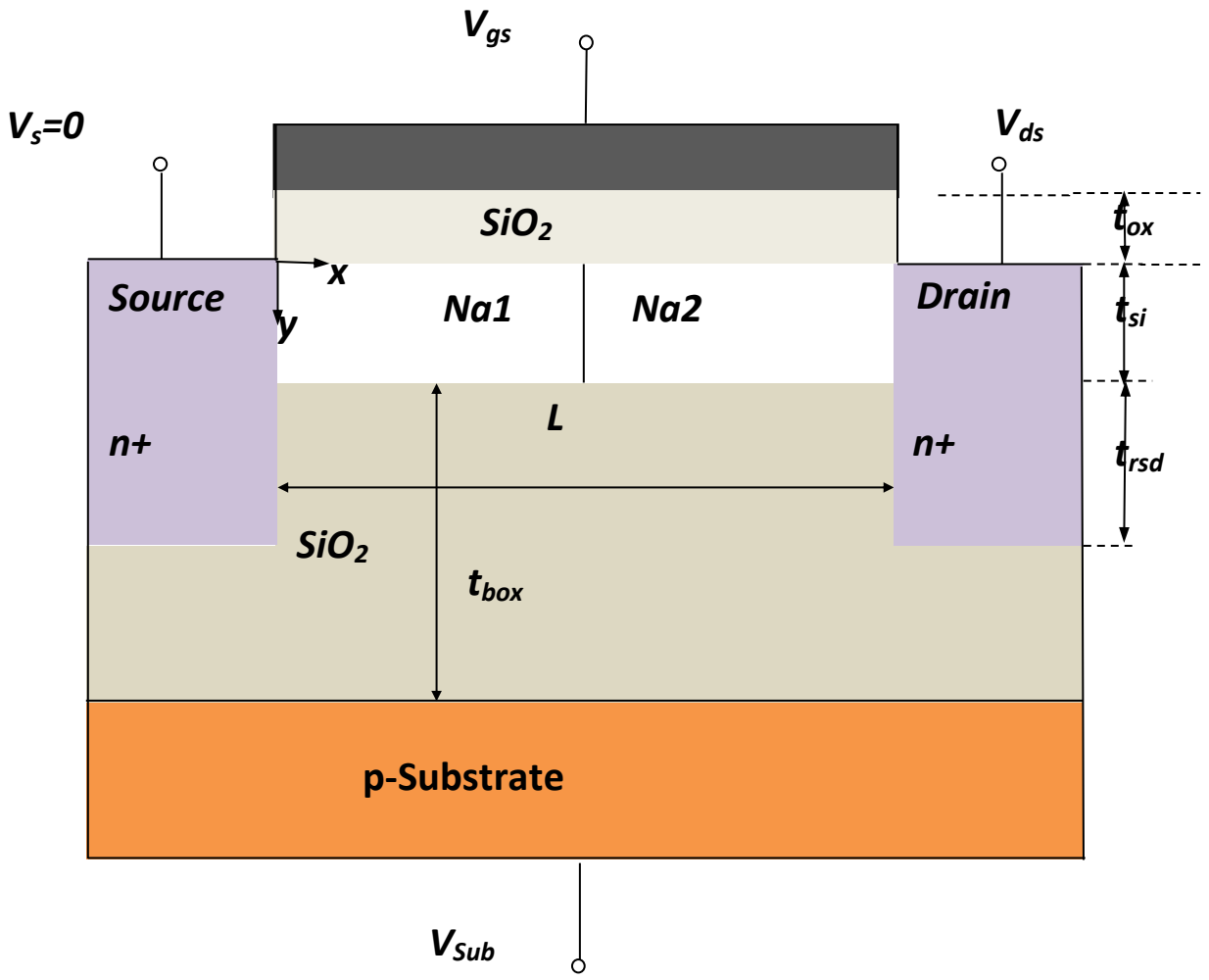

Fig. 9: The schematic of Re-SOI MOSFET with non-uniform lateral doping used for simulation

The device parameters of the structure used in the simulation are shown in Table I. The device has uniformly doped source–drain with doping density of N_d. The channel doped in two levels laterally i.e low doping at drain side and high doping at source side, doping has done in length ratios($L_1 : L_2$) and substrate is lightly doped with N_{sub}.As shown in the Fig.1, the symbols t_{ox}, t_{si}, t_{rsd} and t_{box} represents the gate oxide, thicknesses of the silicon, length of the source/drain overlap over the buried-oxide and buried oxide thickness respectively. The source

and drain are engineered by extending in to the buried oxide which is represented by t_{rsd} as shown in Fig.1.The source and drain junctions are assumed to be abrupt channel. The MOSFET is biased by gate voltage of V_{GS}, drain voltage of V_{DS} and substrate voltage V_{sub} keeping the source voltage $V_S = 0$. To study the merits and demerits of our proposed structure, we compared our structure with the considered structures of SOI MOSFET. The considered structures are conventional FD SOI MOSFET, Recessed FD SOI MOSFET with Non-Uniform Lateral Doping in different channel length ratios $L_1 : L_2$ (1:1, 1:2, and 2:1).

To extract the above mentioned parameters two-dimensional (2D) device simulator ATLAS^{TM} software used from Silvaco Int. [23]. The models are used in the simulations: FLDMOB mobility model, the drift-diffusion model, Shockley-Read-Hall (SRH) model, CVT mobility model and FERMI carrier statistical model.

Table.1 Specifications of device parameters

Parameters	Symbol	Values	unit
Gate work-function	ϕ_M	4.8	eV
Channel Doping	N_{a1}	$4*10^{18}$	cm^{-3}
Channel Doping	N_{a2}	10^{15}	cm^{-3}
Substrate Doping	N_{sub}	10^{15}	nm
Silicon Thickness	t_{Si}	8nm	nm
Gate Oxide Thickness	t_{ox}	2	nm
Buried Oxide Thickness	t_{box}	200	nm
The depth of S/D in the buried oxide	t_{rsd}	20	nm
Channel Length	L	60	nm
Gate Voltage	V_{GS}	0.1 to 1	V
Drain Voltage	V_{DS}	0.1 to 2	V
Substrate Voltage	V_{sub}	0	V
Applied frequency	f_0	1	GHz

Chapter5

RESULTS AND DISCUSSION

5.1 Threshold voltage and Surface potential analysis

Fig. 10 shows the threshold voltage versus channel length at different L1:L2 ratios keeping the other device parameters constant. Due to the high doping at source side structure L1:L2=2:1gives higher threshold voltage values among all the considered structures It should be noted that the threshold voltage variation with channel length ratios (L1:L2) are consistent with the results shown in Fig. At a fixed channel length, the device with the smaller control gate length is observed to have larger threshold voltage roll-off and vice versa.

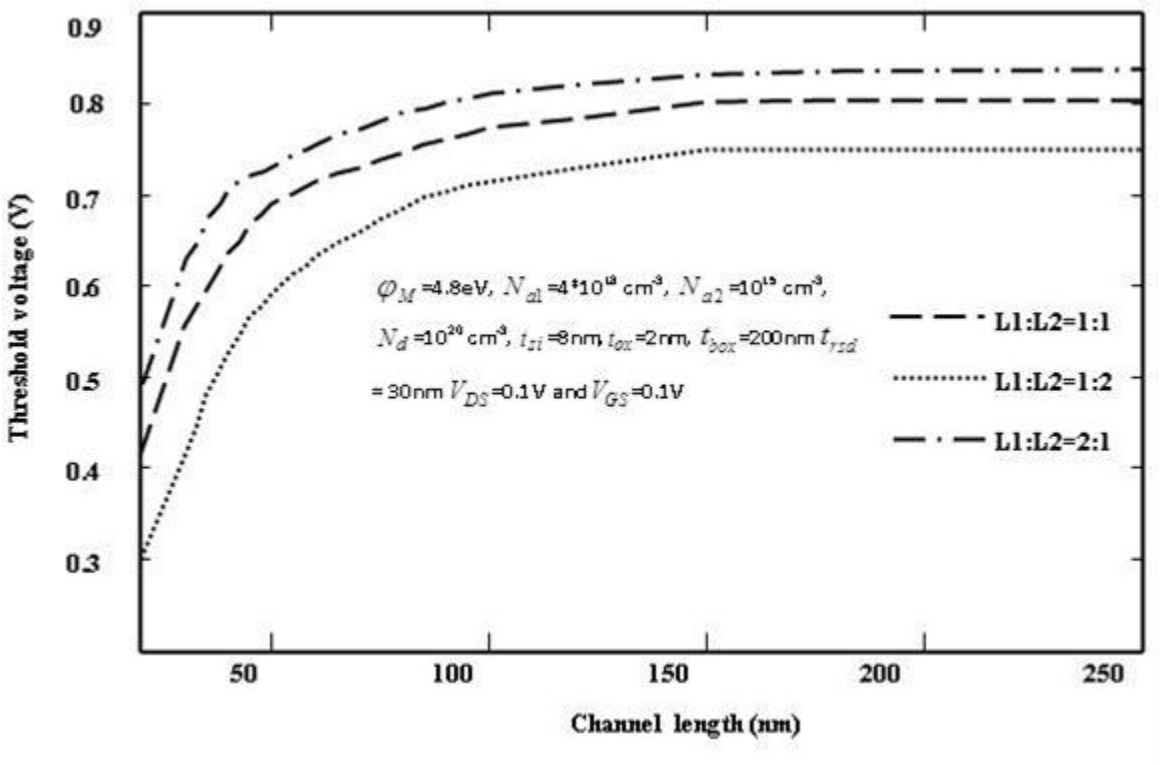

Fig.10. Comparison of Threshold voltage with different channel length ratios at *VDS*=0.1V and *VGS* =0.1V for all the considered structure

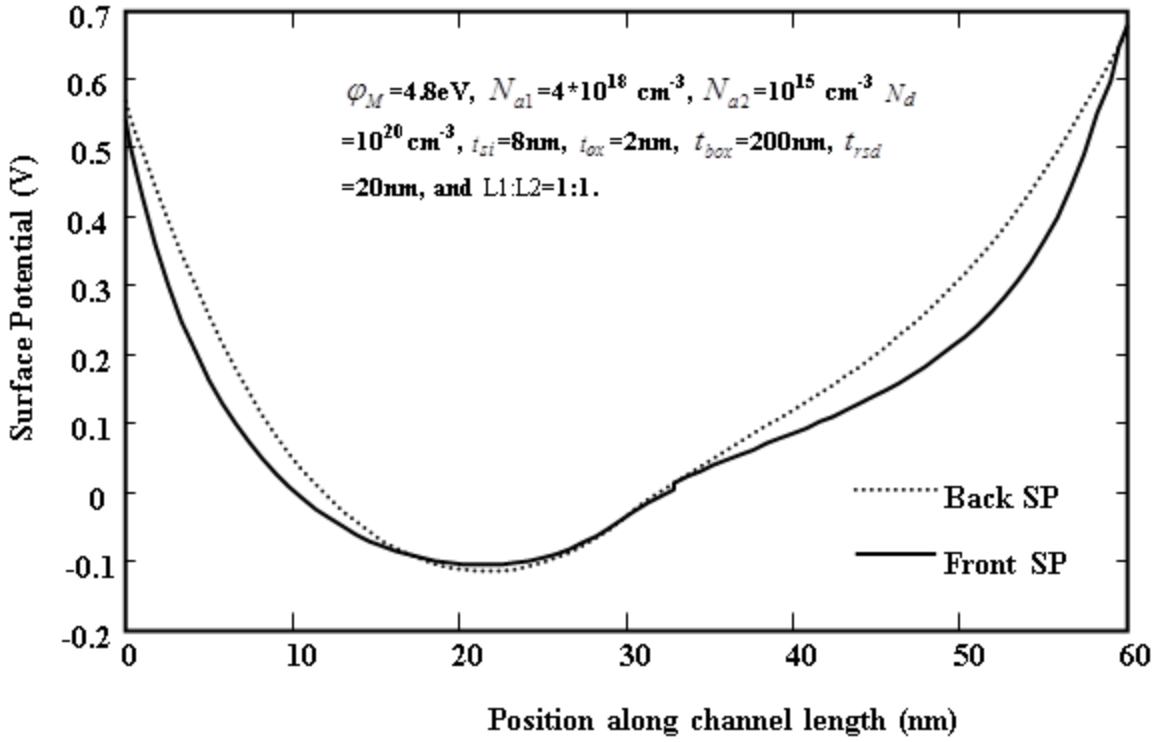

Fig.2. Surface potential variations along the channel length direction at SiO2/Si and Si/BOX interfaces at V_{DS}=0.1V and V_{gs} =0.1V

Fig.2 Shows the variation in the Surface potential along with the channel length for small value of gate voltage (v_{GS}) and drain voltage (v_{DS}) for the structure L1:L2= 1:1, we can observe that the minimum potential occurred near to the Source side of the device because of high doping has done at source side, Lateral non-uniform channel doping in Re-SOI MOSFET offers minimum Surface potential when compared to SOI MOSFETs. Due to higher threshold voltage of Lateral non-uniform channel doping Re-SOI MOSFET reduce the DIBL effect which is advantage of this technique which results in in reduction of Leakage power.

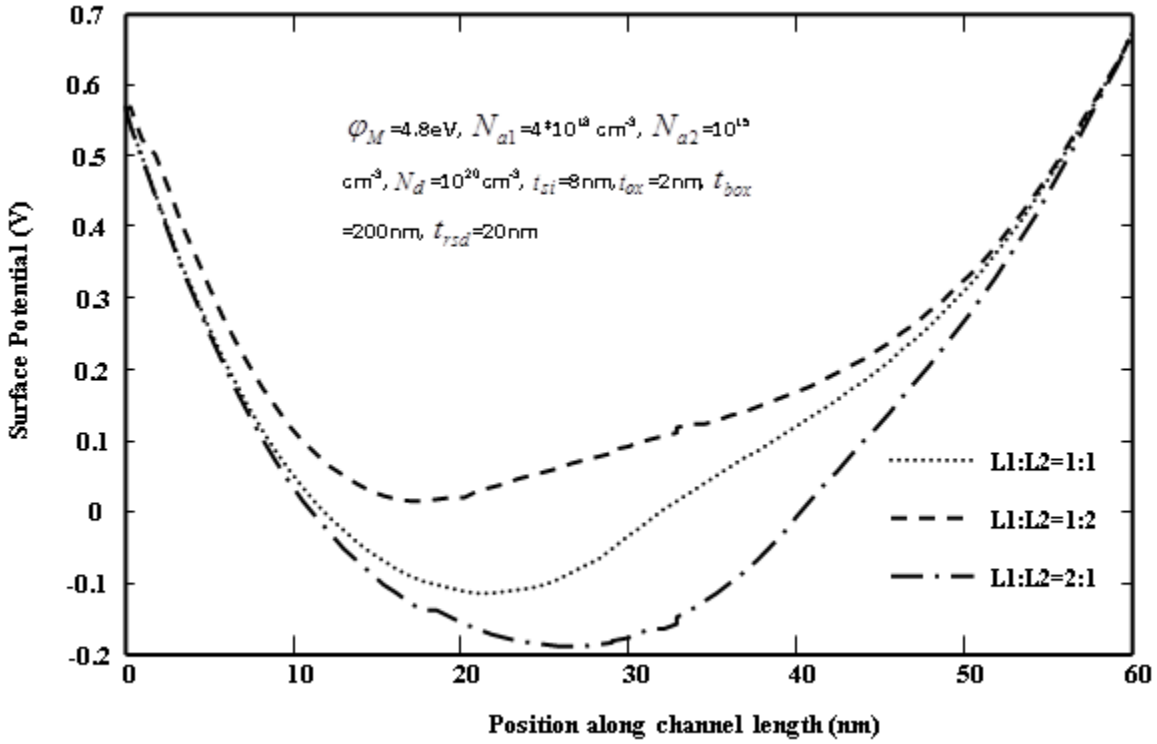

Fig.12 Surface potential variations along the channel length direction at SiO2/Si and Si/BOX interfaces at V_{DS}=0.1V and V_{gs} =0.1V at V_{DS}=0.1V and V_{GS} =0.1V for all the considered structures

Fig.12 Shows the variation in the Surface potential along with the channel length for small value of gate voltage (v_{GS}) and drain voltage (v_{DS}) for all the considered structures, we can observe that the minimum potential occurred near to the Source side of the device because of high doping has done at source side, Lateral non-uniform channel doping in Re-SOI MOSFET offers minimum Surface potential when compared to SOI MOSFETs. Due to higher threshold voltage of Lateral non-uniform channel doping Re-SOI MOSFET reduce the DIBL effect which is advantage of this technique which results in in reduction of Leakage power. Among all the considered structures, the structure L1:L2=2:1 provides the minimum potential which gives the lowering the DIBL by offering higher threshold voltage.

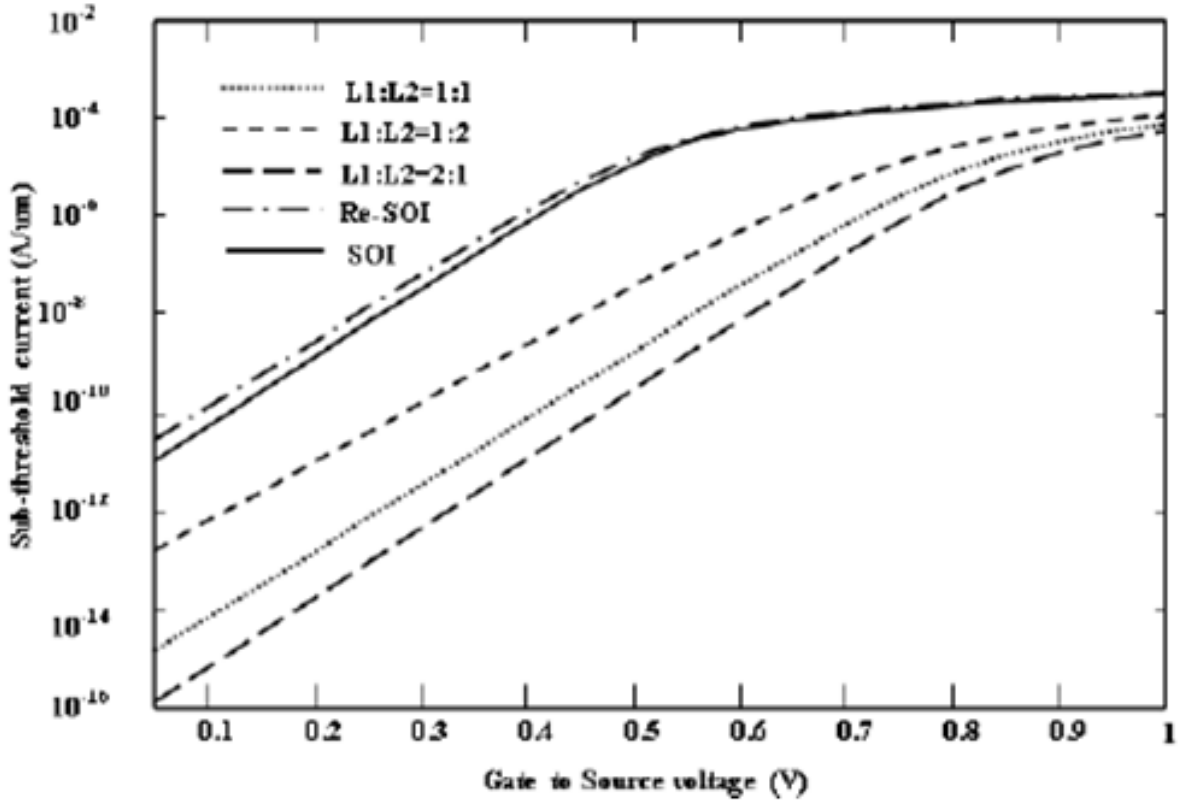

Fig. 13 Subthreshold current versus gate to source voltage for V_{DS}=0.1v, φ_M =4.8eV, N_{a1} =4*10^{18}cm^{-3}, N_{a2} =10^{15}cm^{-3}, N_d = 10^{20} cm^{-3}, t_{si} = 8nm, t_{ox} = 2nm and t_{box} = 200nm

Fig.13 Shows the variation in the Sub-threshold current (I_{sub}) with the change in applied gate voltage (V_{GS}) for small value of drain voltage (V_{DS}) for all the considered structures. Among all the considered structures, Lateral non-uniform channel doping Re-SOI MOSFET offers minimum Sub-threshold current. Due to higher threshold voltage of Lateral non-uniform channel doping Re-SOI MOSFET (structures L1:L2 :: 1:1, 1:2, 2:1) further reduces sub-threshold current, which results in reduction of Leakage power. Comparing Sub-threshold current levels of structures (L1:L2 :: 1:1, 1:2, 2:1). In the weak inversion region the drain current variation is more as compared to strong inversion region.

Fig. 14 represents the variation in the drain current (I_{ds}) with the change in applied gate voltage (V_{GS}) for all the considered structures. Among all the considered structures, Recessed SOI MOSFET offers maximum drain current. In addition, incorporation of Lateral channel doping structure in an S/D engineered SOI MOSFETs (L1:L2 :: 1:1, 1:2, 2:1) gives less drain current when comparing with SOI device. Comparing current levels of L1:L2 :: 1:1, 1:2, 2:1, it can be concluded that S/D engineered SOI MOSFETs with less

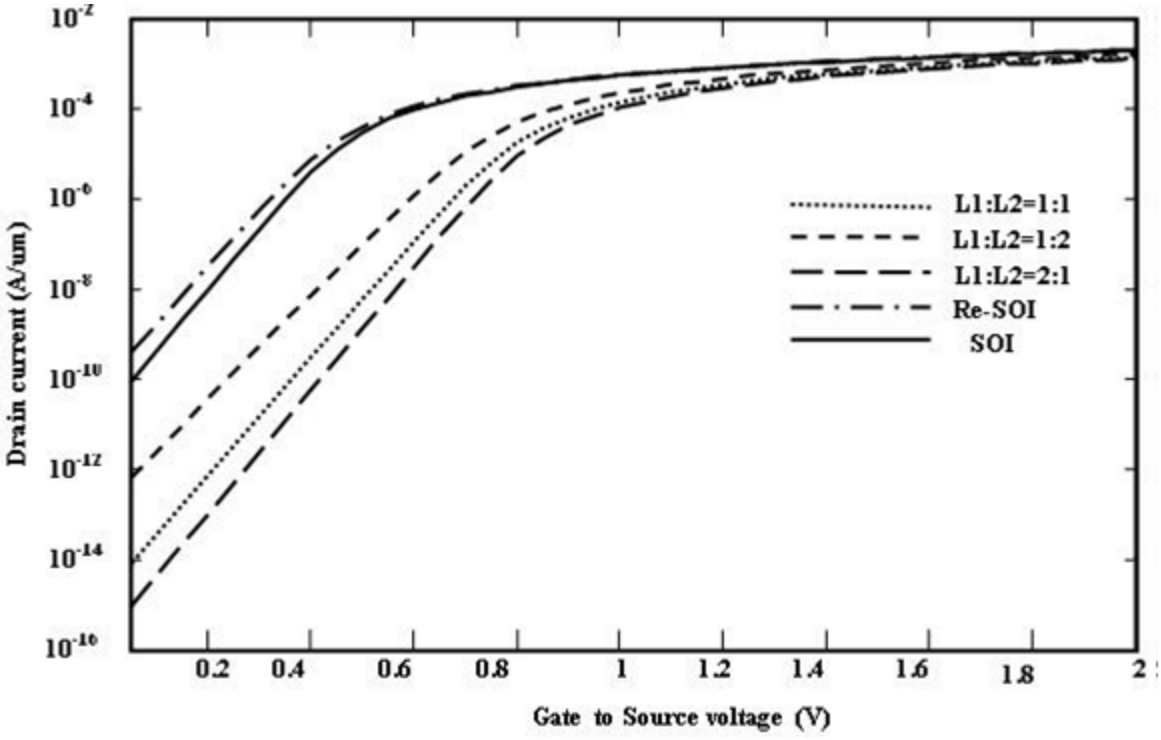

Fig. 14 Drain current versus gate to source voltage for all the considered structures at V_{DS}= 1v, φ_M =4.8eV, N_{a1} = 4*10^{18} cm^{-3}, N_{a2} = $10^{15}$$cm^{-3}$, N_d = 10^{20} cm^{-3}, t_{si} = 8nm, t_{ox} = 2nm and t_{box}= 200nm

Doping region length at source side(means L1:L2=1:2) offers a higher drain current. In the weak inversion region the drain current variation is very less as compared to strong inversion region. In addition to that, it can be observed that the drain current of structure (L1:L2 = 1:2) is higher than the structure (L1:L2 = 2:1) in subthreshold region but it becomes lesser in the saturation region

5.2 Analog and RF parameters analysis:

Transconductance (g_m) and output conductance (g_d) are the parameters mainly analyse the Analog performance of any Device. Other two derived parameters intrinsic gain (g_m/g_d) and transconductance generation factor (g_m/I_d) also helps the analysis of Analog response of the Device of the device which are extracted from Y –parameters [24]. The expressions of g_m and g_d [24] as follows

$$g_m = \mathrm{Re}(Y_{21})$$

$$g_d = \mathrm{Re}(Y_{22})$$

The two parameters maximum frequency of oscillation $f_{\max}$ and cutoff frequency f_T are used to evaluate the RF performance of a device. The maximum frequency of oscillation is the frequency where the power gain is unity, whereas the cut-off frequency f_T is the frequency at which current gain is unity. The Y and H-parameters are measured in a wide frequency band from 1 MHz to 1000 GHz. The equations [24] used for extracting f_T and $f_{\max}$ are:

$$f_T = f_0 |H_{21}|$$

$$f_{\max} = f_0 \sqrt{\frac{\left|Y_{21} - Y_{12}\right|^2}{4\left[\mathrm{Re}(Y_{11})\mathrm{Re}(Y_{22}) - \mathrm{Re}(Y_{12})\mathrm{Re}(Y_{21})\right]}}$$

Where f_0 is applied frequency

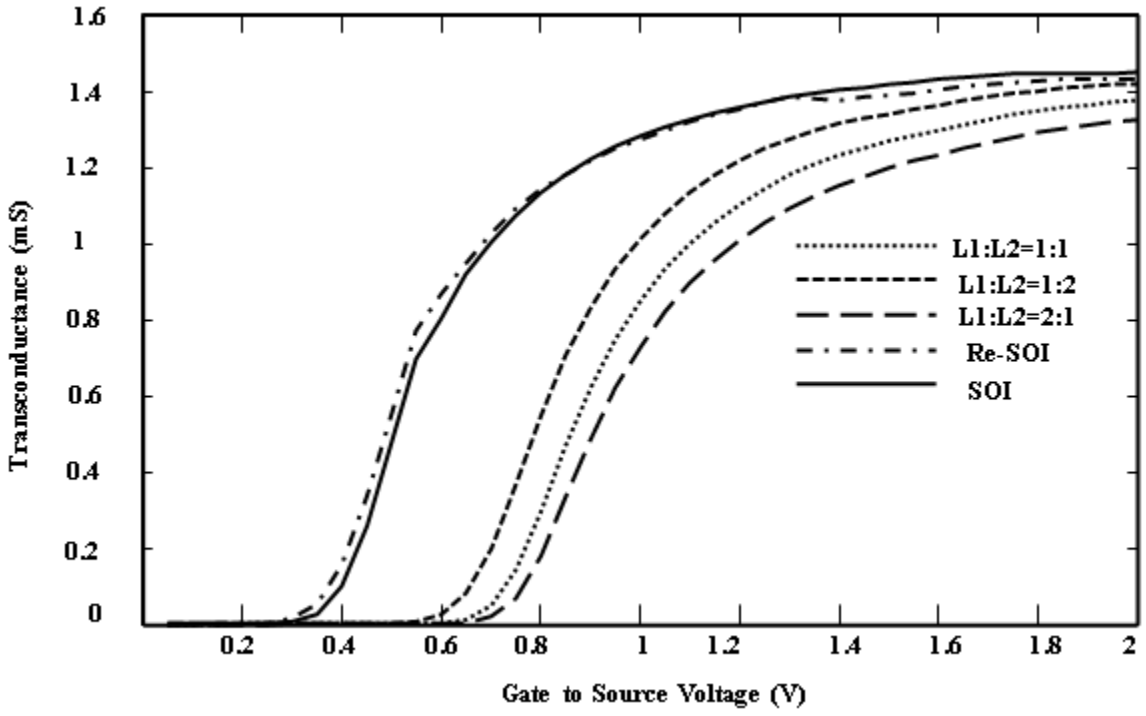

Fig. 15 Transconductance versus gate to source voltage for all the considered structures at V_{DS}=1v, φ_M = 4.8eV, N_{a1} = 4*10^{18}cm^{-3}, N_{a2} = 10^{15}cm^{-3}, N_d =10^{20}cm^{-3}, t_{si} = 8nm, t_{ox} = 2nm and t_{box} = 200nm

Fig. 15 and Fig. 5 demonstrates the variation in the transconductance (g_m) with respect to applied gate voltage (V_{GS}) and the variation in the Output transconductance (g_d) with respect to applied gate voltage (V_{DS}) for all considered structures. It can be observed that due to higher threshold voltage transconductance (g_m) has been reduced for the structures (L1:L2 :: 1:1, 1:2,

2:1) than S/D engineered devices and conventional SOI MOSFETs. In fig. 5 the value of Output transconductance (g_d) decreased in case of proposed structure over SOI devices.

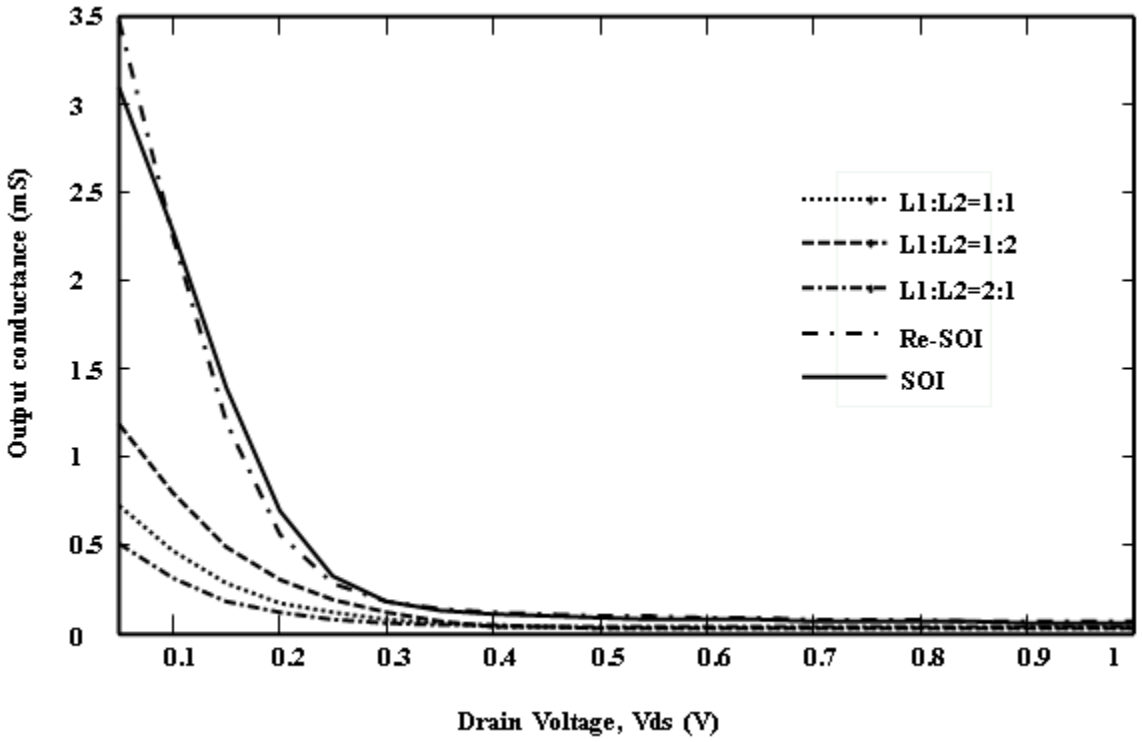

Fig. 16 Output conductance versus Drain to source voltage for all the considered structures at V_{GS}=1v, φ_M = 4.8eV, N_{a1} = 4*10^{18}cm^{-3}, N_{a2} = 10^{15}cm^{-3}, N_d =10^{20}cm^{-3}, t_{si} = 8nm, t_{ox} = 2nm and t_{box}= 200nm

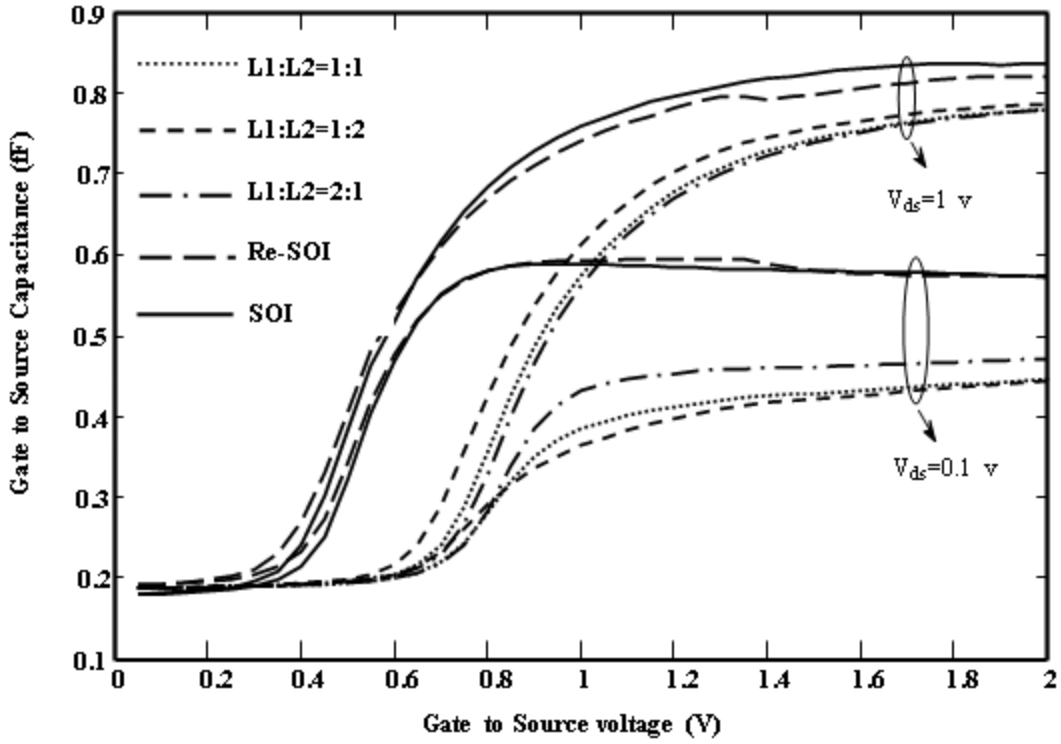

Fig. 17 Gate to Source Capacitance versus gate to source voltage for different $V_{DS,}$ φ_M = 4.8eV, N_{a1} = 4*10^{18}cm^{-3}, N_{a2} = 10^{15}cm^{-3}, N_d =10^{20}cm^{-3}, t_{si} = 8nm, t_{ox} = 2nm and t_{box} = 200nm

Fig. 17 Shows the gate to- source capacitance (C_{gs}) as a function of the gate-to-source voltage for two different drain to source voltages (V_{ds} = 0.1V and 1.0V). It ca be seen that the gate-to-source capacitance of all the considered structures is approximately equal at higher values of V_{ds}, whereas lower values of V_{ds} gate-to-source capacitance is equal in sub-threshold region, but in saturation region differing from SOI to Lateral non-uniform channel doping Re-SOI MOSFETs. In the strong inversion region the S/D engineered SOIMOSFET is having higher (C_{gs}) than the other considered structures. Generally MOSFET works in saturation region when it operating in analog applications. In the figure observed that in saturation region the value of capacitance for LNUCD Re-SOI MOSFETs is further decreased so that the frequency response of device will improve.

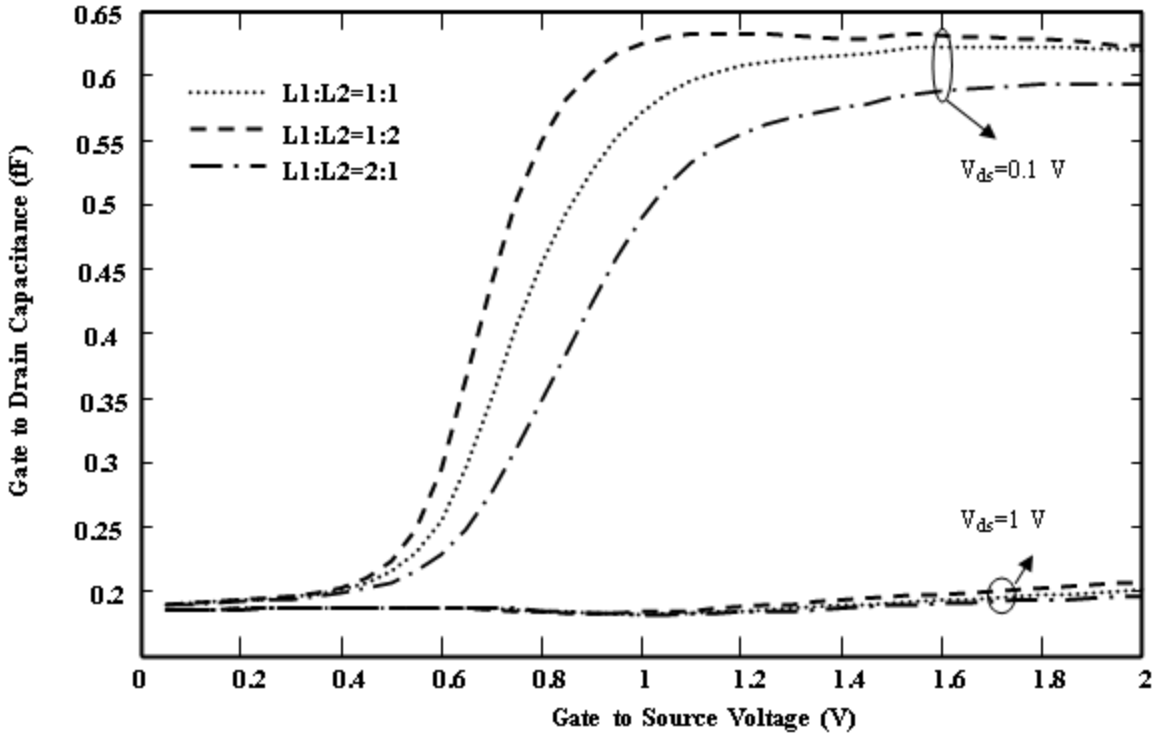

Fig. 18 Gate to drain capacitance versus gate to source voltage for different V_{DS}, , φ_M = 4.8eV, N_{a1} = 4*10^{18}cm^{-3}, N_{a2} = 10^{15}cm^{-3}, N_d =10^{20}cm^{-3}, t_{si} = 8nm, t_{ox} = 2nm and t_{box} = 200nm

Fig.18 shows the dependence of gate to- drain capacitance (C_{gd}) on gate-to-source voltage for two different drain to source voltages (V_{ds} = 0.1V and 1.0V). It is noticed that the gate-to-drain capacitance of all the considered structures is nearly equal in both sub-threshold and saturation regions at higher values of V_{ds}, whereas small values of V_{ds} gate-to-drain capacitance is equal in sub-threshold region but differing in saturation region for all considered structures. To get good frequency response device capacitance should be less, from above figure we can observe that structure Lateral non-uniform channel doping Re-SOI MOSFET (L1:L2=2:1) offers minimum capacitance which results in good frequency response

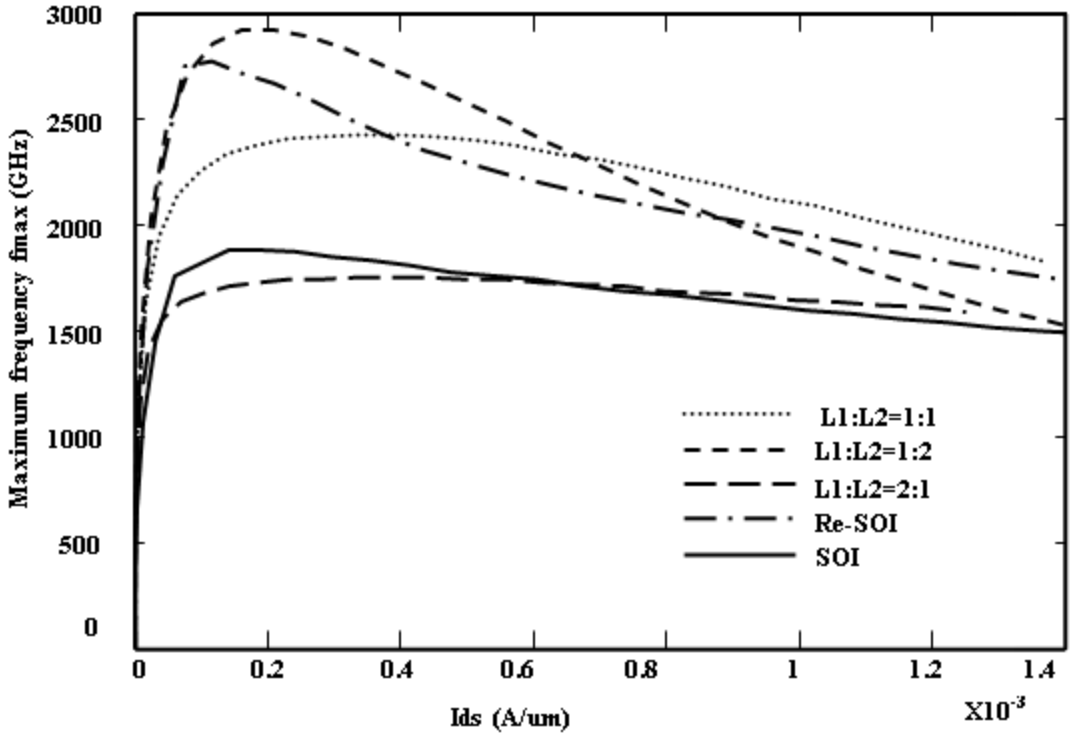

Fig. 19 Maximum frequency versus respective Drain current voltage for all the considered structures at V_{DS}=1v, φ_M =4.8eV, N_{a1}=4*10^{18} cm^{-3}, N_{a2} =10^{15} cm^{-3}, N_d =10^{20} cm^{-3}, t_{si} =8nm, t_{ox}=2nm and t_{box} =200nm

Fig.19 depicts the comparison of Maximum Frequency of Oscillation of all considered structures with change in respective drain currents, among all the considered Structures, Lateral non-uniform channel doping Re-SOI MOSFETs improves the Maximum frequency of Oscillation. Particularly the Re-SOI MOSFET structure with Lateral non-uniform channel doping (L1:L2=1:2) gives F_{max} almost double to F_{max} of SOI MOSFET at V_{gs}=0.95 v. Also we can observed that over the range of Drain current structure (L1:L2=1:2) gives constant F_{max} which shows stability of the device.

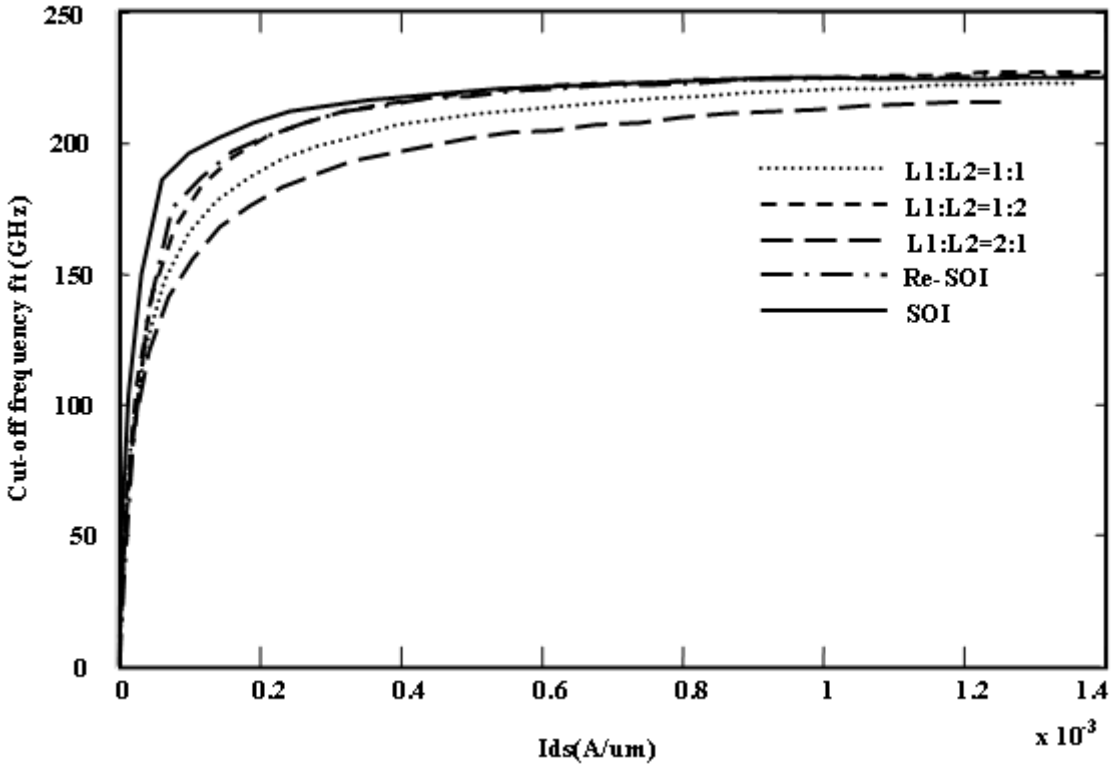

Fig. 20 Cut off frequency versus respective Drain current for all the considered structures at V_{DS}=1V, φ_M = 4.8eV, N_{a1} = 4*10^{18}cm^{-3}, N_{a2} = 10^{15}cm^{-3}, N_d =10^{20}cm^{-3}, t_{si} = 8nm, t_{ox} = 2nm and t_{box} = 200nm

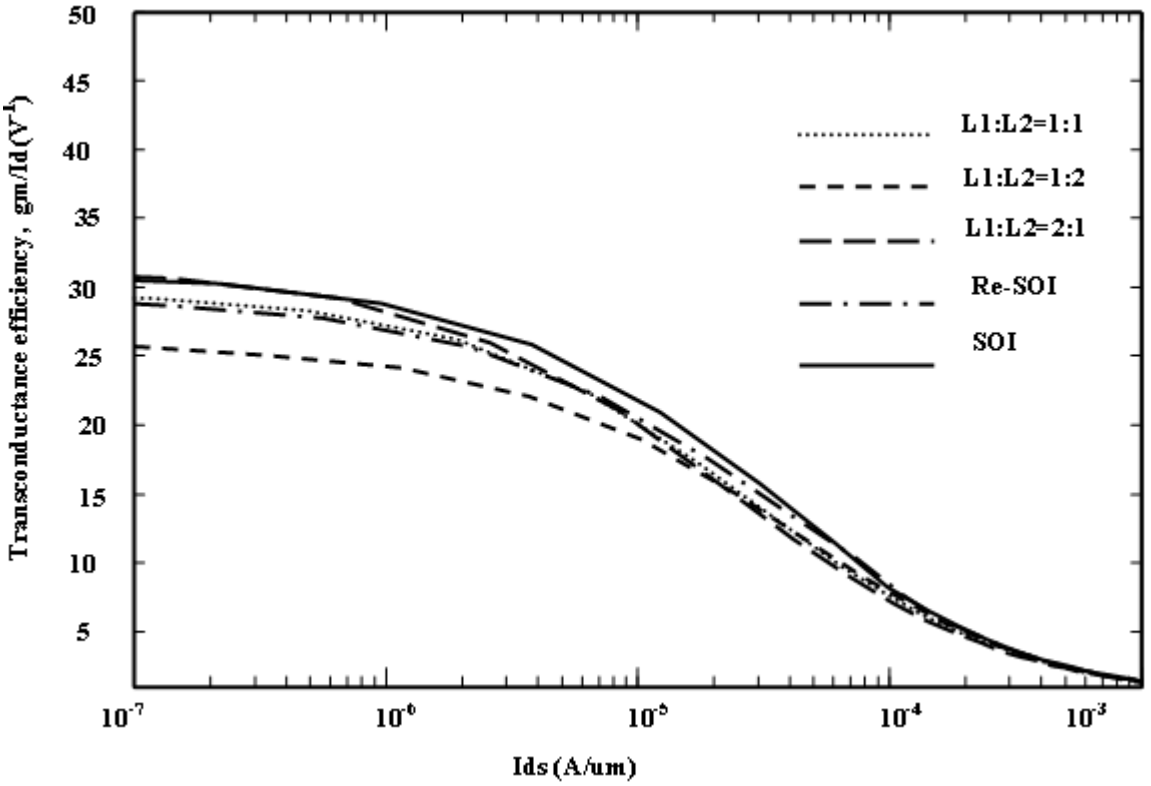

Fig. 21 Transconductance efficiency versus respective Drain currents for all the considered structures at V_{DS}=1V, φ_M = 4.8eV, N_{a1} = 4*10^{18}cm^{-3}, N_{a2} = 10^{15}cm^{-3}, N_d =10^{20}cm^{-3}, t_{si} = 8nm, t_{ox} = 2nm and t_{box} = 200nm

Fig. 20 depicts the comparison of Cut-off Frequency of all considered structures with change in respective drain currents. From all the considered Structures, Lateral non-uniform channel doping Re-SOI MOSFETs (structure L1:L2=1:2) gives the Maximum frequency of Oscillation.

5.3 CONCLUSIONS:

In this project work, Analog and RF parameters for Recessed Fully-depleted SOI MOSFET with non-uniform lateral doping in channel region are plotted. Asymmetric doping in channel region increases the threshold voltage. It is seen that due to higher threshold voltage, sub-threshold current decreases which gives the advantage of lowering the leakage power in sub-threshold region when compared to Re-SOI and SOI MOSFETs. It is also observed that the RF parameter Maximum frequency of oscillations improved drastically by 1000 Giga-hertz while comparing with conventional MOSFET at particular gate voltage. Finally the results explained in chapter 4 are obtained from the commercially available device simulator software ATLAS, by Silvaco Inc.

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