Atlas based simulation study of junctionless double gate (DG) tunnel FET

A dissertation submitted in partial fulfilment of

the requirement for the degree of

Masters of Technology in

VLSI and Embedded Systems

by

Silpeeka Medhi (212EC2139)

to the

Department of Electronics and Communication Engineering
National Institute of Technology Rourkela

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June 2014

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COMMUNICATION ENGINEERING
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ODISHA, INDIA-769008

CERTIFICATE

This is to certify that the thesis report entitled "**ATLAS based simulation study of junctionless double-gate(DG) tunnel FETs**", submitted by **Silpeeka Medhi**, bearing **roll no. 212EC2139** in partial fulfilment of the requirements for the award of **Master of Technology in Electronics and Communication Engineering** with specialization in "**VLSI Design and Embedded Systems**" during session 2012-2014 at National Institute of Technology, Rourkela is an authentic work carried out by her under my supervision and guidance.

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other university/institute for the award of any Degree or Diploma.

Place: Rourkela

Date: 20th May, 2014

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ABSTRACT

Tunnel Field Effect Transistor has recently attracted the attention of many researchers through its high Ion/Ioff ratio and a very less subthreshold slope. In this work Junction-less double gate tunnel field effect transistor's performance has been studied which has been designed using charge plasma concept which can form the source and drain regions without the need for any doping by choosing appropriate work functions for the source and drain metal electrodes. A very important parameter of this device has been studied, i.e. the threshold voltage of this device. It has been seen that the variation of the threshold voltage with respect to the varying channel length of the device in almost nil. Also using it has been found that this device has a subthreshold slope of 56.7mV/decade with channel length of 50nm which is much lesser compared to the 60mV/decade subthreshold slope of a MOSFET, proving that this device can be used for switching performance in the future. Though the performance of the junction-less double gate TFET does not vary much compared to doped double gate Tunnel Field Effect Transistor, it is expected to be removed from all problems associated with random dopant fluctuations. Also its fabricating is possible on single crystal silicon-on-glass substrates which is formed by wafer scale epitaxial transfer

Keyword: charge plasma concept, fabrication, dopants, metal electrode, work function, subthreshold slope, fabrication

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Chapter 1
INTRODUCTION

1.1: MOSFET

A important transistor used in the amplification or switching of electronic signals is the MOSFET, MOS FET, or MOS-FET (metal–oxide–semiconductor field-effect transistor). Though the number of terminals in a the MOSFET are counted as three, drain(D), source(S) and the gate (G), it actually has another fourth-terminal, the body (B). This terminal is usually not taken into consideration as it is joined with the source terminal, making it a 3-terminal device just like the rest of the field-effect transistors.[1] As both the terminals are normally short-circuited internally, the electrical diagrams will always show only three terminals. The bipolar junction transistor, which at one time was very common has been now replaced by the MOSFET in both analog and digital circuits.

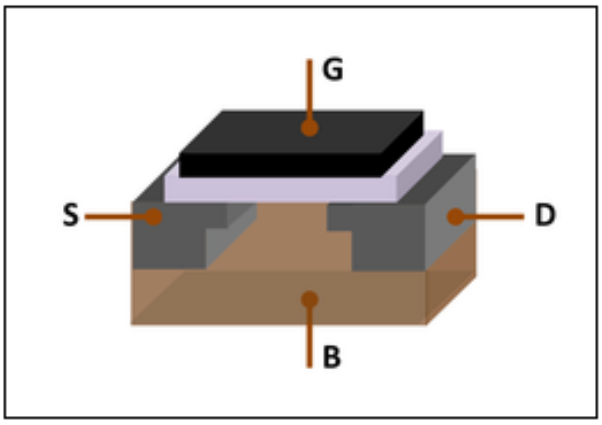

Figure1.1.1. MOSFET showing its 4 terminals drain (D), body (B),gate (G) and source (S)[2]

Figure 1.1.1 shows MOSFET with its four terminals gate (G), body (B), source (S) and drain (D). An insulating layer (white) separates the gate from the body.

When MOSFET is in the enhancement mode, a conducting channel is induced between the drain and source contacts via the field effect due to the voltage drop across the oxide. Enhancement mode means the increase of conductivity along with the oxide field increase. This increase always leads to that addition of carriers to the channel, which can be also termed as the inversion layer. This channel can consist of either the electrons (called an nMOSFET or nMOS), or holes (called a pMOSFET or pMOS). They are always opposite to the substrate type, means pMOS is made with an n-type substrate and nMOS with a p-type substrate. [3]

1.2: Limitations of MOSFET

But the problem with conventional MOSFET is that when IDS-VGS is plotted on a log-lin scale, their subthreshold slope remains fixed. This means that after optimizing the device fully to have the maximum possible sudden transition turn-on with gate voltage and when the subthreshold swing at room temperature reaches its maximum value of 60mV/decade, then further lessening of the threshold voltage is only possible with the shifting of Ids-Vgs characteristics. Shifting of the threshold voltage Vt by 60mV means increasing of the off current by one decade which will result in the increase of the static power.

Figure 1.2.1 shows A typical I_{DS}-V_{GS} curve for a highly-optimized conventional MOSFET, showing the subthreshold swing limited to 60 mV/decade at room temperature. To decrease VT by shifting the curve left, a price in leakage current has to be paid. Solid curve's data is from an optimized asymmetrical double-gate conventional MOSFET in [3], which is then shifted three times. Such a shift could come from engineering the gate work function, for example.

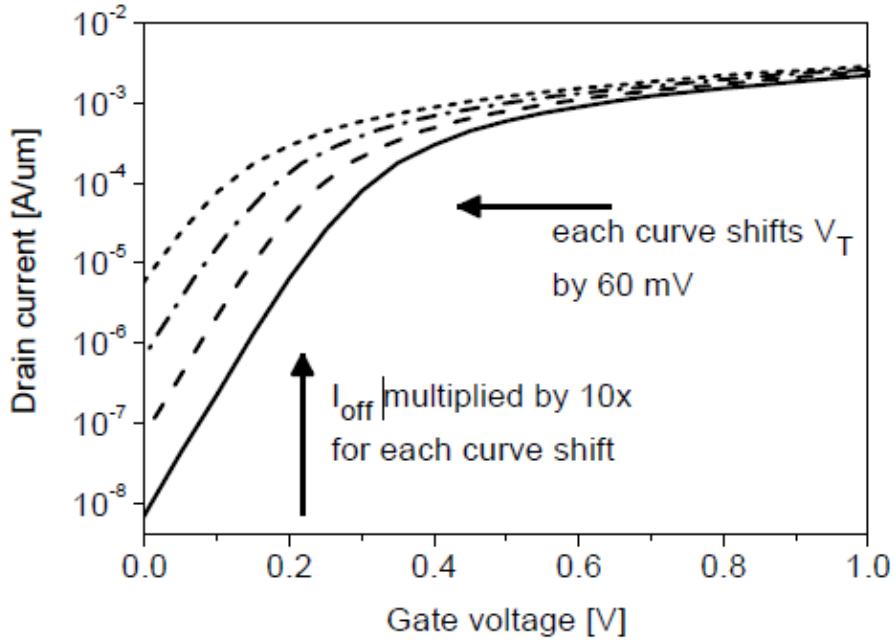

Figure 1.2.1: A typical I_{DS}-V_{GS} curve for a highly-optimized conventional MOSFET[4]

1.3: Scaling

A prominent role in integrated circuits (ICs) is being played by the MOSFET (Metal Oxide Semiconductor Field Effect Transistor) because of their scalability ability. With the advancement in technology, researchers are trying to minimize almost every semiconductor devices. During the past few years, the MOSFET which once had the channel lengths of several micrometres has continually been scaled down to tens of nanometers in the modern integrated circuits.

As calculated by Moore's law [6], shown in the following figure, the dimensions of the MOS transistor have been dwindling since 1960 by 30% per 3 years. Though only increasing rate of the density of the transistor is illustrated by Moore's law, but the diminution of the dimensions of the MOS device has some positive points also like improvement in the density and speed of the circuit by the following mentioned ways:

a) Declination of the length of gate(L_G) increases the operational frequency of the circuit which leads to a faster circuit
b) The area of the chip decreases allowing a better density of the transistor along with reducing the cost of the ICs
c) The constant switching power density enables lesser power for each function else number of circuits during the same power.

Fig 1.3.1 shows the Moore's law of scaling. It can be seen clearly that with the passing years the transistors count on a single chip is also increasing simultaneously.

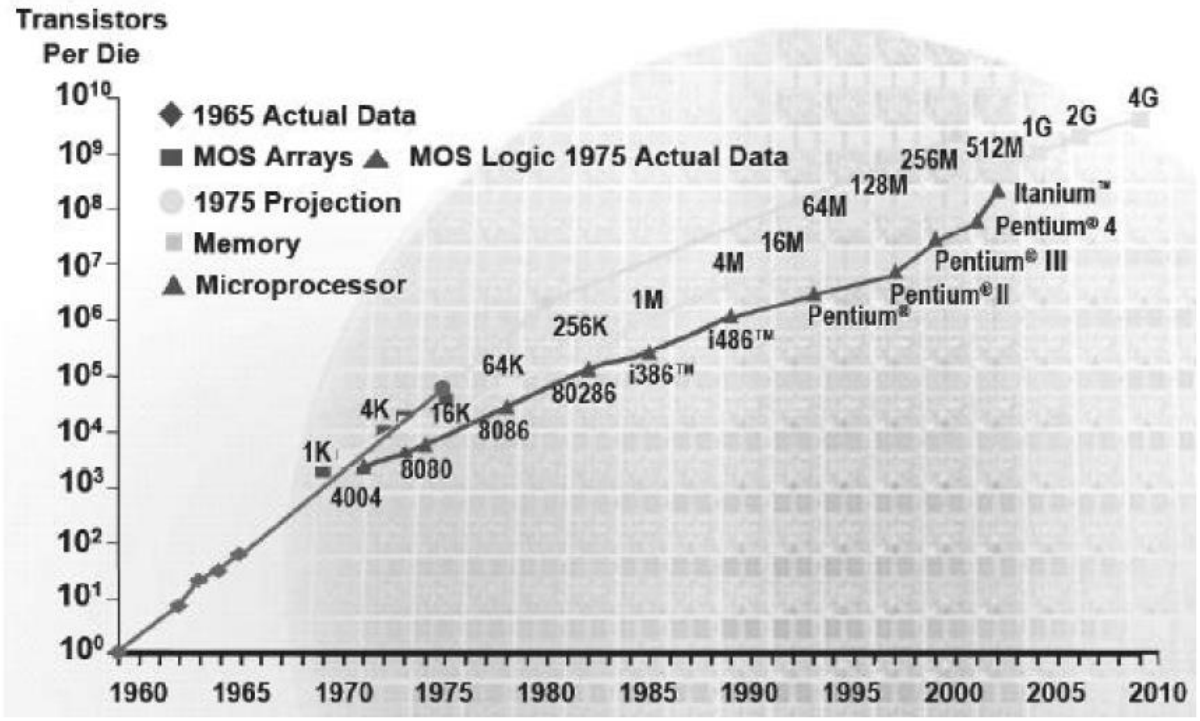

Figure 1.3.1: Moore's law of scaling. [5]

CMOS technology offer a basic advantage by the definite scaling laws. A roadmap has been laid by the International Technology Roadmap for Semiconductor (ITRS) for directing the scaling with respect to cost incurred and power consumption. According to the ITRS 2010 (Figure. 1.3.2), the year 2013 whose technology node is 22nm should have physical channel extent of 10nm and less. This has been made possible by the device engineers throughout the world due to Scaling, which is the modification of the device dimensions in a controlled manner so that it chip area occupied by it decreases without effecting the performance characteristic of the long channel. The scaling approach was proposed by d. Dennarad and his fellow workers in 1972 [7]. Through Scaling along with the reduction of the dimensions of the device which leads to more packing density, it also saves the dynamic power through reduction of the voltages. As the scaling advancing, it shows that the scaling of both the vertical and lateral aspect of the transistor should be by the same factor so as to avoid the SCEs and provide good electrostatic control during the fabrication of the smaller devices. Also the supply voltage can be reduced with the increase in substrate doping concentration, by the same scaling factor.

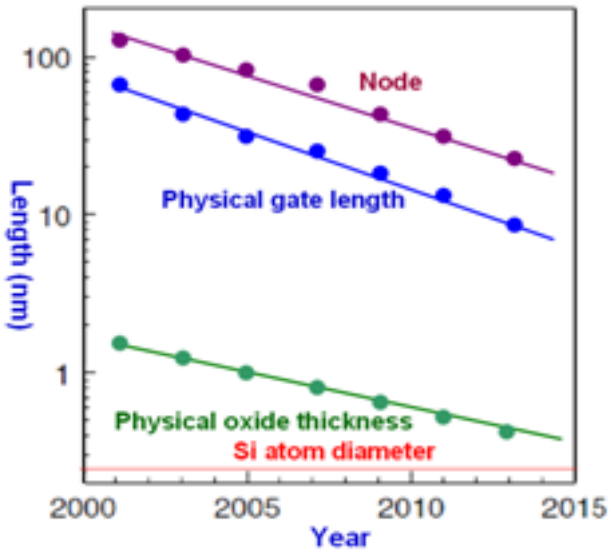

Fig. 1.3.2:. Shrinking gate length with of scaling. years (Courtesy: ITRS 2010)

The rules of scaling in MOSFET as stated by Dennard et al. in 1974 says that all the dimensions of the device, which includes the supply voltages also, are declined by the same factor [6]. It has been seen from the last many years that Scaling, i.e. reduction of physical dimensions of the transistor structure, has always improved the performance of the devices and also its density. The main factor of Scaling is to decrease the Gate length (L_G) and also to decrease the effective oxide thickness which eventually will increase the Cox , so as to increase I_{ON}. Apart from increasing the I_{ON}, scaling also leads to increase of the circuit speed and decrease of the power consumption and area occupied by the circuit [7]. Hence, the circuit's power density remains unchanged.

The decrease in the dimension of the MOSFET have difficulty allied with the process of fabrication of the semiconductor device, the requirement of utilizing very low voltages, and with poorer electrical performance necessitating circuit redesign and innovation. Scaling of MOSFET also leads to varoius short channel effects (SCEs) like drain induced barrier lowering (DIBL), punch through, high leakage currents, quantum tunneling through gate, impact ionization etc.. All these phenomena degrade the performance of circuit. The short channel effect of scaled MOSFET cannot be avoided even with the optimization of properties of the materials used (e.g., peak doping concentration, strain engineering). The main disadvantage of the short channel effect is reduction in the control of the channel through the gate. Also the improvement in leakage current can lead to degradation of the characteristics of MOSFET.

With the present advancement in technology, it is very hard to tell by when will the reduction of the size will stop. Through this reduction, may be we'll be able to produce better materials to avoid any leakage. But at a particular point we need to find a replacement for MOSFET to contine the performance enhancement we are used to presently.

According to R. Dennard scaling of a MOSFET without changing the electric fields inside the device is possible only by scaling the device dimensions by $1/\kappa$, while increasing the doping of the drain and source regions by a factor of κ. Also the voltage applied should be scaled by a factor of $1/\kappa$. Researcher had followed these rules ever since 1974, until rather recently.

The Dennard's scaling rules can no longer be followed as before. The figure1.3.3 shows the trend of scaling from the 1.4 μm node to the 65 nm node. It can be seen that though there has been a deacrese in the supply voltage V_{DD} by about 20% of its initial value, the reduction in the threshold voltage V_T is very less. This has happened only due to Dennard scaling. This had come in some other ways, like changing the doping of the channel region under the gate. On following the rules of scaling properly, there is no change in the electric fields inside a MOSFET. Hence there is no change in the threshold voltage also, unless we make some other changes are.

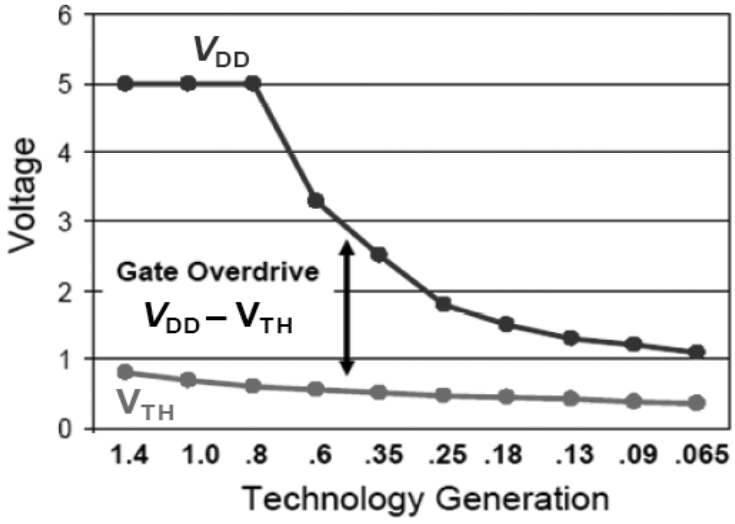

Fig 1.3.3: The trend of threshold voltage and supply voltage scaling vs. technology generation. V_{DD} decreases with device dimensions, but V_T does not.[8]

1.4: Small swing devices

After many researches, it has been seen that to tackle the problems faced by the conventional MOSFET, it is better to replace the device with some new devices instead of finding solutions in the circuit design of the same. And best way to solve the problems would be to design conventional MOSFET which will have a subthreshold swing lesser then 60mV/ decade at room temperature.

Many new ideas have been studied as that to reduce subthreshold swing to less than the

60mV/decade at room temperature. Here two such of devices will be explained which have been experimentally verified. They are IMOS and MEMS/NEMS switches.

1.4.1. IMOS:

Figure 1.4.1(a) shows IMOS. IMOS which is a gated p-i-n junction main purpose is to move into avalanche breakdown. Hence when the device is on its gate is offset from one of the junctions which leads to formation of a very high electric field in the non-gated portion of the i-region [9].

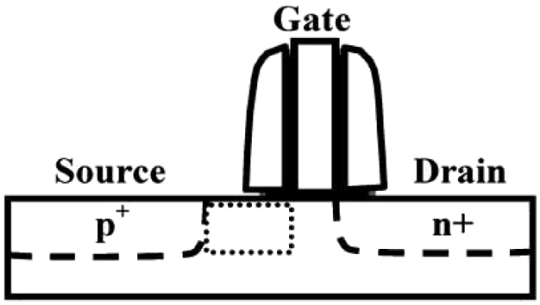

Figure 1.4.1(a): A typical IMOS structure, in which a p-i-n diode is partially gated, with part of the intrinsic region left uncovered[10]

It has been seen from the experimental transfer characteristics of IMOS (impact ionization process) that it can very small subthreshold swing along with high on-current [11]. From the following figure1.4.1 (b) which shows the transfer characteristics of IMOS, it can be studied that, its subthreshold swing is about 4mv/decade for n-channel devices and about 9mV/decade for p-channel devices.

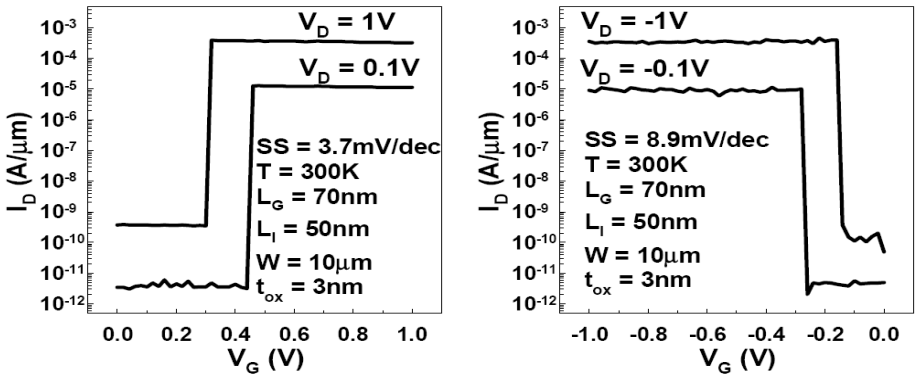

Figure.1.4.1(b) Measured IMOS I_{DS}-V_{GS} characteristics for nchannel (left) and p-channel (right) devices, from [10], where the source was biased at -5.5 V.

The main problems with IMOS include scalability, since there must always be a gated and an ungated region between the source and drain, hot carrier degradation, since impact ionization necessarily creates hot carriers and these can go into the gate oxide, and the difficulty of low-voltage operation, since high voltages are required in order to induce breakdown.

Though IMOS give lesser subthreshold swing, there are many problems faced by it. As it requires both gated and ungated region of intrinsic between the source and the drain for its formation, it faces the problem of scalability. Another problem of IMOS is that of hot carrier degradation. Hot carriers, which are created due to impact ionization can always go into the gate oxide. The next problem is regarding its operation. It requires high voltage for its operation so as to induce breakdown.

1.4.2:MEMS/NEMS

The next small swing switch is the electro-mechanical relay which can be either on the NEMS i.e. nanometer scale or on the MEMS i.e. micron scale. NEMS switches can be divide into either two-terminal devices or the three-terminal devices. Though the two-terminal devices may have very low swing values [12], but they lack in terms of circuit applications. Hence the conventional MOSFETs can be replaced by the three-terminal devices. This type of switches can have many possible designs. Two of the designs are explained below.

One of the design involves the fabrication of a flexible cantilever beam which is electrically connected to source terminal (figure 1.4.2(a)). This beam is activated by a gate electrode which is present underneath and then it is being down so that it touches the drain electrode during the on-state.

The next design uses a typical MOSFET layout, with drain, channel, and source, as in the two devices shown in Figure. 2.11

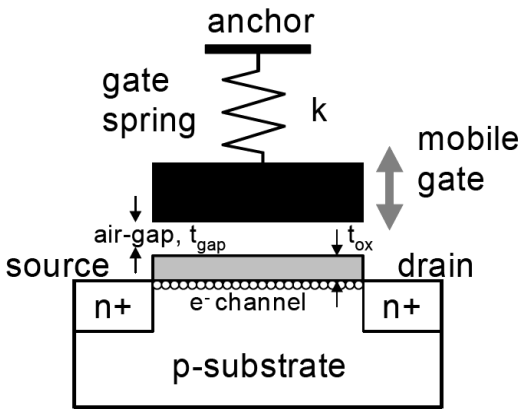

Figure 1.4.2.1(a)

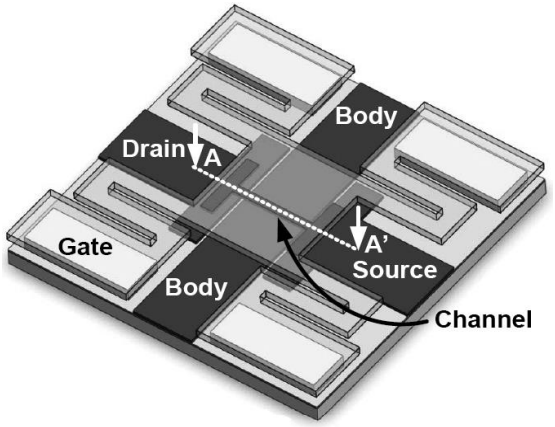

Figure.1.4.2.1(b)

Figure 1.4.2.1: Two possible designs for MOSFET-like MEMS relays, with a source, drain, and gate[13].

Another possibility is to use a more typical MOSFET layout, with source, channel, and drain, as in the two devices shown in Fig. 1.4.2.1. The first design (Figure 1.4.2.1(a)), has a gap filled with

air in between the gate contact and the gate dielectric. The gate of this design moves up and down itself during off-state and on-state respectively.

The second (Figure 1.4.2.1(b)) consist of the drain and source regions on the substrate. This design consist of a gate/channel which can be moved i.e. it can be pulled down into contact with the drain and source when it is in the on-state.

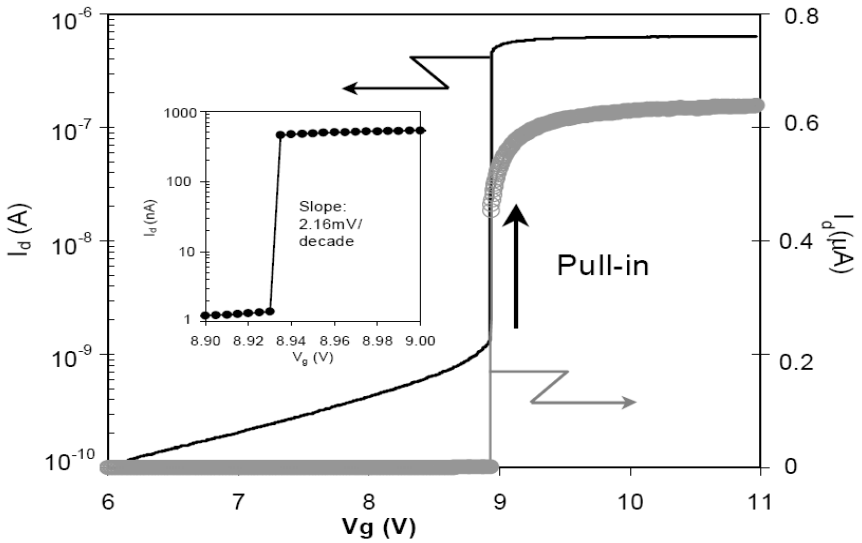

Figure 1.4.2.2(a)

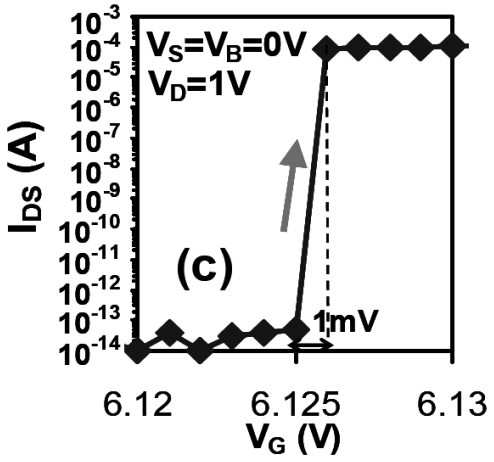

Figure 1.4.2.2(b)

Figure 1.4.2.2: Measured I_{DS}-V_{GS} characteristics for the MEMS switches demonstrating extremely small subthreshold swings[13,14].

The swing in this type of device is set by the voltage step size, has no fundamental limit, and can approach zero. (a) Junction leakage is still present for this relay design (b) Off-state current is much lower for a design in which the source and/or drain is physically separated from the MOSFET channel

These switches can be used in place of the conventional MOSFET because of their benefits like very low off currents along with high ON currents, and small subthreshold swings. But they also faces a few disadvantages like lower speed and due to their mechanical nature they also have to face the problem of reliability, like the structural damage caused when the two pieces need to touch each other and then come back apart for millions of times.

1.4.3: Tunnel FET

As already known, the present day chipmakers are trying their level best to squeeze more and more transistors onto a single chip. For doing that the transistors have to made much smaller which in lead to reduction in the distances between different regions of the transistor. As a result, the electronic barriers which once blocked the current due to its thickness have become so thin that now electron can use its ability to penetrate barrier, known as quantum tunneling, to barrel through them.

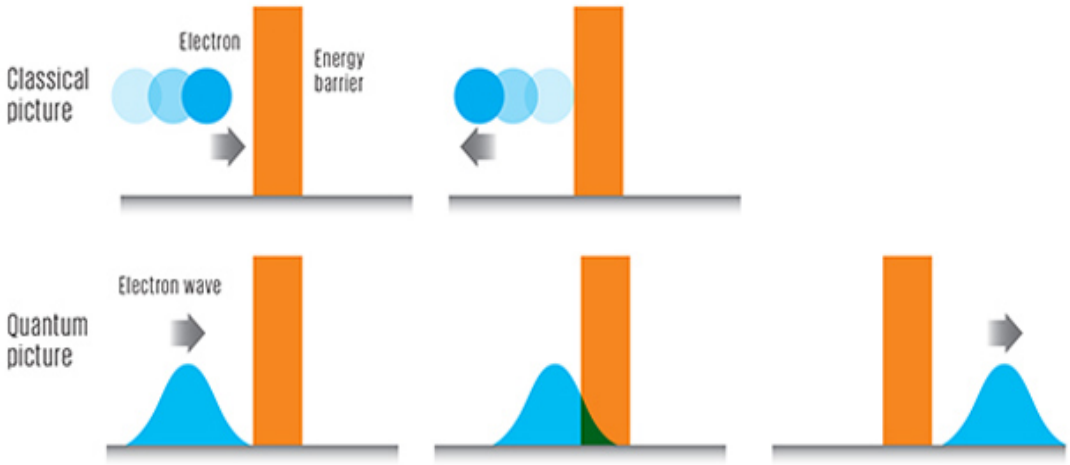

Fig.1.4.3.1: Classic and quantum picture of electron passing through the energy barrier

The above figure shows the passing of electron through the energy barrier in both classic and quantum electrodynamics. In classical electrodynamics, an electron [blue] cannot pass through the energy barrier [orange] until and unless its energy is more than the height of the barrier. Actually there is a finite probability of the electrons for passing through this barrier. For that the barrier should be very thin, such that tunneling event can take place, as shown for quantum electrodynamics.

This property of electrons to be able to tunnel through the thin barriers has been utilized as a pricniciple of operation in the band-to-band tunneling process. From the last few years, transistor using this principle, called as Tunnel Field Effect Transistor(TFET) have caught the attention of the researcher due to its have good sub-threshold swing, very low leakage current, lesser temperature sensitivity and improved short channel characteristics. Unlike the MOSFET, in which the flow of current is controlled by rising or lowering an energy barrier, TFET always keeps its energy barrier high.

Tunnel FET behaves like a ambipolar device. When it is dominant with hole conduction it starts bwhaving like p-type and as n-type when it is dominant with electron conduction. This device alters the probability of electrons materializing one side of the barrier from another side to switch it on or off. The tunneling of the electrons in tunnel field-effect transistor (tunnel FET) can lead to switching of the on and off state at lower voltages compared to the metal oxide semiconductor field effect transistor's (MOSFET) operational voltage. Thus it is able to reduce the power consumed by the electronic devices.

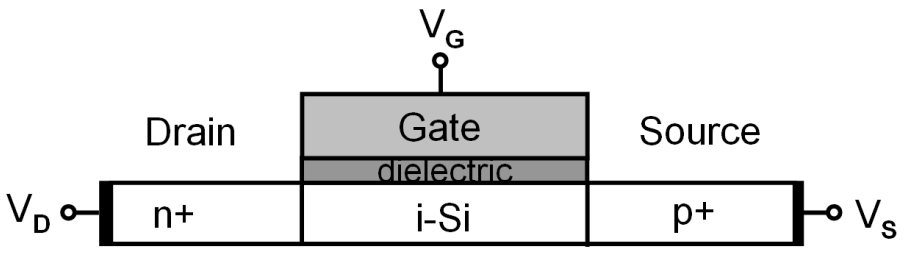

Figure 1.4.3.2: *A simple Tunnel FET device structure, an n-i-p diode with one gate.*

The following figure (figure.1.4.3.3.) shows the comparison between the transfer characteristics of MOSFET and Tunnel FET.

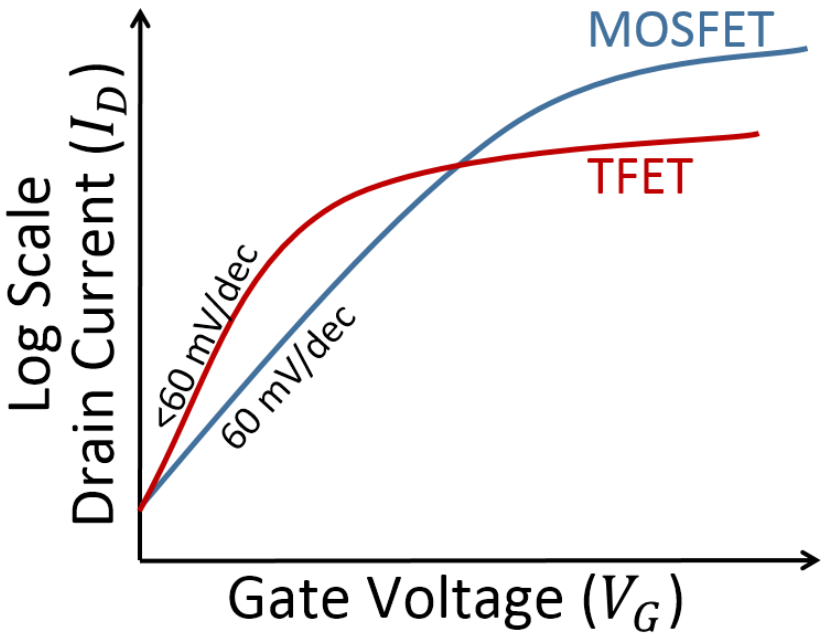

Fig.1.4.3.3: The transfer characteristics of MOSFET and Tunnel FET along with their subthreshold slope.

Tunnel Field effect transistors which are actually gated p-i-n diode, operates under the condition of reverse bias. Unlike MOSFET which uses the mechanism of thermal injection for source carrier injection, Tunnel FET uses the method of band-to-band tunneling for the same. For band-to-band tunneling to occur, an electron has to tunnel from the valence band of semiconductor to the conduction band without the assistance of traps. To allow the particle to tunnel across the band gap, it has to act as the potential barrier. Unlike in indirect tunneling, an electron doesnot require to emit or absorb photon for traveling from the valance band to the conduction band in direct tunneling. The process of direct tunneling in silicon like band gap materials which are indirect, is negligible. This is due to the rapid decrease in the transmission probability with increase in the barrier height. Tunneling in direct tunneling can be increased with the requirement for conservation of perpendicular momentum i.e. when tunnels from the valence band to the conduction band, its perpendicular momentum should not change.

A thick potential barrier between the channel and the source will not allow tunneling to take place for Tunnel FET which is in the OFF state. During this time only a very little amount of leakage current is present which is less than a fA/μm. But when the gate voltage becomes more then the threshold voltage, the Tunnel FET turns into ON state. During the ON state, the thick potential barrier becomes much slender so that a significant amount of current can tunnel.

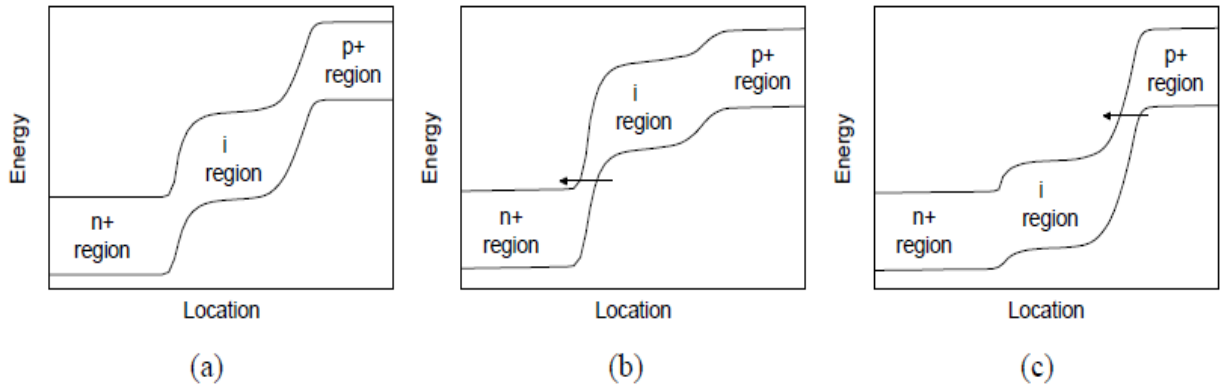

Fig 1.4.3.4: Energy band diagrams of a Tunnel FET captured horizontally across its body (a) the off-state of the transistor where the only current comes from p-i-n leakage, (b) the on-state with a negative bias on the gate leading to pFET-type behavior, and (c) the on-state with a positive bias on the gate leading to nFET-type behavior.

The above figure shows energy band diagram of tunnel FET for various states. Fig (a) shows the energy band of the Tunnel FET during its OFF state with no gate voltage but with a applied reverse bias over the p-i-n junction. Fig (b) shows the lifting of the energy band of the region of intrinsic on the application of negative voltage on the gate and reverse bias across the junction. As a result of the lifting of the energy band, the size of the energy barrier becomes small enough to allow tunneling between the conduction band of the n+-region and the valence band of the intrinsic region. Finally as shown in Fig (c) the energy bands in the same intrinsic region gets pushed down on applying positive gate voltage on the gate allowing band to band tunneling to take place.

But the current flowing through the tunnel FET is much smaller compared to the current flowing through the MOSFET. This leads to problems during tunnel FET's practical application. High threshold voltage is another problem faced by these transistors. A few techniques have been

studied to address these issues like high-k gate dielectric with double gate [15], higher source doping and abrupt doping profile, vertical tunnel field effect transistor (TFET) with SiGe delta doped layer, tunnel bandgap modulation). TFET can be used in a wide scale if its device parameters meet the ITRS guidelines. The structure of the device should be such that it can be incorporated in the existing process flow with not much modification.

1.5 Thesis Organization

After the introduction, these are the following chapters which are included in this thesis:

Chapter 2: This chapter is about the works done by the researchers related to this topic in the past.

Chapter 3: The method of simulation used in this project is explained in this particular chapter.

Chapter 4: This chapter gives the detail explaination about the structure of the device studied along with all its dimensions.

Chapter 5: All the characterestics of the studied device is explained in details in this chapter.

Chapter 6: The conclusion derived from this project is explained here along with the future scope of the same device.

Chapter 2
LITERATURE REVIEW

2.1: Double Gate Tunnel FET [15]

The structure of this device is a lateral n-type Tunnel FET in a thin silicon layer, which is isolated from the substrate by a dielectric layer. The basic design is a gated p-i-n diode. The tunneling in this device takes place between the intrinsic and p+ regions.

The parameters for designing this devices are explained here. The doping levels taken for this device is 1×10^{20}, 1×10^{17}, and 5^{18} atoms/cm3 for the source, intrinsic, and drain regions, respectively along with thickness of silicon film(Tsi) = 10nm and gate oxide (Tox) = 3nm and length of channel (L) = 50 nm. Doping has been optimized in order to create the maximum ON-current, and a low OFF-current .It is desirable to have a high source doping (around 10^{20} atoms/cm3 or even higher) but a lower drain doping. The work function chosen for the gate contact is 4.5 eV, corresponding to a metal gate stack. This could correspond to a stack comprised of tungsten (W) and titanium nitride (TiN).

The schematics diagram of this devices is shown in Fig. 1. This device operates in reverse biased. For simulating it, the source is grounded, and a positive voltage is applied to the drain and a voltage is applied to the gate(s), the n-region is referred to as the drain and the p+ region as the source. When the gate voltage is zero, the width of the energy barrier between the intrinsic region and the p+ region is wider than 10 nm (the minimum for allowing the process of tunneling), and hence the device is in the OFF-state. But with the increase in the positive gate voltage, the bands in the intrinsic region are pushed down in energy, narrowing the tunneling barrier and allowing tunneling current to flow.

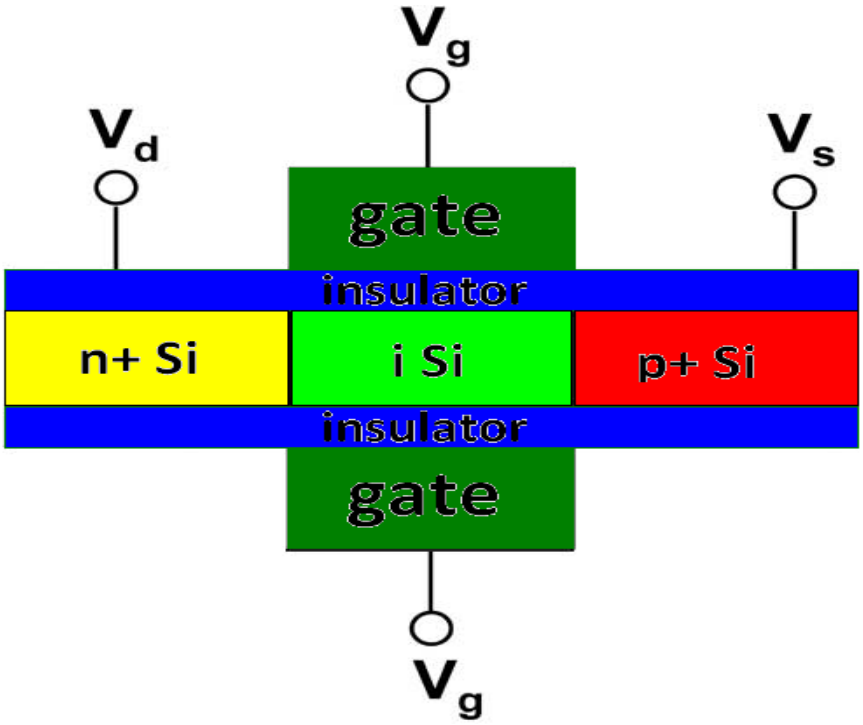

Figure2.1.1: The structure of double gate tunnel FET with an intrinsic length of 59nm, dielectric thickness of 3nm

The simulation results of this structure showed a higher Ion keeping the Ioff very less along with an improved subthreshold.

2.2: Junctionless Tunnel Field Effect Transistor[16]

Bahniman Ghosh et al. proposed and examined a new TFET structure (namely JLTFET), which gives the advantages of both JLFET and TFETcombined together. Fig. 2 shows the proposed double-gate junctionless tunnel field effect transistor (JL-TFET) structure along with the lengths and thicknesses of different layers used in simulation. The simulated JL-TFET is a Si-channel heavily n-type-doped (1 × 1019 cm−3) JLFET with a 20-nm channel length, source/drain extension length of 20 nm, silicon film thickness of 5 nm, 2-nm gate oxide thickness, and 5 nm of isolation in between Control-Gate (CG) and P-Gate (PG), which works as an isolation

between the gates and also as a spacer. The double-gate technology is used to provide better controllability over the channel.

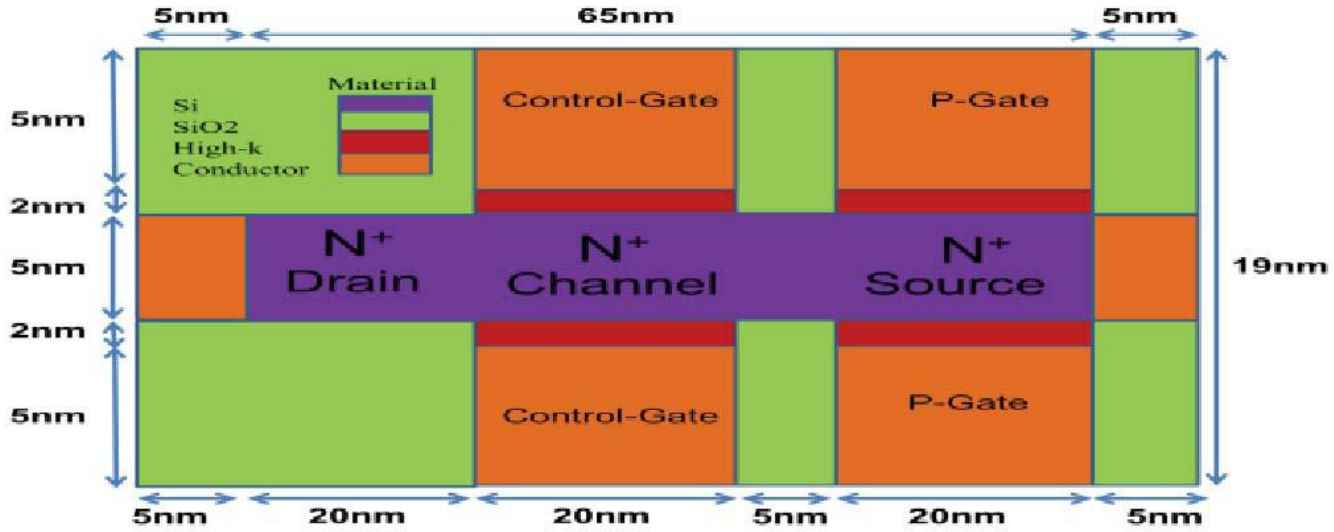

Figure 2.2.1 : Schematical representation of the JL-TFET.

The above explained device structure exhibits excellent ON–OFF characteristics based on the simulations. It seems to be a very promising device for sub-22-nm nodes.

2.3: Dual Material Gate Tunnel Field Effect Transistors [17]

A new two dimensional (2D) analytical model of a Dual Material Gate tunnel field effect transistor (DMG TFET) was presented by T.S.Arun Samuel et al in 2013(7). The cross section view of a Dual Material Gate TFET is shown in Fig. 3. The source and drain is made of highly doped p-type and n-type regions respectively. The intermediate channel region is made of a moderately doped n-type layer. Silicon-di-oxide (SiO2) is used as the gate dielectric. The gate consists of two materials M1 and M2 with gate lengths L1 and L2 with two different work function $m1\ \varphi$ and $m2\ \varphi$. Based on the positive or negative potential applied to the gate terminal, the device behaves as n type TFET and p type TFET respectively. If a positive gate voltage is

applied, the transistor behaves as a n-TFET and a negative gate voltage is applied, the transistor behaves as a p-TFET.

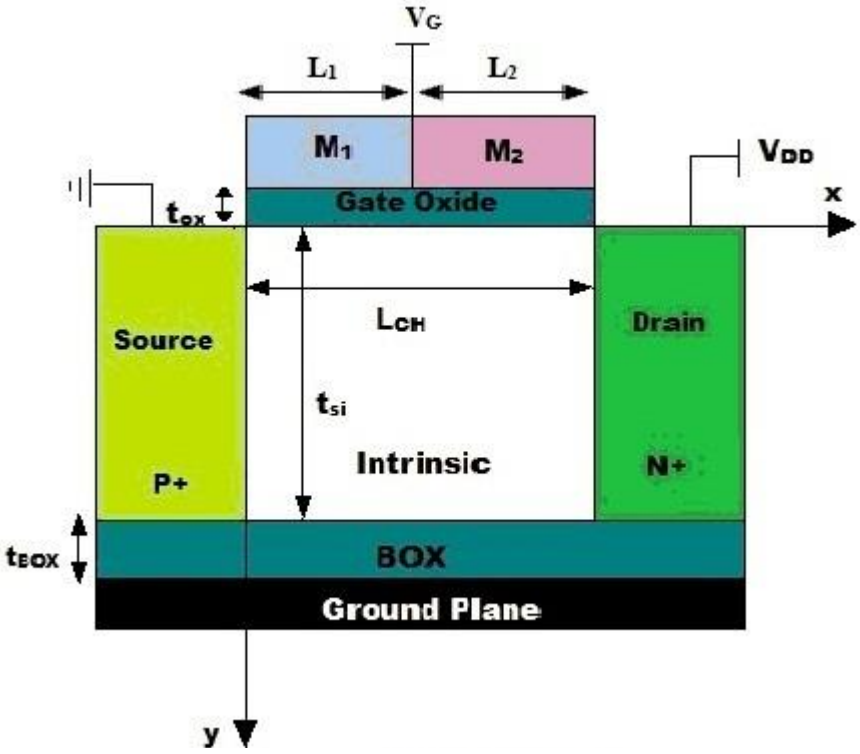

Figure 2.3.1:Schematic diagram of a DMG TFET

From the simulated results, it was concluded that the DMG structure provides wide range of benefits to the TFET performance. It has been analyzed that excellent immunity against SCE is offered by the DMG structure while decreasing channel length.

2.4: PAST work

Significant research was done on Dual Gate Material in a Double Gate Tunnel FET (DMG-DGTFET) by Sneh Saurabh et al, in 2011. Studies showed that varying work function of the gate materials in DMG-DGTFET influences the threshold voltage as well as leakage current in the device due to the variation in the energy barrier at the tunnel junction. Also comparisons were

done between Dual Material Gate and Single Material Gate DGTFET regarding their electrical characteristics as well as short channel effects like DIBL. [18]

In the past work, DGFETs and hetero-gate-dielectric tunneling field-effect transistors (HG TFETs) Radio frequency (RF) performances was analysed by K.Sivasankaran et al in 2012 and In Man Kang et al in2011 respectively.[19]

New models were developed by Koichi Fukuda et al. in 2012 which can be used for the TFETs development as physics-based practical tools. These models were based on band to band tunneling which are nonlocal. [20]

The linearity and analog performance of a Silicon Double Gate Tunnel Field Effect Transistor (DG-TFET) was investigated and the impact of elevated temperature on the device performance degradation had been studied by Rakhi Narang et al in 2011. The impact on the device performance due to the rise in temperature and a gate stack (GS) architecture had also been investigated for the case of Silicon DG-MOSFET and a comparison with DGTFET was made. The parameters governing the analog performance and linearity were also studied.[21]

M. Jagadesh Kumar et al. in 2013 reported a detailed study of the doping-less tunnel field effect transistor (TFET) on a thin intrinsic silicon film using charge plasma concept. Without the need for any doping, the source and drain regions are formed using the charge plasma concept by choosing appropriate work functions for the source and drain metal electrode.[22]

Chapter 3
METHOD OF SIMULATION

3.1: Introduction

Atlas is a software provides general potentials for physically-based two and three-dimensional (2D, 3D) simulation of semiconductor devices. Atlas is designed in such a way that it can be used with the VWF Interactive Tools. The VWF (Virtual Wafer Fabrication) Interactive Tools consist of the following: MaskViews, Optimizer, DeckBuild, TonyPlot, and DevEdit. Their functions are explained below:

- DeckBuild puts forward the condition for runing Atlas command language.
- Crafting a device structure and specifying the meshes used in it require a cooperative surrounding which is made available by DevEdit.
- Optimization across various simulators can be provided by Optimizer.
- IC layout correction is done by MaskViews.
- Through TonyPlot the outputs which are actually the electrical characteristics of the device and the structure files generated for the designed device can be seen.

Through these VWF Tools simulation results can be closely related to advancement of technology and also reflects that the research of the devices was done experimentally. Hence for the approaching semiconductor technology, these tools can prove to be very beneficial. It is also very useful for prediction of all the characteristics and features of the new devices and processes of technology.

Along with Atlas, there exists another process simulator, Athena. It can produce structures prepared by many processing steps. The same structures can be utilized by Atlas as inputs. Later Atlas predicts the different electrical characteristics related to the designed device. Now the

outputs of the Atlas can be given as the used as the inputs to the SPICE modeling software and Utmost device characterization.

Atlas can also be called as a physically-based simulator for devices as it is capable of calculating all the characteristics associated with a particular device with specified structure and voltage biases at the electrodes. The whole device area is divided by these simulators with grids called ‘meshes’ and with mesh points called ‘nodes’. By applying differential equations which are derived from Maxwell’s laws, current conduction and electrical parameters at each location through the structure is determined. This type of physically based simulation has many advantages like, they provide a deep insight of the attributes of a device without experimentally creating the device, calculation of very complex parameters are done very easily and quickly, estimation of the trends with the varying properties of the device according to its different bias conditions can be estimated through these simulations.

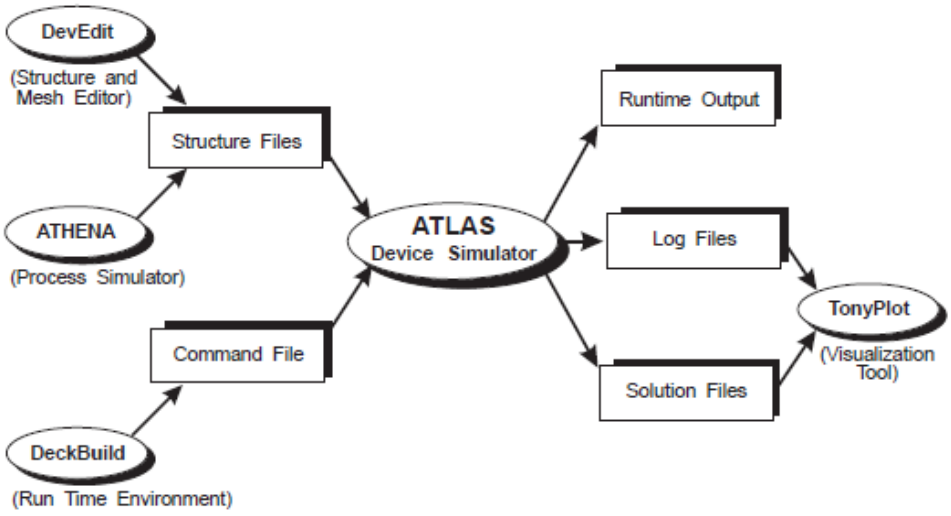

Figure.3.1: Inputs and Outputs of Atlas device simulator.

Informations flowing through Atlas device simulator can be seen in the above diagram (Figure3.1). The text file, which contains Atlas command language and structure file, which has the structure on which simulations has to be performed are the two input files to Atlas device

simulator. Atlas has three types of output files: runtime output which gives the information being processed at every instant of execution of Atlas commands and simultaneously show the errors and warnings, log files which gives all the electrical characteristics which is specified in the Atlas command language and solution files which has the 2D or 3D data of the device parameters at each and every point in the device.

3.2: Steps used for defining a structure

1. Loading structure from Athena

Atlas and Athena are interfaced for loading a structure which is described and generated by Athena. Hence, initially a structure is created and saved in Athena while it still is active. The command used for storing the device structure is:

`STRUCTURE OUTF= <structure name.str>` where *structure name* is the file

Then to load the structure saved above, in Atlas the following command can be used:

`MESH INF=<structure name.str>`

2. Loading a structure from DevEdit

Just like the previous step, for loading a structure into Atlas created by DevEdit both the tools need to be interfaced with each other. The syntax for this operation is as below.

`MESH INF=<structure name.str>`

The above command helps in loading meshes, the location of electrodes, doping of the device etc from DevEdit for the loaded device.

3. Using ATLAS Commands to define a structure.

A set of commands are used in a specified order for defining a structure using ATLAS . These commands are listed below.

The first step is to provide the mesh specification.

Mesh specification starts with a mesh mult statement which multiplies the spacing between the meshes by a factor (specified along with mesh. mult command) so that meshes can be finer or coarser according to the need.

Syntax:

```
MESH SPACE.MULT=<value>
```

After this x.mesh and y.mesh statements are specified as follows

```
X.MESH LOC=<value1>SPAC =<value2>
```

```
Y.MESH LOC=<value3>SPAC=<value4>
```

where '*value1*' and '*value3*' specifies the location of vertical and horizontal mesh line in microns respectively and '*value2*' and '*value4*' specifies the spacing between these mesh lines.

Next division of the device structure into different regions takes place. Different regions consist of different materials with a specific doping profile. For specifying the region the following command is used:

```
REGION
NUMBER=<value>X.MIN=<value1>X.MAX=<value2>Y.MIN<value3>Y.MAX=<va
lue4>MATERIAL=<material1>
```

The region number is specified by '*value*' and '*value1*' to '*value2*' gives the range of the region on the x-axis while '*value3*' to '*value4*' on y-axis. '*material1*' is the material forming the region (like Silicon, SiO_2 etc).

Subsequently electrodes need to be specified. This is done by the following command.

```
ELECTRODE
NAME<electrode1>NUMBER=<value>X.MIN=<value1>X.MAX=<value2>Y.MIN<
value3>Y.MAX=<value4>
```

Where the name of the electrode is given as '*electrode1*'. The location of the electrode is from x.min to x.max and y.min to y.max.

Then, the various region needs to be doped, whose syntax is

```
DOPING<doping profile>CONC =<value><doping type>REGION=<number>
```

Doping profile can vary with its concentration and type of doping which are specified by '*value*' and '*doping type*' respectively. The doping profile can be either be uniform or Gaussian.

To introduce the contacts the following syntax is required:

```
CONTACT NAME<contact name>WORKFUNCTION=<value>
```

where name of the contact is given by '*contact name'* whereas its work function is specified by '*value*'.

Instead of specifying the work function by '*value*', it can also be specified by their name in the contact statement for the commonly used contacts like N.Polysilicon, P.Polysilicon, Aluminium, Tungsten, etc. The statements used for this type of contacts are:

```
CONTACT NAME<f.gate> N.Polysilicon.
```

Sometimes even some external resistors, inductors and capacitors are also required to specify. For that the following syntax is used.

```
CONTACT NAME=<contact name> RESISTANCE=<value1>
CAPACITANCE=<value2> INDUCTANCE=<value3>
```

Here ‘value1’, value2’and ‘value3’ specifies the values of resistance in ohms, capacitance in farads and inductor in henry respectively.

3.3: Specification of models

Usually the statements for MODELS are used to indicate the physical models which are required for simulations. This is excluding the impact ionization which can be specified by the IMPACT statements. The selection of the MODELS is according to the physical phenomenon occuring inside the considered device. These MODELS be divided into the following 5 categories:

1. Carrier Statistics Models
2. Mobility Models
3. Recombination Models
4. Impact Ionization Models
5. Tunneling and Carrier Injection Models.

3.4: Common models

1. Concentration-Dependent Low-Field Mobility Model:

To activate this model, CONMOB is used in the MODELS statement. This model provides the data for low field mobilities of electrons and holes at 300K for silicon and gallium arsenide only.

2. Analytic Low Field Mobility Model:

To activate this model, ANALYTIC is used in the MODELS statement. This model helps in specifing temperature and doping dependent low field mobilities. This model is also specified by default for silicon at 300K.

3. Lombardi CVT Model:

CVT in the models statement are used for activating this model. This model's priority is much more then all other mobility models. In this model, Matthiessen's rule is used for combining the components associated with mobility dependent on transverse field, temperature and doping. On activating this model by default, Parallel Electric Field Mobility Model will also get activated.

4. Shockley-Read-Hall Recombination Model:

The SRH parameter is used in the MODELS statement for activateing this model. There are a few user-definable parameters that used in the MATERIAL statement, like TAUN0 and TAUP0 the electron and hole lifetime parameters. This model indicates the recombination of electron and hole through Shockley-Read-Hall recombination method happening within the device.

5. Auger Recombination Model:

This model can be activated by specifying AUGER in the MODELS statement. The coefficients for electrons and holes for this model are user definable parameters. These coefficients, augn and augp, can be incorporated in the MATERIAL statement.

6. Boltzmann Model:

This model is the default carrier statistics model. It is activated by specifying BOLTZMANN in the MODELS statement. As the name indicates this model follows Boltzmann statistics.

7. Fermi-Dirac Model

This model follows Fermi-Dirac statistics. It is usually in those regions which are heavily doped but with reduced concentrations of carrier. To activate this model FERMI is used in the MODELS statement.

3.5: Tunneling models

1. Standard Band To Band Tunneling Model:

For high electric field, present in the considered device, tunneling of electrons can be caused by the localized electric field such that there is a bending of energy bands at the junction of tunneling. For such kind of situation standard band to band tunneling model can be used. To activate this model BBT.STD needs to specified in the MODELS statement. The tunneling rate can be calculated by the following equation:

$$G_{BBT} = D \ \texttt{BB.A} \ E^{\texttt{BB.GAMMA}} exp\left(-\frac{\texttt{BB.B}}{E}\right)$$

Where *D* is the statistical factor, *E is* electric field. `BB.A`, `BB.B`, and `BB.GAMMA` are user-definable parameters with default values.

BB.A = $9.6615e^{18}$ cm^{-1} V^{-2} s^{-1}
BB.B= $3.0e^{7}$ V/cm
BB.GAMMA= 2.0

This model can be transformed to Klaassen model. For that BBT.STD needs to be replaced by BBT.KL in MODELS statement. The values of user definable parameters changes for this model. They are

BB.A = $4.00e^{14}$ $cm^{-1/2}$ $V^{-5/2}$ s^{-1}
BB.B = $1.9e^{7}$ V/cm
BB.GAMMA= 2.5.

2. Schenk Band to Band Tunneling Model

Phonon assisted band to band tunneling is considered for this type of model. This is a local model which contemplates constant electric field throughout the tunneling length. Its generation recombination rate can be calculated by:

$$G_{BBT}^{SCHENK} = \text{A.BBT.SCHENK} F^{7/2} S \left(\frac{(A^{\mp})^{-3/2} exp\left(\frac{A^{\mp}}{F}\right)}{exp\frac{(\text{HW.BBT.SCHENK})}{kT} - 1} + \frac{(A^{\pm})^{-3/2} exp\left(\frac{A^{\pm}}{F}\right)}{1 - exp\frac{(-\text{HW.BBT.SCHENK})}{kT}} \right)$$

where ,

$A^{\pm}$ =B.BBT.SCHENK$(\hbar\omega \pm$ HW.BBT.SCHENK$)^{3/2}$.

$\hbar\omega$ is the phonon's energy

In this equation S depends on concentrations of the carrier.

3. Kane Band-To-Band Tunneling Model

This is a local band to band model proposed by Kane. This model is similar to the other standard models but includes band gap's influence on tunneling. The tunneling rate for this model is given by

$$G_{BBT} = \frac{D\ \text{BBT.A\_KANE}}{\sqrt{E_g}} F^{\text{BBT.GAMMA}} \exp\left(-\text{BBT.B\_KANE} \frac{E_g^{\frac{3}{2}}}{F} \right)$$

Where *E*g and *F* represents the bandgap and electric field.

4. Non-local Band-to-Band Tunneling Model.

This model is nonlocal in nature unlike all the rest of the models. The spatial variation of energy bands are taken into consideration by this model. It also considers the fact that generation-recombination rate at each point does not depends only on the electric field local to the point. According to BBT.NONLOCAL the tunneling happens through1D slices, at the tunnel junction,

where each slice and the tunnel junction are perpendicular to each other. These slices are parallel to themselves. The specification of tunnel slices can be done in two different ways. They are

(i) Making rectangular area around the tunnel junction using the statements QTX.MESH and QTY.MESH.

(ii) Making a region surrounding the tunnel junction using statements QTREGION.

The first method is applicable for only planar junctions while second method can be used for both planar and non-planar junctions.

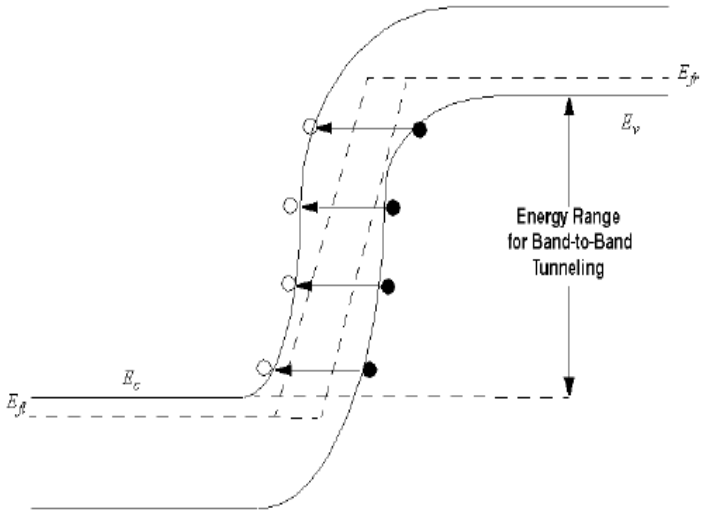

Figure 3.5.1: Schematic of non-local band to band tunneling.

Figure 3.5.1 shows the tunneling of electrons from valence band to conduction band. Tunneling of holes can also be considered. The probability of tunneling is given by WKB approximation

$$T(E) = \exp\left(-2\int_{x_{start}}^{x_{end}} k(x)dx\right)$$

Where $\boldsymbol{k}(x)$ represents the evanescent wave vector between starting point the (x_{start}) and the ending point(x_{end}) of tunneling path.

3.6: Numerical methods

The numerical methods are specified in the METHODS statement. To find solution there are three different types of techniques:

1. Gummel
2. Newton
3. Block

The first method finds solution for one unknown variable while the rest of the variables are constant. This process will continue until a stable solution is obtained. Unlike the gummel method, newton method solves and finds all the unknowns at the same time. Block method is in between newton and gummel methods as it solves a few unknowns at the same time gummel is generally used for the device studied in this project i.e. the tunnel FET.

3.7: Methods to obtain solutions

To calculate current as well as other parameters such as carrier concentrations and electric fields, the device electrodes needs to be supplied with voltages. At first, electrodes are provided with zero voltages, after that the bias voltage applied is varied in small steps. These needs to be specified in the SOLVE statements.

1. DC Solution

A fixed DC bias can be applied on the electrode by using the DC solve statements.

`SOLVE <v.electrode name>=<value>.`

According to this statement the required electrode, '*electrode name*' is supplied with DC voltage '*value*'.

For sweeping the bias of a particular electrode from '*value1*' to '*value2*' in a particular order of steps '*step1*', the following command is used.

SOLVE <v.*electrode name*>=<value1> VSTEP=<step1> VFINAL=<step2> NAME=<*electrode name*>.

Convergence can be obtained for the used equations by supplying a good original presumption for the variables that need to be evaluated at each bias point. Initial solution can be achieved by the given statement,

SOLVE INIT.

2. AC Solution

A simple extension of the DC solution syntax can specify the AC simulations. A post-processing operation to a DC solution leads AC small signal analysis. The conductance and capacitance between each pair of electrodes is the results of AC simulations. The command used for this is

SOLVE VBASE=0.7 AC FREQ=1e9 FSTEP=1e9 NFSTEPS=10

3.8: Prediction of results

The output files of Atlas are of three different types. They are:

1. Run-Time Output

The output seen at the bottom of the Deck Build Window is the run-time output. Any errors occurring during this output will be displayed in the run-time window.

2. Log Files

These files are required for storing the terminal characteristics calculated by Atlas. It consist of the current and voltages for each electrode during the DC simulations. In transient simulations, the time is saved. Whereas for AC simulations, the conductance, capacitances and the small signal frequency are stored.

3. Extraction of parameters In Deck Build

For this the EXTRACT command is introduced inside the Deck Build environment. Thus extracting the various parameters of the device. The command has a flexible syntax that allows

you to construct specific EXTRACT routines. EXTRACT can operate on the earlier solved curve or structure file.

3.9: Models used in simulation of devices under study

As tunneling FET is the studied topic of this thesis, non local band-to-band tunneling model has been considered for the simulation purpose. Apart from non local BTBT model, the other models were also taken into consideration like recombination models like auger recombination and srh models, concentration field mobility model. The carrier statistics model used for this simulation is Fermi model.

3.10: Simulated structure of junctionless double gate tunnel FET(JDGFET))

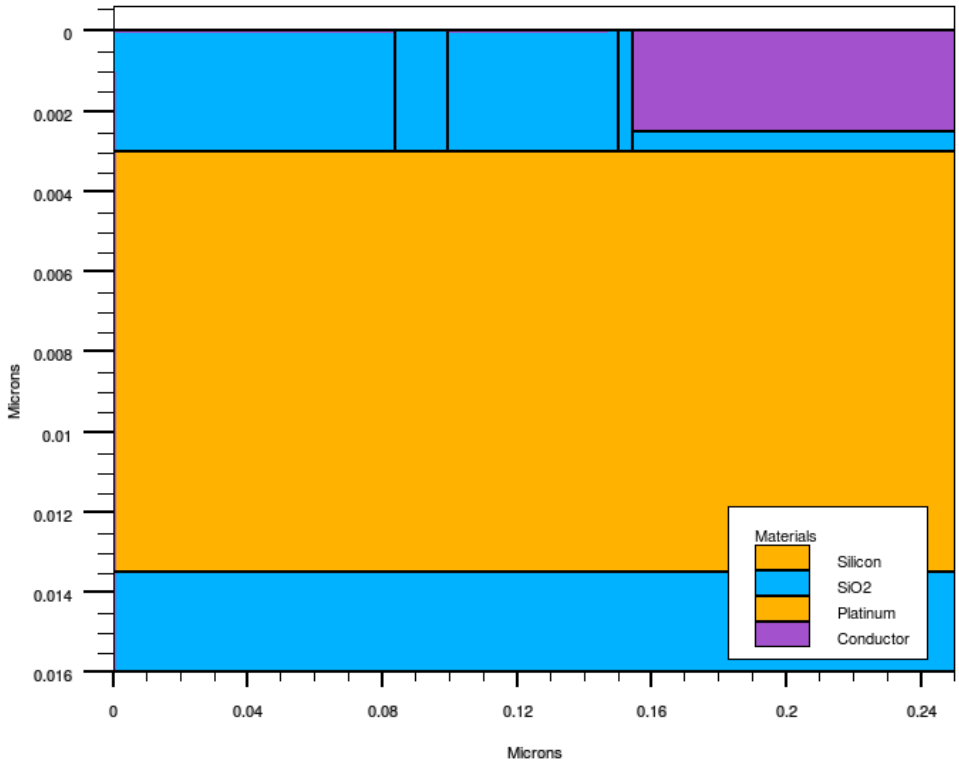

Figure3.10.1:.Tonyplotstructure file of JDGFET

The meshing in the tunneling junction of the device is very fine. In case of less fining in that junction, the simulations results will be exaggerated. As seen from the transfer characteristics in the given graph below, for the less fine meshing of the device, on the logarithmic scale (left side) the resolution of the off region mislaid and on the linear scale (right side), on-current is underrated.

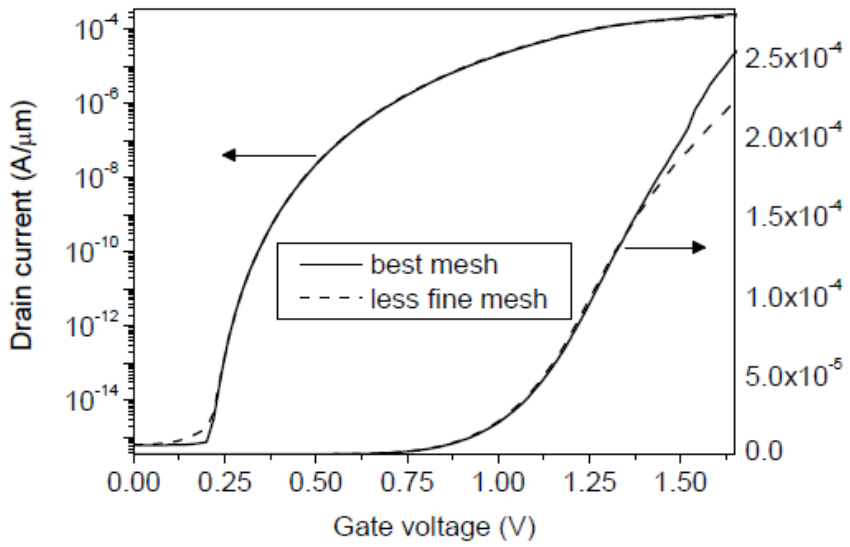

Figure 3.10.2: Transfer characteristics of the Device shown, with both a less fine mesh(dashed lines) and the standard mesh(solid lines).

The following figure (figure 3.10.3) shows the studied device structure with its meshing lines. As can be seen, the meshing near the junction between intrinsic and source where tunneling takes place is finer in comparision with the meshing in the rest of the area of the simulated device.

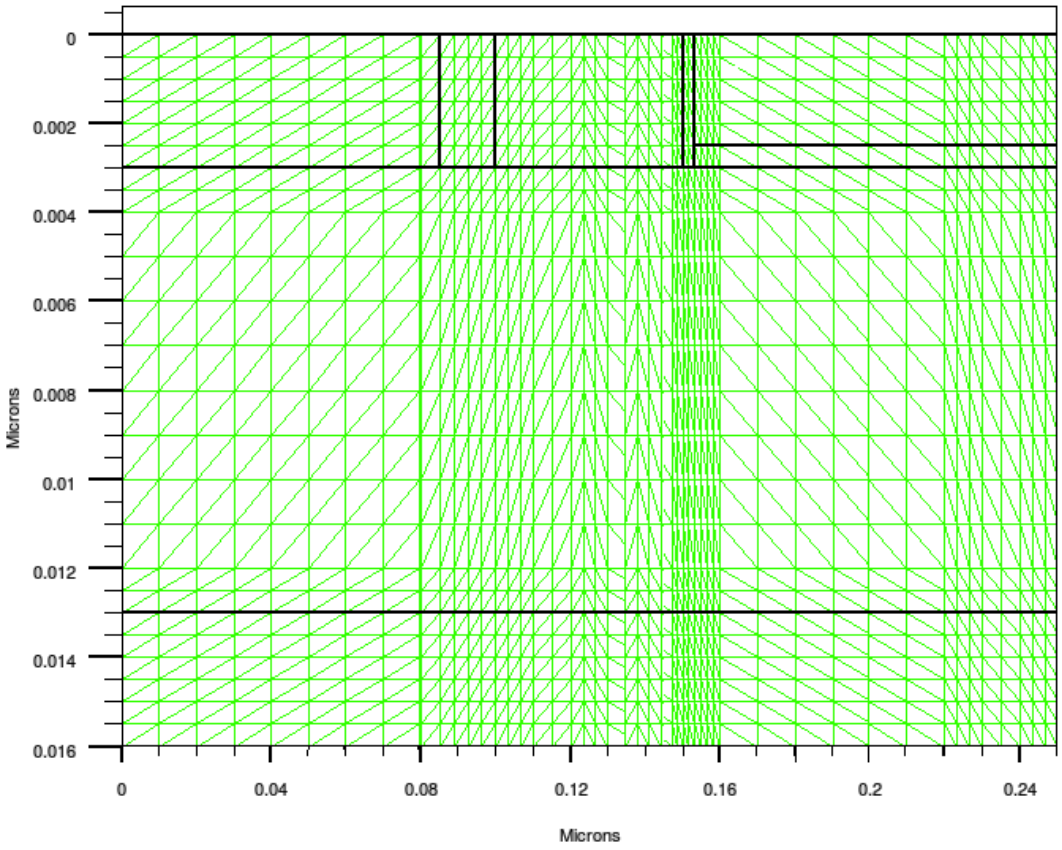

Figure 3.10.3:Tonyplot structure file of JDGTFET with meshes

Chapter 4
DEVICE STRUCTURE

4.1: Introduction

Low subthreshold swing and low OFF-state leakage current are attracting wide attention towards the Tunnel Field Effect Transistors. But due to random dopant fluctuations (RDF) the performance of transistors varies randomly in aggressively scaled devices and also introduces a complex thermal budget due to the need for ion implantation and expensive thermal annealing techniques through presence of doped source and drain regions in TFETs. Hence in this work a junction-less TFET which is already introduced by M. Jagadesh Kumar et al. in 2013 is studied further. Junction-less tunnel field effect transistor has been designed using charge plasma concept which can form the source and drain regions without the need for any doping by choosing appropriate work functions for the source and drain metal electrodes. Though the performance of the doping-less TFET doesnot vary compared to doped TFET, it is expected to be removed from all problems associated with random dopant fluctuations. Also its fabricating is possible on single crystal silicon-on-glass substrates.

4.2: Device Operation and Structure

The parameters taken for the junctionless double gate tunnel FET is same as that with the DGFET with junction. The structure of the device is a lateral n-type Tunnel FET in a thin silicon layer. A dielectric layer separates this thin silicon layer and the substrate. The principal design of this device is a gated p-i-n diode. The tunneling in this device takes place between the intrinsic and p+ regions. Thickness of silicon film(Tsi) = 10nm and gate oxide (Tox) = 3nm and length of channel (L) = 50 nm. The formation of source and drain is without separate doping on the silicon. The “p” source and “n” drain regions in this structure are formed using the concept of charge plasma. The silicon body of the device is doped with a carrier concentration of ni=1 × $10^{15}/cm^3$.[22]

In the intrinsic silicon body, hafnium (work function=3.9 eV) is used as the drain metal electrode for creating the "n" drain region by inducing electrons with a concentration similar to the N+ drain doping of the DFET. Similarly, platinum (work function = 5.93 eV) is used in the intrinsic silicon body as the source metal electrode, for creating the "p" source region by inducing holes with a concentration similar to the P+ source doping of the reference device. To avoid the possibility of silicide formation, a 0.5 nm thick silicon dioxide has been inserted between the source metal electrode and the silicon film. And a layer of silicon dioxide of 3.0 nm thickness has been inserted in between the silicon and the drain metal electrode so as the electron concentration is induced in the drain region. The gate electrode and the source has spacer oxide($L_{GAP,S}$) of thickness 3nm, whereas the thickness of the spacer oxide between the gate electrode and the drain($L_{GAP,D}$) is of 15nm. $L_{GAP,D}$ thickness is almost same as the width of the depletion region on the drain-channel side of the double gate tunnel FET.

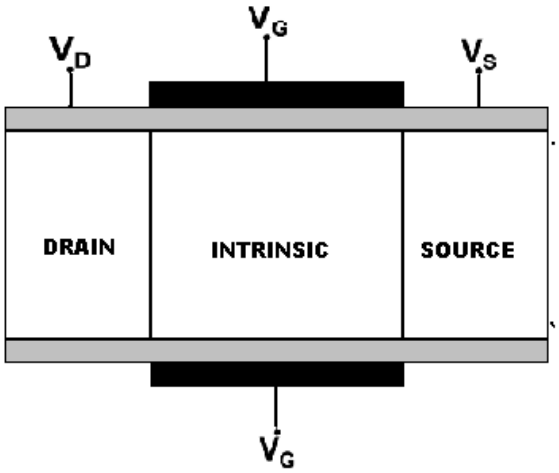

Figure 4.1.1: Cross sectional view of double gate TFET

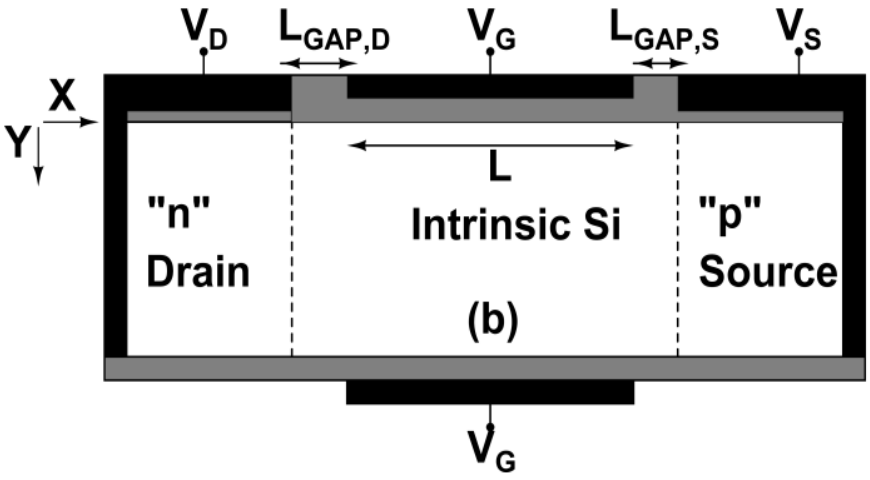

Figure 4.1.2: The junction-less double gate TFET.

The contour plots of the structure with the concentration of electrons and holes across its tunneling junction are shown in the following figures.

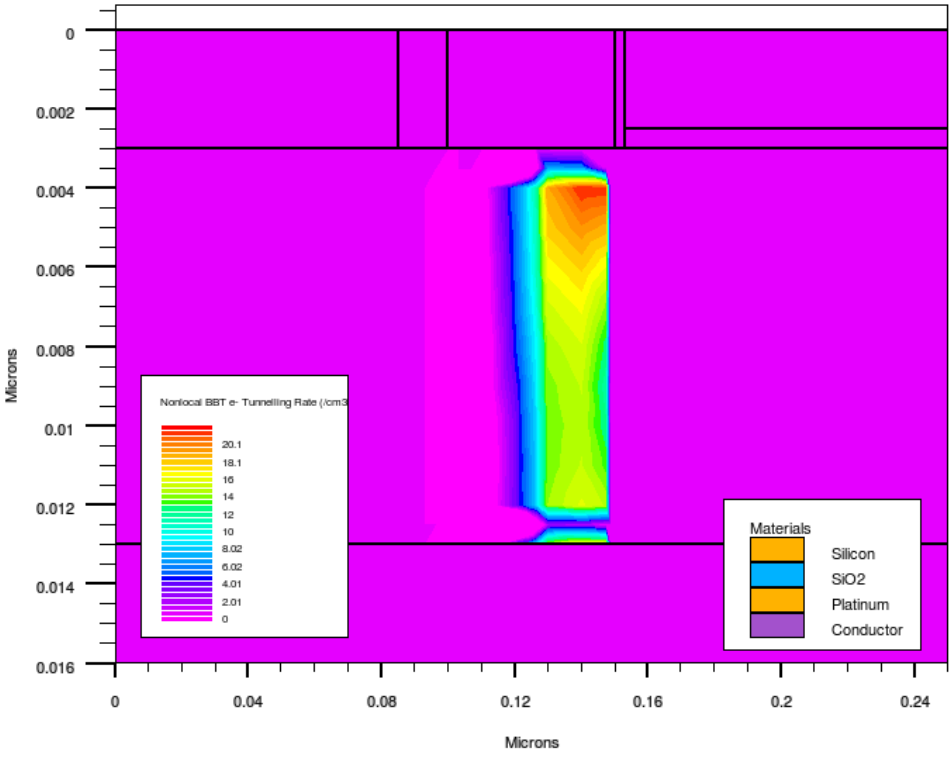

Figure 4.1.3: Contour plot with electron concentration

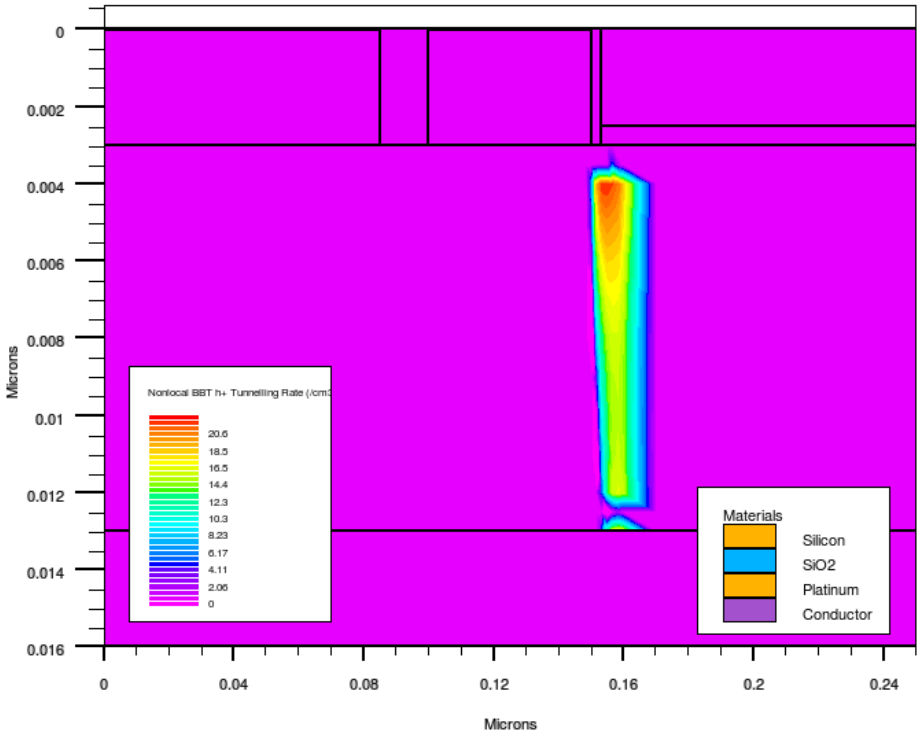

Figure 4.1.3: Contour plot with holes concentration

Chapter 5
SIMULATION RESULTS & DISCUSSIONS

5.1. Introduction

In this chapter, all the simulation results and its discussion are briefly described for the junctionless double gate tunnel field effect transistor. Both the input and the output characteristic of the device has been simulated. Also the transfer characteristic of the device for different dielectric material and temperature were also simulated. The threshold voltage for varying silicon body thickness and gate length has been calculated in this chapter.

5.2 :Energy band Diagram of JDGFET

Figure 5.2 .1 shows energy-band diagram of the simulated device when it is in the OFF-state. Through this energy band diagram, it can be observed that the probability of tunneling of electrons is negligible when the device is in off state, as a large tunneling barrier exists in between the source and channel region. Consequently in this state, the only current present is the p-i-n diode leakage current. But when the device is in ON state, as shown in the energy band diagram below (Figure 5.2.2), the tunneling barrier between the source and intrinsic are of the device lowers significantly, leading to a high possibility of tunneling of electrons from the valence band of the channel to the conduction band of the source.

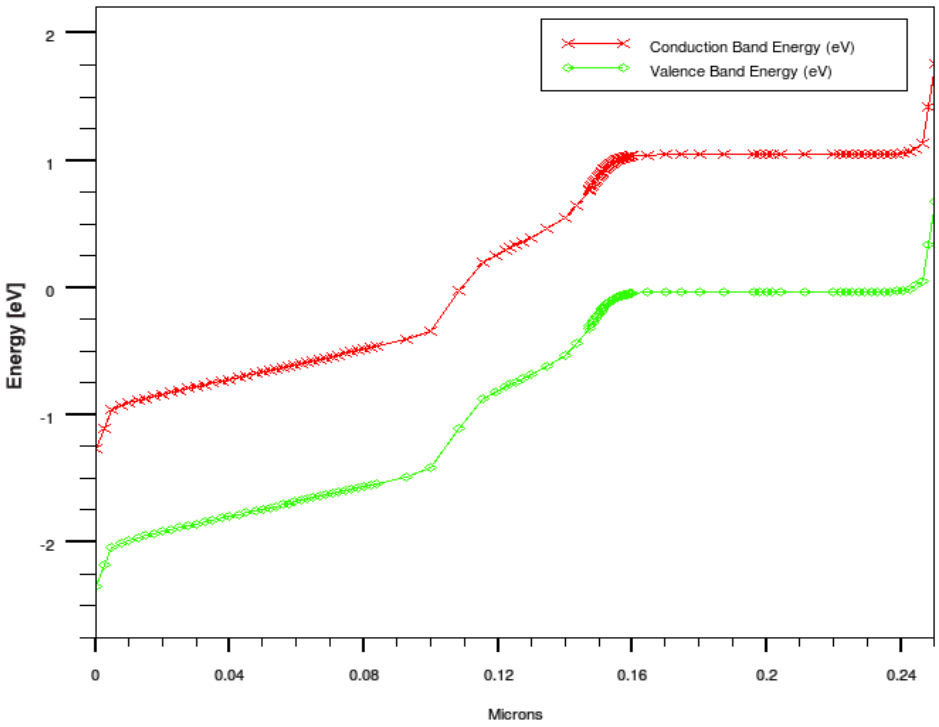

Figure 5.2.1: Energy-band diagram of the device when it is in OFF-state

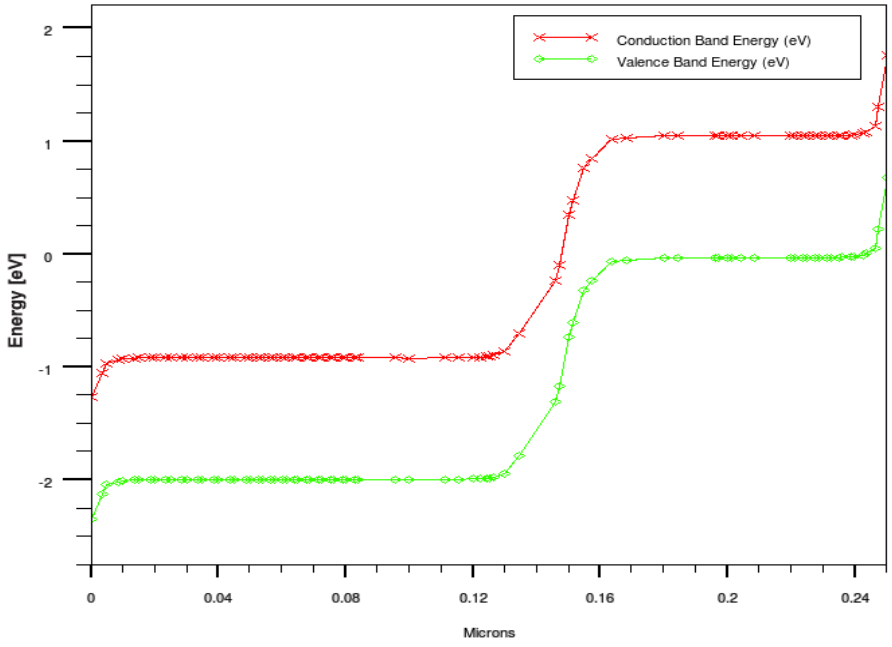

Figure 5.2.2: Energy-band diagram of the device when it is in ON-state

5.3: Input characteristic

The figure 5.3.1 shows the input characteristic for dissimilar drain voltage (V_D/ ranging from 50 mV to 2 V). It can be seen that till as the drain voltage reaches 1V from 50 mV, there is a increase in the tunneling current, because in TFET tunneling current depends on the drain voltage also along with the gate voltage but. But beyond 1V of drain voltage there is not much improvement on the I_{ON}, due to the effect of the short channel effect (such as velocity saturation, DIBL and pinch-off mechanism).

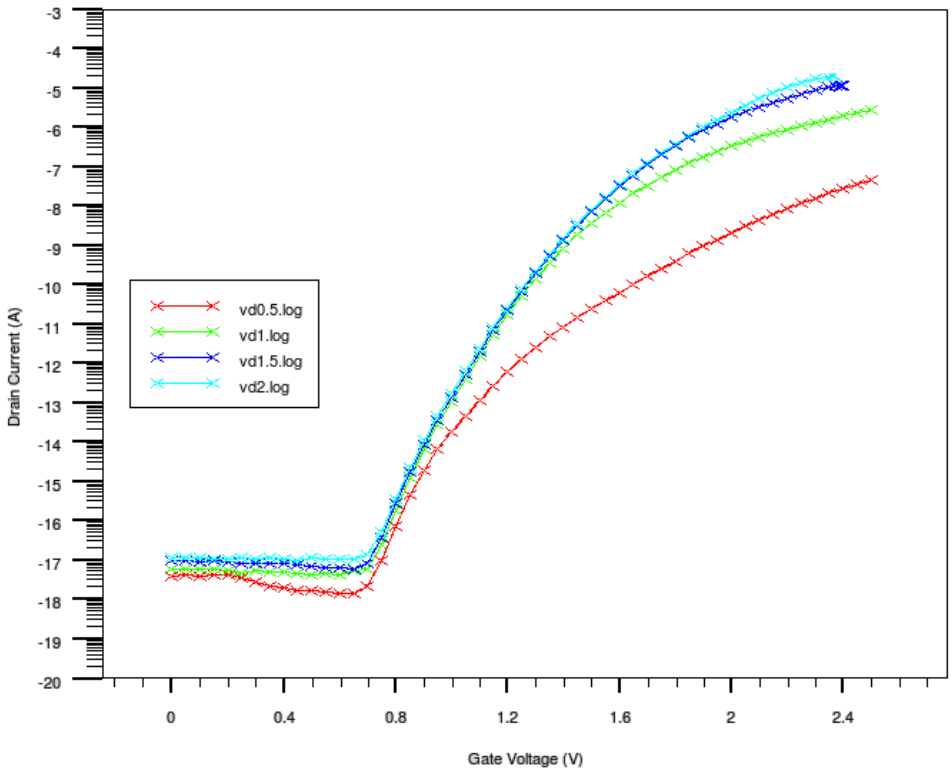

Figure 5.3.1: Transfer characteristics for different drain voltage (V_D) values from 50 mV to 2 V.

5.4: Output characteristic

The output characteristics of junctionless double gate tunnel FET have been studied with varying gate voltages. From the figure (figure 5.4.1) it is observed that the ON-current present on the device when supplied with 50 mV at the V_G terminal is much less as compared to on current during the application of a voltage of 2 V. This happens due to the reason that the tunneling barrier in the first case is wide enough and hence the probability of tunneling of charge carriers would be very less. But with the increment in the applied gate voltage on the gate from 50 mV to 2 V, continuous improvements in I_{ON} are observed. This happens due to continuous reduction in the tunneling barrier width, which in return improves the probability of tunneling of more and more charge carriers and hence there is a continuous increase in the ON-current as the gate voltage sweeps from 50 mV to 2 V.

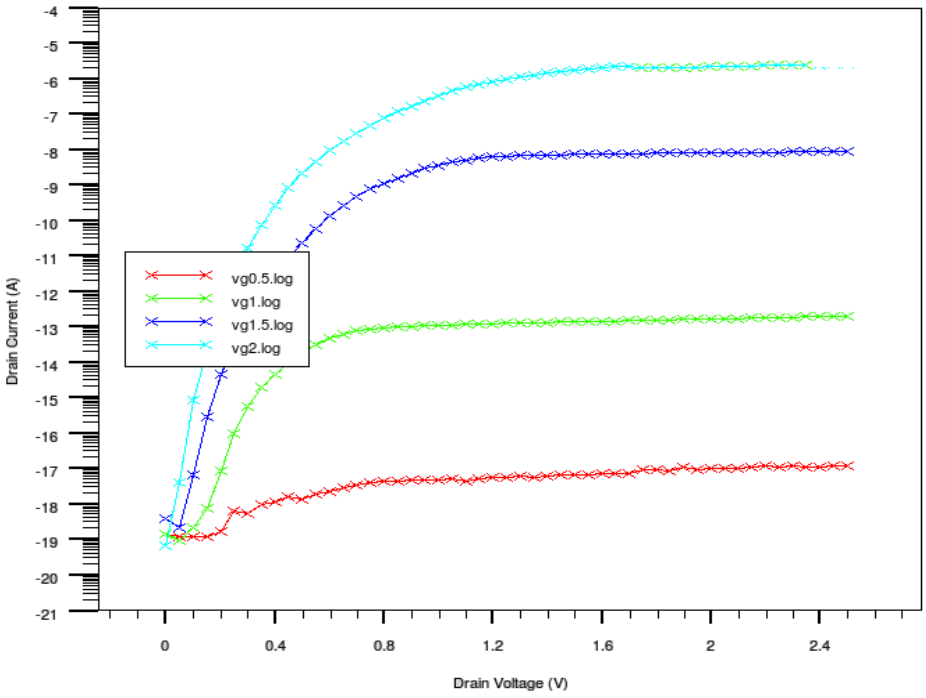

Figure 5.4.1: I_D versus V_D of the device for different V_G values from 50 mV to 2 V.

5.5:Silicon thickness

The following figure (5.5.1) shows the transfer characterestics of the JDGFET for different silicon body thicknes. It is clearly visible that the device responsive to the thickness of the silicon body which in return influence the IDS-VGS curve's shape. From the graph it can be said that a thinner film modifies the electric field lines, increasing the gate control of the barrier width in tunnel junction.

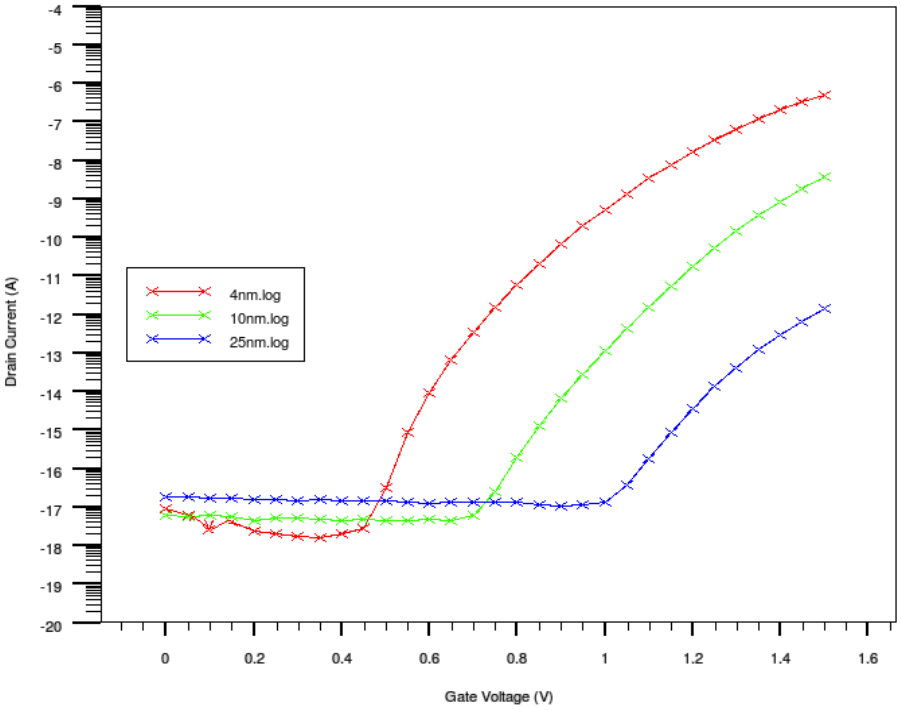

Figure 5.5.1: Transfer characterestic of the device for different silicon body thickness values varying from 4nm to 25nm.

5.6: High K dielectric material

By choosing the best gate dielectric material, the on-current of the device can be improved and also the subthreshold swing of lesser value can be attained. The following figure (figure 5.6.1).

shows the transfer characteristics of JDGFET using various gate dielectric materials. The gate dielectric materials used here are SiO2 (Silicon dioxide), Si3N4 (Silicon Nitrate) and HfO2 (Hafnium Oxide) with dielectric constant of 3.9, 7.5 and 21 respectively. The physical thickness of all the gate dielectric materials for the structure is same, i.e. 3nm on both sides of the silicon body except that in the area in between the silicon film and the source metal electrode consist of the dielectric material with a thickness of 0.5nm only.

The improvement in the Ion because of high-k dielectric materials as can be studied for the device from the figure shown below. The Off- current for the structure is of very less value, i.e. in the range of fA using the high –k dielectric materials also.

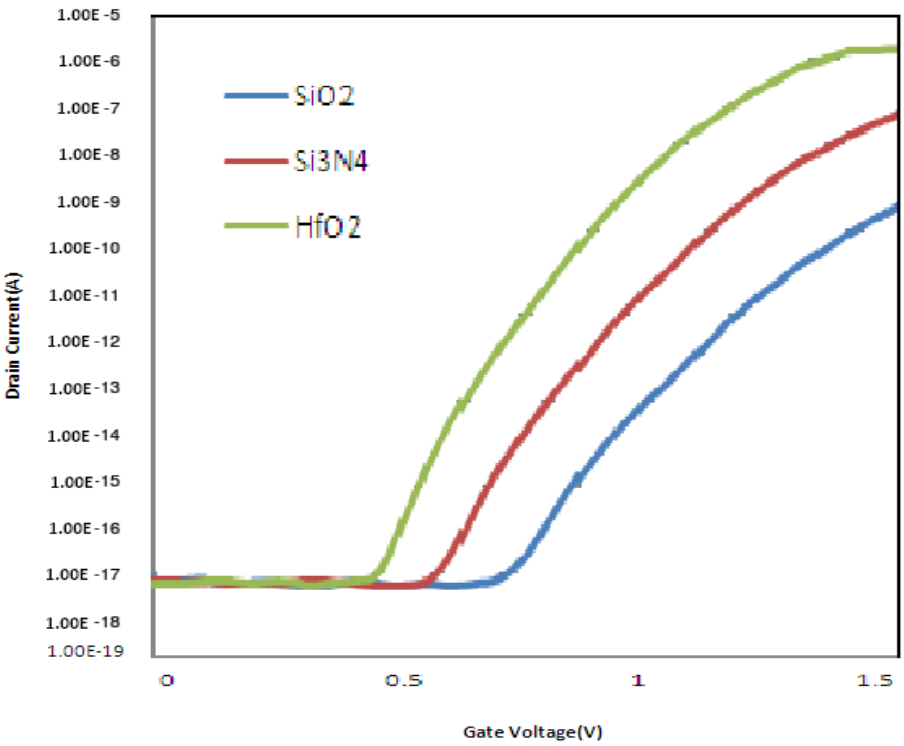

Figure 5.6.1:. Transfer characteristics for different dielectric material

5.7: Threshold voltage:

One of the important parameter of a solid-state switch is its threshold voltage. The definition of threshold voltage for MOSFET is that it is that gate voltage on applying which the transition between both the strong and weak inversion begins. During this transition the carrier concentration at the surface of the inversion channel is equivalent to substrate's doping level, φs=2φF. But for tunnel FET threshold voltage is that gate voltage at which shifting of both the weak and strong control of the width of the tunneling energy barrier begins at the junction of the tunnel (23). The shifting position among a linear dependence and a quasi-exponential dependence of the current over the voltage applied on the gate can be seen at point where modulation takes place in the energy barrier width of tunneling (Wbs).

Earlier, the threshold voltage for single gate Tunnel FET and double gate Tunnel FET were found by the transconductance change method. The same method is already authenticate for MOS transistors. As per this method any non-linear device's threshold voltage is that gate voltage which is equivalent to the highest derivative of transconductnce (dgm/dVg).

The threshold voltage for a tunnel FET has been calculated as (23):

$$V_{TG} = \frac{qN_i t_{si}}{2C_{ox}} + \frac{(\lambda_1\theta_2 + \lambda_2\theta_3 + \lambda_1\theta_1)\alpha^2 C_{si} t_{si}^2}{(\theta_1 + \theta_2 + \theta_3)C_{ox}(2 + \frac{C_{ox}}{C_{si}})\eta} + \phi_{MS}$$

Where

$$\lambda_1 = \frac{KT}{q}\log(\frac{N_d}{n_i}) + V_{ds}$$

$$\lambda_2 = -\frac{KT}{q}\log(\frac{N_s}{n_i})$$

$$\theta_1 = \exp(\alpha L_g) - \exp(-\alpha L_g)$$

$$\theta_2 = \exp(-\alpha w_{bs}) - \exp(\alpha w_{bs})$$

$$\theta_3 = \exp(-\alpha L_g)\exp(\alpha w_{bs}) - \exp(\alpha L_g)\exp(-\alpha w_{bs})$$

Wbs is the width of the tunneling energy barrier, Lg is the length of gate

The threshold voltage for the junctionless double gate tunnel FET has been analyzed for different body thickness and for different gate lengths.

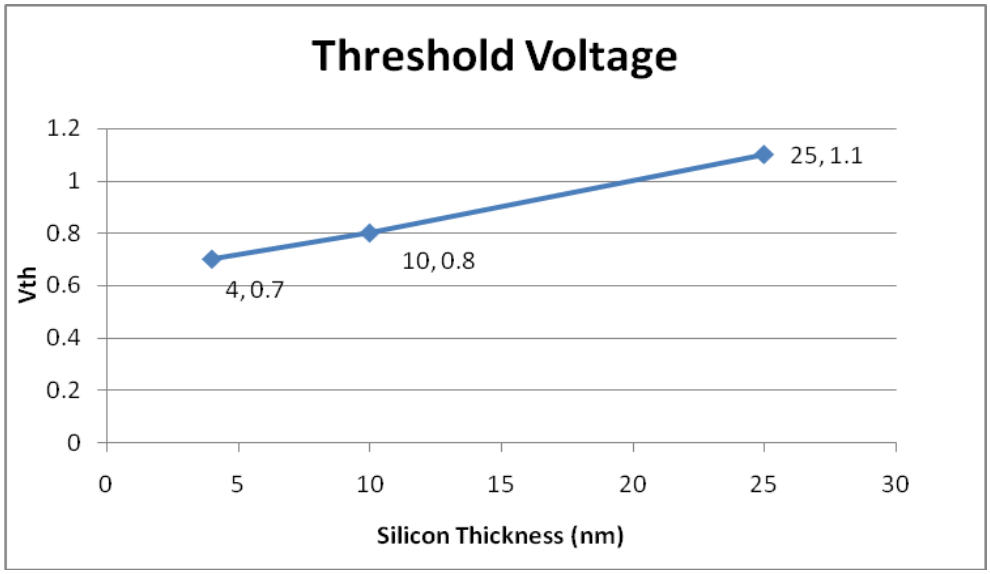

Fig 5.7.1 Threshold voltage V_T vs silicon thickness

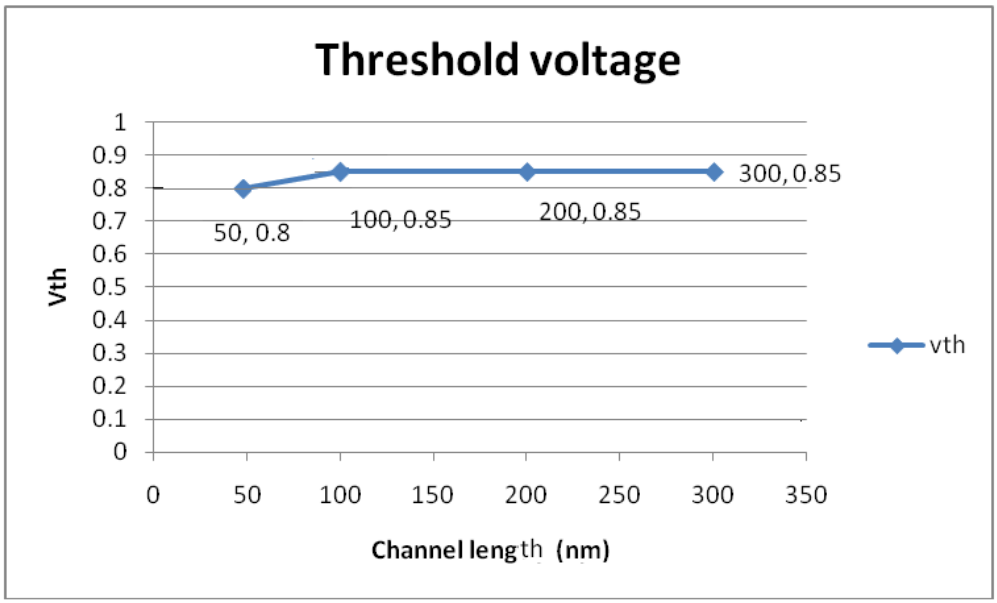

Figure 5.7.2: Threshold voltage V_T vs Channel Length of the device

Figure 5.7.1 shows how the threshold voltage of the junction-less DGFET varies with the varying thickness of the Silicon layer. It can be studied that the threshold voltage and the Silicon layer thickness are proportionate, i.ie. with the increase in the thickness of the Si film, the threshold voltage also increases linearly. As already shown in the *I*ds−*V*gs curve of the junctionless DGFET for dfferent Silicon thickness, it can be concluded that the device is perceptive of the thickness of the Silicon body.

But the same cannot be assumed for the varying channel length. The effect of gate length scaling is restricted on the device threshold voltage as its effect on the device's transfer characteristics is modest provided the length is beyond that vital length upon which there is occurrence of a high p-i-n leakage current in the offset.

From figure (b) it can be seen that a very small V_{TG} roll-off exist for channel length less than 100nm of the junction less double gate tunnel FET. The reason for V_{TG} roll-off in Tunnel FET is much different with respect to the reason in MOSFET. This roll-off happens due to the increase in the diode leakage at short lengths of the device (band-to-band tunneling takes place at lower Vgs which is not controllable by the device gate).

5.8: Temperature

The dependence of the transfer characteristics of the studied device on the varying temperature can be seen in the following figure. It can be viewed that the effect of temperature on the Ioff (off current) is more compared to almost negligible effect of temperature on the Ion(on current) (3, 4). There is a increase in the structures off current flowing on the structure. The Ioff of the structures, which is originates with the creation of carriers on the reverse biased junction, increases with the increase in temperature. Unlike the Ioff, the Ion triggered through band-to-band tunneling, has almost no change with the increase in the temperature. The difference in the temperature dependence in the ON and off-state is due to dominance of BTBT phenomenon in

the ON state, which is weakly dependent on temperature and the SRH dominance at low electric fields which has strong temperature dependence.

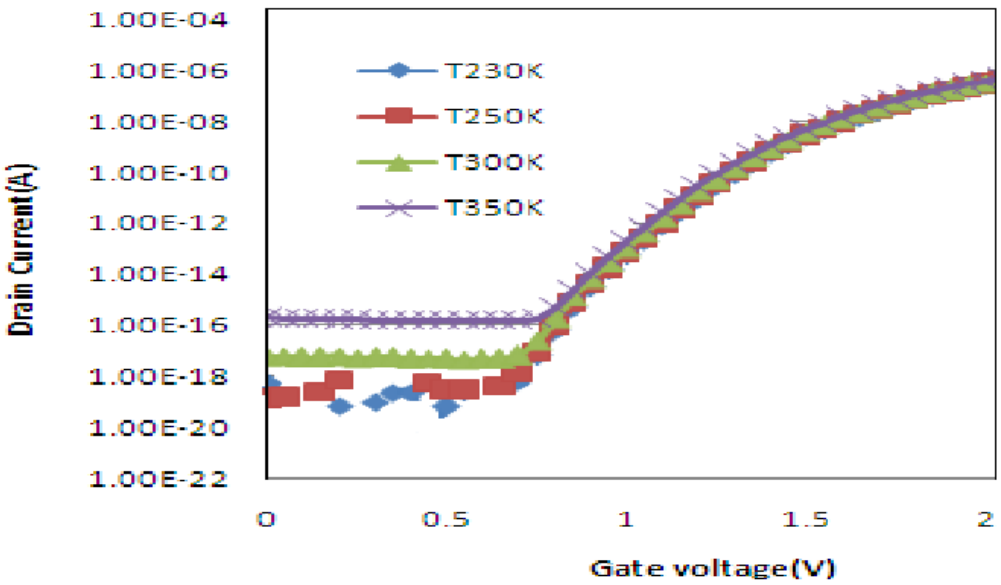

Figure 5.8.1: *Transfer characteristics temperature*

5.9: Subthreshold slope

The subthreshold slope has been calculated for the mentioned device with gate length of 50nm, silicon thickness 10nm and with silicon dioxide as its dielectric material for a temperature of 300K. on applying the drain voltage of 1V the subthreshold slope for the device has been found to be of a value 56.7mV/decade.

Chapter 6
CONCLUSION

6.1 Performance Analysis:

The performance of the junctionless double gate tunnel has been studied. Very good results have been achieved for different performance parameters with the use of optimized device structure parameters, identified by the simulation studies of the impact of variations of different device parameters on the performance parameters of the JDGFET. It can be said that the device will be in its best state on using a thinner silicon body thickness with a dielectric material of higher dielectric constant. The subthreshold slope for the device has been found to around 56.7mV/decade. Also due to the absence of dopant atoms in the doping-less TFET, it is expected to be immune to random dopant fluctuations. Moreover, the fabrication of the doping-less TFET does not demand high thermal budgets for creating the source and drain opening up the possibility of realizing TFETs on other substrates such as single-crystal silicon-on-glass.

6.2: Scope of Future work

In the future, the RF analysis of this device can be studied. Also modeling of the device is another work that can be done in the future.

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