Investigation on Cascade Multilevel Inverter for Medium and High-Power Applications

A Thesis submitted in partial fulfillment of the requirements for the degree of

Doctor of Philosophy
In
Electrical Engineering

By

Y.Suresh

Under the supervision of

Prof. Anup Kumar Panda

Department of Electrical Engineering

National Institute of Technology, Rourkela

July 2012

Investigation on Cascade Multilevel Inverter for Medium and High-Power Applications

Y. Suresh

Department of Electrical Engineering

National Institute of Technology, Rourkela

Investigation on Cascade Multilevel Inverter for Medium and High-Power Applications

A Thesis submitted in partial fulfillment of the requirements for the degree of

Doctor of Philosophy
In
Electrical Engineering

By

Y.Suresh
Roll No.:509EE104

Under the supervision of

Prof. Anup Kumar Panda

Department of Electrical Engineering

National Institute of Technology, Rourkela

July 2012

Declaration

I hereby declare that the work which is being presented in the thesis entitled "Investigation on Cascade Multilevel inverter for Medium and High power Applications" in partial fulfillment of the requirements for the award of the degree of DOCTOR OF PHILOSOPHY submitted to the Department of Electrical Engineering of National Institute of Technology, Rourkela, is an authentic record of my own work under the supervision of Prof. A. K. Panda, Department of Electrical Engineering. I have not submitted the matter embodied in this thesis for the award of any other degree or diploma of the university or any other institute.

Date 17th July, 2012 Y.Suresh

DEPARTMENT OF ELECTRICAL ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY, ROURKELA
ORISSA, INDIA - 769008

CERTIFICATE

This is to certify that the thesis titled "**Investigation on Cascade Multilevel inverter for Medium and High-Power Applications**", submitted to the National Institute of Technology, Rourkela by **Mr. Y. Suresh.**, Roll No. **509EE104** for the award of Doctor of Philosophy in Electrical Engineering, is a bona fide record of research work carried out by him under my supervision and guidance.

The candidate has fulfilled all the prescribed requirements.

The Thesis which is based on candidate's own work, has not submitted elsewhere for a degree/diploma.

In my opinion, the thesis is of standard required for the award of a Doctor of Philosophy degree in Electrical Engineering.

Prof. A. K. Panda
Department of Electrical Engineering
National Institute of Technology
Rourkela – 769008
Email: akpanda@nitrkl.ac.in

BIO-DATA OF THE CANDIDATE

Name : Y.Suresh

Date of Birth : 11st Aug, 1984

Permanent Address : Do No: 23/57, Venkatagiri Town,
Nellore [DT], Andhra Pradesh, India.

Email : ysuresh.ee@gmail.com

ACADEMIC QUALIFICATION

- Pursuing Ph. D in Electrical Engineering, National Institute of Technology, Rourkela.
- M. Tech in Electrical Engineering, National Institute of Technology, Rourkela.
- B. E. in Electrical Engineering from JNTU University, Andhrapradesh.

RESEARCH PUBLICATIONS

JOURNAL

1. A.K.panda, Y.Suresh, "Research on Cascade Multilevel Inverter with Single DC Source by Using Three-Phase Transformers", Int J Electric Power Energy Syst. **(Elsevier)** 40 (2012) 9–20.
2. Y. Suresh, A.K Panda, Research on Cascade Multilevel Inverter by Employing Three-Phase Transformers, IET Power Electron., 5 (5) 2012, 561 – 570.
3. A.K.panda, Y.Suresh, "Performance of Cascade Multilevel Inverter by Employing Single and Three-Phase Transformers", IET Power Electron, 2012 (Accepted)

CONFERENCE

1. Y.Suresh, A.K.Panda, "Performance of Cascaded Multilevel Inverter with Single DC Source by Employing Three- Phase Low frequency Transformers, **IECON-2010** is

the 36th Annual Conference of the IEEE Industrial Electronics Society Pheonix, Arezona , USA -2010.

2. Y.Suresh, A.K.Panda, M.Mahesh , "An Improved Performance of Cascaded Multilevel Inverter with Single DC Source by Employing Three-Phase Transformers" IEEE International power and energy conference **(IPEC)** Singapore, 27-29, oct-2010.
3. Y.Suresh, A.K.Panda, "Dynamic Performance of STATCOM under Single Line to Ground Faults in Power System", 5th **IET** International Conference on Power Electronics, Machines & Drives **(PEMD 2010)**, Brighton, UK, 19th– 21th April 2010, Digital Object Identifier: 10.1049/cp.2010.0125, pp.1-6.
4. M.Suresh, S.S Patniak, A.K.Panda ,Y.Suresh, , "Current Harmonics Cancellation in Three-Phase Four wire systems, **IEEE-PES** Power Systems Conference & Exposition , April -29 , 2011, Phoenix, Arizona, USA.

ACKNOWLEDGEMENTS

I would like to express my sincere gratitude to my supervisor Prof. A. K. Panda, for his guidance, encouragement, and support throughout the course of this work. It was a precious learning experience for me and I am proud to be one of his students. In fact, he is backbone to my research carrier. From him I have gained not only extensive knowledge, but also careful research thoughts.

I am very much thankful to Prof. B. D. Subudhi, Head, Department of Electrical Engineering, for his constant support. Also, I am indebted to him who provided me all official and laboratory facilities.

I am grateful to my Doctoral Scrutiny Members, Prof. K. B. Mohanty and Prof. K. K. Mahapatra for their valuable suggestions and comments during this research period.

I am especially indebted to my colleagues in the power electronics group. First, I would like to specially thank Mr. Mikilli Suresh, who helps me in implementing my real time experiments. We share each other a lot of knowledge in the field of power electronics. I would also thank my beloved friend Mr. Kalapraveen for his valuable thoughts in my research carrier. I would also like to thank the other members of the team, Prof. Matiy, Prof. B. Chitti Babu, Mr. Matada Mahesh, for extending their technical and personal support making my stay pleasant and enjoyable.

This section would remain incomplete if I don't thank the lab assistants Mr. Rabindra Nayak without whom the work would have not progressed.

lastly, with deepest love, I would be grateful to my beloved Father & Mother who supported and encouraged me all the time, no matter what difficulties are encountered.

Y. Suresh

CONTENTS

ABBREVIATIONS

SCR	-Silicon-Controlled Rectifier
GE	-General Electric
IGBT	-Insulated Gate Bipolar Transistor
FACTS	-Flexible Ac Transmission Systems
IGCT	-The Integrated Gate Commutated Thyristors
SiC	-Silicon Carbide Material
TRIAC	-Triode For Alternating Current
BJT	-Bipolar Junction Transistor
MOSFET	-Power Metal-Oxide Semiconductor Field Effect Transistor
CPLD	-Complex Programmable Logic Devices
ASIC	-Application Specific Integrated Circuit
PEBB	Power Electronics Building Blocks
APF	-Active Power Filters
EPQ	-Electric Power Quality
VSC	-Voltage Source Converter
LNG	-Liquefied Natural Gas
NPC	-Neutral-Point-Clamped Converter
NPC-MLI	Neutral-Point-Clamped Multilevel Inverter
FC-MLI	Flying Capacitor Multilevel Inverter
DCC	-Diode-Clamped Converter
FC	-Flying Capacitor Converter
CHB	-Cascade H-Bridge

CHB-MLI	-Cascade H-Bridge Multilevel Inverter
PWM	- Pulse Width Modulation
SVG	-Static Var Generation
MLI	-Multi Level Inverter
CMI	-Cascaded Multilevel Inverter
CMLI	Cascaded Multi-Level Inverter
HBBB	-H-Bridge Building Block
PWM	-Pulse Width Modulation
SVM	-Space-Vector Modulation
CM	-Common-Mode
NPC	-Neutral-Point Clamped
GTO	-Gate Turn Off Thyristors
SVM	-Space Vector Modulation
THD	-Total Harmonic Distortion
SHE	-Selective Harmonic Elimination
SHEPWM	-Selective Harmonic Elimination Pulse Width Modulation
SVC	-Space Vector Control
DTC	-Direct Torque Control
UPQC	-Unified Power-Quality Conditioner
VSI	-Voltage-Source Inverter
DCI	-Diode Clamped Inverter
FCMLI	-Flying Capacitor Multi Level Inverter
HV	-High Voltage

FPGA	-Field Programmable Gate Array
LV	-Low Voltage
EMC	-Electro Magnetic Compatibility
SPWM	-Sinusoidal Pulse Width Modulation
DC	-Direct Current
DSP	-Digital Signal Processing
EMI	-Electro Magnetic Interference
STATCOM	-Static Synchronous Compensators
SSSC	-Static Series Compensators
RTDS	-Real Time Digital Simulator
VFD	-Variable Frequency Devices
APF	-Active Power Filters
PCC	-Point of Common Coupling

NOTATIONS

V_{in}	- Input Voltage
V_{out}	-Output Voltage
P_{in}	-Input Power
P_{out}	-Output Power
D	-Duty cycle
T_S	-Time period
P_{loss}	-Power loss
V_O	-Output Voltage
I_O	-Output Current
V_{dc}	-Input DC voltage
S_{W1}	-Switch
V_{an}	-Phase to neutral voltage
V_{ab}	-Line to Line voltage
V_{a0}	-Phase " a" voltage
C_a, C_b, C_c	-Storage Capacitance
H_1,H_2	-Bridge cell
V_c	-Capacitor votalge
Tr.1	-Transformer 1
N	-Transformation matrix
V_{AS}	-Summation of Phase "a" Votlage
*V*ak	-Input voltage
M	-Modulation index

α_k	-Switching angle
β	-Phase shift angle
φ_{cr}	-Phase difference between two adjacent carriers
V_{sin}	-Reference waveform
V_{tri}	-Carrier waveform
I_L	-Load current
θ	-Transformation angle
i_d	-Active Currents
i_q	-Reactive Currents
I_{Lah}	-Load Harmonic current
f_c	-Cut off frequency
V_{dc}*	-Reference DC link voltage
K_i	-Integral coefficient
K_P	-Proportional coefficient
I_S	-Source Current
I_F	-Filter Current

ABSTRACT

It is hard to connect a single power semiconductor switch directly to medium voltage grids (2.3, 3.3, 4.16, or 6.9 kV). For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels. Multilevel inverters have received more attention in industrial application, such as motor drives, static VAR compensators and renewable energy systems, etc. Primarily multilevel inverters are known to have output voltages with more than two levels. As a result, the inverter output voltages have reduced harmonic distortions and high quality of waveforms. Additionally, the devices are confined to fraction of dc-link voltage. These characteristics make multilevel inverter to adopt for high-power and high-voltage applications. A good number of multilevel inverter topologies have been proposed during the last two decades. Contemporary research has engaged novel converter topologies and unique modulation schemes. Moreover, four major multilevel inverter structures have been reported in the literature these are as follows: cascaded H-bridges inverter (CHB) with separate dc sources, diode clamped (neutral-clamped), and flying capacitors (capacitor clamped), P2 Multilevel inverters. Although different multilevel inverter exists, *Cascade Multilevel Inverter* (CMI) is one of the productive topology from multilevel family. In reality, on comparing with other multilevel based topologies, CMI feature a high modularity degree because each inverter can be seen as a module with similar circuit topology, control structure, and modulation. Therefore, in the case of a fault in one of these modules, it is possible to replace it quickly and easily. Moreover, with an appropriated control strategy, it is possible to bypass the faulty module without stopping the load, bringing an almost continuous overall availability. All this features make CMI an outstanding power converter. However, one of the greatest limitations of CMI

is utilization of separate DC source for each H-Bridge cell. This not only increases cost but also affects the reliability of the system. This is the key motivation for this dissertation.

In the present work, we have investigated different CMI based topologies with separate and single DC sources and finally proposed a new CMI based configuration with single dc source by using three-phase transformers. The proposed CMI based inverter presented in this thesis is well defined with logical and mathematical approach. Additionally to illustrate the merits, it is compared with traditional multilevel inverters. The feasibility of proposed inverter is demonstrated with different illustrations and confirmed by experimental results. The proposed CMI is well suited for *grid / photovoltaic* and *FACTS* systems. To elevate the application of proposed CMI a shunt active power filter (APF) design is demonstrated. In this case, the goal is to inject, in parallel with the load, compensation current to get a sinusoidal source current. The proposed APF is verified through Matlab-simulation. Finally, Opal-RT verifications are performed to verify the final design.

LIST OF FIGURES

LIST OF TABLES

Chapter 1

Introduction

Research Background

Investigation on Medium and High Power Inverters

Introduction to Classical Inverters (Two-Level Inverters)

Introduction to Multilevel Inverters

Manufacturing companies and overview of multilevel inverters

Motivation

Dissertation Objectives

Dissertation Outline

Chapter 1:

1.1 Research Background

Multilevel inverters have been under research and development for more than three decades and have found successful industrial applications. However, this is still a technology under development, and many new contributions and new commercial topologies have been reported in the last few years. The aim of this dissertation is to group and review recent contributions, in order to establish the current state of the art and trends of the technology to provide readers with a comprehensive and insightful review of where multilevel converter technology stands and is heading. This chapter first presents a brief overview of well-established multilevel inverters strongly oriented to their current state in industrial applications and then centers the discussion on the new multilevel inverters that have made their way into the industry. Multilevel inverters have been attracting increasing interest recently the main reasons are; increased power ratings, improved harmonic performance, and reduced electromagnetic interference (EMI) emission that can be archived with multiple dc levels that are synthesis of the output voltage waveform. In particular multilevel inverters have abundant demand in applications such as medium voltage industrial drives, electric vehicles, and grid connected photovoltaic systems. The present work provides a solution to design an efficient multilevel topology which is suited for medium and high power applications. In the subsequent sections the research background is discussed in detailed. Motivation and objectives are clearly outlined.

1.2 Medium and High Power Inverters

There are different power converter topologies and control strategies used in inverter designs. Different design approaches address various issues that may be more or less

important depending on the way that the converter is intended to be used. The issue of waveform quality is one the important concern and it can be addressed in many ways. In practice capacitors and inductors can be used to filter the waveform [1-2]. If the design includes a transformer, filtering can be applied to the primary or the secondary side of the transformer or to both sides. Low-pass filters are applied to allow the fundamental component of the waveform to pass to the output while limiting the passage of the harmonic components. Thus quality of waveform can be adjusted. Note that, normal inverters always generate very low quality output waveforms. To make the output waveform qualitative, low pass (LC filter) are often added in the circuit. Thus, at this point of time readers might have a question that, why the quality of converter output is low? And why Low pass filter are frequently added in the circuit. Further, what kinds of solutions are available to increase quality of output waveform without losing its efficiency? All this are open problems associated with present day inverters. However, eventually all this will be addressed in this thesis. But at first we try to figure out the converter applications from low power to high power and then we summarize the requirements to meet the high power demand. Finally we try to present the problems and solutions available to meet the high power demand.

Consider Table 1.1, which presents the important applications from low power to high power range. From Table 1.1 it is quite predictable that, power inverters are an enabling technology. They are potentially useful for a wide range of applications like; low power devices, home appliances, electric vehicles, photovoltaic, transport (train traction, ship propulsion, and automotive applications), and energy conversion, manufacturing, mining, and petrochemical applications. The inverters mentioned in Table 1.1 are available in a wide range. Note that, either it may be suited for DC or AC. But, at present industries are in chase

of finding new type of power converter for medium to high power range, moreover it seems to be challenging issues for present generation researchers.

TABLE 1.1

Summary of Power Inverters

	Low Power	Medium Power	High Power
Power Range	Up to 2 KW	2-500 KW	More Than 500 KW
Usual Converter Topologies	ac/dc, dc/dc	ac/dc, dc/dc, dc/ac	ac/dc, dc/ac
Typical Power Semiconductors	MOSFET	MOSFET, IGBT	IGBT, IGCT, Thyristor
Technology Trend	High Power Density, High Efficiency	Small Volume and Weight Low Cost and High Efficiency	High Nominal Power of the Converter high Power Quality and Stability
Typical Applications	 Lower-Power Devices  Home Appliances	 Electric Vehicles  Roof PV	  Transportation Power Distribution Renewable Energy Industry 

Although research pioneers have built a numerous power inverters, but still researchers are in look for a new sort of architecture which can produce high quality waveform with less number of components. In other terms improving power quality is the greatest requirement. By considering above aspects, let us make an outline regarding the demanding aspects of power inverters, particular in Medium and high power range.

1.3 Challenging Aspects in Medium and High Power Inverters

The current energy arena is changing. The feeling of dependence on fossil fuels and the progressive increase of its cost is leading to the investment of huge amounts of resources, economical and human, to develop new cheaper and cleaner energy resources not related to fossil fuels [3]. In fact, for decades, renewable energy resources have been the focus for researchers, and different families of power inverters have been designed to make the integration of these types of systems into the distribution grid a current reality. Besides, in

the transmission lines, high-power electronic systems are needed to assure the power distribution and the energy quality. Therefore, power electronic inverters have the responsibility to carry out these tasks with high efficiency. The increase of the world energy demand has entailed the appearance of new power converter topologies and new semiconductor technology capable to drive all needed power. A continuous race to develop higher-voltage and higher-current power semiconductors to drive high-power systems still goes on. However, at present there is tough competition between the use of classic power converter topologies using high-voltage semiconductors and new converter topologies using medium-voltage devices. Power inverters are an amazing technology for industrial practice powered by electric drive systems. They are potentially helpful for a wide range of applications: transport (train traction, ship propulsion, and automotive applications), energy conversion, manufacturing, mining, and petrochemical, to name a few. Many of these processes have been continuously raising their demand of power to reach *higher production rates, cost reduction* (large-scale economy), and *efficiency* [4].

The power electronics research community and industry have reacted to this demand in two different ways: developing semiconductor technology to reach higher nominal voltages and currents (currently 8 kV and 6 kA) while maintaining traditional converter topologies (mainly two-level voltage and current source inverters); and by developing new converter topologies, with traditional semiconductor technology, known as *multilevel inverters* [5]. The first approach inherited the benefit of well known circuit structures and control methods. Adding to that, the newer semi-conductors are more expensive, and by going higher in power, other power-quality requirements have to be fulfilled, thereby there may be need of additional power filters. Therefore it will be quite feasible to choose to build

a new converter topology based on multilevel concept. This is the challenging issue right now.

1.4 Concept of Classical Inverters (Two-Level Inverters)

At present there is tough competition between the use of classic power converter topologies using high-voltage semiconductors and new converter topologies using medium-voltage devices. This idea is shown in Fig.1.1, where inverters are built by adding devices in series. In past, these inverters are only viable options for medium and high-power applications. But in present scenario, multilevel technology with medium voltage semiconductors are fighting in a development race with classic power inverters using high-power semiconductors, which are under continuous development and are not mature. Although, classical inverters are good for low power applications, but they fail to fill the requirements of high-power levels.

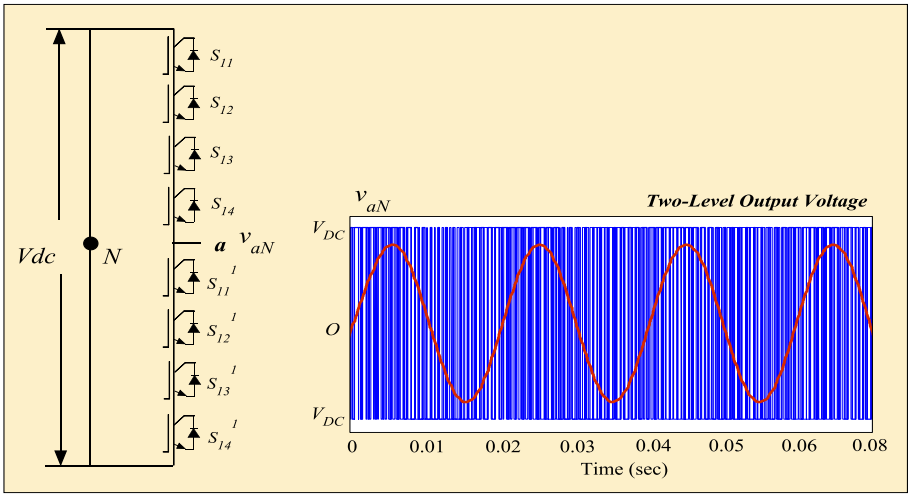


Fig.1.1 Classical converter and output waveform

In view of later, to retrieve the demerits of classical inverters we should know about the multilevel technology and the merits it offer. Multilevel inverters are a good alternative for power applications due to the fact that, they can achieve high power using mature

medium-power semiconductor technology. Practically, multilevel inverters present great advantages compared with conventional and very well-known two-level converter. These advantages are fundamentally focused on improvements in the output signal quality (Voltage & Current) and a nominal power increase in the converter [6].

These properties make multilevel inverters very attractive to the industry and, nowadays, researchers all over the world are spending great efforts trying to improve multilevel converter performances such as the control simplification and the performance of different optimization algorithms in order to enhance the THD [7] of the output signals, the balancing of the dc capacitor voltage [8], and the ripple of the currents. For instance, nowadays researchers are focused on the harmonic elimination using pre-calculated switching functions, harmonic mitigation to fulfill specific grid codes, the development of *new multilevel converter* topologies (hybrid or new ones), and new control strategies [9]. However, before introducing about the multilevel inverters, let's make an overview about the classical inverters and their problems. To address the problems of conventional inverters, one should have an idea about the Medium to high-power range inverters and related challenging issues. Below are some of the facts summarized.

1. At present, application power range of inverter circuits using the basic "inverter leg" building block is vast (<1 kW to 10 MW+)
2. Very large application area is in industrial (PWM controlled induction motor) drives (See Fig.3) are around 3 kW to 100 kW power range. IGBT devices are used almost exclusively in this power range.
3. Recently the application area for these circuits has extended to power levels (>1 MW), Most importantly,

(a) Railway locomotives (1-5 MW)

(b) Ship propulsion (e.g. Frigate 20 MW)

(c) Power systems applications, for example FACTS (Flexible AC Transmission Systems) - see H5CPNW - up to 100 MW+

4. Above all applications use devices like: IGBT (Insulated Gate Bipolar Transistor), GTO (Gate Turn-off Thyristor), IGCT (Insulated Gate Commutated Thyristor). However, design of these high power inverters (MW range) presents serious problems:

   (a) Single devices can't handle the V and I.

   (b) For example a 1 MW drive would be typically supplied at 3.3 kV (UK) or 4.16 kV (US) giving a DC link of 5 to 7 kV. The voltage supplied to the motor is also 3.3 kV (or 4.16 kV).

   (c) Device voltage rating required 8-10 kV - not available.

   (d) Handling high currents by putting devices (or inverters) in parallel is fairly well established. Getting the voltage handling capability remains the problem.

Thus to solve above mentioned problems some of the conventional solutions too available, and solutions are;

1. Using standard converter topologies with devices in series.
2. Using alternative topology inverters which a number of low voltage devices and that have some means for distributing the voltage stress amongst those devices (Multi-level inverters).

Anyhow first case is demonstrated in Fig.1.1. Observe the arrangement (it is also called as classical converter); it uses the semiconductor devices in series [10]. In other sense, by adding devices in series voltage capability is increasing [11]. Somehow with this

arrangement inverters can meet high power demand. But one of the greatest limitations is the output voltage quality. However with classical arrangement converter has the potential to generate only two level output. In fact such kind of waveforms composes with huge harmonic content. Particularly low order harmonics like 3^{rd}, 5^{th}, 7^{th}, .etc. This harmonics drastically affects the equipment performance. Frequently, to suppress such harmonics several low filters are used to improve the quality at the output end. But filter size is still greater in extent if the quality is poor. Additionally, a well known fact is that, designing *Low Pass Filter* is a hectic job and it is bulky in nature too. Plenty of research is going on this subject i.e., to reduce the filter size in the circuits [12-13]. Overall from above prospects we can summarize some of the problems of classical inverters as follows:

(a) The entire DC voltage appears across each switch when it is off. This will be greater than the voltage rating of the individual devices.

(b) The devices will not automatically share the voltage in the off state because of differences in leakage current - high value parallel resistors can be used to overcome this (static sharing).

(c) More seriously, the devices will not share the voltage during switching due to variations in switching speed. Special gate drive techniques and/or special snubbers are required (dynamic sharing). Not well established yet.

(d) Two level output causes very large voltage steps on the load - can be a problem for motor insulation.

(e) Harmonic content (distortion) is larger for a given switching frequency than with multi-level techniques (given in next section)

On the flip side, classical inverters too have finite advantages those are:

a. Standard PWM techniques can be used.
b. Number of power circuit components is less as compared to other (multi-level) circuits.
c. Redundancy can be incorporated (to improve reliability) by using more series devices than actually required - the circuit can then still work if one fails.

However with this demonstration it is clear that conventional inverters have huge drawbacks than merits. So alternative solution to meet the high power demand is through multilevel concept.

1.5 Concept of Multilevel Inverters

Multilevel inverter includes an array of power semiconductor devices and capacitors voltage sources, the output of which generates voltages with stepped waveforms [14-15]. The commutation of the switches permits the addition of the capacitor voltages to obtain high-voltage at the output, while the power semiconductors have to withstand only reduced voltages.

Fig.1.2 shows a schematic diagram of one phase leg of inverters with different numbers of levels, for which the action of power semiconductors is represented by an ideal switch with several positions. Form Fig.1.3, we can observe a two level inverter generates an output voltage with two values (levels) with respect to negative terminal of the capacitor. While the three level inverter generates three voltages, and a nine-level inverter generates a nine level output voltages. In all this cases devices are not arranged in series but they are arranged in such way that, they gain the capability to generate such kind of voltages. Herein, we should remember one important thing i.e. as the number of steps increases in the output waveforms; harmonic content comes down [16]. Thus power quality of such waveforms will

increase drastically. However, in order to generate step kind of waveforms in output side, different *Multilevel* based archetypes are successfully built and verified. But general principle

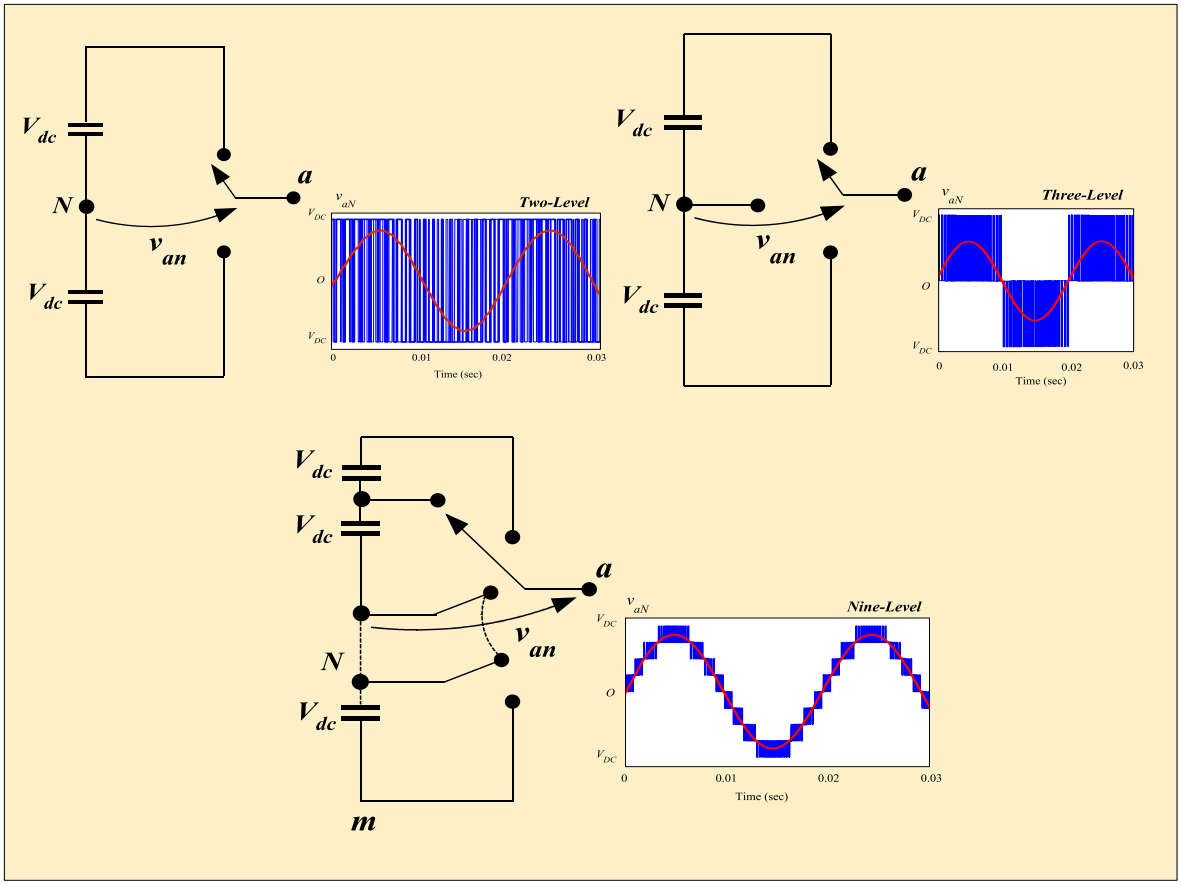


Fig.1.2 Converter output voltage waveforms a) two level b) three level c) nine level

of multilevel inverters is the synthesis of the ac voltage from several different voltage levels on the dc bus. As the number of voltage levels on the input dc side increases, the output voltage adds more steps [17-19], which approach the sinusoidal wave. However, from above thought, to present a general idea about the steps in the output waveform, consider *m* to be the number of steps of the phase voltage with respect to the negative terminal of the inverter, and then the number of steps in the voltage between two phases of the load K is given by equation A and B:

$$K = 2m+1 \quad (1.1)$$

And the number of steps P in the phase voltage of a three phase load in wye connection is

$$P = 2k -1 \quad (1.2)$$

The term multilevel starts with the three-level inverter introduced by the Nabae et al.[15]. However topologically, multilevel inverters are largely divided into many configurations. The most common multilevel converter topologies are the neutral-point-clamped converter (NPC) [15], flying capacitor converter (FC) [18], and Cascade H-Bridge (CHB).

At present these inverters are highly visible in all Medium voltage drives, grid connected systems and FACTS devices. An extensive survey has been done on the multilevel inverters; these are addressed in the next chapter. However, at this point of time it is clear that, multilevel inverters are one of the best option for Medium and high power applications [19]. Now a question may arise; are there any other inverters which are competitive to multilevel inverters? Obviously the answer is yes. Any how to resolve this question and for a better idea, a complete list of high-power inverters are demonstrated in Fig.1.3. However, the main competitors of multilevel technology are: the cycloconverter and load commutated inverters (LCIs).

Other high-power converter topologies like current source and matrix inverters are also observed in the classification. Although they are capable of meeting high power demand, but they are less preferred because of their limited merits. However, some of which have recently found practical application and this content is not discussed in this dissertation as it is mentioned that, study is confined to only multilevel structures. Operating principles,

multilevel waveform generation, special characteristics, modulation schemes, and other information related to the NPC, FC, and CHB are demonstrated subsequently.

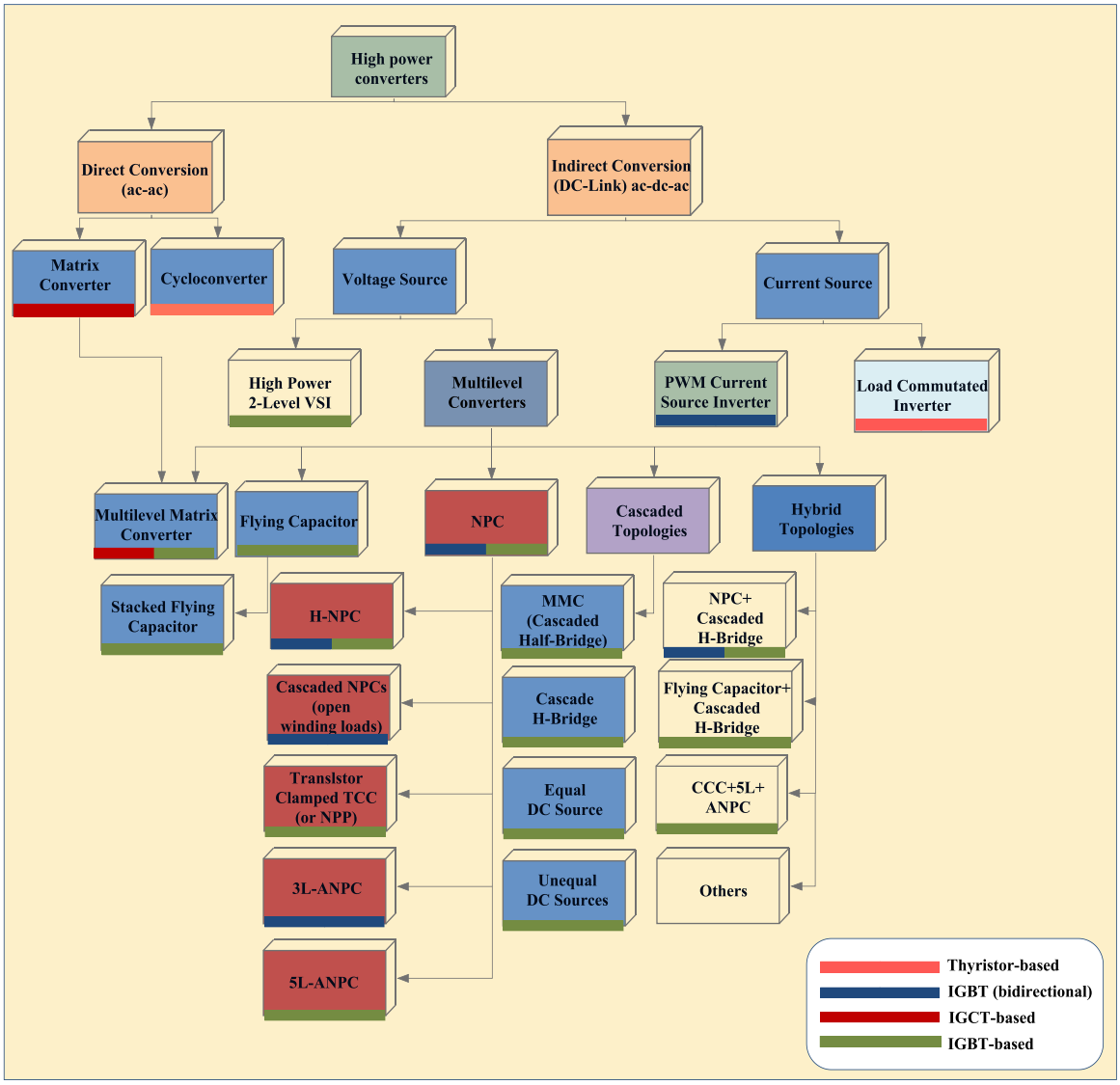


Fig.1.3 Classification of high-power inverters

At first, preliminary studies on multilevel inverters have been performed using three-level inverter that has been proposed by Nabae. In the study, the third level has been constituted by using neutral point of DC line and the topology has been defined as diode clamped (DC) converter [34 35]. Since the first multilevel converter was patented in 1975,

many different multilevel inverter topologies have been introduced and analyzed by different authors. An interesting survey of this kind of device is presented in [36].

Aforementioned Multilevel inverters are power-conversion systems, composed by an array of power semiconductor devices and capacitive voltage sources that, when properly connected and controlled, can generate a multiple-step voltage waveform with variable and controllable frequency, phase, and amplitude. The stepped waveform is synthesized by selecting different voltage levels generated by the proper connection of the load to the different capacitive voltage sources. This connection is performed by the proper switching of the power semiconductors. Then number of levels of a converter can be defined as the number of steps or constant voltage values that can be generated by the converter between the output terminal and any arbitrary internal reference node within the converter. Typically, it is a dc-link node, and it is usually denoted by N and called neutral. To be called a multilevel converter, each phase of the converter has to generate at least three different voltage levels. This differentiates the classic two-level voltage source converter (2L-VSC) from the multilevel family. Some examples of this concept and their respective waveforms for different numbers of levels are already discussed in previous section. However, it is worth to know more about their design in details.

There are many ways to combine power semiconductors and capacitive dc sources to generate multilevel out-put voltages. So for completeness and better understanding of the advances in multilevel technology, it is essential to explore the classic multilevel inverters with performances. Conversely, in order to focus the content of this dissertation on the most recent advances and ongoing research lines, well-established topologies will only be briefly introduced and referred to existing literature. In the following, multilevel topologies will be

referred to those that have extensively been analyzed and documented and have been commercialized and used in practical applications for more than a decade.

In view of later, multilevel technology started with a series-connected H-bridge, which is also known as cascaded H-Bridge converter, in the late 1960s [37]. This was closely followed by low-power development of an FC topology in the same year [38]. Finally, in the late 1970s, the diode-clamped converter (DCC) [39] was first introduced. The DCC concept evolved into the three-level NPC (3L-NPC) converter, we know today as it was proposed in [39]–[42] and can be considered as the first real multilevel power converter for medium-voltage applications. Later, the CHB would be reintroduced in the late 1980s [43], although it would reach more industrial relevance in the mid-1990s [44].

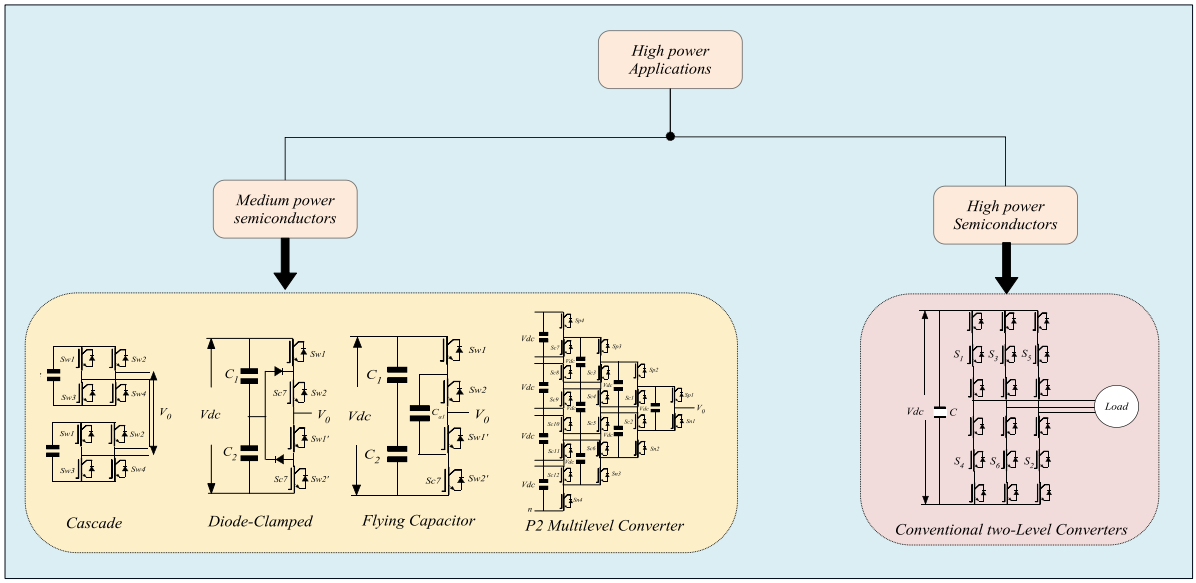


Fig.1.4 Classical two level power inverters versus most common mutlilvel power inverters

In the same way, the early concept of the FC circuit introduced for low power in the 1960s developed into the medium-voltage multilevel converter topology, we know today in the early 1990s [45]. Through the years, the FC has also been reported as the imbricated-cell and multicell converter. The latter is also a name used for the CHB since both are modular

and made by interconnection of power cells. Later, P2 multilevel inverters came into picture in the year 2001 [46]. These four multilevel converter topologies could be considered now as the classic or traditional multilevel topologies that first made it into real industrial products during the last two decades. However, all this structures are demonstrated in Fig.1.4.

Note that, there is not much advancement in p2 architecture. But, research in NPC, FC and CHB are quite good. So our discussion is focused on these three archetypes only. However, principle of operations and discussion of conventional multilevel inverters are discussed in detail.

1.6 A Brief Review of Traditional Multilevel Inverters

1.6.1 Neutral Point clamped Multilevel inverter (NPC-MLI)

An NPC-MLI converter is essentially composed of two traditional two-level VSCs stacked one over the other with some minor modifications. As can be seen in Fig. 1.5, the negative bar of the upper converter and the positive bar of the lower one are joined as one to form the new phase output, whereas the original phase outputs are linked via two clamping diodes to form the neutral point N, dividing the dc-link voltage in two. At this instant, each

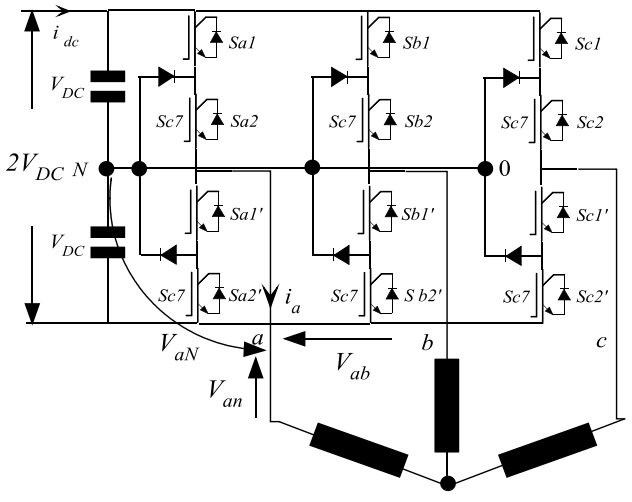


Fig.1.5. Three-level neutral point clamped power circuit

power device has to block only half of the total converter voltage; hence with the same semiconductor technology, the power rating of the converter can be doubled. In addition, the neutral point enables the generation of a zero voltage level, obtaining a total of three different voltage levels. The switching condition of a converter is a set of signals used to control each switching device of the power circuit. They can amend its conduction state and the way the load is connected to the different nodes of the dc side circuit. Therefore, a particular switching state generates an equivalent output voltage level. For the NPC shown in Fig. 1.6, the switching signals are S_{ij}, with the subscript i and j representing the corresponding phase (a, b, or c) and switch number (1 or 2), respectively. Remind that there are only two control

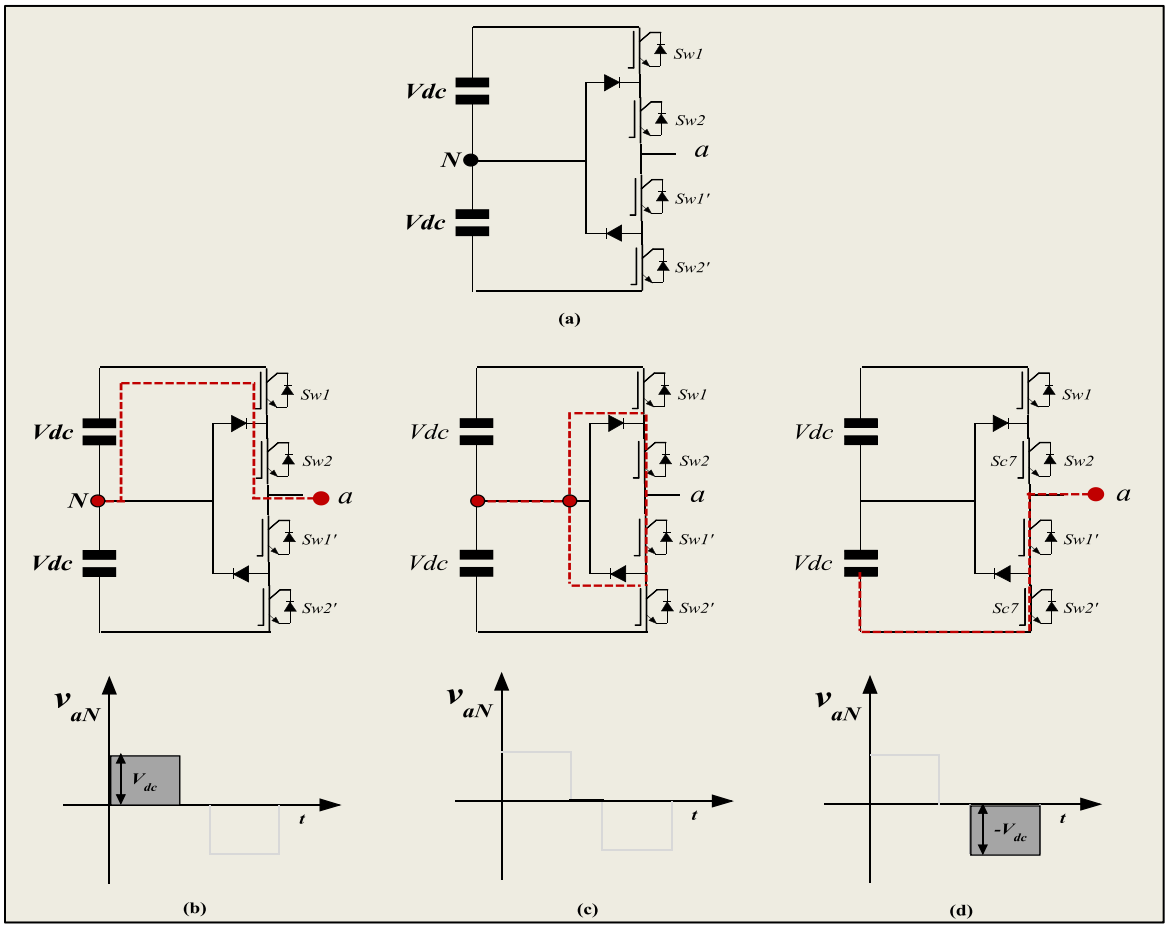


Fig.1.6. Three-level NPC-MLI switching states and corresponding output voltage levels

signals per phase; the other two switches be given inverted gating signals to avoid the dc-link short-circuit. The gate signal is of binary form, representing by **0** for the OFF state of the switch and by 1 for the ON state. Fig. 1.6 shows the three different switching states for one phase of the NPC-MLI and their corresponding output voltage levels. The obtained equivalent circuit is highlighted to demonstrate how the output node **a** is associated to the positive, neutral, and negative nodes of the dc side circuit. Note that one of the four binary combinations (Sw1; Sw2) = (1, 0) is not used since it does not provide a current flow path for the load. The same switching states can be applied for phases b and c. The NPC-MLI structure can be extended to higher power rates and more output voltage levels by adding additional power switches and clamping diodes to be able to block higher voltages. Fig. 1.6 illustrates a three-phase three-level NPC-MLI inverter. Here the name diode clamped (DC) makes more sense, since there are more voltage-level clamping nodes than only connected to the neutral N. As far a concern the number of clamping diodes needed to share the voltage which is enhanced dramatically. This fact, together with the increasing difficulty to control the dc-link capacitor unbalance, has kept the industrial approval of the NPC topology up to three levels only.

1.6.2 Flying Capacitor Multilevel Inverter (FC-MLI)

The FC-MLI topology is in some way similar to the NPC-MLI, with the main difference being that the clamping diodes are replaced by flying capacitors [62], as can be seen in Fig. 1.7. Here the load cannot be directly connected to the neutral of the converter to

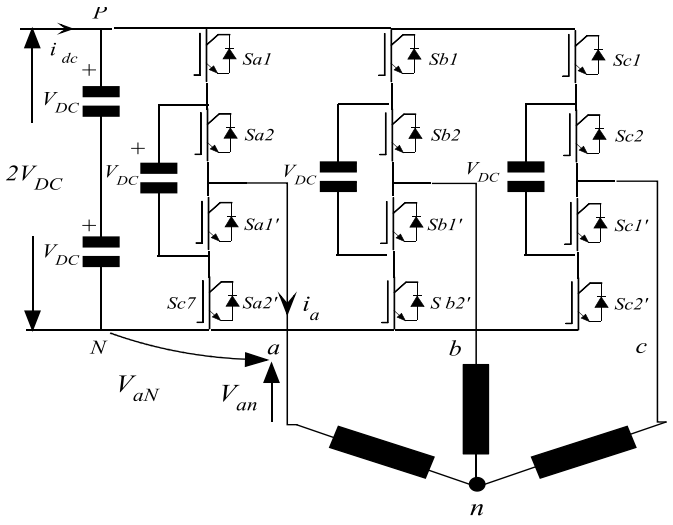


Fig. 1.7 Three-level flying capacitor power circuit.

generate the zero voltage level. Instead, the zero level is obtained by connecting the load to the positive or negative bar through the flying capacitor with opposite polarity with respect to the dc-link. Like with the NC-MLI, only two gating signals are necessary per phase to avoid dc link and flying capacitor short- circuit.

However, in the FC, the inverted gating signals are related to different switching devices. The switching states and their equivalent power circuits with the corresponding output voltage levels are illustrated in Fig. 1.8.

Another difference with the NPC is that the four combinations of Sw1; Sw2 are allowed. Only three are shown in Fig. 1.8. The middle circuit in Fig.1.8 shows (S_{w1}; S_{w2}) = (1,0) which generates the zero level. The same level is obtained with (S_{w1}; S_{w2}) = (0, 1). This property is known as voltage level redundancy and can be used for control or optimization purposes. Perhaps the key and most important difference with the NPC-MLI topology is that the FC-MLI has a modular structure and can be more easily extended to attain more voltage levels and higher power rates.

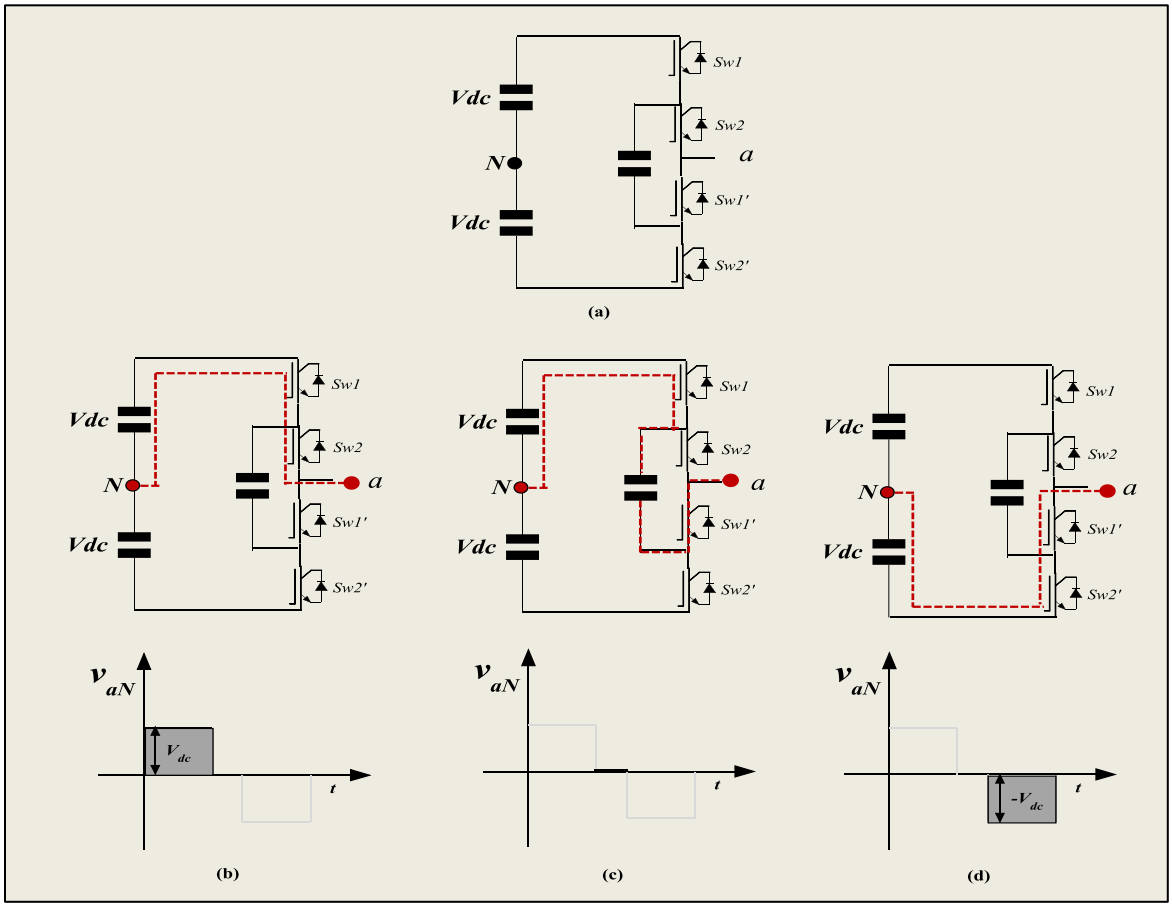


Fig. 1.8 Three-level FC-MLI switching states and corresponding output voltage levels

1.6.3 Cascaded H-Bridge Multilevel Inverter (CHB-MLI)

CHB-MLIs formed by the series connection of two or more single-phase H-bridge inverters, hence the name [63]. Each H-bridge corresponds to two voltage source phase legs, where the line–line voltage is the inverter output voltage. Therefore, a single H-bridge converter is able to generate three different voltage levels. Each leg has only two possible switching states, to avoid dc-link capacitor short-circuit. Since there are two legs, four different switching states are possible, although two of them have redundant output voltage. Fig. 1.9 shows the three

different output voltage levels and their corresponding equivalent circuits. The zero level can be generated connecting the phase outputs to the positive or the negative bars of the inverter.

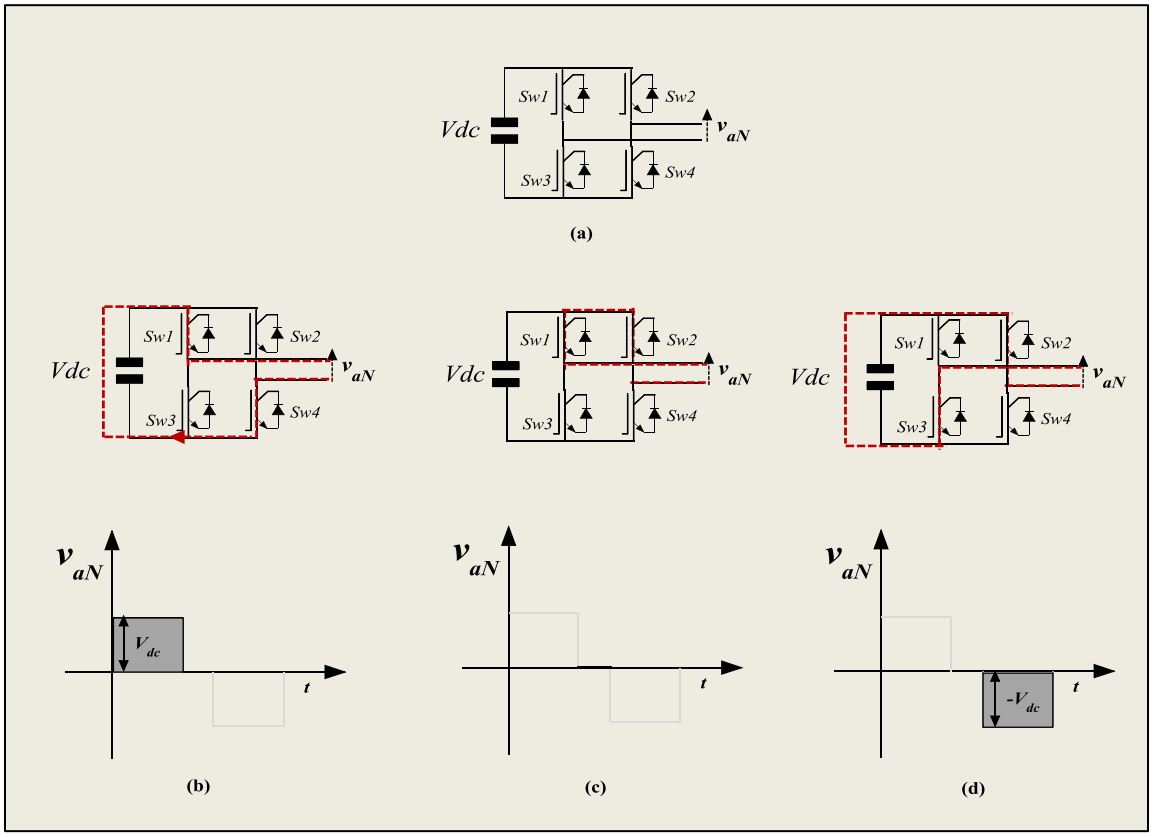


Fig. 1.9 Three-level CHB-MLI switching states and corresponding output voltage levels

When two or more H- bridges are connected in series, their output voltages can be combined to form different output levels, increasing the total inverter output voltage and also its rated power. The complete thesis is devoted for this archetype and in depth details of architecture is articulated in subsequent sections.

1.7 Multilevel Topologies and Manufacturing companies

The inverters are commercialized by several manufacturers in the field, offering different power ratings, front-end configurations, cooling systems, semiconductor devices, and control schemes, among other technical specifications. There are a number of high-power drive manufacturers around the world, including ABB (Switzerland), Siemens

(Germany), Toshiba (Japan), Rockwell Automation (Canada), General Electric (US), AS1 Robicon (US) and Alstom (France). These companies use various power converter technologies, For instance, ABB produces three-level neutral point clamped inverter fed drives, Rockwell manufactures GCT current source inverter based drives, Robicon promotes cascaded H-bridge multilevel inverter technology, Toshiba uses multilevel NPC/H-bridge hybrid inverters, and Alstom is developing flying-capacitor based multilevel inverter. However, for completeness some of the manufacturer information is mentioned in Table 1.1. Further, the most relevant parameters and ratings for each of these classic multilevel topologies that are published in recent past are listed in Table 1.2. The parameters for each category are given for the different manufacturers. Meanwhile, their corresponding reference is given at the table. As can be observed from the Table 1.2, the 3L-NPC-MLI and the CHB-MLI are the most popular multilevel topologies used in the industry. It is not straightforward or fair to compare the commercially available 3L-NPC-MLI with the 7L to 17L-CHB-MLI listed in Table 1.2 since the first will have worse power quality and the second will have a more complex circuit structure. However, some evident differences between them can be concluded from Table II.

1) The NPC-MLI features medium-/high-voltage devices [integrated gate-commutated thyristor (IGCT) and medium voltage/high-voltage insulated-gate bipolar transistors (IGBTs)], whereas the CHB exclusively uses low-voltage IGBTs (LV-IGBTs).

2) The CHB-MLI reaches higher voltage and higher power levels.

3) The NPC-MLI is definitely more suitable for back-to-back regenerative applications. The CHB-MLI needs substantially higher number of devices to achieve a regenerative option (a three-phase two-level voltage source inverter (VSI) per cell).

4) The CHB-MLI needs a phase-shifting transformer usually to conform a 36-pulse rectifier system. This is more expensive but improves input power quality.

TABLE 1.1

Manufacturing Companies of Classical and Multilevel Inverters

Converter configuration	Solid State Device	Power Range	Manufacturer
Two-level Inverter (VSI)	IGBT	1.4 MVA-7.2 MVA	Alstom (VDM5000)
NPC Inverter (NPC VSI)	GCT	0.3 MVA 5 MVA 3 MVA 27 MVA	ABB (ACS 1000) (ACS 6000)
	GCT	3 MVA-20 MVA	General Electric (Innovation Series MV-SP)
	IGBT /IGCT	0.6 MVA-0.9 MVA	siemens (SIMVERT-MV)
	IGBT	0.4 MVA-4.5 MVA	GE-Toshiba (Dura-Bilt5 MV)
	GTO	2.5 MVA-18 MVA	Toshiba (Tosvert- μ/S650)
Cascaded H-Bridge Inverter (VSI)	IGBT	0.3 MVA-22 MVA	Robicon (Perfect harmony)
	IGBT	0.5 MVA-6 MVA	Thshiba (TOSVERT-MV)
	IGBT	0.45 MVA-7.5 MVA	General Electric (Innovation MV-GP Type H)
NPC/H-Bridge	IEGT	6 MVA-26 MVA	GE-Thosbhiba (Dura-Bilt5 MV)
Flying Capacitor Inverter (VSI)	IGBT	0.3 MVA-8 MVA	Alstom (VDM6000 Symphoney)

5) The NPC-MLI has a simpler circuit structure, leading to a smaller footprint.

6) Although both topologies generate the same amount of levels, when using the same number of power switches, commercially available CHBs have more output voltage levels (up to 17, compared with three for the (NPC-MLI). Hence, lower average device switching - frequencies are possible for the same output voltage waveform quality. Therefore, air cooling

and higher fundamental output frequency can be achieved without derating and without use of an output filter. Further, in preceding section only single phase archetype are clarified with principle of operation. But to have better idea about the classical inverter and traditional multilevel inverters their three-phase architectures with simulated waveforms is presented Fig. 1.10. This figure describes how a multilevel inverter generates voltage waveforms for different power ranges.

TABLE 1.2

Traditional Multilevel Topologies and Their Commercial Ratings

Parameter	Multilevel Topology		
	3L-NPC	CHB	4L-FC
Max.Power	27 MW [a], 31.5 MVA [b], 40 MVA [c], 44 MW [d], 33.6 MW [e], 37 MW (f, i), 27 MVA [h], 10 MW [n]	120 MW [b], 15 MW [c], 5.6 MW [g], 10 MVA [j], 11.1 MVA [k], 6 MVA [l], 6250 KVA [m]	2.24 MW [o]
Output Voltage [KV]	2.3/3.3/4.16 [a,b], 2.3/3.3/4.16 [d, f, h, n], 3.3/6.6 [e]	2.3-13.8 [b], 3.3/6.6 [c,l], 2.3/4.16/6/11 [g], 3/6/10 [j], 3/4/6/10 [k], 3/3.3/4.16/6/6.6/10 [m]	2.3/3.3/4.16 [o]
Max.Output freq. [HZ]	82.5 [a], 250 [b], 90 (3), 140 [d,n], 300 [e], 120 (6), 100 [h,i]	330 [b], 120 [c,g, k-m], 50 [j]	120 [o]
Diode front end[# pulses]	12/24 [a-e, h], 24 [f], 12/18 [i], 12/24/36 [n]	18/36 [b,c,l], 30 [g], 36 [k], 24/30/42/48 [m]	18/24/36 (diode+SCR) [o]
Active front end option	3L-NPC in back-to-back [a-e,h,n]	3-Phase VSI per cell [j]	4L-FC in back-to-back [o]
Power semiconductor	IGCT [a,b,d,h], MV/HV-IGBT [b,e,f,h,i,n], IEGT [c,h]	LV-IGBT [b,c,g,j-m]	MV-IGBT [o]
Cooling system	air/water [a,b,c,d,n], water [c,e], air [i]	air/water [b,m], air [c,g,k,l]	air [o]
Modulation Method	PWM [b-f, n], SHE [c,i], SVM [h,i]	PS-PWM [b,c,g,j-m]	PS-PWM [o]
Voltage levels	3	9/13, 7/13, 11 [g], 7/11/13/19 [j], 13 [k], 9/1115/17 [m]	4 [o]
Power cells	-	4/6 [2], 3/6 [c,l], 5 [g], 3/5/6/9 [j], 6 [k], 4/5/7/8 [m]	3 [o]

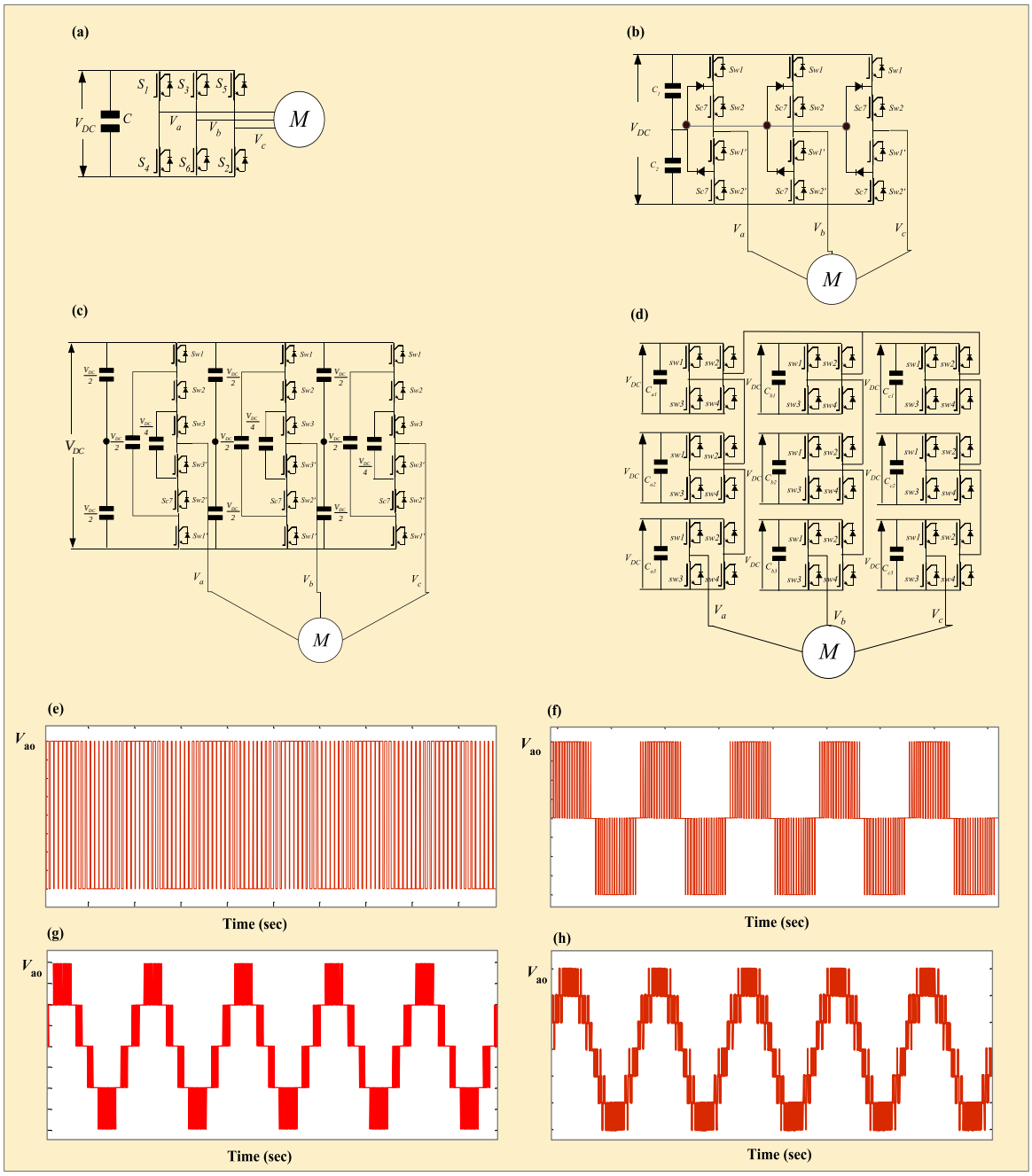


Fig. 1.10. Topologies and phase voltages of the conventional two-level and multilevel voltage source inverters. (a) Two-level VSI (b) Three-level NPC-MLI inverter. (c) Five-level FC-MLI inverter. (e) Performance of two-level VSI. (f) Performance of three-level NPC-MLI. (g) Performance of five-level FC-MLI Inverter. (h) Performance Seven-level CHB-MLI inverter

Generally speaking, the medium-voltage range is considered in the power converter industry from 2.3 to 6.6 kV and high power in the range of 1–50 MW [63]. In any of this range these inverters can be easily expandable.

While distinguishing the three most significant topologies for specific applications in terms of the losses and the output voltage quality [64]–[65], the 3L-NPC-MLI has become well recognized architecture because of a simple transformer rectifier power circuit structure, with a lower device count when considering both the inverter and rectifier, and less number of capacitors. Although the NPMLI structure can be extended to higher number of levels, these are less attractive because of higher losses and uneven distribution of losses in the outer and inner devices [66]. In particular, the clamping diodes, which have to be connected in series to block the higher voltages, introduce more conduction losses and produce reverse recovery currents during commutation that influence the switching losses of the other devices even more. Moreover, dc-link capacitor voltage balance becomes unattainable in higher level topologies with a passive front end when using conventional modulation strategies [67]–[69]. In this case, the standard multilevel stepped waveform cannot be retained, and higher *dv/dts* (more than one-level transitions) is necessary to balance the capacitors for certain modulation indexes. On the other hand, the CHB-MLI is well suited for high-power applications because of the modular structure that enables higher voltage operation with classic low-voltage semiconductors. The phase shifting of the carrier signals moves the frequency harmonics to the higher frequency side, and this, together with the high number of levels, enables the reduction in the average device switching frequency ($\leq$ 500 Hz), allowing air cooling and lower losses. However, it requires a large number of isolated dc sources, which have to be fed from phase-shifting isolation transformers, which are more expensive and bulky,

compared with the standard transformer used for the NPC-MLI. Nevertheless, this has effectively been used to improve the input power factor of this converter, reducing input current harmonics. Although the FC-MLI is modular in structure, like the CHB-MLI, it has found less industrial penetration, compared to the NPC and CHB, mainly because higher switching frequencies are necessary to keep the capacitors properly balanced, whether a self-balancing or a control-assisted balancing modulation method is used (e.g., greater than 1200 Hz) [66]. These switching frequencies are not feasible for high-power applications, where usually they are limited in a range of 500–700 Hz. This topology also requires initialization of the FC voltages.

1.8 Merits of Multilevel Inverters

Till now we have distinguished about most prominent multilevel architectures. Let us draw our attention on multilevel merits over conventional archetypes. In reality, multilevel inverter has numerous merits over a conventional two-level converter that uses high switching frequency pulse width modulation (PWM). The striking features of a multilevel converter can be briefly summarized as follows.

1. *Staircase waveform quality*: Multilevel inverters not only can generate the output voltages with very low distortion, but also can reduce the dv/dt stresses; therefore electromagnetic compatibility (EMC) problems can be reduced.
2. *Common-mode (CM) voltage*: Multilevel inverters produce smaller CM voltage; as a result, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. Furthermore, CM voltage can be eliminated by using advanced modulation strategies such as that proposed in [60].
3. *Input current*: Multilevel inverters can draw input current with small distortion.

4. *Switching frequency*: Multilevel inverters can operate at both fundamental switching frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency.

Multilevel inverters do have some disadvantages. One particular drawback is the greater number of power semiconductor switches are required. Even though lower voltage rated switches can be utilized in a multilevel converter, each switch requires a related gate drive circuit. This may cause the overall system to be more expensive and complex. But significant merits over conventional two-level inverters outweigh the demerits of multilevel inverters.

1.9 Motivation

The present day's multilevel concept seems to be an alternative, economical and efficient solution for medium and high power application. In-fact, for a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly [47]. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations such as laminators, mills, conveyors, pumps, fans, blowers, compressors, and so on. As a cost effective solution, multilevel converter not only achieves high power ratings, but also enables the use of low power application in renewable energy sources such as photovoltaic, wind, and fuel cells which can be easily interfaced to a multilevel converter system for a high power application.

The most common initial application of multilevel inverters has been in traction, both in locomotives and track-side static inverters [48-49]. More recent applications have been for power system inverters for VAR compensation [50] and stability enhancement [51], active filtering [52], high-voltage motor drive [53], high-voltage dc transmission [54], and most recently for medium voltage induction motor variable speed drives [55]. Many multilevel

converter applications focus on utility interface for renewable energy systems [43], flexible AC transmission system (FACTS) [56, 61].

The inverters in such application areas as stated above should be able to handle high voltage and large power. For this reason, two-level high-voltage and large-power inverters have been designed with series connection of switching power devices such as gate-turn-off thyristors (GTOs), integrated gate commutated transistors (IGCTs) [57], and integrated gate bipolar transistors (IGBTs) [58], because the series connection allows much higher voltages. At the same time**,** the series connection of switching power devices has big problems [59]**,** namely, non equal distribution of applied device voltage across series-connected devices that may make the applied voltage of individual devices much higher than blocking voltage of the devices during transient and steady-state switching operation of devices.

As alternatives to effectively solve the above-mentioned problems, several circuit topologies of multilevel inverter and converter have been researched and utilized. Fig.2.1 shows some of the most common multilevel topologies and conventional (two-level) high power inverters. In view of latter, the output voltage of the multilevel inverter has many levels synthesized from several DC voltage sources. Indeed, the quality of the output voltage is improved as the number of voltage levels increases, so the quantity of output filters can be decreased.

However, from previous discussion it is clear that, *Multilevel Level* inverters are majorly visible in medium voltage drives, grid-connected photovoltaic/wind-power generators and FACTS devices (DVR, STATCOM, UPQC, and UPFC), etc. As far as concern, NPC, FC and CHB are visible in different type of applications. But from the literature it is noted that CHB has been quite noticeable in every application. The major

strengths of the inverters are; (1) Extremely reliable, (2) modularized circuit layout and packaging is possible because each H-bridge cell has the same structure, (3) it does not need extra clamping diodes or voltage balancing capacitors, and (4) it requires the reduced number of components to achieve the same number of output voltage levels among the conventional multilevel inverters. However, it needs separate dc sources for real power conversions, and thus its applications are likely to be limited due to this fact. Moreover, an instantaneous peak value of the ac output voltage could not exceed the sum of every individual input dc voltage source. Therefore, a case where it needs to supply with high voltage output from such low voltage, it requires additional H-bridge cells or step-up transformers if H-bridge cells to match the voltage magnitude between the low dc voltage and the high ac voltage, of cause, avoiding the transformer has the additional benefits of reducing cost, size, weight and complexity of the inverter. However, the removal of the transformer and hence its galvanic isolation capability has to be considered carefully. On flip side, limitation of CHB is usage of separate dc source for each H-bridge. But, research pioneers are in hunt of finding solution to this problem. In fact, multilevel inverters with single dc sources operation is a burning issue. This dissertation is devoted to this issue. In the present work, we have investigated different multilevel level inverters. Later we have carried a research work on cascade multilevel inverter (CMI) with single dc source. Finally we proposed a CMI **with** single dc source by employing three-phase transformers. The proposed multilevel inverter is well suitable for grid-connected photovoltaic/wind-power generators and FACTS devices. Herein, the proposed CMI is particularly designed for *Active Power Filter* (APF). Motivations behind this aspect are given below.

Nowadays, most popular word in power quality improvement techniques is active power filters (APFs) [23-25]. These APF's can be used as a practical solution to solve the problems caused by the lack of electric power quality, EPQ. In present days, the emerging technology of power-electronic devices and the new developments in digital signal processing (DSP) , Field programming gate array system (FPGA) have made possible its practical use [33]. These power filters can fully compensate the nonlinear loads of electrical power systems: harmonics, reactive power, unbalances, *etc*. There are many configurations of APFs, from shunt and series connection to hybrid passive-active filters [26]. The target is to optimize the design using the advantages of each filter with the different configurations. However, for any APF, voltage source converter (VSC) is the backbone. Indeed a perfect VSC can improve APF performance significantly [27].

In the recent past [28-30] numerous APF configurations have been designed with classical (two level) inverters. However, classical inverters have draw back that their rating is sometimes very close to load (up to 80%) in some typical applications. Thus classical inverters fail to operate in high power occasions. Although classical inverters can increase their rating by connecting devices in series but such arrangement doesn't provide complete solutions. Further, classical converter suffers from high switching losses, large output filters, increased *dv/dt* and quality problems. In spite of classical archetypes, in recent multilevel based VSC configurations are gaining their importance because of their promising features [31]. Recent surveys signify multilevel voltage-source inverters provide a cost-effective solution in the medium-voltage energy management market. Multilevel inverters are expectantly good and have been widely accepted by researcher and industries. Applications of multilevel inverters are vast and they have been successfully adapted to chemical, oil, and

liquefied natural gas (LNG) plants, water plants, marine propulsion, power generation, energy transmission, and power-quality devices.

Although different multilevel converter exits, cascade multilevel inverter is one of the productive topology from multilevel family. Additionally, CMI feature a high modularity degree because each inverter can be seen as a module with similar circuit topology, control structure, and modulation. Therefore, in the case of a fault in one of these modules, it is possible to replace it quickly and easily. Moreover, with an appropriated control strategy, it is possible to bypass the faulty module without stopping the load, bringing an almost continuous overall availability. All this features make CMI [32] an outstanding power converter.

In present work, we have investigated different CMI based topologies and finally we proposed CMI based configuration with three-phase transformers. However, ultimate goal of the work is to study an APF with proposed VSC.

The proposed VSC based converter presented in this research work is well defined with logical and mathematical approach. Additionally it is compared with conventional multilevel inverters. The feasibility of proposed converter demonstrated with different illustrations and confirmed by simulation and experimental results.

Further shunt APF design is demonstrated with propose VSC. In this case, the goal is to inject, in parallel with the load, a compensation current to get, *e.g.*, a sinusoidal source current. Eventually, at the end of the section, practical design considerations are presented. The APF parameters are justified. The proposed filter is issued in a simulation platform to adjust the component values.

1.10 Dissertation Objectives

From the preceding discussion, the dissertation objectives may outline as follows:

- To develop new multilevel based VSC configuration that can optimize size and enhance the performance and improves the power quality aspects.
- Developed multilevel based VSC to facilitate increased range of output-voltage amplitude changes, and at the same time it gains the potential to increase quality of output voltage and input currents, ability to decrease transformers count, elimination of the lower order harmonic component without using additional filters, easy adaptation to medium and high power applications, increased output voltage levels, reduced number of components, usage of single dc source, complete elimination of common-mode disturbances, compact in size (when compared to other CMI based topologies), effective operation beneath lower modulation indexes, low individual switching frequency etc.
- Proposed CMI based multilevel inverter with different switching techniques are realized with, Fundamental switching, SHEPWM, Sinusoidal PWM.
- Prototype verification of proposed CMI with different switching techniques.
- Finally design of Active power filter with proposed CMI.
- Proposed filter is verified with Real time digital simulator.

1.11 Dissertation Outline

To analyze the performance and effectiveness of the cascaded multilevel inverter (CMI) by employing three-phase transformers the following five contributions are proposed in this dissertation:

1. Importance of CMI is investigated

2. Design of CMI with single DC source is investigated.
3. Limitation of Conventional CMI based architectures is presented.
4. Further, Proposed CMI with single dc source by employing three-phase transformers is demonstrated.
5. Design of Active power filter (APF) with proposed CMI is presented.
6. Finally, Future work and discussion is presented

Based on the flow of the contributions, this dissertation is divided into five chapters.

Chapter 1 Provides the brief introduction about multi-level inverters.

Chapter 2 The literature written about multilevel VSI's are discussed. All published VSI topologies are categorized based on their structures. Further, multilevel manufacturing company is demonstrated. In addition, the topologies and operation principles of different types of multilevel inverter are discussed and finally Importance of CMI is explored and different switching techniques are demonstrated.

Chapter 3 CMI with single DC source performance is explored. Particular attention is focused on merits and demerits of CMI with single DC sources. Applications of presented topologies are also demonstrated in detail.

Chapter 4 The proposed CMI with single dc source by employing three-phase transformers are introduced. The proposed CMI is verified with mathematical issues. Prototype verification is carried out with three major switching techniques namely; Fundamental switching, Selective harmonic elimination (SHEPWM), sinusoidal PWM. Finite comparison is carried out among the switching techniques. Finally the advantages of the proposed CMI with sinusoidal PWM are demonstrated.

Chapter 5 Design of active power filter with the proposed CMI is presented. Verifications using Real time digital simulator is presented.

Chapter 6 Discussion and future work is presented.

Chapter 2

Cascade Multilevel Inverter

Importance of Cascade Multilevel Inverter

Applications of Cascade Multilevel inverter

Modulation Techniques for Cascade Multilevel inverters

Performance of a Cascade Multilevel inverter

Summery

Chapter 2

Although it is an enabling and already proven technology, multilevel converters present a great deal of challenges and even more importantly, they offer a wide range of possibilities that their research and development is still growing in depth and width. Researchers all over the world are contributing to further improve energy efficiency, reliability, power density, simplicity, and cost of multilevel converters, and broaden their application field as they become more attractive and competitive than classic topologies. Recently, many publications have addressed multilevel converter technology and stressed the growing importance of multilevel converters for high-power applications. By considering all this previous publications an in-depth verification is carried out on ***cascade multilevel inverter****. In the previous chapter evaluation of high power converters are demonstrated. Moreover, concept of multilevel inverters is also introduced. In this chapter an in-depth investigation on cascade multilevel converters is carried out with experimental verifications. Later in Section 2.1 importance of cascade multilevel inverter is studied. Further, section 2.2 studies the applications of CMI. Section 2.3 provides the details of most important switching techniques which are adopted for CMI. Further, section 2.4 presents the performance verification for CMI with separate DC source with different switching technique. Finally, the Challenging issues for CMI with single DC are exclusively presented in last section.*

2.1. Importance of Cascade Multilevel Inverter

In previous chapter a brief review is done on NPC-MLI, FC-MLI and CHB-MLI. However, on comparing these three commercial topologies of multilevel voltage-source inverters, cascade multilevel inverter reaches the higher output voltage and power levels (13.8 kV, 30 MVA) and the higher reliability due to its modular topology. Cascade

multilevel inverters are based on a series connection of several single-phase inverters. This structure is capable of reaching medium output voltage levels using only standard low-voltage mature technology components. Typically, it is necessary to connect three to ten inverters in series to reach the required output voltage. These converters also feature a high modularity degree because each inverter can be seen as a module with similar circuit topology, control structure, and modulation [70]. Therefore, in the case of a fault in one of these modules, it is possible to replace it quickly and easily. Moreover, with an appropriated control strategy, it is possible to bypass the faulty module without stopping the load, bringing an almost continuous overall availability [71]. Numerous publications have been visible in the literature, particularly on this architecture. However, research on cascade multilevel inverter is a hot topic in multilevel based structures. So it's feasible to know the reason behind its significance.

In general inverters are compared in terms of feasibility of their utilization and applications. According to the MIL-HDBK-217F standards, the reliability of a system is indirectly proportional to number of its components, consequently less the components more reliable is the system [72]. Therefore, let's make the component verification of above mentioned inverters, so that it would be clear about the issues like; switching losses, reliability and cost factor. Compared to m-level DC-MLI, FC-MLI uses *m-1* capacitors on the dc bus, the CMI uses only *(m-1)/2* capacitors for same *m-level.* Clamping diodes are not required for FCMI and CMC. But balancing capacitors are must for FCMI. But for CMI such balancing – capacitors are completely absent. However, this is summarized in Table 2.1. After comparing CMI with DC-MLI, and FC-MLI, CMI requires least number of components and its dominant advantage is circuit layout with flexibility and outstanding

availability due to their intrinsic component redundancy. Due to these features, the cascade multilevel inverter has been recognized as an important alternative for *power market*.

TABEL 2.1

Comparison of Traditional Multilevel Topologies

Converter Type	DC-MLI	FC-MLI	CMI
Main switching	*(m-1)*2*	*(m-1)*2*	*(m-1)*2*
Main diodes	*(m-1)*2*	*(m-1)*2*	*(m-1)*2*
Clamping diodes	*(m-1)*(m-2)*	*0*	*0*
Balancing capacitors	*0*	*(m-1)*(m-2)/2*	*0*
DC Bus Capacitors	*(m-1)*	*(m-1)*	*(m-1)/2*

2.2 Applications of Traditional Cascade Multilevel Inverter

Although traditional cascade multilevel inverter suffers with separate dc sources but the applications of traditional CMI's are vast. In fact this is the only architectures which have been noticed in every application. Fig.2.2 presents complete details of applications and for the sake of simplicity some of the prominent applications are mentioned below.

2.2.1 Traction

Traction systems need a rectification stage of a high voltage low-frequency ac power from the catenary and a fully controllable inversion stage to feed the traction motors. MMCs have been proposed to be used as an interface between the catenary voltage and low-voltage motor drives. The configuration used in [73] connects a single-phase line of 15 kV/16.7 Hz to three-phase 600 V induction motor drives using an MMC and a medium-frequency transformer. Classical cascade multilevel inverters have also been proposed as a part of a power-quality compensator to reduce harmonics, reactive power, negative sequence, and the volatility of the load [74]. Applications of cascade inverters on electric vehicles have been found in [75],

where a back-to-back multilevel cascade topology is proposed, and in [76-77], where a cascade inverter with floating dc link is used as an inductor less boost inverter.

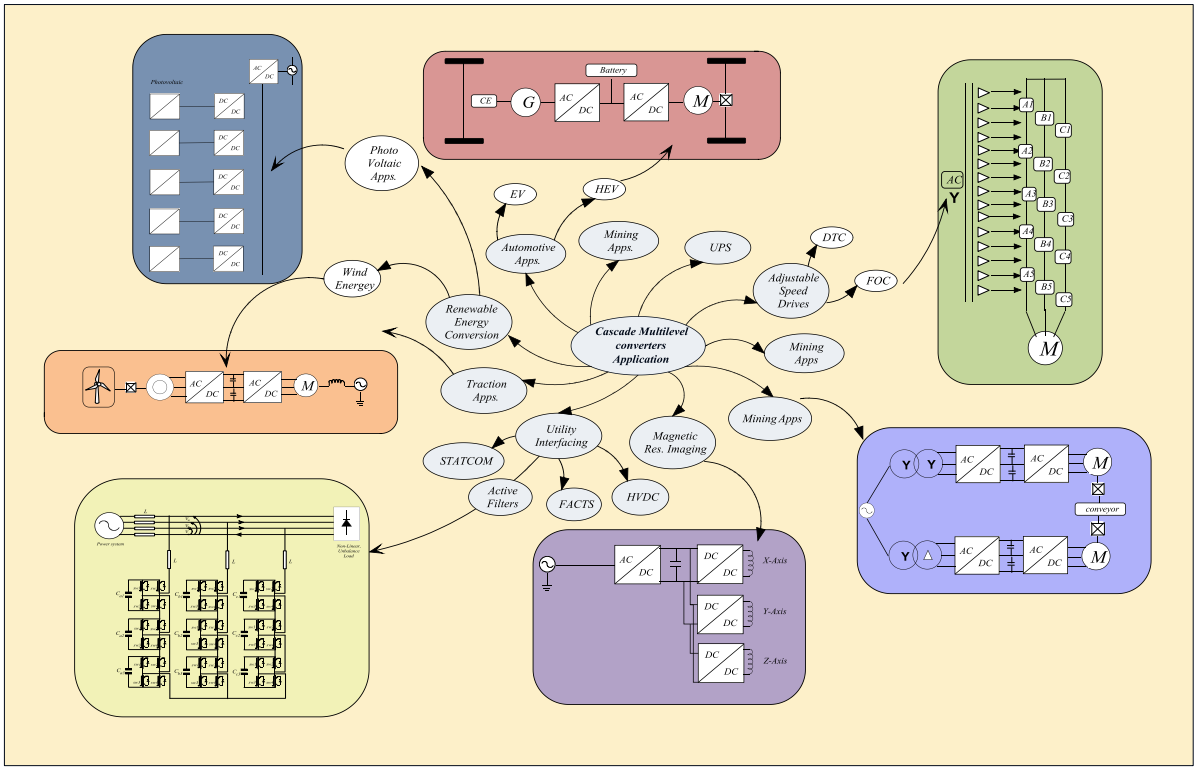


Fig. 2.1 Cascade multilevel converter applications

2.2.2 LNG Plant

The Liquid Natural Gas (LNG) plant presents a cyclic behaviour during the year, monitoring the turbine from the energy station in summer and reversing the power direction in winter when the energy consumption is higher. The use of a compressor directly connected to a gas turbine leads to an efficiency of 25%, due to the low efficiency of the turbine (approximately 30%). In fact combination of synchronous motor and a cascade multilevel regenerative converter, the efficiency has been improved to 36%. Due to the high power involved in this system (45 MW) and the bidirectional power flow, it is necessary to use a high-power converter with regeneration capability [22]. The cascade multilevel inverter emerges as the appropriate choice, considering also its extremely high availability. Cascade

inverters can minimize the maintenance effect in the production cycle, increasing the mean time between failures and, at the same time, reducing the maintenance work duration.

2.2.3 Pumps and Fans

Pumps and fans are intensively used in almost all industry sectors. High-voltage high-power pumps and fans are used in water plants, oil and gas plants, cooling systems, geothermal and nuclear power plants, underground mining, furnaces and boilers, and so on. The use of cascade inverters to drive these devices could lead to an important efficiency improvement, because they typically run with variable speed at partial load. The use of variable speed drives, instead of dampers and throttling valves, to control the flow speed can reduce drastically the amount of power required. Fig. 2.1 shows an industrial fan application, where a 1-MW, 13.8-kV induction motor is driven by a converter connected directly to the distribution system. The distance from the drive and the motor is about 800 m. The configuration shown in [100] presents the problem of voltage resonances at the motor terminals due to high-voltage variations over the long cables, requiring an *LC* filter between the converter and the load. However, if a CHB inverter is used, the voltage variations are greatly reduced, and the filter is also smaller if any.

2.2.4 STATCOM

One of the best suited applications for cascade multilevel inverters is the power quality devices, like STATCOMs and universal power quality conditioners [78]. These devices are connected directly to medium-voltage networks, as shown in Fig.2.1, and do not require the injection of active power in a nominal operating point. To accomplish with the first requirement, it is possible to connect as many inverters as required to reach the operating voltage, without the use of a transformer. The second requirement determines a

simplification of the cascade topology, which does not require a rectifier and input transformer stage, significantly reducing its costs. A combination of modulation and control techniques can provide floating and balanced dc voltages [79], [80]. Another alternative shown in [81] is to use photovoltaic cells to provide the floating dc voltages. The mentioned topology requires additionally a maximum power point tracker strategy to optimize the use of photovoltaic cells. However, in this case, it is possible to temporarily inject active power to the load. Additionally, according to recent survey CMI are extensively used in compressors (82%), synchronous motors (92%), converters (98%) and power generation plants (47%), in addition it is best suited for the power quality devices, like STATCOMs and universal power quality conditioners [82 - 83].

Recently, some new topologies of cascade multilevel inverters have also emerged. This includes asymmetric/hybrid cascade circuit topologies, cascade circuit topology with floating dc link, Cascade inverter with variable multilevel dc-link, MMC based cascade modules, Regenerative cascade inverter topologies, high frequency transformer-based power modules and finally low frequency transformer base multilevel inverters [84]. These multilevel inverters can extend rated inverter voltage and power by increasing the number of voltage levels. They can also increase equivalent switching frequency without the increase of actual switching frequency, thus reducing ripple component of inverter output voltage and electromagnetic interference effects. In over all, the application of cascade multilevel inverters (CMI) was prominent for motor drives and utility applications. Thus, the cascade inverter has drawn great interest due to the great demand of medium-voltage high-power inverters.

However, one of the major parts in the CMI operation is switching strategy. Indeed, a perfect switching can improve CMI performance dramatically.

2.3 Modulation Techniques and Control Strategies for Multilevel inverters

As discussion is confide to only cascade multilevel inverters, so switching techniques which are suitable for CMI are mentioned herein. However, in literature numerous modulation techniques have been proposed for cascade multilevel inverters. Some of the prominent switching techniques are demonstrated in Fig.2.2. While, a high number of power electronic devices and switching redundancies bring a higher level of complexity compared with a two-level inverter counterpart. This complexity could

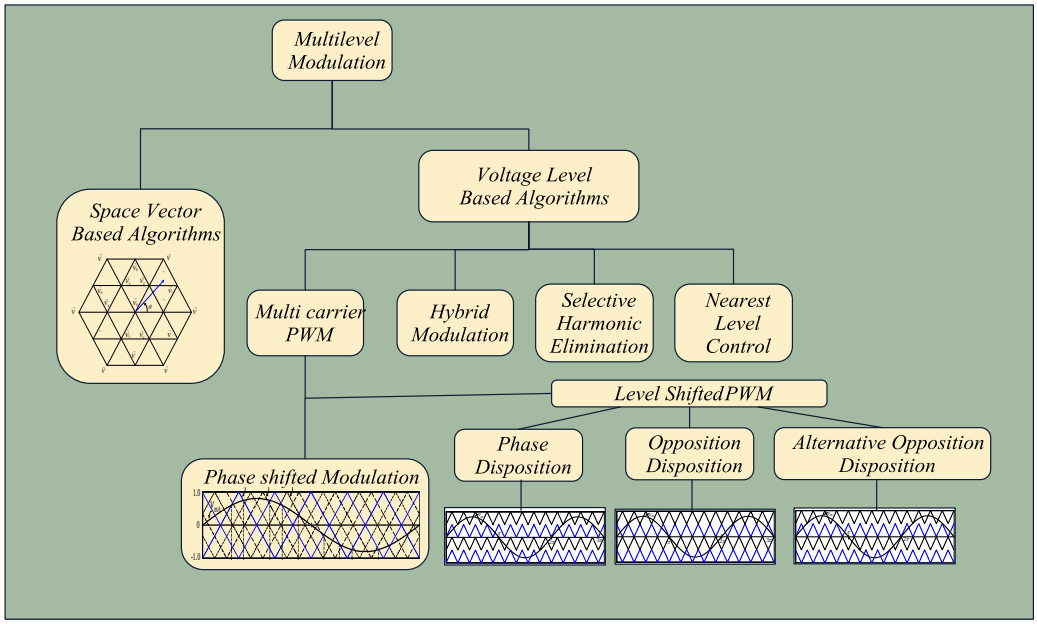


Fig. 2.2 Details of PWM techniques

be used to add additional capabilities to the modulation technique, namely, reducing the switching frequency, minimizing the common-mode voltage, or balancing the dc voltages. Modulation techniques for cascade multilevel inverters are usually an extension of the two-level modulations [85].

According to their switching frequency, they can be classified as follows [86]: 1) fundamental switching frequency, where each inverter has only one commutation per cycle, for example, multilevel selective harmonic elimination (SHE), space vector control, and nearest voltage level, and 2) high switching frequency, where each inverter has several commutations per cycle, for example, multilevel PWM and space vector modulation (SVM).

2.3.1 Multilevel SHE

SHE techniques can be applied to cascade multilevel inverters using two approaches. The first one is to consider one commutation angle per inverter; thus, the number of harmonics that can be eliminated is $N_{\text{inv}} - 1$. The switching pattern of multilevel SHE can be obtained by solving a similar set of equations to two-level SHE [87]. Numeric mathematical methods used to solve these equations are Newton-Raphson, resultant theory [88], and genetic algorithms [89]. The typical waveform obtained by this technique is shown in Fig. 2.3. In these waveforms, it is possible to note that there exists a high difference among the conducting times, which produces an unbalanced power distribution. If a multipulse transformer is used, this power unbalance can lead to a distorted input current. In [76], this effect is reduced by a simple change of conducting angles. This modulation technique can be applied to symmetrical inverters, when the number of output voltage levels is high or when the inverter has unequal dc links [90]. The second approach is to combine the original SHE with the multilevel version [91], as it can be seen in the waveform of Fig. 2.3, where there are a number of switching angles per voltage level. Mostly, in SHE, the Fourier coefficients or harmonic components of the predefined switched waveform with the unknown switching angles are made equal to zero for those undesired harmonics, while the fundamental

component is made equal to the desired reference amplitude. This set of equations is solved offline using numerical methods, obtaining a solution for the angles.

However, in all these cases, the number of harmonics eliminated is independent from the number of output voltage levels, and the switching frequency is higher than the fundamental. It is possible to note that there are several different possibilities to synthesize the output voltage, allowing a further optimization in terms of switching frequency. For converters with a higher number of levels, like CHB, SHE is also known as staircase modulation because of the stair-like shape of the voltage waveform. The basic idea is identical to SHE; the difference is that each angle is associated to a particular cell. The operating principle of this technique is to connect each cell of the inverter at specific angles to generate the multilevel output waveform, producing only a minimum of necessary commutations. The operating principle is illustrated in Fig. 2.10; note that only one angle needs to be determined per power cell.

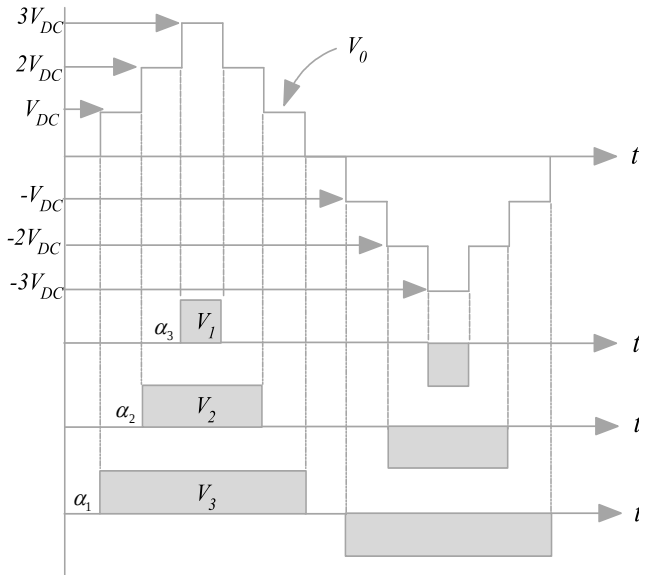


Fig. 2.3 One angle per voltage level with multilevel selective harmonic elimination technique

The main advantage, like in SHE, is that the converter switches very few times per cycle, reducing the switching losses to a minimum. In addition, low-order harmonics are eliminated, facilitating the reduction of output filter volume, weight, and cost.

2.3.2 Multilevel SVM

The space vector modulation (SVM) algorithm is basically also a PWM strategy with the difference that the switching times are computed based on the three-phase space vector representation of the reference and the inverter switching states rather than the per-phase in time representation of the reference and the output levels as in previous analyzed methods. However, multilevel converters enclose a large number of vector states which can be used to modulate the reference [92,93]. Moreover, each state vector has a number of redundancies, as shown in Fig. 2.4. Multilevel SVM must take care of this behaviour to optimize the search of the modulating vectors and to apply an appropriate switching sequence [94], [95].

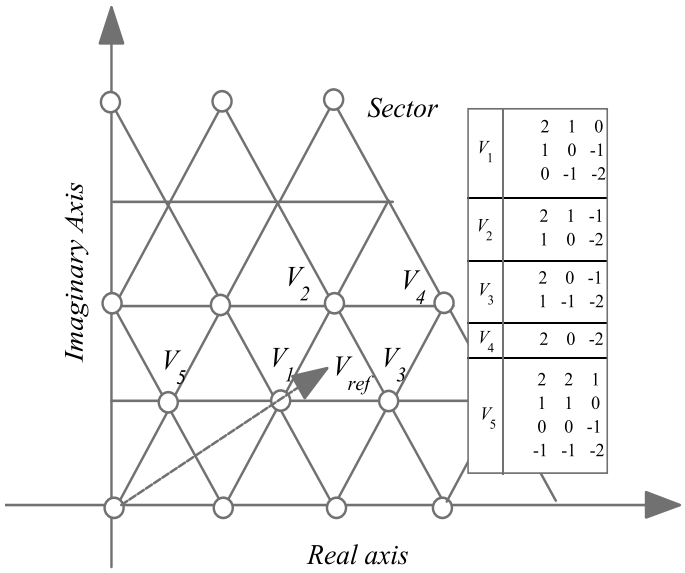


Fig. 2.4. Multilevel Space Vector Modulation

On the other hand, the same properties of state and switching redundancy allow the improvement of the modulation technique to fulfill additional objectives like, reducing the

common mode output voltage [94], reducing the effect of over modulation on the output currents [95], improving the voltage spectra and minimizing the switching frequency [96], and controlling the dc-link voltage when floating cells are used [97], [98]. In general, one of the advantages of SVM techniques for multilevel converters is the reduction of computation and implementation complexity compared to carrier-based PWM algorithms because the number of carriers does not increase as the number of converter levels increases. This advantage makes the digital implementation of the algorithms easier. In addition, the vector redundancies and the switching sequences can be used for other control purposes and can be designed according to a specific criterion depending on the application. It has to be noticed that in order to achieve a proper time average, the modulation period Ts is small, leading to high switching frequencies, comparable to carrier-based PWM (above 1 kHz), and therefore not useful for very high-power applications.

2.3.3 Multilevel Carrier-Based PWM

Multilevel carrier-based PWM uses several triangular carrier signals, which can be modified in phase and/or vertical position in order to reduce the output voltage harmonic content. There are two common carrier modifications applied to these multilevel inverters. In fact, Level-shifted PWM is widely noticed in NPC inverters and can also be used in cascade inverters. In [99], it is shown that this modulation technique is applied to a five-level inverter. This modulation technique produces an uneven distribution of power among cells, which further results in high harmonic content in the input current. In [100], this drawback is avoided using a rotating carrier, which balances the power of each cell. In [100], the level-shifted modulation is used inside each CMI inverter and synchronized with the other cells to produce the multilevel output voltage. Phase-shifted PWM is the most commonly used

modulation technique for cascade multilevel inverters because it offers an evenly power distribution among cells and it is very easy to implement independently of the number of inverters [101], [102]. This modulation shifts the phase of each carrier in a proper angle to reduce the harmonic content of the output voltage. Moreover, it is possible to work in the over modulation region when a common-mode term is added to the reference.

2.3.4 Phase Shifted (PS-PWM)

Phase-shifted PWM (PSPWM) is a natural extension of traditional PWM techniques, specially conceived for FC [103] and CHB [104] converters. Since each FC cell is a two-level converter, and each CHB cell is a three-level inverter, the traditional bipolar and unipolar PWM techniques can be used, respectively. Due to the modularity of these topologies, each cell can be modulated independently using the same reference signal.

A phase shift is introduced between the carrier signals of contiguous cells, producing a phase-shifted switching pattern between them. In this way, when connected together, a stepped multilevel waveform is originated. It has been demonstrated that the lowest distortion can be achieved when the phase shifts between carriers are 180 or $360^{\circ}/k$ for a CHB Inverter. (where k is the number of power cells). This difference is related to the fact that the FC and CHB cells generate two and three levels, respectively.

A Five-level CHB example of the operating principle is illustrated in Fig. 2.5. Since all the cells are controlled with the same reference and same carrier frequency, the switch device usage and the average power handled by each cell is evenly distributed. For the case of the CHB, this means that multipulse diode rectifiers can be used to reduce input current harmonics. It is noticed in the FC, the advantage of the even power distribution is that once the flying capacitors are properly charged (initialized to their corresponding values), no un-

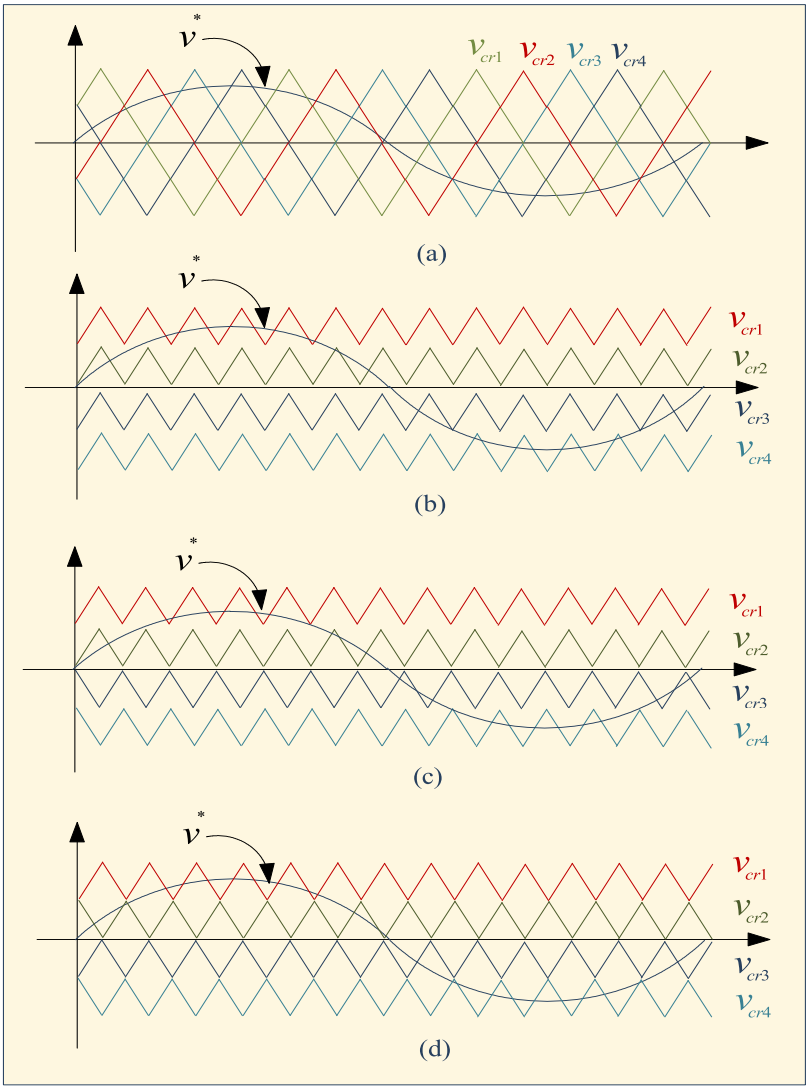


Fig. 2.5 Phase shifted and Level shifted PWM carrier arrangements

(a) Phase shifted PWM (b) PD, (c) POD, (d) APOD

-balance will be produced due to the self-balancing property of this topology [105], hence there is no need to control the dc-link voltages. Another interesting feature is the fact that the total output voltage has a switching pattern with k times the frequency of the switching pattern of each cell. This multiplicative effect is produced by the phase-shifts of the carriers.

Hence, better total harmonic distortion (THD) is obtained at the output, using k times lower frequency carriers.

2.3.5 Level Shifted PWM (LS-PWM)

Level-shifted PWM (LSPWM) is the natural extension of bipolar PWM for multilevel inverters. Bipolar PWM uses one carrier signal that is compared to the reference to decide between two different voltage levels, typically the positive and negative busbars of a VSI. By generalizing this idea, for a multilevel inverter, $m-1$ carriers are needed. They are arranged in vertical shifts instead of the phase-shift used in PS-PWM. Each carrier is set between two voltage levels; hence the name B level shifted. Since each carrier is associated to two levels, the same principle of bipolar PWM can be applied, taking into account that the control signal has to be directed to the appropriate semiconductors in order to generate the corresponding levels. The carriers span the whole amplitude range that can be generated by the converter. They can be arranged in vertical shifts, with all the signals in phase with each other, called phase disposition (PD-PWM); with all the positive carriers in phase with each other and in opposite phase of the negative carriers, known as phase opposition disposition (POD-PWM); and alternate phase opposition disposition (APOD-PWM), which is obtained by alternating the phase between adjacent carriers [106-107]. An example of these arrangements for a five-level inverter (thus four carriers) is given in Fig. 2.5, respectively.

In brief, rather than level shifted PWM, phase shifted PWM technique has finite merits like, no rotation in switching, less switching losses and easy to implement. Indeed, in present article all productive topologies are implemented with sinusoidal PWM approach. Next sections provide the details of conventional CMI topology and performance verifications and challenging aspects to resolve.

2.4 Pefromance of Traditional Cascade Multilevel Inverter With Separate DC Source

Until now, importance of CMI, applications of CMI and appropriate switching techniques, which are suitable for CMI are discussed. However, before introducing the proposed version of CMI let us have the performance verification of traditional CMI with separate dc source. Note that to explore the potential of traditional CMI, performances are presented with three different switching techniques.

For a while, let us analyze the basic CMI. Consider architecture shown in Fig.2.6, which is a series H-bridge inverter appeared in 1975 [108], furthermore several recent patents have been obtained for this topology as well. Since this topology consist of series power conversion cells, the voltage and power level may be easily scaled. Numerous advantages have been figured out using this topology,

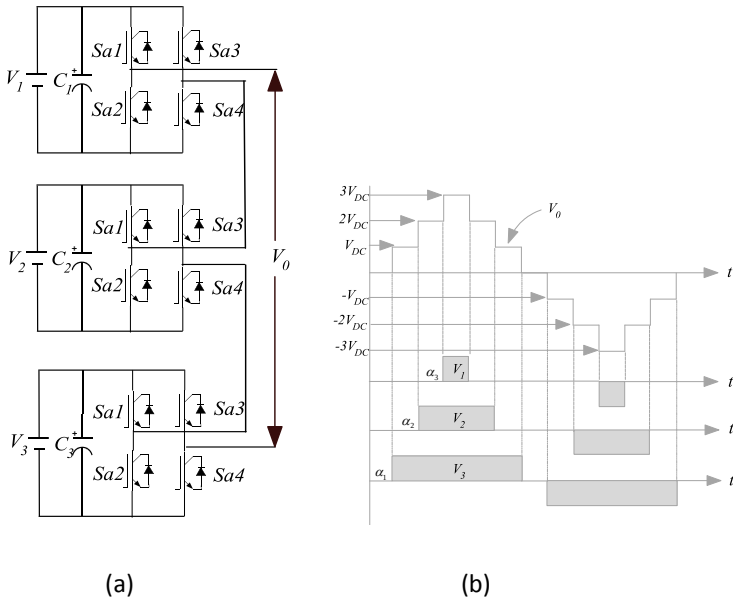


Fig.2.6 a) Conventional cascade H-Bridge multilevel inverter (7level)

b) Operational waveforms for seven level inverter

which are extensively used in Medium and high power applications. Fig.2.6 (b) provides output characteristics of seven level H-Bridge cell. Examining Fig.2.6 (b), the output phase voltage can be expressed as $v=v_1+v_2+v_3$, this is because all the inverters are connected in series. Each single-phase full bridge inverter can generate three level outputs V_{dc}, 0 and $-V_{dc}$ and this is made possible by connecting the dc sources sequentially to the ac side via the four switching devices. Minimum harmonic distortion can be obtained by controlling the conducting angles at different inverter levels.

Further, Fig.2.7 illustrates the details of seven level three phase star connected CMI. It is just identical to single-phase type but the configuration is built for three individual phase which are 120^0 apart. However, on a close observation, three phase archetype uses total nine dc sources and for each phase it uses three dc sources. Readers should aware about the number of dc sources in structure. However, a complete list of drawbacks of this architecture

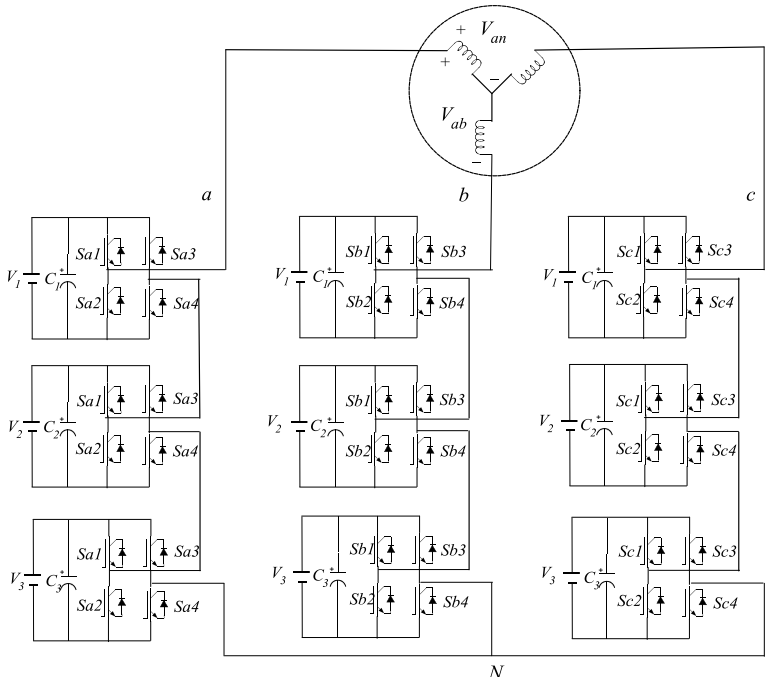


Fig.2.7 Details of conventional three phase seven level cascade multilevel inverter

is presented in the end of the section. Later, Fig.2.8, Fig.2.9 and Fig.2.10 demonstrate performance verification and FFT spectra details for conventional CMI. Note that, herein performances have been done with three switching approaches.

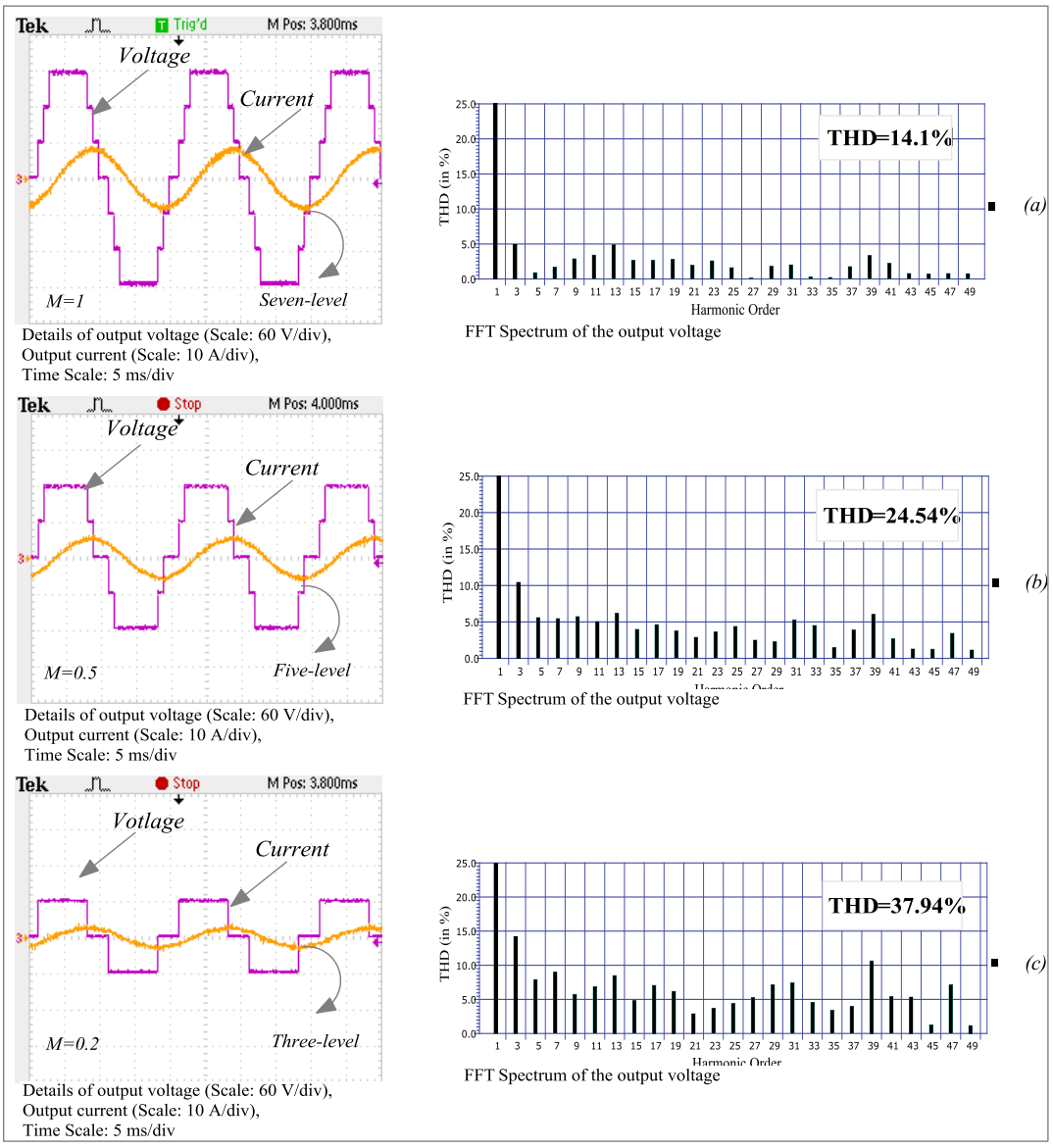


Fig.2.8 a) Performance of cascade multilevel inverter with three-phase transformers by using fundamental frequency approach at Modulation index 1 ,0.5, 0.2 (from top to bottom)

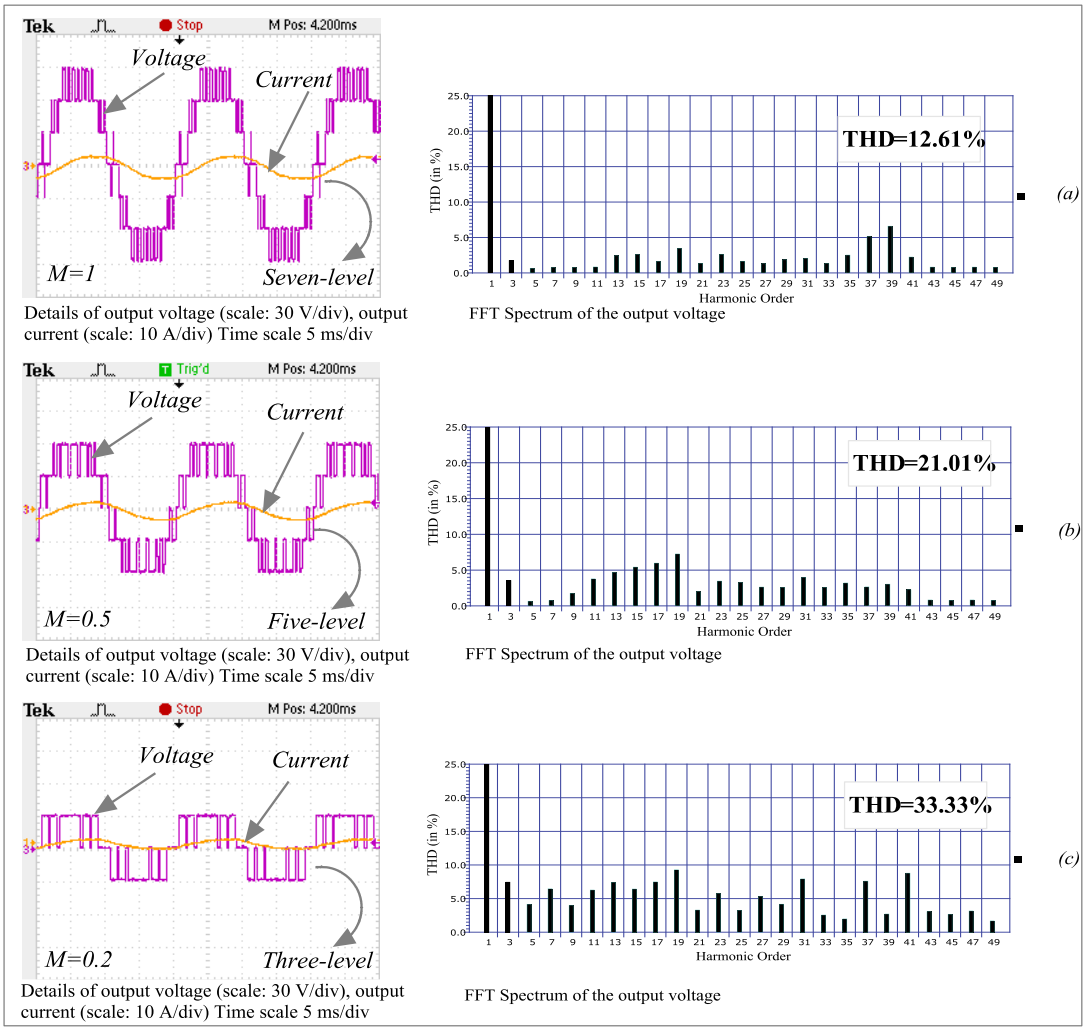


Fig.2.9 a) Performance of cascade multilevel inverter with three-phase transformers by using selective harmonic PWM approach at Modulation index 1 ,0.5, 0.2 (from top to bottom)

Finite reason behind applying three switching approaches is to explore and find out the potential of traditional CMI and to clarify that trouble-free adoption of different switching approaches to the CMI is possible.

Details of hardware prototype setup are demonstrated in chapter 4. Coming to experimental results, on observing Fig 2.8 (fundamental switching approach), Fig.2.9 (selective harmonic PWM approach), and Fig.2.10 (sinusoidal PWM approach) output voltage waveforms are almost sinusoidal in fashion.

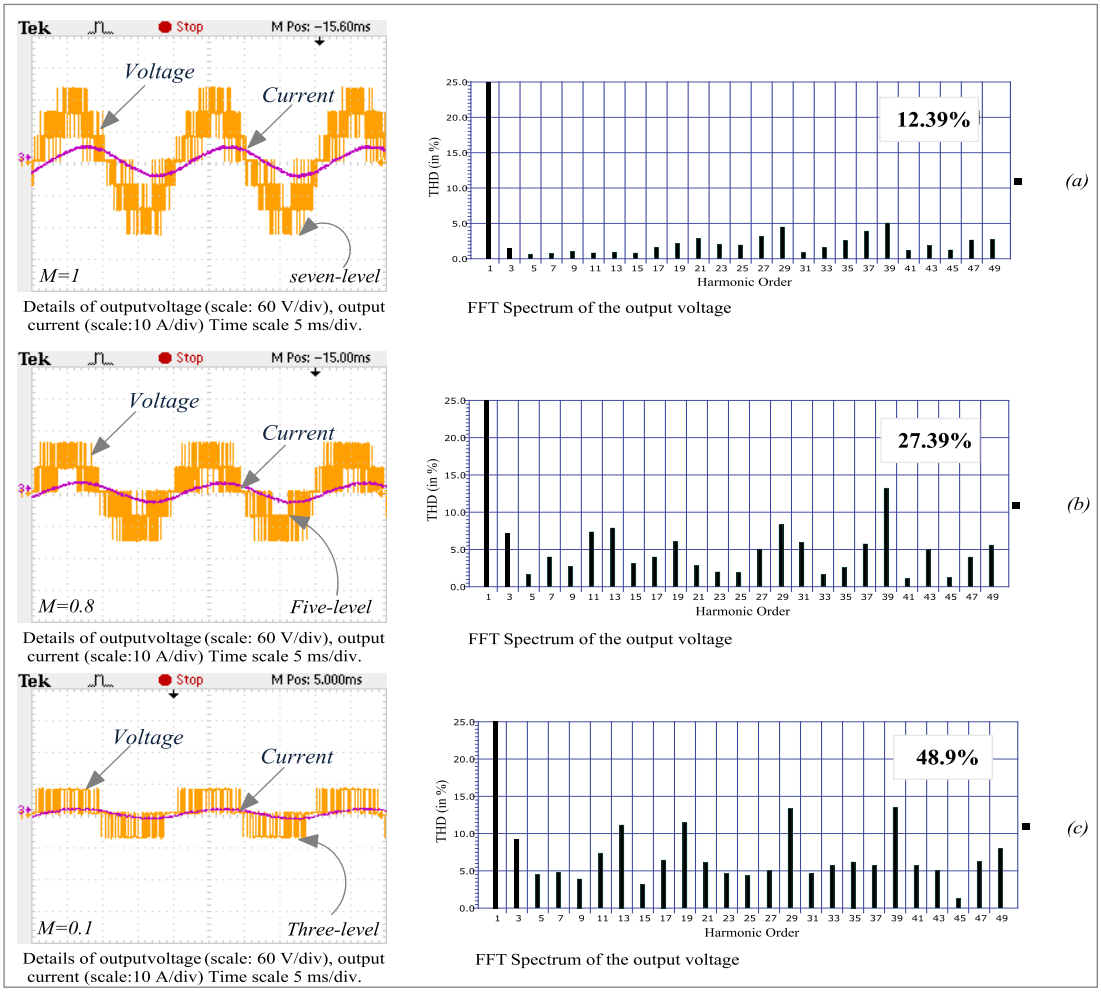


Fig.2.10 a) Performance of cascade multilevel inverter with three-phase transformers by using fundamental frequency approach at Modulation index 1, 0.5, 0.2 (from top to bottom)

In particular at modulation index 1 corresponding FFT spectra signifies complete elimination of lower order harmonics. But in all the cases 3rd and its multiple harmonics are unavoidable in phase voltage. However, on comparing three switching approaches i.e. fundamental switching (Fig.2.8), Selective harmonic elimination PWM (Fig.2.9) and Sinusoidal PWM (Fig.2.10), Sinusoidal PWM have shown some improved performances at higher modulation indexes. Moreover, SPWM approach is quite easy to handle and implement. From this prospects it is evident that traditional CMI based converters are cost-effective, efficient, possible to modularize circuit layout and easy to pack, because each level

has the same structure, and there are no extra clamping diodes or voltage balancing capacitors.

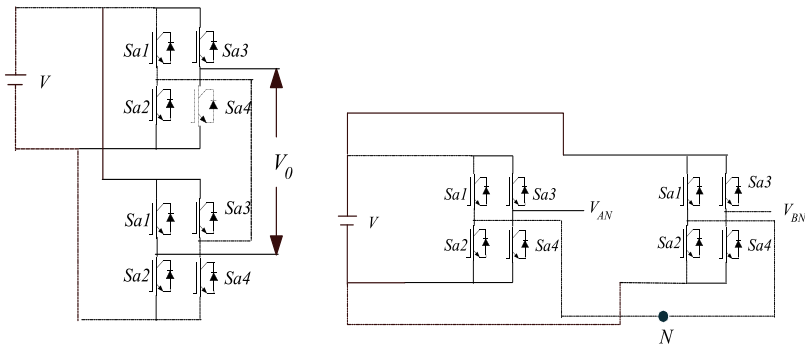


Fig. 2.11 Short circuit possibility of CMI

But, this CMI uses large number of isolated voltages required to supply each H-Bridge cell and there is a possibility of short circuit of the input dc voltage sources if they are connected to common dc supply and this is shown in Fig.2.11.

2.5 Challenging issues in Cascade Multilevel Inverter with separate DC source

From above prospects it is clear that traditional CMI performance is quite impressive, moreover it is possible to adopt different switching approaches very easily (compare to other multilevel structures). All these reasons made this inverter topology to establish in the market for medium and high power applications. But on the flip side, there are some aspects that require further development and research. These are summarized as below;

- The first issue that needs attention is the efficiency improvement [69]. Although several advances have been reported to reduce the switching losses using an optimal modulation technique; but the conduction losses are far more critical due to the series connection of several semiconductors and high output currents. In order to reduce these losses, new advances in the semiconductor technology are expected.

- The use of floating cells could simplify the design of the input transformer or even eliminate it, which should reduce losses, cooling requirements, cost and volume.
- To reach *higher voltage levels* with less number of switching components is another prominent issue. So **new kind of architectures** and designs are essential.
- Particular attention is focused on **CMI with minimum number of *DC source.*** Because separate dc source is a greatest limitation.
- Increasing the blocking voltage and other related technologies like gate drivers and sensors are also need to be modified.

Although their exits huge requirements, but research pioneers always look for most efficient and cost effective inverter and this thesis is completely devoted for this aspect. In fact we placed our complete attention on the design of the CMI with single dc source. However, with the help of single dc source, CMI gains additional capabilities and functions. Further, to reduce the numbers of dc sources count in CMI, in recent past, some of the topologies came in existence and some of the prominent archetypes will be verified in the next chapter.

2.6 Summary

This chapter has figured out some of the remarkable topologies of multilevel inverter. An in-depth investigation has been done on each inverter. Particularly, NPC-MLI, FC-MLI and CHB-MLI have been explored. Further, importance of cascade multilevel inverter is demonstrated through component verifications. Applications of CMI are presented in detail. Later, appropriate switching techniques which are suitable for CMI are demonstrated. Further, experimental verifications for traditional CMI i.e. CMI with separate DC source are presented with three different switching techniques. Finally, challenging issues in CMI are exclusively identified.

Chapter 3

Cascade Multilevel Inverters with Minimum Dc Sources

Cascade Multilevel Inverter with Separate DC Source

Cascade Multilevel Inverter with Minimum DC Sources

Hybrid Cascade H-Bridge Multilevel Inverter Sources

Cascade H-Bridge Multilevel Inverter by Employing Single Phase Transformers

Cascade Multilevel Inverter with Cascade Transfomers

Summary

Chapter 3

In the previous chapter importance of cascade multilevel inverter is explored. Furthermore, PWM based switching techniques are also introduced. Finally, performance of traditional CMI is verified with different switching techniques. At the end it is concluded that CMI based converters have a greatest limitation i.e. usage of separate dc source for each H-Bridge cell. In this chapter we have investigated cascade multilevel based architectures with reduced dc source. With this approach we try to reduce the dc source count and thereby complexity and cost of converter. Coming to details, section 3.1 provides the particulars of CMI with unequal DC source. Section 3.2 presents the details of CMI with minimum dc sources. Section 3.3 & 3.4 presents the details of hybrid CMI converters. Section 3.5 & 3.6 provides the details of CMI with single-phase transformers. Note that all productive topologies which are presented in this chapter are exclusively verified with prototype experiments. Later at the end of the section, a comparative study is carried out among the converters and finally demerits of converters are demonstrated.

3.1 Cascade H-Bridge With Unequal Dc Sources

Basically the DC voltages of the H-bridge power cells introduced in the preceding section are all the same. On the other hand, different dc voltages may be selected for the power cells [109 -110]. Fig.3.1 constructed with unequal dc voltages, the number of voltage levels can be increased without necessarily increasing the number of H-bridge cells in cascade. This permit more voltage steps in the inverter and thereby yields improved voltage waveform for a same number of power cells. In the present structure the dc voltages for *H1 H2* and *H3* are chosen as *E*, 2*E*, 3*E* respectively. The three-cell inverter leg is able to produce thirteen level voltage waveform i.e., the voltage waveform constitutes: 6E, 5*E*, 4*E*, 3*E*, 2*E*, *E*,

0, *–E*, *–2E*,*–3E*,*–4E*,*–5E*,*–6E*. Fig.3.2, Fig.3.3 and Fig.3.4 present the details of output voltage and FFT spectra. With the present structure, quality of waveform can be improved predominantly. Further this kind of operation facilitates to use very less number of DC sources. But at the same time there are some drawbacks associated with the CHB inverter using unequal dc voltages. The merits of the modular structure are basically lost. In addition, switching pattern design becomes much more difficult due to the reduction in redundant switching states. Therefore, this inverter topology has limited industrial applications.

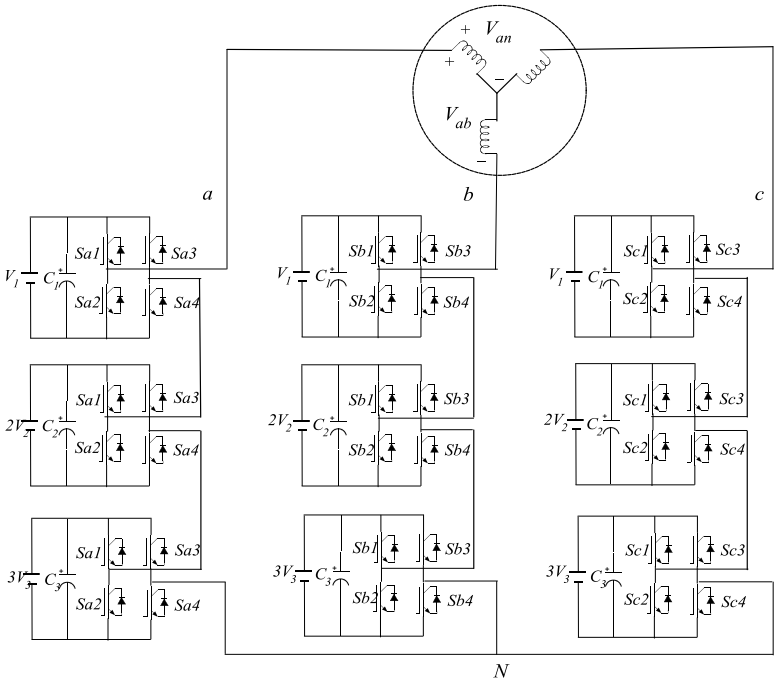


Fig.3.1 Cascade multilevel converter with minimum number of dc sources

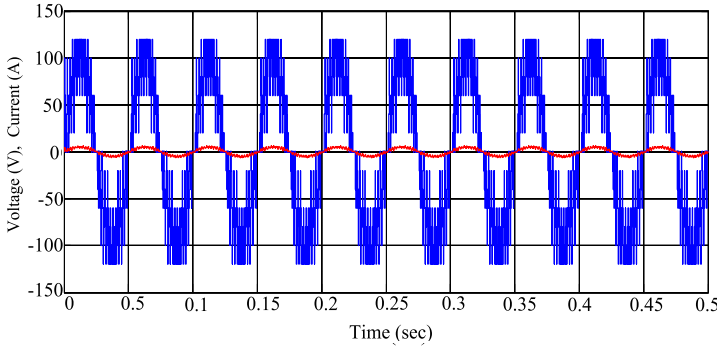


Fig. 3.2 Simulation verification cascade multilevel converter with unequal dc voltages

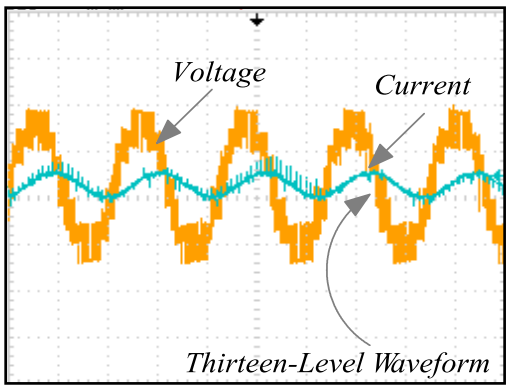


Fig.3.3 Details of output voltage (scale: 60 V/div), output current (scale 5 A/div), of cascade H-Bridge multilevel inverter with unequal dc sources at m=0.85

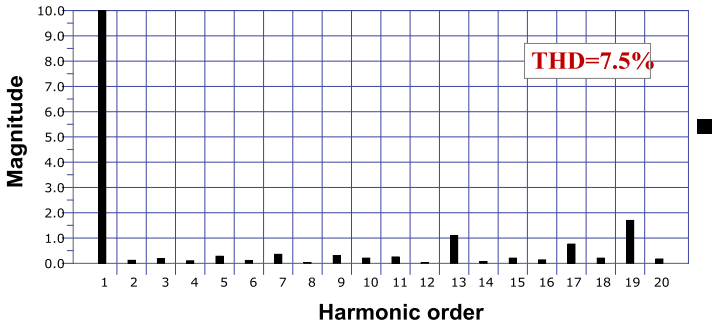


Fig.3.4 Detials of FFT Spectra

3.2 Cascade Multilevel Inverter With Minimum Dc Sources

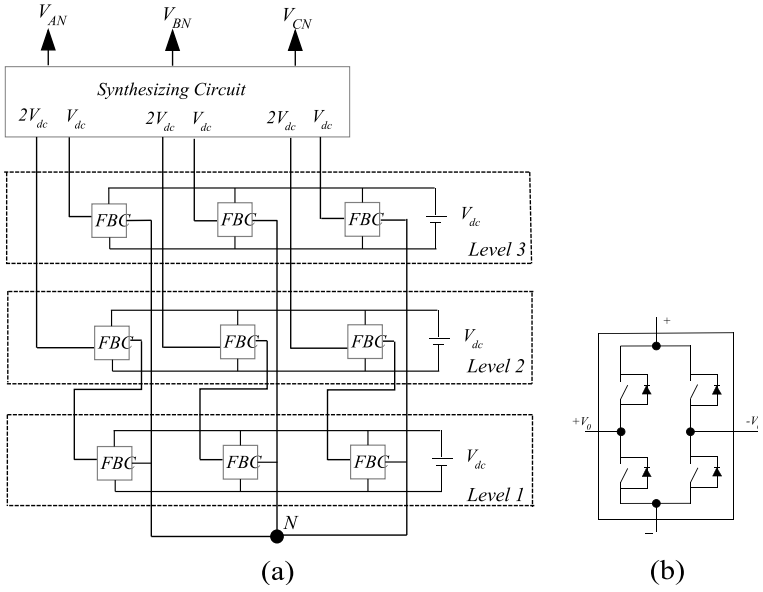


Fig.3.5 Cascade multilevel inverter with single dc-source with minimum number of isolated dc sources a) circuit diagram b) full-Bridge cell (FBC)

This is one of the productive topology form CMI family. Author had finite contribution regarding this archetype [112, 134]. CMI with minimum dc sources is shown in Fig 3.5. Fig.3.5 (a) demonstrates structure with three dc sources with nine H-Bridge cells and Fig 3.5 (b) shows the schematic of an H-bridge converter, which is a basic unit in the converter and defined as a full-Bridge cell (FBC). Based on the switch combinations of each FBC, three output-voltage levels at $+V_0$ with respect to $-V_0$ and vice versa can be synthesized, i.e., $+V_{dc}$, 0 and $-V_{dc}$. In fact, three-phase multilevel inverter illustrated in Fig 3.5 (a) consists of nine FBCs, three DC sources, and a synthesizing circuit. The FBCs in levels 1 and 2 are cascaded to generate a three-phase output voltage of $\pm 2V_{dc}$, while the FBCs in level 3, which is independent from levels 1 and 2, are used to generate $\pm V_{dc}$ three-phase output voltages.

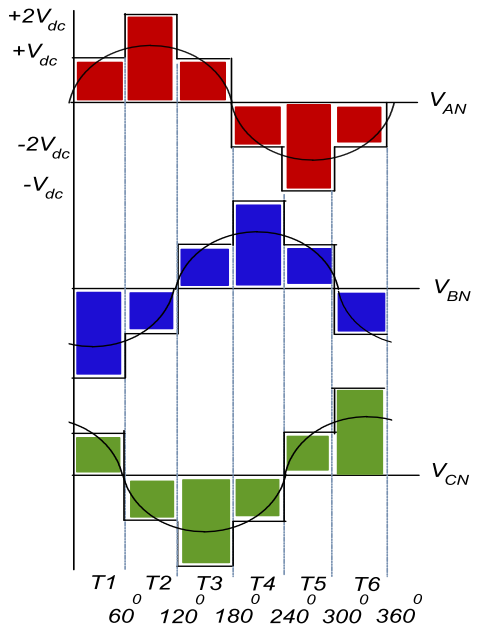


Fig.3.6 Output waveform of CMI with three dc source

To clearly explain how the proposed converter works, the FBCs in level 1 are used as an example. If one of the FBCs switches, the others, which share the same DC voltage, must

keep floating or use the same switching patterns. Otherwise, a short circuit of the DC sources or shoot-though will be introduced. By applying this principle, a possible synthesized phase-voltage waveform of the proposed converter is thus illustrated in Fig.3.6. To generate three-phase waveforms, one cycle of the voltage waveform is equally divided into six parts. Each part, therefore, has a width of 60^0. In general, the zero-sequence voltage of the system should be maintained at zero at all times. As far as concern, the key point is summation of the three voltages in each part should be maintained to zero, this is predictable form above Fig.3.6.

However Fig. 3.7, Fig.3.8 and Fig. 3.9 demonstrate the experimental verification and FFT reports at modulation index 1. Observing FFT spectra, THD is about 30%. Though lower order harmonic are eliminated, presence of harmonic content is very high, which is not acceptable, but comparing with conventional seven level structures this converter requires only three dc sources. Thus converter is economical but not efficient. These classes of converter are extensively used in motor drive application. However, for better idea some of the merits and demerits of this converter are:

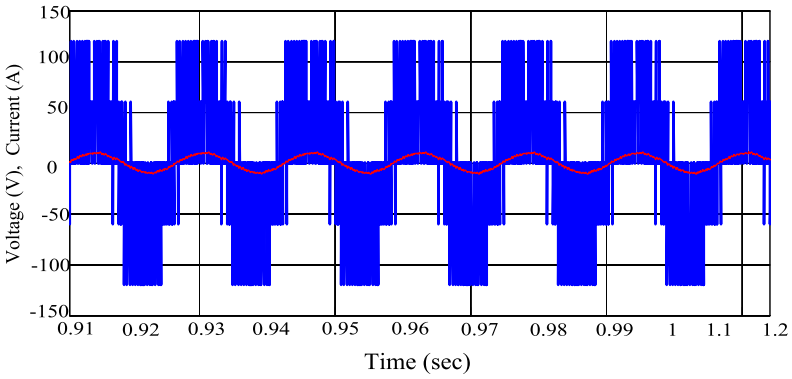


Fig.3.7 Simulation verification for CMI with reduced dc source

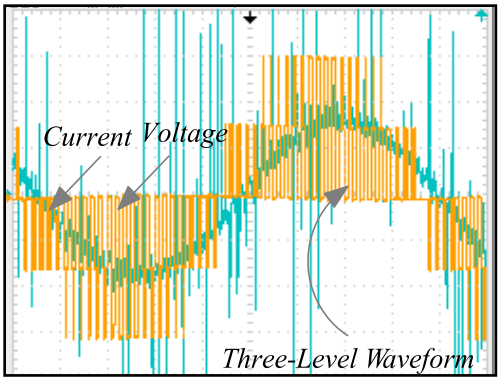


Fig.3.8 Experimental Output voltage (scale: 60 V/div), output current (scale: 2 A/div)

of CMI with three dc sources at m=0.85

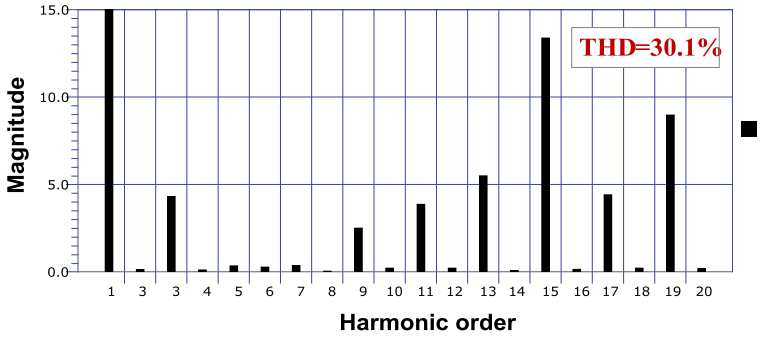


Fig.3.9 Details of FFT Spectra

Merits

- *Reliability of system improved greatly.*
- *Less in price tag as only three dc sources are used.*
- *Finite Modularity, easy in circuit layout and packaging.*
- *Finally, it confers feasibility to CMC for manufacturing and flexibility in sense of power expansion.*

Demerits

- *Complex switching.*
- *Poor THD of the output voltage.*

3.3 Hybrid Cascade Multilevel With Bottom Three Leg Inverter

The topology hybrid multilevel inverter is shown in Fig. 3.10, which includes complete three-phase architecture [113-114]. The bottom is one of a standard 3- leg inverter with a dc power source. The top is an H-bridge in series with each standard inverter leg [115-116]. The H-bridge can use a capacitor, battery or other dc power source. The output voltage v_1 of this leg (with reference to the ground) is either $+Vdc/2$ (S5 closed) or $-Vdc/2$ (S6 closed). This leg is allied in series with a full H-bridge, which in turn is provided by a capacitor voltage. If the capacitor is used and charged to $Vdc/2$, then the output voltage of the H-bridge can take on the values $+Vdc/2$ (S1, S4 closed), 0 (S1, S2 closed or S3, S4 closed), or $-Vdc/2$ (S2, S3 closed). Fig. 3.11 shows an output voltage example. The capacitor's voltage regulation control method consists of monitoring the output current and the capacitor voltage so that during periods of zero voltage output, either the switches S1, S4, and S6 are closed or the switches S2, S3, S5 are closed, depending on whether it is necessary to charge or discharge the capacitor. The method followed here depends on the voltage and current not being in phase. It represents that either positive or negative current is needed when the voltage is passing through zero in order to charge or discharge the capacitor. Consequently, the amount of capacitor voltage the scheme can regulate depends on the phase angle difference of output voltage and current. One of the critical issue in this topology is charging and discharging of a capacitor and it is entirely depends on the modulation index.

However, in the present case level shifted PWM is adopted. Charging and discharging periods are demonstrated in the Fig.3.11. To operate successfully modulation index is chosen as 1.54 [117]. The simulation and experimental verifications are presented in Fig.3.12, Fig.3.13, respectively and FFT spectra is presented in Fig.3.14. Examining further,

performance of converter is exceptionally flexible. FFT spectra specifies elimination of lower order harmonics. However, as modulation index decrease odd harmonic components are significantly noticed. In fact, these classes of converters are widely used in utility interface applications with renewable energy source due to its functions and features. In common the hybrid cascade multilevel inverters adapted for solar grid application, because the bottom standard 3-leg inverter connects with a solar panel and the top three H-bridges use a battery separately as an energy storage device. Converter is exceptionally good but, charging and discharging of converter is a hectic job.

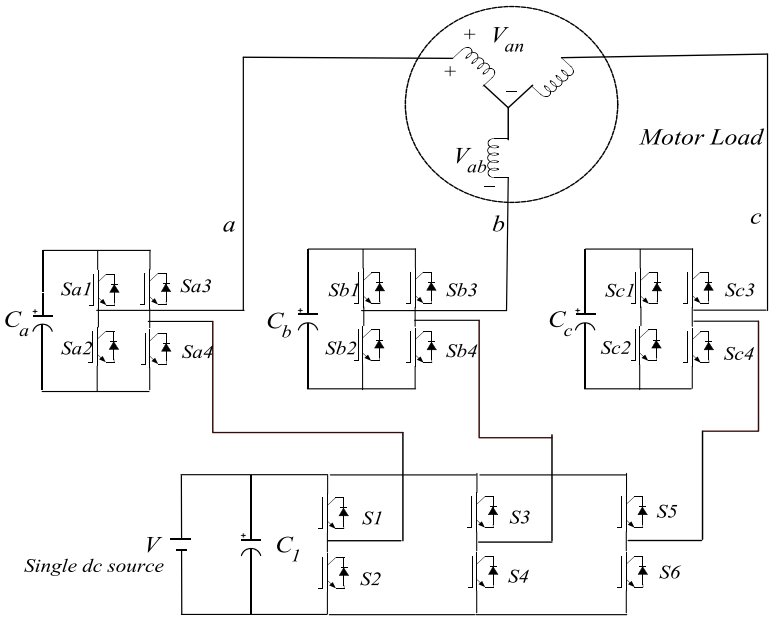


Fig.3.10 Hybrid cascade multilevel inverter with single dc-source

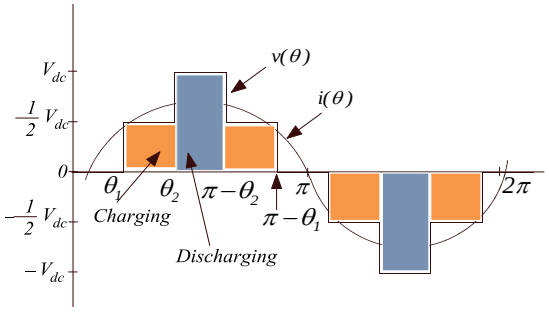


Fig.3.11 Five level output waveform

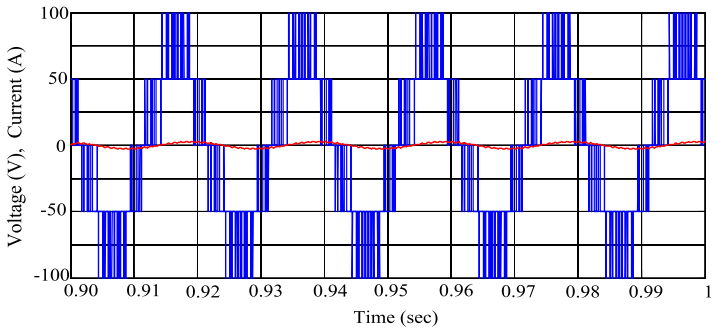


Fig. 3.12 Simulaiton verification of Five level Hybrid cascade multilevel inverter

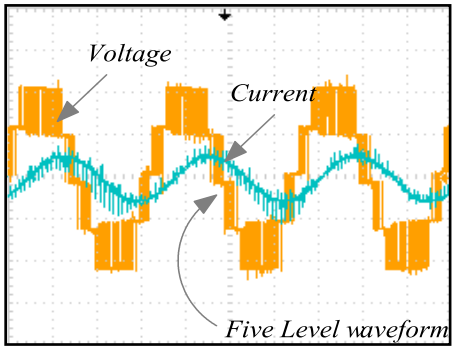


Fig.3.13 Experimental output voltage (scale 60 V/div), output current (scale: 5A/div) of the hybrid cascade multilevel inverter at m=0.85

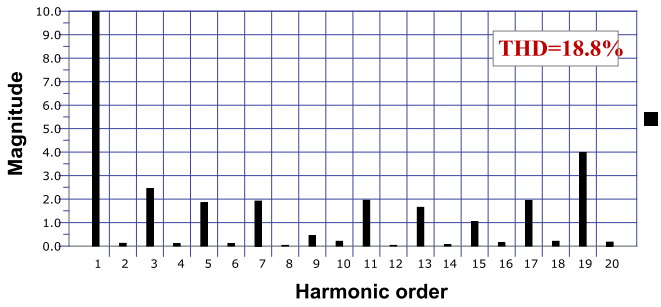


Fig.3.14 Detials of FFT Spectra

Further it fails to operate at lower modulation index. Some of the attractive features of this converter are given below:

Merits:

- *Cost effective*
- *Packaging/layout is much easier because of simplicity of structure and lower component count.*

- *Improvement in reliability.*

Demerits

- *Complex switching.*
- *Narrow modulation index range*

3.4 Hybrid Cascade H-Bridge Multilevel Inverter

In the preceding section hybrid CMI uses standard 3-leg inverter for bottom leg, but in the present case we build entire converter with H-Bridge modules [119-120] and a 7-level hybrid cascade H-Bridge architecture [120] is presented in Fig.3.15, to clarify further. The dc source for the first H-bridge (H_1) is a battery or fuel cell with an output voltage of V_{dc}, while the dc source for the second H-bridge (H_2) is a capacitor whose voltage is to be held at V_c.

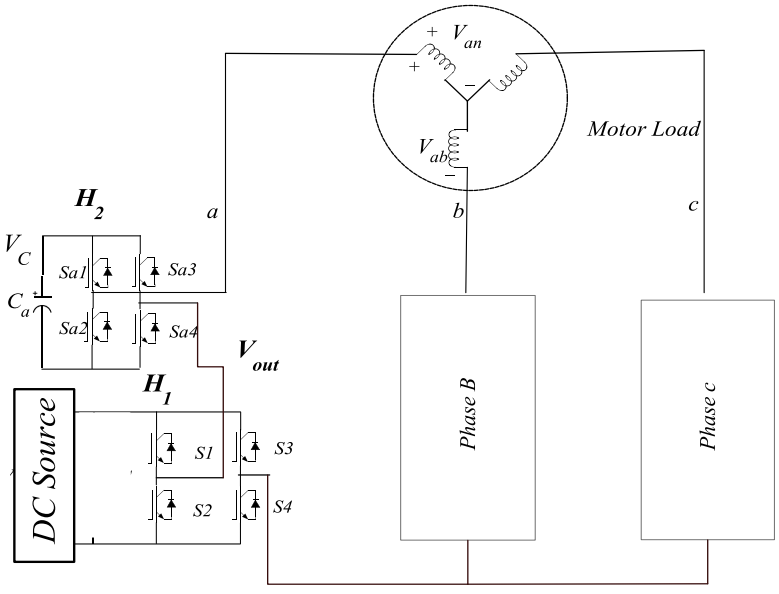


Fig.3.15 Hybrid cascade H-bridge multilevel inverter with single dc-source

The output voltage of the first H-bridge is denoted by V_1 and the output of the second H-bridge is denoted by V_2. By opening and closing the switches of H1 appropriately, the output voltage V_1 can be made equal to $-V_{dc}$, 0, or V_{dc}, while similarly the output voltage of

H2 can be made equal to $-V_c$, 0, or V_c. Therefore, the output voltage of the inverter can have the values $-(V_{dc} + V_c)$, $-V_{dc}$, $-(V_{dc} - V_c)$, $-V_c$, 0, V_c , $(V_{dc} - V_c)$, Vdc, and $(V_{dc} + V_c)$, which constitute nine possible output levels. To balance the capacitor's voltage, not all the possible voltage levels should be used in a cycle. A simple seven-level output voltage case $-3V_{dc}/2$, $-V_{dc}$, $-V_{dc}/2$, 0, $V_{dc}/2$, V_{dc}, $3V_{dc}/2$ can be designed, as shown in Fig.3.16, when the capacitor's voltage V_c is chosen as $V_{dc}/2$. By choosing the nominal value of the capacitor voltage to be one-half that of the dc source, the values of the levels are equal; however, this is not strictly required. The criteria for this capacitor balancing scheme is that: 1) the capacitance value is chosen large enough so that the variation of its voltage around its nominal value is small, generally speaking, one can choose the capacitor–load time constant to be ten times than that of the fundamental period); and 2) the capacitor charging energy is greater than or equal to the capacitor discharge energy in a cycle.

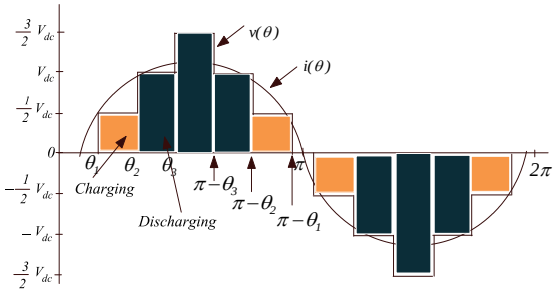


Fig.3.16 Seven level output waveform

This class of converters can operate both in fundamental frequency switching and PWM control. At the same time with this control approaches, charging and discharging of the capacitor can be done effectively. As far as concern in any of the cases; modulation index range should be extended to greater than 1 so that converter gains adequate time to charge up and regulate the voltage. However, to confirm the mentioned findings, performance verifications are exposed in Fig.3.17, Fig.3.18 and Fig.3.19. On inspecting, votlage and

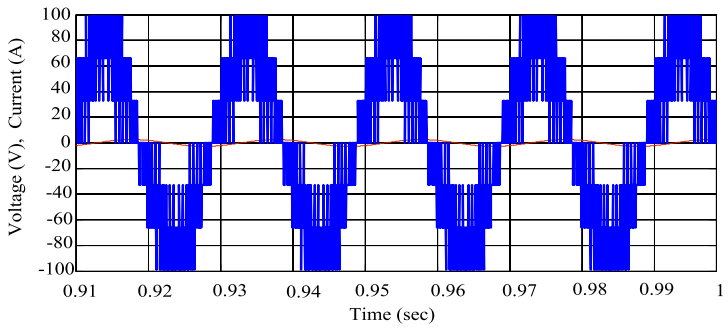


Fig.3.17 Simulaiton verification of seven level Hybrid cascade multilevel inverter

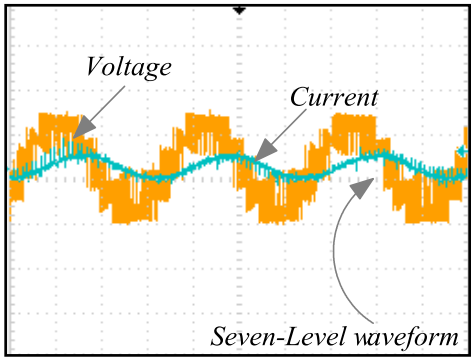


Fig.3.18 Experimental Output voltage (scale: 60 V/div), output current (scale: 5 A/div) of the hybrid cascade H-Bridge multilevel inverter at m=0.85

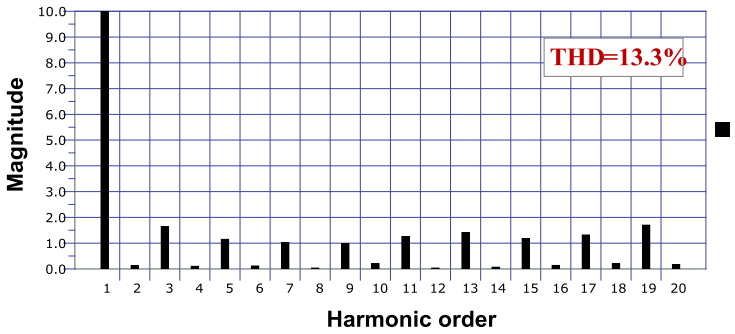


Fig.3.19 Details of FFT Spectra

current wavefroms are quite good and FFT spectra specifies significat reduction in lower order harmonics. In overall, this class of converters are extensively observed in motordrive applications. On the other side covnerter had great limitation that, it fails to operate at lower modualiton index. Addtionally, as level increases component count increases drastically

thereby realibily comes down. However, some of the feauters of the converter are given below.

Merits:

- *Significant improvement in reliability*
- *Price tag of converter drastically comes down because of limited DC source.*
- *Modularized circuit layout*
- *Good output waveforms.*

Demerits

- *Narrow modulation index range, because converters usually operate for longer discharging time and shorter charging time.*

3.5 Cascade H-Bridge Multilevel Inverter by emplyoing single phase transfomers

Fig.3.20 shows the CMC with single dc source by employing single phase transformers. To be noticed, these classes of converters are extensively used in utility interfacing applications [121]. But, this structure utilizes the single phase transformers for each H-Bridge. By employing transformers in each H-bridge this can be easily coupled to grid connected systems [122]. However, each H-Bridge module generates a three outputs voltages of $+V_{DC}$, Zero, $-V_{DC}$. In similar fashion rest of the H-Bridges generates the same voltages but at the end all voltages are added up with transformer, thereby the shape of the output voltage is like a step waveform. In fact the operation is similar to conventional cascade H-Bridge but summing up of voltages is done through the transformers. However, the performances of mentioned architecture are demonstrated in Fig.3.21, Fig.3.22 and Fig.23.

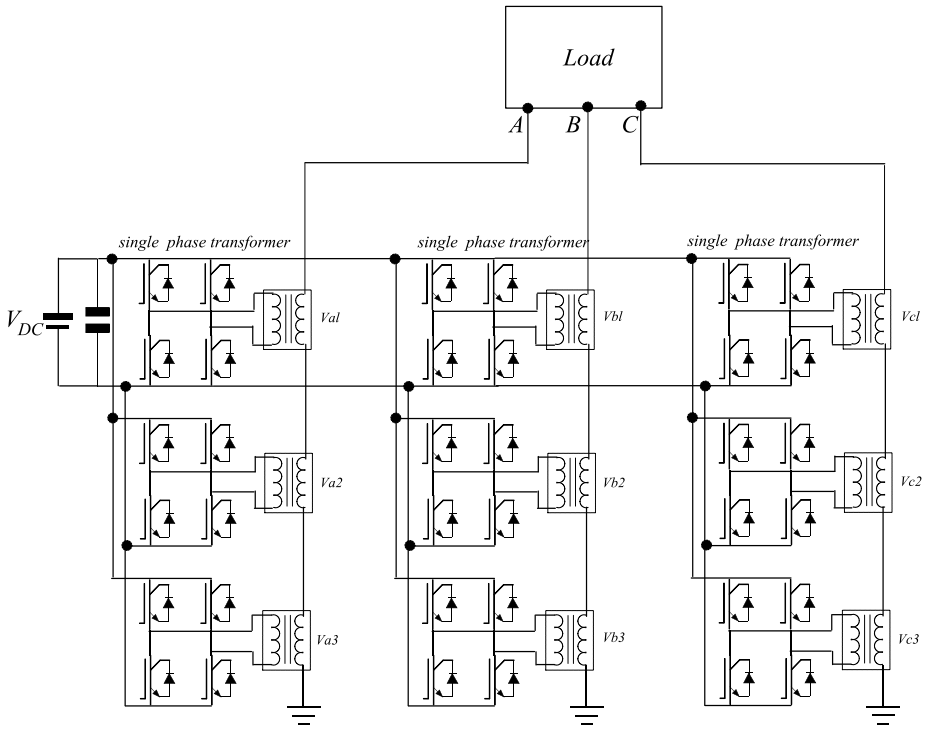


Fig.3.20 Details of cascade multilevel inverters with Single dc source by employing single phase transformers

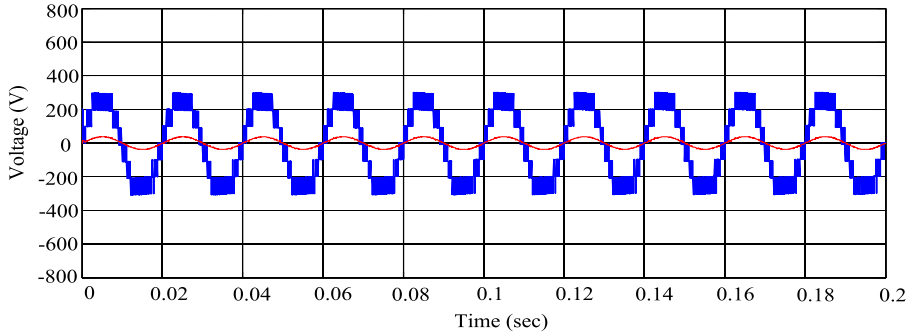


Fig.3.21 Simulaiton verification of Output voltage and current waveform of the cascade multilevel inverter with single-phase transformers

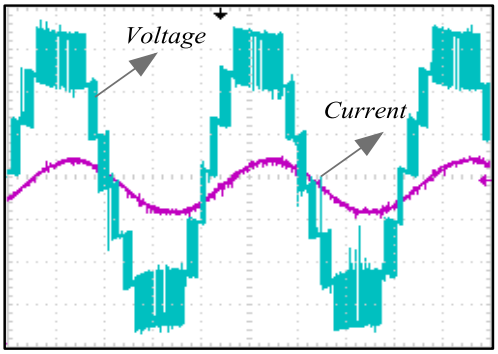


Fig.3.22 Experimental Output voltage (scale: 60 V/div), output current (scale: 5A/div) of the cascade multilevel inverter with single-phase transformers

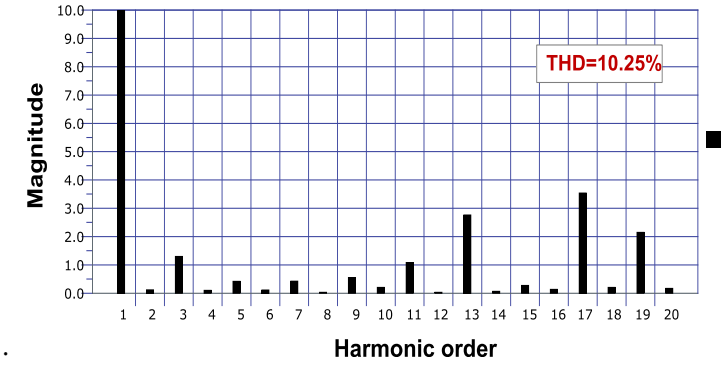


Fig.3.23. Details of FFT Spectra

On inspecting the verfications, a seven level output is observed in the output wavefrom. Due to the presence of lekage reactaces, waveforms are little bit smoother. However, this archtype has fintie merit regarding DC sources. Because it uses only single source. Due to this fact complexity on control part drastically reduces. But this archtype too have demerits like; usage of many transfomers. In fact, for every additional level in the output voltage transformers count incresaes dramitically.

3.6 Cascade Multilevel Inverter With Cascade Transfomers

Fig.3.24 and Fig.3.25 demonistrates the CMI with cascade transfomers and its operation. This class of converters are highly visible in grid connected / Photo voltiac systems. Authors [123] have finite contributions regarding this archtype. On inspecting the architecteur, due to transfomerms on the secondary we can convert the power from ac utility, from a relatively low dc votlages by itself. Furhter galvanic isolation probelms are also evaded. Adding to above merits, it does not require any output filter because of transfomers. Because it is a known fact that leakage reactance can drastically nullify the high-order harmnics [124].

However, regarding operation point of view, it is quite different while comparing with other techniques. Because in this switching synthesis, one converter is operated in mode

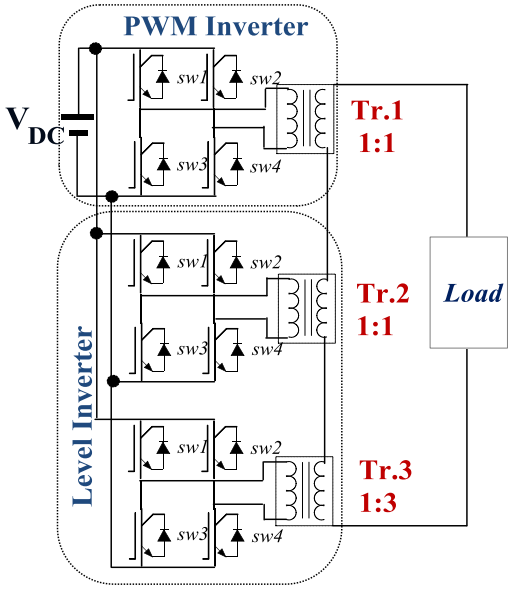


Fig. 3.24. Details of Cascade multilevel inverter with Single dc source by employing cascade transformers

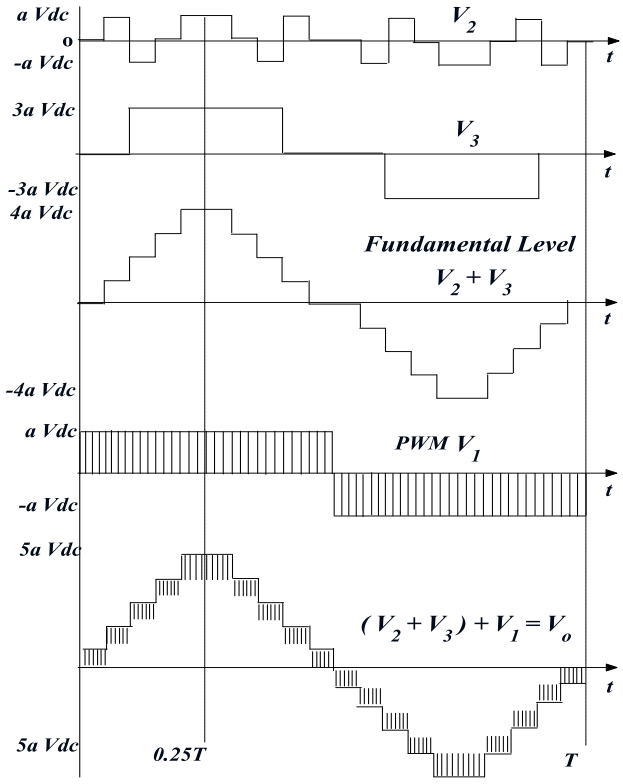


Fig. 3.25. Output voltage waveforms for cascade H-Bridge multilevel inverter by employing transformers

PWM bridge and rest in fundemntal switching mode. This helps to nullify the switchig losses and therby increases the efficiency. however, in depth assesment of toplogy can found in above references. In fact there are huge control approaches based on this switching logic. But in all the cases fundemental principle is same. However, for better understanding experimental results and FFT report of output votalge are exposed in Fig.3.26 and Fig.3.27 for CMI with cascade transfomers.

Observing keenly, eleven-level output could be predicted in the output votlage wavefrom. At this point readers should observe that, terminal votlages of transformer 2 and 3 are fundemntal votlages and terminal votlage for transfomer 1 is PWM voltage. Combining all such votlages produces a resultant wavefrom. This is an efficient technique to reduce the switching losses. One of the finest merit is, it uses single DC source. But at the same moment its greatest limitation is complexity in switching scheme, poor quality in the wavefroms because of the third harmonic componet and usage of many switching componets.

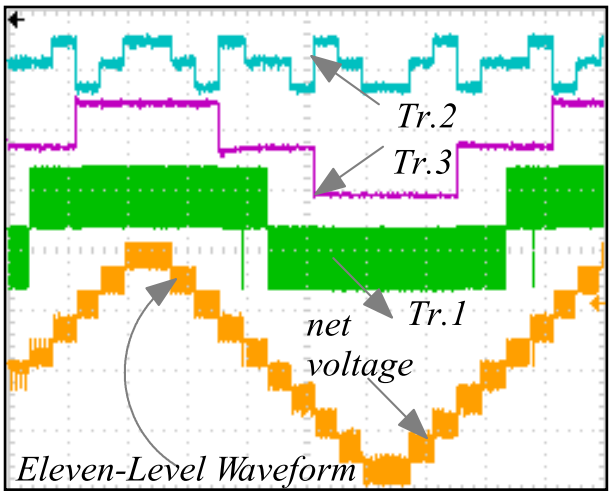


Fig. 3.26. Experimental Output voltage waveforms for cascade H-Bridge multilevel inverter by employing cascade transformers with different turn ratios

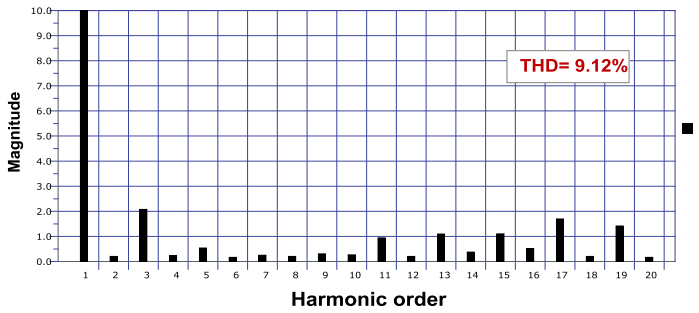


Fig. 3.27. Details of FFT Spectra

Thus, from above discussion it is concluded that, though converters are quite good from structure point of view, but still they have drawbacks such as, usage of many DC sources, poor DC bus capacitors and output voltage quality. For this reason, we proposed a new structure with single dc source by using three phase transformers. Proposed structure drastically improves the output voltage quality with single dc source and single DC bus capacitance. Adding to that, proposed converter features a high modularity degree because each converter can be module with similar circuit topology and it significantly fit to attain a higher efficiency because the devices can be switched at minimum frequency.

3.8 Summary

This chapter presented most prominent CMI based topologies with reduced number of dc sources. Further, all productive topologies are verified with prototype experiments. However, with this finding conventional CMI based architectures and their performances are summarized. Further, at the end it is concluded that mentioned topologies has finite demerits like excessive number of switching components are required to generate higher number of voltage levels.

Chapter 4

Proposed Cascade Multilevel Inverter

Proposed CMI with three-phase transformers

Performance Verifications

System Hardware

Experimental Results

Comparative Study

Summary

Chapter 4

In the previous chapter cascade multilevel inverter with minimum number of dc sources are discussed and drawbacks of such inverters are also demonstrated. In this chapter, proposed architecture is introduced. Furthermore, it is verified with most prominent switching techniques like fundamental switching, SHE-PWM, Sinusoidal PWM. Finally, it is has been verified with prototype experiments. In the present chapter, the proposed CMI with single DC source by employing three phase transformers are presented in section 4.1. The mathematical verification for proposed version is presented in Section 4.2. The three switching techniques for proposed CMI are demonstrated in section 4.3. The details of system hardware and prototype setup for proposed CMI are presented in section 4.4 and 4.5. Further, section 4.6 demonstrates the experimental results for proposed CMI. Finally last section provides the significance of the proposed CMI.

4.1 Proposed CMI With Single Dc Source By Using Three Phase Transfomers

Recently, R&D in multilevel converters and their applications have been very visible in the literature [124]. Particularly while systems are dealing with utility applications, transformer coupling often becomes essential. Such features are observed in Neutral point converter (NPC). In general numerous transmission and distribution systems are facilitated with NPC employing zigzag transformers. This class of converter is highly preferred because of the lower harmonic content and improved power quality aspects. In fact NPC with zigzag transformer size is quite larger because large numbers of components are utilized. However, in spite of that archetype, presented converter can effectively replace in such areas. This is because present CMI is coupled with low frequency three phase transformers. Further in presence of PWM operation, voltage and current waveforms are almost equal to that of NPC

converters performance. All these features facilitate the converter to operate perfectly for utility applications.

In the preceding chapter, Fig. 3.26 and Fig.3.30 illustrates the CMI with single dc source by employing single-phase transformers [126-127]. These classes of converters are extensively used in utility interfacing applications [128]. But these structures utilize the single phase transformers for each H-Bridge, which makes the converter size big and thereby increasing the cost. Meanwhile, Fig. 4.1 demonstrates H-Bridge multilevel inverter with single dc source and several low frequency three phase transformers, this make the size of the equipment come down with less price tag.

Now, coming to structure point of view, each primary terminal of the transformer is connected to an H-Bridge module so as to synthesize output voltages of $+V_{DC}$, Zero, $-V_{DC}$. Every secondary of transformer is connected in series to enhance the output voltage level. Further, each phase terminal is delta connected to restrain the third harmonic component. Fig. 4.1 expresses that, primary of each phase is three phase and secondary is single phase terminal. All three terminals are series connected to generate phase voltage. Therefore, each phase can be expressed independently. As a result each phase multilevel inverter can be depicted as an isolated H-Bridge cascaded multilevel inverter. We can obtain the relation between input and output voltages of three phase transformer as

$$\left[V_{AK};V_{BK};V_{CK}\right] = N\left[T\right]\begin{bmatrix} V_{ak} \\ V_{bk} \\ V_{ck} \end{bmatrix} \tag{4.1}$$

$V_{ak,}$ $V_{bk,}V_{ck}$ are primary terminal of phase “a”, phase “b” and phase “c” Where, T is transformation matrix and defined as

$$T = \begin{bmatrix} 2/3 & -1/3 & -1 \\ -1/3 & 2/3 & -1/3 \\ -1/3 & -1/3 & 2/3 \end{bmatrix} \tag{4.2}$$

Similarly, N is the transformation ratio (n_2/n_1) between primary and secondary and if there is a balanced input, then sum of each phase voltage would become zero.

$$V_{ak} + V_{bk} + V_{ck} = 0 \tag{4.3}$$

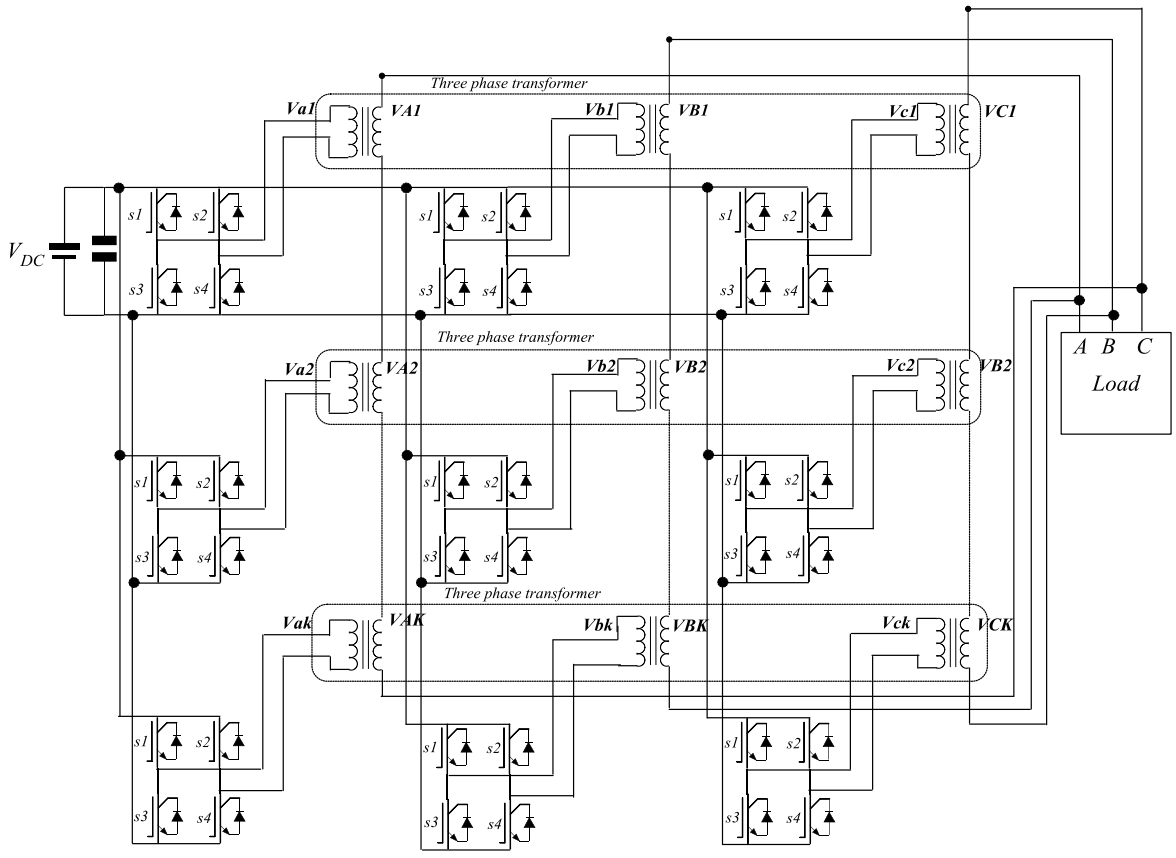


Fig. 4.1 Proposed multilevel inverter employing three-phase transformer

$$\begin{bmatrix} V_{Ak} \\ V_{Bk} \\ V_{Ck} \end{bmatrix} = N \begin{bmatrix} V_{ak} \\ V_{bk} \\ V_{ck} \end{bmatrix} \tag{4.4}$$

From (4.4) CMI with three-phase configuration, we are obtaining each phase output voltage of transformer as product of input voltage and transformation matrix *N*. But under

unbalanced condition, equation (4.4) is not satisfied because primary of transformer is connected to an H-Bridge cell generating V_{dc}, zero, -V_{dc}. So, the output voltage of V_{ak}, V_{bk}, and V_{ck} are equal to V_{dc}. Thus summation of three voltages is not equal to zero; due to this fact output voltage is unbalanced. However, equation (4.1) holds good for all conditions. In other terms, we can generate voltages at $V_{ak}=V_{DC}$, $V_{bk=}$-V_{DC}, and $V_{ck}=0$. Summation of such voltages will result to zero. However, the fundamental idea behind this is, magnetic circuit concept, notifying that flux at the primary of phase "a" will be equally influenced on phase "b" and phase "c" and becomes -1, so unbalanced relationship is also included in equation (4.1). As shown in Fig.4.1, proposed multilevel inverter secondaries are connected in series so that the output is the sum of three voltages. Thus it can be represented as

$$\left[V_{AS};V_{BS};V_{CS}\right]=\left[\sum_{i=1}^{k}V_{Ai};\sum_{i=1}^{k}V_{Bi};\sum_{i=1}^{k}V_{Ci}\right] \tag{4.5}$$

Herein, output voltage V_{AS} is defined as summation of phase "a" voltages i.e. $V_{A1}+V_{A2}+V_{A3}$. In a similar fashion corresponding summation will produce V_{BS} and V_{CS}. Further, to confirm the proposed CMI working pattern, output voltage characteristics are examined in the next section.

4.2 Output voltage characteristics

Output voltage of the three-phase transformer will be determined by combination of A, B and C voltages and there are three possibilities in output voltage of transformer. Switching pattern of each phase and output voltage of each transformer is shown in Fig. 4.2. It is to be noted that, presented voltages are resultant voltages of phase "a" and such voltages are obtained by summation of three voltages i.e $V_{ak,}$ V_{bk} and V_{ck}. However, Output voltage of proposed inverter is sum of secondary terminal voltages of transformer, which are connected

in series and all these are independent of switching range from $0<\alpha_k<\pi/2$. From Fig.4.2, output voltage of phase "a" (V_A) is figure out to be symmetrical in nature. In general form, Fourier expression can be written as:

$$V_{AK} = \sum_{n=1}^{\infty} b_{nk} \sin(n\theta) \tag{4.6}$$

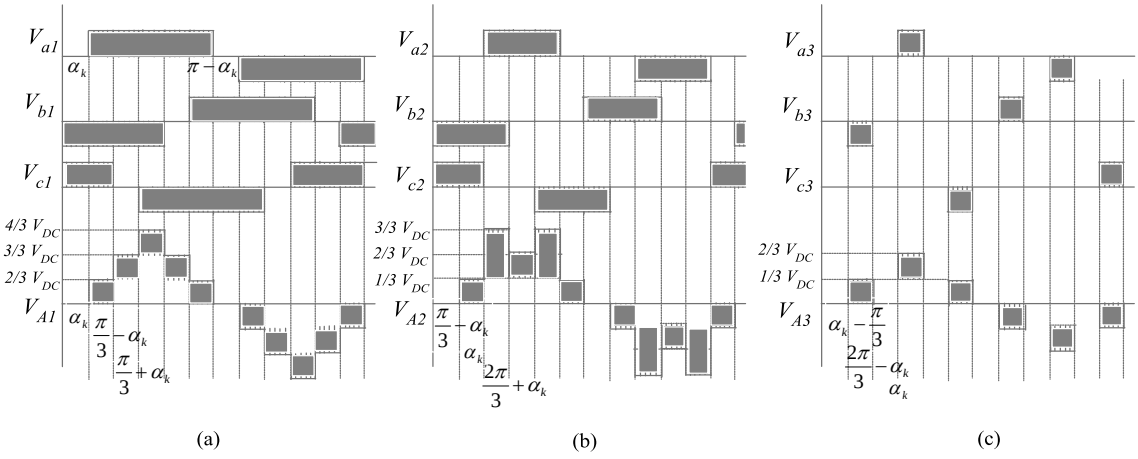


Fig.4.2 Details of swithing pattern and output voltage waveform characteristics for CMI with three-phase transfomers

Where b_{nk} is a constant.

Output characteristics of phase "a" voltage can be obtained between three switching ranges i.e $0 \le \alpha_k \le \pi/6$, $\pi/6 \le \alpha_k \le \pi/3$, $\pi/3 \le \alpha_k \le \pi/2$. And these are shown in Fig.4.2.

For case-1 i.e. $0 \le \alpha_k \le \pi/6$, $\pi/6$:

$$b_{nk} = \frac{4V_{dc}}{\pi}\left[\int_{\alpha_k}^{\pi/3-\alpha_k} \sin(n\theta)\,d\theta + \frac{3}{3}\int_{\pi/3+\alpha_k}^{\pi/3+\alpha_k} \sin(n\theta)\,d\theta + \frac{4}{3}\int_{\pi/3+\alpha_k}^{\pi/2} \sin(n\theta)\,d\theta\right]$$

$$\text{i.e. } b_{nk} = \frac{4V_{dc}}{n\pi}\cos(n\alpha_k) \tag{4.7}$$

For case-2, i.e. $\pi/6 \le \alpha_k \le \pi/3,\ \pi/3;$

$$b_{nk} = \frac{4V_{dc}}{\pi}\left[\begin{array}{l}\int_{\pi/3-\alpha_k}^{\alpha_k} \sin(n\theta)\,d\theta + \frac{3}{3}\int_{\alpha_k}^{2\pi/3-\alpha_k} \sin(n\theta)\,d\theta \\ + \frac{2}{3}\int_{2\pi/3-\alpha_k}^{\pi/2} \sin(n\theta)\,d\theta\end{array}\right]$$

$$b_{nk} = \frac{4V_{dc}}{n\pi}\cos(n\alpha_k). \tag{4.8}$$

For case-3, i.e. $\pi/3 \le \alpha_k \le \pi/2$

$$b_{nk} = \frac{4V_{dc}}{\pi}\left[\int_{\alpha_k-\pi/3}^{2\pi/3-\alpha_k} \sin(n\theta)\,d\theta + \frac{2}{3}\int_{\alpha_k}^{\pi/2} \sin(n\theta)\,d\theta\right]$$

$$b_{nk} = \frac{4V_{dc}}{n\pi}\cos(n\alpha_k). \tag{4.9}$$

From equations (4.7, 4.8, 4.9), Fourier progression is same. In a similar fashion Fourier transform for primary voltages of transformer V_{ak}, V_{bk}, V_{ck} are given as

$$V_{ak} = \sum_{n=1}^{\infty} b_{nk}\sin(n\theta)$$

$$V_{bk} = \sum_{n=1}^{\infty} b_{nk}\sin(n\theta - \frac{2n\pi}{3})$$

$$V_{ck} = \sum_{n=1}^{\infty} b_{nk}\sin(n\theta + \frac{2n\pi}{3}) \tag{4.10}$$

Which are 120^0 apart from each phase and coefficients of b_{nk} and V_{ak} are half wave symmetries, henceforth odd function can be written as

$$b_{nk} = \frac{4V_{dc}}{n\pi}\cos(n\alpha_k). \tag{4.11}$$

Using equation (1), output phase voltage of V_{AK} can be expressed as:

$$V_{AK} = \sum_{n=1}^{\infty} b_{nk}\sin(n\theta) - 1/3 \times \sum_{n=1}^{\infty} b_{nk}\left(\sin(n\theta) + 2\sin(n\theta)\cos(\frac{2n\pi}{3})\right) \tag{4.12}$$

In above equation if *n=3, 9…3(p-2), 3p,* then equation becomes zero i.e.

$$V_{AK} = 0 \tag{4.13}$$

This represents, all triplen harmonic component does not appear in the three-phase output voltage.

And if *n=1, 5, 7, 11…..p,* then equation becomes

$$V_{AK} = \sum_{n=1}^{\infty} b_n \sin(n\theta) \tag{4.14}$$

Thus least harmonics in output waveform will be *5, 7, 11, p-2, p.*

4.3 Performance Verifications

Herein, performance of the proposed architecture is verified by using three major switching techniques namely; fundamental frequency, selective harmonic elimination and sine triangle PWM. The main idea behind the operation with different techniques is to explore the potential of the proposed CMI. However, to verify the performance of the proposed CMI, prototype experimentation is carried out in the laboratory and adequate results are presented to confirm the findings.

4.3.1 Fundamental Frequency Approach

Before proceeding, let's compare the output waveform characteristic of conventional CMI and the proposed CMI with three-phase transformers. This is demonstrated in Fig.4.3 (a). However, conventional converter characteristic waveform and its switching fashion is quite different when compare to the proposed one. Note that, three single phase transformer produce seven level output waveform by using three switching angles. In fact, minimum harmonic switching angle can be easily solved by the Newton-Raphson approach and this kind of approach is observed in numerous publications [109]. Later, Fig.4.3 (b) gives the details of output characteristics of CMI with three-phase transformers and output waveform.

At this point one should observe that switching criterion is quite different and in particular Fig.4.3 (b) provides the characteristics at each transformer terminal in phase "a". Thus one can finds the difference between the conventional switching and proposed switching. However, mathematical verifications are already done in preceding sections.

To demonstrate the fundamental frequency approach, consider the theoretical output voltage waveforms V_{A1}, V_{A2} and V_{A3} of each of the three-phase transformers. The output voltages are connected in series to produce a net output voltage i.e. $V_{A1}+V_{A2}+V_{A3}$ and this situation is shown in Fig.4.3 (b). Output characteristics shown in Fig.4.3 (b) are the solutions from (4.16). The phase voltage V_{A1} is obtained by three input voltages i.e. v_{al}, v_{b1} and v_{c1} (observe Fig.4.1). In a similar fashion V_{A2} and V_{A3} can be obtained. As far as concerned these output voltages are independent of switching angles, range from $0<\alpha_k<\pi/2$. So output voltage can be represented as:

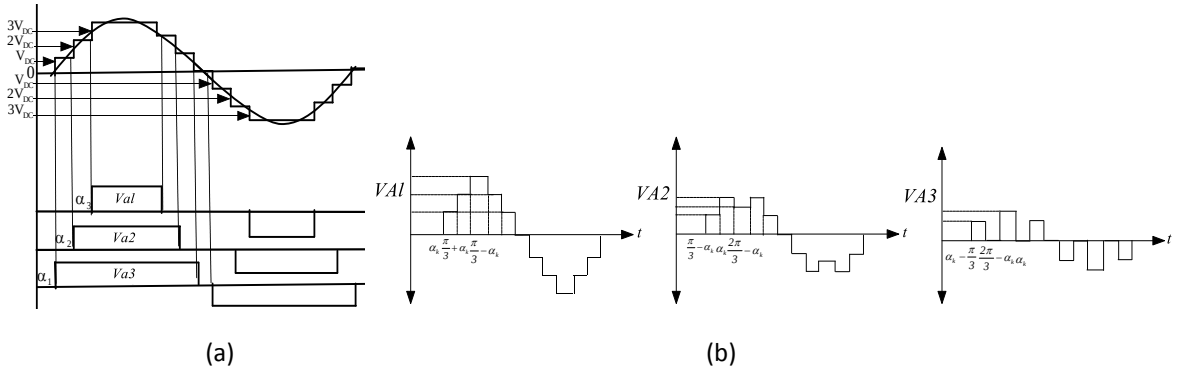


Fig.4.3 Details of waveforms for (a) conventional seven level inverter,

(b) proposed CMI with three-phase transformers

$$V_{out} = 4V_{DC} / n\pi(\cos(n\alpha_1)+\cos(n\alpha_2)+\cos(n\alpha_3)) \quad (4.15)$$

Aforementioned, output voltages of converter are controlled by switching angles, which are represented by α_1, α_2, α_3, all these angles lie between 0 and $\pi/2$ and it can be represented as $0\leq \alpha_1\leq \alpha_2\leq \alpha_3\leq\pi/2$. In practice by controlling the switching angles, fundamental component can

be synthesized and meanwhile, 5th and 7th harmonic components can be suppressed. But interesting feature is that 3rd harmonic component can be completely eliminated because secondary side of transformer is delta connected. Indeed, from above scenario, a set of nonlinear equation can be written to find switching angles.

$$\begin{aligned} &\cos(\alpha_1)+\cos(\alpha_2)+\cos(\alpha_3)=3m\pi/4 \\ &\cos(5\alpha_1)+\cos(5\alpha_2)+\cos(5\alpha_3)=0 \\ &\cos(7\alpha_1)+\cos(7\alpha_2)+\cos(7\alpha_3)=0 \end{aligned} \tag{4.16}$$

Table 4.1
Calculated Switching Angle Based On the Modulation Index

Modulation Index (M)	α_1	α_2	α_3
0.1	76.42	-	-
0.2	61.93	-	-
0.3	50.22	86.24	-
0.4	44.21	74.33	-
0.5	40.80	66.12	89.45
0.6	39.44	58.61	83.10
0.7	35.35	53.90	74.50
0.8	29.80	54.46	65.55
0.9	17.76	43.05	63.21
1	11.7	31.27	58.60

Where, m is the modulation index, which is varied from 0.1 to 1. Herein, switching angles of each switch are calculated by Newton-Raphson method on the basis of area of each switch. All delay angles can be determined by applying linearization method to each area. These prospects are useful in eliminating lower order harmonic components. Nevertheless, by solving above limitation with Newton-Raphson method three switching angles α_1,α_2, α_3 can be predicted, which are less than $\pi/2$.

Fig.4.4 illustrated the calculated switching angles and actual switching angles at different modulation indexes. It can be observed from above Table 4.1 that, at modulation index 1 switching angle of transformer one is 11.70^0 and its extinction angle is 168.3^0, which produces output voltage V_{Al} shown in Fig.4.3b. Similarly for transformers two and three

switching angles are 31.2^0 and 58.6^0 and there corresponding extinction angles are 148.8^0 and 121.4^0. From Fig.4.4 one can observe a slight difference between actual and calculated switching values, but by adjusting these values manually we can solve the problems. Rest of the switching angles from M=0.1 to 1 were given in table 4.1.

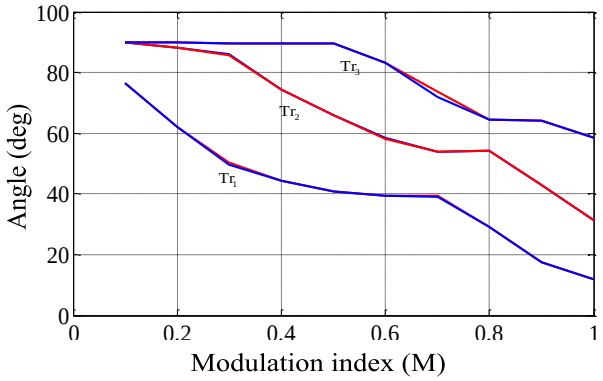


Fig.4.4 Variation of switching angles based on different modulation indexes

4.3.2 Multilevel Selective Harmonic Elimination PWM Technique

The multilevel SHEPWM technique has a theoretical potential to achieve the highest output power quality at low switching frequencies in comparison to other methods [112]. Due to mathematical complexity SHEPWM is less preferred. But still this method is effective in suppressing significant harmonics in the system. Applying SHEPWM to multilevel converter is well presented by several authors [127]. But in present case we adopt this technique to the CMI with three-phase transformers.

4.3.2.1 Harmonic elimination and phase shift

Consider the generalized three level SHEPWM shown in Fig.4.5 and let m be the number of chopped switching angles per quarter-cycle. The output waveform is assumed to be odd quarter wave symmetry, whose amplitude equals E. Because of odd quarter wave symmetry, the dc component and even harmonics are equal to zero. Thus generalized Fourier expression of the three level SHEPWM can be written as:

$$V_{out}(wt) = \sum_{n=1}^{\infty} a_n \sin(nwt) \tag{4.17}$$

$$a_n = \frac{4E}{n\pi} \sum_{K=1}^{M} (-1)^{k+1} \cos(n\alpha_k) \tag{4.18}$$

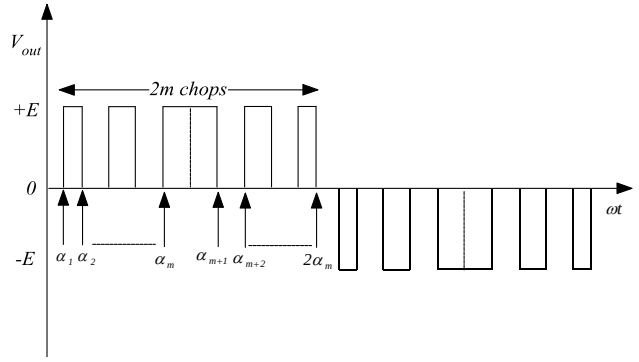


Fig.4.5 Details of generalized three-level SHEPWM waveform

Where M is the number of switching angles per quarter [116], and α_k is switching angles which must satisfies following conditions

$$\alpha_1 < \alpha_2 < \alpha_3 ..... < \alpha_M \tag{4.19}$$

E is the amplitude of the dc source and n is the harmonic order.

This entire prospect is for only single cell and to extend further switching, phase shifting is carried out for each subsequent series cells. In the present case, consider β as the phase shifted angle. However, in practice if the number of switching angles in a quarter period is m, then the first significant harmonic crest for each cell is just above 2 mth harmonic. One of the crest harmonic can be eliminated by the phase shift, and other will be suppressed. If the 2m+3 harmonic is selected for elimination, the phase shift angle β can be obtained as

$$\beta = \frac{2\pi}{3(2m+3)} \tag{4.20}$$

At the moment, consider the proposed three cell three phase converter. Corresponding switching for each cell is obtained by solving a set of nonlinear equations. Herein, M is considered as five, i.e. basic quarter waveform is chopped at five instants, so that low order harmonic is predominantly reduced. To find switching angle consider the below inequalities;

Herein, for each cell, generalized expression is defined by including phase shift angle β.

$$a1 = \frac{4E}{n\pi}[\cos n\alpha_1 - \cos n\alpha_2 + \cos n\alpha_3 + ...\cos \alpha_k] \tag{4.21}$$

$$a2 = \frac{4E}{n\pi}[\cos n(\alpha_1 - \beta) - \cos n(\alpha_2 - \beta) + \cos n(\alpha_3 - \beta) + ...\cos(\alpha_k - \beta)] \tag{4.22}$$

$$a3 = \frac{4E}{n\pi}[\cos n(\alpha_1 + \beta) - \cos n(\alpha_2 + \beta) + \cos n(\alpha_3 + \beta) + ...\cos(\alpha_k + \beta)] \tag{4.23}$$

Resolving above inequalities $\alpha_1, \alpha_2, \alpha_3 \ldots\ldots\ldots \alpha_k$ values are obtained. For other two phases 120° apart is considered for switching. Newton-Raphson approach is utilized to solve above inequality. From structure point of view secondary terminals are delta connected, so third harmonic and its multiples are automatically eliminated. Due to this fact, 1, 5, 7, 11, 13 harmonics are considered for chopping. In practice, with this scenario output voltage does not consist of any harmonics upto 13^{th}, except fundamental. As the numbers of chopping angles are low, switching losses are also drastically reduced. But in case of conventional structure high quality output voltages are not achieved as three phases are individual and so low order harmonics are primarily observed, thereby number of chopping are to be increased to achieve qualitative output voltages with better THD. Nevertheless, to demonstrate the effectiveness of presented CMI, conventional CMI verifications are also incorporated with same number of chopping.

Generalized equation for switching first H-Bridge cell are illustrated below. Solving above inequality with Newton-Raphson approach α_1, α_2, α_3, α_4, α_5 are calculated.

$$\begin{aligned}
&\cos(\alpha_1)-\cos(\alpha_2)+\cos(\alpha_3)-\cos(\alpha_4)+\cos(\alpha_5)=3m\pi/4\\
&\cos(5\alpha_1)-\cos(5\alpha_2)+\cos(5\alpha_3)-\cos(5\alpha_4)+\cos(5\alpha_5)=0\\
&\cos(7\alpha_1)-\cos(7\alpha_2)+\cos(7\alpha_3)-\cos(7\alpha_4)+\cos(7\alpha_5)=0\\
&\cos(11\alpha_1)-\cos(11\alpha_2)+\cos(11\alpha_3)-\cos(11\alpha_4)+\cos(11\alpha_5)=0\\
&\cos(13\alpha_1)-\cos(13\alpha_2)+\cos(13\alpha_3)-\cos(13\alpha_4)+\cos(13\alpha_5)=0
\end{aligned} \tag{4.24}$$

Rests of the inequality are solved in similar fashion, but by including angle β. To verify theoretical fact, experimental verifications are presented in succeeding section.

4.3.3 Multilevel Sinusoidal PWM Technique

4.3.3.1 PWM techniques

In chapter 2, Fig.2.9 provides the complete details of PWM techniques. Author [125] had reported about multicarrier based PWM techniques. Aforementioned, carrier based PWM approaches are quite good to handle. According to literature study two major carrier based PWM approaches are presented. Specifically, phase shifted PWM and level shifted PWM techniques. An In-depth assessment between PWM methods can be found in [99]. In brief, rather than level shifted PWM, phase shifted PWM technique had finite merits like; no rotation in switching pattern, less switching losses and easy to implement. In the present configuration we adopt phase shifted PWM approach to the proposed CMI.

4.2.3.2 Switching and phase shifting

For multilcell switching, phase shifting is an important criterion. Present CMI utilizes nine H-bridge cells and for each phase, it uses three cells. Thus three carriers are chosen with appropriate phase shift. In general with unipolar switching multicell converter requires *(m-1)/2* triangle carriers. But in the present case *(m-1)/4* carriers are required, which signifies that carrier count is drastically reduced. For example, for thirteen level output waveform (13-1)/2 carriers are needed in conventional structures, where as it is half in present case i.e. *(13-*

1)/4. Besides, all triangle carriers in conventional proposed topologies have same frequency and same peak to peak amplitude, but then phase differences between two adjacent carriers are given by:

$$\varphi_{cr} = 360 / (m-1) / 4 \tag{4.25}$$

By using above equation (4.25) appropriate phase shift are incorporated for conventional and proposed topologies.

4.3.3.3 Unipolar switching

Unipolar switching scheme is considered for generating pulses. Fig.4.6 (a) provides details of single H-Bridge operation and (b) unipolar switching criteria. Herein, the thirteen level voltage source modulation is accomplished by comparing the duty cycles with a set of carrier waveforms. The switching function V_{sin} is compared with triangular carrier V_{tri} of frequency f_s and with definite amplitude.

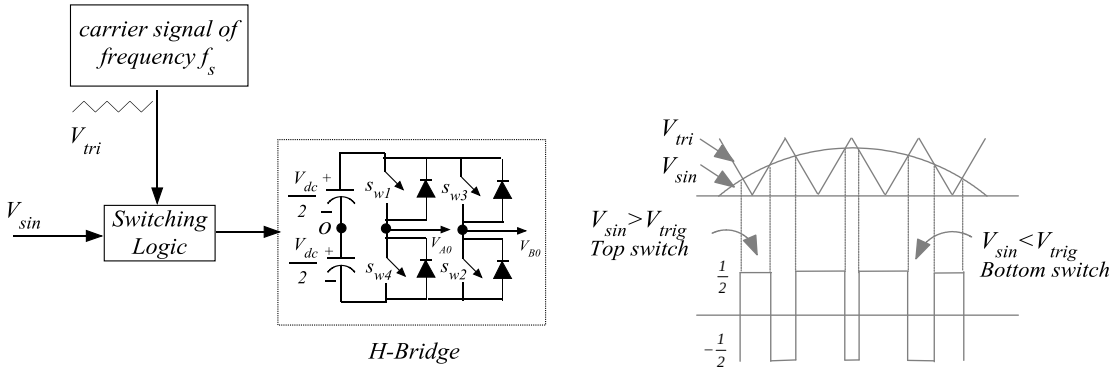


Fig.4.6 a) Details of single H-Bridge Cell b) Unipolar modulation of one arm of H-Bridge of VSC

Switching function V_{sin} is modulated with carrier following the principle of unipolar PWM i.e.

Condition:1.1 $V_{sin} > V_{tri}$. Then SW1 is on and resultant voltage $V_{A0} = +1/2Vdc$

Condition:1.2 $V_{sin} < V_{tri}$, Then SW2 is on and resultant voltage $V_{A0} = -1/2Vdc$

In similar fashion for other phase leg of H-bridge,

Condition:2.1 $V_{sin} > V_{tri}$ Then SW3 is on and resultant voltage $V_{BO} = +1/2Vdc$

Condition:2.2 $V_{sin} < V_{tri}$ Then SW2 is on and resultant voltage $V_{BO} = -1/2Vdc$

Therefore net voltage levels obtained for one H-Bridge is V_{dc}, *0*, $-V_{dc}$. The process is repeated for other H-bridges with a carrier phase shifted by the corresponding angles. Sum of all these three voltages results in producing resultant output voltage waveform.

4.4 System Hardware

Details of prototype setup for proposed CMI are demonstrated in Fig.4.7. Further, for the experimentation FPGA based module was used. An analog expansion daughter board is interfaced between the FPGA module and the insulated gate bipolar transistor (IGBT) inverter. To program the FPGA, two distinct software packages are used in Matlab and Xilinx ISE. In Matlab the programme is written, and with the help of ISE the program is configured to run the FPGA. The main bridge between the two packages is System Generator which is added as a part of Matlab to convert the Simulink math code to VHDL code that the ISE recognizes. Later, proposed circuit topology was realized with system generator and appropriate VHDL code is generated and dumped to Xilinx sparatn-3 FPGA board. Fig.4.7 indicates the construction of CMI using three-phase transformers.

Total nine H-bridge modules are used. The measured quantities are the load currents, load voltages, which are measured with hall-effect voltage and current transducers. Input dc voltage is taken as 60 V and for transformers, transformation ratios are taken as 1:1. With the help of FPGA, PWM signals are generated. Target output voltage and its frequency are 110 Vac and 50 Hz respectively. For experimentation highly inductive load is considered.

Detailed component list is given in Table 4.2. To be specific, prototype experiments are carried out with aforementioned switching techniques for the proposed CMI.

Fig.4.7 Details of Prototype set up for the proposed cascaded multilevel converter with three-phase transformers

Table 4.2
Hardware specifications

Items	Specifications and Features
Switching Devices	FGH20N60UFD 600 V, 20 A Fair Child Semiconductors
Transformers	EI lamination (3 EA) 1:1 ratio
Input Voltage	1-single DC, 60 V
Output Voltage	13-level , 220 V
FPGA	Xilinx Spartan3 Device Generate PWM signals
Translator	SN74LVCC3245A Bi-directional Voltage Translator
Current Sensor	LTS 25-NP 25 A
Voltage Sensor	LV 25-P 1200 V
Load Parameters	R=400 Ω, L=1000 mH

4.5 Experimental Results

4.5.1 Fundamental Frequency Approach

Fundamental switching criterion is demonstrated in section 4.3.1. Switching is carried out with three switching angles per quarter period. Fig.4.8 provides the experimental results

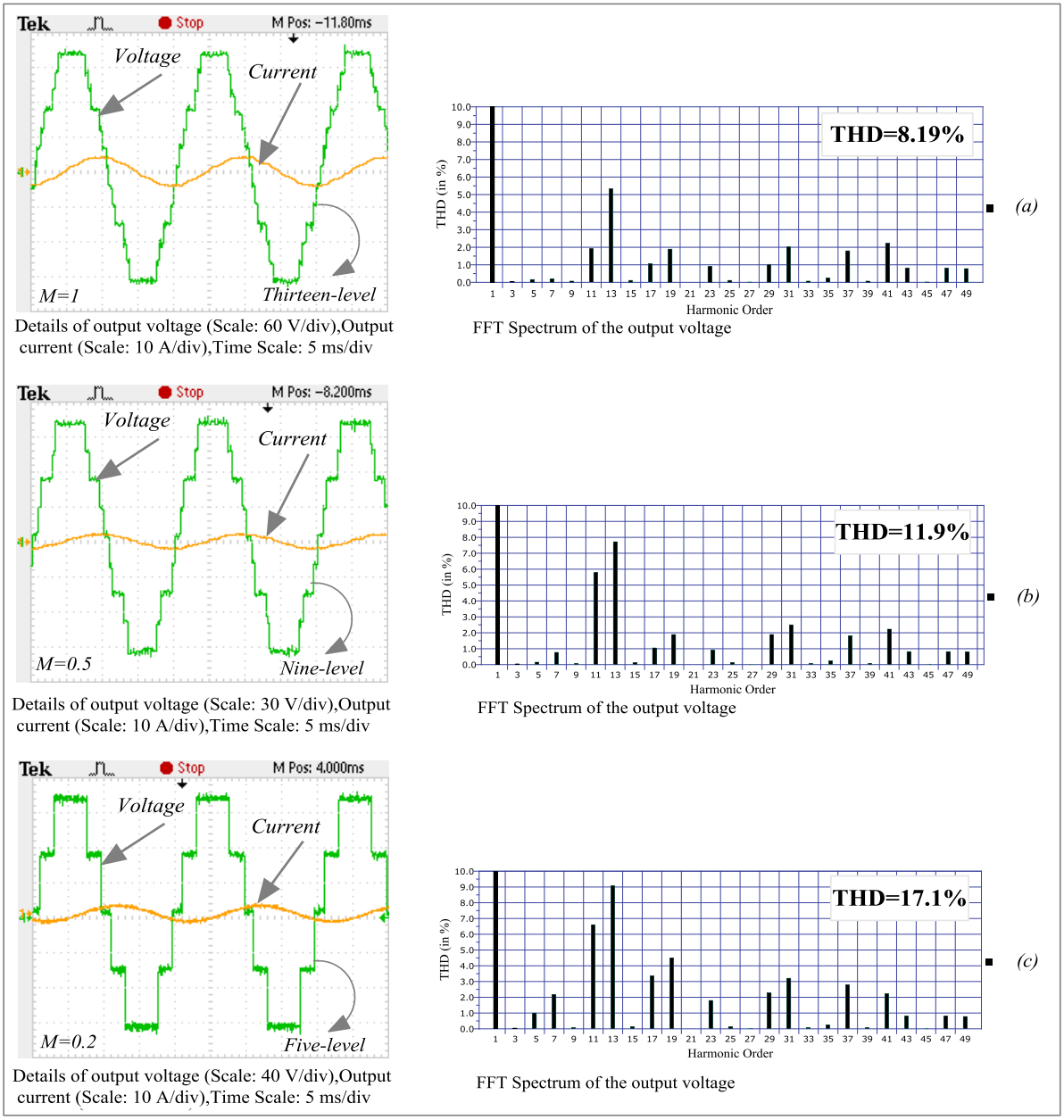


Fig.4.8 Performance of the proposed cascaded multilevel inverter with by using fundamental frequency approach at modulation index 1, 0.5, and 0.2 (from top to bottom)

of the proposed CMI. For simplicity, results of phase "a" only are presented. All the waveforms for parallel connected resistive and inductive loads (400 Ω + 1000 mH) were taken at the modulation indexes 1.0, 0.5 and 0.2 respectively. Observing Fig.4.8 at modulation index 1, we can notice that 13 level performances are achieved with just nine H-bridge cells. This defines the inherent potential of a converter. In fact this is an important finding regarding the proposed CMI.

Further in Fig.4.8 information of FFT spectra for corresponding voltages are also reported. Observing THD, voltage harmonics gradually increases with decrease in modulation index and at modulation index 1 its THD is 8.19% and at 0.1 it is around 17.1% and lowest harmonic component is 11^{th}, rest all the harmonics are suppressed and as modulation index reduces all odd harmonic components are noticed. But for all the modulation indexes it is evident that third harmonic component is completely absent.

4.5.2 Selective Harmonic Approach

Multilevel selective harmonic approach is demonstrated in section 4.3.2. With the help of five switching angles the proposed CMI is operated. As before prototype experiments are carried out for the proposed and conventional CMI with same load parameters. Fig.4.9 highlights the performance of the proposed CMI with SHEPWM approaches. Output waveforms and FFT spectra are provided. Validation is done for three modulation indexes i.e. 1, 0.5 and 0.2. Observing the output voltage of the proposed CMI at modulation index 1, it is almost sinusoidal in fashion and respective FFT spectra correspond complete elimination of lower order harmonics.

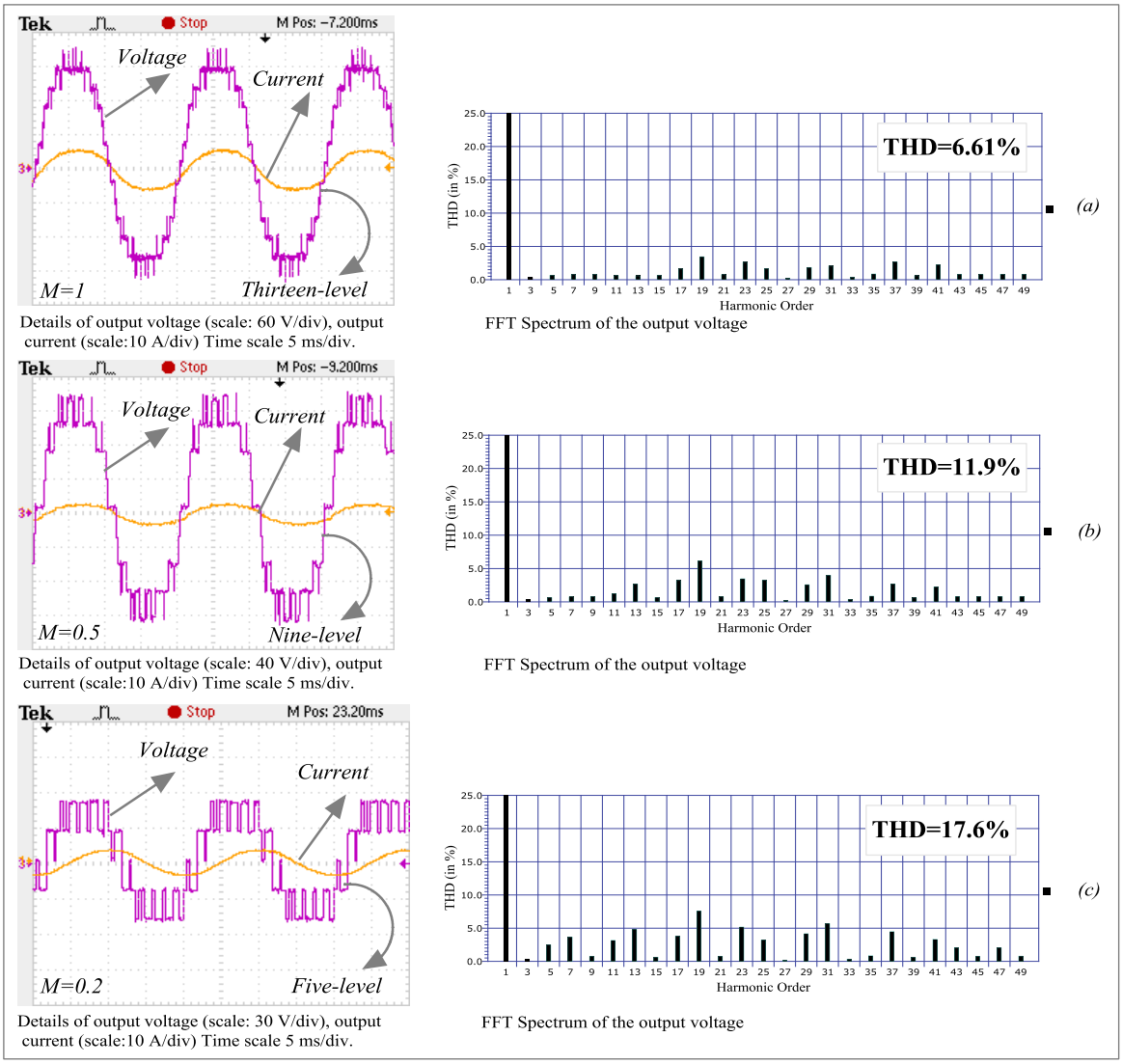


Fig.4.9 Performance of the proposed cascaded multilevel inverter with by using selective harmonic PWM approach at Modulation index 1 ,0.5, 0.2 (from top to bottom)

Later, on scrutinizing Fig.4.9, difference in output waveform could be predicted. In fact, at modulation index 1 voltage level becomes twice as compared to traditional CMI (CMI with single-phase transformers). Additionally, as modulation index decreases level reduces but for all modulation indexes third and its multiple harmonics are completely eliminated. On the other side, conventional FFT spectra specifies presence of lower order harmonics particularly at modulation index 1 and for all modulation indexes 3rd harmonic

component are also noticed. However, attractive feature of SHEPWM is that, numbers of switching is reduced per cycle and so reduce the switching losses. In addition, predominant harmonics are completely eliminated and thereby facilitate an option to design output filter. But, one distinct limitation of SHEPWM is prerequisite of offline calculations to compute the angles for variety of modulation indexes.

4.5.3 Sinusoidal PWM Approach

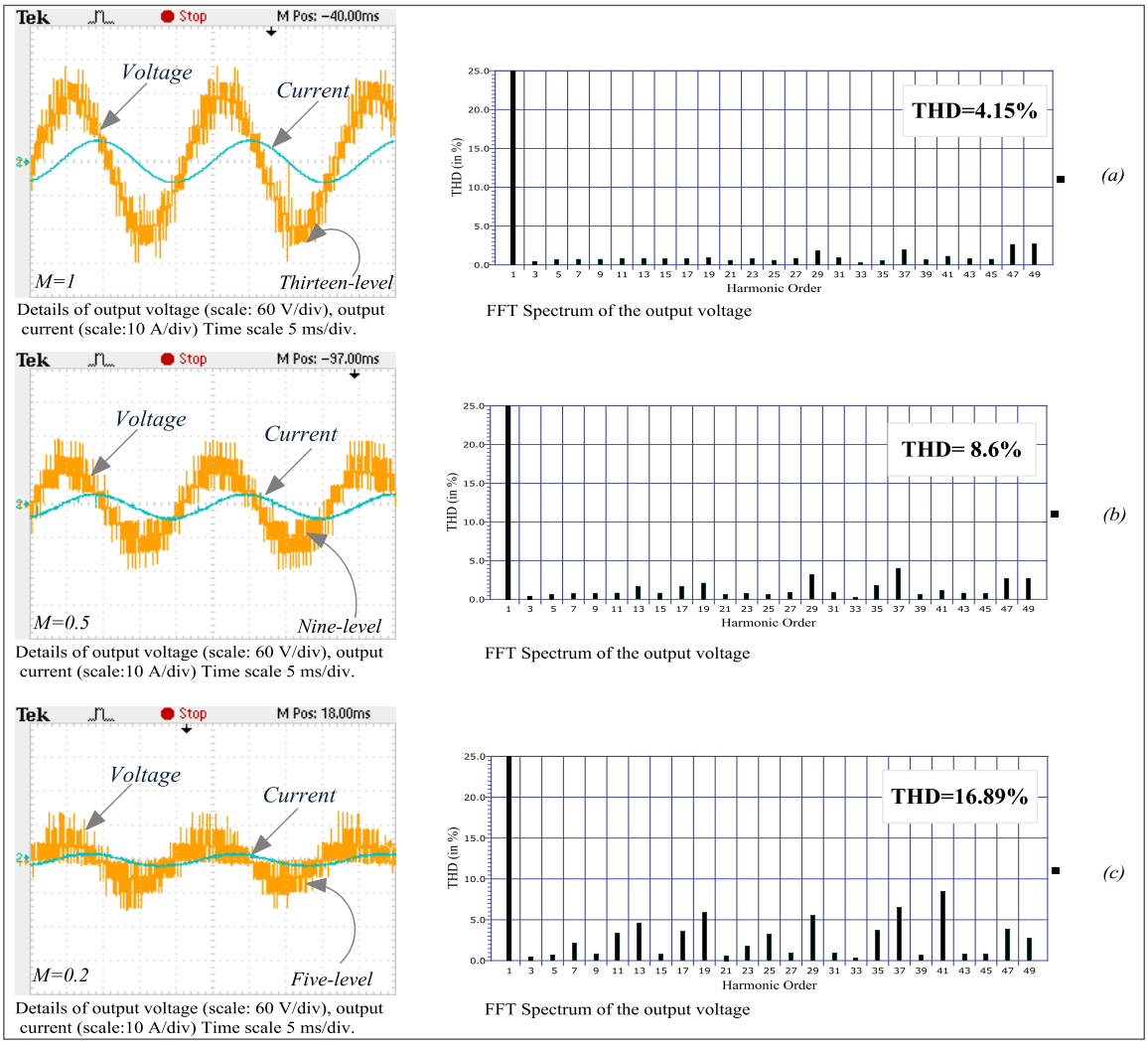


Fig.4.10 Performance of the proposed cascaded multilevel inverter with by using sinusoidal PWM approach (a) & (b) Modulation index= 1, (c) & (d) Modulation index = 0.8, (e) & (f) Modulation index = 0.6, (g) & (h) Modulation index= 0.4. (i) & (j) Modulation index= 0.2

Switching criterion is demonstrated in section 4.3.3. Proposed CMI is set to operate at a switching frequency of 5 kHz. Fig.4.10 highlights the performance of the proposed CMI at different modulation indexes. Observing verifications, it is clear that output waveforms are very close to sinusoidal at modulation index 1 and corresponding FFT spectra signifies complete elimination of lower order harmonics. Note that, in previous chapter 3 all traditional inverters performances are presented with PWM approach. But, performances are disaster when compared to the proposed one. Adding to that, FFT spectra specifies the presence of low order harmonics like; 3, 5, 7, 11, 13, and 15 (monitor in previous chapter.3). Further, as modulation index decreases harmonic content increases dramatically. However, such drastic changes are not visible in the case of the proposed CMI. Furthermore, one of the interesting observations is that the proposed CMI response is quite impressive under lower modulation indexes with SPWM. In fact output voltages and FFT spectra are excellent and promising when compared with other techniques. Overall, with the help of prototype experiments and findings, potential of the proposed CMI is explored.

4.5.4 Important Feauters of Proposed CMI

Besides above issues, conventional cascade multilevel inverters use a circulating switch pattern in order to maintain the same ratio in switch utilization. Therefore, they employ switches which are identical in the voltage and current ratings. Assuming that the magnitude of the output voltages and output power are equivalent, the voltage ratings of each switch are determined by the number of series-connected switches. Consequently, we can say that the proposed method is more advantageous as far as numbers of components are used. Most importantly there is significant improvement in output voltage quality which is not possible in other structures. In addition, usually, these traditional multilevel inverters employ

a three 3-phase low-frequency transformer at the output terminal for a high-power grid connection. In this point, the proposed circuit topology has a valuable merit. Considering that the output voltage is synthesized by an accumulation of each transformer output, it does not require an additional transformer for galvanic isolation. Although the proposed scheme needs three three-phase transformers, the cost and size will be slightly increased, because the capacity of the transformer is 1/3 of the transformer which is applied to the conventional method.

4.6 Comparitive Study

After comparing it is observed that, conventional multilevel inverter requires too many DC sources and DC capacitors to generate 13 output voltage levels. We can find that a conventional multilevel inverter needs 18 DC sources with 72 switches or single dc source with 18 single-phase transformers to generate 13 level output. In the case of CMI with reduced sources it requires 9 DC sources with 84 switches and in Hybrid converters, 15 DC bus capacitors are required for the generation of 13-level outputs. But the proposed converter requires only single dc source. Detailed comparison is given in Table 4.3.

Table 4.3

Components Comparison with Conventional Cascade Multilevel Inverter

Item / Type	Conventional Cascade H-bridge	Conventional CMI with unequal DC sources	CMI with Minimum DC sources	Hybrid CMI with bottom three-leg inverter	Hybrid CMI bottom H-bridge inverter	CMI with single phase transformers	CMI with three-phase transformers
Main Switching Devices	72	36	84	106	60	72	36
DC-Bus Capacitors	18	36	9	15	12	1	1
Input DC sources	18	18	9	1	3	1	1
Output Transformers	0	0	0	0	0	18	3

Further, it is also viable to compare proposed CMI with conventional multilevel inverters. So, to explore the significance of proposed CMI with traditional multilevel inverter

Table 4.4

Components Comparison with Traditional Multilevel Inverter

Item / Type	Switch	Clamping diode	Balancing capacitor	DC-Bus	Transformers
Diode Clamped	$(m-1)\times 2\times 3$	$(m-1)\times(m-2)\times 3$	N.A	$(m-1)\times 3$	N.A
	72	396		36	
Flying capacitor	$(m-1)\times 2\times 3$	N.A	$[(m-1)\times(m-2)]\times 3/2$	$(m-1)\times 3$	N.A
	24		210	36	
Cascaded FB-cell	$(m-1)\times 2\times 3$	N.A	N.A	$(m-1)\times 3/2$	Multi-winding outputs
	72			18	
Proposed converter	$(m-1)\times 2/2$	N.A	N.A	single	three
	36				

Table 4.4 is presented. On investigating in case of diode clamped, a large number of clamping diodes are the worst drawback. Plenty of balancing capacitors are a weak point in flying capacitor type inverter. Among them, the cascade full-bridge cell type looks good to increase the number of output levels. However, each cell has an isolated power supply. The provision of isolated supply becomes a limitation in the power electronic circuit design. Moreover, complexity in control and voltage imbalance problems also arises. Nevertheless, such problems are evaded with proposed technique, because it uses single dc source.

Further, comparing with Neutral Point Clamped (NPC) inverter, the proposed CMI confirms promising characteristics. Frequently NPC inverters employing zigzag transformers is used in transmission and distribution systems, because converter provides high quality voltage and current waveforms with lower harmonic content. In reality NPC with zigzag transformer size is quite larger because large numbers of components are utilized. However, in-spite of that archetype, presented converter can effectively replace in such areas. This is

because present CMI is coupled with low frequency three phase transformers. Further in presence of PWM operation, voltage and current waveforms are almost equal to that of NPC converters performance. All these features facilitate the converter to operate perfectly for utility applications.

4.7 Summary

This chapter presented a new version of cascaded multilevel inverter, which employed a single dc input source and low frequency three-phase transformers. Performance of the proposed CMI is investigated with three switching techniques namely, fundamental frequency switching, selective harmonic elimination PWM and sinusoidal PWM approaches.

Fundamental frequency approach to the proposed CMI has definite advantages like; little transition loss of switch due to low switching frequency and reduced electromagnetic interference, which is suitable for high voltage applications but on the other hand, it is much difficult for a time variable non-liner system due to its complicated off-line computation algorithms.

Selective harmonic elimination PWM approach to proposed version of CMI provides the highest quality out voltages. Observing the CMI performance, harmonic content is drastically reduced and lowest harmonic content observed is 17^{th}, thus SHEPWM attains high quality output waveforms with reduced switching frequency. This feature facilitates for high power application, but an important limitation of SHEPWM is complicated hardware implementation.

Sine triangle PWM approach for present converter provides excellent performance. On Observing FFT spectra, least harmonic component noticed at modulation index 1 is 37^{th} and such performance is similar to 48 pulse converter (NPC-with zigzag transformers).

SPWM approach is easy to handle and implement, particularly while dealing with the time variable non-linear systems. Thus converter can be easily implemented for utility applications like STATCOM (static synchronous compensators), SSSC (static series compensators) UPQC (unified power quality conditioners) etc.

Chapter 5

Proposed Active Power Filter

Introduction to Active Power Filter

Proposed System Configuration

Control Strategy

Simulation Results and System Performance

Verifications with Real Time Digital Simulator

Summary

Chapter 5

In the previous chapter proposed cascade multilevel inverter with single dc source are discussed and drawbacks of such inverters are also demonstrated. However, it is concluded that proposed version of CMI is suitable for grid connected systems and FACT devices. So In this chapter, proposed architecture is introduced as an active power filter, which is a FACTS device. The proposed APF is verified with Real time digital simulator (OPAL-RT). This chapter is organized as follows. Section 5.1 provides the details of active filters and their importance in the power network. Section 5.2& 5.3 presents the details of proposed APF and control strategies. The ***Simulation*** *and* ***Real Time Verifications*** *are presented in Sections 5.4 and 5.5 respectively.* Finally Section 5.6 states all concluding remarks.

5.1 Introduction to Active Power Filter

Electrical power is perhaps the most essential raw material used by commerce and industry today. It is an unusual commodity because it is required as a continuous flow. From the consumers' point of view continuity of supply is an important aspects but in the present days, due to presence of non-linear loads continuity seems to be distractive and it's all because of power quality problems [129]. It is important to realize that the electrical load is not static. Differences in duty cycles of equipment and variations in working patterns contribute to a constantly changing load pattern. This results in generating harmonics [130]. Today harmonics is a buzz word heard form electrical utilities to customers. While harmonic voltages and currents are, by themselves, imperceptible, the physical phenomena that accompany them are perceivable. The adverse effects of harmonics in electrical power systems are very real, and failures related to voltage and current harmonics very often occur without warnings [133]. Beginning from semiconductor devices every load is non-linear in

nature and due to this, voltage and current waveforms are non-sinusoidal in nature, this represents existence of harmonics. As more and more variable frequency devices (VFDs), electronic

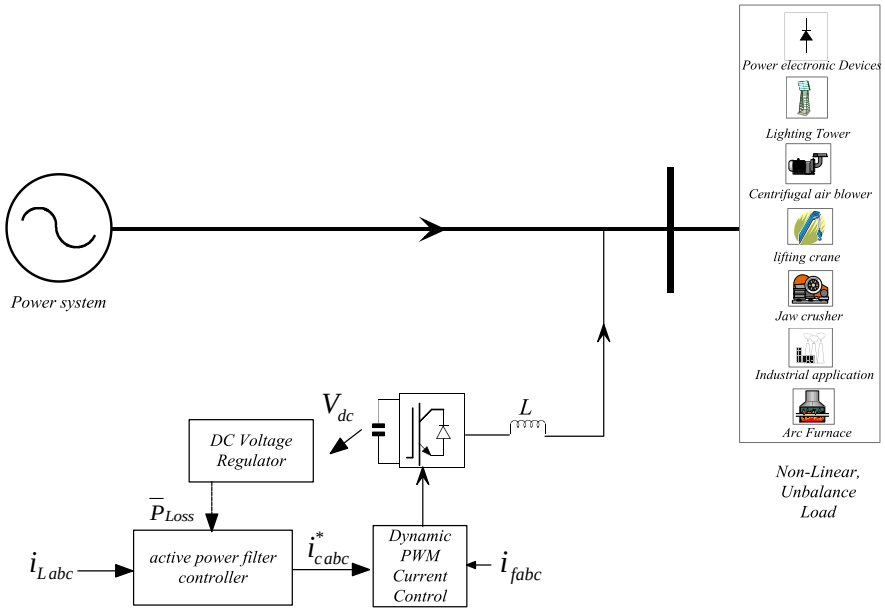


Fig.5.1 Simplified diagram of Active Power filter applied to non-linear loads in the power system

ballasts, battery chargers, and static VAR compensators are installed in facilities, the problems related to harmonics are expected to get worse [131-132]. Just because harmonics is becoming a more prevalent problem power conditioners became prominent. In this criterion, several APF (active power filters) are developed for harmonic compensation in the power networks [135-138]. Fig.5.1 illustrates simplified diagram of APF applied to a power system. Several authors had already built different APFs with different topologies [139-140].

5.2 Proposed System Configuration

The proposed cascaded multilevel inverter topology is presented as active filter for harmonic isolator in power network and arrangement is shown in Fig.5.2. The system is configured three-phase three-wire with *50 Hz* supply. APF is connected parallel to the system

at the PCC (point of common coupling). Thus CMI act as voltage source and is capable of blocking harmonic current that flow from the non-linear loads. Proposed structure is adopted with i_d-i_q strategy. This is demonstrated briefly in next section.

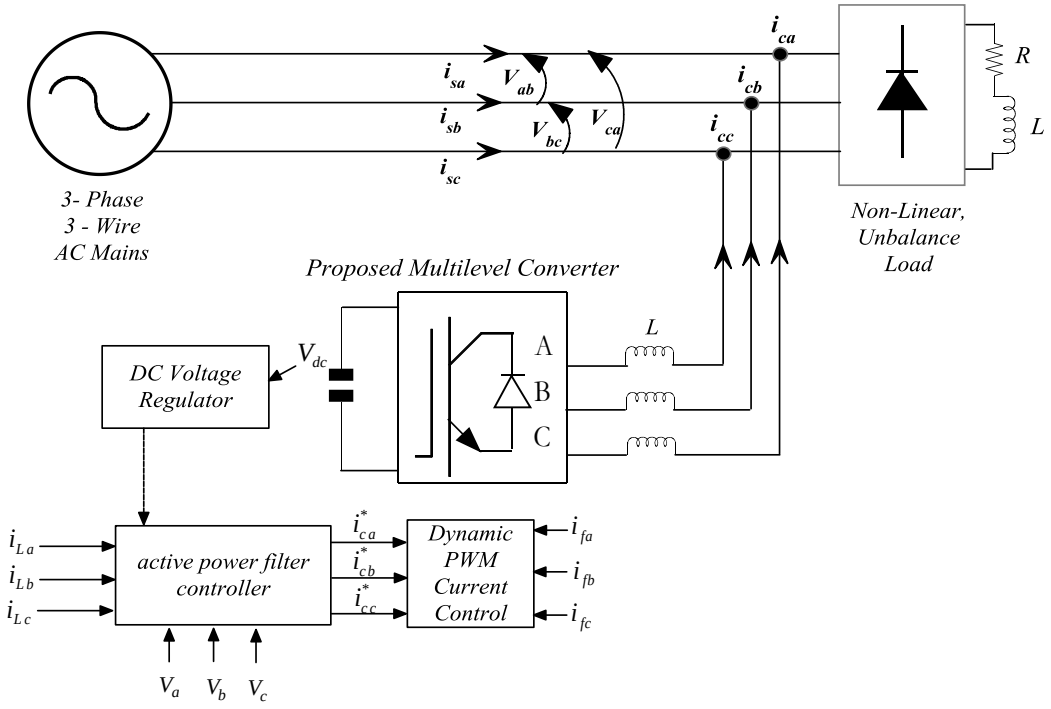


Fig. 5.2. Block diagram of power network

To compensate effectively, APF design is an important criterion. In brief for perfect compensation, controller must be capable to achieve the following requirements: i) extract and inject load harmonic currents, ii) maintain a constant dc link voltage, iii) avoid absorbing or generating the reactive power with fundamental frequency components.

Herein, the active filter control algorithm is implemented to compensate both harmonics and reactive power absorbed by the contaminated load. Besides, to attain the compensation currents, filter behavior is analyzed. The power analysis can be done considering the multilevel inverter as a sinusoidal voltage source in parallel to contaminated load [156]. As a matter of fact, this voltage source cannot deliver the active power in the long

term; this issue has taken into account for control analysis. Fig. 5.3 shows the architecture for mathematical analysis.

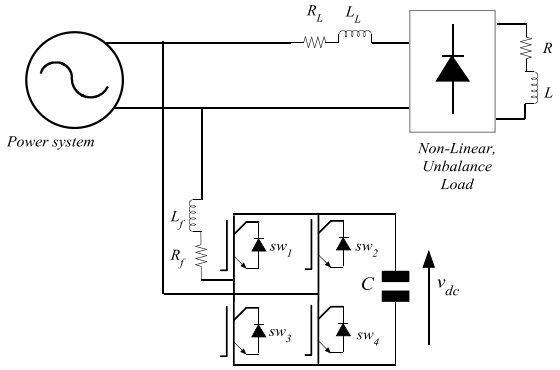


Fig. 5.3. Simplified system under steady state

The interaction between two voltage sources, interfaced by line impedance (under steady state), is governed by the geometrical relation. From Fig. 5.3 general expression of load current can be written as:

$$i_L(t) = \sum_{n=1}^{\infty} (I_{Lan} \times sin(n\omega t + \theta_{Lan})) \tag{5.1}$$

This load current is decomposed into three components specifically, active and reactive at fundamental frequency and the entire harmonic component. i.e.

$$i_L(t) = I_{La1} cos\theta_{La1} \times sin\,\omega t + I_{La1}\, sin\,\theta_{La1} \times cos\,\omega t + \sum_{n=2}^{\infty} (I_{Lan} \times sin(n\omega t + \theta_{Lan})) \tag{5.2}$$

$$i_L(t) = i_{La,actif}(t) + i_{La,reactif}(t) + \times i_{Lah}(t) \tag{5.3}$$

Compensation current that filter should produce is

$$i_c = (-i_{La,reacitve}(t) + i_{Lah}(t)) \tag{5.4}$$

Thus filter should achieve this compensation, through finite control actions. Extraction of compensation currents are demonstrated in next section.

5.3 Control Strategy

a) Harmonic current extraction

In the present paper i_d-i_q strategy is followed for perfect compensation [141]. This compensation strategy is demonstrated in Fig. 5.4. In this method reference currents are obtained through instantaneous active and reactive currents i_d and i_q of the nonlinear load. *dq* load current can be obtained from equation (5.5). Two stage transformations yields relation between the stationary and rotating reference frame. Fig.5.5 shows voltage and current vectors in stationary and rotating reference frames. The transformation angle θ is sensitive to all voltage harmonics and unbalanced voltages; as a result $d\theta/dt$ may not be constant. Arithmetical relations are given in equation 5.5 and 5.6; finally reference currents are obtained from equation (5.7). One of the major advantages of this approach is that, angle θ is calculated directly from main voltages.

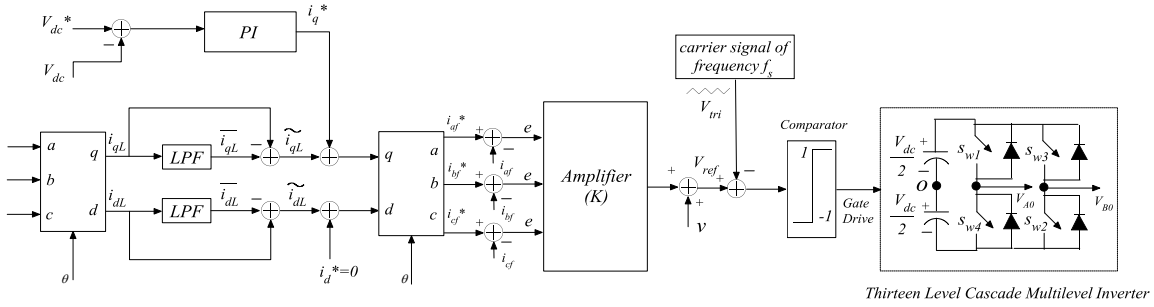


Fig. 5.4. Control block diagram for proposed APF

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \frac{1}{\sqrt{v_\alpha^{\,2} + v_\beta^{\,2}}} \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{5.5}$$

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} cos\theta & sin\theta \\ -sin\theta & cos\theta \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix}, \; \theta = tan^{-1}\left(v_\alpha / v_\beta \right) \tag{5.6}$$

$$\begin{bmatrix} ic_\alpha \\ ic_\beta \end{bmatrix} = \frac{1}{\sqrt{v_\alpha{}^2 + v_\beta{}^2}} \begin{bmatrix} v_\alpha & -v_\beta \\ v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} ic_d \\ ic_q \end{bmatrix} \tag{5.7}$$

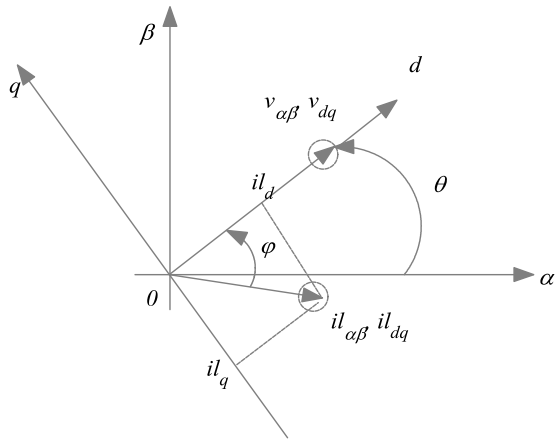


Fig.5.5. Voltage and current vectors in stationary and rotating reference frames

Thus enables the system to be frequency independent by avoiding the PLL in the control circuit, consequently synchronizing problems with unbalanced and distorted conditions of main voltages are also evaded. Thus $i_d - i_q$ achieves large frequency operating limit essentially by the cut-off frequency of voltage source inverter (VSI). From the control diagram of shunt active filter, load currents i_d and i_q are obtained from park transformation, then they are allowed to pass through the high pass filter to eliminate dc components in the nonlinear load currents. Filters used in circuit are Butterworth type, to reduce the influence of high pass filter. An alternative high pass filter (AHPF) can be used in the circuit, which can be obtained through the low pass filter (LPF) of same order and cut-off frequency. This can be achieved simply from the difference of the input signal and filtered one. Butterworth filter used in harmonic injecting circuit have cut-off frequency equal to one half of the main frequency ($f_c=f/2$), with this a small phase shift in harmonics and sufficiently high transient response can be obtained.

5.3.1 Harmonic current regulator

Reference currents obtained are synthesized and then sent to current regulator, which generates command signals to the compensator. Hysteresis control provides fast response and suitable for non-sinusoidal current tracking. It is obvious, by using hysteresis, variable switching pattern is achieved, which drastically varies the switching frequency and phase interaction in the system. To evade this phenomenon a voltage source pulse width modulation technique is utilized. These prospects achieve zero steady state error for dominant frequencies. A current regulator is adopted in the system to track the harmonic currents. This not only save computational time, but also simplified the structure. Fig.5.4 demonstrates the current control approach, which resolved the commanded current signal into commanded voltages and then synthesized to voltage source modulator. Further, commanded voltages expressed in PWM duty cycles by normalizing them to dc voltage and giving appropriate range.

5.3.2 Multilevel voltage source modulation

The basic ramp comparison current controller with two level topology given in [164, 165], is extended to proposed multilevel inverter. Here, the thirteen level voltage source modulations is accomplished by comparing the duty cycles with a set of carrier waveforms. Fig.5.6 demonstrates the switching function, V_{sin} so obtained is compared with triangular carrier V_{tri} of frequency f_s and with definite amplitude.

Switching function V_{sin} is modulated with carrier following the principle of unipolar PWM i.e.

Condition:1.1 $V_{sin} > V_{tri}$. Then SW1 is on and resultant voltage $V_{A0} = +Vdc/2$

Condition:1.2 $V_{sin} < V_{tri}$, Then SW2 is on and resultant voltage $V_{A0} = -Vdc/2$

In similar fashion for other phase leg of H-bridge,

Condition:2.1 $V_{sin} > V_{tri}$ Then SW3 is on and resultant voltage $V_{BO} = +Vdc/2$

Condition:2.2 $V_{sin} < V_{tri}$ Then SW2 is on and resultant voltage $V_{BO} = -Vdc/2$

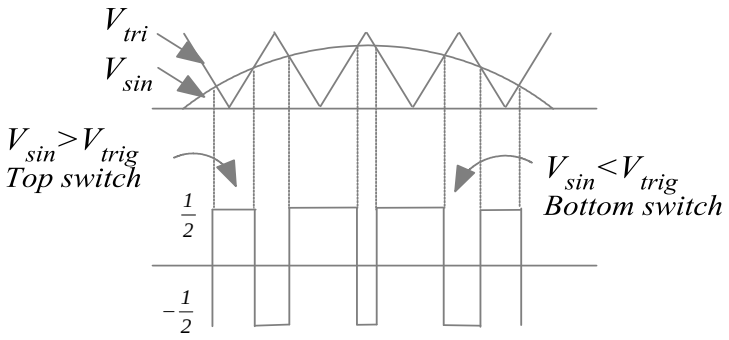


Fig.5.6 Unipolar modulation of one arm of H-Bridge of VSC

Therefore net voltage levels obtained for one H-Bridge is V_{dc}, *0,* $-V_{dc}$. The process is repeated for other H-bridges with a carrier phase shifted by the corresponding angles. Sum of all these three voltages results in producing net output voltage waveform. Unipolar switching scheme is considered for generating pulses. Phase shifted modulation (PSM) is carried out for proposed CMI based APF. As it is well known that phase shifted modulation have definite advantages over level shifted PWM like; no rotation in switching, easy to implement, device conduction period and device switching period are constant. These advantages facilitate reduction of switching losses. Consequently, switching scheme provides cost effective solution for converter.

5.3.3 DC voltage controller

The voltage regulator is incorporated on dc side and is performed by proportional – integral (PI) controller. Inputs to the PI controller are, difference between dc link voltage (V_{dc}) and reference voltage (V_{dc}*). To operate effectively, it is imperative to keep the DC capacitor voltage at a constant value, because capacitor voltage directly influences the real

power conversion. To maintain voltage constant, no real power should be transferred. But due to converter switching, small amount of real power is utilized. To operate APF successfully real power needs to be controlled; this is done by regulation of the first harmonic active current of positive sequence (i_d^+). Further, reactive power flow is controlled by the first harmonic reactive current of positive sequence i_q^+. On the other hand, considering that primary job of active power filters is just the elimination of the harmonics caused by non-linear loads, current i_q^+ is set to zero. In fact by controlling both active and reactive positive sequence currents, power flow can be controlled smoothly. To analyze controller performance a step response is presented in next section.

5.4 Simulation Result and System Performance

The proposed system is configured in Simulink. Powersim block is used to build inverters and diode bridge rectifiers. Further, real time experiments are carried out for evaluating the proposed APF. Studies are conducted on a three-phase bridge feeding a highly inductive load. Herein, performances are analyzed on the basis of observation thereby avoiding all-inclusive explanations. In fact, presented verifications are constructive for researchers and industries. Simulation has been conducted for balanced non-linear load under different main voltages (balanced sinusoidal, unbalanced sinusoidal) conditions.

Fig. 5.8 and Fig. 5.9 demonstrate the thirteen-level terminal and filter voltages when connected to power network. Fig.5.10 to Fig.5.13 illustrates APF performance while feeding a contaminating load under balanced supply voltages. Fig. 5.11 shows the performance of the system with and without APF. APF is initiated at 12 ms and it is taken out at 20 ms. The waveforms in the figure show source current, load current, compensation current and DC link voltage respectively from top to bottom order. Fig. 5.12 demonstrates the steady state

performance of the APF with filter. It is evident that system maintains sinusoidal current injected at the point of common coupling from source side. To highlight the dynamic performance, system is subjected to sudden change in load. Fig. 5.13 illustrates the dynamic performance. It is observed that APF performance is quite satisfactory under this circumstance. Observing the verifications, APF has confirmed the excellent performance. Overall APF responses are quite satisfactory in all the events. Additionally high quality current waveforms are achieved with the help of proposed configurations. Further, to validate the proposed approach the APF is verified with Real time digital simulator (OPAL-RT).

5.4.1 Proportional-Integral (PI) Controller Design Aspects

Due to inherent benefit of the proposed topology dc capacitor voltage control is quite simple. A single PI controller is involved in the structure. Change in dc link voltage (V_{dc}) and reference voltage (V_{dc}*), are retrieved together from network. Fig.5.7 represents step response of the capacitor voltage for different values of the PI controller integration coefficient *(k_i),* for a proportional efficient *(k_P)* at 0.75. It can be seen that as k_i increases, the overshoot increases while the rising times decreases. Increase in proportional term k_p increases noise, which in turn, degrades reference current extraction. Increase k_i may improve the reference current, but under damped oscillation are encountered. Also large transits in the capacitor voltages may develop which in turn, tends to trip the protection circuit. In simulation and in practice, k_p and k_i are both chosen as 0.75 and 1 respectively. Voltage ripple is independent of integrator coefficient and decreases as capacitance increases.

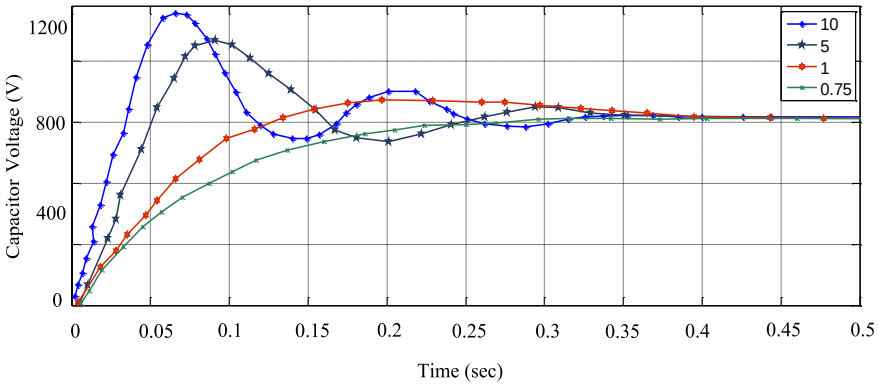


Fig. 5.7 Step response of capacitor voltage for different valued of K_P *at* K_I=0.75

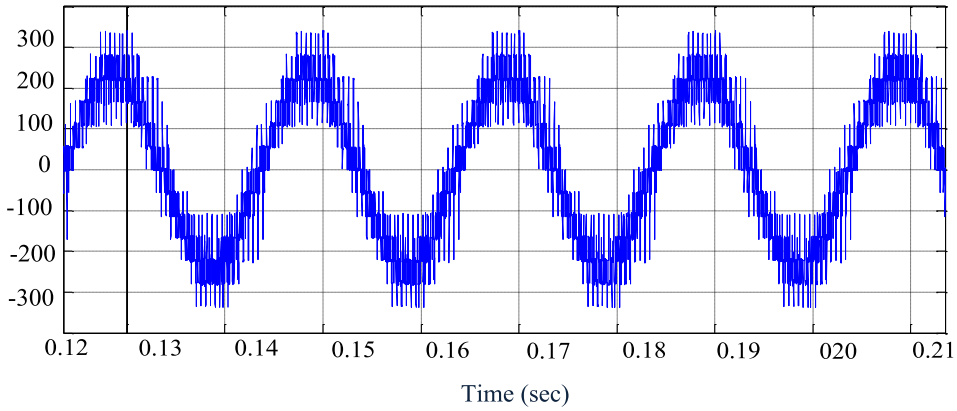


Fig. 5.8 Details of simulated thirteen-level output waveform

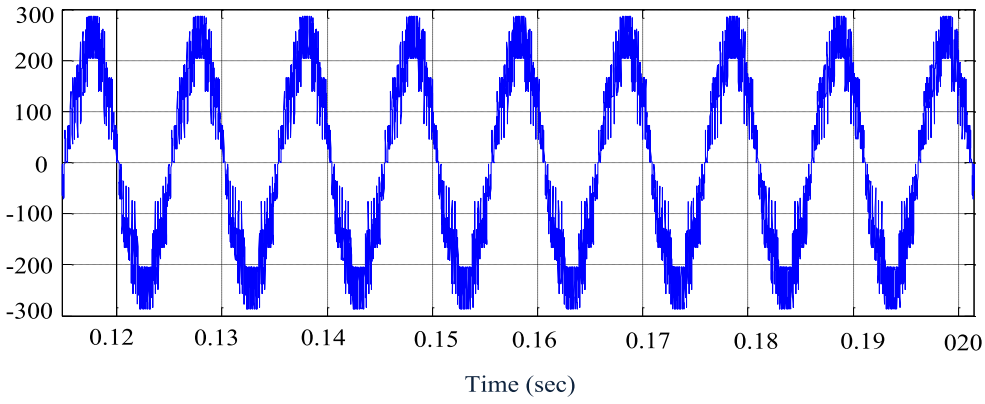


Fig. 5.9 Details of simulated thirteen-levels filter output waveform

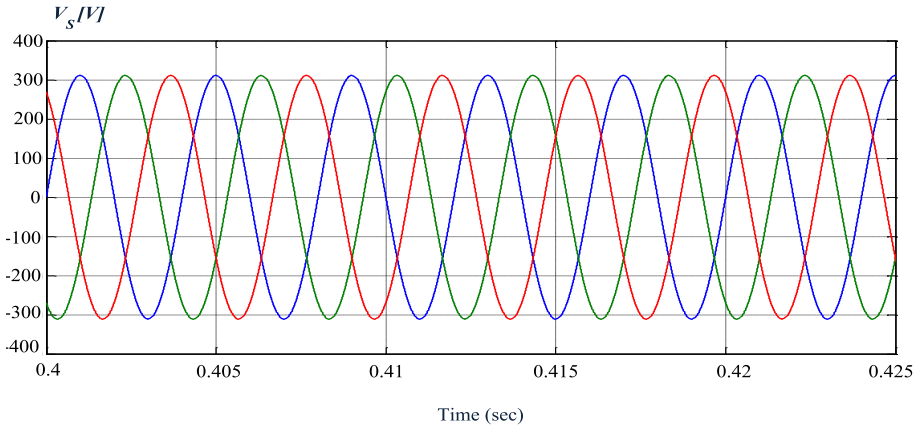


Fig. 5.10 Balanced supply voltages

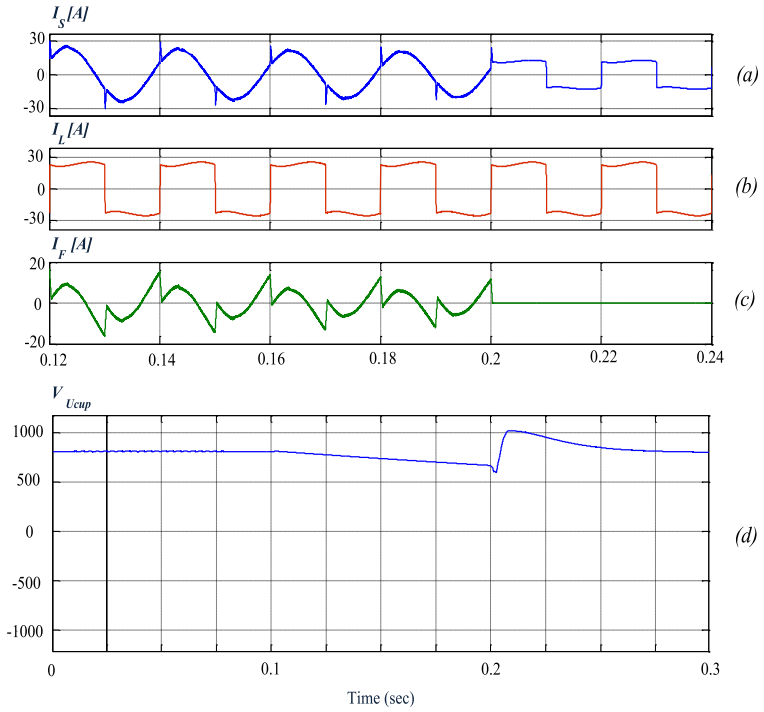


Fig. 5.11. Details of APF performance (with and without filter) (a) source current (b) load currents (c) filter current and (d) dc capacitor voltage, under balanced condition

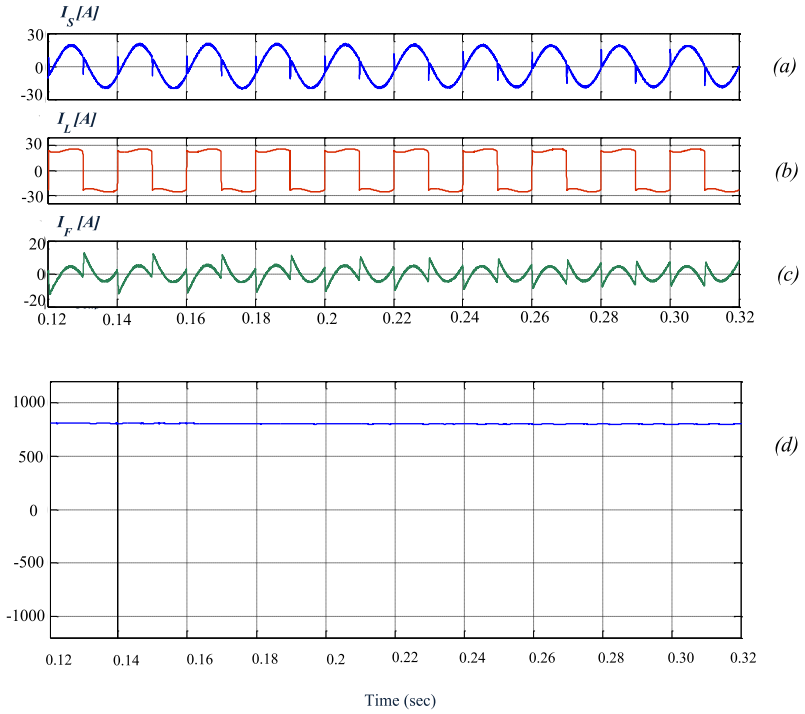


Fig. 5.12. Details of steady state performance (a) source current (b) load currents (c) filter current and (d) dc capacitor voltage, under balanced condition

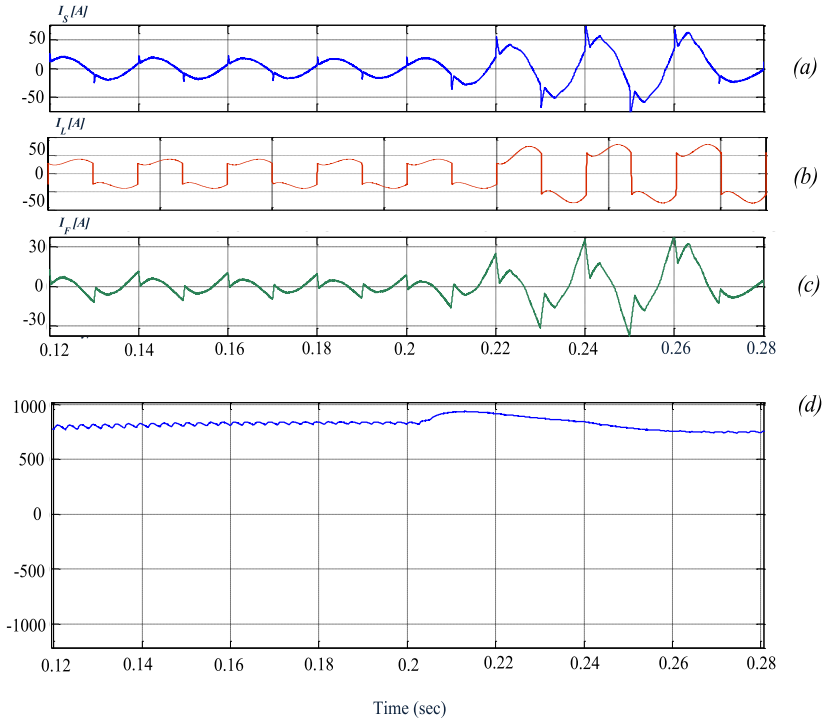


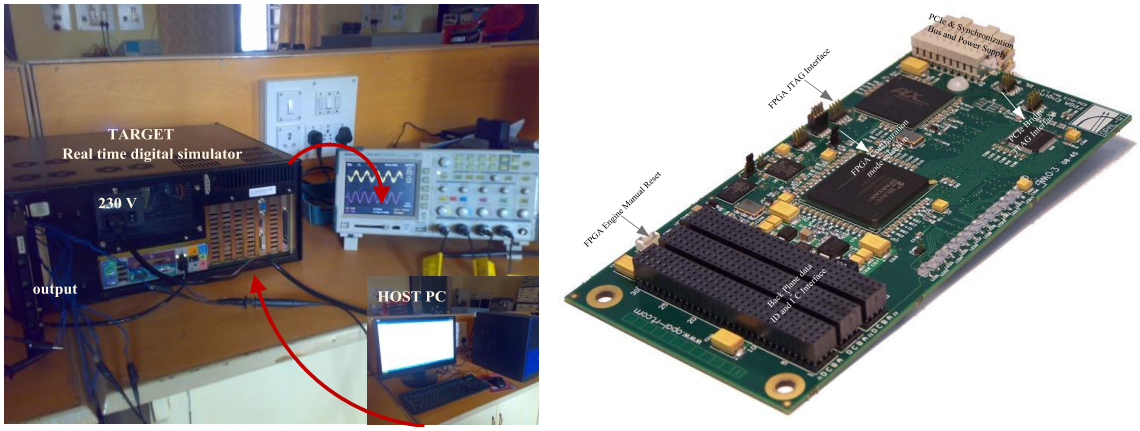
Fig. 5.13. Details of APF performance with step change in load (a) source current (b) load currents (c) filter current and (d) dc capacitor voltage, under balanced condition

5.5 Verifications with Real Time Digital Simulator

The Real Time Digital Simulator (OPAL-RT) allows developers to accurately and efficiently simulate electrical power systems and their ideas to improve them. The OPAL-RT Simulator [144-145] operates in real time, therefore not only allowing the simulation of the power system, but also making it possible to test physical protection and control equipment. This gives developers the means to prove their ideas, prototypes and final products in a realistic environment. The OPAL-RT is a fully digital power system simulator capable of continuous real time operation. It performs electromagnetic transient power system simulations with a typical time step of 50 microseconds utilizing a combination of custom software and hardware. The proprietary operating system used by the OPAL-RT guarantees "Hard real time" during all simulations. It is an ideal tool for the design, development and testing of power system protection and control schemes. With a large capacity for both digital and analog signal exchange (through numerous dedicated, high speed I/O ports) physical protection and control devices are connected to the simulator to interact with the simulated power system.

The real time digital simulation hardware used in the implementation of the OPAL-RT is modular, hence making it possible to size the processing power to the simulation tasks at hand. Fig.5.14 demonstrates typical hardware configurations. The OP5142 (Fig 5.14 .b) is one of the key building blocks in the modular OP5000 I/O system from Opal- RT Technologies. It allows the incorporation of FPGA technologies in RT-LAB simulation clusters for distributed execution of HDL functions and high-speed, high-density digital I/O in real-time models. Based on the highest density Xilinx Spartan-3 FPGAs, the OP5142 can be attached to the backplane of an I/O module of either a Wanda 3U- or Wanda 4U-based

Opal-RT simulation system. It communicates with the target PC via a PCI-Express ultra-low-latency real-time bus interface. As can be seen, the simulator can take on several forms including a new portable version which can easily be transported to a power-plant or substation for on-site pre-commissioning tests. Each rack of simulation hardware contains both processing and communication modules. The mathematical computations for individual power system components and for network equations are performed using one of two different processor modules.



(a) (b)

Fig.5.14 a) Details of OPAL-RT Hardware setup b) OP5142 layout and connectors

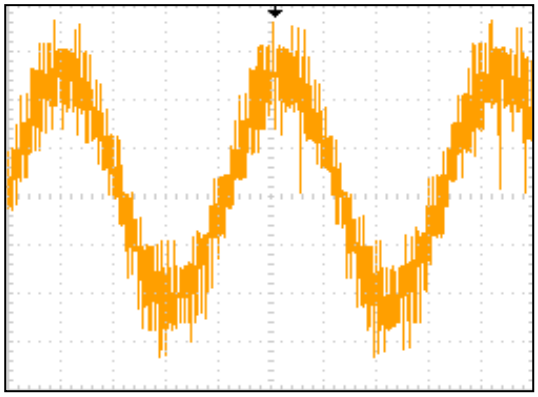


Fig. 5.15. Detials of output votlage of phase a . scale (100 V/div), Time scale: 5 ms/div

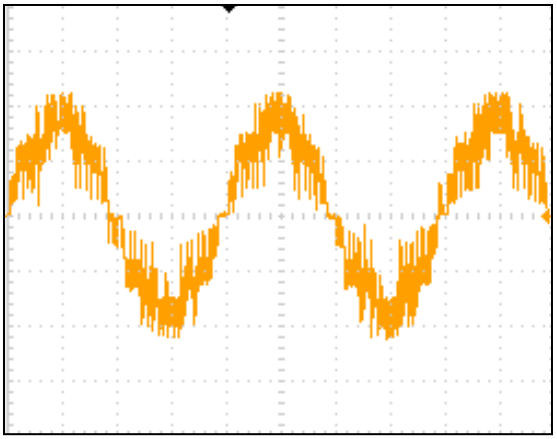


Fig.5.16. Details of thirteen level filter voltage of phase a. scale (100 V/div). Time scale: 5 ms/div

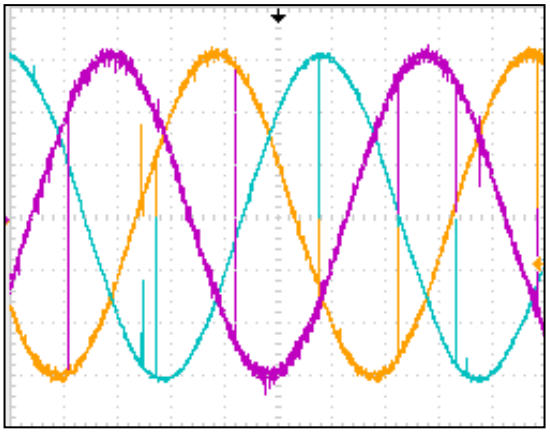


Fig.5.17. Detials of balanced supply votlages, scale (100 V/div), Time scale: 10 ms/div

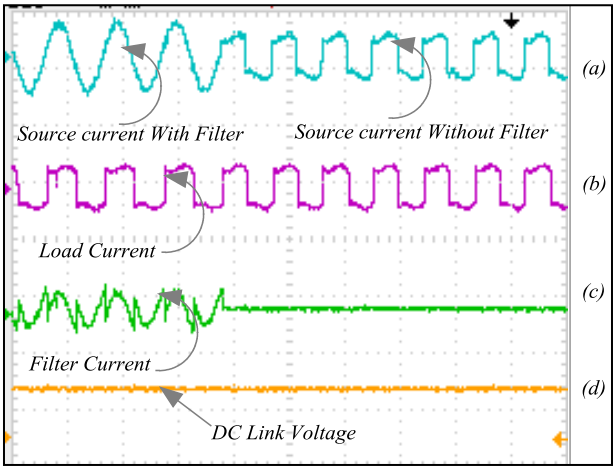


Fig. 5.18. Performance of a system (with and without APF) (a) Supply current (scale: 30 A/div). (b) Load current (scale: 30 A/div.). (c) Filter current (scale: 20 A/div.). (d) DC capacitor voltage (800 V) under balanced condition. Time scale: 20 ms/div

Fig. 5.15 and Fig. 5.16 highlights the Real-Time performance of the proposed APF for line to ground voltage and filter voltage, when connected to power network. It can be observed that simulation results (Figs. 5.8 & 5.9) are in close agreement with Real-Time experimental ones. The transformer ratios are scaled in *1:1* which results *in* yielding a *thirteen level* output voltages at the inverter terminals. The source voltage is 115 V and dc capacitor voltage reference at the APF is set to 800 V to achieve a nominal voltage at the inverter terminals under steady state. In the beginning, APF performance is evaluated under balanced event. Fig. 5.17 shows the details of the balanced supply voltages. Fig. 5.18 highlights the performance of power network, with and without APF operation. Fruitfully, APF provides necessary compensation.

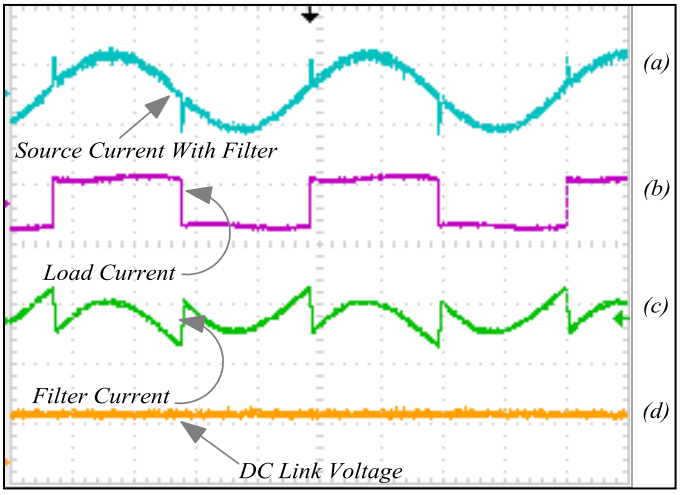


Fig. 5.19. Performance of a APF under study state conditons (a) Supply current (scale: 30 A/div). (b) Load current (scale: 30 A/div.). (c) Filter current (scale: 20 A/div.). (d) DC capacitor voltage (800 V). Time scale: 5 ms/div

Extending further, APF operation under steady state is shown in Fig.5.19. It is observed that, source current waveform has almost no harmonic content and is practically in phase with the source voltage. To analyze the dynamic performance of proposed APF, a step change is produced in nonlinear load. Fig. 5.20 shows this situation and APF behavior is

quite good. Details of harmonics with and without compensation are given in Fig. 5.21 and Fig.5.22. Presented FFT spectra figured out elimination of lower order harmonic components successfully. On the other hand, proposed APF has many inherent benefits like control scheme is very simple as only one storage element is involved. Further, three-phase transformers drastically reduce the size when compared to conventional one.

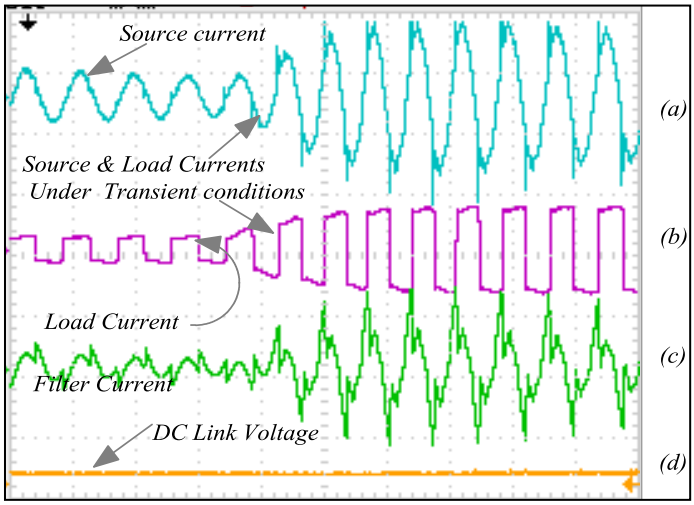


Fig. 5.20. Performance of a system (with and without APF) (a) Supply current (scale: 30 A/div). (b) Load current (scale: 30 A/div.). (c) Filter current (scale: 20 A/div.). (d) DC capacitor voltage (800 V) under balanced condition. Time scale: 25 ms/div

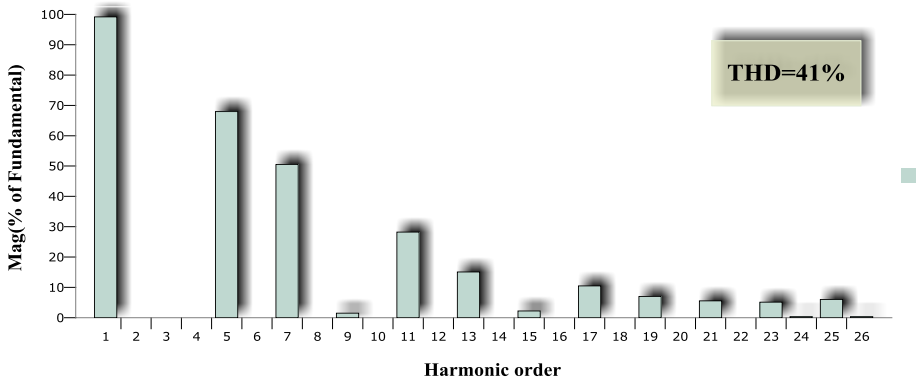


Fig. 5.21. Details of harmonic spectra of source current before compensation

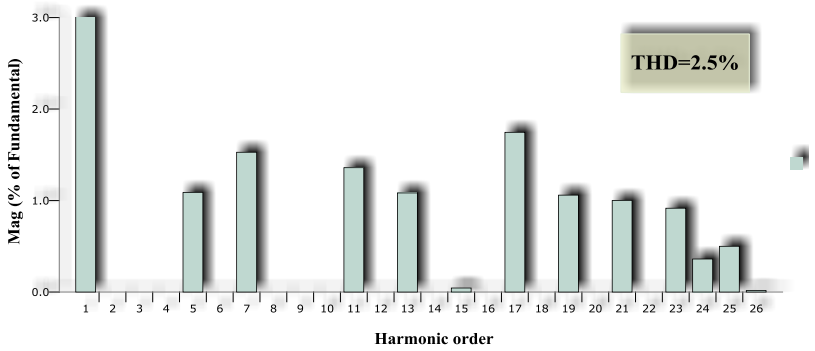


Fig. 5.22. Details of harmonic spectra of source current after compensation

5.6 Summary

This chapter has proposed a new cascaded multilevel based APF with single dc source and reduced number of transformers. Proposed APF has many advantages like; increasing utilization rate as only one dc source is used with isolated transformers. Again since less number of equipments are used, the size and weight will trim down. Low switching frequency ensures less transition loss, which reduces EMI problems. On the other hand, complexity in control dissection is drastically reduced because of single storage device. In fact this is an additional merit for this APF. i_d-i_q method is used for obtaining reference currents in the system. This approach has considerable merit as angle 'θ' is calculated directly from main voltages. This enables operation to be frequency independent and thus large numbers of synchronization difficulties are evaded. It is also observed that DC voltage regulation system valid to be a stable one and steady-state error free system was obtained. The proposed filter, compensating a contaminating load, was simulated and verified with prototype experiments. The Real time verifications are carried out for balanced, unbalanced and transient events. High quality voltage and current waveforms signifies the excellent performance of the proposed APF. The results also confirm improved transient performance of the APF over a range of load fluctuations and operating conditions.

Chapter 6

Conclusion

Summary

Future Work

6.1 Summary

In power electronics converters (PEC) with PWM of medium/high voltage/power and some specific applications and operating conditions, solutions (for example 3-phase VSI presented in chapter 1) are not attractive. In-addition, very high frequency of the switches in semiconductor devices of high voltage/power (need a compromise between output-voltage quality and regulation dynamics with application of an output filter), higher voltage stresses, and smaller *dv /dt* and EMI problems (without any special countermeasures), and for a moment an inadequate value of the peak voltage in semiconductor devices (for a peak voltage of 6 kV, the recommended voltage is about 3.5 kV) would be the main cause for development of *Multilevel Technology* in PECs in the year 1980s–1990s, in particular multilevel VSI. However, at present this technology is well renowned and gained their presence in numerous applications.

The main advantages of the present multilevel VSI are:

- ✓ Wide range of output-voltage amplitude amendments;
- ✓ Accuracy in modeling output voltage and current;
- ✓ Trouble-free adaptation to low-voltage energy storage;
- ✓ Reduction in voltage hazard and current elements (dependent on applied topology);
- ✓ Decreased level of common-mode disturbances.

In view of latter, multilevel inverters have matured from being an emerging technology to a well-established and attractive solution for medium-voltage high-power drives. As presented in this thesis, these converters have overcome the technical barriers that had been the curb for their deep use as an optimized solution in the power market. Modeling,

control strategies design, and modulation methods development have been broadly discussed in the thesis.

Renowned multilevel topologies such as NPC, FC, and CHB are addressed with principle of operation. Some of the interesting features in terms of power quality, power range, modularity, and other characteristics achieving high-quality output signals being specially designed for medium and high-power applications are completely presented. From the study it has been confirmed that CHB-MLI proved to be a reliable one, when compared with other two. Although this inverter topology has been established in the market of medium-voltage drives, there are some aspects that require further development and research. The first issue that needs attention is the efficiency improvement [69]. Second one is usage of separate dc source for each H-bridge cell.

Therefore, research on improving the performance of CHB-MLI becomes a key motivation for this thesis. An extensive survey has been done to resolve this problem. Later, most attractive and remarkable architectures of CMI with separate DC sources are verified. In-depth discussion is carried out among traditional CMIs. Finally demerits of traditional CMI based topologies are addressed. From traditional CMIs it has been known that although topologies are quite good in structure point of view, but they use large number of switching components to generate high number of voltage levels. Meanwhile, THD problems are also raised in traditional CMIs which are a major concern while designing the multilevel topologies.

To eliminate the problems associated with traditional CMIs, a new version of CMI is proposed. The proposed CMI is designed with single DC source by using three-phase transformers. The effectiveness and validity of the proposed version is demonstrated with

prototype experiments. Since less number of components are utilized, the proposed structure is reliable, efficient, cost-effective and compact. The attractive features of the proposed converters are: low switching frequency and reduce electromagnetic interference problems, increase utilization rate because of single dc source, removal of third harmonic component, as three-phase transformer are employed on secondary side. Consequently, these characteristics allow one to achieve high quality output voltages and input currents. Also it has an outstanding availability due to their intrinsic component redundancy. Due to these features, proposed architecture is superior over the conventional structures. The remarkable attributes of the proposed converter is well suitable for grid-connected photovoltaic/ wind-power generator, flexible alternating current systems.

To show the applications of the proposed version a new active power filter (APF) is designed. In contrast with conventional topologies, number of transformers is drastically reduced in the proposed structure resulting in reduction of installation area, cost and complexity of control system. Herein, APF is designed to work as voltage source and operates as harmonic isolator. Control strategy for detecting the current harmonics is based on i_d-i_q theory. DC link voltage control is analyzed together with effect of controller gain and delay time in the system's stability. The controller is able to perform all required tasks for correct operations of the APF. Comprehensive computer simulations are performed to verify the performance of the proposed filter and further it is validated with Real time digital simulator.

6.2 Future Work

1. In the proposed multilevel inverter expansion for 3-phase applications, total number of transformer in the circuit can be reduced by using of cascaded 3-phase transformer circuit

instead of single-phase transformer circuit. In the scheme, total number of switching components in the circuit is still a drawback to achieve lower cost and smaller size of the inverter compared with conventional multilevel inverter. This is a challenging issue and new modifications have to be carried out so as to reduce total switching components.

2. The proposed inverter has been operated by only three control schemes, namely Fundamental switching, SHEPWM and sinusoidal PWM. Applying the improved switching techniques can still improve the output quality. So potential of proposed version could be explored by adopting different switching techniques.
3. The proposed version of CMI is only adopted for active power filter applications. In fact the merits of CMI can be used to build for photovoltaic/grid connected systems. So it can extend to multiple applications like STATCOM, SSSC and UPQC etc.

References

1. Fazel SS, (2007) Investigation and comparison of multi-level converters for medium voltage applications. Ph.D. Thesis, Berlin Technical University.
2. Baker RH, (1980) High-voltage converter circuit. US Patent 4203151.
3. Meynard TA, Foch H, Forest F, Turpin C, Richardeau F, (2002) Multi-cell converters: derived topologies. IEEE Transact ions on Industrial Electronics, vol.49, no.5:978–987.
4. J.-S. Lai and F. Zheng Peng, "Multilevel converters-a new breed of power converters," IEEE Trans. Ind. Applicat. , vol. 32, no. 3, pp. 509–517, May 1985.
5. R. Teodorescu, F. Blaabjerg, J. K. Pedersen, E. Cengelci, S. Sulistijo, B. Woo, and P. Enjeti, B Multilevel converters a survey, in Proc. Eur. Power Electron. Conf., Lausanne, Switzerland, 1999.
6. L. M. Tolbert, F. Z. Peng, and T. G. Habetler, B Multilevel converters for large electric drives, IEEE Trans. Ind. Appl. , vol. 35,pp. 36–44, Jan./Feb. 1999.
7. J. Rodriguez, J.-S. Lai, and F. Z. Peng, B Multilevel inverters: A survey of topologies, controls, and applications, IEEE Trans. Ind. Electron., vol. 49, pp. 724–738, Aug. 2002.
8. J. Rodriguez, B. Wu, S. Bernet, J. Pontt, and S. Kouro, B, "Multilevel voltage source converter topologies for industrial medium voltage drives, IEEE Trans. Ind. Electron. (Special Section on High Power Drives ,vol. 54, pp. 2930–2945, Dec. 2007.
9. M. Marchesoni, "High-performance current control techniques for application to multilevel high-power voltage source inverters," IEEE Trans. Power Electron. , vol. 7, no. 1, pp. 189–204, Jan. 1992.

10. L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats,B The age of multilevel converters arrives, IEEE Ind. Electron. Mag. , pp. 28–39, Jun. 2008.
11. Meynard, T.A., and Foch, H.: 'Multi-level conversion: high voltage chopper and voltage-source inverter', IEEE-PESC Conf. Rec., 1992,pp. 397–403
12. J. K. Steinke, "Switching frequency optimal PWM control of a threelevel inverter," *IEEE Trans. Power Electron.*, vol. 7, no. 3, pp. 487–496, Jul. 1992.
13. Z. Pan, F.Z. Peng, K.A. Corzine, V.R. Stefanovic, J.M. Leuthen, and S. Gataric, "Voltage balancing control of diode-clamped multilevel rectifier/inverter systems," IEEE Trans. Ind. Applicat., vol. 41, no. 6, pp. 1698–1706, Nov. 2005.
14. B. Ozpineci, L.M. Tolbert, and J.N. Chiasson, "Harmonic optimization of multilevel converters using genetic algorithms," IEEE Power Electron. Lett., vol. 3, no. 3, pp. 92–95, Sept. 2005.
15. A. Nabae, I. Takahashi, and H. Akagi, "A neutral-point clamped PWM inverter," IEEE Trans. Ind. Applicat. , vol. 1A-17, no. 5, pp. 518–523, Sept. 1981.
16. B.P. McGrath, D.G. Holmes, and T. Meynard, "Reduced PWM harmonic distortion for multilevel inverters operating over a wide modulation range," IEEE Trans. Power Electron., vol. 21, no. 4, pp. 941–949, July 2006.
17. M. Marchesoni and P. Tenca, "Diode-clamped multilevel converters: A practicable way to balance dc-link voltages," IEEE Trans. Ind. Electron. , vol. 49, no. 4, pp. 752–765, Aug. 2002.

18. K.A. Corzine and X. Kou, “Capacitor voltage balancing in full binary combination schema flying capacitor multilevel inverters,” IEEE Power Electron. Lett., vol. 1, no. 1, pp. 2–5, Mar. 2003.
19. A. Bendre and G. Venkataramanan, “Neutral current ripple minimization in a three-level rectifier,” IEEE Trans. Ind. Applicat. , vol. 42, no. 2, pp. 582–590, Mar. 2006.
20. C. Rech and J.R. Pinheiro, “Hybrid multilevel converters: Unified analysis and design consider-ations,” IEEE Trans. Ind. Electron. , vol. 54, no. 2, pp. 1092–1104, Apr. 2007.
21. L. Yacoubi, K. Al-Haddad, L.-A. Dessaint, and F.Fnaiech, “Linear and nonlinear control techniques for a three-phase three-level NPC boost rectifier,” IEEE Trans. Ind. Electron., vol. 53, no. 6, pp. 1908–1918, Dec. 2006.
22. P. Lezana, C.A. Silva, J. Rodrguez, and M.A. Prez, “Zero-steady-state-error input-current controller for regenerative multilevel converters based on single-phase cells,” IEEE Trans. Ind. Electron. , vol. 54, no. 2, pp. 733–740, Apr. 2007.
23. T.A. Meynard and H. Foch, “Multi-level choppers for high voltage applications,” in Proc. European Conf. Power Electronics and Applications, 1992, pp. 45–50.
24. H. Akagi, “New trends in active filters for power conditioning,” IEEE Trans. Ind. Applicat., vol. 32, pp. 1312–1322, Nov./Dec. 1996.
25. H. Akagi, A. Nabae, and S. Atoh, “Control strategy of active power filters using multiple voltage-source PWM converters,” IEEE Trans. Ind. Applicat. , vol. 22, pp. 460–465, May/June 1986.
26. F. Z. Peng, H. Akagi, and A. Nabae, “A new approach to harmonic compensation in power systems — A combined system of shunt passive and series active filters,” IEEE Trans. Ind. Applicat. , vol. 26, pp.983–990, Nov./Dec. 1990.

27. L. Morán, J. Dixon & R. Wallace, "A Three-Phase Active Power Filter Operating with Fixed Switching Frequency for Reactive Power and Current Harmonic Compensation", IEEE Transactions on Industrial Electronics, Vol. 42, Nº 4, August 1995, pp 402-408.
28. S. Srianthumrong and H. Akagi, "A medium-voltage transformerless ac/dc power conversion system consisting o f a diode rectifier and a shunt hybrid filter," IEEE Trans. Ind. Appl. , vol. 39, no. 3, pp. 874–882, May/Jun. 2003.
29. H. Fujita, S. To minaga, and H. Akagi, "Analysis and design of a d c voltage-controlled static var compensator u sing quad-series voltage-source inverters," IEEE Trans. Ind. Appl., vol. 32, no. 4, pp. 970–978, Jul./Aug. 1996.
30. L. A. Morán, I. Pastorini, J. Dixon & R. Wallace, "Series Active Power Filter Compensates Current Harmonics and voltage Unbalance Simultaneously", IEE Proceedings on Generation, Transmisión and Distribution, Vol. 147, Nº 1.January 2000. pp. 31-36.
31. H. Akagi, H. Fujita, S. Yonetani, and Y. Kondo, "A 6.6-kV transformerless STATCOM b ased on a five-level diode clamped PWM converter: System design and experimentation o f a 200-V, 10-kVA laboratory model," IEEE Trans. Ind. Appl. , vol. 44, no. 2, pp. 672–680, Mar. 2008.
32. Micah Ortúzar, Rodrigo Carmi, Juan Dixon and Luis Morán, "Voltage-Source Active Power Filter, Based on Multi-Level Converter and Ultracapacitor DC Link", IEEE Transactions on Industrial Electronics, Vol. 53, Nº 2, April 2006, pp. 477- 485.
33. H. Rudnick, J. Dixon and Luis Morán, "Delivering Pure and Clean Power", IEEE Power & Energy Magazine, Vol. 1, Nº 5, September/October 2003, pp32-40.

34. Ogasawara, S., and Akagi, H.: 'Analysis of variation of neutral point potential in neutral-point-clamped voltage source PWM inverters'. Conf. Rec. IEEE-IAS Annual Meeting, Toronto, Canada, 1993, pp. 965–970.
35. ÇolakI, Kabalci E. The control methods of multi-level inverter. TUBAV Sci 2009;1:45–54.
36. Jouanne, A.V., Dai, S., and Zhang, H.: 'A multilevel inverter approach providing DC-link balancing, ride-through enhancement,and common-mode voltage elimination', IEEE Trans. Ind. Electron., 2002, 49, pp. 739–745
37. W. McMurray, "Fast response stepped-wave switching power converter circuit," U.S. Patent 3 581 212, May 25, 1971.
38. J. A. Dickerson and G. H. Ottaway, "Transformerless power supply with line to load isolation," U.S. Patent 3 596 369, Aug. 3, 1971.
39. P. M. Bhagwat and V. R. Stefanovic, "Generalized structure of a multilevel PWM inverter," IEEE Trans. Ind. Applicat., vol. 19, no 6, pp. 1057-1069, Nov./Dec. 1983.
40. R. H. Baker, "Bridge converter circuit," U.S. Patent 4 270 163, May 26, 1981.
41. Celanovic, N., and Boroyevich, D.: 'A comprehensive study of neutralpoint voltage balancing problem in three-lever neutral-point clamped voltage source PWM inverters', IEEE Trans. Power Electron., 2000, 15, pp. 242–249.
42. Lee, Y.H., Kim, R.Y., and Hyum, D.S.: 'A novel SVPWM strategy considering dc-link balancing for a multi-level voltage source inverter'. Proc. IEEE APEC, Dallas, USA, 1999, pp. 509–514.

43. M. Marchesoni, M. Mazzucchelli, and S. Tenconi, “A non conventional power converter for plasma stabilization,” in Proc. IEEE 19th Power Electron. Spec. Conf., Apr. 11–14, 1988, pp. 122–129.\
44. P. W. Hammond, “A new approach to enhance power quality for medium voltage drives,” in Proc. Ind. Appl. Soc. 42nd Annu. Petroleum Chem. Ind. Conf., Sep. 11–13, 1995, pp. 231–235.
45. Ryszard Strzelecki, Grzegorz Benysek, “Power electronics in smart electrical energy networks,” Springer-ISBN 978-1-84800-317-0, 2008.
46. F. Z. Peng, “A generalized multilevel i nverter topology with self voltage balancing,” IEEE Trans. Ind. Applicat ., vol. 37, March/April 2001, pp. 611–618,.
47. K. Corzine and Y. Familiant, “A new cascaded multilevel H-bridge drive,” IEEE Trans. Power Electron. , vol. 17, no. 1, pp. 125–131, Jan. 2002.
48. B. P. McGrath and D. G. Holmes, “Natural capacitor voltage balancing for a flying capacitor converter induction motor drive,” IEEE Trans. Power Electron. , vol. 24, no. 6, pp. 1554–1561, Jun. 2009.
49. M. Hagiwara, K. Nishimura, and H. Akagi, “A medium-voltage motor drive with a modular multilevel PWM inverter,” IEEE Trans. Power Electron, vol. 25, no. 7, pp. 1786–1799, Jul. 2010.
50. J. Wang and F. Z. Peng, “Unified power flow controller using the cascade multilevel inverter,” IEEE Trans. Power Electron, vol. 19, no. 4, pp. 1077–1084, Jul. 2004.
51. Q. Song and W. Liu, “Control of a cascade STATCOM with star con-figuration under unbalanced conditions,” IEEE Trans. Power Electron. ,vol. 24, no. 1, pp. 45–58, Jan. 2009.

52. J. Zaragoza, J. Pou, S. Ceballos, E. Robles, C. Jaen, and M. Corbalan, "Voltage-balance compensator for a carrier-based modulation in the neutral-point-clamped converter," IEEE Trans.lnd. Electron., vol. 56, pp. 305–314, Feb. 2009.

53. H. Okayama, R. Uchida, M. Koyama, S. Mizoguchi, S. Tamai, H. Ogawa, T. Fujii, Y. Shimomura, "Large capacity high performance 3-level GTO inverter system for steel main rolling mill drives," in Conf. Rec. IAS Annu. Meeting , 1996, pp. 174–179.

54. S. Bernert, "Recent developments of high power converters for industry and traction applications," IEEE Trans. Power Electron. , vol. 15, no. 6, pp. 1102–1117, Nov. 2000.

55. S. Alepuz, S. Busquets-Monge, J. Bordonau, J. Gago, D. Gonzalez, and J. Balcells, "Interfacing renewable energy sources to the utility grid us-ing a three-level inverter," IEEE Trans. Ind. Electron., vol. 53, no. 5,pp. 1504–1511, Oct. 2006.

56. Y. Cheng, C. Qian, M. L. Crow, S. Pekarek, and S. Atcitty, "A comparison of diode-clamped and cascaded multilevel converters for a STATCOM with energy storage," IEEE Trans. Ind. Electron. , vol. 53, no. 5, pp. 1512–1521, Oct. 2006.

57. P. K. Steimer, H. E. Gruning, J. Werninger , E. Carroll, S. Klaka, S. Linder "IGCT—A new emerging technology for high power, low cost inverters," IEEE Ind. Appl. Mag. , vol. 5, no. 4, pp. 12–18, Jul./Aug. 1999.

58. H. Brunner, M. Hieholzer, T. Laska, A. Porst, "Progress in development of the 3.5 kV high voltage IGBT/diode chipset and 1200 A module applications," in Proc. IEEE Int. Symp. Power Semicond. Devices IC's, 1997, pp. 225–228.

59. B. Wu, High-Power Converters and AC Drives. New York: Wiley-IEEE Press, Mar. 2006.

60. N. S. Choi, J. G. Cho and G.H. Cho, "A general circuit topology of multilevel inverter," in Proc. IEEE-PESC, 1991, pp. 96-103.

61. Hirofurni Akagi, Shigenori Inoue, Tsurugi Yoshii,‖ Control and performance of a transfomerless Cascade PWM STATCOM with star configuration,‖ *IEEE Trans. Ind. Application*, Vol. 43 No. 4, July/Aug 2007.

62. Surin Khomfoi and Leon M. Tolbert, "Chapter 17 Multilevel power converter" Power electronic Handbook, Elsevier Publications.

63. F. Z. Peng and J. S. Lai, "Multilevel cascade voltage-source inverter with separate DC sources," U.S. Patent 5 642 275 , June 24, 1997.

64. D. Krug, S. Bernet, S. S. Fazel, K. Jalili, and M. Malinowski, "Comparison of 2.3-kv medium-voltage multilevel converters for industrial medium-voltage drives," IEEE Trans. Ind. Electron. , vol. 54, no. 6,pp. 2979–2992, Dec. 2007.

65. S. S. Fazel, S. Bernet, D. Krug, and K. Jalili, "Design and comparison of 4-kv neutral-point-clamped, flying-capacitor, and series-connected H-bridge multilevel converters," IEEE Trans. Ind. Appl., vol. 43, no. 4,pp. 1032–1040, Jul./Aug. 2007.

66. Meynard, T.A., and Foch, H.: 'Multi-level conversion: high voltage chopper and voltage-source inverter', IEEE-PESC Conf. Rec., 1992,pp. 397–403.

67. M. Marchesoni and P. Tenca, "Theoretical and practical limits in multi-level mpc inverters with passive front ends," in Proc. EPE, Graz, Austria,Aug. 2001.

68. J. Pou, R. Pindado, and D. Boroyevich, "Voltage-balance limits in four-level diode-clamped converters with passive front ends," IEEE Trans.Ind. Electron. , vol. 52, no. 1, pp. 190–196, Feb. 2005.

69. S. Busquets-Monge, S. Alepuz, J. Bordonau, and J. Peracaula, “Voltage balancing control of diode-clamped multilevel converters with passive front-ends,” IEEE Trans. Power Electron. , vol. 23, no. 4, pp. 1751–1758, Jul. 2008.

70. J. Wen and K. M. Smedley, “Synthesis of multilevel converters based on single- and/or three-phase converter building blocks,” IEEE Trans. Power Electron. , vol. 23, no. 3, pp. 1247–1256, May 2008.

71. P. Lezana and G. Ortiz, “Extended operation of cascade multicell converters under fault condition,”IEEE Trans. Ind. Electron. , vol. 56, no. 7, pp. 2697–2703, Jul. 2009.

72. S. Sirisukprasert, J. S. Lai and T. H. Liu, “A novel cascaded multilevel converter drive system with minimum number of separated DC sources,” in Proc. IEEE-APEC, 2001, pp. 1346–1350.

73. M. Glinka, “Prototype of multiphase modular-multilevel-converter with 2 MW power rating and 17-level-output-voltage,” in Proc. IEEE 35th PESC, 2004, vol. 4, pp. 2572–2576

74. L. Zhou, Q. Fu, X. Li, and C. Liu, “A novel multilevel power quality compensator for electrified railway,” in Proc. IEEE 6th IPEMC, May 2009, pp. 1141–1147.

75. A. Dell’Aquila, M. Liserre, V. G. Monopoli, and C. Cecati, “Designof a back-to-back multilevel induction motor drive for traction systems,”in Proc. IEEE 34th Power Electron. Spec. Conf. , Jun. 2003, vol. 4,pp. 1764–1769.

76. Z. Du, B. Ozpineci, L. M. Tolbert, and J. N. Chiasson, “DC–AC cascaded h-bridge multilevel boost inverter with no inductors for electric/hybridelectric vehicle applications,” IEEE Trans. Ind. Appl. , vol. 45, no. 3,pp. 963–970, May 2009.

77. J. R. Rodriguez, J. Pontt, M. Perez, P. Lezana, and P. W. Hammond, “High power synchronous machine fed by a cascaded regenerative inverter,” in Conf. Rec. IEEE IAS Annu. Meeting, Oct. 2008, pp. 1–7.

78. C.-C. Hua, C.-W. Wu, and C.-W. Chuang, “A digital predictive current control with improved sampled inductor current for cascaded inverters,” IEEE Trans. Ind. Electron. , vol. 56, no. 5, pp. 1718–1726, May 2009.

79. J. A. Barrena, L. Marroyo, M. A. R. Vidal, and J. R. T. Apraiz, “Individual voltage balancing strategy for PWM cascaded H-bridge converter-based STATCOM,” IEEE Trans. Ind. Electron. , vol. 55, no. 1, pp. 21–29,Jan. 2008.

80. Y. Liu, A. Q. Huang, W. Song, S. Bhattacharya, and G. Tan, “Small-signal model-based control strategy for balancing individual DC capacitor voltages in cascade multilevel inverter-based STATCOM,” IEEE Trans. Ind. Electron. , vol. 56, no. 6, pp. 2259–2269, Jun. 2009.

81. P. Flores, J. Dixon, M. Ortuzar, R. Carmi, P. Barriuso, and L. Moran, “Static Var compensator and active power filter with power injection capability, using 27-level inverters and photovoltaic cells,” IEEE Trans. Ind. Electron. , vol. 56, no. 1, pp. 130–138, Jan. 2009.

82. Z. Wu, Y. Zou, and K. Ding, “Analysis of output voltage spectra in a hybrid diode-clamp cascade 13-level inverter,” in Proc. IEEE 36th PESC, Jun. 2005, pp. 873–879.

83. D. Kai, Z. Yunping, L. Lei, W. Zhichao, J. Hongyuan, andZ. Xudong, “Novel hybrid cascade asymmetric inverter based on 5-level asymmetric inverter,” in Proc. IEEE 36th Power Electron. Spec. Conf., Jun. 2005, pp. 2302–2306.

84. Z. Du, B. Ozpineci, and L. M. Tolbert, “Modulation extension control of hybrid cascaded H-bridge multilevel converters with 7-level fundamental frequency switching scheme,” in Proc. IEEE Power Electron. Spec. Conf. , Jun. 2007, pp. 2361–2366.

85. J. I. Leon, S. Vazquez, S. Kouro, L. G. Franquelo, J. M. Carrasco, and J. Rodriguez, “Unidimensional modulation technique for cascaded multilevel converters,” IEEE Trans. Ind. Electron. , vol. 56, no. 8,pp. 2981–2986, Aug. 2009.

86. J. Rodriguez, S. Kouro, J. Rebolledo, and J. Pontt, “A reduced switchingfrequency modulation algorithm for high power multilevel inverters,” inProc. IEEE 36th Power Electron. Spec. Conf., Jun. 2005, pp. 867–872.

87. Z. Du, L. M. Tolbert, and J. N. Chiasson, “Active harmonic elimination for multilevel converters,” IEEE Trans. Power Electron. , vol. 21, no. 2, pp. 459–469, Mar. 2006.

88. Z. Du, L. M. Tolbert, J. N. Chiasson, and B. Ozpineci, “Reduced switching-frequency active harmonic elimination for multilevel converters,” IEEE Trans. Ind. Electron. , vol. 55, no. 4, pp. 1761–1770, Apr. 2008.

89. M. Perez, S. Kouro, J. Rodriguez, and B. Wu, “Modified staircase modulation with low input current distortion for multicell converters,” in Proc. IEEE Power Electron. Spec. Conf. , Jun. 2008, pp. 1989–1994.

90. M. G. Hosseini Aghdam, S. H. Fathi, and G. B. Gharehpetian, “Elimination of harmonics in a multi-level inverter with unequal DC sources using the homotopy algorithm,” in Proc. IEEE ISIE , Jun. 2007, pp. 578–583.

91. V. G. Agelidis, A. I. Balouktsis, and M. S. A. Dahidah, “A five-level symmetrically defined selective harmonic elimination PWM strategy: Analysis and experimental validation,” IEEE Trans. Power Electron. , vol. 23, no. 1, pp. 19–26, Jan. 2008.

92. O. Lopez, J. Alvarez, J. Doval-Gandoy, and F. D. Freijedo, "Multilevel multiphase space vector PWM algorithm," IEEE Trans. Ind. Electron., vol. 55, no. 5, pp. 1933–1942, May 2008.

93. Ebrahim Babaei , Seyed Hossein Hosseini, ―New cascaded multilevel inverter topology with minimum number of switches‖ *Elsevier Energy Conversion and Management* Vol.50 July 2009 pp 2761–2767.

94. A. K. Gupta and A. M. Khambadkone, "A space vector modulation scheme to reduce common mode voltage for cascaded multilevel inverters," IEEE Trans. Power Electron., vol. 22, no. 5, pp. 1672–1681, Sep. 2007.

95. A. K. Gupta and A. M. Khambadkone, "A general space vector PWM algorithm for multilevel inverters, including operation in over modulation range," IEEE Trans. Power Electron. , vol. 22, no. 2, pp. 517–526, Mar. 2007.

96. Z. Cheng and B. Wu, "A novel switching sequence design for five-level NPC/H-bridge inverters with improved output voltage spectrum and minimized device switching frequency," IEEE Trans. Power Electron. , vol. 22, no. 6, pp. 2138–2145, Nov. 2007.

97. V. Oleschuk, F. Profumo, A. Tenconi, R. Bojoi, and A. M. Stankovic, "Cascaded three-level inverters with synchronized space-vector modulation," in Conf. Rec. 41st IEEE IAS Annu. Meeting, Oct. 2006, vol. 2, pp. 595–602.

98. J. I. Leon, S. Vazquez, A. J. Watson, L. G. Franquelo, P. W. Wheeler, and J. M. Carrasco, "Feed-forward space vector modulation for single-phase multilevel cascaded converters with any DC voltage ratio," IEEE Trans. Ind. Electron. , vol. 56, no. 2, pp. 315–325, Feb. 2009.

99. M. Angulo, P. Lezana, S. Kouro, J. Rodriguez, and B. Wu, “Level-shifted PWM for cascaded multilevel inverters with even power distribution,” in Proc. IEEE Power Electron. Spec. Conf., Jun. 2007, pp. 2373–2378.

100. R. Inzunza and H. Akagi, “Design and performance of a transformerless shunt hybrid active filter for installation on a 6.6-kV power distribution system,” IEEE Trans. Power Electron., vol. 20,no. 4, pp. 893–900, Jul. 2005.

101. R. Gupta, A. Ghosh, and A. Joshi, “Switching characterization of cascaded multilevel-inverter-controlled systems,” IEEE Trans. Ind. Electron. , vol. 55, no. 3, pp. 1047–1058, Mar. 2008.

102. Y.-M. Park, H.-S. Yoo, H.-W. Lee, M.-G. Jung, S.-H. Lee, C.-D. Lee, S.-B. Lee, and J.-Y. Yoo, “A simple and reliable PWM synchronization and phase-shift method for cascaded H-bridge multilevel inverters based on a standard serial communication protocol,” in Conf. Rec. 41st IEEE IAS Annu. Meeting , Oct. 2006, vol. 2, pp. 988–994.

103. M. A. Perez, P. Cortes, and J. Rodriguez, “Predictive control algorithm technique for multilevel asymmetric cascaded H-bridge inverters,” IEEE Trans. Ind. Electron., vol. 55, no. 12, pp. 4354–4361, Dec. 2008.

104. P. Zanchetta, D. B. Gerry, V. G. Monopoli, J. C. Clare, and P. W. Wheeler, “Predictive current control for multilevel active rectifiers with reduced switching frequency,” IEEE Trans. Ind. Electron. , vol. 55, no. 1, pp. 163– 172, Jan. 2008.

105. Mariusz Malinowski, K. Gopakumar, Jose Rodriguez and Marcelo A. Perez “A Survey on Cascade Multilevel inverters”, IEEE Trans. Ind. Electron. , vol. 57, no. 7, July 2010.

106. G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto,B, "A new multilevel PWM method: A theoretical analysis",IEEE Trans. Power Electron. , vol. 7, pp. 497–505, Jul. 1992.

107. M. D. Manjrekar, P. K. Steimer, and T. A. Lipo, "Hybrid multilevel power conversion system: a competitive solution for high-power applications," IEEE Trans. Ind. Applicat., vol. 36, pp. 834–841, May/June 2000.

108. R.H. Baker, Electric Power Converter, U.S. Patent (1975) Number 3, 86,643.

109. Jose Rodriguez, Leopoldo G. Franquelo, Samir Kouro, Jose I. Leon, Ramon C. Portillo Ma Angeles Martin Prats, Marcelo A. Perez "Multilevel converters: an enabling technology for high-power applications", Proceedings of the IEEE Vol.97, No.11, November 2009.

110. H. Kuhn, N. E. Rüger, A. Mertens, "Control Strategy for Multilevel Inverter with Non-ideal DC Sources" IEEE Power Electronics Specialists Conference, PESC, pp. 632 – 638. 2007.

111. Shuai Lu; Mariéthoz, S.; Corzine, K.A. "Asymmetrical Cascade Multilevel Converters With Noninteger or Dynamically Changing DC Voltage Ratios: Concepts and Modulation Techniques ," IEEE Trans. Ind. Electronics, vol. 57, no. 7, July 2010.

112. Siriroj Sirisukprasert," The Modeling and Control of a Cascaded-Multilevel Converter-Based STATCOM " Dissertation submitted to the faculty of the Virginia Polytechnic Institute and State University (2004).

113. Z. Cheng and B. Wu, "A novel switching sequence design for five-level NPC/H-bridge inverters with improved output voltage spectrum and minimized device switching frequency," IEEE Trans. Power Electron., vol. 22, no. 6, november 2007.

114. Farid Khoucha, Soumia Mouna Lagoun, Khoudir Marouani, Abdelaziz Kheloui, and Mohamed El Hachemi Benbouzid, "Hybrid Cascaded H-Bridge Multilevel-Inverter Induction-Motor-Drive Direct Torque Control for Automotive Applications," IEEE Trans. Ind. Electronics, vol. 57, no. 3, march 2010.
115. M. Fracchia, T. Ghiara, M. Marchesoni, and M. Mazzucchelli, "Optimized modulation techniques for the generalized N-level converter," in Proc. IEEE Power Electronics Specialist Conference, Madrid, Spain, 1992, pp. 1205–1213.
116. S. Khomfoi, L. M. Tolbert, "Multilevel Power Converters," Power Electronics Handbook, 2nd Edition Elsevier, 2007, ISBN 978-0-12- 088479-7, Chapter17, 451-482.
117. J. A. Barrena, L. Marroyo, M. A. R. Vidal, and J. R. T. Apraiz, "Individual voltage balancing strategy for PWM cascaded H-bridge converter based STATCOM," IEEE Trans. Ind. Electron. vol. 55, no. 1, January 2008.
118. Shoji Fukuda, Takatsugu Yoshida, and Shigeta Ueda "Control Strategies of a Hybrid Multilevel Converter for Expanding Adjustable Output Voltage Range ," IEEE Trans. Ind. Applicat., vol. 45, no. 2, March/April 2009.
119. Nami, A.; Zare, F.; Ghosh, A.; Blaabjerg, F; "A Hybrid Cascade Converter Topology With Series-Connected Symmetrical and Asymmetrical Diode-Clamped H-Bridge Cells ," IEEE Trans. Power Electronics, vol. 26, no. 1, January 2011.
120. Domingo A. Ruiz-Caballero, Reynaldo M. Ramos-Astudillo, Samir Ahmad Mussa, , and Marcelo Lobo Heldwein, "Symmetrical Hybrid Multilevel DC–AC Converters With Reduced Number of Insulated DC Supplies," IEEE Trans. Ind. Electronics, vol. 57, no. 7, July 2010.

121. Rajesh Gupta, Arindam Gosh,“ Contorl of cascaded transformer multilevel inverter based D-STATCOM,” Elsevier, Electric power system research”,vol. 77, pp. 989-999, 2007.

122. C. Wang, “Research on the topology, PWM algorithm and balance control of neutral point voltage in multilevel converters,” Ph.D. dissertation, Tsinghua Univ., Beijing, China, 2008.

123. Tao Yu, Chaejoo Moon, Sungjun Park, SungGeun Song, Joungmin Lim, “A Study on Novel PWM HBML Inverter Using Common-arm,” in IEEE International Conference on Industrial Technology (ICIT 2006)

124. Feel-soon kang, Sung-jun Park, Man Hyung Lee, Cheul-U Kim, “An Efficient Multilevel-synthesis approach and its application to a 27-level inverter,” ,” IEEE Trans. Ind. Electronics, vol. 52, no. 6, Dec 2005.

125. Brendan Pete McGrath, Donald Grahame Holmes, “Multicarrier PWM Strategies for Multilevel Inverters,” IEEE Trans. Ind. Electronics, vol. 49, no. 4, Aug 2002.

126. Tao Yu, Chaejoo Moon, Sungjun Park, SungGeun Song, Joungmin Lim, “A Study on Novel PWM HBML Inverter Using Common-arm,” in IEEE International Conference on Industrial Technology (ICIT 2006)

127. Damoun Ahmadi, KeZou, Cong ,Yi Huang, and Jin Wang , “ Universal Selective Harmonic Elimination for High Power Inverters,” ,” IEEE Trans. Power. Electronics, vol. 26, no. 10, Dec 2011.

128. G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Scuitto, “A new multilevel PWM method: A theoretical analysis,” IEEE Trans. Power Electron., vol. 7, no. 3, pp. 495–505, Jul. 1992.

129. R. Schottler and R.G. Coney, “Commercial application experiences with SMES,” Power Eng. J., June 1999.

130. D. Chapman, “The cost of poor power quality,” Copper Development Assoc., March 2001.

131. G.W. Massey, “Estimation method for power system harmonic effect on power distribution transformer,” IEEE Trans. Ind. Applicat., vol. 30, no. 2, pp. 485–489, 1994.

132. W. Neves, H.W. Dommel, and W. Xu, “Practical distribution transformer models for harmonic studies,” IEEE Trans. Power Delivery, vol. 10, no. 2, pp. 906–912, 1995.

133. M.T. Bishop, J.F. Baranwski, D. Heath, and S.J. Benna, “Evaluating harmonic-induced transformer heating,” IEEE Trans. Power Delivery, vol. 11, no. 1, pp. 305–311, 1996.

134. B. Singh, K. Al-Haddad, and A. Chandra, “A review of active filters for power quality improvement,” *IEEE Trans. Ind. Electron.,* vol. 46, no. 6, pp. 960–971, Dec. 1999.

135. Oleg Vodyakho and Chris C. Mi, Senior “Three-Level Inverter-Based Shunt Active Power Filter in Three-Phase Three-Wire and Four-Wire Systems”, IEEE Transactions On Power Electronics, Vol. 24, No. 5, May 2009

136. Mauricio Aredes, Jurgen Hafner, and Klemens Heumann,“ Three-Phase Four-Wire Shunt Active Filter Control Strategies”, IEEE Transactions On Power Electronics, Vol. 12, No. 2, March 1997.

137. Pedro Rodriguez, J. Ignacio Candela, Alvaro Luna, Lucian Asiminoaei, Remus Teodorescu, and Frede Blaabjerg “Current Harmonics Cancellation in Three-Phase Four-Wire Systems by Using a Four-Branch Star Filtering Topology”, IEEE Transactions On Power Electronics, Vol. 24, No. 8, August 2009.

138. B. N. Singh, B. Singh, A. Chanda, and K. Al-Haddad, “Digitalimplementation of a new type of hybrid filter with simplified con-trol strategy, ” in Conf. Rec. IEEE-APEC 1999, pp. 642 –648.

139. N. G. Jayanti, M. Basu, I. Axente, K. Gaughan, and. F. Conlon, “Developmentof laboratory prototype of a 12 kVA digital shunt active filter”, inProc. 34th IEEE Ind. Electron. Soc. Conf. (IECON), 2010, Florida, USA,Nov. 10th–13th, 2008, pp. 3129–313.

140. P. Salmeron and R. S. Herrera, “Distorted and unbalanced systems compensation within instantaneous reactive power framework”, IEEE Trans. Power Del., vol. 21, no. 3, pp. 1655–1662, Jul. 2006.

141. Vasco Soares, Pedro Verdelho, and Gil D. Marques, “An instantaneous active and reactive current component method for active filters” IEEE Trans. Power Electron Vol.15 no.4: July 2000, pp 660–669.

142. D.M. Brod and D.M. Novotny, Current control of VSI-PWM inverters, IEEE Trans. Ind. Appl. Vol.**21** June 1985, pp. 562–570.

143. Rajesh Gupta, Arindam Gosh,“ Contorl of cascaded transformer multilevel inverter based D-STATCOM,” Elsevier, Electric power system research, vol.77, June 2007, pp. 989-999.

144. Peng Xiao, Ganesh Kumar Venayagamoorthy, and Keith A. Corzine , Seven – level shunt active filter for high power drive systems, IEEE Trans On Power Electronics, vol 24, no. 1 Jan 2009.

145. Salman Mohagheghi, Ganesh Kumar Venayagamoorthy, Satish Rajagopalan and Ronald G. Harley, Hardware Implementation of a Mamdani Fuzzy Logic Controller for

a Static Compensator in a Multimachine Power System, IEEE Trans on Indus. App vol 45, no. 4 Jan 2009.

Table 1.2 references (chapter 1):

[a] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724–738, Aug. 2002.

[b] S. Rizzo and N. Zargari, "Medium voltage drives: What does the future hold?" in Proc. 4th IPEMC Conf., Aug. 14–16, 2004, vol. 1, pp. 82–89.

[c] R. D. Klug and N. Klaassen, "High power medium voltage drives—Innovations, portfolio, trends," in Proc. Eur. Conf. Power Electron. Appl., 2005, pp. 1–10.

[d] B. Wu, High-Power Converters and AC Drives. New York: Wiley-IEEE Press, Mar. 2006.

[e] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multi-level voltage-source-converter topologies for industrial medium-voltage drives," IEEE Trans. Ind. Electron. , vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[f] P. Steimer, "High power electronics, trends of technology and applications," in Proc. PCIM , Germany, May 2007.

[g] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives,"IEEE Ind. Electron. Mag. , vol. 2, no. 2, pp. 28–39, Jun. 2008.

[h] J. Rodriguez, B. Wu, S. Bernet, N. Zargari, J. Rebolledo, J. Pontt, and P. Steimer, "Design and evaluation criteria for high power drives," in Conf. Rec. IEEE IAS Annu. Meeting, Oct. 5–9, 2008, pp. 1–9.

[i] J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. A. M. Prats, and M. A. Perez, "Multilevel converters: An enabling technology for high-power applications," Proc. IEEE , vol. 97, no. 11, pp. 1786–1817, Nov. 2009.

[j] B. K. Bose, "Power electronics and motor drives recent progress and perspective," IEEE Trans. Ind. Electron., vol. 56, no. 2, pp. 581–588, Feb. 2009.

[k] ABB. [Online]. Available: www.abb.com

[l] SIEMENS. [Online]. Available: www.siemens.com

[m] TMEIC-GE. [Online]. Available: www.tmeic-ge.com

[n] Ansaldo Sistemi Industriali. [Online]. Available: www.asiansaldo.com

[o] Converteam. [Online]. Available: www.converteam.com