PERFORMANCE IMPROVEMENT OF AC-DC POWER FACTOR CORRECTION CONVERTERS FOR DISTRIBUTED POWER SYSTEM

MATADA MAHESH

Dissertation submitted in partial fulfillment of the requirements for the degree of

Doctor of Philosophy
In
Electrical Engineering

Under the supervision of

Prof. Anup Kumar Panda

Department of Electrical Engineering

National Institute of Technology, Rourkela

October 2011

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Declaration

I hereby declare that the work which is being presented in the thesis entitled "***Performance Improvement of AC-DC Power Factor Correction Converters For Distributed Power System***" in partial fulfillment of the requirements for the award of the degree of ***DOCTOR OF PHILOSOPHY,*** submitted to the Department of Electrical Engineering of National Institute of Technology, Rourkela, Orissa is an authentic record of my own work under the supervision of **Prof. A. K. Panda**, Electrical Engineering Department. I have not submitted the matter embodied in this thesis for the award of any other degree or diploma of the university or any other institute.

Date: 19th October, 2011 Matada Mahesh

DEPARTMENT OF ELECTRICAL ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY, ROURKELA

ORISSA, INDIA – 769008

CERTIFICATE

This is to certify that the thesis entitled "***Performance Improvement of AC-DC Power Factor Correction Converters For Distributed Power System***", being submitted to the National Institute of Technology, Rourkela by *Mr. Matada Mahesh*, Roll No. 507EE006 for the award of Doctor of Philosophy in Electrical Engineering, is a bona fide record of research work carried out by him under my supervision and guidance.

The candidate has fulfilled all the prescribed requirements

The Thesis which is based on candidate's own work, has not submitted elsewhere for a degree/diploma.

In my opinion, the thesis is of standard required for the award of a Doctor of Philosophy degree in Electrical Engineering.

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RESEARCH PUBLICATIONS

JOURNAL

1. Matada Mahesh, and A. K. Panda, "Improved dynamic response of single-phase AC-DC power factor correction converter," *International Journal in Power System Optimization and Control* (***IJPSOC-09***), vol. 1, no. 1, pp. 43-48, Jan. 2009.
2. Matada Mahesh, and A. K. Panda, "High-power factor three-phase AC-DC soft-switched converter incorporating zero-voltage transition topology in modular systems for high-power industry applications," ***IET - Power Electron***., vol. 4, no. 9, pp. 1032-1042, Nov. 2011.

3. Matada Mahesh, and A. K. Panda, "Increase of efficiency of a AC-DC PFC boost converter by a novel soft-switching technique", *Intl. Journal of Electric Power Components and Systems*, **Taylor and Francis Publication,** accepted for future publication.

CONFERENCE

1. Matada Mahesh, and A. K. Panda, "Two sided PWM control of switching power factor correction AC-DC converter", *IEEE-International Conf. on Industrial Technology, (IEEE-ICIT'09),* pp. 1-6, Monash University – Gippsland, Australia, Feb. 2009.
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4. Matada Mahesh, A. K. Panda "Implementation of a ZVT based Power Factor Correction Converter", *IEEE-International Power and Energy Conf., (IPEC'10),* pp. 693-698, Singapore, 2010.

ACKNOWLEDGEMENTS

I express my sincere gratitude to my academic and research advisor **Prof. Anup Kumar Panda** *for his excellent guidance, research attitude, encouragement, and kind co-operation throughout the course of my research work. I consider myself fortunate to have worked under his guidance. My family and I are greatly indebted to him.*

I am grateful to my Doctoral Scrutiny Members, **Prof. B. D. Subudhi**, **Prof. K. B. Mohanty**, *and* **Prof. G. S. Rath**, *for their valuable suggestions and numerous help towards my research work.*

I am especially indebted to my past teammates in my Power Electronics research group, **Mr. Swapnajit Pattnaik** *and* **Mr. K. Aroul** *with their meaning-full discussions and moral support. I would like to thank my present research friends* **Mr. Y. Suresh**, **Mr. M. Suresh**, *and* **Mr. T. Ramesh** *for extending their technical and personal support. It has been a great pleasure to work with such a helpful, hard working, and creative group.*

It has been a great pleaser to work in the Center for Power Electronics and Drives (PED) Laboratory of the Electrical Department. I would like to acknowledge the PED Laboratory staff, technician **Mr. Rabindra Nayak** *and* **Mr. Chotilal**, *without them the work would not have been progressed.*

I am grateful to the concerned authorities of my parent Institution, Manipal Institute of Technology, Manipal for sanctioning of leave for my PhD studies.

Without my family's sacrifice and support, this research work would not have been possible. I would like to express my greatest admiration to my mother for her sacrifice and positive encouragement that she showered on me throughout this research work. I shall also always remain

indebted to my parent in-laws for the continuous support they gave me and especially for taking care of my son and supporting my wife (in her busy schedule) during my absence which helped me to complete this thesis in time. I also thank my brother, **Mr. M Bharatish**, *sister in-laws for extending support and encouragement given during my difficult times of my research work.*

My son **Master Nenad** *suffered a lot in my absence from home and I thank him profusely for his sense of understanding and unwavering faith in me.*

Finally, I would end this note by placing my wife **Mridula J** *at the bottom of my heart for the moral and emotional support she gave along with the tolerant effort she put to make this research work complete.*

I dedicate this work to all my family members and relatives.

Above all, I salute the divine powers, the Almighty for their abundant blessings for giving me strength and energy to complete this study successfully.

Matada Mahesh

Dedicated with reverence to memories of my Father,

Late M. M. Jagadeeshaiah

A Great Philosopher, Humanist and Educationist.

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ABBREVIATIONS

AC	Alternating Current
ACMC	Average Current Mode Control
CCM	Continuous Conduction Mode
DC	Direct Current
DCM	Discontinuous Conduction Mode
DPS	Distributed Power System
EMI	Electro Magnetic Interference
ESR	Equivalent Series Resistance
IC	Integrated Circuit
IEEE	Institute of Electrical And Electronics Engineers
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NIT	National Institute of Technology
PF	Power Factor
PFC	Power Factor Correction
PSIM	POWER-SIM (Power Electronics And Drives Simulator)
PWM	Pulse Width Modulation
RMS	Root Mean Square
SC	Semiconductor
THD	Total Harmonic Distortion
ZCS	Zero Current Switching
ZCT	Zero Current Transition
ZVS	Zero Voltage Switching
ZVT	Zero Voltage Transition

Note: Abbreviations are used and mentioned as and when it is required in the theses.

NOMENCLATURE

ΔI_L	Inductor ripple current
A	Scaled down sine signal input to multiplier of ACMC
B	Output signal of voltage compensator in ACMC
C	Output singal of low-pass-filter in ACMC
C_{in1}	Line input filter capacitor
C_{in2}	High frequency bypass capacitor after bridge rectifier
C_o	Output capacitor of boost converter
$\cos \phi$	Cosine of the angle between input voltage and fundamental current
C_r	Resonance capacitor in soft switching converters
C_{sn}	Snubber capacitor
C_{st}	Storage capacitor
C_{vf}	Capacitor in voltage loop of ACMC
D	Duty cycle
D_1-D_4	Diodes in bridge rectifier and/or auxiliary diodes in proposed converters
DB	Boost diode
$dnom$	Nominal duty ratio of semiconductor switch
D_{peak}	Maximum value of transistor duty cycle
D_r	Resonant diode
E_{on_M}	Turn-on energy losses of MOSFET
f_s	Switching frequency of converter
I_{1_RMS}	RMS value of the fundamental input line current
I_{B_RMS}	RMS value of the body diode current of MOSFET
I_D	Drain current of MOSFET
i_{DB}	Boost diode current
I_{F_avg}	Average value of forward current of diode

I_{F_B}	forward current through body diode of MOSFET
I_{F_RMS}	RMS value of forward current diode
I_{in}	Input line current
$I_{in\_peak(max)}$	Maximum value of input current to converter
I_o	Output load current
I_{RMS}	RMS value of the input line current
I_{rr}	reverse recovery current of the boost diode
i_{SW}	current through the MOSFET switch
K_d	Distortion factor lies between zero and one
K_θ	Displacement factor lies between zero and one
L_b	Boost indcuor of boost converter
L_{in}	Input line filter inductor
L_{min}	Minimum value of boost inductor
L_r	Resonant inductor in soft-switching converters
L_{sn}	Snubber inductor
L_{st}	Storage inductor
P_{APP}	Apparent power
P_{C_DM}	Condcution losses of body diode of MOSFET
P_{CM}	Conduction losses of controlled device MOSFET
P_{out}	Output power of boost converter
P_{Real}	Real Power
R_{Dson}	On-state resistance of MOSFET
R_{in}	Resistance of source impedance
R_{Load}	Load resistance
SW	Controlled switch MOSFET of converter with passive snubber circuit

SW_1	Controlled main switch in proposed PFC converter with active snubber
SW_{1_D}	Body diode of main switch of boost converter
SW_2	Controlled auxiliary switch in PFC converter with active snubber
SW_{2_D}	Body diode of auxiliary swich in soft-switched boost converter
T	Time period of a switching cycle
t_{fv}	Fall time of voltage across MOSFET during turn-on
t_{ri}	Rise time of current in MOSFET during turn-on
V_{ac}	AC line input voltage
V_{csn}	Voltage across snubber capacitor
V_{cst}	Voltage across storage capacitor
V_{D_DB}	Voltage across the body-diode of MOSFET
V_{D0}	Diode on-stage voltage
V_{DS}	Drain-source voltage of MOSFET
V_{Drr}	Voltage across boost diode during reverse recovery interval
V_{in}	Input of boost converter or output of bridge rectifier
$V_{in\_peak(min)}$	Minimum value of input peak voltage
V_o	Output voltage
V_{RMS}	RMS value of voltage
V_{sw1}	Voltage across main switch in boost converter
V_{sw2}	Voltage across auxiliary switch in boost converter
X	Voltage compensator block in ACMC
Y	Current controller block in ACMC
Z	Feed-forward or low pass filter block in ACMC
Z_s	Input source line impedance

Note: Notations are used and mentioned as and when it is required in the theses.

ABSTRACT

In present situation, the increase in the utilization of computers, laptops, uninterruptable power supplies, telecom and bio-medical equipments has become uncontrollable as its growth is rising exponentially. Hence, increase in functionality of such equipments leads to the higher power consumption and low power density which provided a large market to distributed power systems (DPS). The development of these DPS posed challenges to power engineers for an efficient power delivery with stringent regulating standards; this is the motivation and driving force of this research work. The objective is to minimize the switching losses of front-end converters employed in DPS, with the primary aim of achieving nearly unity power factor operation of converters.

Single-phase and three-phase rectifiers are increasingly used in the field of alternating current – direct current (AC-DC) power converters as front-end converters in DPS. For power factor correction (PFC) stage, conventional single-phase AC-DC PFC boost converter is the most suitable topology because of its inherent advantages. These PFC boost converters exhibit poor dynamic regulation of output voltage owing to low pass filter in the voltage feedback loop. Research effort has been made to mitigate this problem of AC-DC PFC boost converters. An extended pulse width modulation switching technique has been investigated and proposed especially for single-phase and three-phase AC-DC PFC boost converters to improve the dynamic response of output voltage during transient periods.

Current trends demand the miniaturization of front-end converters in DPS. One of the several methods to achieve the same is operation of PFC converter at higher switching frequency; this in turn increases the switching losses of a PFC converter. Suitable soft switching techniques are generally employed to minimize these switching losses. Also these techniques alleviate the semiconductor switches of PFC converters from extra voltage and/or current stresses. In this research work, two types of zero voltage transition (ZVT) techniques

in PFC boost converters for medium as well as for high power converters are proposed: (1) Boost converter with passive auxiliary circuit and (2) Boost converter with active auxiliary circuit. These PFC converters are designed to operate for 400 V, 100 kHz, 500 W and/or 1500 W specifications. The operation principles and a detailed steady-state analysis of each ZVT based AC-DC PFC boost converters are described and presented. The proposed converters are more reliable and achieve high efficiency with low total harmonic distortion.

Besides improving circuit topology and efficiency, effort is made to achieve power expandability and higher power density for the front-end converters in DPS by modular approach. In addition, this approach also provides higher reliability, easier thermal management, and maintainability.

The proposed converters presented in this research work are well defined by their mathematical modeling and its modes of operations. The prototypes of all the proposed converters are developed in the Power Electronics and Drives laboratory, National Institute of Technology, Rourkela. Their feasibility are verified and confirmed by simulation and experimental results.

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Chapter 1

Introduction

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- **Power factor correction (PFC) techniques**
- **Performance parameters of PFC converter**
- **Soft switching of converter topologies**
- **Modular system**
- **Motivation**
- **Objectives**
- **Dissertation structure**

Introduction

1.1 Research Background

In present situation, the increase in the utilization of computers, laptops, telecom, bio-medical equipments, and uninterruptable power supplies is uncontrollable as its growth is rising exponentially. Hence, increase in functionality of such equipments leads to the higher power consumption and low power density. On the other hand, today's industry/market demands the miniaturization of power sources with higher power density at reasonable price. Therefore, the power supplies for the telecom and computer applications are required to provide more power with less cost and small size.

To achieve these requirements, distributed power system (DPS) is widely adopted. Hence, DPS has evolved from a conventional approach (such as centralized system) by employing isolated DC-DC converters to intermediate bus architecture using non-isolated converters [1, 2].

The requirements aimed by DPSs continue to expand beyond its initial goal of dealing with power distribution problems associated with computer and telecom applications. While centralized power system continues to be a cost effective solution for some applications, additional important factors such as the easier thermal management, higher reliability, need of tight regulation during load current transients, reduced current ripple and the increased quantity of voltages required on a board, have spawned a multitude of distributed power solutions. The basic configuration of a typical DPS is shown in Fig. 1.1. In this system, the front end converters used in DPS applications adopt a two stage approach. In the first stage, the front-end converters connected in parallel provide the power factor correction (PFC) and the second stage provides isolation and highest regulation of the required output DC voltage. As a result, the overall performance of the entire system strongly depends on the choice and

design of individual stages [2-4]. Because of this modular approach, DPS system has many advantages over centralized power system. It is widely adopted for telecom and computer server applications because of its inherent advantages such as higher reliability, modularity, high power density, easier thermal management and easy maintainability [5-10]. Because of these benefits of DPS over the centralized power system, installations of DPSs are rising up especially for power sources to telecom and computer applications.

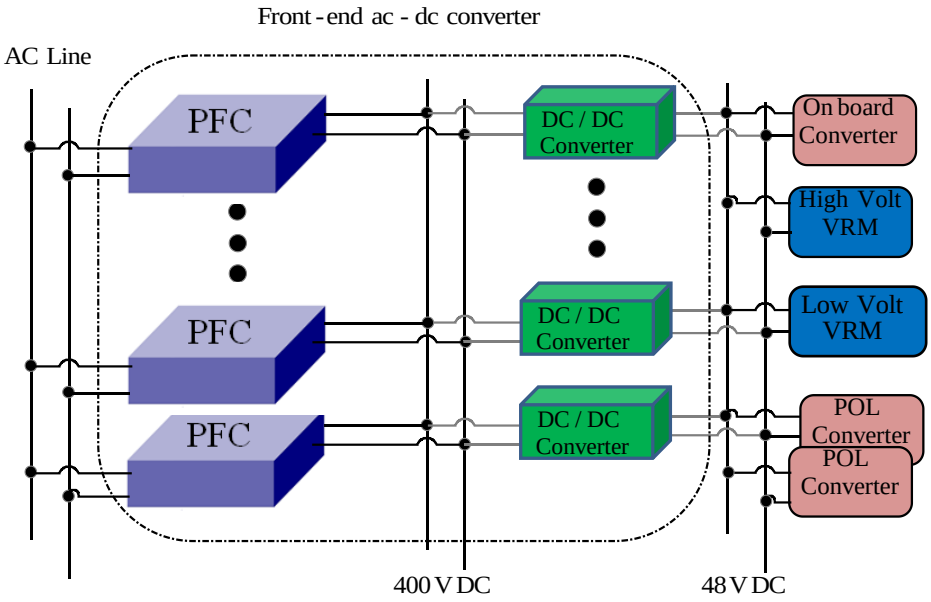


Fig. 1.1 Structure of basic distributed power system

Now a day, high compact, flexible DPS servers for telecom, data networks and computer applications are available in market. A typical image of DPS for telecom server is shown in Fig. 1.2. At the bottom of the server, front-end (AC/DC) converter modules are placed. It can be seen that several modules are placed side by side to provide the energy demanded by the load. After the front-end converter modules, the following stage converters, which are known as load converters on the circuit boards on the equipment modules are located on the upper berth of the rack. Therefore, these load converters are also called on-

board converters. As the size of the racks is fixed for a given DPS, it is desired to have more space for the equipments such as telecom boards or computer servers. Thus, the size and volume of the power supply has to be minimized.

Fig. 1.2 Image of DPS for telecom server system

On the other hand, increase in number of equipments in a system implies more power consumption. Hence, more power is to be supplied from power sources within less volume, which means higher power density. Moreover, DPS for server system has a fixed rack width, such as 19'', 23'' or 26'', 7ft frame work, and the power modules are vertically slide inside the rack, as shown in the bottom part of the Fig. 1.2 . By reducing the profile of power modules, more modules could fit into the rack and provide more power. Therefore, 1.75'' width of module becomes a standard size in a rack, as shown in the bottom part of the Fig. 1.2. By reducing the profile of power modules, more modules could fit into the rack and

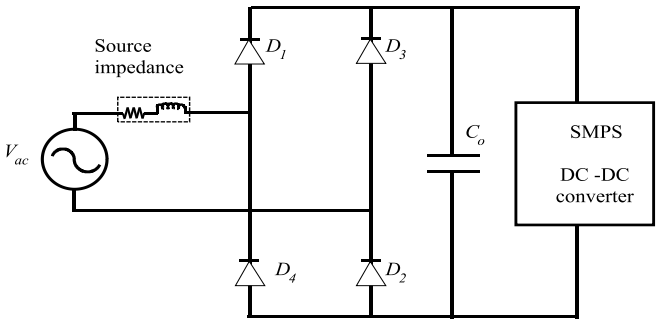
provide more power. Therefore, 1.75'' width of module becomes a standard profile from presently existing power modules.

1.2 Effects of non-linear loads in the power grid

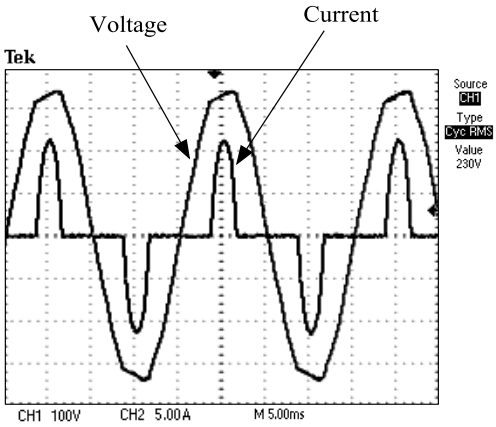
Obtaining power from the utility power grid can be done in different ways. Most of the electronic equipments connected to the electricity power grid draw high peak discontinuous non-sinusoidal line current rather than smooth sine wave current. This current is composed of number of harmonic currents, which flow through electricity power grid as well as in the equipment itself. Fig. 1.3 shows the illustration of experimental set-up of single-phase alternating current-direct current (AC-DC) bridge rectifier followed by bulk capacitor. The schematic of single-phase bridge rectifier shown in Fig. 1.3(a) has been tested in the laboratory. The converter of such arrangement draws a discontinuous non-sinusoidal peak current and hence the presence of harmonic currents in the AC-DC rectifier circuit as well as in the power grid to which this converter is connected. The narrow peak input current occurs due to the short on-time duration of bridge rectifier diodes as the diodes conduct only when instantaneous input voltage is greater than the output voltage. Table 1.1 shows the specification and component values of the AC-DC rectifier circuit under test. The results obtained from the test circuit are shown in Fig. 1.3(b), which shows the input line voltage and line current waveforms of supply frequency 50 Hz. Fig. 1.3(c) represents the harmonic spectrum of the line current.

Table 1.1: Specification and components used in the test circuit of Fig. 1.3

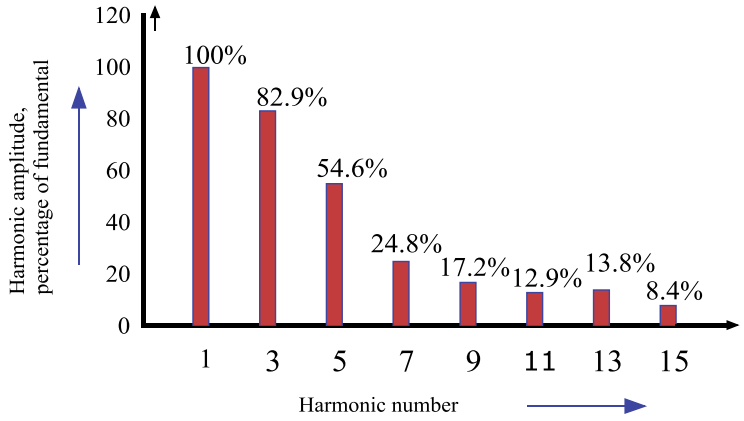
Sl. No	Parameter	Value
1	V_{ac}	230 V(rms)
2	Source impedance, Z_s	R_{in} = 0.4 Ω, L_{in} = 800 μH
3	Output voltage, V_o	320 V (5% ripple)
4	Output power, P_{out}	300 W
5	Load	Constant power load
6	C_o	450 μF/600 V, ESR = 150 mΩ
7	Diodes (in bridge rectifier)	25NSR120 SQ, R_d=20 mΩ



(a) Schematic diagram



(b) Experimentally obtained input voltage and current waveforms



(c) Measurement of harmonics on bridge rectifier + filter capacitor

Fig. 1.3 Single-phase AC-DC bridge rectifier with bulk capacitor

The distortion in the input voltage signal is due to the impedance drop across the source impedance caused by this peak current. In general, the power factor (PF) of a bridge rectifier configuration is dependent on the parasitic resistance of the components, type of the load connected and the size of the capacitor. In the circuit shown above, output capacitor of value 1.3 µF/W is used. This is selected based on a thumb rule, 1 µF-2 µF / Watt for power supplies [11]. For the illustration shown in Fig. 1.3, the resulting PF is equal to 0.35. This low PF and hence, the degradation of the power quality is not only due to the phase-difference between the fundamentals of the voltage and current but also due to the presence of high harmonic current. Thus, a bridge rectifier followed by a bulk capacitor is an

inefficient process, which produces a large spectrum of harmonic signals that may interfere with other equipments connected to the same power grid.

Summarizing, a conventional AC-DC bridge rectifier with bulk capacitor has following main drawbacks:

- It generates harmonics and electromagnetic interference (EMI) in the power grid.
- It has low PF which results in reduced efficiency of the system.
- It increases the operating temperature in the transmission lines as well as in the other equipments connected to the grid.
- It reduces the capacity of line to provide a maximum power to the load.

Thus, in order to overcome the above mentioned drawbacks of a converter, it is essential to improve the power factor of a system.

1.2.1 Definition of power factor

The concept of power factor is a measure of how well the power from the utility grid is utilized. Its value lies in the range between 0 and 1, and it is computed as the ratio of the real power to the apparent power.

$$PF = \frac{Real\ \ power}{Apparent\ \ power} \tag{1.1}$$

Real power is measured in watts and is the power required to do real work. Assuming that the line voltage is a perfect sinusoidal, the real power (P_{Real}) is defined as the product of the fundamental of the voltage (V_{RMS}), the fundamental of the current (I_{1_RMS}) and the phase displacement ($cos\ ø$) between these two fundamentals:

$$P_{Real} = V_{RMS}\ \ I_{1\_RMS}\ cos(\phi) \tag{1.2}$$

Apparent power ($P_{app.}$), is measured in volt-amps, is the real power plus the reactive power,

which makes up the power required to produce the magnetic fields needed to produce real work. It is the product of the RMS voltage (V_{RMS}) and RMS current (I_{RMS}):

$$P_{App.} = V_{RMS} \; I_{RMS} \tag{1.3}$$

by definition (1.1), and from (1.2) and (1.3), the PF can be expressed as:

$$PF = \frac{I_{1\_RMS}}{I_{RMS}} \cos(\phi) \tag{1.4}$$

$$PF = K_d \cos(\phi) \tag{1.5}$$

where K_d is the distortion factor given by,

$$K_d = \frac{I_{1\_RMS}}{I_{RMS}} = \frac{I_{1\_RMS}}{\sqrt{I_{1\_RMS}^2 + I_{2\_RMS}^2 + ... + I_{n\_RMS}^2}} \tag{1.6}$$

where '*n*' is the order of the n^{th} harmonic current.

The displacement power factor K_θ is the cosine of the displacement angle between the fundamental input current and the input voltage,

$$K_\theta = \cos(\phi) \tag{1.7}$$

hence, (1.5) => $PF = K_d \; K_\theta$ (1.8)

A measure of harmonic content in a circuit is total harmonic distortion (THD) defined as the square root of the ratio of the sum of all of the squared higher-order harmonics to the amplitude of the fundamental harmonic. THD is defined as:

$$THD = \frac{\sqrt{I_{2\_RMS}^2 + I_{3\_RMS}^2 + ... + I_{n\_RMS}^2}}{I_{1\_RMS}} \tag{1.9}$$

From equations (1.5), (1.6) and (1.9), we get the relationship between the THD and the PF:

$$PF = \frac{1}{\sqrt{1 + THD^2}} \cos(\phi) \tag{1.10}$$

Therefore, the objective of a power factor correction circuit is to maintain a negligible phase angle between the input voltage and current and to keep the harmonics content to a minimum level.

1.2.2 Compliance and regulations of line current harmonics

As early as 1980, the efforts made in the various power quality surveys by various utilities research organizations, corporate industrial campus, and commercial building installations [12,13] revealed that for better understanding of various power quality problems and to provide cost effective solution to specific problems, monitoring of power quality is the first important step.

Considering the various effects of harmonics and its problems, discussed in the previous section, Electricity regulatory commissions and utilities, all over the world have started imposing penalty for harmonics dumping by the user into the supply lines. In India, Central Electricity Authority through its statutory body Central Electricity Regulatory Commission has notified Institute of Electrical and Electronics Engineers (IEEE) Std. 519-92--(revised version of IEEE Std 519-1981) through legislature [14], about the allowable limits for harmonics in the electrical system. It is essential for both the utility and user industry to understand the related standard and to know the limits specified therein. The IEEE Standard 519 imposes limits on particular harmonics as well as on the THD of the current waveform. The detailed recommended practices of harmonic voltage and current limits have well reported in reference [14].

1.3 Power factor correction techniques

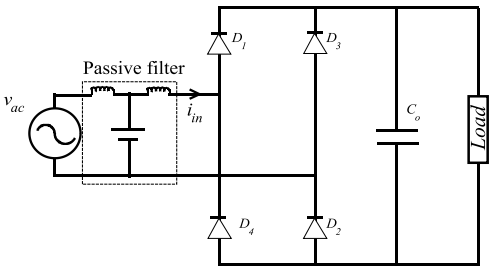
As mentioned earlier, due to the proliferation of non-linear loads in the distribution

systems, current and voltage harmonics are generated in the power grid. Therefore, there is a need to compensate these undesired distortions in order to minimize their effects on the distribution system and hence to improve its efficiency. Broadly, two methods have been come across to eliminate the harmonic related problems and to enhance the overall performance of the grid or distribution systems, namely passive method, and active method. These two harmonic filtering methods are presented and briefly discussed in the following sections.

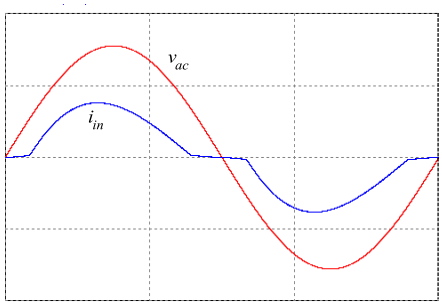
In passive PFC approach, an L-C filter is inserted between the AC line and the input port of the diode rectifier of AC-DC converter [15-16] as shown in Fig. 1.4(a). This technique is simple and rugged but has bulky size and heavy weight components. One filter is to be connected to eliminate one particular harmonic and hence system becomes bulky and expensive in order to eliminate significant amount of harmonics. Moreover, the power factor cannot be very high in this technique.

In active PFC converter techniques, power electronics DC-DC converter is employed and operated at high frequency to shape the input line current as sinusoidal as possible. The simplified basic block diagram of active PFC technique is shown in Fig. 1.4(b). The commonly used topologies as DC-DC converter in active PFC converter are boost, buck, buck-boost, flyback, cuk, or sepic topologies [16-20]. In active PFC technique, the input power factor can reach nearly unity and the AC-DC interface of power converter emulates a pure resistor [15-23]. The boost converter is widely used as a DC-DC converter for PFC applications and is most suitable topology for PFC pre-regulator in telecom applications because of its inherent properties [16, 23, 24]. Hence the DC-DC converter of boost topology is the basic interest of our research and our significance of novel techniques are applied to boost converter in PFC pre-regulator system. The active PFC methods have many

advantages over the passive PFC techniques high power factor, reduced harmonics, smaller size and weight. Hence our research is focused in the area of active PFC converter to achieve near unity input power factor and hence to increase quality of power in the grid.

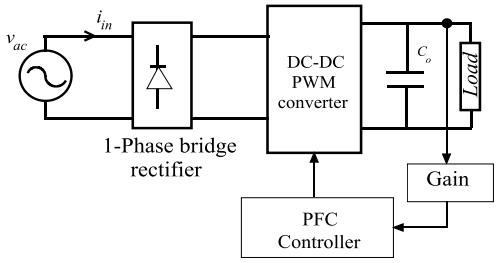


Passive power factor correction technique

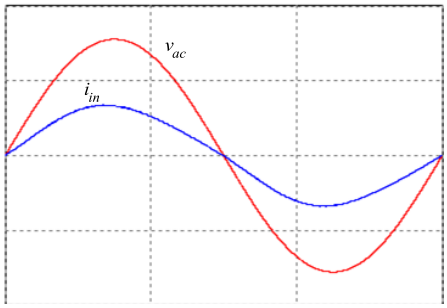


Input voltage and input current response of passive PFC technique

(a)



Active power factor correction technique



Input voltage and input current response of active PFC technique

(b)

Fig. 1.4 Methods of power factor correction techniques

1.3.1 PFC control methods

The PFC control methods are broadly classified into two groups [16, 24-25]. 1) Active control and 2) Automatic control of line current. Active control method is associated with continuous conduction mode (CCM) of the inductor current and hence it is referred as CCM shaping techniques. On the other hand, the automatic control is used when converter operates in discontinuous conduction mode (DCM). For medium and high power applications, CCM is suitable because of low EMI and better input current waveform [16,

24]. The DCM method is employed for low power applications, i.e. 300 W or less. Furthermore, the active control method is classified as follows:

(a) Charge control, (b) Hysteresis mode control, (c) Average current mode control (ACMC), (d) Peak current mode control and e) Non-linear carrier control.

Each control strategy has its own merits and demerits based on the topology of the DC-DC converter employed in PFC converter. ACMC is the fact of standard technique used in industry today for the boost AC-DC PFC converter because of its advantage of less THD, improved noise and easy to shape input current waveform [16, 24, 26-31].

Fig. 1.5 shows the block diagram of ACMC based single-phase PFC boost converter. The feedback system has two control loops. Namely, voltage control loop and current control loop. In Fig. 1.5, block 'X' represents the voltage loop, which is also referred as outer loop and regulates the output voltage that is higher than the peak value of input voltage. Block 'Y' is the inner current loop which is much faster loop. In current control loop, current tracking forces the average value of boost inductor current to track the reference current so that it has the same shape as that of rectified input voltage [32, 33]. This task gives the input a nearly unity power factor. Block 'Z' is basically a low pass filter, which provides the voltage feed-forward signal to the multiplier. This block causes power input of the AC-DC PFC converter to remain constant at a specified level (determined by the load) irrespective of the changes in the line voltage. The magnitude of feedforward signal is proportional to the RMS value of the input voltage.

1.4 Performance parameters of PFC converter

1.4.1 Low bandwidth and its effect on the active PFC converter

In the approach to meet international standard regulations and recommendations, such as IEC 100-3-2, IEE-519, in high quality rectifiers, the main effort is devoted to the quality of

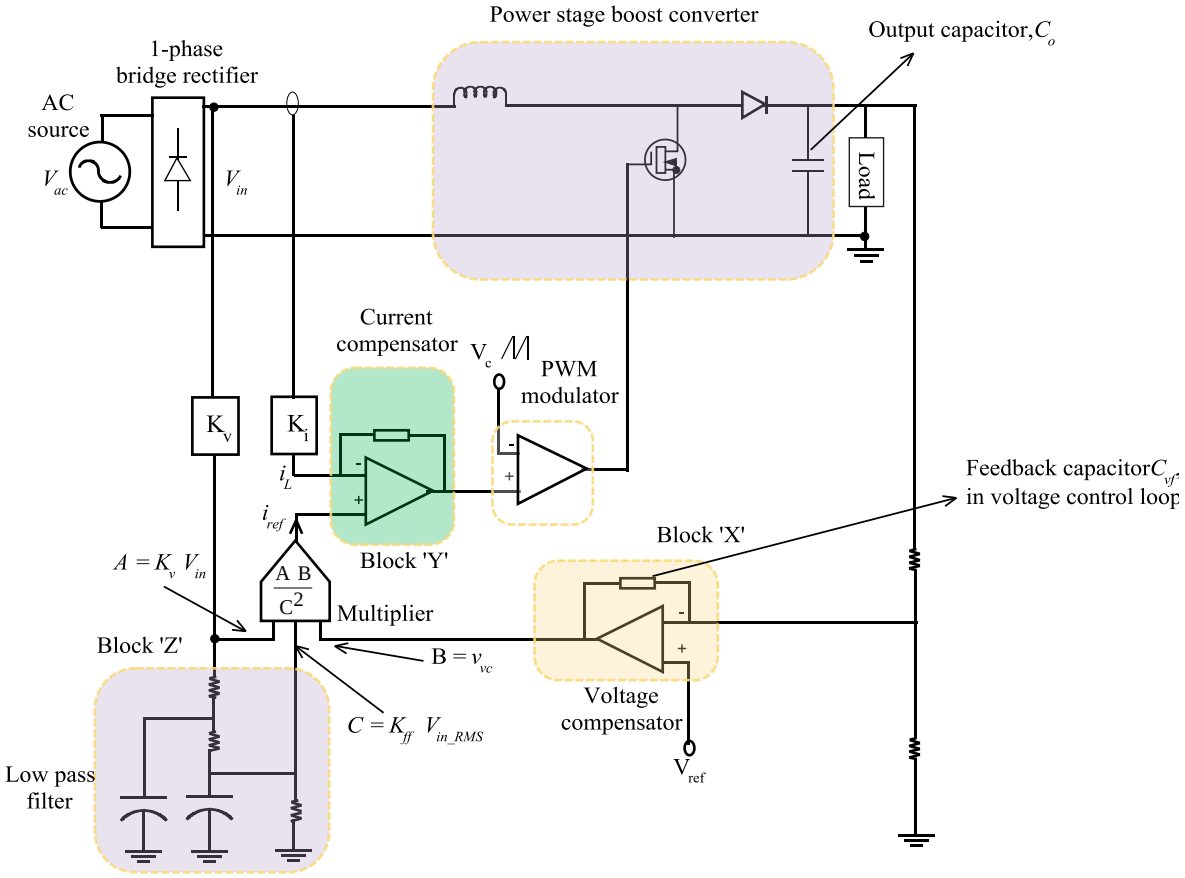


Fig. 1.5 Block diagram of ACMC PFC boost

the input current waveform. But the dynamic response of the output voltage in such converters is sacrificed. This is due to the fact that a low-pass filter has to be placed in the output voltage feedback loop when the bulk capacitor is used at the output terminals of PFC converter [30, 32, 33]. This low pass filter in the voltage feedback loop is needed to reduce the THD of the input line current and hence the improved input power factor of overall system. This makes the poor dynamic response of a converter. For the applications, especially power supplies to air-craft, bio-medical equipments and defense etc, the dynamic response of power supplies cannot be neglected. The most possible operating modes within the PFC boost converter are discussed in this section. The trade-off between output capacitor C_o and voltage loop feedback capacitor C_{vf}, pointed in Fig. 1.5 has been reported in reference [29]. This is essentially based on the effect of output capacitor C_o and voltage loop feedback

capacitor C_{vf} employed in ACMC PFC boost converter, and which can be analyzed on two dimensional graph as presented in Fig. 1.6.

In the linear design region, a very high output capacitor valued along with lower feedback capacitor is used to have the advantage of fast dynamic operation with low ripple on the output voltage. This is the commonly used mode in PFC converters. Hence, earlier design has been stated on this linear region to avoid any undesirable, unknown phenomena inside PFC converter due to the shortage in other operating modes information and analysis.

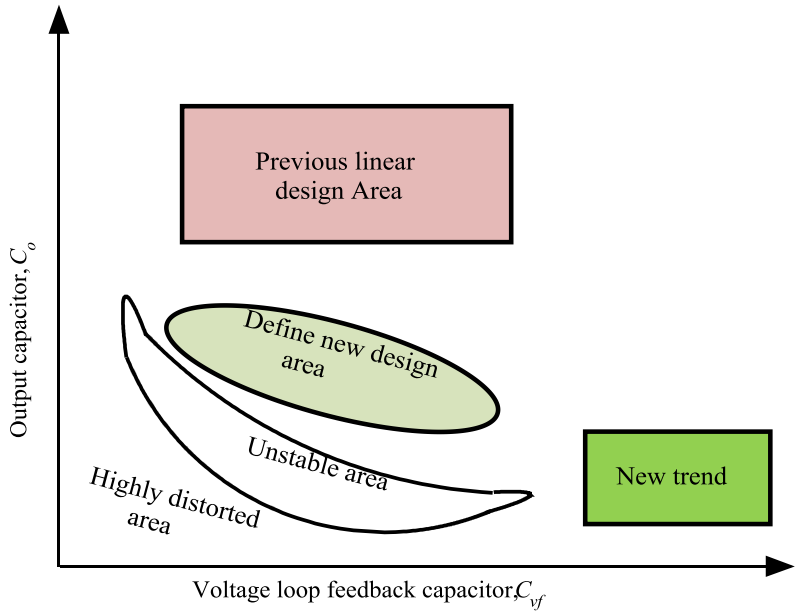


Fig. 1.6 Graph showing all possible dynamic operation of PFC boost converter

Based on the nonlinear design models, new stable and unstable operation regions have been identified by authors reported in references [29, 35-37]. The progressed research in improving the power density, a new stable design regions are identified for a medium output capacitor values and slightly higher feedback capacitors than that used in linear region design. A good performance has been noticed with improvement in dynamic response. However, this leads to the use of a second stage DC-DC converter to obtain regulated output

voltage as this approach has higher output ripple voltage. Unstable region and highly distorted regions also have been detected which result in asymmetrical input current waveform and increased amplitude in the output voltage ripple. In some worst case conditions, input current is seen to be non-sinusoidal current, this is due to the saturation of feedback amplifier in voltage control loop.

The concept of improvement in the dynamic regulation and to decrease the bulk capacitor size can be expressed from the simple example. A second DC-DC converter is cascaded with the first converter, with the bulk capacitor placed in between as shown in Fig. 1.7. Due to the two stage power processing, system efficiency depends on the efficiencies of both stages and obviously efficiency of entire system will be much lower than that of each stage also the controlling of the complicated power circuit cannot be neglected.

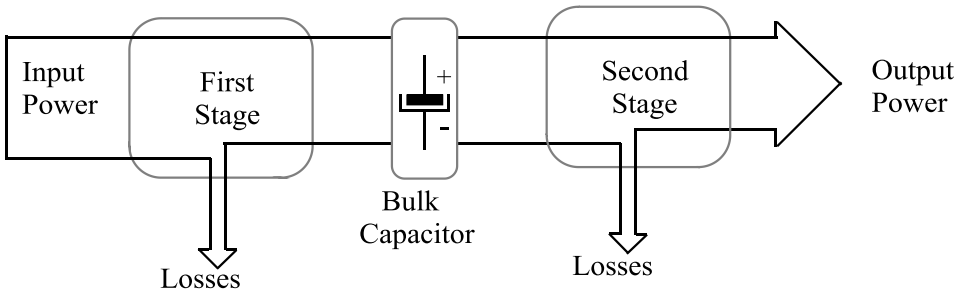


Fig. 1.7 Two-stages in cascaded approach to improve dynamic response of PFC converter

Practically speaking, the dynamic response of PFC converter is mainly restricted by low bandwidth of voltage loop control in the feedback system. Several other methods have been proposed to improve the dynamic response of PFC converters. The extension method of two stage approach discussed above is proposed in reference [34], in which first stage is having dual output voltage of equal magnitude and same is fed to the second stage converter. The main idea in this method is to reduce the value of output capacitor and hence exhibits increased power density and improved dynamic response with no penalty in the efficiency of

converter. This method can be applied to all other possible topologies of DC-DC converter in PFC AC-DC rectifiers. In reference [38], authors have proposed novel dynamic improvement based on dual controller method. In this technique, the voltage control block has two loops. One loop is having low bandwidth which is active during steady state operation and other loop is having high bandwidth which is active during transient response of a system. Only one loop will be operating at any instant of time. The better dynamic performance can be achieved with this method but the additional auxiliary circuit is incorporated to drive either of two voltage loops to transit from steady state to transient or vice versa lead to the complexity in the control circuit.

The simple novel idea is introduced in reference [39], in which the PFC boost converter is of soft switching. In this proposed method, voltage loop has a variable gain, with small steady state error and to achieve wide bandwidth with sufficient phase margin. The compensation network is optimized dynamically to achieve a satisfactory result during transient period. It has been noticed that, the transient response from full-load to low load is improved by 31% when compared with the conventional pulse width modulation (PWM) control.

The novel two sided PWM control is proposed in our research and is discussed in chapter 2 of this thesis to improve the dynamic response of PFC boost converter.

1.4.2 Losses in PFC converter

For application like DPS, high power density and low profile begin to be the standard approach. Since, the volume of passive components of the converter reduce with the increasing of the switching frequency, the converters are operating at higher switching frequencies. It is still questionable that PFC is able to operate at such a high switching frequency. In a conventional PFC boost converter, because of the CCM operation, large

diode's reverse recovery current flows. Therefore PFC converter has large switching loss and is not able to work at high switching frequency. Furthermore, especially at low input line voltage condition, a large conduction loss is caused by input diode bridge and MOSFET on-state resistance due to high line current level.

One of the major issues in operating the PFC converter at high switching frequency is the occurrence of switching loss during switching transient period. Although conduction loss approximately remains same for all different switching frequencies, switching loss increases proportionally to the switching frequency. Hence, to enable the converter to operate at higher switching frequency and to improve the efficiency, switching loss must be eliminated or minimized. In the past years, much research and efforts have been done to minimize the PFC converter switching loss as well as conduction loss.

The active power switch used in the PFC converter is one of the most eminent sources for power loss. The device losses are broadly classified into three categories: conduction losses, switching losses and blocking losses. The blocking losses are also referred as leakage losses and are normally being neglected. Metal oxide semiconductor field effect transistor (MOSFET) is the active switching device used in the boost converter of our proposed research work; hence, hereafter the discussion on losses is applicable to MOSFET in boost converter unless it is specified in the thesis. The conduction loss of the MOSFET is the current square times the on-state resistance of the device. On the other hand, switching loss is due to the overlapping of the voltage and current waveforms during switching transition. This switching loss is approximated as the half the drain voltage times the inductor current over the switching time [40-43]. The switching loss of MOSFET also includes the loss due to output (drain-source) capacitance. The charge is stored in the output capacitor of MOSFET device. This stored charge is dissipated during turn on transition of MOSFET and

this is calculated as half the output capacitance times the square of drain-source voltage times the switching frequency. The other losses also exist in the converter due to MOSFET body diode conduction loss, control circuit and gate drive loss.

A new concept based on energy balance condition is reported to calculate the switching loss due to the output capacitance of MOSFET [44-47]. The relationship between output capacitance and switching loss of MOSFET is found as a combined ratio which can't be separated into two terms; The result obtained from this method shows that switching energy loss can remain same and is given by 0.5 (I_D)(V_{DS}) (t_{fall}+t_{rise}), as the total of switching and output capacitance losses [43]. On the other-hand, the effect of output capacitance of MOSFET affects the rise and fall times over the switching period. The switching losses in each semiconductor device of the converter are calculated and the converter is to be designed to eliminate or to minimize the losses to improve the overall efficiency of the converter.

1.4.2.1 MOSFET and Diode loss calculation

1.4.2.1.1 Conduction losses

Conduction losses in power MOSFET are calculated using an MOSFET approximation with the drain-source on-state resistance R_{DSon}.

$$v_{Ds}\,(i_D) = R_{DSon}\,(i_D)\,(i_D) \tag{1.11}$$

v_{Ds} and i_D are drain-source voltage and the drain current respectively. The typical value of R_{DSon} can be read from the device data-sheet diagram.

Therefore, the instantaneous value of MOSFET conduction losses is:

$$p_{CM}(t) = v_{Ds}\,(i_D) = [R_{DSon}]\; i_D^2(t) \tag{1.12}$$

By integrating the above equation, over the period of cycle, the average value of the MOSFET conduction losses can be obtained as,

$$P_{CM} = \frac{1}{T}\int_0^T p_{CM}(t)dt = \frac{1}{T}\int_0^T R_{DSon}\, i_D^2(t)dt = R_{DSon}\, I_{DRMS}^2 \tag{1.13}$$

where I_{DRMS} is the RMS value of the MOSFET on-state current.

The conduction losses of the anti-parallel diode of MOSFET are also considered as it conducts for short duration of operation of the PFC converter topology proposed and described in chapter 4. The conduction losses of body diode of MOSFET can be calculated using a diode approximate equivalent circuit which is a series connection of voltage source V_{D0} representing diode on-state voltage and a diode on-state resistance R_{DSon}, V_{D_DB} being the voltage across the diode and i_{F_B} the current through the body diode:

$$v_{D\_DB} = v_{D0} + R_{DSon}\,(i_{F\_B}) \tag{1.14}$$

The instantaneous value of power loss due to body diode conduction is given by,

$$p_{C\_DB}(t) = v_{D\_DB}(t)\, i_{F\_B}(t) = (v_{D0})\, i_{F\_B}(t) + R_D\, i_{F\_B}^2(t) \tag{1.15}$$

If I_{B_RMS} is the *RMS* value of body diode current, the average value of body diode conduction losses over a period of switching cycle T is

$$P_{C\_DB} = \frac{1}{T}\int_0^T p_{C\_DB}(t)\, dt = \frac{1}{T}\int_0^T [v_{D0}\, i_{F\_B}(t) + R_D\, i_{F\_B}^2(t)]dt = v_{D0}\, I_{F\_Bavg} + R_D\, I_{F\_BRMS}^2 \tag{1.16}$$

In the same way, the conduction loss of the main or boost diode of converter can be calculated and is given by,

$$P_{CD} = \frac{1}{T}\int_0^T p_{CD}(t)\, dt = v_D\, I_{F\_avg} + R_D\, I_{F\_RMS}^2 \tag{1.17}$$

where, P_{CD} is the total conduction losses of boost diode.

I_{F_avg} and I_{F_RMS} are average and RMS values of forward current flowing through diode under consideration respectively.

1.4.2.1.2 Switching losses and gate drive losses

The switching loss is the sum of the switching losses during turn-on and turn-off processes of the MOSFET. Whenever the boost diode in PFC boost converter switches off, the reverse recovery current of that diode flows through the MOSFET as soon as MOSFET turns on. Hence the turn-on losses of MOSFET is the sum of switch–on energy loss without considering the boost diode reverse recovery effect and switch on energy dissipation caused by reverse recovery current of boost diode in the MOSFET. To have clarity in the calculation of total switching losses within the MOSFET device, a switching characteristics of a MOSFET shown in Fig. 1.8 is considered. Fig. 1.8(a) presents the drain-source voltage V_{DS} and drain current i_D waveforms without considering the reverse recovery current of boost diode in a converter. The qualitative overview of the instantaneous power loss of a MOSFET, which is a product of device voltage and current waveforms, is shown in Fig. 1.8(b), while Fig 1.8(c) shows the reverse recovery current switching effects of the boost diode on the switching losses of the MOSFET during turn-on process. The total turn-on energy losses, E_{on} of the MOSFET is approximately equal to the sum of total energy enclosed by the triangle during turn-on process of Fig. 1.8(b) and the total energy stored in the boost diode shown in Fig. 1.8(c).

Therefore, $$E_{on\_M} = V_{DS}\ (I_{D\_on}) \left[\frac{t_{ri} + t_{fv}}{2}\right] + Q_{rr}\ (V_{DS}) \tag{1.18}$$

where, t_{fv} is the voltage V_{DS} fall time and t_{ri} is the current I_D rise time of MOSFET during turn-on process.

The turn-off energy losses in the MOSFET can be calculated in the similar manner. From Fig. 1.8(b), considering the turn-off transition of MOSFET,

$$E_{off\_M} = V_{DS}\ (I_{Doff}) \left[\frac{t_{rv} + t_{fi}}{2}\right] \tag{1.19}$$

where t_{rv} is the rise time of the MOSFET drain-source voltage and t_{fi} is the fall time of the MOSFET drain current i_D.

Turn-on energy in the boost diode consists of mostly of reverse recovery energy, denoted by E_{onD}: Hence, It can be calculated as follows,

$$E_{on\_D} = \int_0^{tri+tfv} v_D(t)\, i_F(t)\, dt \approx E_{on\_Drr} = \frac{1}{4} Q_{rr}\, V_{Drr} \tag{1.20}$$

V_{Drr} is the voltage across the boost diode during reverse recovery (not shown in Fig. 1.8).

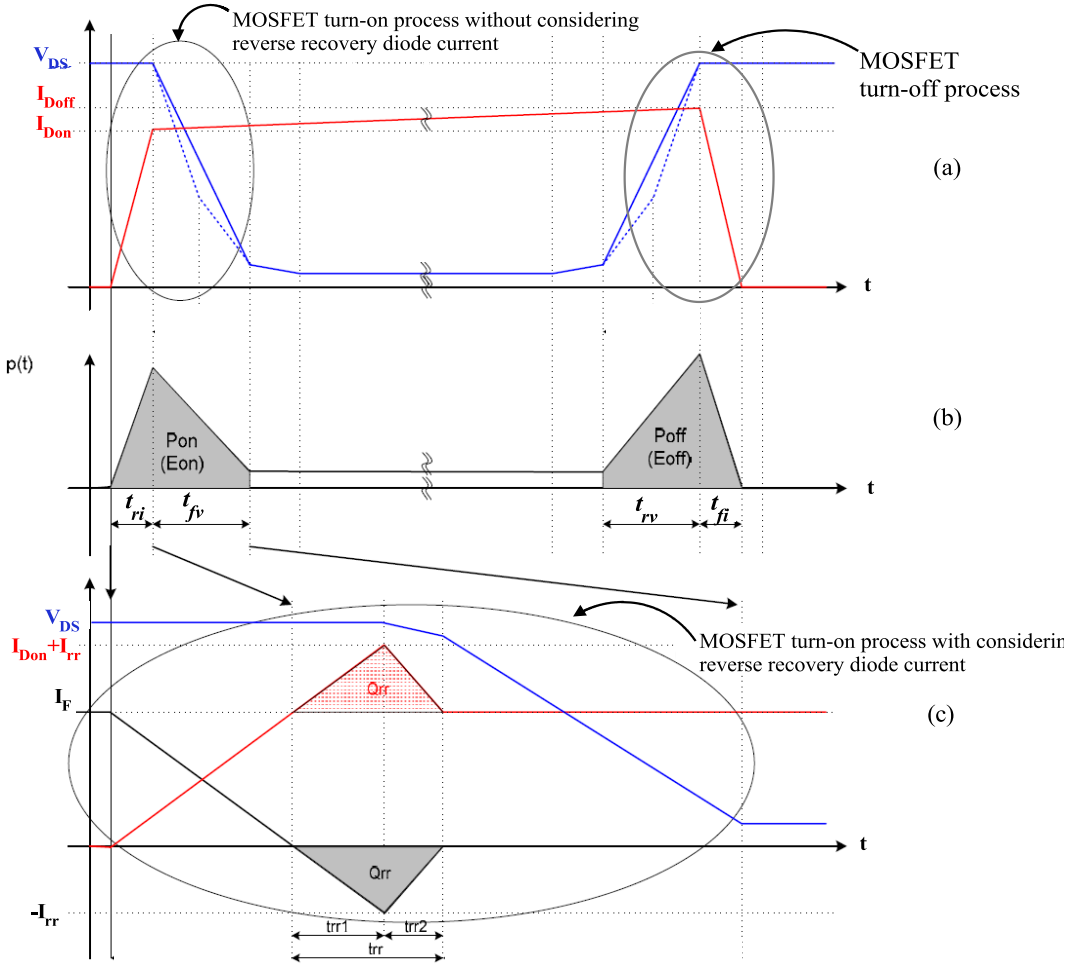


Fig. 1.8 switching characteristics of MOSFET

For the worst case condition, this voltage is approximated as the output voltage (higher) level of boost converter. The switch off losses within the diode is normally neglected. Hence, the switching losses in the MOSFET and the boost diode are the product of switching energies and the switching frequency of the converter. Therefore,

$$P_{SW\_M} = (E_{on\_M} + E_{off\_M})\ f_s \tag{1.21}$$

$$P_{SW\_D} = (E_{on\_D} + E_{off\_D})\ f_s \approx E_{on\_D}\ (f_s) \tag{1.22}$$

Gate drive losses of the parameters of the MOSFET are defined by the gate charge Q_g, the gate driving voltage V_g and switching frequency f_s as,

$$P_g = Q_g\ V_g f_s \tag{1.23}$$

hence, the total loss in the converter can be expressed as,

$$P_{total\_loss} = P_{CM} + P_{C\_DB} + P_{CD} + P_{SW\_M} + P_{SW\_D} + P_g \tag{1.24}$$

$$P_{total\_loss} = P_C + P_{SW} + P_g \tag{1.25}$$

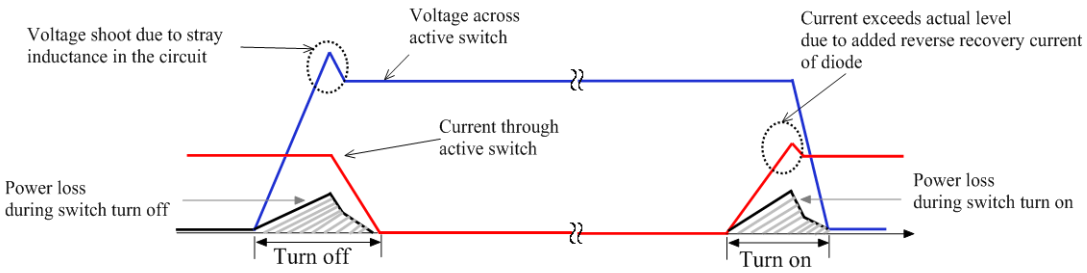
where, $P_C = P_{CM} + P_{C\_DB} + P_{CD}$ and $P_{SW} = P_{SW\_M} + P_{SW\_D}$

The overall efficiency of a converter is determined by a ratio of output power delivered to the load to the input power of the converter. Hence,

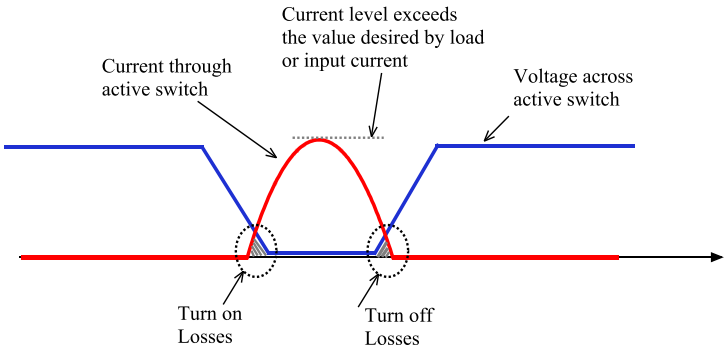
$$\eta_{converter} = \frac{P_{out}}{P_{in}} \tag{1.26}$$

where, P_{out} is the power consumed by the load and P_{in} is the power input to the converter. Overall efficiency η can be improved by reducing the losses in a converter. The approximate switching losses of conventional hard switched converter and that of resonant converter switching losses are shown in Fig. 1.9. By the application of suitable soft switching technique in a converter, the unavoidable switching losses can be minimized. However, the stress and strain of a switching device during turn-on and turn-off processes

shown in Fig. 1.9(a) and Fig. 1.9(b) can also be eliminated by employing suitable soft switching techniques such as ZVT, ZCT and active clamp topologies. When switching frequency becomes very high, a significant compromise has to be made between conduction loss and frequency related losses such as, switching loss and gate drive loss. Several soft switching driver circuits for converters are proposed in the past for improvement in the efficiency of a converter [48-52].



(a) Conventional hard switching



(b) Resonant converter switching

Fig. 1.9 Unavoidable switching losses in converters

1.5 Soft switching converter topologies

In 1980s, lots of research efforts were established towards the use of resonant converters. The basic circuit diagram of conventional boost PWM switch is shown in Fig. 1.10. A fundamental deviation from the conventional forced turn-off approach is the 'zero current' switching technique reported in references [53, 54]. In probing for a general zero

current switching (ZCS) technique, authors have proposed the 'resonant switch' in reference [55]. By simply replacing the power switches in conventional PWM converters by resonant switches, new families of converters called 'quasi-resonant' converters were introduced. This new family of converters can be viewed as hybrid converters between PWM converters and resonant converters. Diverse forms of quasi-resonant concepts in PWM converters have been reported in literature [56-78]. These quasi-resonant converters utilize the principle of inductive or capacitive energy storage and transfer in a similar fashion as PWM converters and the circuit topologies also resemble those of PWM converters. It is to be noted that, in

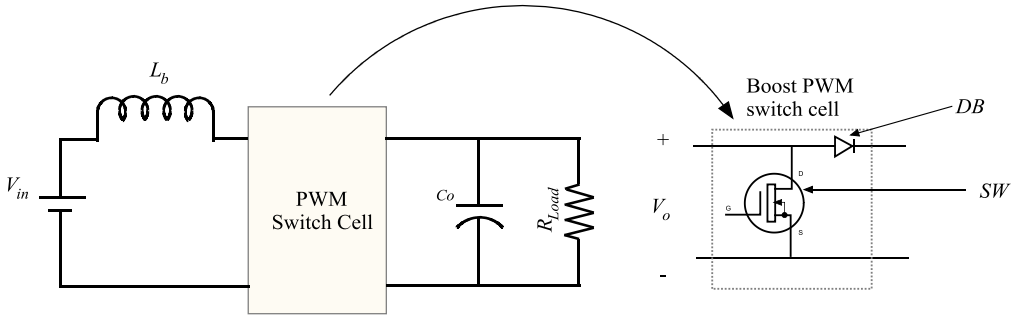


Fig. 1.10 Conventional boost converter PWM switch cell

these converters, an *LC* tank circuit always present near the power switch and is used not only to obtain the sinusoidal voltage or current waveforms of the power switch but also to store and transfer energy from input to output in a manner similar to the conventional resonant converters. A resonant inductor L_r is connected in series with active switch *SW* to achieve ZCS operation and resonant capacitor C_r in parallel with active switch *SW* provides ZVS operation. In general, the actual implementation of the resonant switch can be either a 'half-wave' configuration or a full-wave configuration. The basic resonant switch configurations for ZCS operation of a switch *SW* are shown in Fig. 1.11 (a)-(c). The resonant diode D_r in series with the active switch *SW* creates ZCS half wave configuration as this

arrangement provides unidirectional current and on the other hand, the resonant diode D_r connected in anti-parallel with switch *SW* provides ZCS full-wave configuration. Similarly, the half-wave and full-wave configuration of ZVS resonant converters can be obtained and have been reported in reference [79]. It has been found that, the resonant converters employing half-wave resonant switches have DC voltage conversion ratios sensitive to load

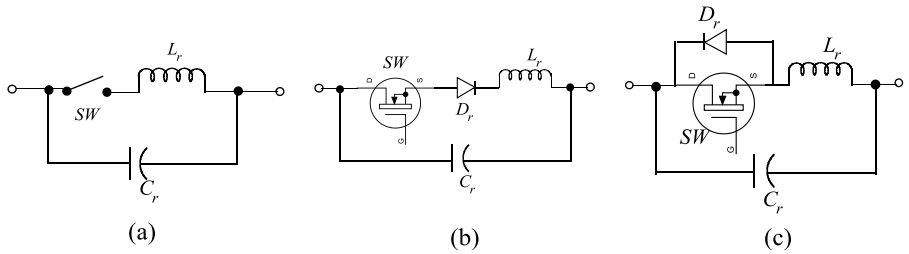
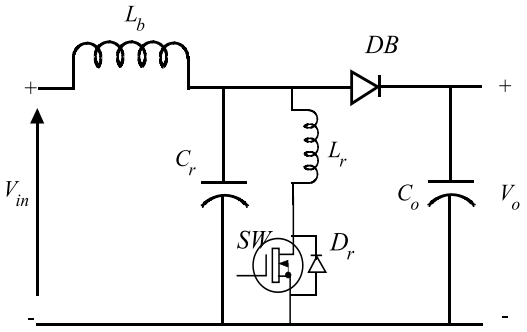


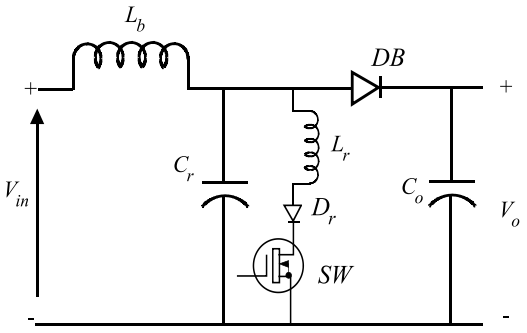
Fig. 1.11 Resonant switch configurations (a) General topology (b) Half-wave configuration and (c) Full-wave configurations

variation. However, the DC voltage conversion ratios can be made load independent by simply modifying the resonant switch into a full-wave configuration [66]. Fig. 1.12 shows the basic topologies of soft switching resonant converters. In the ZCS quasi-resonant switch converter shown in Fig. 1.12(a) and Fig 1.12(b), the boost diode *DB* operates with ZVS and the active switch *SW* and resonant diode D_r operate with ZCS. On the other hand, the active switch *SW* and resonant diode D_r operate in ZVS and boost diode *DB* operate with ZCS in full-wave ZVS quasi-resonant converter shown in Fig 1.12(c).

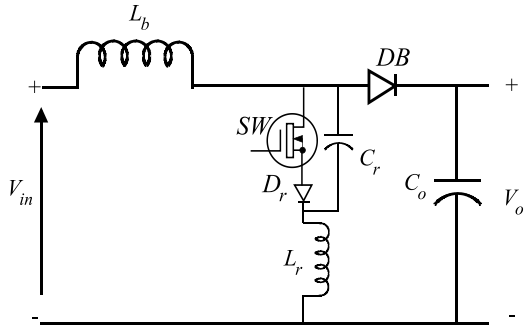
There are some drawbacks in quasi-resonant converters which are discussed above, such as, the limitation of maximum switching frequency in ZCS quasi-resonant converters. This is because of the capacitive turn-on switching loss caused by the discharge of the output capacitance of the switch in ZCS quasi-resonant converters. Since, this loss is proportional to the switch output capacitance, switching frequency and proportional to the square of the input voltage. It has a particularly significant effect on the performance of the ZCS quasi-resonant



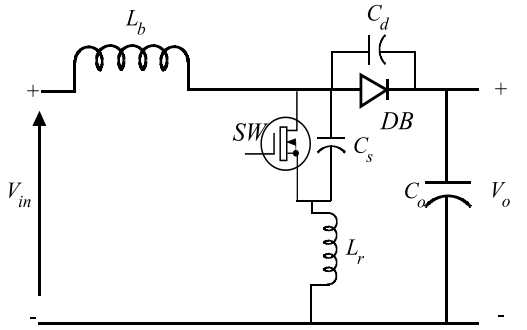
(d) Full-wave ZCS quasi-resonant boost converter



(c) Half-wave ZCS quasi-resonant boost converter



(a) Full-wave ZVS quasi-resonant boost converter



(b) ZVS Multi-resonant boost converter

Fig. 1.12 Basic topologies of soft switching resonant converters

converters. In addition to this, the current level flowing through the circuit components will be higher than the required values of input current and load current. ZVS quasi-resonant converters do not suffer from turn-on switching loss, and therefore can operate at higher frequencies than ZCS quasi-resonant converters. Since, they do not circulate a significant amount of energy; they can achieve extremely high efficiencies. However, their applications are very limited because of design constraints imposed by the characteristics of today's semiconductor devices that limit their input voltage and load range [80]. The multi-resonant converters are the resonant converters which overcome the above mentioned drawbacks of ZVS and ZCS quasi-resonant converters. In multi-resonant converters, soft switching is achieved by unique arrangement of a multi-element network that absorbs all major parasitic in the resonant circuit, including the active switch output capacitance, diode junction

capacitance and transformer leakage inductance. The ZVS based multi-resonant converter is shown in Fig. 1.12(d). This unique arrangement of parasitic element in the converter allows these converters to operate at high switching frequencies with favorable soft switching conditions for all the semiconductor devices in a converter, i.e. with zero voltage turn-on of the switch(es) and zero voltage turn-off of the diode(s). Like any other ZVS converters, ZVS multi resonant converters require constant off-time, variable-frequency control, but they can also be modified to operate at a constant frequency [56, 81,82]. But the major drawback of multi-resonant converters is the increased circulating energy which is caused by a continuous resonance of the multi-element resonant circuit. The effect of this circulating energy is particularly significant for applications with wide input voltage range. Also, since multi-resonant converters regulate the output voltage with constant off-time, their frequency increases as the load decreases and the input voltage increases. Therefore, frequency dependent losses increase. This increased conduction losses (due to the increased circulating energy) and increased frequency-dependent losses significantly affect the partial-load efficiency. However, for properly designed converters that reduce the circulating energy, high partial-load efficiency can be maintained down to 30% - 40% of full load [56].

Apart from these resonant converters, other soft switching techniques known as active clamp converters for AC-DC PFC converters as well as for DC-DC converters have been reported in the literature [83-87]. These techniques achieve soft switching to main switch as well as to other switching devices in a converter, but the soft switching process under zero voltage switching is load dependent. Hence, the voltage and current ratings of the switches employed in these active-clamped converters are higher than the source voltage and load current levels [88-89].

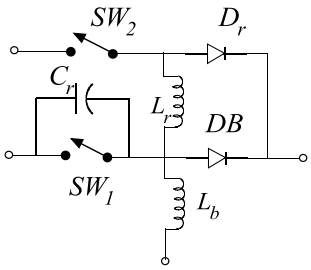
To reduce the semiconductor device switching losses and to overcome some of the

drawbacks of a converter discussed above, passive snubber techniques came into the research [71, 90-96]. The soft switching by adding auxiliary passive circuit (which consists of only passive switches and passive elements) in association with conventional DC-DC PWM converter achieves ZVS or/and ZCS of active switch as well as other passive semiconductor devices employed in auxiliary circuit. These soft switching techniques with passive snubber circuits are popular and still rolling in the industrial research because of their simplicity in design and increased efficiency of converters. However, some of the lossless passive snubber circuits proposed in references [71, 92,94, 96] suffer from increased device stress and hard switching of boost switch and boost diode at higher frequency operation of a boost converter.

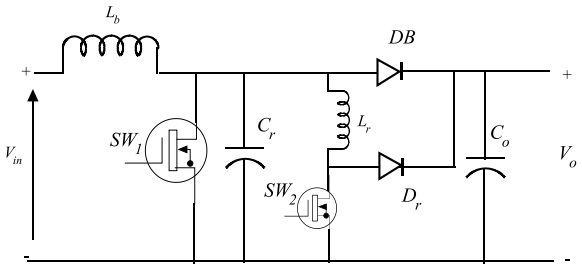
The succeeding and most attractive soft switching techniques in these days are zero voltage transition (ZVT) and zero current transition (ZCT) PWM techniques which are most commendable ones among other existing soft switching techniques [47, 79, 97-98] and considerable research effort has been come across in this ZVT and ZCT soft switching technique [47, 72, 79, 97-117]. In ZVT and ZCT soft-switching techniques, one auxiliary active switch, passive devices and elements forming an auxiliary circuit is connected in parallel with the conventional boost active switch. The basic ZVT and ZCT topologies are shown in Fig. 1.13. This arrangement provides a partial resonance period created by a shunt auxiliary circuit to achieve ZCS or ZVS during the switching transition. This technique retains the advantages of a conventional PWM converter and quasi-resonant converter because once the switching transition is over, the converter operation reverts to the regular PWM operation mode. Hence, the features of the ZCT PWM and ZVT PWM soft switching converters are summarized as follows:

- Zero voltage/current turn-on/off for the active power switch over the wide line and load range.

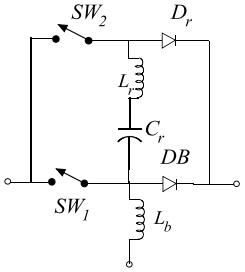
- Low voltage/current stresses of the power switch and rectifier diode.
- Constant switching frequency operation in the converter.
- Minimal circulating energy within the converter.



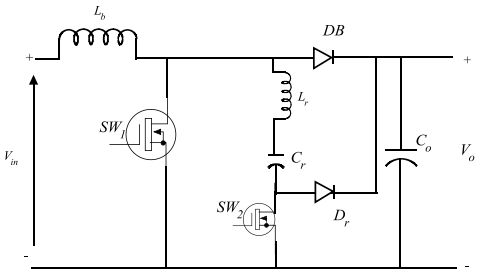
(a) ZVT PWM switching cell



(b) Boost ZVT PWM switching cell



(c) ZCT PWM switching



(d) Boost ZCT PWM switching cell

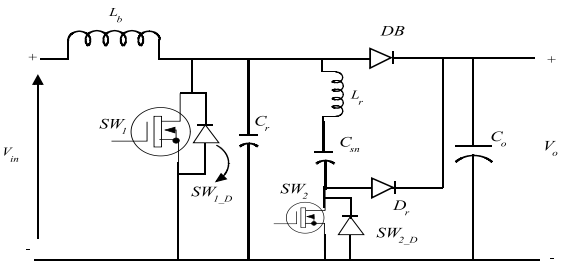


Fig. 1.13 Basic topologies of ZVT and ZCT PWM converters

As discussed earlier, the proliferation of utilization of laptops, biomedical equipments and portable equipments applicable to all applications, claim for power sources of high power

density and high efficiency. Power density in PFC pre-regulator power sources can be improved by reduction of losses and size of components. Size reduction of magnetic components and other passive elements can be done up to certain extent depending upon the operating switching frequency of the converter. Thus, the recent demands for high efficiency, high power density, and reasonable cost power supply for telecom and computer applications in DPS motivates to design pre-regulator PFC boost converters with active or passive auxiliary circuits at different load conditions.

The proposed converters of our research work can achieve high efficiency and high power density by reducing losses and operating at high switching frequency. Also, these topologies reduce the voltage or/and current stresses, which lead to the low power rating components at reasonable cost of an overall system.

1.6 Modular system

The use of three-phase AC-DC rectifiers with high quality input currents with excellent output voltage regulation to meet telecommunication standards have been reported in references [10, 84, 118-122]. The main intension of this approach is to achieve higher power expandability and low volume occupancy of distributed power system sources. In this modular approach, three identical single-phase AC-DC converter modules are connected in parallel to form a three-phase converter system with or without using the neutral line of the three phase power supply (which may not be available in some applications or installations). With this approach, the single output filter capacitor is enough at the output of the three-phase converter whose volume and weight are reduced drastically owing to the fact that, like the three-phase rectifier, the dominant ripple frequency is six times the input source frequency. This approach of three-phase AC-DC converter has its own vantage of providing 48 V or 24 V DC voltage output from three-phase AC supply with a direct

single stage power converter with automatic PFC, electrical isolation and simple DC-DC control characteristics. Fig. 1.14 shows basic block diagram three identical AC-DC PFC converters in modular system. Besides the above mentioned merits, the modular approach has the following advantages [10, 84, 120, and 121].

- Improved reliability and performance of converters.
- Flexibility in expanding the power rating of converters.
- Low periodic maintenance and repair of power converters because of the use of standard single-phase converter units.
- Avoids the use of expensive components of larger rating which may occur in single high power converter.
- Calibration of components directing to reduction in manufacturing cost and time.

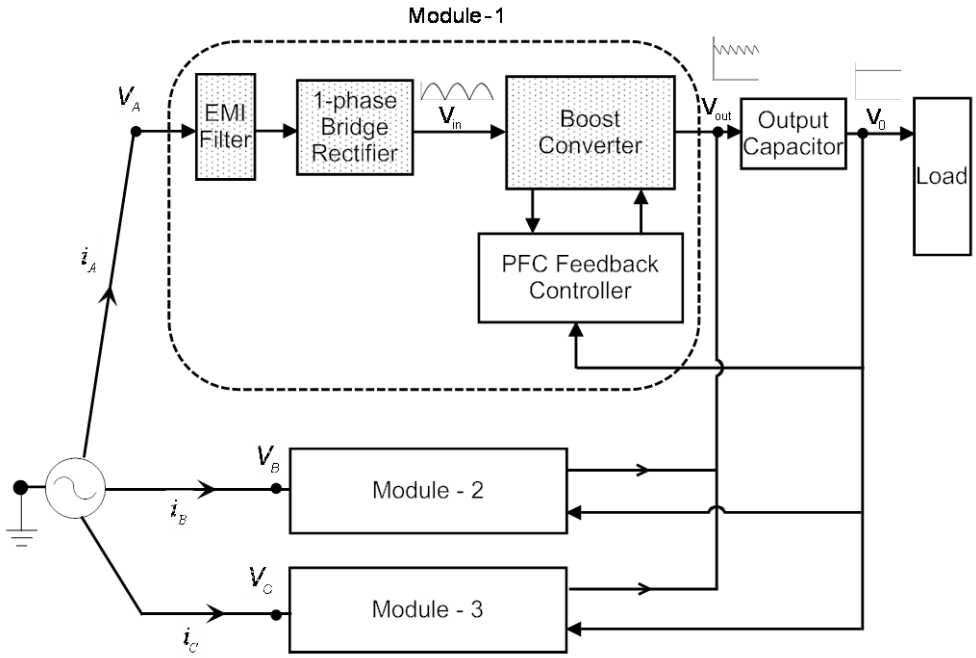


Fig. 1.14 Block diagram of three identical PFC converters in modular approach

Modular approach presented in [121] for three – phase applications suffers from problem of phase current interactions between different modules, this phase current interaction affects the slope of the boost inductor current during the off period of the main switch. In the proposed converters of our research work, no such interaction takes place between modules as such systems have been developed and is well presented in [84, 120].

1.7 Motivation

The tremendous requirements of power sources for almost all electronic products under different power ratings pose stiff challenges to power supply designer. Regulated voltage at DC bus bar, increased current requirements and the dynamic characteristics of AC-DC active PFC converters create new demands on power distribution and management. The issues such as high efficiency, high power density, and fast dynamic response etc, became critical for specific applications such as power sources to telecom and computer servers, bio-medical equipments, and aeronautical engineering. The transfer of electrical power from power grid to customer end with low cost and increased efficiency has been made possible due to advances in Power Electronic converter design with sophisticated control methods. But compromise is to be done in some extends with size, weight and cost etc. in today's Power Electronic apparatus.

The cost, size and performance advantages have promoted Power Electronics applications extensively in industrial, commercial, residential, aerospace and military environments in recent years. Today, a market demands the miniaturization of power sources. This compels to go for high switching operations of power converters which reduce the size of magnetic components employed in converters. High switching operation of converters leads to the increased switching losses which reduce the efficiency of converters. Another basic requirement for electronic loads in DPS is to provide galvanic isolation to

satisfy safety standards and to achieve flexible system configuration. These requirements can be fulfilled by employing active PFC converters is DPS. The research is still progressing to achieve fast dynamic response, better efficiency, and high power expansion with stringent regulatory standards, which motivates to develop improved performance of active PFC converters employed in DPS. A simple extended PWM switching technique has been investigated in our research work and employed in AC-DC PFC converter to improve the dynamic response during step change in load current and line voltage. The same concept is extended to three-phase system in modular approach to expand the power rating of converters.

Increased popularity of DPS claims for high power density and efficiency of AC-DC PFC converters. Power density will be improved by reduction of losses and size of components. Size reduction can be done up to certain extent depending upon the operating switching frequency of the converter. Several topologies were proposed in past few years such as: quasi-resonant converter, resonant converter and ZVT-PWM converter; to reduce losses. But resonant converters suffer from the disadvantage of high voltage and current peaks. This in-turn causes the device ratings to be much higher than the hard-switched counterparts. ZVT techniques become popular as it provides reduced voltage and current stresses with much reduced switching losses. Recent demands of high efficiency, high power density, low cost power supply in DPS motivates to design ZVT based AC-DC PFC converter with active and passive auxiliary circuits. The proposed converters can achieve high efficiency by reducing switching losses. It reduces voltage and current stresses, which leads to low cost and low power ratings components.

Besides increased efficiency, power expansion and reliability of AC-DC PFC converters employed in DPS are quite significant. These requirements can be accomplished

with the modularity approach. In addition, this approach also provides easier thermal management and maintainability. These requirements motivate to implement soft switching technique in modular system of ZVT based PFC converters to achieve high power density with improved efficiency.

1.8 Objectives

From the preceding discussion, the dissertation objectives may be streamlined as follows:

- To develop efficient PWM control technique for single-phase as well as for three-phase AC-DC PFC boost converters. A simple extended PWM technique overcomes the sluggish response of PFC converters and also reduces the voltage stress of PFC boost converter components during transient periods.
- To implement soft switching techniques in single-phase AC-DC PFC boost converter topology employing active auxiliary circuit and passive snubber circuit. This proposed technique will improve power density and efficiency for medium power applications. Another main objective is to eliminate the voltage and/or currents stresses of boost semiconductor switches as well as semiconductor switches of auxiliary circuit itself. The proposed converters can achieve better efficiency at side load range.
- To develop three-phase modular system of power rating 1.5 kW, 400 V, 100 kHz with reduced switching losses, reduced voltage and current stresses of semiconductor devices.

1.9 Dissertation structure

From the introduction, it can be observed that, several fundamental factors have been considered for the improvement of performance of front-end AC-DC PFC pre-regulator. To meet certain factors with respect to performance improvement requirement of PFC converter,

in this dissertation, different proficiencies have been investigated, which include dynamic response, different converter topologies to meet high power efficiency and modular approach solution to achieve power expandability for front end converters in distributed power system. In chapter 2, issues of PWM control in PFC converter have been discussed. For PFC stage, it is desirable to have better dynamic response for change in input voltage or load current. Due to the presence of low bandwidth filter in the voltage control loop, the system has slow response. Therefore, it is essential to find out the extended PWM switching technique to achieve fast dynamic response in PFC converters. A simple extended version of PWM technique is proposed for front-end AC-DC PFC converter for dynamic improvement. From the theoretical analysis, simulation and experimental verification, it is demonstrated that by applying two sided PWM technique for single-phase and three-phase PFC converters, a faster dynamic response can be obtained with primary achievement of nearly unity input power factor of converter.

High switching frequency of PFC circuit can result in smaller EMI filter size and boost inductor size. With higher switching frequency, switching loss is the major concern. To allow PFC circuit operating with switching frequency of 100 kHz, in chapter 3, PFC boost converter with passive snubber circuit has been discussed. Firstly, the boost converter with passive snubber circuit is discussed and its optimistic design is described. This topology can achieve higher efficiency by minimizing switching loss with voltage and current levels within the permissible limits. The performance evaluation of a single-phase PFC boost converter prototype developed in a laboratory has been analyzed and verified with a simulation results. Furthermore, to overcome the drawbacks of PFC converter with passive snubber circuit, a simple active snubber ZVT based PFC boost converter is proposed in chapter 4. An optimal design methodology for PFC boost converter with active snubber circuit has been presented.

Through the analysis and practical verification of single-phase circuit operation at full load condition and soft switching process of all semiconductor devices show that successful auxiliary resonant converter design relies on proper design of boost inductor and selection of snubber capacitor components. Furthermore, PFC boost converter with auxiliary snubber circuit exhibits small switching loss due to its soft switching capability and soft turn-off of boost diode. Therefore, it is able to operate at high switching frequency to achieve high efficiency while maintaining nearly sinusoidal input line current.

In chapter 5, a modular approach solution for front-end AC-DC PFC converter is proposed to gain the inherent advantages of modularity for DPS. To obtain the benefits of modular approach, three identical single-phase AC-DC PFC converters with soft-switching topologies have been demonstrated. Here, the single-phase converter circuits proposed in chapter 3 and chapter 4 are developed in modular approach and corresponding results have been presented. The experimental result show that, the modular approach is able to achieve the power expandability of 1.5 times the power developed by single-phase converters proposed in chapter 3 and chapter 4.

Last chapter 6 is dedicated to summary of overall thesis and future work on performance analysis and its improvement of front-end AC-DC PFC converters.

Chapter 2

Dynamic Performance Improvement of PFC Converter by Enhancement in PWM Technique

- **Introduction**
- **Design analysis of PFC feedback control system**
- **PWM control**
- **Operation of proposed two sided PWM technique**
- **Simulation and Experimental results**
- **Summary**

Introduction

Chapter 1 explained in detail the dynamic response problems occurring in PFC AC-DC converters. Due to input power variation in PFC converters, output load voltage contains a ripple voltage, whose frequency is twice the line frequency, which affects the input current waveform unless the voltage loop bandwidth is held below the half of the line frequency. This low bandwidth in voltage loop makes the active PFC converters to have sluggish transient response. This sluggish transient response problem is further compounded by large voltage overshoots and voltage drops enforcing additional stress on the PFC components, as well as on its downstream switch mode power supply load. It was pointed out that, simple way of obtaining good transient response is possible only by sacrificing the efficiency of the overall system by cascading the PFC pre-regulator with second DC-DC converter [29, 34].

In chapter 1, it is also discussed about the various methods proposed to ameliorate the dynamic response without permitting propagation of the ripple through voltage loop. Even though effective methods have been proposed for improvement of the voltage loop dynamics, the conventional low bandwidth design of the voltage loop is still predominant. This is mainly due to unresolved controller design and PWM technique issues. This motivated us to focus on the research of dynamic improvement of converters employed for PFC applications.

Following above discussion, in this chapter investigation of improvement in the dynamic response of a AC-DC PFC boost converter with novel PWM strategy is carried out. This novel PWM control strategy for PFC applications has been published in our publications [123, 124]. The advantages of the proposed scheme are:

(a) The bandwidth of voltage loop can be still maintained small to avoid ripple frequency

propagation through the voltage loop and hence eliminates the distortion in input current.

(b) This novel PWM strategy can be applied to three-phase PFC converter in modular system, hence exhibiting the higher power expandability.

(c) Improves the audio susceptibility of the converter system.

The high quality of input current in AC-DC PFC converter is often achieved by a current mode PFC controller Integrated Chip's (IC) such as UC3854, UC3853, AN-1077, IR1150, etc. As described in section 1.3.1 of chapter 1, these PFC controllers essentially have current loop, voltage loop and feed-forward loop to achieve unity input PF in PFC pre-regulator system. The important conception of each loop is discussed in detail and this outlines the importance and significance of this study.

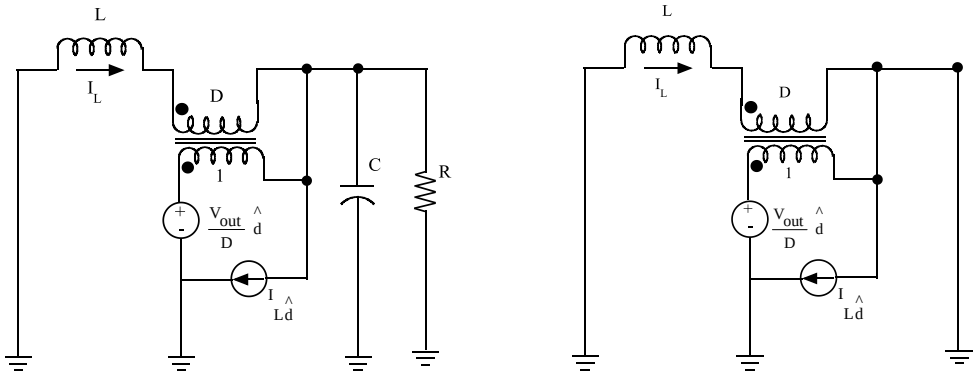
2.1 Design analysis for PFC feedback control system

2.1.1 Current Loop Compensator

Excellent references exist on current loop design [32, 125-128]. The objective of this loop is to track a reference sine waveform whose frequency is twice the line frequency. This reference signal has a high *dv/dt* around the zero crossings of the line. Therefore the loop needs gain at frequencies corresponding to the higher order Fourier coefficients needed to recreate the reference waveform. This implies high bandwidth for the current loop. A bandwidth of 10 kHz can be considered for this type of PFC application which is usually adequate for 50 Hz or 60 Hz line frequency [32, 128]. In order to design a proper current loop compensator, the equivalent model of the boost converter is analyzed. By applying three terminals PWM switch model [32, 128] to the boost converter, the small signal equivalent circuit of the boost converter shown in Fig. 2.1 is obtained. The power stage small signal duty to current transfer function of the exact model of boost PFC converter shown in Fig. 2.1(a) is

$$G_{id}(s) = \frac{2\ V_0\ R_{SENSE}}{R\ (1-D)^2} \frac{1+\left(\frac{s}{\omega_z}\right)}{1+\frac{s}{\omega_0 Q}+\left(\frac{s}{\omega_0}\right)^2} \tag{2.1}$$

where D is the duty cycle and $\omega_z = \frac{2}{R\,C}$, $\omega_0 = \frac{(1-D)}{\sqrt{LC}}$, $Q = R(1-D)\sqrt{C/L}$.



(a) Exact model (b) Simplified equivalent model at high frequency

Fig. 2.1 Model of boost PFC converter using PWM switch model

The 'R_{SENSE}' term is not seen directly from the Fig. 2.1(a) and (b) but is included here since it relates the actual inductor current to the signal at the current loop error amplifier. In the equation (2.1), it can be observed that, the power converter stage DC gain, poles and zeroes are moving as the instantaneous line voltage changes (D changes with the line voltage). It is well known that, the output capacitor in a PFC converter is large enough in order to meet the hold-up time requirement and to minimize the 100 or 120 Hz ripple. Fig. 2.1(b) shows the simplified form of the small signal equivalent circuit of the boost converter, which is obtained by assuming the large output capacitor to meet holdup-time requirement and less switching frequency ripple (high switching frequency) [32]. This is essentially a reasonable approximation for realistic circuit design. The simplified form of current loop transfer function for the equivalent circuit shown in Fig. 2.1(b) is given by,

$$G_{id}^{s}(s) = \frac{V_0 \; R_{SENSE}}{s \; L \; V_{SE}} \tag{2.2}$$

where V_{SE} is the triangular voltage peak to peak.

The bode plots of exact model of equation (2.1) and simplified model of equation (2.2) are plotted in Fig. 2.2 for selected instantaneous line voltages (including high line and low line voltages). It can be observed that although the power-stage DC gain, poles and zero are changing with the line, the high-frequency portions of the responses are converging to the response of simplified model as shown in Fig. 2.2. Hence, the simplified model approach is used for designing current control loop as it is easier and details obtained from high frequency equivalent circuit is adequate to design the current loop.

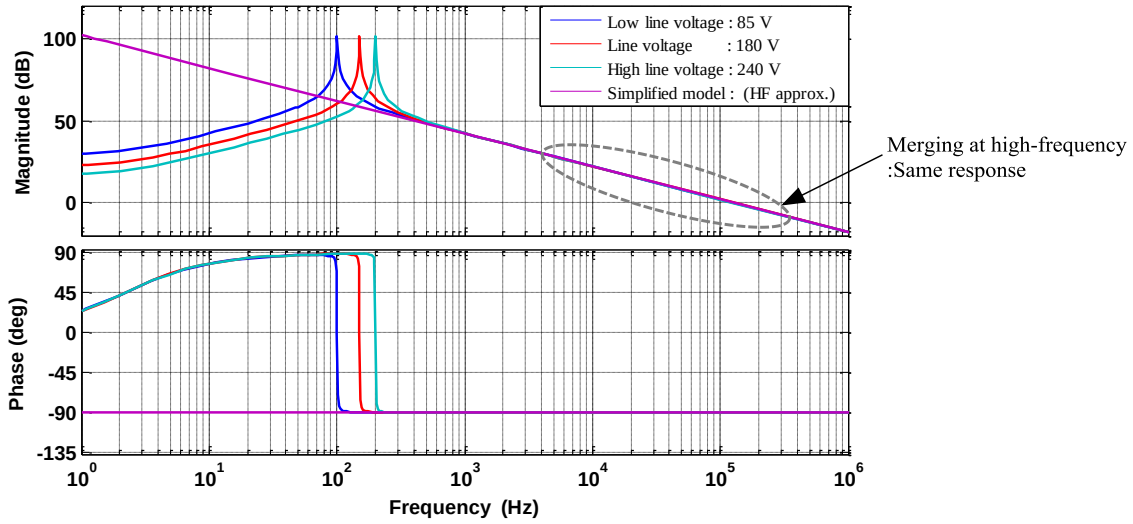


Fig. 2.2 Magnitude and phase response of exact model and simplified model of boost PWM switch

In ACMC method, current control loop is essentially a current amplifier with a two pole, single zero compensation network and this is shown in Fig. 2.3. The zero is placed to achieve the desired phase margin and the pole is placed at or after one-half of the switching frequency to reduce the switching noise of the sensed inductor current [129].

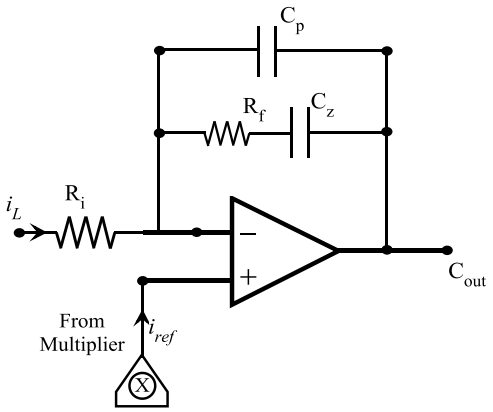


Fig. 2.3 Circuit diagram of current loop error

The transfer function of current loop error amplifier shown in Fig. 2.3 is given by,

$$A_v = \frac{1 + s R_f C_z}{s R_i (C_p + C_z)\left[(1 + s R_f)\left\{\frac{C_p C_z}{C_p + C_z}\right\}\right]} \tag{2.3}$$

here, R_i and R_f are input and feedback resistors of current loop amplifier.

C_p and C_z capacitances to have pole and zero of transfer function.

C_{out} is the output of current loop error amplifier.

i_L and i_{ref} are measured inductor and derived sinusoidal currents respectively.

2.1.2 Voltage feedforward loop compensation

The RMS voltage feedforward control is performed in many PFC IC controller circuits in order to achieve a constant gain in voltage loop over varying input voltages and to provide input voltage correction to the line current [32, 102, 130]. It can be observed in Fig. 1.5 of chapter 1, that the required average value of the rectified AC input is obtained by a two pole low pass filtering circuit, i.e. the output of block 'C' is squared before being used as a divider term in deriving the reference current signal i_{ref}. The addition of this term in the multiplier does not warrant a change in output of a voltage compensator for change in the input voltage for a given load. In fact, the output of a voltage compensator becomes proportional to the output power for

normal operating range [126, 130]. A broad sense of two pole feedforward low-pass filter suitable for PFC circuit is shown in Fig. 2.4. The key advantage of this feeforward technique is constant loop gain and constant peak power over the specified input range of voltage. In a PFC feedback system of Fig. 1.5, of chapter 1, the output of a multiplier is the reference current signal and it is given by,

$$i_{ref} = \frac{(A)(B)}{(C)^2} \tag{2.4}$$

where A= $K_v v_{in}$, (K_v: Input voltage gain),

B= v_{vc}, (v_{vc}: Output voltage signal of voltage compensator), and

C=$K_{ff} V_{in\_rms}$, (K_{ff}: gain of input voltage feedforward signal)

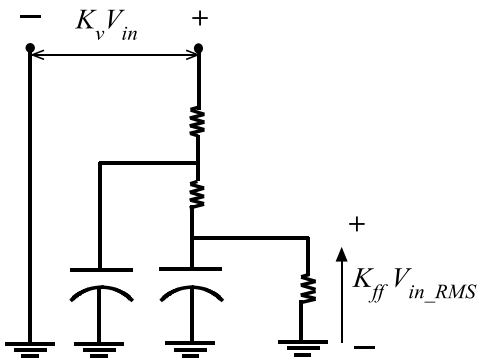


Fig. 2.4 Second order low-pass filter in feedforward loop

Since both the rectified output voltage and boost converter output voltage contain 2nd harmonic component [130], there exists a ripple in B and C components of Fig. 1.5 of chapter 1. Hence, ripples in components B and C are injected into the current reference i_{ref}. From equation (2.4), it can be derived that,

$$\frac{\Delta i_{ref}}{i_{ref}} = \frac{\Delta B}{B} - 2\frac{\Delta C}{C} \tag{2.4a}$$

here, ΔB and ΔC are unknown, the worst case occurs when they have a phase shift of 180^0. Considering absolute value of equation (2.4a), we obtain,

$$\left|\frac{\Delta i_{ref}}{i_{ref}}\right|_{worst} = \left|\frac{\Delta B}{B}\right| + \left|2\frac{\Delta C}{C}\right| \tag{2.4b}$$

From the above equation (2.4b), it can be concluded that, for a system looking to achieve 1.5% THD, it is typical to allow the feedforward circuit 'C' to contribute less than 0.5% distortion and the total distortion of 'B' should be smaller than 0.5% [131]. The selection of cut-off frequency of the feedforward low-pass filter and voltage compensator gain should be based on this criterion.

2.1.3 Voltage loop compensation

The voltage control loop is very essential in feedback system of PFC converters to achieve a proper stability of the system. But there are some trade-offs in designing voltage control loop that are particular to AC-DC PFC converter application. The key requirement of power balance, on the line frequency time scale, necessitates that the feedback voltage loop's bandwidth must be less than the half of the line frequency. If not, the voltage loop will distort the input line current in order to regulate the output voltage [32, 130]. This makes a trade-off between input PF and transient response.

Generally, a transconductance type amplifier is employed in voltage loop compensator which is compensated by connecting impedance between the amplifier's output and ground. Usually, the output current of amplifier is not sufficient to drive a resistive load unless the desired DC gain is very high [130]. This implies capacitive loading and hence the integral gain. In such cases, the integral compensation can be used. The transconductance amplifier of voltage loop compensator (voltage error amplifier) is shown in Fig. 2.5. Its transfer function is given by,

$$A_v = g_m \frac{1 + s R C_1}{s(C_1 + C_2)\left(1 + s R\left[\frac{C_1 C_2}{C_1 + C_2}\right]\right)} \tag{2.5}$$

where, g_m is the transconductance of the voltage error amplifier. R, R_1, R_2, C_1 and C_2 are the elements of transconductance amplifier circuit.

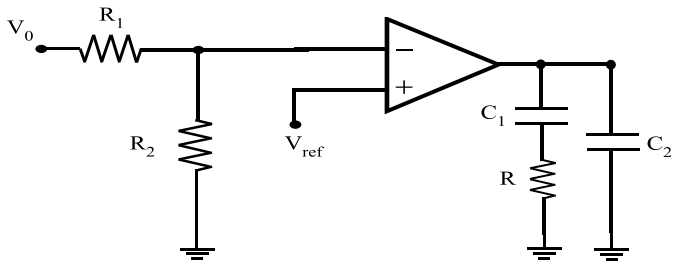


Fig. 2.5 Voltage loop error amplifier configuration in PFC feedback system

In order to analyze voltage control loop in PFC applications, the basic low frequency model of the output of the power stage and the current feedback loop have to be considered. The power stage and the current feedback loop compose the voltage controlled current source driving the output capacitor connected in parallel with load resistor. This arrangement essentially forms an integrator and it has gain characteristics which rolls off at a constant 20dB per decade rate with increase in frequency. The low frequency small signal equivalent circuit for the power stage with the current loop closed [128, 130] is shown in Fig. 2.6.

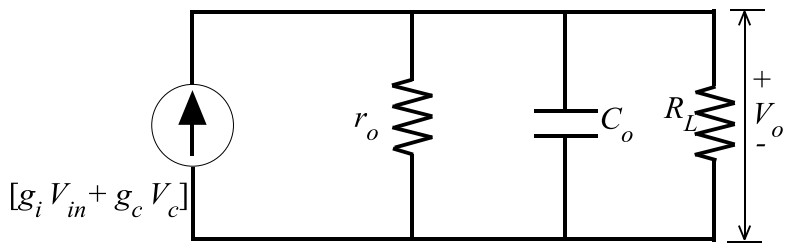


Fig. 2.6 Small signal model of outer voltage loop for constant power loads, r_0=R_L

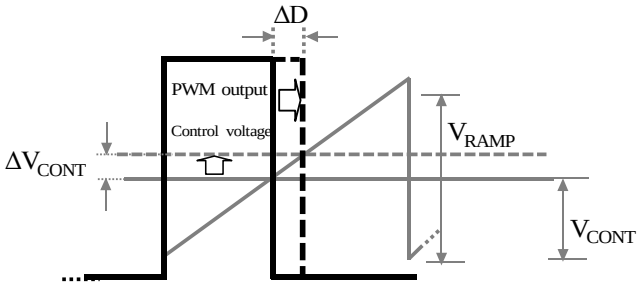
In above Fig. 2.6, $g_c = K\frac{V_{in\_RMS}^2}{V_0}$, $g_i = K^2\frac{V_{in\_RMS}\ V_c}{V_0}$, and $r_0 = \frac{V_0}{I_{out}}$, for the constant power load case, $R_L = -\frac{V_o}{I_{out}}$. From the small signal model, the control to output voltage transfer function can be obtained as:

$$G_V = \frac{\tilde{V}_0}{\tilde{V}_c} = \frac{g_c}{C_0\, s} \tag{2.6}$$

For constant power applications, a phase margin of 45^0 [131] for voltage compensation is employed.

2.2 PWM control

PWM control plays a vital role in high switching operation of converters. The output of the feedback controller (output of current controller) is applied to one of the inputs of the PWM modulator comparator. On the other input of this comparator, a saw-tooth voltage ramp of specified frequency is applied. Since the feedback signal is connected to the inverting input of the error-amplifier, if the output is below the set regulation value, the output of error amplifier goes high.



Pulse Width Modulator Gain
(Unit - V^{-1})

$$D = \frac{V_{CONT}}{V_{RAMP}}$$

$$\Delta D = \frac{\Delta V_{CONT}}{V_{RAMP}}$$

$$G_{PWM} = \frac{\Delta D}{V_{CONT}} = \frac{1}{V_{RAMP}}$$

Fig. 2.7 Gain of pulse width modulator

This causes the PWM to increase pulse width (hence duty cycle) and thus makes the output voltage to rise. Similarly, if the output of the converter whose value is to be regulated

goes above its set value, the error amplifier output goes low, causing the duty cycle to decrease. The generation of pulse from this PWM to drive the switch in converters is shown in Fig. 2.7. As mentioned previously, the output of the PWM modulator stage is a duty cycle and its input is the control voltage or the output of the error amplifier. So, the gain of this PWM stage is not a dimensionless quantity, but has units of 1/V. From Fig. 2.7, it can be obtained that; the gain of PWM modulator is equal to $1/V_{RAMP}$. Where V_{RAMP} is peak to peak amplitude of ramp saw tooth signal.

2.2.1 Issues surrounding PWM control

As described in previous section 2.1, it is well known that, active PFC AC-DC converters always use closed-loop negative feedback systems with PWM technique to achieve objectives of line and load regulation. Most PWM controllers use a clock-edge to set one edge of the PWM signal and feed-back to set the other edge of the PWM signal. But, one edge available for control remains unused. This direct duty cycle control has disadvantages like slow response to sudden input changes, poor audio susceptibility and poor open loop line regulation [132-134]. In both current mode and voltage mode control of PWM is restricted and it uses one of two edges available for control [15, 133, 134]. Controller with hysteresis based on power converters makes use of both edges but the switching frequency is allowed to vary and control scheme is sensitive to commutation noises [24, 135-137]. Variation in the switching frequency makes it difficult to filter the ripple components in the input and output waveforms of the converters [138]. Therefore, it is essential to have constant switching frequency for easy design of input EMI filter and magnetic components with primary objective to obtain unity power factor in power supplies. Saw-tooth ramp generator is required in PFC converters to stabilize fixed frequency PWM control. Many commercial PWM controller ICs are available with/without saw-tooth generator.

ICs with a saw-tooth generator are limited in switching frequency and ICs that do not include the saw-tooth ramp generator are available that operate at much higher switching frequency. Still there exists a challenging task for power supply design engineers in generation of the high frequency saw-tooth ramp with the fast reset. Employing two sided PWM technique improves the dynamic response of the power factor correction converter and it is most suitable for high frequency applications [133, 134].

2.2.2 Comparison of PWM and two sided PWM techniques

In broad sense, PWM-scheme is classified by whether one or both edges are modulated. The latter requires a double-sided or triangular carrier signal (with equal slope) to generate PWM pulses. Fig. 2.8 shows the difference between single-sided (conventional PWM) and two sided latch PWM modulation techniques. In double sided modulation technique, the pulse transition from high to low is occurring at 't_1' which is intersection of positive ramp of triangle signal and control signal, pulse transition from low to high is happening at intersection of negative ramp of triangle signal and control signal. In case of conventional PWM technique, pulse transition from high to low is occurring at 't_2' the intersection of positive ramp of saw-tooth signal and control signal, transition from low to high is taking place at the instant of end period of saw-tooth signal. It can be observed that, the same number of output transitions occurs per period T in two sided PWM technique and that of single sided PWM technique, but the signal is sampled twice in two sided PWM technique. Also, the carrier slew-rate is doubled in two sided PWM technique so the requirement for f_c/f is halved. In Fig 2.8, it can be observed that, over a period of cycle from nT to $(n+1)\,T$, the transition of pulse from high to low for two sided PWM technique is occurring at instant t_1, and transition from high to low for single sided PWM technique is happening at $t=t_2$, here $t_1<t_2$, hence the quick response is achieved by the two sided PWM technique rather than

single sided PWM technique. This response is mainly depending on the slope, i,e peak value of carrier signal. In two sided PWM technique, the ramp amplitude is chosen to meet the equal ramp slope criteria for optimal current mode to achieve better dynamic performance of the system. Thus the two sided PWM method stabilizes any transient responses on the load or input line quicker than conventional PWM method for properly designed control loops [134]. This novel approach motivated us to employ two sided PWM scheme to AC-DC PFC boost converter.

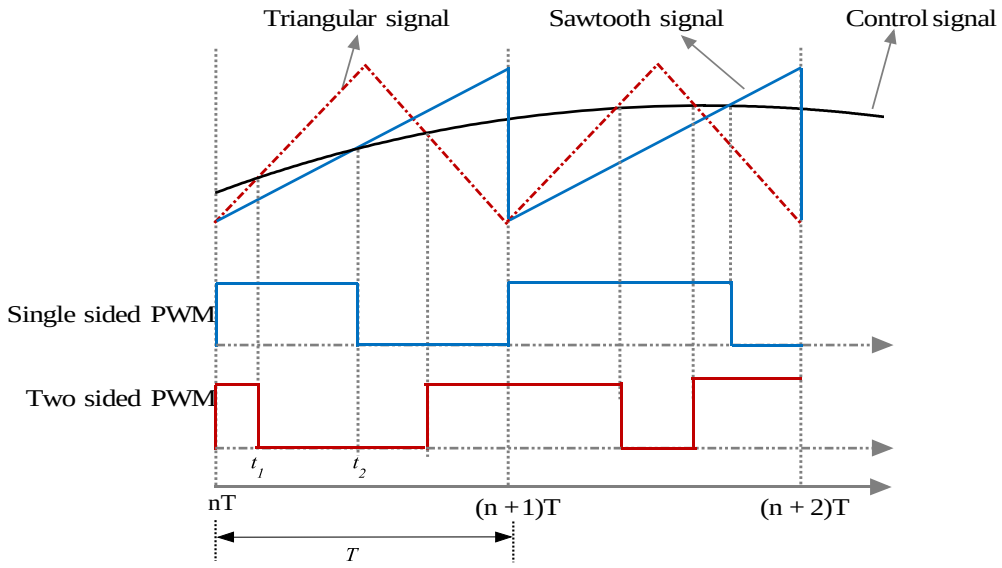


Fig. 2.8 Comparison of two sided and single sided PWM techniques

2.3 Operation of proposed two sided PWM control

Fig. 2.9 shows a sensor-less current mode control implementation in inner current mode control of two sided active PFC AC-DC boost converter. This scheme achieves modulation of both edges while maintaining fully latched operation. In this PWM scheme two comparators are used instead of one to set and to reset the switch. One comparator is used for the comparison between the feedback signal s*ign* and ramp to set the switch while another comparison between an offset feedback signal and ramp to reset the switch. The ramp is not a saw-tooth, which is hard to generate at high frequencies [134], but a triangular ramp wave with equal rising and

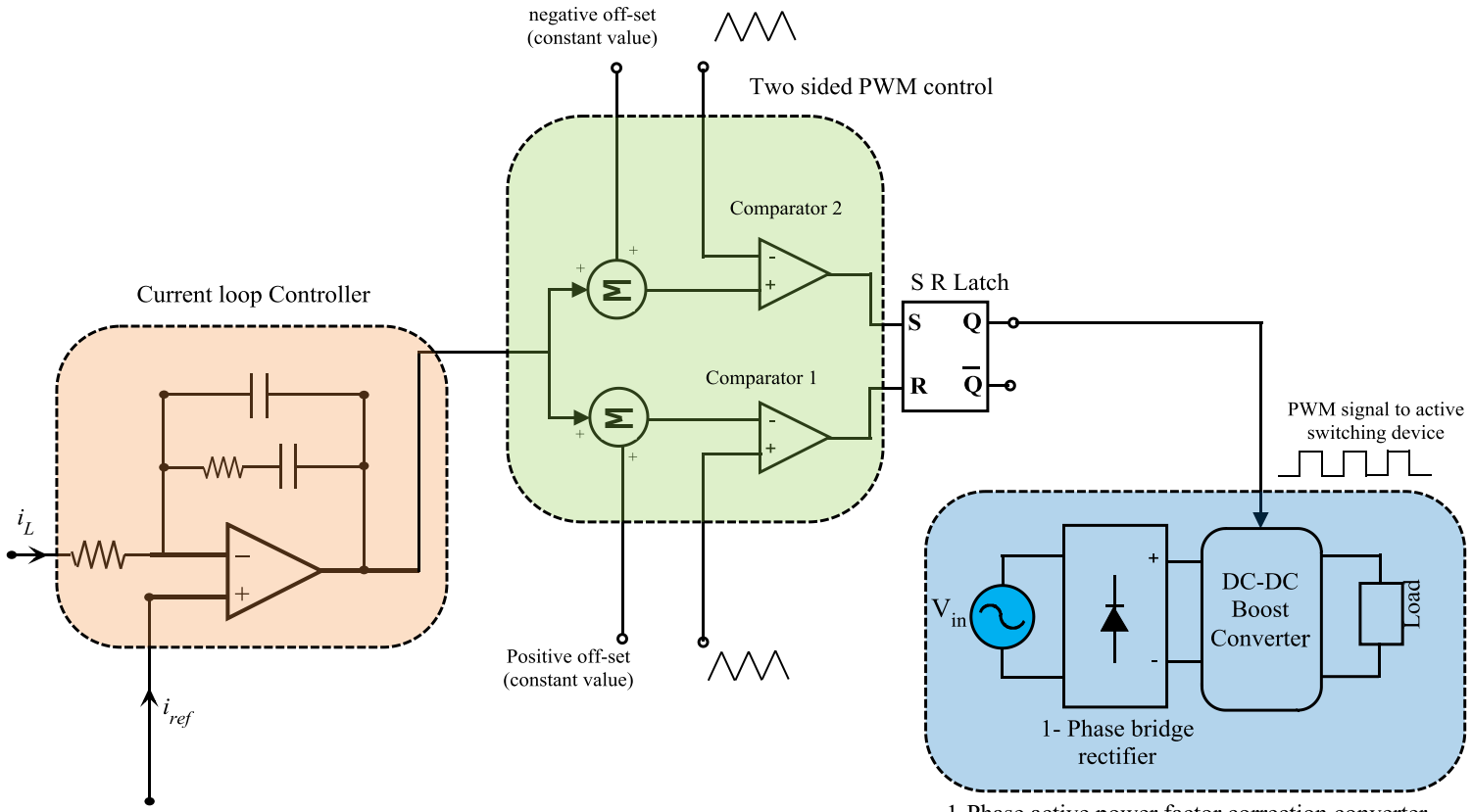


Fig. 2.9 Two sided latched PWM schematic for PFC AC-DC boost converter

falling slopes is used to stabilize the duty ratio of the switch and to set the switching frequency. The ramp amplitude is chosen to meet the equal ramp slope criteria for optimal current mode control.

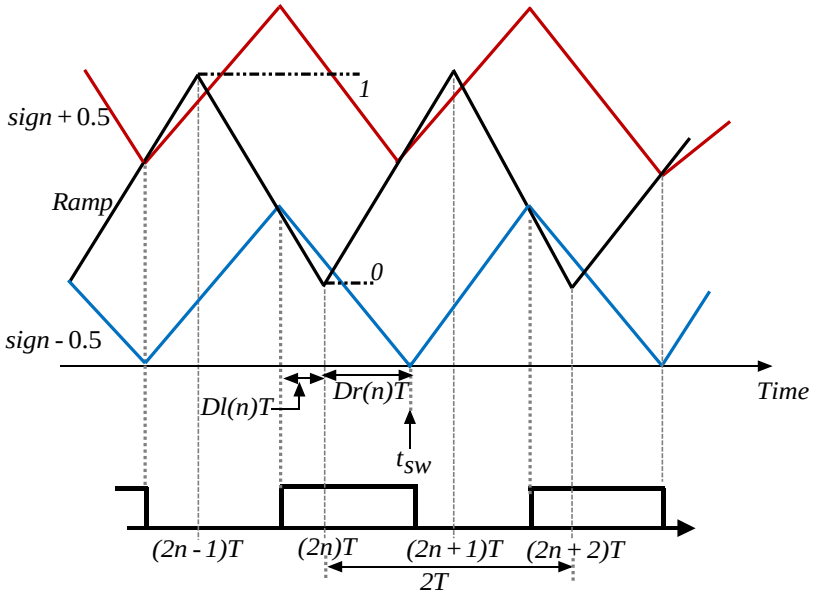


Fig. 2.10 Theoretical timing diagram for proposed two sided latched PWM technique

Fig. 2.10 shows the timing diagram of the signals in the proposed two sided PWM scheme for active PFC AC-DC converter. There is a triangular ramp with equal rising and falling slopes. This ramp is compared to the feedback signal with two appropriate offsets. The resulting PWM signal is shown at the bottom of the Fig. 2.10. Note that the delay between consecutive rising and falling edges is *T*. The ramp slope is chosen to be equal to the feedback signal at duty ratio of half. This is a design choice and depends on the nominal duty ratio.

2.3.1 Time domain analysis

By applying the switch set and reset criteria for a current mode control of two sided PWM technique shown in Fig. 2.9 and assuming that the converter is operating in the CCM of

operation, the following equations can be obtained. The mathematical analysis is similar to the method used in [133, 134].

$$sign((2n-dl(n))T)-\tfrac{1}{2}=dl(n) \tag{2.7}$$

$$sign((2n-dr(n))T)+\tfrac{1}{2}=dr(n) \tag{2.8}$$

The signal *'Sign'* is control signal which is output of a current controller. In other words, the signal *'Sign'* is obtained as the integral of the difference of the reference signal and the switching signal waveform. However, the gain of the integral is obtained using the equal slope criteria when the reference signal is half the input voltage.

$$\frac{\frac{Vin}{2}}{T_i}=\frac{1}{T}=>T_i=\frac{V_{in}}{2}T \tag{2.9}$$

where, 1/T is the ramp slope for a ramp signal of unit amplitude and V_{in} is the input voltage to boost converter. Let us define, the nominal duty ratio of the converter in steady state be *'dnom'*. This term is essentially used to eliminate *'V_{in}'* and *'V_{ref}'* from the duty ratio equations.

$$sign((2n+dr(n))T)=sign((2n-dl(n))T)+\frac{(V_r-V_{in})}{\frac{V_{in}}{2}T}[dl(n)\_dr(n)]T \tag{2.10}$$

also,

$$sign((2n+dr(n))T)=sign((2n-dl(n))T)+2(dnom-1)[dl(n)+dr(n)] \tag{2.11}$$

The relationship of signal *'sign'* between present time step and the next time step is as follows,

$$sign((2n+1)-dl(n+1))T)=sign((2n+dr(n))T)+\frac{V_r}{\frac{V_{in}}{2}T}[2-dr(n)-dl(n+1)]T \tag{2.12}$$

$$sign((2n+1)-dl(n+1))T)=sign((2n+dr(n))T)+2\,dnom[2-dr(n)-dl(n+1)] \tag{2.13}$$

By substituting the nominal duty ratio in the above two equations, we get,

$$dr(n)-1/2=dl(n)+1/2-2(1-dnom)(dl(n)+dr(n)) \tag{2.14}$$

$$dl(n+1)+1/2=dr(n)-1/2+2\ dnom(2-(dr(n)-dl(n+1))) \tag{2.15}$$

By simplifying equations (2.14) and (2.15) and by considering reference and input voltage quantities, right duty ratio '*dr'* and left duty ratio *'dl'* can be obtained as [134],

$$dr = dnom + \frac{1}{2}(1-2\,dnom)^2 \tag{2.16}$$

and $$dl = dnom - \frac{1}{2}(1-2\,dnom)^2 \tag{2.17}$$

From the previous analysis and simplified expressions of *'dl'* and *'dr'*, it can be summarized that, the nominal duty ratio *'dnom'* is always equal to the average of the left and right duty ratios. The nominal duty ratio *dnom = 0.5*, when both left and right duty ratios are equal. At all points except at *dnom=0.5*, the right duty ratio is greater than the left duty ratio. This causes problem at extreme values when the left duty ratio approaches zero and the right duty ratio approaches unity.

The value of nominal duty ratio for the two extreme cases is computed as follows.

$$dr = 1 = dnom - \frac{1}{2}(1-2\,dnom)^2 \tag{2.18}$$

or $$dnom = \frac{1+\sqrt{5}}{4} = 0.809 \tag{2.19}$$

$$dl = 0 = dnom - \frac{1}{2}(1-2\,dnom)^2 \tag{2.20}$$

or $$dnom = \frac{3-\sqrt{5}}{4} = 0.191 \tag{2.21}$$

It is to be noted that, this stability bound is not fundamental to this approach, however it is the result of meeting the equal slope criteria at *dnom=0.5*.

2.3.2 Design procedure of single-phase AC-DC PFC boost converter

As noted in section 1.4.1 of chapter 1, the boost converter topology operating in CCM is most popular for medium and high power AC-DC PFC applications. Hence, the conventional

boost converter operating in CCM is considered to employ two sided PWM technique to improve the transient response of the AC-DC PFC converter. Table 2.1 shows the design basic specifications that will govern the main attributes of the circuit components. However, the design procedure for the PFC boost converter elements is same for both the single sided PWM and two sided PWM control techniques.

Table 2.1 Specification of PFC AC-DC boost converter

Rated Output Power	P_{out} =500 W
Universal Input Voltage Range	V_{in}= 85 V to 265 V (rms)
Line Frequency	f_{line} = 47 – 63 Hz
Nominal Regulated Output Voltage	V_o = 400 V
Switching Frequency	f_s = 100 kHz
Target Efficiency	$\eta \geq 95\%$
Hold-Up Time	t_{hold_up} = 20 ms

Following are the standard design equations of the main components of the PFC AC-DC boost converter; the procedure is reported in [130, 139-141]. There are many other factors involved in the design process of PFC boost converter. However, the following equations are intended to provide a frame work for the design.

$$P_{in(\max)} = \frac{P_{out(\max)}}{\eta_{\min}} = \frac{500}{0.95} = 526.32\ W \tag{5.22}$$

$$I_{in\_RMS(\max)} = \frac{P_{in(\max)}}{V_{in\_RMS(\min)}} = \frac{526.32}{85} = 6.2\ A \tag{2.23}$$

$$I_{in\_peak(\max)} = \sqrt{2}\, I_{in\_RMS(\max)} = \sqrt{2}\ (6.2) = 8.77\ A \tag{2.24}$$

2.3.2.1 Boost Inductor

Typically the boost inductor to be operated in CCM is designed with the ripple current 20% of the peak current [130, 140, 142].

$$V_{in\_peak(\min)} = \sqrt{2}V_{in\_RMS(\min)} = \sqrt{2}\ (85) = 120.21V \tag{2.25}$$

Maximum value of transistor duty cycle,

$$D_{peak} = 1 - \frac{V_{in\_peak(\min)}}{V_o} = 1 - \frac{120.21}{400} = 0.7 \tag{2.26}$$

Inductor ripple current, $\Delta I_L = (0.20) I_{in\_peak(\max)} = (0.20)8.77 = 1.75A$ (2.27)

$$\Delta I_{L\_peak(\max)} = I_{in\_peak(\max)} + \frac{\Delta I_L}{2} = 8.77 + \frac{1.75}{2} = 9.64A \tag{2.28}$$

$$L_{\min} = \frac{V_{in\_peak(\min)}\, D_{peak}}{f_s\,(\Delta I_L)} = \frac{120.21(0.7)}{100000(1.75)} = 480\,\mu H\ (\min imum) \tag{2.29}$$

2.3.2.2 Output capacitor

In power supply design, the value of the output capacitor is computed based on the following [102, 130]; 1) Amount of the tolerable output ripple voltage by the capacitor and 2) Holdup time of the power supply. Hence, the determination of output capacitor value is mainly depending on the output voltage ripple allowed and on the holdup time in brownout conditions.

2.3.2.3 Output voltage ripple limit

The criterion for selection of output capacitor is the amount of tolerable ripple in the out voltage,

hence, $C_0 \geq \dfrac{P_{out}/V_0}{2\pi\,(f_{line})(\%\Delta V_{0\_ripplie})} = \dfrac{500/400}{2\pi\,(50)(0.03)(400)} = 331.57\,\mu F$ (2.30)

where ΔV_{0_ripple} is the desired peak to peak output voltage ripple and 30% is considered in this design. De-rating the output capacitor value by 20% for tolerance in order to guarantee minimum capacitance requirement is satisfied.

$$C_0 \geq \frac{C_{0(\min)}}{(1-\Delta C_{tol})} = \frac{331.57\,\mu}{(1-0.2)} \tag{2.31}$$

$\therefore C_0 \geq 414.46\ \mu F$

2.3.2.4 Holdup time requirement

Typical power supplies in distributed power system employ a PWM stage after PFC stage to provide isolated DC output for end user. Hence, some applications, especially computing, have the holdup time requirement. This means that, the power supply must be able to sustain its load output for short duration. 20 *ms* of holdup time is an accepted standard in the industry. Hence, the minimum capacitance required for a 20 *ms* holdup time can be calculated as,

$$C_0 \geq \frac{2(P_{out})t_{holup}}{(V_o^2 - V_{0\_\min}^2)} = \frac{2(500)20(10^{-03})}{(400^2 - 250^2)} \tag{2.32}$$

$\therefore C_0 \geq 205.12\,\mu F$

where the t_{holdup} is the minimum holdup time and V_{o_min} is the minimum output voltage that the load will operate. The calculations of equations (2.31) and (2.32) yield an output capacitor C_0 to a minimum value of 414.46 μF. To meet minimum holdup time and output voltage ripple requirements, the higher standard capacitance value of 450 μF, *600 V* is selected.

2.4 Simulation and Experimental Results

2.4.1 Single phase AC-DC PFC boost converter

Based on the theoretical analysis described in above sections, the two sided PWM technique for improvement in dynamic response of AC-DC PFC converter is evaluated. A 500 W, 400 V and 100 kHz switching frequency, universal input single-phase AC-DC PFC boost converter prototype is designed and implemented with a feedback PFC controller IC-UC3854. A separate auxiliary circuit is developed to generate triangular waveform to achieve two sided PWM technique successfully. Besides, the conventional AC-DC PFC converter circuit using

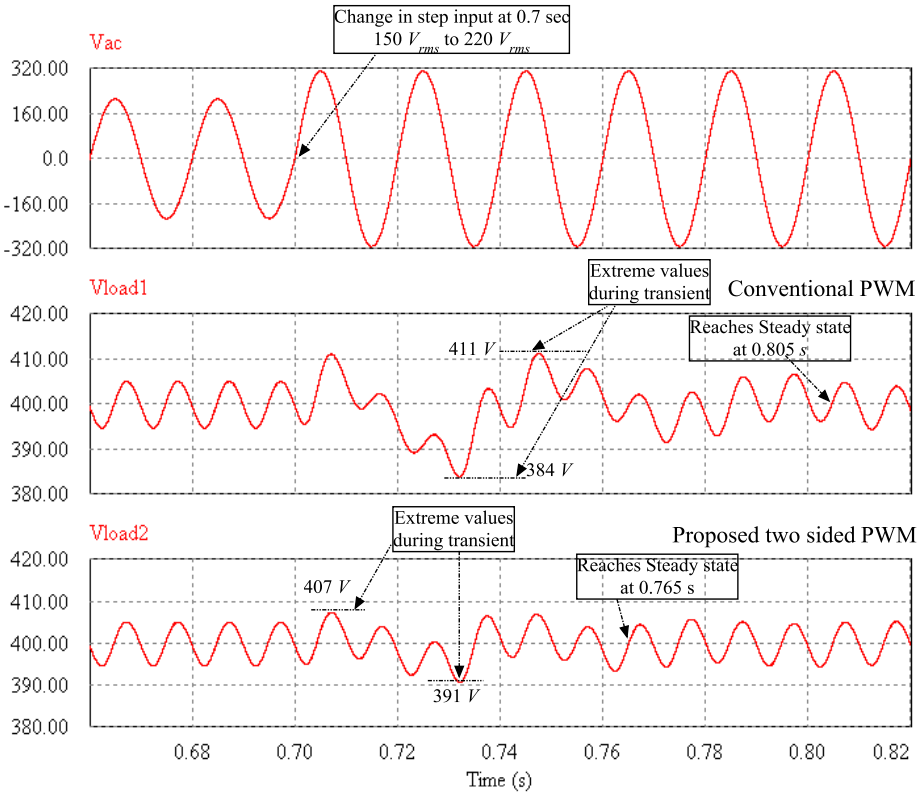
identical devices and ACMC was built with same PFC controller IC with single sided (regular) PWM technique as the benchmark. All the converter circuit parameters are listed in Table. 2.2.

The configuration of the proposed AC-DC PFC converter is developed in association with its sophisticated feedback system and simulated in Power-Sim (PSIM) Power Electronics and Drives simulation package. The purpose of this simulation is to verify the control algorithms, design the controller parameters, and to verify static and dynamic performances of the proposed system with conventional system.

Table 2.2 Components employed in the proposed

Component	Value/Model	
	Simulation	**Experimental**
Bridge rectifier	Ideal	DFB2060 (Fairchild SC)
MOSFET	Ideal	IRFP460 (International Rectifier)
Fast-recovery Diode	Ideal	RHRP3060 (Fairchild SC)
Output capacitor	450 μF, 600 V	UNLYTIC make– (UL30-series)
Boost inductor	1 mH	Sendust toroid, part No. CS468125 and 32 single layer turns of 16 AWG
Low line filter inductor (L_{in})	5.6 μH	5.6 μH

Fig. 2.11 shows the steady-state and transient response of simulation results of proposed two sided PWM AC-DC PFC converter as well as conventional PWM AC-DC PFC converter. Fig. 2.11(a) and Fig. 2.11(b) show simulated input voltage, input current and output voltage waveforms of proposed converter and conventional converter for a step change in voltage from 150 V_{RMS} to 220 V_{RMS} and 220 V_{RMS} to 150 V_{RMS} respectively. The step change in input voltage from 150 V_{RMS} to 220 V_{RMS} and vice versa is occurring at instant 0.7 sec. In both cases (change in voltage from high to low and low to high, Fig. 2.11(a) and Fig. 2.11(b)), the two sided PWM PFC converter recovers its steady state at around 0.765 sec and that of conventional PWM PFC



(a)

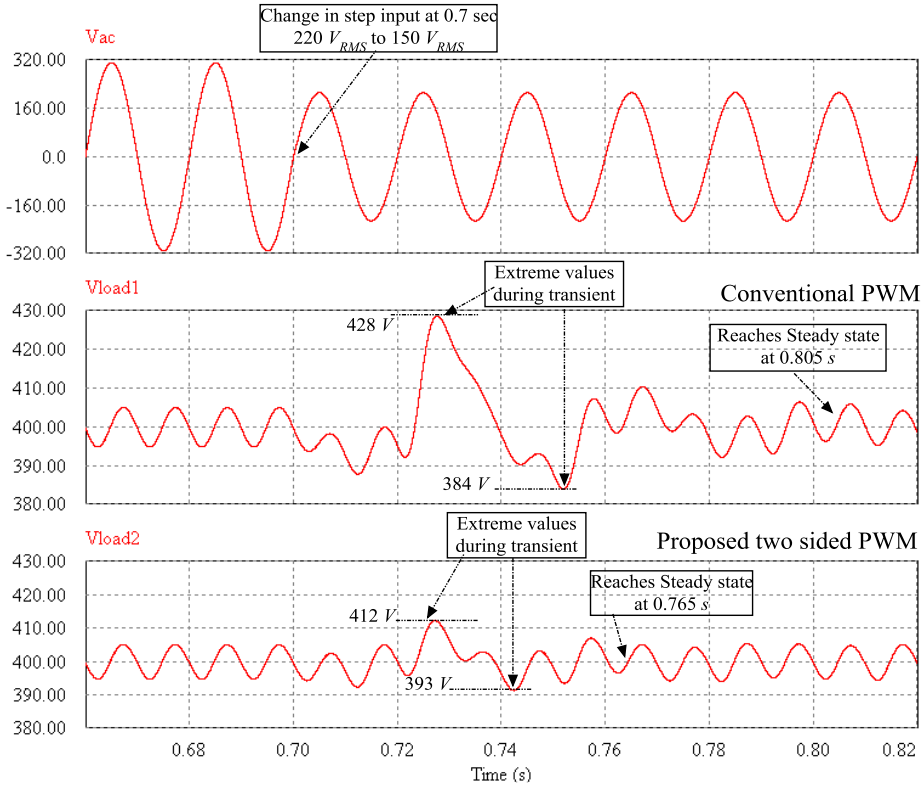
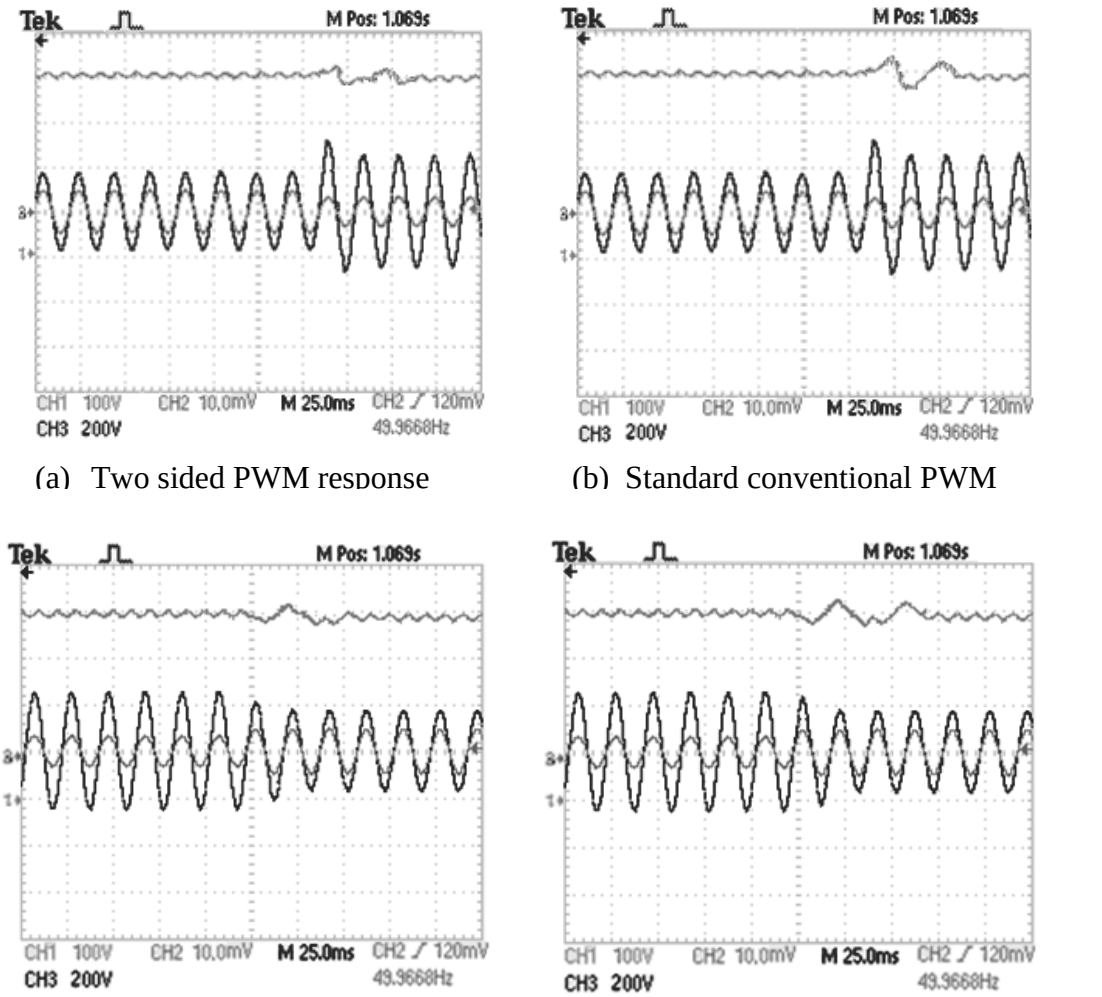


Fig. 2.11 Comparison of dynamic response of output voltage for a step change in input voltage
(a) 150 V_{RMS} to 220 V_{RMS} (b) 220 V_{RMS} to 150 V_{RMS}

converter is recovering at 0.805 sec. However, the overshoot and under shoot voltage stresses on devices and output capacitor are more in case of conventional PWM PFC converter and these limits are noted and marked in Fig. 2.11. It can be seen from these figures that, the proposed two sided PWM technique increases the dynamic response at least by 5% under worst case condition for a large change in input voltage.

The experimental results of dynamic response due to step change in input voltage from 150 V_{RMS} to 220 V_{RMS} and vice versa have been observed, recorded by Digital Storage Oscilloscope and are shown in Fig. 2.12. The identical response with respect to simulation results are verified during step change in the input voltage. In experimental results, as soon as there is change in the input voltage, the peak voltage (surge) spike appears on input voltage in both cases where same response has not occurred in simulation results. This is because the discrete transition simulators like '*PSIM'* are incapable of showing parasitic effect processes such as surge current or voltage. It can also be observed that, the two sided PWM technique provides quick response in comparison with conventional PWM technique employed in single-phase AC-DC PFC converter.

The performance of transient response for load change is also obtained by simulation of both the converters. The output voltage waveform in transient state, in which load is changed from full load to 50% of full load and vice versa for both the converters are shown in Fig. 2.13. When the load is changed at time t = 0.8 sec, in both cases, (a) 50% to full load and (b) full load to 50% load change, the output voltage overshoots to 388 V and 410 V respectively. After about 20 ms, the output voltage recovers to its stable state in case of two sided PWM technique. However, the overshoot and undershoot of output voltage just after the load change are almost same but the output voltage is in two sided technique recovers back to its stable state quickly.



(a) Two sided PWM response (b) Standard conventional PWM

(c) Two sided PWM response (d) Standard conventional PWM response

Fig. 2.12 Experimentally obtained dynamic response of conventional and two sided PWM techniques for an input change from (a) and (b) 150 V_{RMS} to 220 V_{RMS} (c) and (d) 220 V_{RMS} to 150 V_{RMS} *Scale: Ch1: 100 V/div, Ch2:3: 200 V/div, Ch2: 2 A/div.*

The percentage of improvement with respect to load change transient output voltage is verified by experimental results shown in Fig. 2.14. Fig. 2.14 shows the comparison of output voltage dynamic response to a load step from 0.625 A to 1.25 A for both control schemes. It is found by experimental result that the half load to full load response is improved by 25% in two sided PWM technique when compared with the conventional PWM control technique. The photograph of the prototype of single-phase AC-DC PFC boost converter with proposed technique is shown in Fig. 2.15.

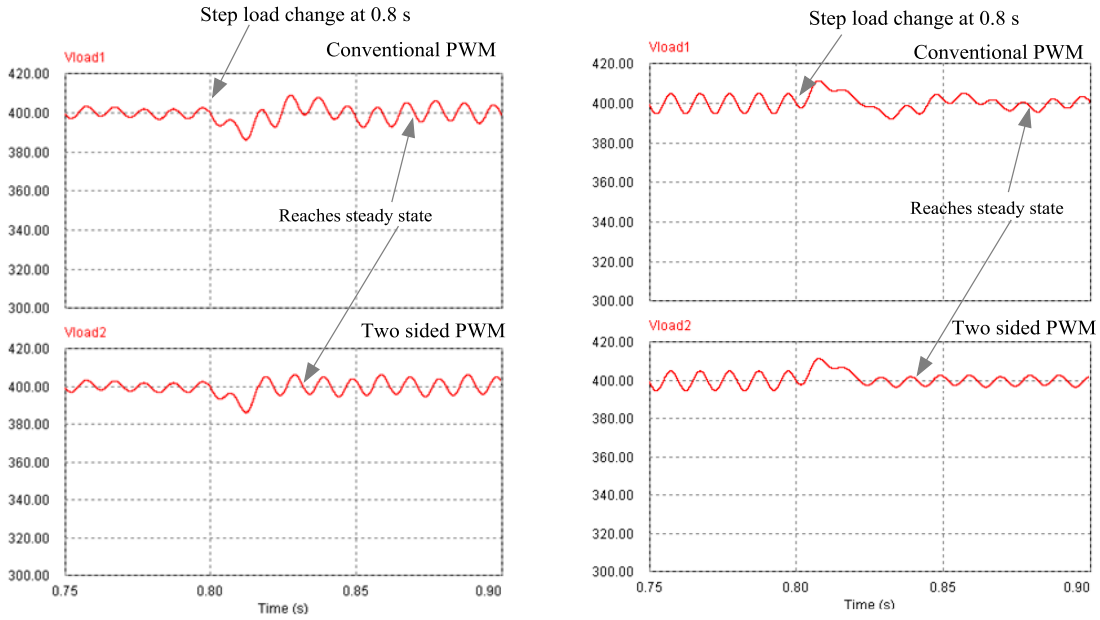
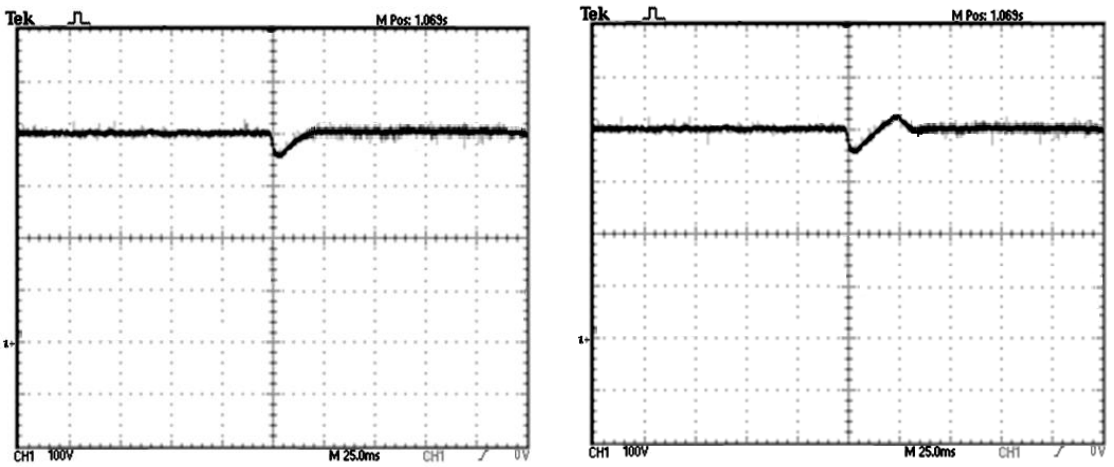


Fig. 2.13 Comparison of dynamic response of output voltage for step change in load
(a) From 50% to full load (b) Full load to 50% load



(a) Two sided PWM technique (b) Conventional PWM technique

Fig. 2.14 Output voltage comparison of two sided PWM technique and conventional PWM technique for a load current change from 50% of full load to full load
Scale: 100 *V/div*, 5 *ms /div*.

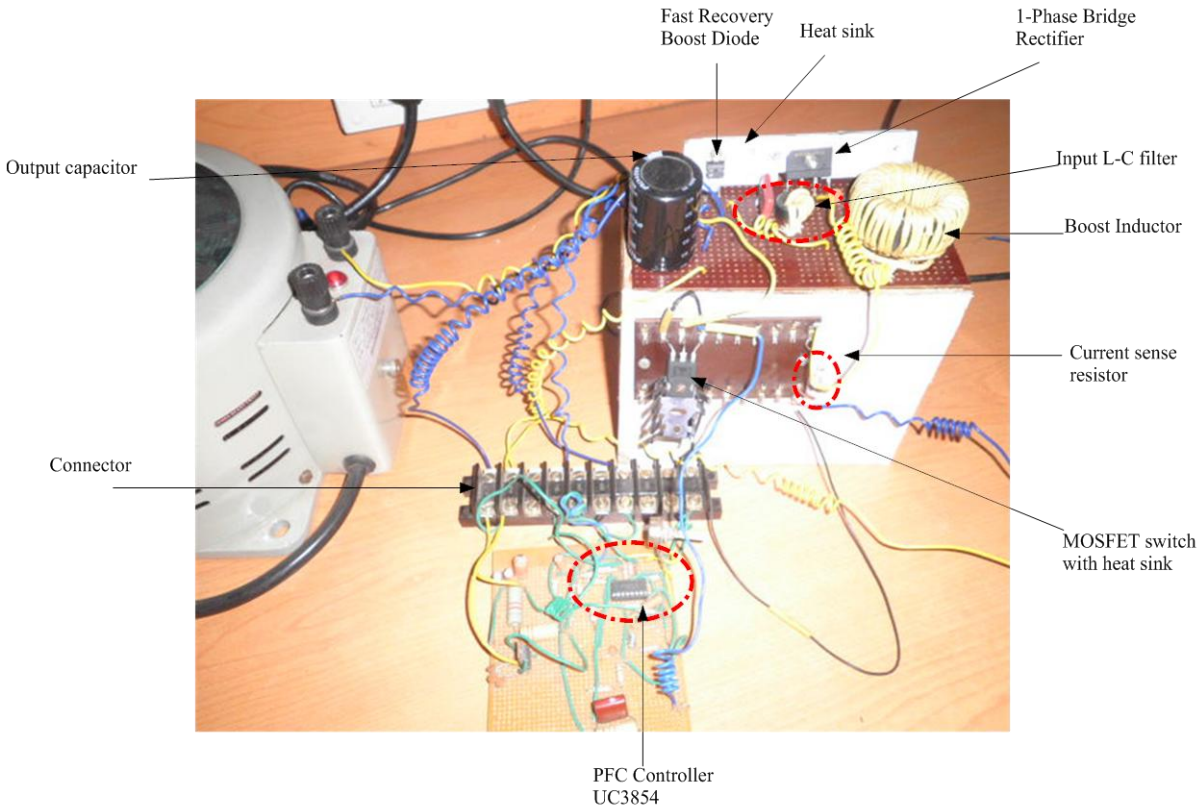


Fig. 2.15 Hardware prototype of single-phase PFC AC-DC converter with two sided PWM technique

2.4.2 Three-phase AC-DC PFC converter in Modular system

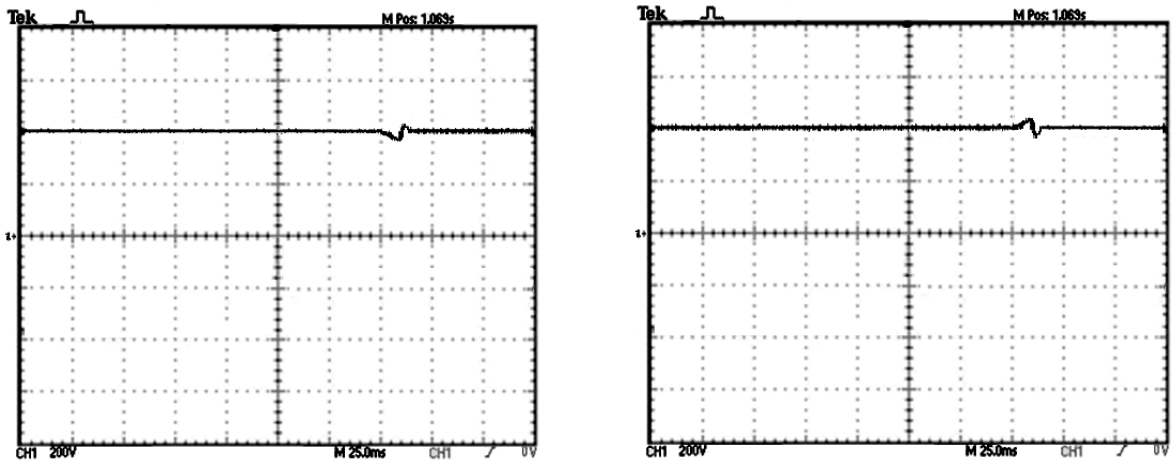
Prototypes of modular three-phase AC-DC converter with two sided PWM technique and modular three-phase system with conventional PWM technique have been built and tested in the Power Electronics and Drives Laboratory, National Institute of Technology (NIT), Rourkela, with component values as shown in Table 2.3. The components employed in each module of proposed three-phase modular system are mentioned in Table 2.2 of section 2.4.1. The complete explanation of three-phase AC-DC PFC converter with sophisticated feedback control in modular approach is described in chapter 5.

Table 2.3 Specifications of three-phase AC-DC PFC converter in modular approach

Rated Output Power (Each module)	*500 W*
Rated output power (Complete module	*3*500 = 1500 W*
Input Voltage	*215* V_{RMS}
Line Frequency	f_{line} *= 50 Hz*
Nominal Regulated Output Voltage	V_o *= 400 V*
Switching Frequency	f_s *= 100 kHz*
Target Efficiency	$\eta \geq 95\%$
Hold-Up Time	t_{hold_up} *= 20 ms*

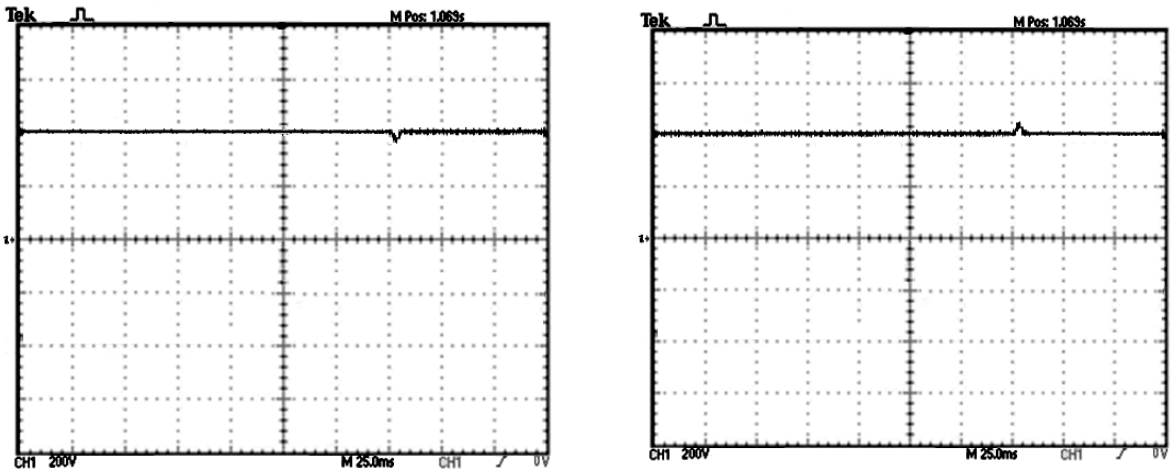
The experimental results of the proposed two sided PWM technique as well as conventional PWM technique in modular approach are shown in Fig. 2.16. Fig. 2.16 (a) shows the transient response of output voltage when load changes from 50% to full load and vice versa for conventional PWM three phase AC-DC PFC converter. On the other hand, Fig. 2.16 (b) shows the transient response of three-phase modular system of two sided PWM technique. It can be observed from Fig. 2.16 (b) that, the output voltage recovered to its steady state within 1.2 ms, which is around 30% improvement in comparison to three-phase modular system with conventional PWM technique. In specific, DC output voltage is barely disturbed in spite of low bandwidth of the DC voltage loop due to the load feedforward. It is indicated that good dynamic performance can be achieved with two sided PWM technique. In comparison of transient response of output voltage of single-phase two sided PWM technique shown earlier in Fig. 2.14 (a), and that of three-phase modular system shown in Fig. 2.16 (b), the three-phase modular system provides improved transient response at least by 20% over the single-phase PFC system.

This is due to the fact of high value of output capacitor connected across the output terminals in three-phase modular system, which improves the stability of output voltage.



50% of full-load to full-load Full-load to 50% of full-load

(a) Conventional PWM technique in modular system



50% of full-load to full-load Full-load to 50% of full-load

(b) Two sided PWM technique in modular system

Fig. 2.16 Dynamic response of output voltage for step change in load for three-phase modular system. *Scale: 200 V/div, 5ms/div.*

The performance characteristics of the three-phase system operation in modular approach with two sided PWM technique under variable load condition are presented in Fig. 2.17. Over the wide range of output power, it can be observed that, the PF varies from 0.999 to 0.995 from full-load to 25% of full load and total THD varies from 4.5% to nearly 10% from full-load to 25% of full-load and it is less than 5% at maximum load.

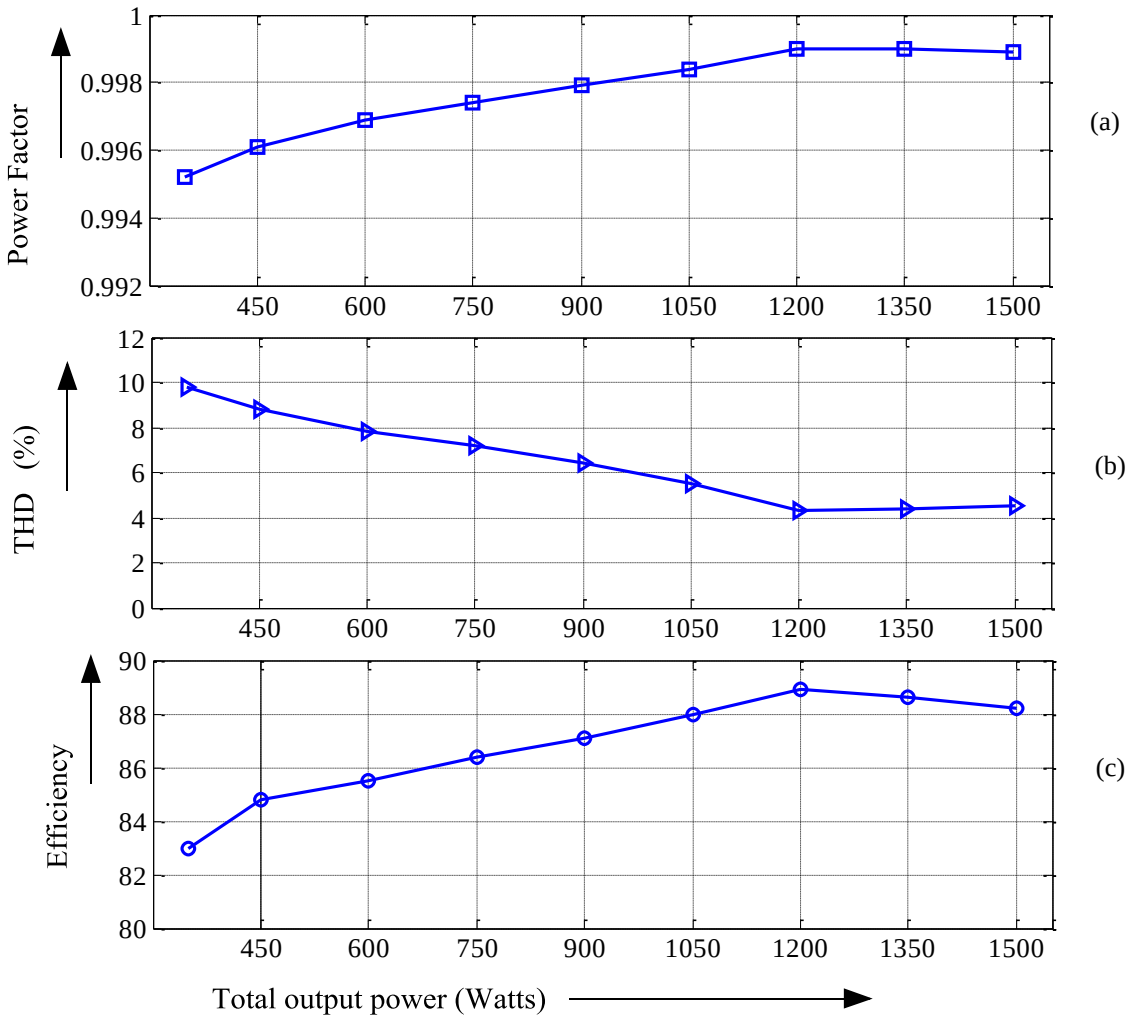


Fig. 2.17 Experimental performance characteristics of proposed three-phase modular system
(a) Power factor (b) % THD and (c) % efficiency

The proposed three-phase converter in modular approach exhibits maximum efficiency nearly 89% and at lower load conditions, the efficiency of system is lower as the converter is designed for full load condition.

2.5 Summary

The basic and main idea of incorporation of two sided PWM technique in AC-DC PFC boost converter is to improve the dynamic response of the single-phase and three-phase AC-DC PFC boost converters over the conventional PWM PFC boost converters. The comparison of two sided PWM technique and conventional PWM technique is described. The single-phase and three-phase AC-DC PFC boost converters are implemented with the proposed new two sided technique. The predicted transient response, theoretical analysis and simulation results of the proposed converters are being confirmed by the comparison of experimental results obtained from corresponding single-phase PFC and three-phase PFC converters. In addition to this, experimental results have also shown that, the proposed technique in PFC converter is capable of operating over a wide range of load without any problem. These AC-DC PFC converters controlled by two sided PWM technique have achieved nearly unity input power factor even at light load condition with low THD.

Chapter 3

Application of ZVT to PFC Boost Converter with Passive Auxiliary Circuit

- **Introduction**
- **Circuit description and PFC feedback system**
- **Operating principle of proposed converter**
- **Design procedure**
- **Simulation and Experimental results**
- **Comparison of efficiency curves**
- **Summary**

Introduction

The miniaturization of telecom and computer server equipments together with growing requirements for on-board power processing in DPS have spurred significant research and development efforts in the area of high power density and low profile power supplies. To accomplish high power density, it is required to operate PWM converters at higher switching frequencies, since the size of the reactive components (especially inductors) will reduce with the increase of switching frequency. Although, high power density can be achieved by operating PWM converters at higher switching frequencies, it is still questionable that, is PFC converter is capable of operating at such a high switching frequency? This question arises because AC-DC PFC converter circuit operating in CCM exhibits large diode reverse recovery current which results in the increased conduction loss of active switches used in the converter. In addition to this, at low line input voltage range, large amount of conduction loss is caused by diode bridge rectifier, large MOSFET on-state resistance, and diode drop, which results in low efficiency of PFC pre-regulator circuit.

The PFC converter operating at high switching frequency has two major issues; (1) Emission of EMI into utility grid and (2) generation of switching losses during switching transient period. However, passive filtering method is employed to reduce the EMI emissions into the utility. On the other hand, conduction losses remain almost constant for different switching frequencies but switching loss increases proportionally with the switching frequency. Thus it is essential to reduce the switching losses of AC-DC PFC converter operating at high switching frequency. In the last couple of decades, significant effort has been performed to minimize or to eliminate the PWM converter switching losses by employing soft switching techniques in PWM DC-DC as well as in AC-DC PFC converters [55-101, 107, 143-155].

The soft switching technique not only minimizes the switching loss but also provides

normal and safe operation of semiconductor switches in PWM converters [15, 84]. The soft switching is achieved in association with auxiliary circuit called snubber circuit. Hence snubbers are used to reduce switching losses, stresses and noise in semiconductor switch during its turn-off and turn-on processes. These stresses, strains and noise are due to parasitic capacitance, stray inductance and other imperfections in practical circuit and devices. Generally, passive snubbers are more desirable due to their inherent reliability, simple design, higher performance/cost ratio and independence [70, 94-96, 100, and 143]. These auxiliary passive circuits essentially minimize the switching losses of PWM converters to which they employed.

In this chapter, a novel passive snubber circuit is investigated and proposed to achieve soft switching in PFC boost converter with the primary objective of achieving near unity input power factor of PFC pre-regulator. The application of this novel passive snubber topology in AC-DC PFC boost converter applications is not yet reported in the literature. However, this passive snubber circuit is employed in the soft switching of DC-DC buck converter, which is reported in reference [92] for low power applications. The proposed passive snubber circuit provides ZCS and ZVS conditions for turn ON and OFF of MOSFET switch respectively in boost converter, and it does not introduce extra voltage and current stress on the semiconductor controlled MOSFET switch. In the proposed technique, by considering the magnitude of ripple current flowing in the switch, the peak switch current during the resonance interval is designed to be less than the designed switch current without the snubber. Hence, the proposed passive snubber technique does not introduce over current stress on the controlled semiconductor active switch.

This chapter is organized as follows: Section 3.1 presents description of the proposed passive snubber circuit and feedback system of AC-DC PFC boost converter. The operating principle, steady state analysis and equivalent modes of operations are described in section

3.2. Design procedure for practicability of the proposed topology is illustrated in section 3.3. In section 3.4, the simulated and experimental results are shown to prove the theoretical and mathematical analysis. Section 3.5 presents the comparison of efficiency curves of hard switched AC-DC PFC boost converter with that of the proposed single-phase AC-DC PFC boost converter. Finally important features are summarized in section 3.6.

3.1 Circuit description and PFC feedback system

3.1.1 Circuit description

The proposed single-phase AC-DC PFC boost converter with passive snubber circuit is shown in Fig. 3.1. The single-phase module of the proposed converter is composed of a

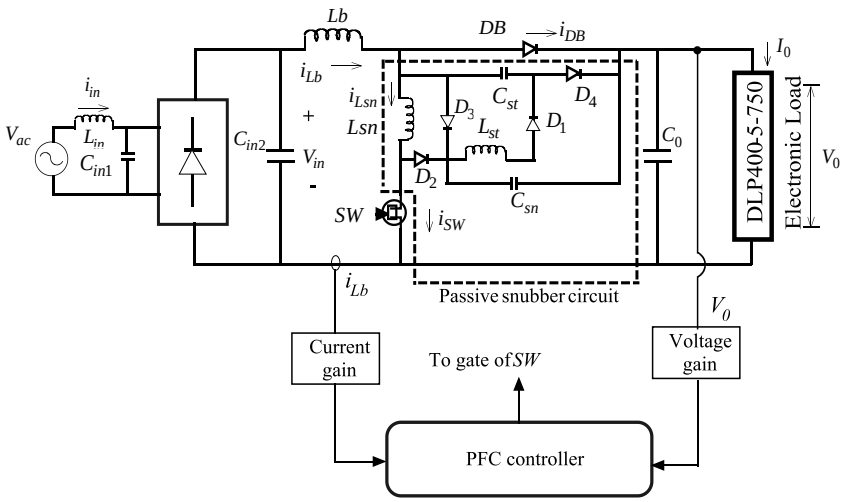


Fig. 3.1 Proposed single-phase AC-DC PFC boost converter with passive snubber circuit

small EMI filter (L_{in} and C_{in1}) followed by single-phase bridge rectifier, a low value of high frequency bypass capacitor filter C_{in2} and a DC-DC boost converter incorporated with auxiliary passive circuit. *Lb* is the boost inductor, *DB* is the boost diode. C_o is the output filter capacitor. The passive snubber circuit is composed of a snubber inductor L_{sn}, storage inductor L_{st}, storage capacitor C_{st}, snubber capacitor C_{sn} and auxiliary diodes D_1, D_2, D_3 and D_4. The concept of operation involves the transfer of snubber capacitor (C_{sn}) energy to a storage capacitor C_{st} via a resonance process and then delivers it to the output in the

successive switching action. In this passive snubber circuit, snubber elements C_{sn} and L_{sn} are fully discharged within a switching period, and hence provides zero current turn-on and zero voltage turn-off to the active switch of boost converter. The auxiliary diodes D_1, D_2, D_3, and D_4 are also turned ON and turned OFF under ZVS or/and ZCS.

The DC output voltage V_o and boost inductor current i_{Lb} of a proposed single-phase AC-DC PFC soft switched converter are sensed accurately and fed to the feedback system. A CCM PFC controller eight pin IC ICE2PCS01 is employed in feedback system which uses ACMC to achieve nearly unity input power factor in addition to obtaining the regulated output voltage. The detailed description of this ACMC is method reported in reference [156]. In this method, the inductor current is continuously monitored and the current loop is designed to regulate the average inductor current such that it is proportional to the off duty cycle of switch *SW* and thus inductor current follows rectified input voltage. Hence, the input line current is as sinusoidal as possible and in this PFC control IC ICE2PCS01, it is not required to sense the input voltage in the proposed PFC converter as that was required in PFC UC3854 controller described in section 2.1.2 of chapter 2. The triggering pulses generated from PFC controller IC ICE2PCS01 are fed to active switch *SW* of the proposed converter.

3.1.2 PFC feedback system

The simplified block diagram of current averaging circuit which is inbuilt in the PFC controller IC ICE2PCS01 is shown in Fig. 3.2. The boost inductor current i_{Lb} is sensed by a shunt resistor R_{sense} of the power converter circuit. As this sensed signal is of negative polarity together with switching ripple, the controller need to do signal averaging and convert the polarity to positive in order to apply to the following PWM block. The transfer function of averaging circuit block shown in Fig. 3.2 is given by,

$$K_{ave}(S) = \frac{V_{comp}}{i_{Lb}} = \frac{\frac{K\,R_{SENSE}}{V_{0\_EA}}}{1 + s\frac{K\,C_{comp}}{V_{0\_EA}\,(g_{OTA})}} \tag{3.1}$$

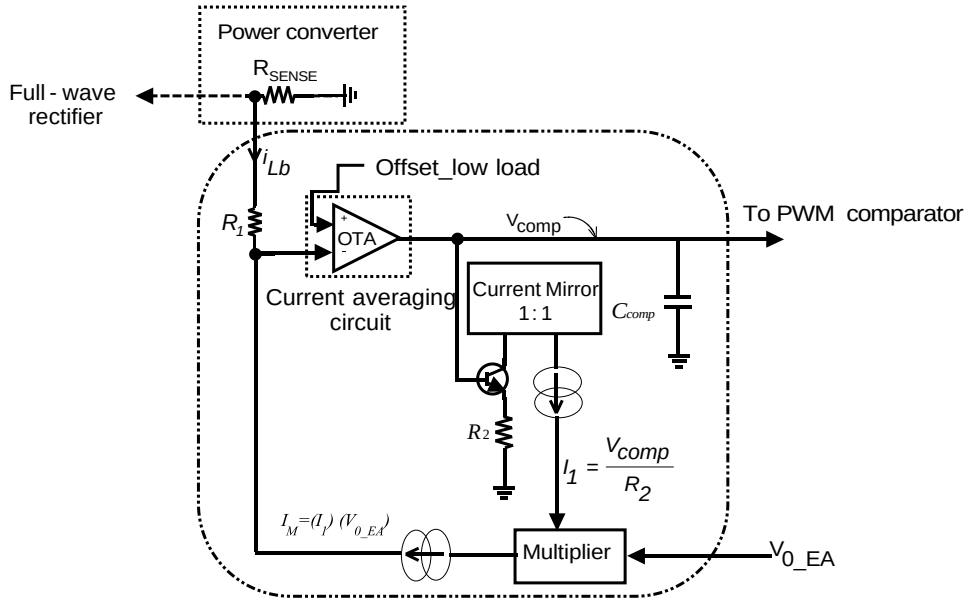


Fig. 3.2 Inductor current averaging block diagram in PFC AC-DC converter with passive snubber

where $K = R_2/R_1$, and g_{OTA} is the trans-conductance of the error amplifier *OTA* for current averaging circuit and V_{0_EA} is the variable controlled by voltage loop. C_{comp} is the capacitor at output terminal of the averaging circuit which filters out the switching current ripple. So the corner frequency of the averaging circuit f_{ave} must be lower than the switching frequency f_s of the converter. hence,

$$C_{comp} = \frac{g_{OTA}\,(V_{0\_EA})}{K\,(2\pi\, f_{ave})} \tag{3.2}$$

Under normal mode of operation, the signal V_{comp} is proportional to the averaged inductor current and is applied to PWM comparator block to generate required triggering pulses. To regulate the output voltage, a multiplier in the feedback system controls the amplitude of the sinusoidal reference signal in accordance with the voltage error signal generated from output voltage of the proposed converter. When the load decreases, the output voltage increases. To maintain constant load voltage, the control circuit senses the load voltage and the pulse width is automatically reduced in the switching cycle and the output voltage is regulated and maintained almost constant.

3.2 Operating principle of proposed converter

To simplify the steady state analysis and operating intervals of the circuit, the following conditions are assumed during one switching cycle.

- Semiconductor switches, inductors, and capacitors are ideal.
- The bridge rectifier output voltage V_{in} is constant over a switching period, as switching frequency is quite high compared to *AC* input frequency.
- Output filter capacitor C_o is large enough to maintain a constant output voltage V_o.
- The reverse recovery time of diodes D_1, D_2, D_3 and D_4 are ignored.

The circuit behavior during one switching cycle can be explained in nine intervals with the help of key waveforms shown in Fig. 3.3. The operating states of the proposed converter shown in Fig. 3.4 are analyzed under steady state condition and Table 3.1 shows the conduction state of auxiliary diodes in various intervals of operation.

Table 3.1: Conduction state of auxiliary diodes D_1-D_4 in a proposed

Note: √ Diode in conduction.

	Intervals									
Diodes	$t_0<t<t_1$	$t_1<t<t_2$	$t_2<t<t_3$	$t_3<t<t_4$	$t_4<t<t_5$	$t_5<t<t_6$	$t_6<t<t_7$	$t_7<t<t_8$	$t_8<t<t_9$	$t_9<t<t_{10}$
D_1	None		√	√						None
D_2				√		√	√			
D_3									√	
D_4							√	√	√	

The equivalent circuits are described below.

Mode 1 ($t_0<t<t_1$): Prior to $t=t_0$, only boost diode *DB* is under conduction, switch *SW* and all auxiliary diodes are in OFF state. This interval is shown in Fig. 3.4(a). At instant $t=t_0$, the switch *SW* is turned ON by applying triggering pulses, hence it turns-on with ZCS. The rate of rise of switch current i_{SW} during turn-on transition is limited by snubber inductor L_{sn}. During this interval, current in snubber inductor L_{sn} ramps up linearly while the boost diode current i_{DB} ramps down in a complimentary manner.

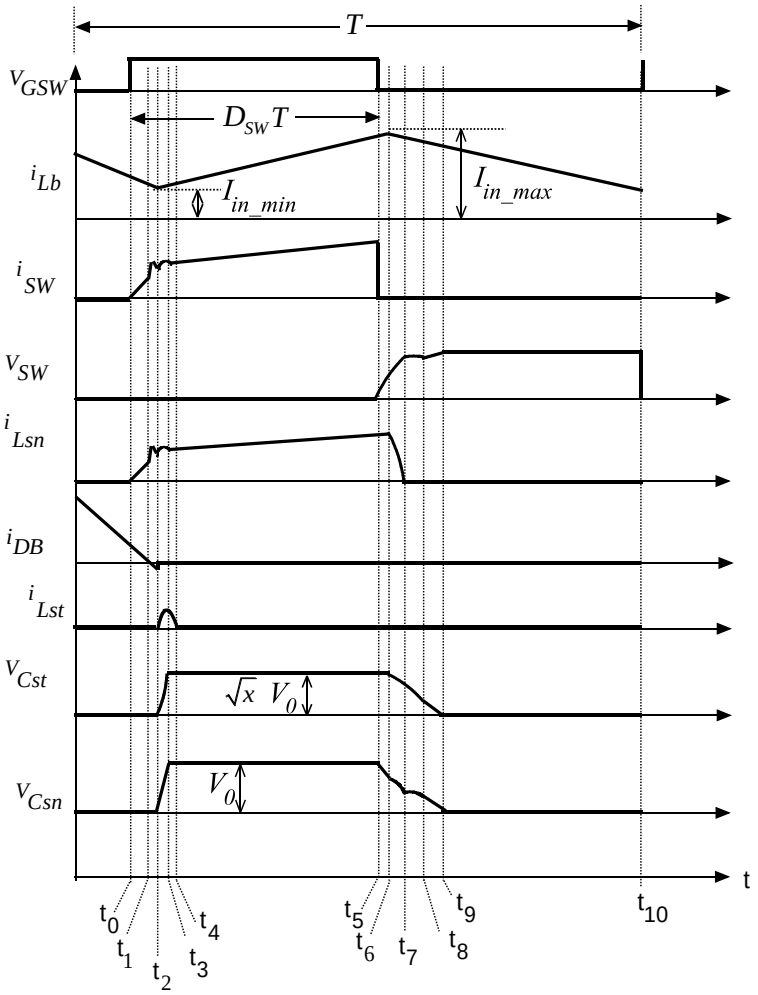


Fig. 3.3 Key waveforms of the proposed soft switching PFC AC-DC boost converter with passive snubber circuit

The following equations can be obtained for the *interval 1*,

$$i_{Lb}(t) = i_{Lb}(t_0) + \frac{(V_{in} - V_0)}{Lb}(t - t_0) \tag{3.3}$$

$$i_{SW}(t) = i_{Lsn}(t) = i_{Lsn}(t_0) + \frac{V_0}{L_{Sn}}(t - t_0) \quad 、 \tag{3.4}$$

$$i_{DB}(t) = i_{DB}(t_0) + \frac{V_0}{L_{sn}}(t - t_0) \tag{3.5}$$

$$V_{SW}(t) = V_{Csn}(t) = 0 \tag{3.6}$$

At the instant $t=t_1$, switch current i_{SW} reaches I_{in} ($i_{Lb}(t_1)$) and boost diode current i_{DB} falls to zero. Then, the switch current i_{SW} continues to rise and i_{DB} current continues to fall in reverse direction. As a result, at $t=t_2$, the reverse recovery current of *DB* falls to $-I_{rr}$,

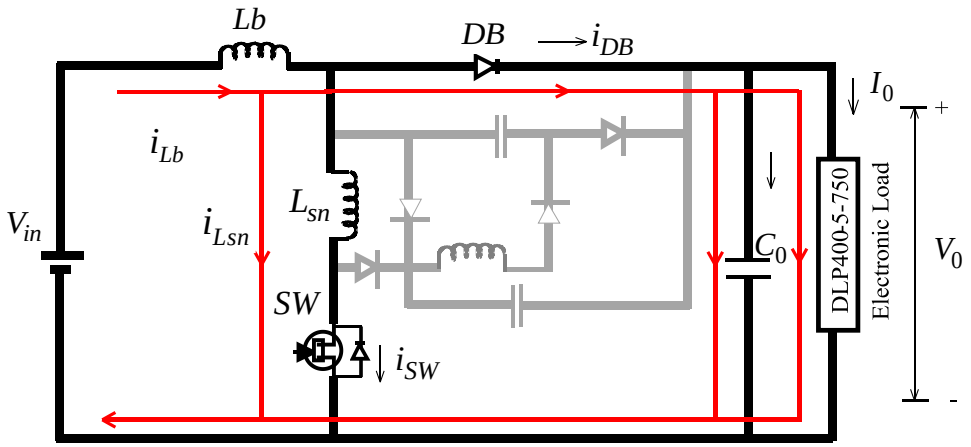


Fig. 3.4(a) Converter operation in interval (t_0-t_2)

thus the boost diode *DB* turn-off under ZVS and this mode ends at $t=t_2$. During this stage,

$$i_{DB}(t) = -\frac{V_0}{L_{sn}}(t-t_1) \tag{3.7}$$

$$i_{SW}(t_2) = i_{Lsn}(t_2) = I_{in} + I_{rr} \tag{3.8}$$

$$i_{DB}(t_2) = -I_{rr} \tag{3.9}$$

$$t_{12} = t_{rr} = \frac{L_{sn}}{V_0} I_{rr} \tag{3.10}$$

here, I_{rr} and t_{rr} are the reverse recovery current and reverse recovery time of the boost diode *DB* respectively, for the given forward current values of $I_F=I_{in}$ and $-di/dt=-V_0/L_{sn}$.

Mode 2 ($t_2<t<t_3$): The equivalent circuit during this mode is as shown in Fig. 3.4(b). As soon as boost diode *DB* turns off, the auxiliary diode D_1 becomes forward biased and hence the resonant circuit is formed along the path C_{sn}-L_{st}-D_1-C_{st}-L_{sn}. During this interval, the snubber capacitor C_{sn} and storage capacitor C_{st} starts charging by output voltage V_0. Hence, the following equations can be obtained during this interval,

$$i_{Lb}(t) = i_{Lb}(t_2) + \frac{V_{in}}{Lb + L_{sn}}(t-t_2) \tag{3.11}$$

$$i_{Lsn}(t) = i_{Lb}(t) + \frac{V_0}{Z_1}\sin\omega_1(t-t_2) \tag{3.12}$$

$$i_{Lst}(t) = i_{Lsn}(t) - i_{Lb}(t) = \frac{V_0}{Z_1}\sin\omega_1(t-t_2) \tag{3.13}$$

$$V_{Csn}(t) = V_0 \frac{1}{(1+x)}[1-\cos\omega_1(t-t_2)] \tag{3.14}$$

$$V_{Cst}(t) = xV_{Csn}(t) \tag{3.15}$$

where

$Z_1 = \sqrt{L_{eqt}/C_{eqt}}$, $\omega_1 = \sqrt{\frac{1}{L_{eqt}\ C_{eqt}}}$, $L_{eqt} = L_{sn} + L_{st}$, $C_{eqt} = (C_{sn}\ C_{st})/(C_{sn} + C_{st})$

and $x = C_{sn}/C_{st}$ is the raio between C_{sn} and C_{st}.

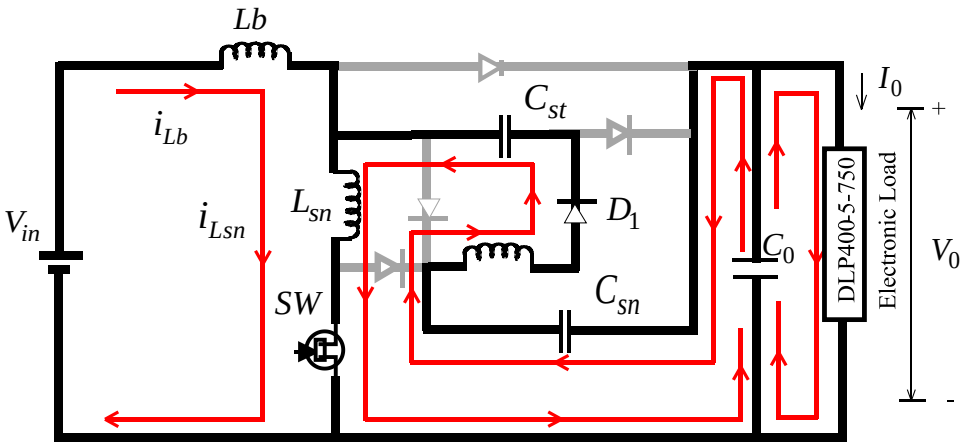


Fig 3.4(b) Converter operation in interval (t_2-t_3)

This mode continues until the snubber capacitor C_{sn} charges to a level of output voltage V_0. Hence at $t=t_3$, $V_{Cst}(t_3) = V_0$,

thus by using (3.14),

we have, $cos\omega_1(t_3-t_2) = -x$ (3.16)

By substituting (3.16) into (3.15), we have

$V_{cst}(t_3) = xV_0$ (3.17)

hence, in order to ensure the existence of t_2 for charging snubber capacitor C_{sn} completely, the value of x in (3.16) should be less than or equal to 1. Therefore, $C_{St} \geq C_{Sn}$.

by using (3.16), we have, $(t_3 - t_2) = \frac{1}{\omega_1}\left(\pi/2 + \sin^{-1} x\right)$ (3.18)

Mode 3 (t_3<t<t_4): Fig. 3.4(c) shows the equivalent circuit during mode 3. At t_3, as soon as snubber capacitor C_{sn} reaches to a level of output voltage V_0, the auxiliary diode D_2

becomes forward biased, hence D_2 turns-on with ZCS. During this interval, the energy stored in storage inductor L_{st} is transferred to the storage capacitor via the resonance path L_{sn}-D_2-L_{st}-D_1-C_{st}. The following equations are valid during this interval,

$$i_{Lb}(t) = i_{Lb}(t_3) + \frac{V_{in}}{(L_b + L_{sn})}(t - t_4) \tag{3.19}$$

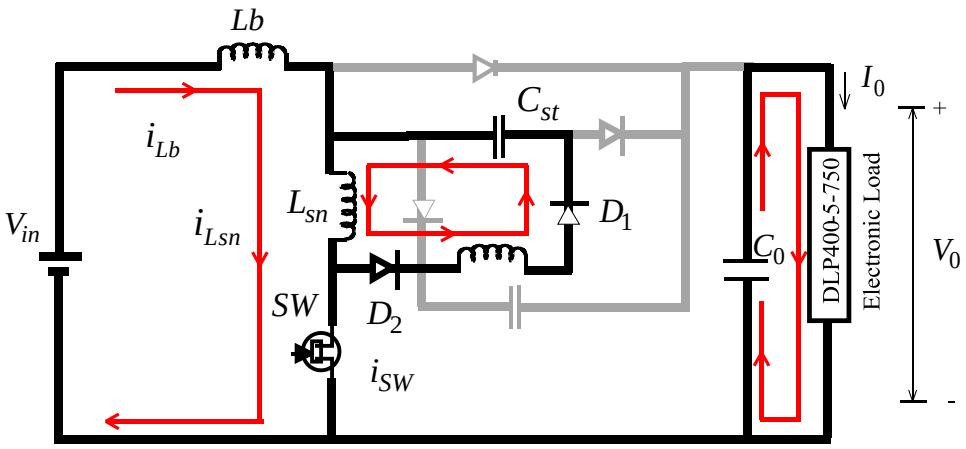


Fig. 3.4(c) Converter operation in interval (t_3-t_4)

$$i_{Lsn}(t) = i_{Lb}(t) + \frac{V_0}{Z_2}\cos[\omega_2(t - t_3) + \phi_2] \tag{3.20}$$

$$i_{Lst}(t) = \frac{V_0}{Z_2}\cos[\omega_2(t - t_3) + \phi_2] \tag{3.21}$$

$$V_{Csn}(t) = V_0 \tag{3.22}$$

$$V_{Cst}(t) = \sqrt{x}\ \ V_0 \sin[\omega_2(t - t_3) + \phi_2] \tag{3.23}$$

where $Z_2 = \sqrt{L_{eqt}/C_{st}}$, $\omega_2 = \sqrt{\frac{1}{L_{eqt}\ C_{st}}}$, and $\phi_2 = \tan^{-1}\left(\sqrt{\frac{x}{1-x}}\right)$.

This mode ends when the energy from L_{st} is transferred to storage capacitor C_{st} completely. Hence the current through storage inductor gradually ceases to zero at t_4, and hence both diodes D_1 and D_2 are turned OFF at near zero current.

Mode 4 (t_4<t<t_5): As shown in Fig. 3.4(d), the switch current i_{SW} continues to conduct. A load is supplied by the output capacitor C_0 and the input power continues to store in the boost inductor *Lb*. This interval defines the duty cycle of the switch *SW* and is equivalent to switch ON period of conventional hard switch PWM boost converter. In this interval, the passive snubber circuit is completely inactive.

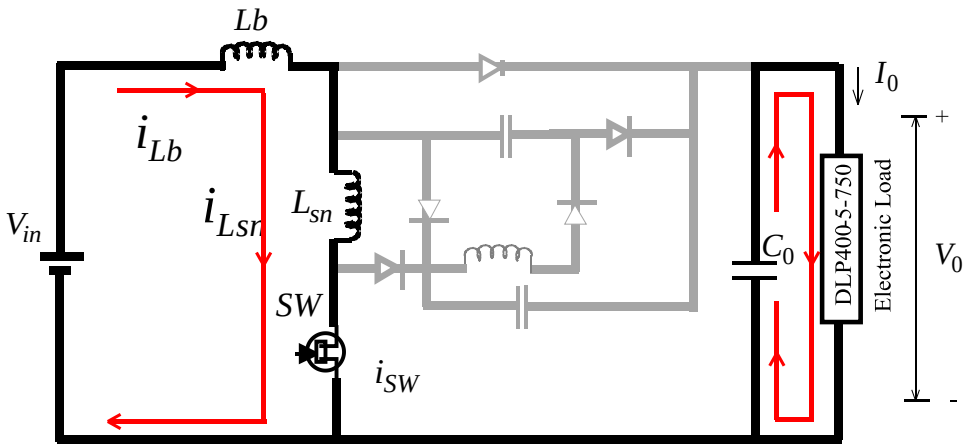


Fig. 3.4(d) Converter operation in interval (t_4-t_5)

During this interval,

$$i_{Lb}(t) = i_{Lsn}(t) = i_{Lb}(t_4) + \frac{V_{in}}{(L_b + L_{sn})}(t - t_4) \tag{3.24}$$

$$i_{Lst}(t) = 0 \tag{3.25}$$

$$V_{Csn}(t) = V_0 \tag{3.26}$$

$$V_{Cst}(t) = \left(\sqrt{x}\right)V_0 \tag{3.27}$$

Mode 5 (t_5<t<t_6): This interval is shown in Fig. 3.4(e). The triggering pulse to switch *SW* is removed at t_5, thus the switch is turned-off near ZVS and its rate of change of voltage is limited by snubber capacitor C_{sn}. During this interval, the current in snubber inductor L_{sn} keeps flowing and it acts as a current source and hence the current flows through the auxiliary diode D_2 and auxiliary diode D_1 will not be conducted as it is reverse biased by a storage

capacitor voltage V_{Cst}. During this interval the capacitor C_{sn} is discharged to load through I_{in} (input current $i_{Lb}(t)$). During this mode,

$$i_{Lb}(t) = i_{Lsn}(t) = i_{Lb}(t_5) + \frac{V_{in} + V_{Csn}(t) - V_0}{(L_b + L_{sn})}(t - t_5) = I_{in} \tag{3.28}$$

$$i_{Lst}(t) = 0 \tag{3.29}$$

$$V_{Csn}(t) = V_0 - \frac{Iin}{C_{Sn}}(t - t_5) \tag{3.30}$$

$$V_{Cst}(t) = \left(\sqrt{x}\right)V_0 \tag{3.31}$$

$$\therefore V_{Cst}(t_6) = \left(\sqrt{x}\right)V_0 \Rightarrow\Rightarrow V_{Cst}(t_5) \tag{3.32}$$

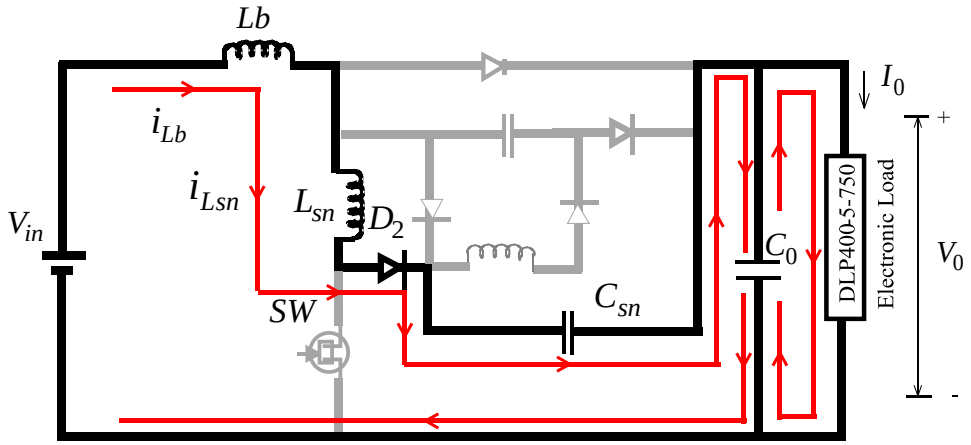


Fig. 3.4(e) Converter operation in interval (t_5-t_6)

This mode ends when the snubber capacitor voltage V_{csn} drops to a level of $\sqrt{x}\,V_o$.

From (3.30), we have,

$$(t_6 - t_5) = (1 - \sqrt{x})\,\frac{C_{sn}}{I_{in}}V_0 \tag{3.33}$$

***Mode 6 (t_6<t<t_7)*:** The equivalent circuit during this mode is shown in Fig. 3.4(f). During this interval, the energy stored in the capacitors C_{st} and C_{sn} is discharged to output load. The diodes D_1 and D_3 are reverse biased hence the snubber capacitor C_{sn} is discharged through D_2 and the storage capacitor C_{st} discharges through D_4.During this interval,

$$i_{Lb}(t) = i_{Lsn}(t) = i_{Lb}(t_6) + \frac{(V_{in} + V_{Csn}(t) - V_0)}{(L_b + L_{sn})}(t - t_6) \tag{3.34}$$

$$i_{Lst}(t) = 0 \tag{3.35}$$

$$V_{Csn}(t) = \left(\sqrt{x}\right)V_0 - \frac{I_{in}}{C_{st}(1+x)}(t - t_6) - \frac{I_{in}}{x\ \omega_3\ C_{st}(1+x)}\ sin\omega_3 (t - t_6) \tag{3.36}$$

$$V_{Cst}(t) = \left(\sqrt{x}\right)V_0 - \frac{I_{in}}{C_{st}(1+x)}(t - t_6) \tag{3.37}$$

here,

$$\omega_3 = \sqrt{\frac{1}{L_{sn}\ C_{eqt}}}\ .$$

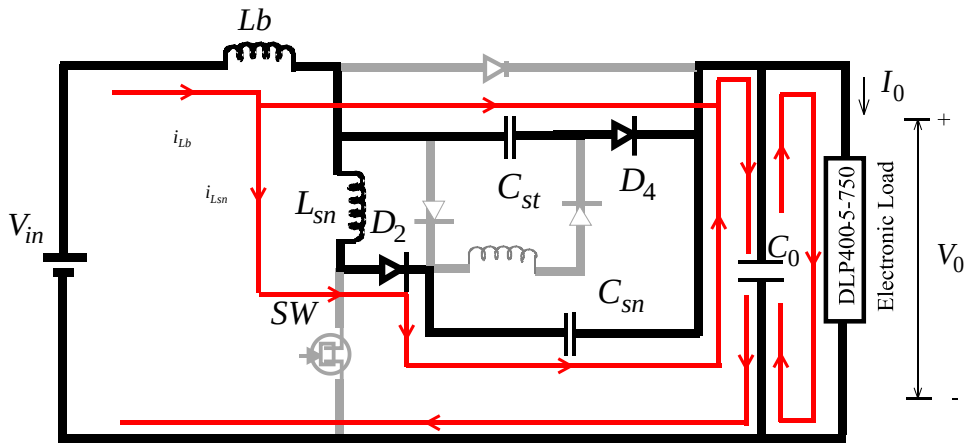


Fig. 3.4(f) Converter operation in interval (t_6-t_7)

At the end of this mode, the snubber inductor current i_{Lsn} gradually ceases to zero, hence the diode D_2 is turned OFF at ZCS. At $t=t_7$, the following equations are valid,

$$i_{Lsn}(t_7) = 0 \tag{3.38}$$

$$v_{Csn}(t_7) \cong \left(\sqrt{x}\right)V_0 - \frac{I_{in}}{1+x}\sqrt{\frac{L_{sn}}{C_{st}}}\ \sqrt{\frac{x}{1+x}}\left(\frac{\pi}{2} + \sin^{-1}x + \frac{\sqrt{1-x^2}}{x}\right) \tag{3.39}$$

$$v_{Cst}(t_7) \cong \left(\sqrt{x}\right)V_0 - \frac{I_{in}}{1+x}\sqrt{\frac{L_{sn}}{C_{st}}}\ \sqrt{\frac{x}{1+x}}\left(\frac{\pi}{2} + \sin^{-1}x + \frac{\sqrt{1-x^2}}{x}\right) \tag{3.40}$$

Mode 7 (t_7<t<t_8): This interval of operation is shown in Fig. 3.4(g). The discharge of storage capacitor C_{st} continues to discharge by I_{in} during this interval. The path D_3-L_{st}-D_1

will not conduct as D_1 is reverse biased by storage capacitor voltage v_{Cst}. During this mode, following equations are valid.

$$i_{Lb}(t) = i_{Lsn}(t) = i_{Lb}(t_7) + \frac{(V_{in} + V_{Cst}(t) - V_0)}{Lb}(t - t_7) \tag{3.41}$$

$$i_{Lsn}(t) = i_{Lst}(t) = 0 \tag{3.42}$$

$$V_{Cst}(t) = V_{Cst}(t_7) \tag{3.43}$$

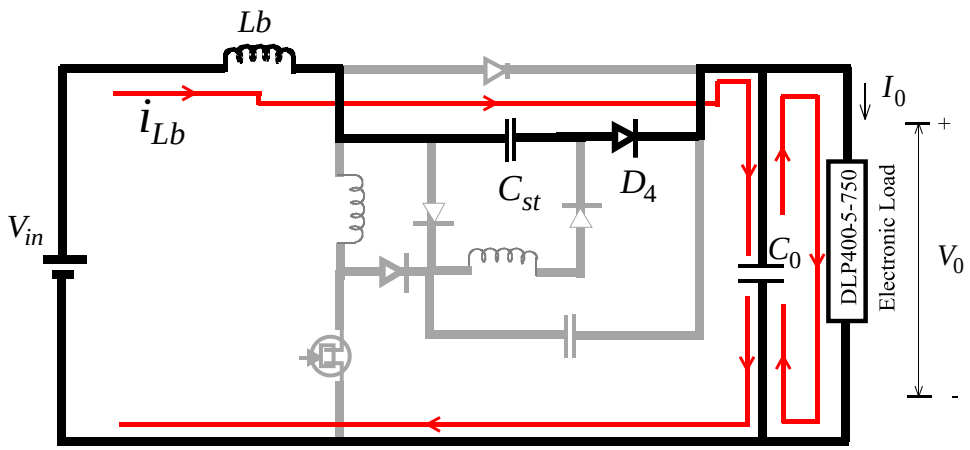


Fig. 3.4(g) Converter operation in interval (t_7-t_8)

$$V_{Cst}(t) = V_{Cst}(t_7) - \frac{I_{in}}{C_{st}}(t - t_7) \tag{3.44}$$

This interval ends at t_8, at this instant the voltage level of storage capacitor v_{cst} is given by

$$V_{Cst}(t_8) = V_{Csn}(t_7) \tag{3.45}$$

Mode 8 (t_8<t<t_9): Fig. 3.4(h) shows the equivalent circuit during this interval. At instant t=t_8, the diode D_3 becomes forward biased and hence the earlier remained energy in the snubber capacitor C_{sn} is discharged to output load. Simultaneously, the stored capacitor C_{st} continues to discharge through D_4. This mode ends when both the capacitors C_{sn} and C_{st} are completely discharged and hence both the diodes D_3 and D_4 are turned OFF at near zero voltage. During this mode,

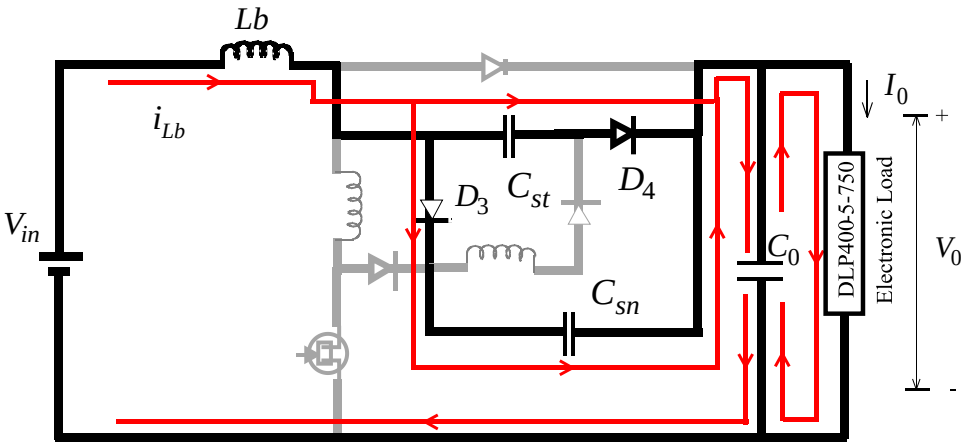


Fig. 3.4(h) Converter operation in interval (t_8-t_9)

$$i_{Lb}(t) = i_{Lb}(t_8) + \frac{(V_{in} + V_{Cst}(t) - V_0)}{Lb}(t - t_8) \tag{3.46}$$

$$i_{Lsn}(t) = i_{Lst}(t) = 0 \tag{3.47}$$

$$V_{Csn}(t) = V_{Csn}(t_8) - \frac{I_{in}}{C_{st}(1+x)}(t - t_8) \tag{3.48}$$

$$V_{Cst}(t) = V_{Cst}(t_8) - \frac{I_{in}}{C_{st}(1+x)}(t - t_8) \tag{3.49}$$

***Mode 9 (t_9<t<t_{10})*:** The equivalent circuit for this interval is as shown in Fig. 3.4(i). This interval is essentially a boost diode conduction mode which connects the load to supply line through boost inductor *Lb*. The passive snubber circuit is not active and the response of this stage is similar to that of the switch OFF period of conventional hard switched PWM boost converter.

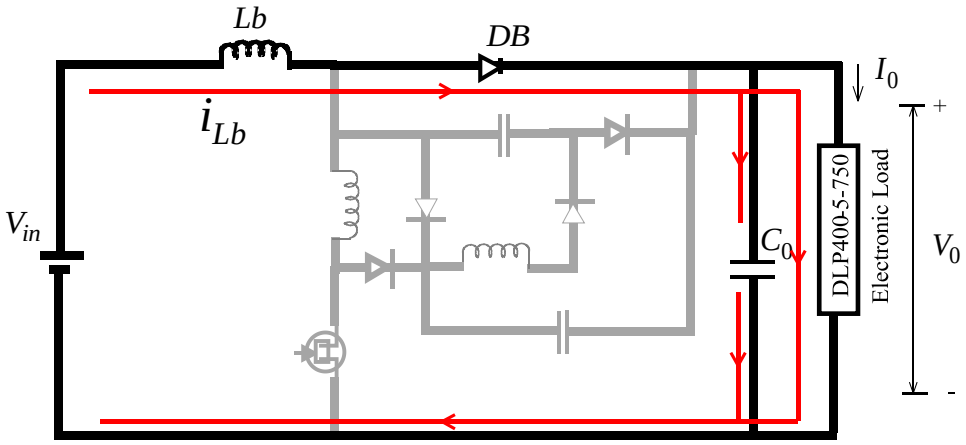


Fig. 3.4(i) Converter operation in interval (t_9-t_{10})

During this interval, the following equations are valid,

$$i_{Lb}(t) = i_{Lb}(t_9) + \frac{(V_{in} - V_0)}{Lb}(t - t_9) \tag{3.50}$$

$$i_{Lsn}(t) = i_{Lst}(t) = 0 \tag{3.51}$$

$$V_{Csn}(t) = V_{Cst}(t) = 0 \tag{3.52}$$

$$V_{SW}(t) = V_0 \tag{3.53}$$

At the instant $t=t_{10}$, one complete cycle is completed and the next switching cycle is repeated from that instant onwards.

From the key waveforms of the analysis shown in the Fig. 3.3, the minimum on-time '$t_{on,MIN}$' and minimum off-time '$t_{of,MIN}$' of the active switch can be obtained as follows,

$$t_{on,MIN} = \frac{L_{sn} I_{in}}{V_0} + \frac{1}{\omega_1}\left(\frac{\pi}{2} + \sin^{-1} x\right) + \frac{1}{\omega_1}\tan^{-1}\sqrt{\frac{1}{x} - 1} \tag{3.54}$$

$$t_{off,MIN} = \frac{C_{sn} V_0}{I_{in}}\left(1 + \frac{1}{\sqrt{x}}\right) \tag{3.55}$$

here, the minimum on-time '$t_{on,MIN}$' in the minimum time required to transfer the complete stored energy from snubber capacitor C_{sn} to the reset circuit. This time is measured from t_0 to t_4. While the '$t_{off,MIN}$' is the total time measured from 't_5' to 't_9'.

If the actual on time of the switch is shorter than $t_{on,MIN}$, the complete energy would not be transferred to the storage capacitor C_{st} before the turn-off of the switch *SW*. Hence, the switch has to be turned off with some non-zero voltage of snubber capacitor C_{sn}, which may result in nonzero voltage switching of the switch. On the other hand, if the actual turn-off time of the switch *SW* is shorter than $t_{off,MIN}$, then C_{st} cannot be completely discharged before the switch *SW* is turned ON. Then, when the switch is turned ON, C_{st} cannot be completely discharged. Then the snubber capacitor voltage v_{Csn} is nonzero before the switch is turned OFF. Hence, the switch will be turned OFF with nonzero voltage. In both of the cases, as

described in Fig. 2 and Fig. 3, the switch can still be turned ON with zero current from '*mode 9'* to '*mode 1'* (next successive switching cycle), due to the presence of snubber inductor L_{sn}, even if the main switch cannot be turned OFF with zero voltage.

3.3 Design procedure

The procedure of selecting boost converter components *Lb*, and C_o is the same as that for a conventional PWM boost converter as described in section 2.3.2, chapter 2, hence, in this chapter, the more focus is given on the designing of the passive auxiliary circuit, where the snubber, storage inductors and snubber, storage capacitors are most important components for proposed soft switching.

3.3.1 Snubber inductor L_{sn}

It was mentioned in the introduction of this chapter that, one of the main problems of the boost converter is reverse recovery current of the boost diode. This is a function of the diode's turn-off *di/dt* and can be improved by diverting the flow of current through it eventually. Hence, the precise value of L_{sn} is computed by considering the rate of rise of switch current during turn-on period of MOSFET switch, hence,

$$L_{sn} \leq \frac{t_{12}\, V_0}{I_{in\_\max}} \tag{3.56}$$

where t_{12} is the reverse recovery time which is a part of interval 1 described in section 3.2. I_{in_max} is the peak value of input current I_{in}.

3.3.2 Snubber and storage capacitors C_{Sn} and C_{St}

The values of C_{sn} and C_{st} are designed by the following standard iterative procedure. In the initial step, $x \in [0,1]$ is arbitrarily selected. In the second step, it is to be ensured that the MOSFET switch voltage stress during mode 5 must be less than V_0. Based on this, by substituting '*x'* into (3.39) and assuming V_{Cs} is less than V_0, it can be found that,

$$C_{Sn} \geq \frac{x}{1+x}\left(\frac{I_{in}}{V_0(1+x)}\right)^2 \left(\pi/2 + \sin^{-1} x + \frac{\sqrt{1-x^2}}{x}\right)^2 \quad (3.57)$$

The minimum value of input current I_{in}, I_{in_min} which ensures the soft switch is calculated by substituting 'x' into (3.55) with the designed minimum OFF time t_{off,MIN_d}. Thus,

$$I_{in\_\min} = \frac{C_{sn}\, V_0}{t_{off,MIN\_d}}\left(1+\frac{1}{\sqrt{x}}\right) \quad (3.58)$$

here, t_{off,MIN_d} is the designed minimum off time value of t_{off_MIN}.

The arbitrarily selected value of '*x'* is accepted if above calculated value of I_{in_min} is below the designed minimum input current for PFC boost converter (procedure described in section 2.3.2, chapter 2). Otherwise, another value of '*x'* is selected and the same steps are repeated. With the proper selection of '*x'*, C_{st} is obtained from the value of C_{sn}, i.e. $C_{st}=C_{sn}/x$.

3.3.3 Storage inductor L_{st}

One of the important factors considered in soft-switching is the reduction of current stress on the MOSFET device. Hence, the suitable value of storage inductor L_{st} is calculated based on the current stress on the switch which is not higher than the designed input line current ripple ΔI_{in}. Thus, based on (3.13), we have

$$L_{st} = \left(\frac{V_0}{\Delta I}\right)^2 \frac{C_{sn}}{1+x} - L_{sn} \quad (3.59)$$

Note: It is required to compare the calculated value of t_{on_MIN} in (3.54) with the minimum duty cycle ratio duration required for the boost converter to achieve soft switching and to obtain nearly unity input power factor of the proposed converter. i.e. $D_{Min}\, T > t_{on\_MIN}$. If this condition is satisfied, above calculated set of components will be taken. Otherwise, the new set of values will be chosen again.

3.4 Simulation and Experimental results

A prototype of the proposed single-phase AC-DC PFC boost converter with passive snubber circuit has been built and fabricated in the Power Electronics and Drives

laboratory, NIT, Rourkela. The proposed converter operates with an input voltage of 215 V_{rms}, output voltage V_0=400 V, 500 W and a switching frequency of 100 kHz. The schematic of the proposed converter is simulated in PSIM simulator package to verify the theoretical and design analysis of the proposed converter. The major parameters and components employed in the prototype are tabulated in Table 3.2.

Table 3.2: Components used in the Proposed 1-phase PFC with passive snubber converter

Component	**Value/Model**	
	Simulation	**Experiment**
Bridge Rectifier IC	Ideal	GBJ 2506-BP
Switch, SW	Ideal	IRFP 460
Auxiliary Diodes ($D_1 - D_4$)	Ideal	RHRP 3060
Boost Diode, DB	Ideal	DSEI 30-12A
Low line filter inductor (L_{in})	5.6μH	5.6μH
Input filter (C_{in1})	0.47μF, 275V	0.47μF, 275V
Input HF bypass capacitor (C_{in2})	1μF, 630V	1μF, 630V
Boost inductor (Lb)	1.5 mH	1.5 mH
Snubber inductor (L_{sn})	2.5 μH	2.5 μH
Storage inductor (L_{st})	62.5 μH	62.5 μH
Snubber capacitor (C_{sn})	0.68 μF	0.68 μF
Storage capacitor (C_{st})	1.2 μF	1.2 μF
output capacitor (C_0)	450μF, 600V	450μF, 600V

The simulation and experimental results of snubber inductor current i_{Lsn}, storage inductor current i_{Lst}, snubber capacitor voltage V_{Csn}, and storage capacitor voltage V_{Cst} waveforms are shown in Fig. 3.5 and Fig. 3.6 respectively. From Fig. 3.5 and Fig. 3.6, it

can be verified that, the experimentally obtained waveforms presented in Fig. 3.6 are closer to that obtained in simulation response shown in Fig. 3.5. This is a proof of evidence that, the simulation and experimental results are strongly agree with the theoretical designed analysis of the operating principle of the proposed PFC converter with passive snubber circuit.

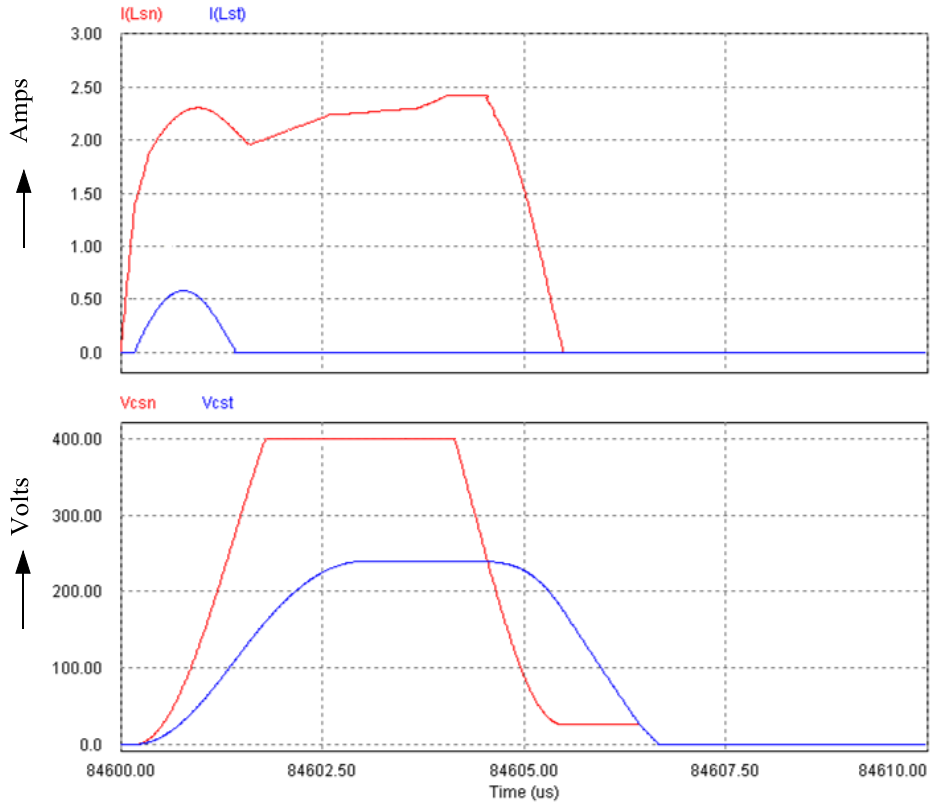


Fig. 3.5 Simulation results of resonant elements of proposed passive snubber circuit
Top: Snubber inductor (L_{sn}) and storage inductor (L_{st}) currents
Bottom: Snubber capacitor (C_{sn}) and storage capacitor (C_{st}) voltages

Fig. 3.7 and Fig. 3.8 show the simulation and experimental switching waveforms respectively of MOSFET switch *SW* at full load condition. Comparing simulated results shown in Fig. 3.7 with experimentally obtained results presented in Fig. 3.8, the experimentally obtained results are nearly identical to simulation results, except that the

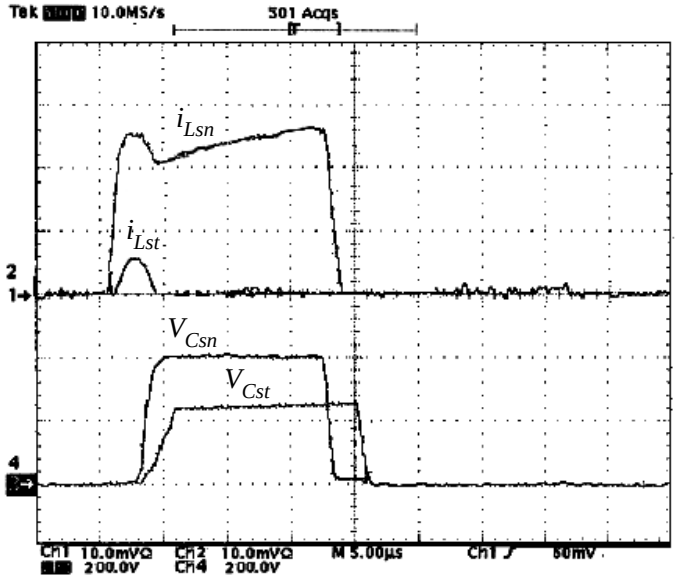


Fig. 3.6 Experimental results of resonant elements of proposed passive snubber circuit
Top: Snubber inductor (L_{sn}) and storage inductor (L_{st}) currents
Bottom: Snubber capacitor (C_{sn}) and storage capacitor (C_{st}) voltages
Scale: Ch1, Ch2: 2 A/div, Ch3, Ch4: 200 V/div, 1 µsec/div

presence of *di/dt* effect in Fig. 3.8 across the MOSFET switch, which is due to stray inductance of the circuit. However, the voltage across the MOSFET switch *SW* is equal or within the output voltage level. In both the cases, the switch turns on with zero current and turns off with zero voltage.

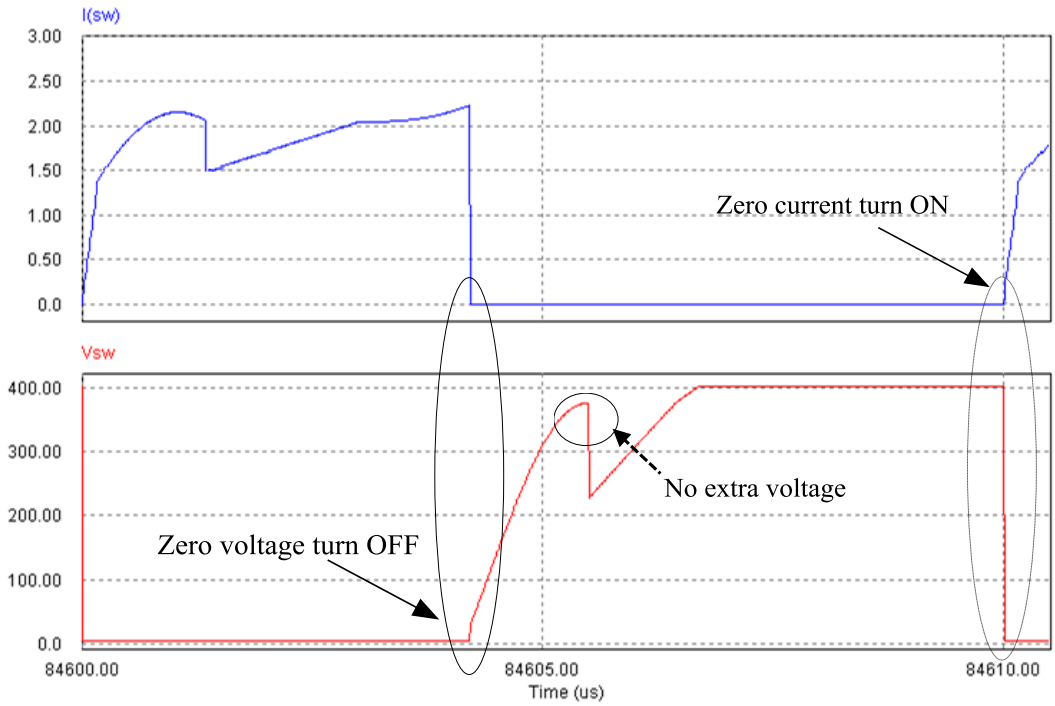


Fig. 3.7 Simulation results of switching characteristics of switch *SW* of proposed converter

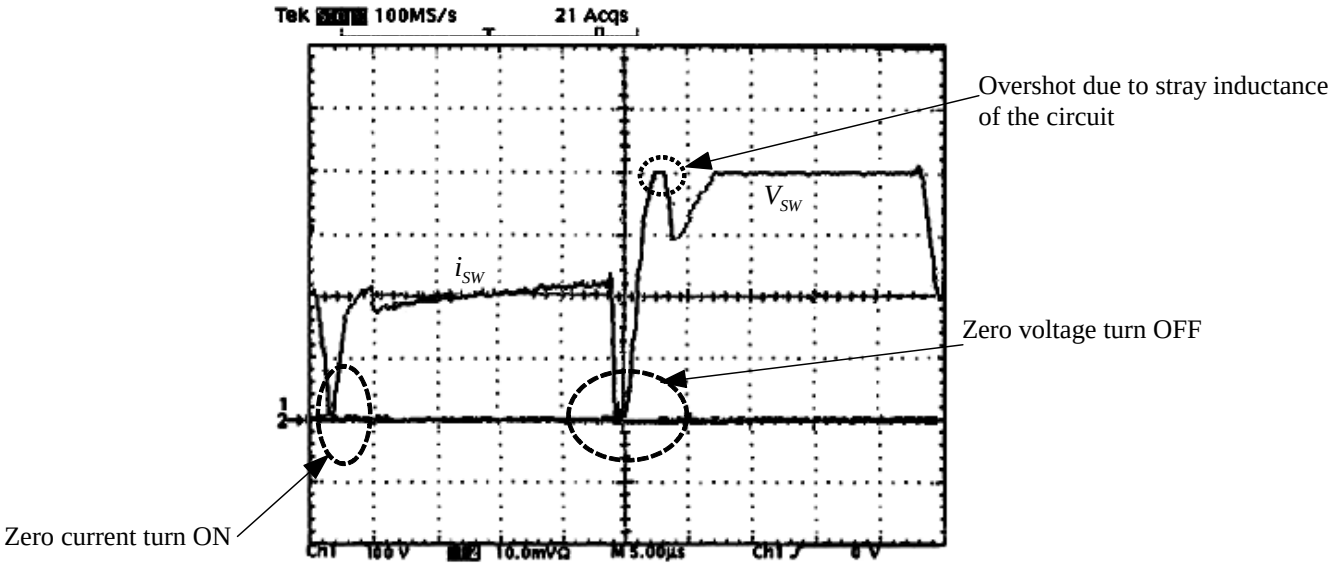


Fig. 3.8 Experimental results of switching characteristics of switch SW of proposed converter
Scale: Ch1: 100 V/div, Ch2: 1 A/div, 1μs/div

The simulation and experimental results of soft switching characteristics of boost diode *DB* are shown in Fig. 3.9 and Fig. 3.10 respectively. The boost diode *DB* exhibits zero voltage turn-off and zero current turn-on processes.

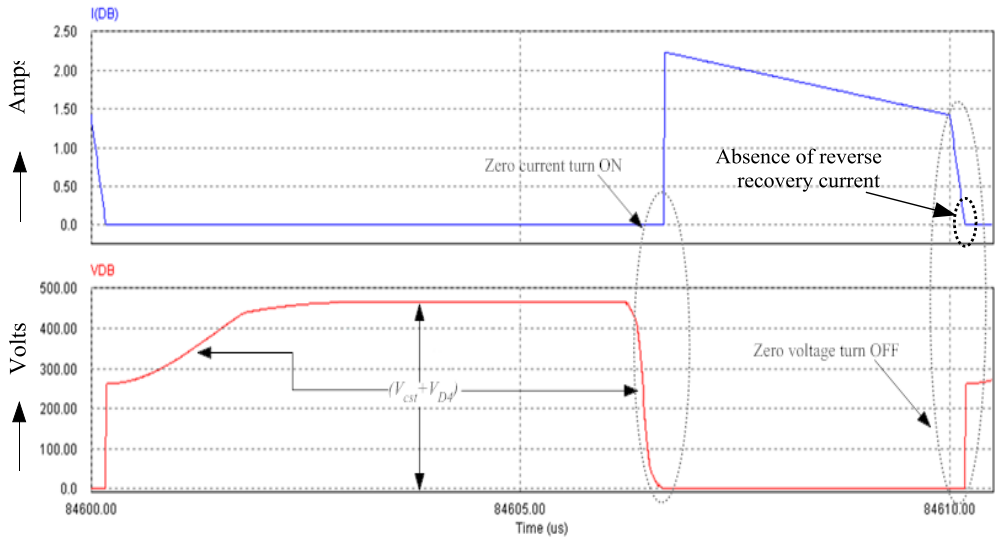


Fig. 3.9 Simulation results of soft switching of boost diode in proposed passive snubber converter
Top: Boost diode current i_{DB} waveform. *Bottom:* Boost diode voltage V_{DB} waveform.

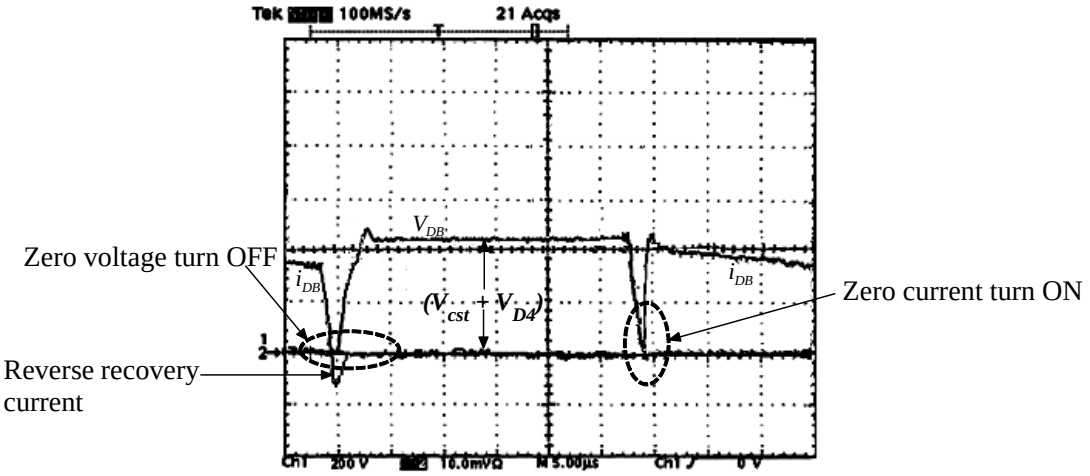
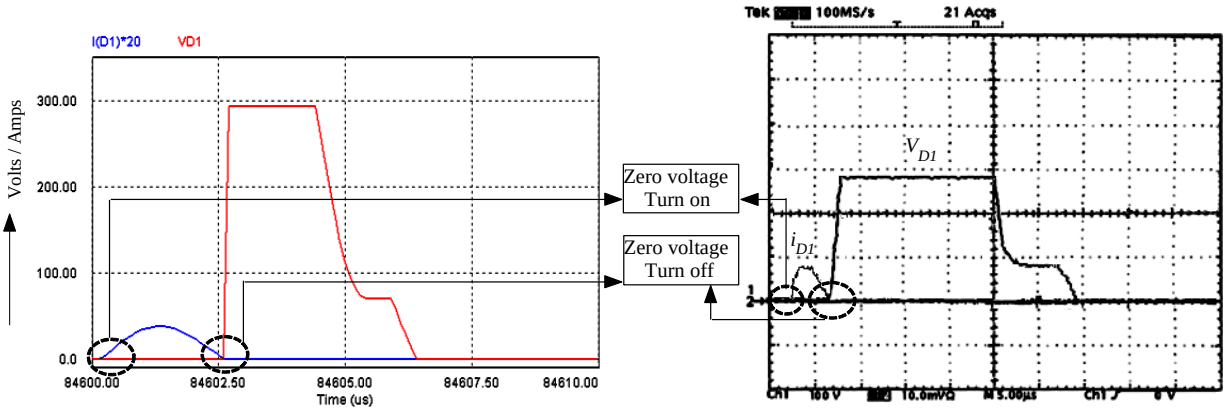


Fig. 3.10 Experimental result of soft switching of boost diode in proposed passive snubber converter
Scale: Ch1: 200 V/div, Ch2: 1 A/div, 1µs.

The experimentally obtained result shown in Fig. 3.10 almost resembles the simulated switching results of boost diode *DB* presented in Fig. 3.9, except that the absence of reverse recovery current of boost diode *DB* in the Fig. 3.9. This is because, the discrete transition simulators like PSIM do not apply full physical model of device and as a result such simulators are not capable of showing parasitic processes such as reverse recovery process. In the proposed converter, the boost diode *DB* turns off with ZVS and turns on with ZCS.

Fig. 3.11 shows the simulated and experimental results of voltage and current waveforms of auxiliary diode D_1. This diode starts conducting at the beginning of the *'mode 2'* (t_2-t_3) and terminates its conduction at the end of the *'mode 3'* (t_3-t_4). This diode exhibits zero voltage turn-on and turn-off processes.

The simulated and experimentally obtained switching voltage and current waveforms of auxiliary diode D_3 are presented in Fig. 3.12. This device conducts only during 'interval 8' (t_8-t_9) and experiences zero current turn-on and zero voltage turn-off. From Fig. 3.11 and Fig. 3.12, it can be observed that, the voltage across and current through these diodes D_1 and D_3 are well below the load voltage and load current, hence there are no voltage and current stresses on these devices.



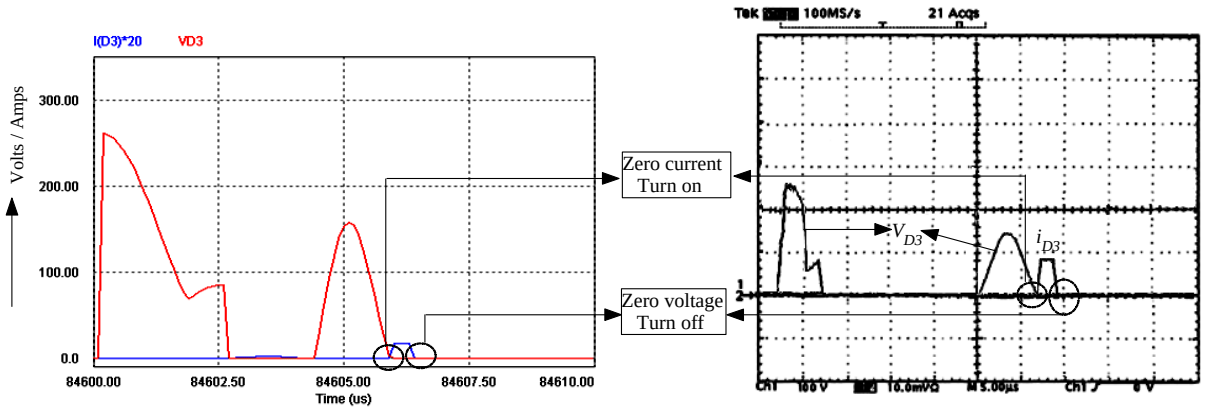
(a) (b)

Fig. 3.11

(a) Simulated voltage and current switching waveforms of auxiliary diode D_1 (*Current signal is magnified by a factor 20)*

(b) Experimental voltage and current switching waveforms of auxiliary diode D_1.

(c) *Scale:* 100 V/div, 2 A/div, 1μs/div



(a) (b)

Fig. 3.12

(a) Simulated voltage and current waveforms of auxiliary diode D_3 (Current signal is magnified by factor 20)

(b) Experimental voltage and current waveforms of auxiliary diode D_3.

Scale: 100 V/div, 1 A/div, 1 μs/div

The other auxiliary diodes D_2 and D_4 conduct for very short duration over a period of switching cycle and it is noticed that these also experience soft switching with the permissible voltage and current ratings in the principle of operation of a proposed converter.

The experimental input voltage and input current waveforms of a proposed soft switched PFC AC-DC converter for an input voltage of 215 V at full load condition are

presented in Fig. 3.13. It is ascertained that, the input current is in phase with input line voltage and the measured value of the THD of input current is found to be 7.7% and its corresponding input PF is 0.997. The Fig. 3.14 shows the experimental set-up of proposed single-phase PFC with passive snubber converter.

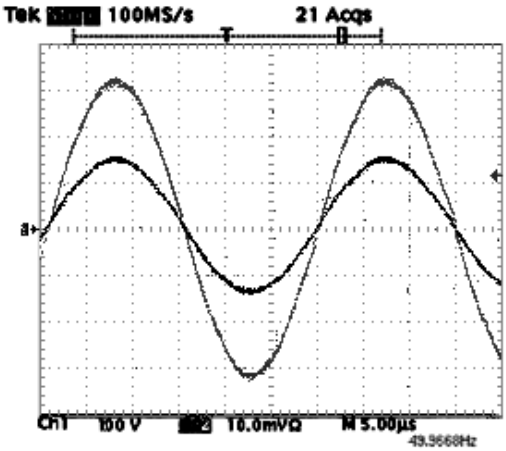


Fig. 3.13 Experimental input voltage input current waveforms of proposed 1-phase PFC AC-DC converter with passive snubber circuit
Scale: Ch1: 100 V/div, Ch2: 2 A/div, 2.2m s.

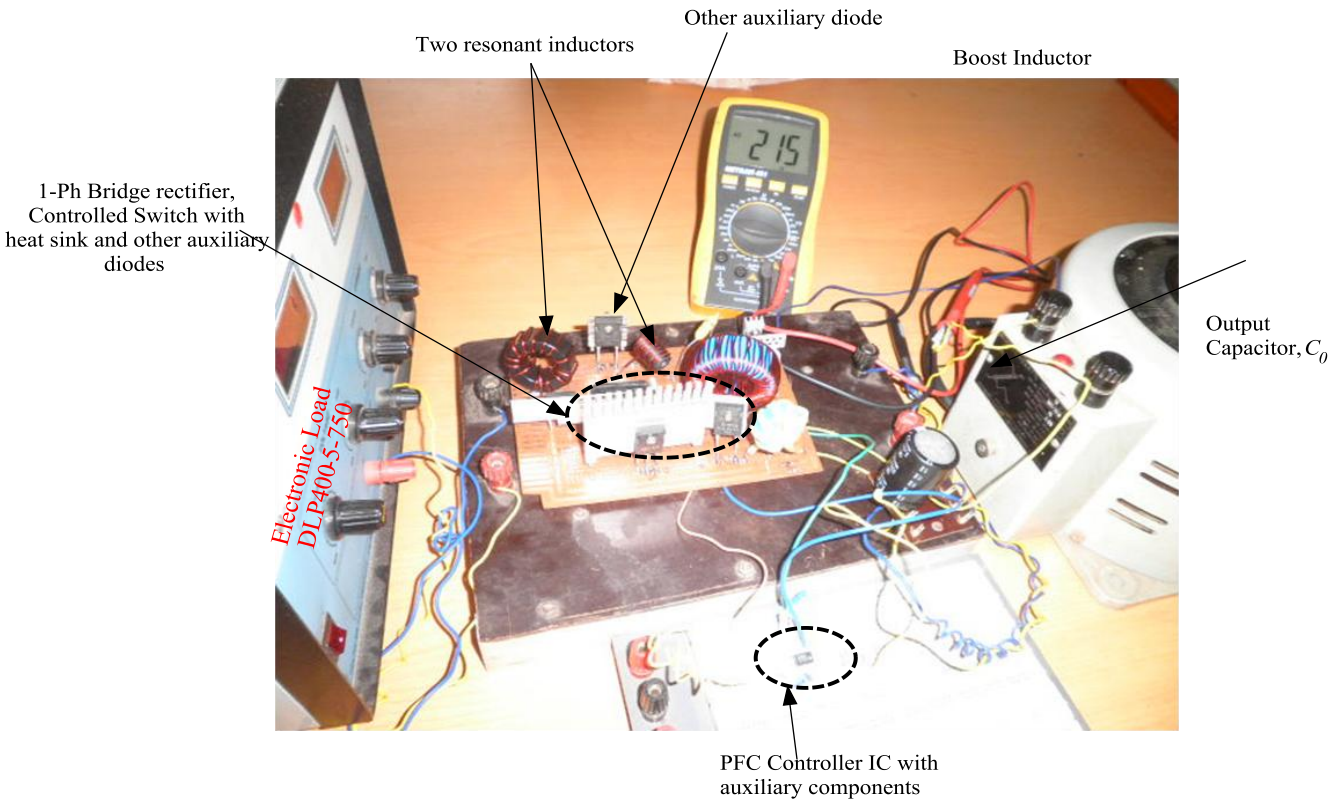


Fig. 3.14 Prototype of proposed 1-phase AC-DC PFC converter with passive snubber circuit

3.5 Comparison of efficiency curves

The comparison of efficiency curves of proposed soft switched PFC boost converter with that of hard switched PFC converter for a nominal input voltage of 215 V is presented in Fig. 3.15. It is observed that the efficiency curve of the proposed soft switched converter is relatively higher than that obtained in the hard switched converter. It can also be observed that, the efficiency of the proposed single-phase soft switched converter varies from 89.5 % to 97.3%. The highest efficiency of the proposed soft switched converter is obtained at full load power of 500 W which is around 6% higher than that of the conventional hard switched PFC converter. It is noted that, the performance of the proposed converter is superior to the converters reported in references [71, 72, 84, 97, 102] with respect to the efficiency parameter. The high efficiency of the proposed converter concludes the correctness of the designed value of components.

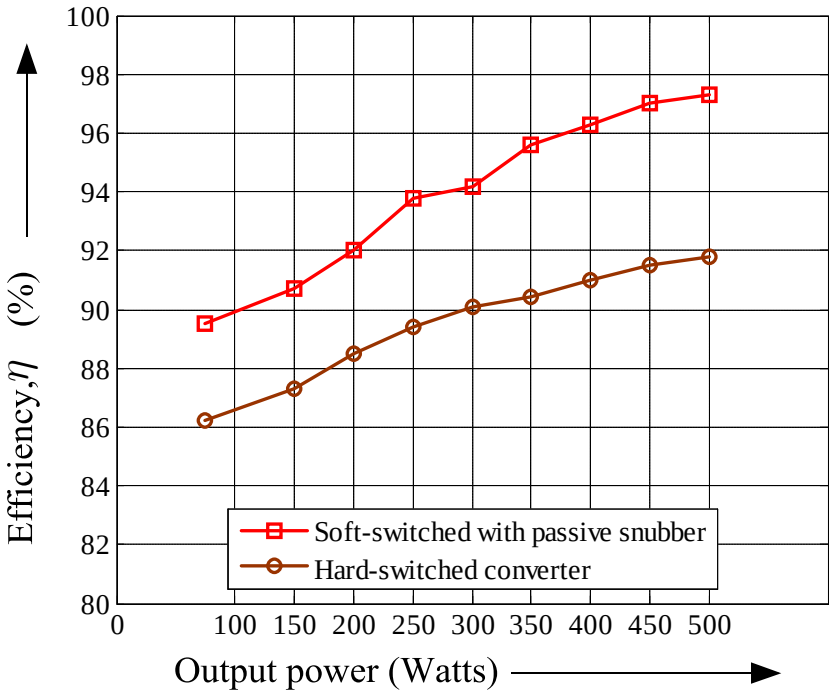


Fig. 3.15 Comparison of efficiency curves of single-phase conventional hard switched PFC converter and proposed single-phase soft switched PFC converter

3.6 Summary

A high power quality single-phase AC-DC PFC boost converter with passive auxiliary circuit for medium and high power applications is proposed in this chapter. The auxiliary passive snubber circuit employed in AC-DC PFC boost converter has been explained with the emphasis on the mathematical and theoretical analysis. The predicted operating modes and simulation results of the proposed converter are confirmed by the comparison of experimental results obtained from a realized prototype of 500 W, 400 V and 100 kHz AC-DC PFC boost converter. All measurement results are carried out briefly on this proposed soft switched PFC boost converter. The maximum efficiency of 97.3% is achieved at full load condition. In the proposed, both the active switch and boost diode are turned on with zero current and turned off exactly at zero voltage. On the other hand, all other semiconductor switches are turned on and off under exact ZVS and/or ZCS. The proposed soft switching PFC converter has achieved nearly unity power factor at full load condition and even at light load condition with low THD.

Chapter 4

Application of novel ZVT to PFC Boost Converter with Active Auxiliary Circuit

- **Introduction**
- **Topology description and PFC feedback system**
- **Operating principle and analysis**
- **Design procedure**
- **Simulation and Experimental results**
- **Performance of proposed converter**
- **Summary**

Introduction

In the previous chapter, soft switching of PFC boost converter with passive auxiliary circuit was discussed. Although this soft switching technique performs well with respect to reliability of the system and efficiency, passive snubber circuits (dissipative circuit consisting of diodes and passive components) shift the switching power loss from the switch to the snubber circuit and therefore may not provide a reduction in the overall switching power loss [15, 76]. The recent soft switching technique with passive snubber proposed in reference [92] however reduces the switching losses but exhibits voltage stress on boost diode of boost converter. This is because; the boost diode voltage is sum of voltages of storage capacitor and one of the auxiliary diodes. Although, some of the soft switching techniques proposed in reference [71, 95, 157, 159-162] can help to minimize switching losses at switching frequencies, they typically experience at least two of the following limitations;

1) Extra voltage stress across the active switch, due to the variation of the voltage across the snubber capacitor during resonance interval. This leads to the additional off-state stress on the active switch.
2) Current stress on the switch, this is because the switch current includes the discharging current of the snubber capacitor and main current flow for energy conversion.
3) Soft switching cannot be ensured at heavy load conditions because the snubber circuit cannot completely reset before the next energy absorbing process.

A relatively simple active snubber circuit consisting of auxiliary switch, resonant elements inductor, capacitor, and auxiliary diodes can overcome the drawbacks of the passive circuit discussed above. With the aim of achieving an improvement in overall performance of PWM DC-DC as well as AC-DC PFC converters, soft switching with active snubber circuits have been subject of intensive research from a couple of decades [73, 97-100, 103, 107, 144,

147]. In addition, it has been reported that soft switching with active snubber circuit techniques provide improved performance with respect to efficiency and EMI of the converter when compared with soft switching techniques with passive snubber circuit [73, 88, 97, 107, 144, 147, 157, 158].

These soft switching techniques with active snubber circuits allow the power converters to operate with higher switching frequencies without penalizing the trade-off between converter efficiency and switching losses. Among all soft switching techniques, the switch commutation under zero voltage transition (ZVT) is better among the best soft switching techniques [113]. A systematic approach to study the synthesis and properties of the generalized form of soft switching with active snubber category of circuits has been presented in [88, 110, 112, 113]. In ZVT technique, a resonant circuit is employed in parallel with the power switch and hence the partial resonance is created by the shunt resonant circuit to achieve ZCS or ZVS during the switching transition only [79].

In this chapter, a novel active snubber circuit is employed in a boost converter of a single-phase AC-DC PFC boost converter to achieve ZVT of an active switch. This proposed circuit not only provides soft switching to main switch, but also provides exact or near zero voltage/zero current switching to auxiliary switch and as well as to other semiconductor diodes. The proposed circuit also provides zero voltage turn off condition to the active switch with extended operating range of load power.

This chapter is organized as follows: Section 4.1 describes the description of the topology of the proposed single-phase AC-DC PFC converter with auxiliary circuit. The mode of operation of each interval and steady state analysis are discussed in section 4.2. Design considerations for practicability of the proposed topology are illustrated in section 4.3. In section 4.4, the special features of the proposed converter are summarized. In Section 4.5 simulation and experimental results are presented to prove the theoretical analysis.

Section 4.6 shows the comparison of efficiency curves of proposed soft switched AC-DC PFC converter with hard switched AC-DC PFC converter for a wide range of output power. Finally important features are summarized in the section 4.7.

4.1 Topology description

Fig. 4.1 shows the proposed single-phase AC-DC PFC soft switched boost converter. This proposed converter is composed of a small EMI filter (L_{in} and C_{in1}) followed by single – phase bridge rectifier, a low value of high frequency bypass capacitor filter C_{in2} and a DC-DC boost converter. SW_1 is the main switch of the boost converter. The active snubber is composed of a snubber capacitor C_B, a resonant inductor L_r, auxiliary switch SW_2 and auxiliary diodes D_1, D_2 and D_3. The active snubber circuit when switched properly ensures lossless switching. The DC output voltage and boost inductor current of proposed converter are sensed accurately and fed to the corresponding feedback system. A continuous conduction mode PFC controller IC ICE2PCS01 is employed which uses ACMC to achieve nearly unity input power factor and to obtain a regulated output voltage [156]. The complete description of PFC feedback system described in section 3.1.2 of chapter 3 is applicable for this proposed AC-DC PFC converter with active snubber. This is because the objective of the feedback system is same for both the converters proposed in chapter 3 and as well as in chapter 4. However, in this proposed soft-switched PFC converter, the generated gating pulses of IC ICE2PCS01 controller are fed to dual driver IC UC3706. This dual driver IC UC3706 provides required alternative gate pulses with adequate dead band to both switches SW_1 and SW_2 of the proposed single-phase AC-DC boost converter. Whereas, in the proposed soft-switched converter presented in chapter 3, does not have IC UC3706 arrangement as that converter has only one active switch, hence, gating pulses of IC ICE2PCS01 are applied to switch *SW*.

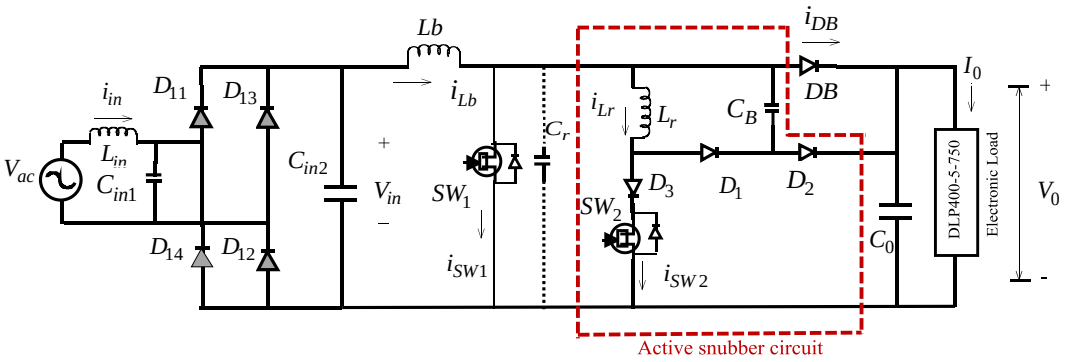


Fig. 4.1 Proposed 1-phase PFC AC-DC boost converter with active snubber circuit

4.2 Operating principle and analysis

To simplify the steady state analysis and operating intervals of the proposed converter, the following conditions are assumed during one switching cycle.

- Semiconductor switches, inductors, and capacitors are ideal.
- The bridge rectifier output voltage V_{in} is constant over a switching period as switching frequency is quite high compared to *AC* input frequency.
- Output filter capacitor C_o is large enough to maintain a constant output voltage V_o.
- The reverse recovery time of diodes D_1, D_2 and D_3 are ignored.

The circuit behavior during one switching cycle can be explained in eight intervals with the help of key/theoretical waveforms shown in Fig. 4.2. The equivalent operating states of the proposed converter shown in Fig. 4.3 are analyzed under steady state condition. The equivalent circuits are described in the following intervals.

Interval 1 (t_0 - t_1): Fig. 4.3(a) shows the operating state of the circuit during this interval. During the time prior to t_0, the switches SW_1 and SW_2 are in off state and the boost diode *DB* is conducting the boost inductor current. At $t=t_0$, the auxiliary switch SW_2 is turned on by applying a gate pulse. The auxiliary switch SW_2 and auxiliary diode D_3 are turned on at ZCS and the resonant inductor L_r limits the rapid rate of rise of current through auxiliary switch SW_2. During this interval, the current in resonant inductor L_r ramps up linearly

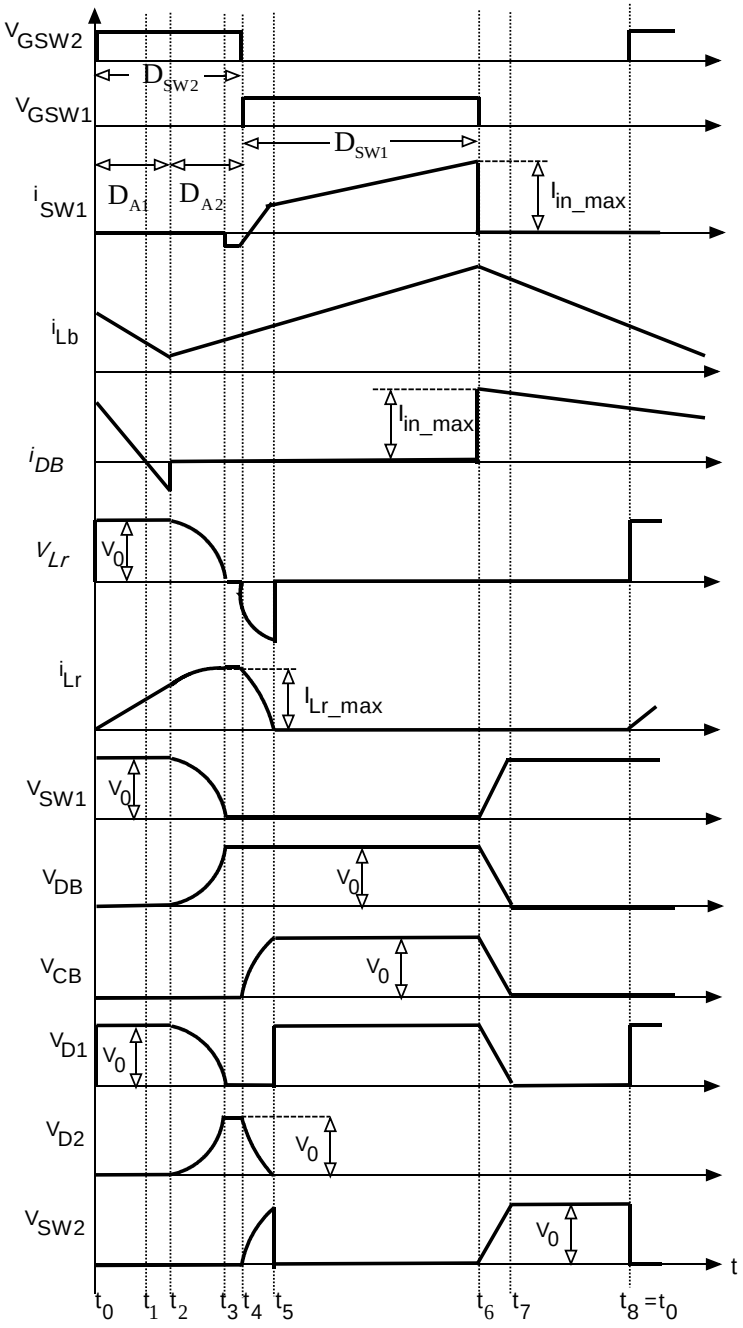


Fig. 4.2 Key waveforms of the proposed soft-switch PFC AC-DC boost converter with active snubber circuit

While the boost diode current i_{DB} ramps down in a complimentary manner. This interval completes when the boost diode current i_{DB} reaches to zero.

During this interval,

$$i_{Lb}(t)=i_{Lb}(t_0)+\frac{(V_{in}-V_0)}{Lb}(t-t_0) \tag{4.1}$$

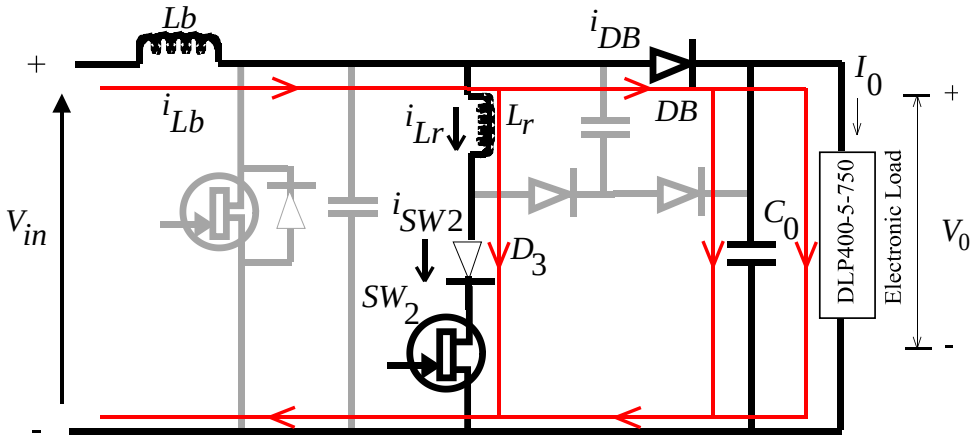


Fig. 4.3(a) Equivalent circuit of converter operation during interval $(t_0\text{-}t_1)$

$$i_{Lr}(t)=i_{sw2}(t)=\frac{V_0}{L_r}(t-t_0) \tag{4.2}$$

$$i_{DB}(t)=i_{Lb}(t_0)-i_{Lr}(t)=i_{Lb}(t_0)-\frac{V_0}{L_r}(t-t_0) \tag{4.3}$$

$$V_{cr}(t)=V_{sw1}(t)=V_0 \tag{4.4}$$

Interval 2 (t_1 – t_2): Fig. 4.3(b) shows the operating state of the circuit during this interval. In this interval, the boost diode current i_{DB} continues to fall in the reverse direction and the resonant inductor current i_{Lr} continues to rise linearly. This can also be referred as reverse recovery interval of boost diode. This interval ends, when the boost diode current i_{DB} reaches its maximum reverse recovery current $-I_{rr}$. Thus the boost diode *DB* turns off under ZVS.

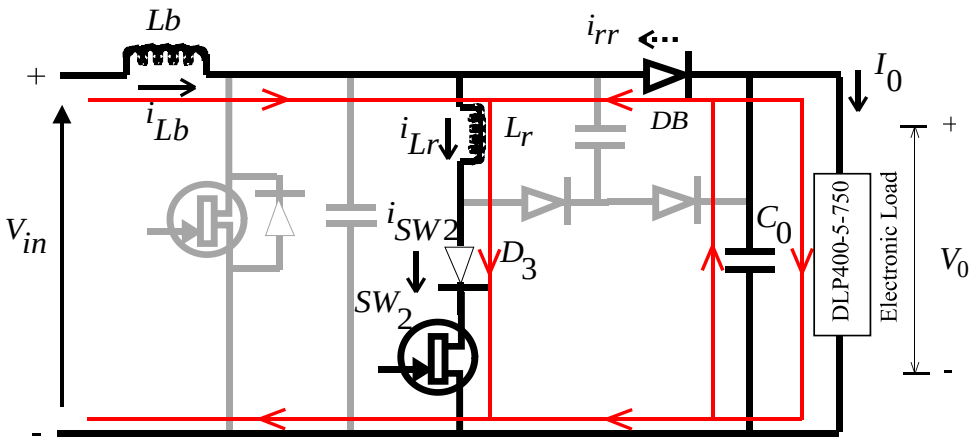


Fig. 4.3(b) Equivalent circuit of converter operation during interval $(t_1\text{-}t_2)$

During this interval,

$$i_{Lb}(t)=i_{Lb}(t_1)+\frac{(V_{in}-V_0)}{Lb}(t-t_1) \tag{4.5}$$

$$i_{Lr}(t)=i_{sw2}(t)=i_{Lb}(t_1)+\frac{V_0}{L_r}(t-t_1) \tag{4.6}$$

$$V_{cr}(t)=V_{SW1}(t)=V_0 \tag{4.7}$$

$$i_{DB}(t_2)=-I_{rr} \tag{4.8}$$

$$t_{12}=t_{rr}=\frac{L_r}{V_0}I_{rr} \tag{4.9}$$

here I_{rr} and t_{rr} are the reverse recovery current and the reverse recovery time of the boost diode *DB* respectively, for the given value of input current of i_{Lb} and $-di/dt = -V_0/L_r$.

Interval 3 (t_2 - t_3): During this interval, the parallel resonance occurs between L_r and C_r as shown in Fig. 4.3(c). A load is supplied by the output capacitor C_o. The energy already stored in the capacitor C_r is transferred to resonant inductor L_r through the resonant path C_r- L_r- D_3-SW_2. Hence, the resonant inductor current rises in sinusoidal fashion from the instant 't_2' and reaches its maximum at 't_3'. During this interval,

$$i_{Lb}(t)=i_{Lb}(t_2)+\frac{(V_{in}-v_{cr})}{L_b}(t-t_2) \tag{4.10}$$

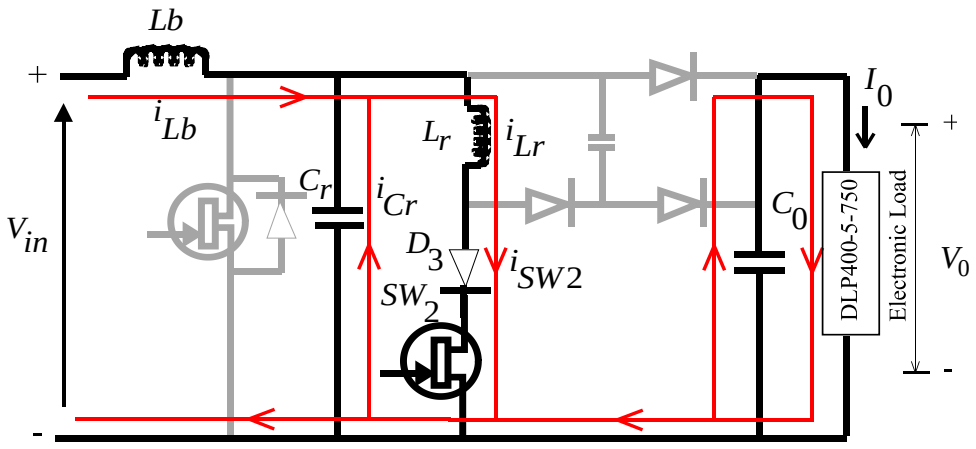


Fig. 4.3(c) Equivalent circuit of converter operation during interval *(t_2-t_3)*

$$i_{Lr}(t) = i_{sw2}(t) = i_{Lb}(t_2) + I_{rr}\cos\omega_1(t - t_2) + \frac{V_0}{Z_1}\sin\omega_1(t - t_2) \tag{4.11}$$

$$V_{cr}(t) = V_{sw1}(t) = V_0\cos\omega_1(t - t_2) - Z_1 I_{rr}\sin\omega_1(t - t_2) \tag{4.12}$$

where $\omega_1 = 1/\sqrt{L_r C_r}$ *and* $Z_1 = \sqrt{L_r / C_r}$.

This interval ends when the total energy stored in capacitor C_r is transferred to resonant inductor L_r and hence the voltage across main switch SW_1 becomes zero at instant 't_3'. At this instant, the resonant current and energy levels of resonant inductor L_r reach their maximum values and hence following equations can be obtained.

$$i_{Lr}(t_3) = I_{Lr\text{-}max} = i_{Lb}(t_2) + \frac{\sqrt{V_0^2 + Z_1^2 I_{rr}^2}}{Z_1} \tag{4.13}$$

$$E_{Lr\text{-}max} = \frac{1}{2}L_r I_{Lr\text{-}max}^2 = \frac{1}{2}L_r [i_{Lb}(t_2) + I_{rr}]^2 + \frac{1}{2}C_r V_0^2 \tag{4.14}$$

During this interval, the parasitic capacitors of switch SW_1 and diode D_1 are discharged from V_0 to zero and the boost diode *DB* and auxiliary diode D_2 are charged from zero to V_0.

Interval 4 (t_3 - t_4): As shown in Fig. 4.3(d), the resonant current which was flowing through C_r, is diverted to body diode of the main switch SW_1 and this body diode SW_{1_D} conducts the excess current of the resonant inductor L_r provided by the input boost inductor current $i_{Lb}(t)$. During this interval,

$$i_{Lb}(t) = i_{Lb}(t_3) + \frac{V_{in}}{Lb + L_r}(t - t_3) \tag{4.15}$$

$$i_{Lr}(t) = i_{sw2}(t) = I_{Lr\text{-}max} \tag{4.16}$$

$$i_{sw1\_D}(t) = I_{Lr\_max} - i_{Lb}(t) \tag{4.17}$$

$$V_{cr}(t) = V_{SW1}(t) = 0 \tag{4.18}$$

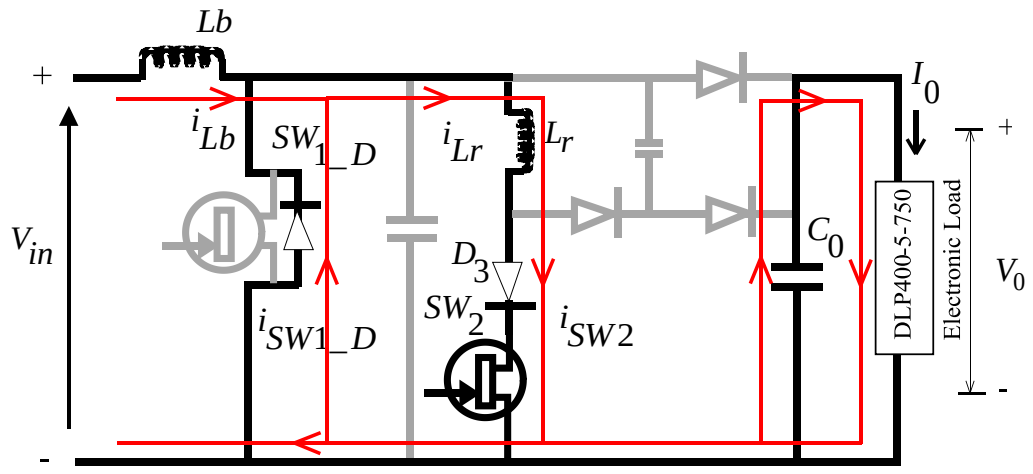


Fig. 4.3(d) Equivalent circuit of converter operation during interval *(t_3-t_4)*

The conduction of body diode SW_{1_D} of main switch SW_1 maintains a zero voltage across the main switch SW_1 and hence provides ZVT for the main switch SW_1. This interval continues until the triggering gate pulse V_{GSW1} is applied to gate of the SW_1.

Interval 5 (t_4 - t_5): Fig. 4.3(e) shows operating state of series resonance interval. The triggering pulse is applied to the main switch SW_1 at instant *'t_4'* and the gate signal of auxiliary switch SW_2 is removed simultaneously. Hence, the main switch SW_1 is turned on with ZVT and the current in boost inductor *Lb* rises linearly and the auxiliary switch SW_2 turned off with near ZVS and its growth of rapid change of drain to source voltage is limited by snubber capacitor C_B. During this resonance period, the energy stored in the resonance inductor L_r is transferred to the snubber capacitor C_B.

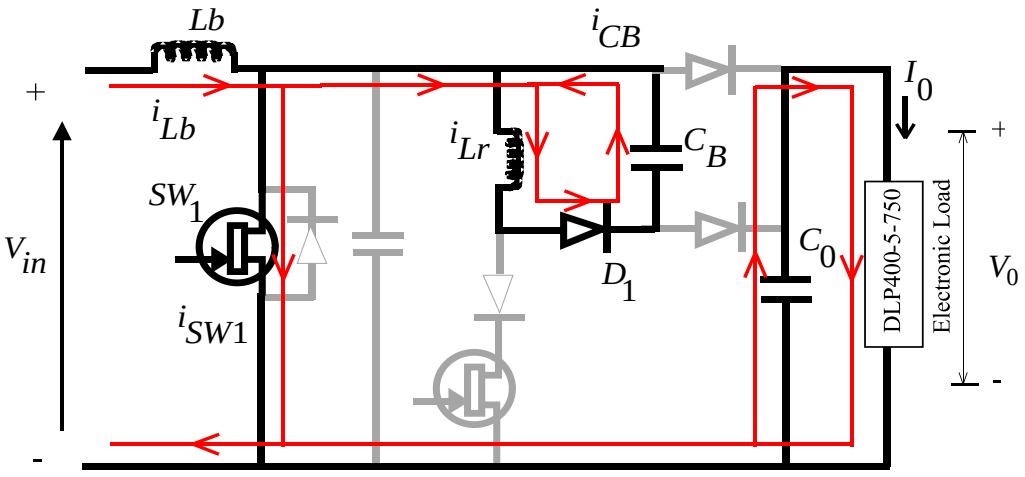


Fig. 4.3(e) Equivalent circuit of converter operation during interval *(t_4-t_5)*

During this interval,

$$i_{Lb}(t)=i_{Lb}(t_4)+\frac{V_{in}}{Lb}(t-t_4) \tag{4.19}$$

$$i_{Lr}(t)=i_{D1}(t)=I_{Lr\text{-}max}\cos\omega_2(t-t_4) \tag{4.20}$$

$$V_{CB}(t)=V_{SW2}(t)=Z_2\,I_{Lr\text{-}max}\sin\omega_2(t-t_4) \tag{4.21}$$

$$V_{cr}(t)=V_{SW1}(t)=0 \tag{4.22}$$

where $\omega_2 = 1/\sqrt{L_r C_B}$ and $Z_2 = \sqrt{L_r / C_B}$.

At the end of this interval, the total energy from resonant inductor L_r is transferred to the snubber capacitor C_B. The energy balance equation is given by,

$$\frac{1}{2}L_r\,I_{Lr\_max}^2=\frac{1}{2}\,C_B\,V_0^2 \tag{4.23}$$

This interval ends when the snubber capacitor voltage V_{CB} reaches V_0 and the resonant inductor current i_{Lr} ceases to zero. As the resonant inductor current i_{Lr} ceases to zero at *'t_5'*, the auxiliary diode D_1 is turned off near ZCS. At the same instant, voltage across switch SW_2 drops abruptly down to zero and may produce oscillations between resonant inductor L_r and output capacitance of the auxiliary switch SW_2 and such oscillations are prevented by auxiliary diode D_3 .

Interval 6: (t_5 - t_6): During this interval, the main switch SW_1 continues to conduct as shown in Fig. 4.3(f). A load is supplied by the output filter capacitor C_0 and the input power is stored in boost inductor L_b. This interval is equivalent to switch-on period of conventional PWM boost converter. In this interval, the active snubber circuit is completely inactive.

During this stage,

$$i_{Lb}(t)=i_{sw1}(t)=i_{Lb}(t_5)+\frac{V_{in}}{Lb}(t-t_5) \tag{4.24}$$

$$i_{Lr}(t)=0 \tag{4.25}$$

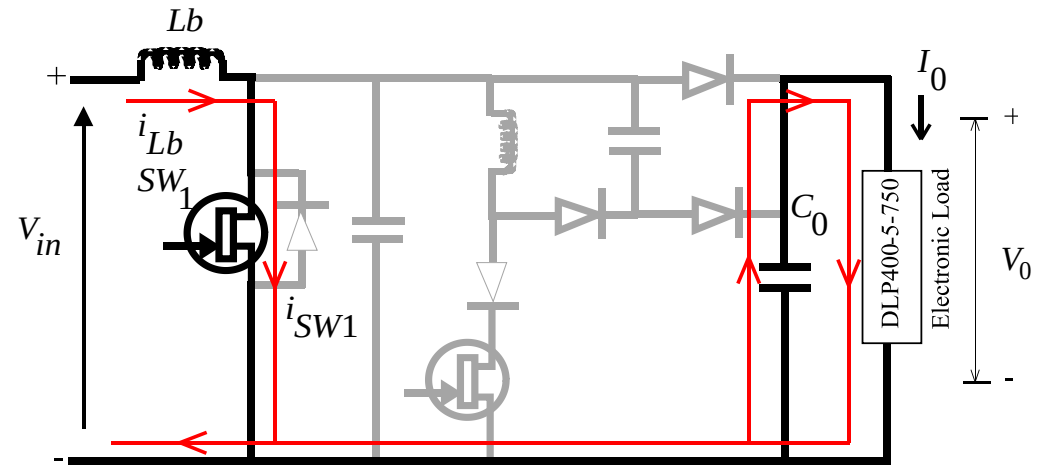


Fig. 4.3(f) Equivalent circuit of converter operation during interval $(t_5\text{-}t_6)$

$$V_{cr}(t) = V_{SW1}(t) = 0 \tag{4.26}$$

Interval 7 (t_6 - t_7): This interval is shown in Fig. 4.3(g). The triggering pulse to the main switch SW_1 is removed at *'t_6'*. Thus, near ZVS turn off of main switch SW_1 is achieved, at the same instant, the auxiliary diode D_2 becomes forward bias due to the boost inductor current i_{Lb} and turns on with ZVS. As the auxiliary diode D_2 is turned on, the snubber capacitor C_B limits the rapid change of drain to source voltage of main switch SW_1. During this interval, the capacitor C_r is charged to output voltage V_0 and the energy stored in the snubber capacitor C_B is released to output capacitor C_0 and hence C_B voltage discharges from V_0 to zero.

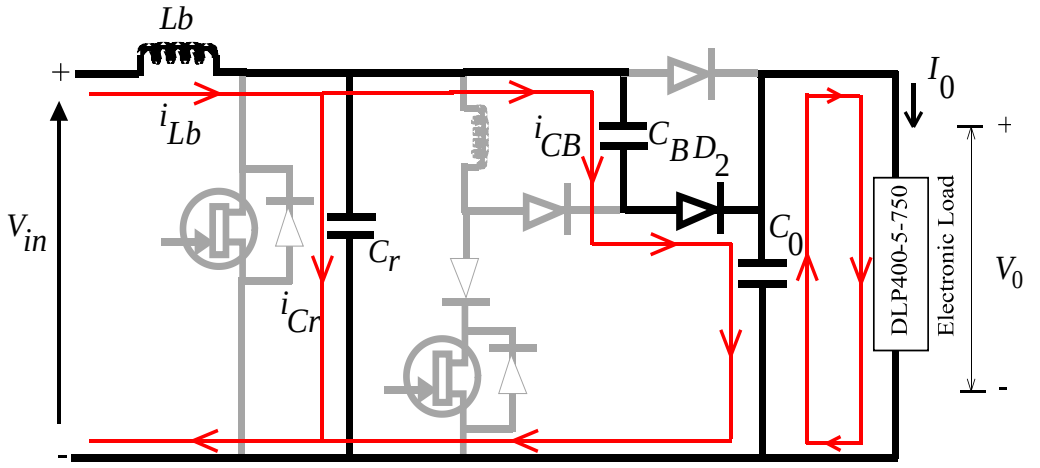


Fig. 4.3(g) Equivalent circuit of converter operation during interval $(t_6\text{-}t_7)$

During this interval,

$$i_{Lb}(t)=i_{Lb}(t_6)+\frac{(V_{in}-V_0-V_{CB})}{Lb}(t-t_6) \quad (4.27)$$

$$i_{Lr}(t)=0 \quad (4.28)$$

$$V_{cr}(t)=V_{SW1}(t)=V_0-v_{CB}(t) \quad (4.29)$$

Interval 8 (t_7 – t_8): Fig. 4.3(h) shows the operating state of the circuit during this interval. In this interval, the boost diode *DB* starts conducting the load current and the boost inductor current starts decreasing. The snubber circuit is not active during this interval. The response of this stage is similar to that of the switch-off period of conventional PWM boost converter.

During this interval,

$$i_{Lb}(t)=i_{DB}(t)=i_{Lb}(t_7)+\frac{(V_{in}-V_0)}{L_b}(1-D_{SW1}-D_{SW2}) \quad (4.30)$$

$$i_{Lr}(t)=0 \quad (4.31)$$

$$V_{cr}(t)=V_{SW1}(t)=V_0 \quad (4.32)$$

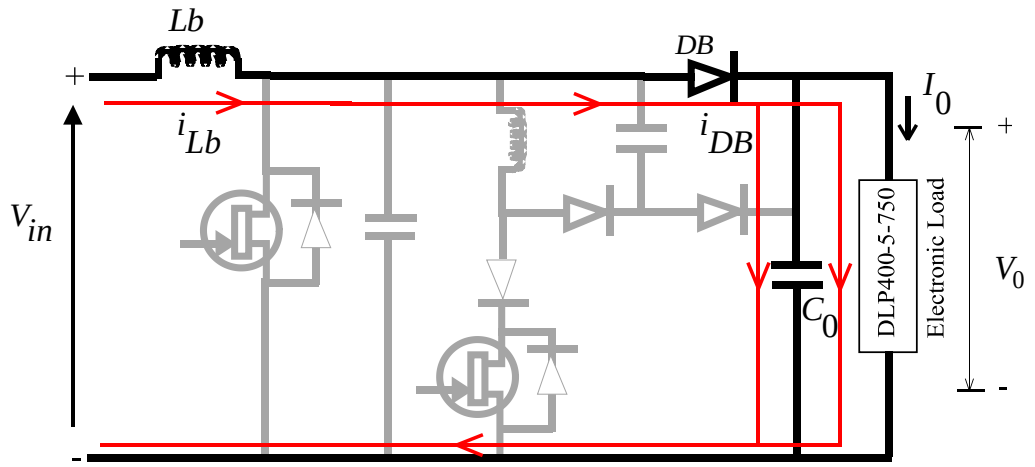


Fig. 4.3(h) Equivalent circuit of converter operation during interval $(t_7\text{-}t_8)$

where D_{SW1} is the duty cycle of the main switch SW_1 and D_{SW2} is the duty cycle of the auxiliary switch SW_2. From Fig. 4.2, D_{SW2} is given by,

$D_{SW2}=D_{A1}+D_{A2}$ (4.33)

here, D_{A1} is the duty cycle for the interval (t_0-t_2) and D_{A2} is the duty cycle for the interval (t_2-t_4). At the instant $t=t_8$, one complete cycle is completed and the next switching cycle is repeated.

4.3 Design procedure

Since, the design example of the conventional hard switched PWM boost converters has been presented in earlier literature and text books; hence, in this thesis the significant importance is given on design example of active snubber circuit components. However, the necessary condition for the output voltage of the proposed PFC boost converter is derived and is same as that of the output voltage equation of the conventional PWM converter. This is because, the ZVT boost converter operates as same as that of a conventional boost converter throughout its switching cycle except during the switch turn-on and turn-off processes. The prototypes of proposed soft-switched PFC converter and as well as hard-switched PFC converter are developed and tested in the Power Electronics and Drvies laboratory, at NIT, Rourkela. Their specifications are identical and are tabulated in the Table 4.1.

Table 4.1 Specification of proposed single phase soft switched and hard switched PFC AC-DC boost converter

Input voltage (V_{ac})	215 V_{RMS}, 50 Hz
Output voltage (V_0)	400 V
Output Power (P_0) (each module)	500 W
Switching frequency (f_s)	100 kHz
Input current peak ripple (ΔI_{Lb})	20 %
Output voltage ripple (ΔV_0)	5 %

4.3.1 Boost converter components

4.3.1.1 Boost inductor Lb

From Fig. 4.2, Neglecting the turn off transition $(t_6 - t_7)$ of switch SW_1, writing voltage-second balance equation of the boost inductor Lb from equations (4.1), (4.5), (4.10), (4.15), (4.19), (4.24) and (4.30); we obtain,

$$\frac{(V_{in}-V_0)}{Lb}D_{A1}+\frac{V_{in}}{L_b+L_r}D_{A2}+\frac{V_{in}}{Lb}D_{SW1}+\frac{(V_{in}-V_0)}{L_b}(1-D_{SW1}-D_{SW2})=0 \quad (4.34)$$

We have, $D_{A1} + D_{A2} = D_{SW2}$, if $Lb >> L_r$, on Simplification of (4.34), we get,

$$V_0=\frac{V_{in}}{[1-D_{SW1}-D_{SW2}+D_{A1}]} \quad (4.35)$$

if $D_{A2} << D_{A1}$,

$$(4.35) \Rightarrow \quad V_0 \approx \frac{V_{in}}{(1-D_{SW1})} \quad (4.36)$$

The above equation (4.36) is identical to the output voltage expression of conventional hard-switched boost converter.

If peak-to-peak ripple current of the boost inductor $Lb=\Delta I_{Lb}$,

Then $\Delta I_{Lb} \approx i_{Lb}(t_6)-i_{Lb}(t_2)$ (4.37)

Neglecting duty cycle D_{A2}, we obtain,

$\Delta I_{Lb} \approx (V_{in}/Lb)\, D_{SW1}\, T$ (4.38)

From (4.36) and (4.38),

$\Delta I_{Lb} \approx (V_0/Lb)\,(1-D_{SW1})\, DSW1\, T$ (4.39)

$$\therefore \quad Lb \approx \left(\frac{V_o}{(\Delta I_{Lb})\,(f_s)}\right)(1-D_{SW1})\, D_{SW1} \quad (4.40)$$

Where $f_s = 1/T$, switching frequency of the converter.

Lb will be maximum for $D_{SW1} = 0.5$. Hence, Lb should be greater than the value calculated in (4.40) at $D_{SW1}=0.5$; therefore, minimum value of boost inductor (Lb_{min}) is

$$Lb_{\min} = \frac{V_0}{4(\Delta I_{Lb})\,(f_s)} \tag{4.41}$$

From the specification of the soft-switched proposed converter, the computation of value of boost inductor '*Lb*' is found to be 1.5 *mH*. This boost inductor is fabricated from a sendust toroidal core (part number – CS468125, CWS make) having 38 single layer turns of 13 AWG is used.

4.3.1.2 Output Capacitor C_0

The converter hold-up time and ripple of output voltage are influenced by the value of output capacitor. In this design, the criterion for selection of this capacitor is based on the amount of tolerable ripple in the output voltage V_0 is considered and is given by,

$$C_{o(\min)} \geq \frac{P_{out}/V_0}{(2\pi)\,f_r\,(\Delta V_0)} \tag{4.42}$$

where f_r is the frequency of the rectified sine wave and ΔV_0 is the output voltage ripple in terms of percentage. Considering the all above factors, the output capacitor of value 450 μF, 600 V is selected.

4.3.1.3 Active snubber circuit components

A widely used method presented in [99, 100, 102] is applied to design active snubber components to achieve proper ZVT and soft-switching to other semiconductor devices. The component values and devices of the proposed soft-switched single-phase PFC AC-DC converter are tabulated in Table 4.2.

The base values were selected as

Base Voltage V_0 = 400 V (4.43)

Base Current $I_b = I_{Lb\_max} - (\Delta I_{Lb})/2$ (4.44)

Where $I_{Lb\_\max} = \frac{\sqrt{2}\left[\frac{P_o}{\eta}\right]}{V_{in\_RMS\,(min)}} = \frac{\sqrt{2}\left[\frac{500}{0.99}\right]}{90} = 7.93\ A$ (4.45)

$$\Delta I_{Lb} = I_{Lb\_\max}\ (20\%) = (7.93)\ (0.20) = 1.6\ A \tag{4.46}$$

$$I_b = I_{Lb\_\max} - \frac{(\Delta I_{Lb})}{2} = 7.93 - \frac{1.6}{2} = 7.13\ A \tag{4.47}$$

Table 4.2 Parameter set employed in the evaluation tests of the soft switched active PFC converter

Parameter	**Device number/Value**
Four Rectifier diodes (to form bridge)	25NSFL
MOSFETs (SW_1, SW_2)	IRFP 460
Hyper fast diode (DB)	DSEI 30-12A
Auxiliary diodes, (D_1, D_2 & D_3)	RHRP 3060
Low line filter inductor (L_{in})	5.6 μH
Input filter (C_{in1})	0.47 μF, 275 V
Input HF bypass capacitor (C_{in2})	1 μF, 630 V
Boost inductor (Lb)	1.5 mH
Resonant inductor (L_r)	10 μH
Snubber capacitor (C_B)	5.6 nF, 400 V
Output capacitor (C_0)	450 μF, 600 V

4.3.1.3.1 Resonant inductor L_r

The value of L_r mainly depends on how fast the reverse recovery current of boost diode DB reaches its zero value. Due to production spread of the diodes and the circuit conditions, the reverse recovery characteristics may vary for different diodes. For this, a beneficial characterization is to set the time it takes for the resonant inductor current i_{Lr} to slew from zero to the maximum boost diode current equal to three times the diode's specified (by manufacturer) reverse recovery time. Assuming the maximum value of reverse-recovery time (t_{rr}) of selected boost diode DB to be 60n sec,

$$L_r = \frac{V_0}{I_{Lb\_\max}} 3\, t_{rr} = \frac{(400)}{7.93}\,(3)\,(60)(10^{-09}) \tag{4.48}$$

Therefore, minimum value of L_r required is,

$$L_r = 9.08\ \mu H \tag{4.49}$$

Resonant inductor 'L_r' is fabricated by a sendust toroidal core (part number – CS234125, CWS make) having 12 single layer turns of 14 AWG. Both the cores (*Lb* and L_r) employed in the proposed soft switching converter exhibit low loss, high flux density as well as relatively high saturation level.

4.3.1.3.2 Snubber Capacitor C_B

The snubber capacitor C_B is selected based on the complete energy transfer from resonant inductor L_r to snubber capacitor C_B. It is also essential to have a selected snubber capacitor C_B to be larger than that of resonant capacitor C_r to ensure complete discharge of the resonant capacitor during resonant interval. Otherwise, the larger value of the resonant capacitor increases the minimum duty cycle and hence the increased conduction losses in the converter. Based on energy transfer balanced equation, from (4.14) and (4.23), we obtain,

$$\frac{1}{2}L_r\,[i_{Lb}(t_2)+I_{rr}]^2+\frac{1}{2}C_r V_0^2 \approx \frac{1}{2}C_B V_0^2 \tag{4.50}$$

$$\frac{1}{2}\,(9.08)(10^{-6})\,[7.13+2]^2+\frac{1}{2}\,(480)\,(10^{-12})\,(400)^2=\frac{1}{2}\,C_B\,(400)^2 \tag{4.51}$$

$$\therefore\quad C_B = 5.21\ nF \tag{4.52}$$

here $i_{Lb}(t_2) = I_b$ base current value calculated in equation (4.47) and the peak reverse recovery current I_{rr} is found from the manufacturer's data sheet of employed boost diode *DB* for a given maximum forward current of the converter. The other advantage of this proposed AC-DC PFC boost converter is that, it is not required to have extra component of resonance capacitor C_r across the main switch SW_1 of the boost converter, however, the output capacitance of main switch SW_1 will serve the purpose of resonant capacitor and its value is considered from the manufacturer's data sheet of the switch SW_1.

4.3.1.3.3 Verification of selected auxiliary components

In interval 5, according to (4.21), if the value of C_B is decreased, voltage stress across SW_2 will increase. Hence to limit the *dv/dt* of the switch SW_2, the following condition is to be satisfied,

$$t_{45} = \pi/2 \left(\sqrt{(L_r)(C_B)}\right) \geq t_{f2} \tag{4.53}$$

$$\therefore \qquad t_{45} = \pi/2 \left(\sqrt{(9.08\mu)\ (5.25n)}\right) = 342.9\ ns \geq t_{f2} \tag{4.54}$$

In interval 7, the rate of rise of voltage across the main switch SW_1 is limited by snubber capacitor C_B, hence the discharge time of snubber capacitor during this interval should satisfy the following condition,

$$t_{67} = \frac{C_r + C_B}{I_{Lb\_\max}} (V_0) \geq t_{f1} \tag{4.55}$$

$$\therefore \qquad t_{67} = \frac{[(480)(10^{-12}) + (5.21)(10^{-09})]}{7.93}(400) = 287\ ns \geq t_{f1} \tag{4.56}$$

here, $t_{f1}$and t_{f2} are fall time ratings of the main switch SW_1 and auxiliary switch SW_2 respectively, whose worst case maximum value is found to be 98*n* sec of the switching devices employed in the proposed converter.

4.4 Special features of the proposed converter

The proposed single-phase AC-DC PFC boost converter is incorporated with ZVT based active snubber circuit which achieves advantages over other soft switching converters. The features of the proposed soft switched AC-DC converter are briefly summarized as follows:

1) All semiconductor devices operate with soft switching in the proposed converter. The main switch SW_1 is turned on with exact ZVT and is turned off near ZVS, the auxiliary switch SW_2 is turned on with ZCS and is turned off near ZVS. Other semiconductor devices of the proposed converter also operate with soft switching.

2) There is a little extra voltage stress on the boost diode of *DB* of single-phase AC-DC PFC boost converter with passive snubber circuit proposed in chapter 3 of this thesis. This extra voltage stress on the boost diode *DB* is eliminated in this proposed AC-DC PFC converter with active snubber circuit.

3) There is no extra voltage stress on the auxiliary switch SW_2 of this converter. Based on the energy balance condition, resonant current flows through auxiliary switch. So, there is less current stress on the auxiliary switch with acceptable levels. The voltage and current levels of auxiliary diodes D_1, D_2 and D_3 are within the permissible limits.

4) There is no current stress in the main switch SW_1 and its body diode of the proposed soft switched PFC boost converter. But the main switch of similar topology of DC-DC converter described in [112] is subjected to undergo additional current stress and strain. This extra current stress of main switch in [112] occurs as the body diode of main switch conducts twice in each switching cycle with abrupt change in current.

5) No input voltage sensing is required as it is needed in other active PFC converters presented in [33, 84, 91, 95, 99, 121, 126, 127].

6) The efficiency is higher even at lighter loads when compared to DC-DC converter proposed in [97] as there is no energy loss (due to absence of resonant diode) during resonance intervals.

7) At light load conditions, the on state time of the main switch's body diode is increased when the input current is decreased. However, turn off process of main switch with ZVT will not be affected under these conditions.

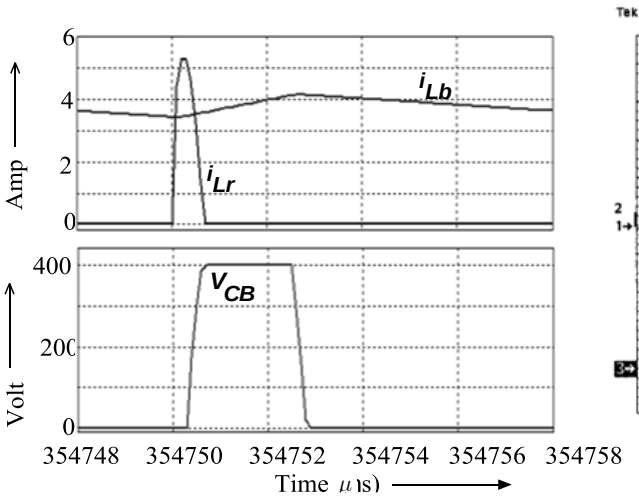
4.5 Simulation and experimental results

In simulation, a feedback system has been developed in *SIMULINK* environment and is linked with a power converter which is developed in Power-Sim (PSIM) Power electronics and Drives simulation package. The two models (boost converter and feedback system) built

in different environment are coupled by SIMCOUPLER. The single-phase AC-DC soft switched PFC boost converter shown in Fig. 4.1 is tested with the implementation of an experimental prototype on the electronic load DLP-400-5-750 (From ALLTEST Instruments), and the performance efficiency of the proposed converter is compared with that of the conventional hard-switched single-phase AC-DC PFC converter.

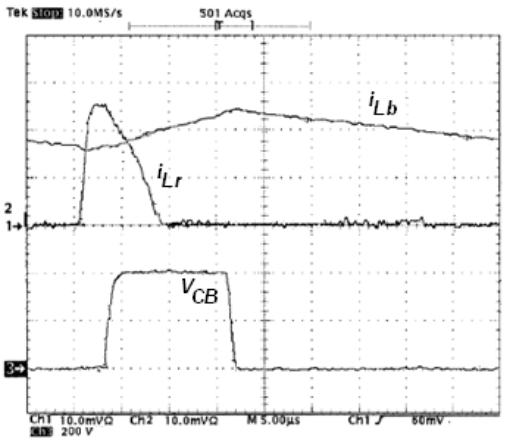
4.5.1 Response of resonant elements

Fig. 4.4 shows the comparison of simulated and experimental waveforms of resonant inductor current i_{Lr}, boost inductor current i_{Lb}, and snubber capacitor voltage V_{CB} at full load condition. It can be observed that, the experimentally obtained waveforms shown in Fig. 4.4(b) are closer to that obtained in simulation. This is a proof of evidence that, the simulation and experimental results are strongly agreed with the theoretical designed analysis of the operating principle of the proposed converter.



(a) Simulation waveforms

Top: Resonant inductor current (i_{Lr}), and boost inductor current (i_{Lb})
Bottom: Snubber capacitor voltage (V_{CB})



(b) Experimental result waveforms

Scale: 2A/div, 200 V/div, 1 μsec/div

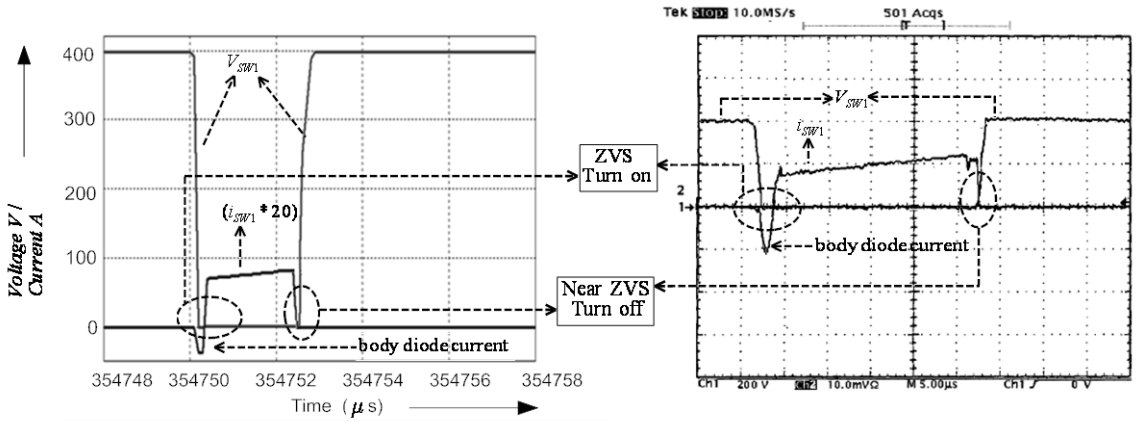
Fig. 4.4

4.5.2 Main switch SW_1

Fig. 4.5 shows the simulation and experimental switching waveforms of main switch SW_1 of the proposed soft-switched converter at full load condition. The main switch SW_1 is

turned on under exact ZVT when voltage across C_r is zero and it can be observed that the switch has not exceeded its voltage and current limits.

The main switch SW_1 also turns off under near ZVS. The current and voltage waveforms obtained through simulation and experimental investigations are in close agreement with theoretical analysis.



(a) (b)

Fig. 4.5 Simulation and experimental switching characteristics of a main switch SW_1
a) *Simulated results:* voltage and magnified current waveforms of SW_1.
b) *Experimental results:* voltage and current waveforms of SW_1. *Scale:* 200 V/div, 2 A/div, 1 µs/div.

4.5.3 Auxiliary switch SW_2 and boost diode DB

The simulation and experimental switching waveforms of auxiliary switch SW_2 and boost diode DB at full load condition are presented in Fig. 4.6. It can be observed that, from Fig. 4.6 (a) and Fig. 4.6 (b), the auxiliary switch SW_2 is turned on with ZCS because of resonant inductor L_r and turns off under ZVS when the resonant current flowing through L_r and C_r ceases to zero. The auxiliary switch SW_2 is active only for a short period of time, which is verified by its conduction period and is too small. It is also noted that, there is no voltage oscillations across the switch SW_2 just after the turn-off process of an auxiliary switch SW_2. But, such oscillations across auxiliary switch are occurring in the converter topology depicted in the reference [97]. This is due to the relationship between resonant inductor L_r and output capacitance C_{oss} of an auxiliary switch SW_2. This oscillation is prevented by an

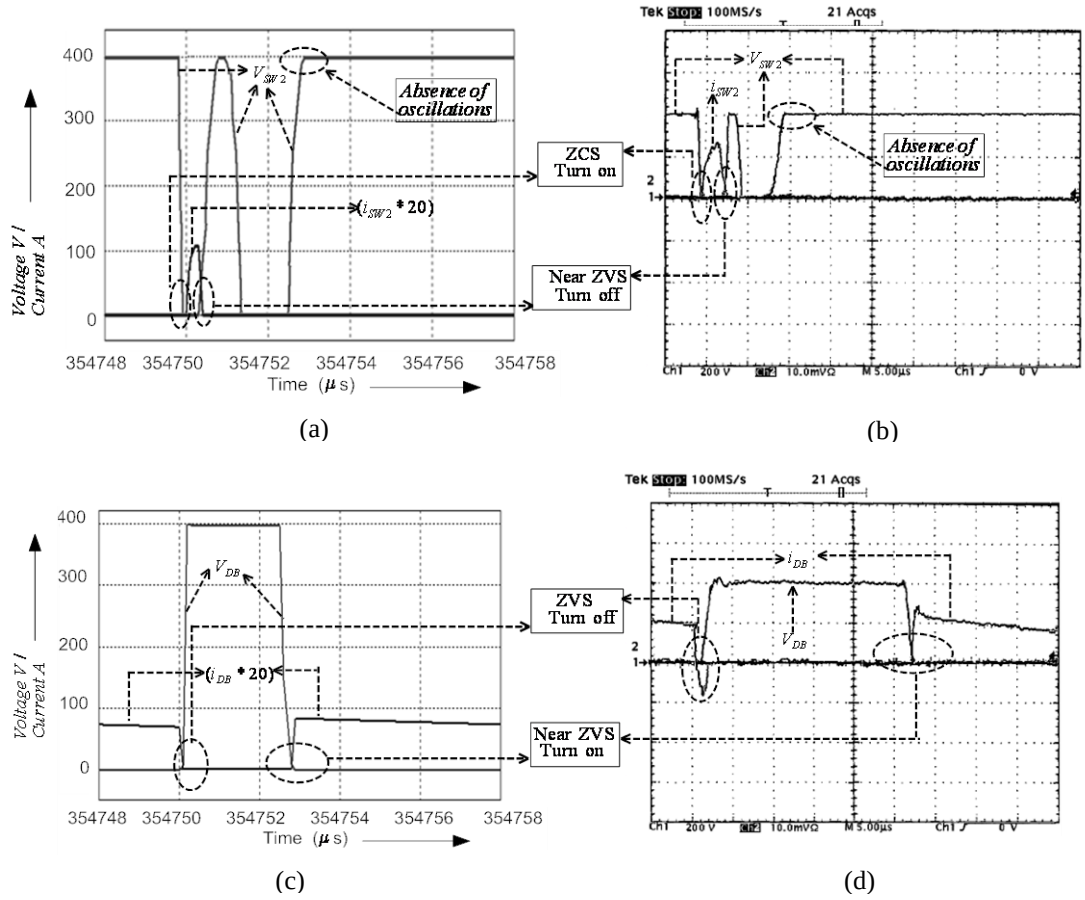


Fig. 4.6 Simulation and experimental switching waveforms of auxiliary switch SW_2 and boost diode *DB*

Simulation waveforms: ***Experimental waveforms:***

(a) Voltage and magnified current waveforms of auxiliary switch SW_2. (b) Voltage and current waveforms of SW_2

(c) Voltage and magnified current waveforms of boost diode *DB.* (d) Voltage and current waveforms of *DB.*

Scale: 200V/div, 2 A/div, 1 µs/div.

auxiliary diode D_3 connected in series with auxiliary switch SW_2 of a proposed converter. Also the current and voltage stresses of an auxiliary switch SW_2 are well within in the permissible limits. The switching waveforms of boost diode *DB* are presented Fig. 4.6 (c) and (d). The boost diode *BD* also turns-on and off under ZVS. The experimentally obtained results are almost closer to simulation results of the boost diode *DB*, except that in Fig. 4.6(c) absence of reverse recovery current in boost diode *DB* as discrete transition simulators like PSIM don't apply full physical model of device and as a result such simulators are incapable of showing parasitic processes such as reverse recovery. A high frequency hyper-fast recovery diode is used as a boost diode in the proposed converter. The reverse recovery current which exists for shorter period may lead to substantial increase in conduction losses

of main switch SW_1. However such losses due to reverse-recovery current can be eliminated in future of similar projects by employing silicon carbide diodes which are now available in the market. The all auxiliary diodes D_1, D_2 and D_3 conduct for very short intervals over a period of switching cycle and it is also noticed that these also experience soft switching processes with the permissible voltage and current ratings in the principle of operation of a proposed PFC converter with active snubber circuit.

The simulation and experimentally obtained input voltage and current waveforms of a proposed PFC converter with active snubber for an input voltage of 215 V at full load condition are presented in Fig. 4.7 and Fig. 4.8 respectively. The experimentally obtained input voltage and current waveforms are measured and recorded by CW240 Clamp-on Power Meter in the laboratory. The screen (LCD-liquid crystal display) of this meter displays only horizontal grid lines. From both the figures (Fig. 4.7 and Fig. 4.8), it is ascertained that, the input current signal is in phase with the input line voltage. This confirms the quality of input line current which is almost sinusoidal and correctness of derived equation (4.36) which is essential for boost converter of proposed active snubber topology.

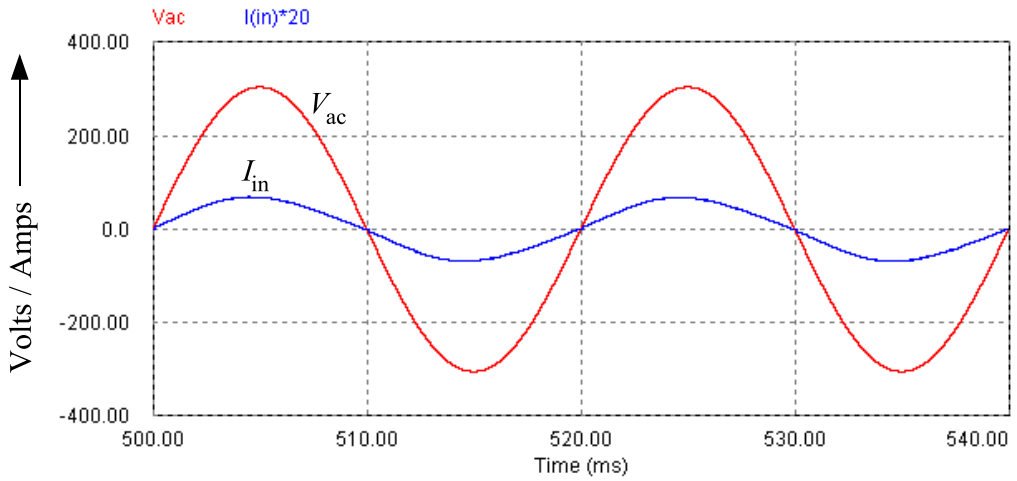


Fig. 4.7 Simulation results of input voltage and magnified input current waveforms of proposed converter with active snubber for an input voltage of 215 V_{RMS}

This proof affirms that the proposed active snubber topology provides near unity power factor operation and is perfectly suitable for PFC applications. The value of the THD of input current is found to be 4.2% and its corresponding input PF is 0.999.

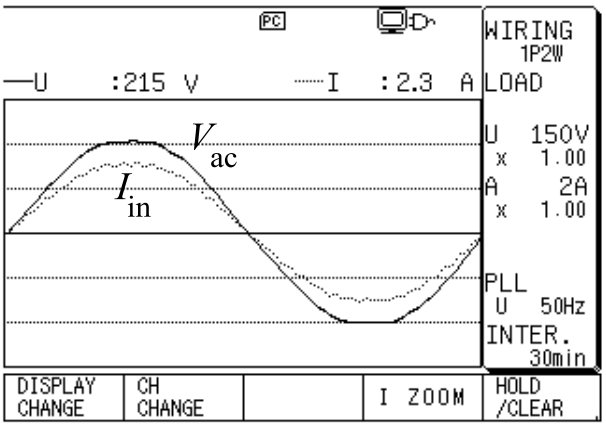


Fig. 4.8 Experimental input voltage and input current waveforms of proposed single-phase PFC AC-DC converter with active snubber circuit for an input voltage of 215 V_{RMS} .

4.6 Performance of proposed converter

The performance of a proposed converter can be analyzed by comparing the efficiency curve with that of the other converter efficiency curves. Fig. 4.9 shows the comparison of efficiency curves with respect to the output load of all the three converters namely, (1) soft switching with auxiliary snubber circuit, (2) soft switching with passive snubber circuit and (3) hard switching of conventional PFC converters. Among all the three methods, the converter proposed with active snubber circuit achieves a maximum efficiency of 98.3% which is around 1.02% more than that of a soft switching converter with passive auxiliary circuit and 7.08% higher than the conventional hard switched PFC converter at full-load condition. The improvement of efficiency of proposed PFC AC-DC converter with other converters at low load condition (15% of full-load) is also expressed in Fig. 4.9. The

proposed converter has a higher efficiency compare to the converters proposed in references [71, 73, 74, 76, 92, 97, 178].

The higher efficiency in PFC converter with active snubber circuit is because of the perfect soft-switching processes of semiconductor devices in comparison with PFC converter with passive snubber circuit. In addition to this, the PFC AC-DC converter with passive snubber circuit has more number of resonant elements (almost twice that of resonant elements in active snubber circuit), which leads to the substantial increase in conduction losses and significant effect of parasitic elements. On the other hand, PFC AC-DC converter with passive snubber circuit with its higher component count and design simplicity still make it competitive, when compared to the ZVT PFC AC-DC converter with an active snubber circuit. The variation of PF and THD with respect to output load for all the converters discussed so far will be elaborated in three-phase systems (chapter 5) of this thesis. The Fig. 4.10 shows the experimental set-up of proposed single-phase PFC AC-DC converter with an active snubber circuit.

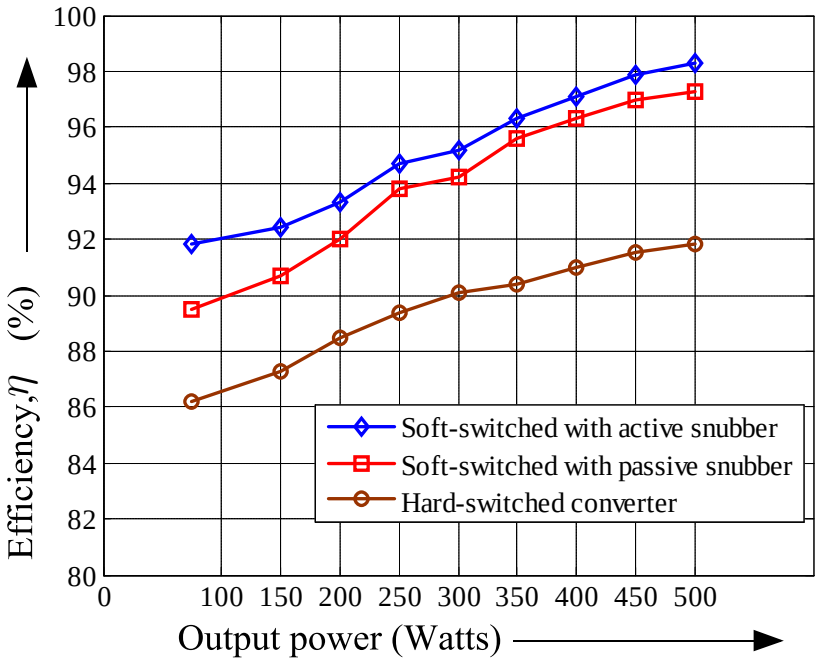


Fig. 4.9 Comparison of efficiency curves of conventional hard switched PFC converter, soft switched PFC converter with passive snubber and proposed soft switched converter with active snubber circuit

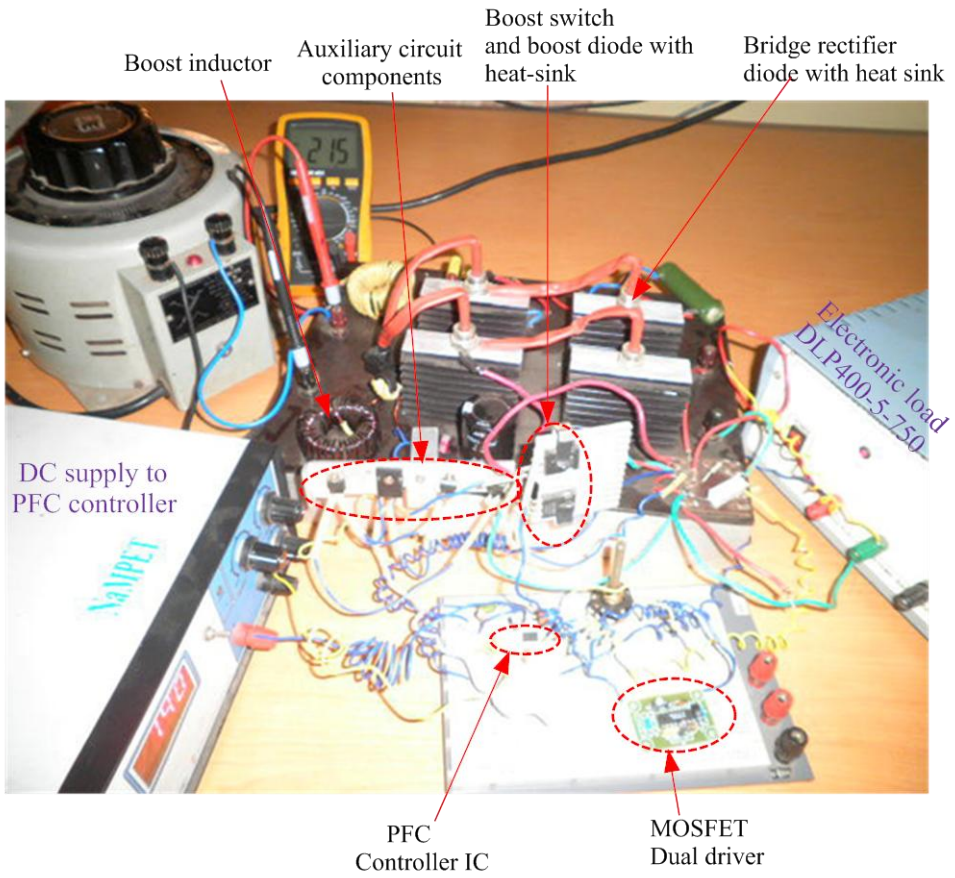


Fig. 4.10 Hardware prototype of single-phase PFC boot converter with an active snubber circuit

4.7 Summary

A novel auxiliary snubber circuit is incorporated in the boost converter of single-phase PFC AC-DC converter to improve the performance with respect to the efficiency of the converter. The main idea is to reduce the switching losses by achieving a process of soft switching in a main switch of boost converter and as well as in other semiconductor devices in the converter. In this technique, the snubber energy is recuperated to the load without using the main switch path; hence the conduction loss of the system is reduced. In the proposed topology, the main switch is turned on with exact ZVT and is turned off near ZVS. The boost diode turns on and off with ZVS. There are no extra voltage stress and current strain on the main switch and as well as on the boost diode. An auxiliary switch SW_2 is

turned on with ZCS and is turned off near ZVS due to the resonant elements resonant inductor L_r, resonant capacitor C_r and snubber capacitor C_B. The excess voltage on an auxiliary switch does not take place, but based on the energy balance condition, resonant current flows through auxiliary switch. Hence, there is less current stress on the auxiliary switch which is within the acceptable levels. All other auxiliary diodes are turned on and turned off under/near ZVS and/or ZCS. The voltage and current stress and strain on all other auxiliary diodes are within the permissible limits. A prototype suitable for input voltage of 215 V_{RMS} with a specification of 400 V, 500 W and 100 kHz converter is developed and tested in the Power Electronics and Drives laboratory to verify with the simulation result.

Chapter 5

High Power Factor Three-Phase Soft-Switched AC-DC PFC Converters in Modular System

- **Introduction**
- **1.5 kW 3-phase PFC boost converter with passive snubber in modular system**
- **Simulation and experimental results**
- **1.5 kW Three-phase PFC boost with active snubber in modular system**
- **Simulation and experimental results**
- **Performance characteristics**
- **Summary**

Introduction

With the development of telecom and information technology sector, the power supply industries are under constant pressure of developing front-end AC-DC PFC converter with low volume, higher efficiency, lower profile, less cost. In addition to these factors, expandability of power range for a given high power specification of converter is also a challenging task. This chapter finds a suitable solution for high power rating converter that expands power range of a converter system in modular approach. A systematic modular approach also provides higher power density, easier thermal management and high reliability of a system. The research effort is focused on the development of the university level prototypes of three-phase AC-DC soft-switched PFC converters each of power rating 1.5 kW.

In the previous chapters of this thesis, importance was given to the improvement of dynamic response and efficiency of single-phase AC-DC PFC boost converters for medium power (500 W) applications. Two different soft switching techniques were proposed and described to improve the efficiency of single-phase AC-DC PFC boost converters.

For high power AC-DC applications, three-phase power supplies are widely employed in various applications including power sources to telecom and computer server systems. In case of three-phase AC-DC converters, there are typically two configurations: (1) A group of three single-phase PFC rectifiers (referred as three-phase AC-DC modular system) and (2) A three-phase PFC rectifiers. The latter rectifiers have distinctive features over the former, such as constant power flow which allows use of smaller capacitors, fewer switches and higher efficiency due to reduced switching and conduction losses [163]. However, the modular system (parallel operation of two or more modules) of three-phase PFC rectifiers can expand the power range to a much higher level and permits to use ($n+1$) modules (n is required number of

modules) for the redundancy purpose in order to improve the system reliability. Added to this, modular system is superior with respect to thermal management, maintainability, cost, requirement for maintenance and repair of power converter modules because of the use of standard single-phase converters [7, 12, 163]. Hence, active PFC AC-DC front-end converters of DPS have been attracting increased attention due to continuously growing power quality concerns. Therefore, single-phase parallel configurations with AC-DC PFC boost, SEPIC and CUK converters have been developed and reported in the references [84, 164, 165, 166]. A great amount of work has been reported concerning the three-phase PWM boost [84, 121, 167-169], buck [170, 171], buck-boost [172] converters for various power supply applications. Either of these converters often requires either input voltage and/or output safety isolation transformations and also provides a unity input power factor, limited input harmonic currents fed-back to AC power grid, high efficiency and high power density. One of the main drawbacks found in earlier years of the three-phase modular approach is the interference of the phase currents between two phases, this is instanced by the authors in the reference [121], however, in the proposed converter of this chapter, this draw back has been overcome by employing individual control loop to each module and such modular systems have been well presented in [84, 120, 167].

The main objective of this chapter is to achieve power range expandability of PFC front-end converter in modular approach and the aim of this chapter is to show the improvement in the performance characteristics of three-phase AC-DC PFC converter in modular system. The significance importance is given to improve the efficiency by minimizing the switching losses of the PFC boost converter by employing passive snubber circuit and active snubber circuit separately. In this chapter, two different soft-switching techniques in three-phase PFC boost converters in modular approach are presented and described separately. The two soft-switching

techniques; PFC with passive snubber and PFC with active snubber circuits already applied in single-phase AC-DC PFC boost converters in chapter 3 and chapter 4 respectively of this thesis are now applied to three-phase AC-DC PFC boost converters in modular system. Hence, this chapter mainly has two parts: 'Section 5.1' deals with the application of soft-switching technique with passive snubber circuit in three-phase AC-DC PFC boost converter and 'Section 5.3' deals describes about the application of soft-switching technique with active snubber circuit employed in three-phase AC-DC PFC boost converter in modular approach.

5.1 A 1.5 kW three-phase AC-DC PFC boost converter with passive snubber circuit in modular system

Fig. 5.1 shows the three-phase AC-DC PFC boost converter with passive snubber circuit schematic with simplified feedback block diagram in modular approach. The output voltage and all three inductor currents of power converter are accurately sensed and are fed to the feedback system. The complete feedback system consists of a group of three identical feedback systems and it is connected in such a manner that, one boost converter is connected to its corresponding feedback module.

5.1.1 Converter block schematic and functionality

The converter design is described in brief with reference to the detailed block schematic shown in Fig. 5.1. The complete block schematic represents functionality of a proposed three-phase soft-switched converter. An identical single-phase AC-DC PFC boost converter with passive snubber circuit is connected in each line of a three-phase AC supply input filter circuit consisting of L_{in} and C_{in1}. The outputs of all the three converter modules are connected in parallel

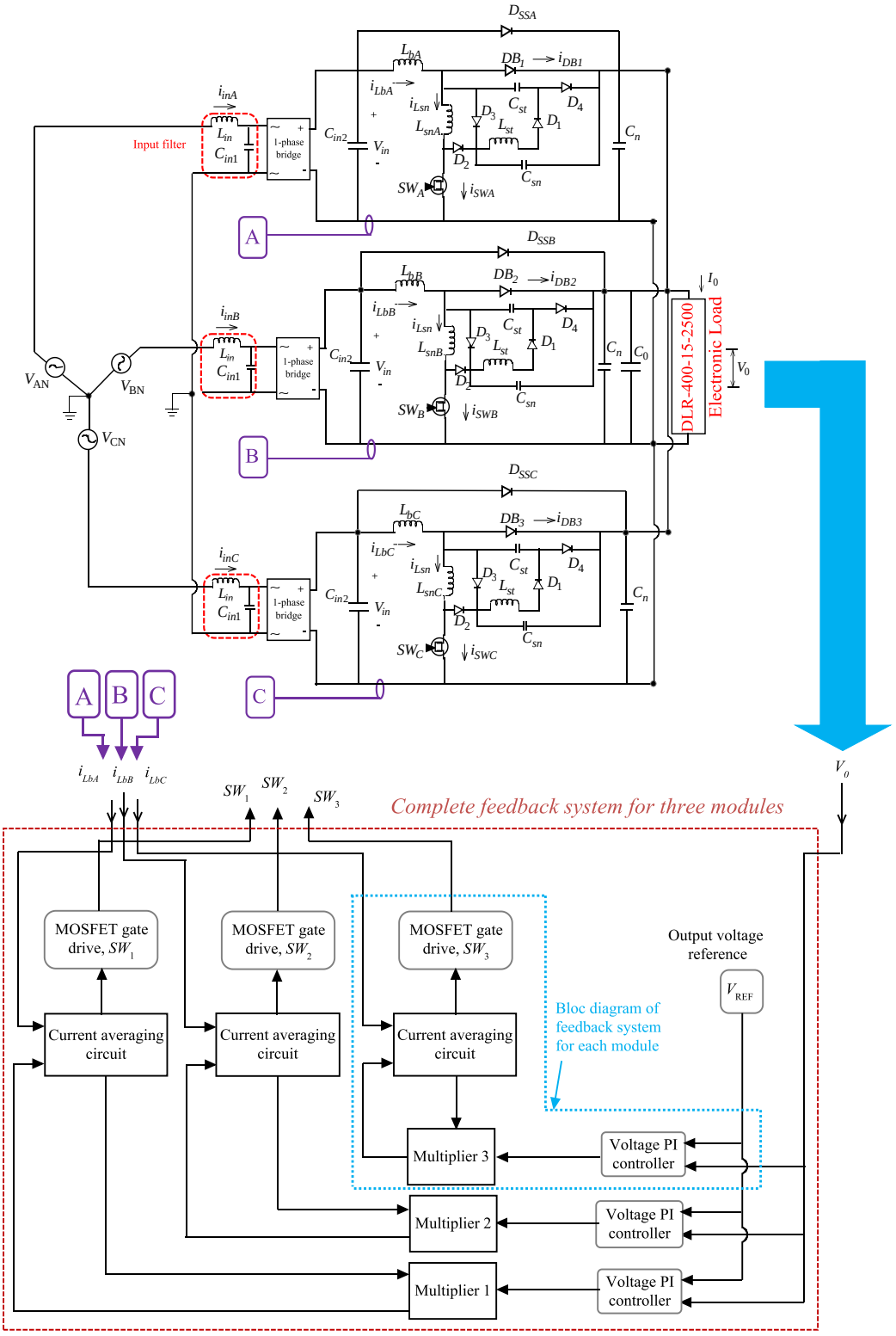


Fig. 5.1 Block schematic of proposed 1.5 kW soft-switched PFC boost converter in modular system

to raise the power level of the total converter system. The capacitor C_{in2} in all the three converters is to filter out the noise and its value is not too large to distort the input wave shape signal even at low output power and high line input conditions. The circuit topology and feedback system of each module of proposed three-phase AC-DC PFC converter is same as that of the single-phase AC-DC PFC converter with passive snubber circuit described in section 3.1.1 and 3.1.2 respectively of chapter 3. The working principle of each converter module shown in Fig. 5.1 is same as that described in section 3.2 of chapter 3 of single phase soft-switched PFC converter. However, it is understood that, the input voltage to all the three single-phase AC-DC PFC converters is displaced by 120^0 from one another.

As described earlier in sections 3.1.1 and 3.1.2 of chapter 3, the latest PFC IC ICE2PCS01 from Infineon Technologies [156, 174, 175] is used in each feedback system. The triggering pulses generated from PFC controller IC of each module are fed to their corresponding MOSFET switch of power boost converters arranged in modular system. In the proposed converter system, it is not required to sense and feed the input voltage signal to feedback system to keep the input power almost constant, this is the special feature of PFC IC used in this proposed three-phase converter, but such arrangement (sensing input voltage and feeding to feedback system) is essentially required in other AC-DC PFC converters presented in [84, 91, 95, 99, 102, 121, 124].

To regulate the output voltage, multipliers in the feedback system control the amplitude of the corresponding sinusoidal reference signal in accordance with the voltage error signal generated from output voltage of each module of the proposed converter. When the load decreases, the output voltage increases. To maintain constant load voltage, the control circuit senses the load voltage and feeds back to the feedback system. The pulse width is automatically

reduced in the switching cycle and the output voltage is regulated and maintained almost constant.

5.1.2 Schematic design and component selection

The design procedure, which is developed by standard method of design procedures presented in references [97, 99, 102, 152, 160] has been followed which is based not only on the soft switching turn-on and turn-off requirements of the MOSFET switch in each module and other semiconductor switches on the proposed converter, but also the transfer of the snubber energy to the load. The complete design procedure for resonant elements of each module of the proposed converter is described in section 3.3 of chapter 3 and the same concords with the proposed each module of three-phase AC-DC PFC modular system.

The MOSFETs employed are selected by their capacity to carry the peak inductor current, support the flyback (reflected) boost voltage and their ability to generate low conduction losses for achieving higher efficiency. In this design, three SPA20N65C3 (650 V/20.7 A/0.19 Ω) MOSFETs from Infineon Technologies were used. The boost rectifier diodes must also have a nearer voltage and current ratings as the MOSFET's. The boost *DB* diode in each module must also be very fast to reduce the MOSFET's turn-on losses. Three boost diodes RHRP 3060 (600 V/30 A) from Fairchild Semiconductor are used in the proposed system. The Fast recovery epitaxial diodes DSEI30-12A from IXYS Corporation (auxiliary diodes $D_1 - D_4$ in each module) which assist in auxiliary circuits are used in the proposed modular converter. Standard axial rectifier diodes 1N5408 from Vishay Electronics (D_{SSA}, D_{SSB}, D_{SSC}) provide soft-start function which limit the start up inrush current thus reducing the stress on the corresponding boost diode of each module. Just after start-up, when output capacitor becomes equal to regulated voltage of 400 V, these protective diodes (D_{SSA}, D_{SSB}, and D_{SSC}) become reverse biased.

To develop a better understanding about the performance of a three-phase modular system of a continuous boost PFC circuit, a 1500 W prototype PFC boost circuit model was built. To meet the requirements of EMI, power quality standards of IEEE-519 and having a smaller input EMI filter, with switching frequency below 150 kHz was preferred. Thus for all the different measurements made, the switching frequency was always kept to about 100 kHz and the boost inductor ripple current was considered to be less than 20% of its maximum peak value. Table 5.1 shows the brief specifications of the proposed AC-DC PFC boost converter. The component values and devices of the proposed three-phase AC-DC PFC converter with passive snubber circuit are tabulated in Table. 5.2

Table 5.1 Specifications of 1500 W Three-phase AC-DC PFC proposed converter

General	
Product	Universal input 1500 W PFC AC-DC boost converter with passive snubber circuit.
Operating ambient	Full operation: -10^0 *C* to $+40^0$ *C*.
Input	
Input range	85V to 265 V AC/50 Hz (Nominal: 215 V AC/ per phase).
Hold-up time	Better than 20 *mS* at 215 *V* AC input, measured at full load.
Input power factor	Greater than 0.99 at full load condition.
Input circuit	Three wire system with safety ground.
Inrush current	< 40 Amps for less than 5 cycles at 215 V AC input
Efficiency	Typically 96.5% at full-load, 215 V input and nominal output voltage.
Output	
Nominal output	Nominal value of +400 *V DC* with ripple less than 5 *V* pk-pk.
Max. Load current	About 3.8 Amps.
Voltage regulation	Output to be within 400 $V \pm 5$ *V* at specified ambient, specified input line and specified output current conditions.

Table 5.2 Parameter set employed in the evaluation tests of the proposed AC-DC PFC boost with passive snubber circuit

Component	***Value/model***	
	Simulation	**Experimental**
Bridge Rectifier IC with heat sink (In each module)	Ideal	GBJ 2506-BP
MOSFETs (SW_A, SW_B, SW_C)	Ideal	SPA20N65C3
Auxiliary Diodes ($D_1 - D_4$), (In each module)	Ideal	DSEI 30-12A
Boost Diode (DB_1, DB_2,DB_3)	Ideal	RHRP 3060
Low line filter inductor (L_{in}), (In each module)	5.6 µH	5.6 µH
Input filter (C_{in1}), (In each module)	0.47µF, 275 V	0.4 µF, 275 V
Input HF bypass capacitor (C_{in2}), (In each module)	1 µF, 630 V	1 µF, 630 V
Boost inductor (L_{bA}, L_{bB}, L_{bC})	1.5 mH	1.5 mH
Snubber inductor (L_{snA}, L_{snB}, L_{snC})	2.5 µH	2.5 µH
Storage inductor (In each module)	62.5 µH	62.5 µH
Snubber capacitor (C_{sn}), (In each module)	0.68 µF	0.68 µF
Storage capacitor (C_{st}), (In each module)	1.2 µF	1.2 µF
Output HF bypass capacitor (C_n), (In each module)	1 µF, 600 V	1 µF, 600 V

The proposed three-phase soft-switched converter was designed to operate in the CCM of operation for the whole line period and for wide range of output power levels. The hardware layout was developed with great care, so as to minimize the effects of EMI. DC electronic load *model No.* **DLR-400-15-2500** from **"Alltest Instruments Inc.,"** has been used for technical evaluation of the proposed converter. Overall converter performance was tested with an electronic load to ascertain that the design meets the required specifications.

5.2 Simulation and experimental results

In simulation, three individual feedback systems are developed in SIMULINK environment and are linked with a power converter which is developed in PSIM package through Sim-Coupler module. Fig. 5.2 shows the complete simulation schematic layout of a proposed three-phase AC-DC PFC converter in modular approach. The advantage of Sim-Coupler module

is to make use of PSIM's capability in power simulation and MATLAB/SIMULINK capability in control simulation, thus greatly shortening the time to set-up and simulate a power electronic system. In this simulation, the sensed inductor currents and output voltage are fed to feedback system which is developed in SIMULINK environment through a Sim-Coupler. After processing of a feedback system the triggering pulses obtained from control system are applied to MOSFETs of a power boost converter in Power-Sim environment via Sim-Coupler.

Fig. 5.3 shows the input voltage, input currents and output voltage waveforms of a proposed converter for an input voltage of 245 V_{RMS}. This is tested for beyond the nominal input voltage to check for the higher range of input voltage level (As proposed converter is designed for universal input voltage). In the upper graph of Fig. 5.3, three phase input voltages, output voltage waveforms along with magnified input current waveform of phase A are shown, both input voltage and current of phase *A* are almost sinusoidal and are in phase. This ascertains that each AC line input current is in phase with its corresponding sinusoidal input voltage; this is the evidence of theoretical analysis that, proposed three-phase converter operates at nearly unity power factor. In the lower graph of Fig. 5.3, it can be observed that, three input currents are displaced by 120^0. This confirms that, there is no phase displacement between the each input line current with its corresponding input voltage.

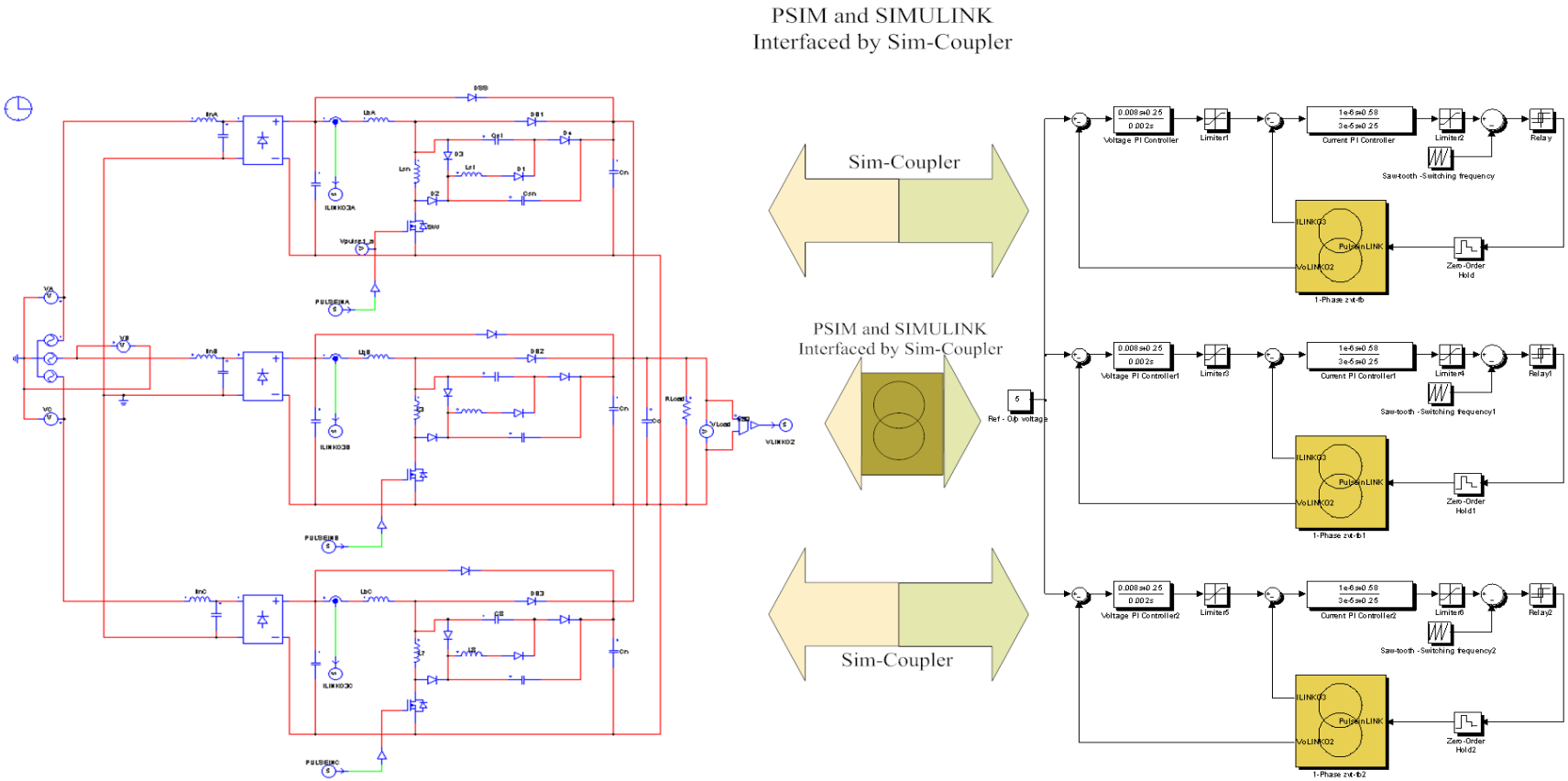


Fig. 5.2 Simulation layout of proposed three-phase AC-DC PFC boost converter with passive snubber circuit in modular system (Power converter in PowerSim (PSIM) and feedback system in SIMULINK)

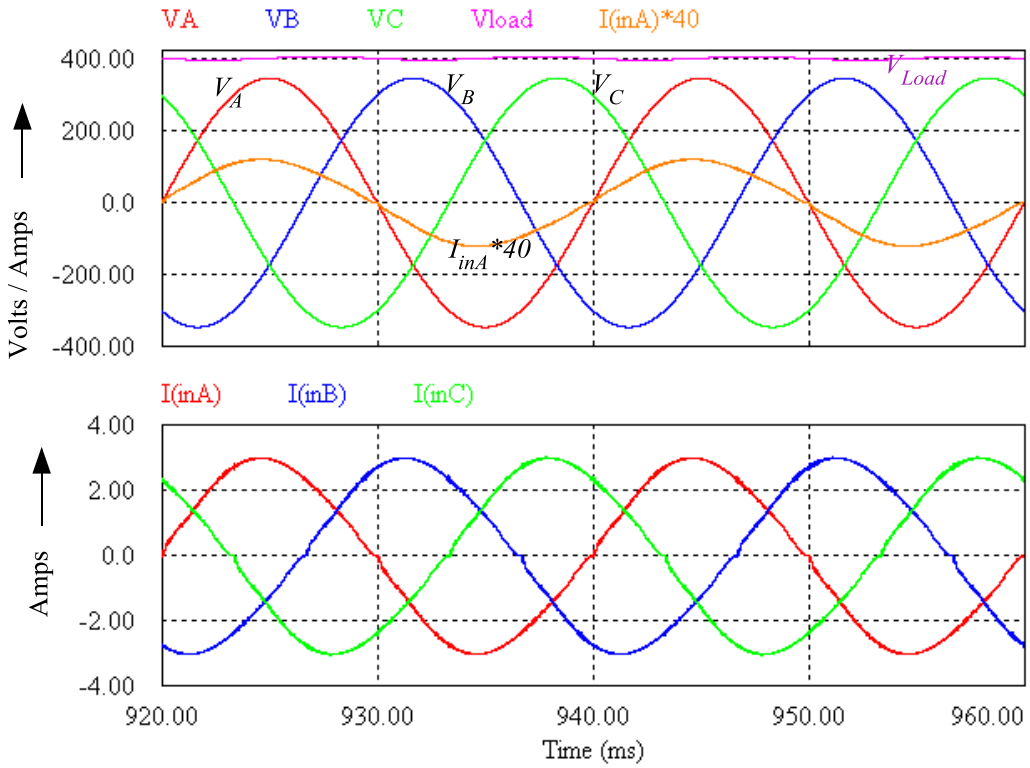


Fig. 5.3 Simulated input voltage and current waveforms of a proposed three-phase AC-DC PFC converter with passive snubber circuit in modular approach

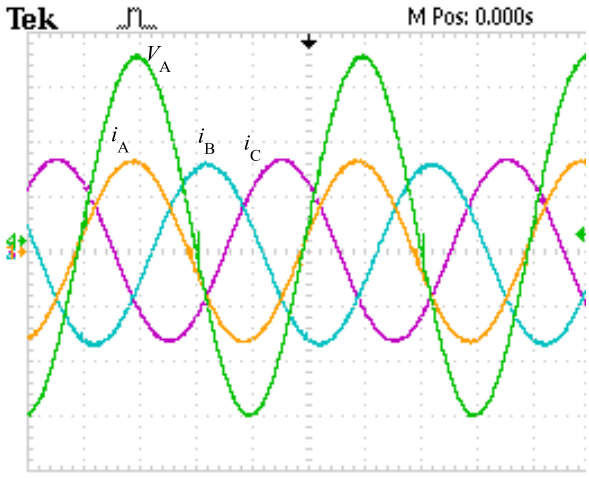


Fig. 5.4 Experimental input voltage and current waveforms of a proposed three-phase AC-DC PFC converter with passive snubber circuit in modular approach Scale: 100 V/div, 2 A/div, 5 ms/div.

The oscillogram of Fig. 5.4 shows the input voltage and current measurements of the 1.5 kW prototype of the proposed three-phase AC-DC soft-switched PFC converter. All the three current waveforms and input voltage of phase *A* are almost sinusoidal to that shown in simulated results of Fig. 5.3. This justifies that the mathematically designed converter components strongly agree with the predicted waveforms of a proposed PFC converter.

The experimental results measured and recorded by oscillogram are shown in Fig. 5.5. The three-phase input current waveforms at a variable load conditions from full-load to 25% of full-load for an input voltage of 215 V_{RMS} are shown in Fig. 5.5 (a) - (d). It is evident that the proposed three-phase soft-switched converter with passive snubber circuit operates at nearer to unity power factor over a wide range of load variation and input current decreases with decrease in load level.

The transient response of the proposed three-phase AC-DC PFC boost converter with passive snubber circuit at load step from 1.5 kW (full-load) to 0.75 kW (half load) and vice versa are shown in Fig. 5.6 (a) and Fig. 5.6(b) respectively. It can be seen that, during transition from full-load to half load step change of Fig. 5.6 (a), the output voltage rises from the nominal output voltage V_0=400 *V* to the maximum value of 425 *V*, on the other hand, during transition from half load to full-load, (see Fig 5.6 (b)), the output voltage undershoots to a level of 385 *V* and recovers to its nominal output voltage level without disturbance. It is observed that the proposed three-phase soft-switched converter maintains almost constant load voltage at all output power levels starting from 25% of full-load to full-load.

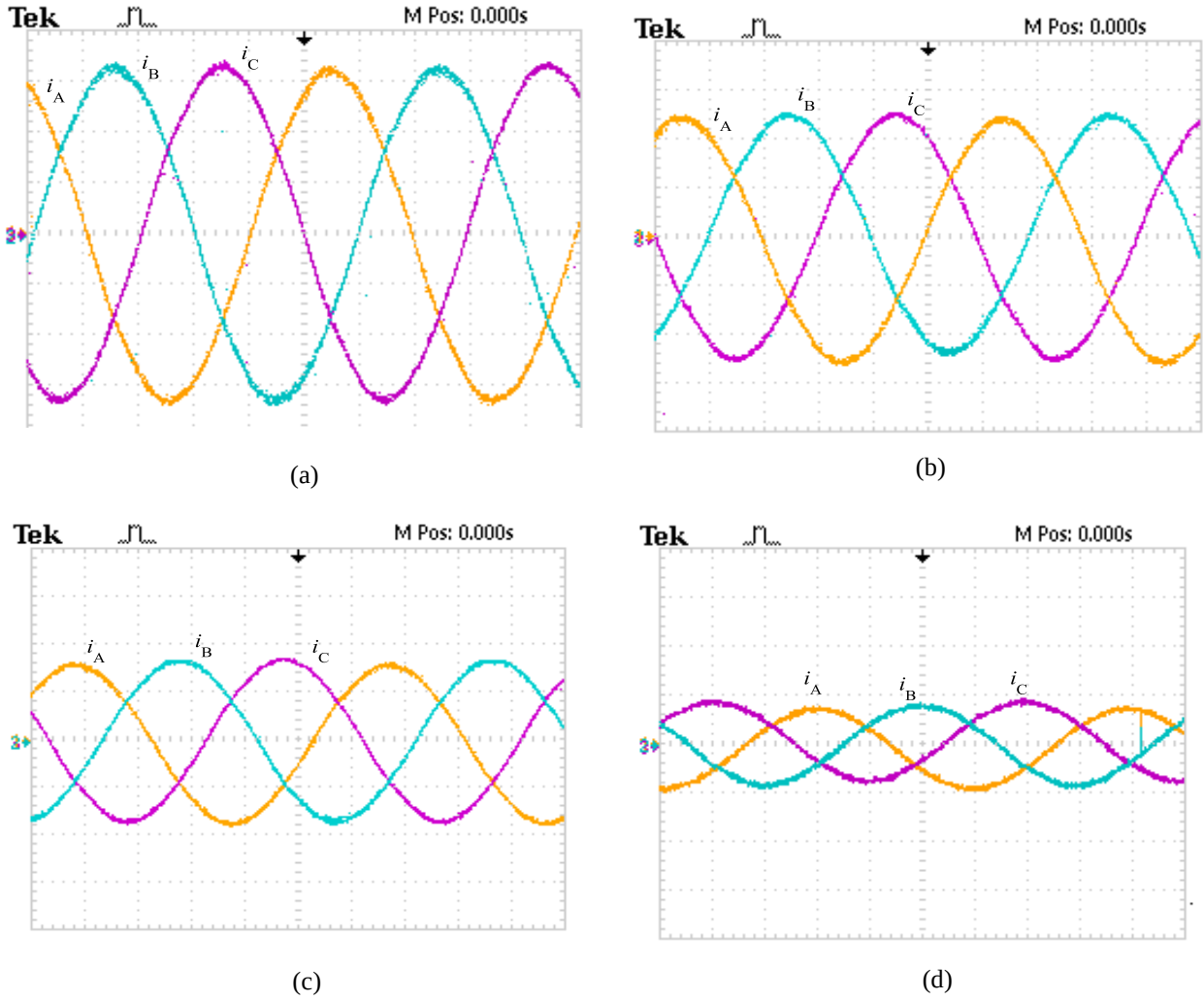
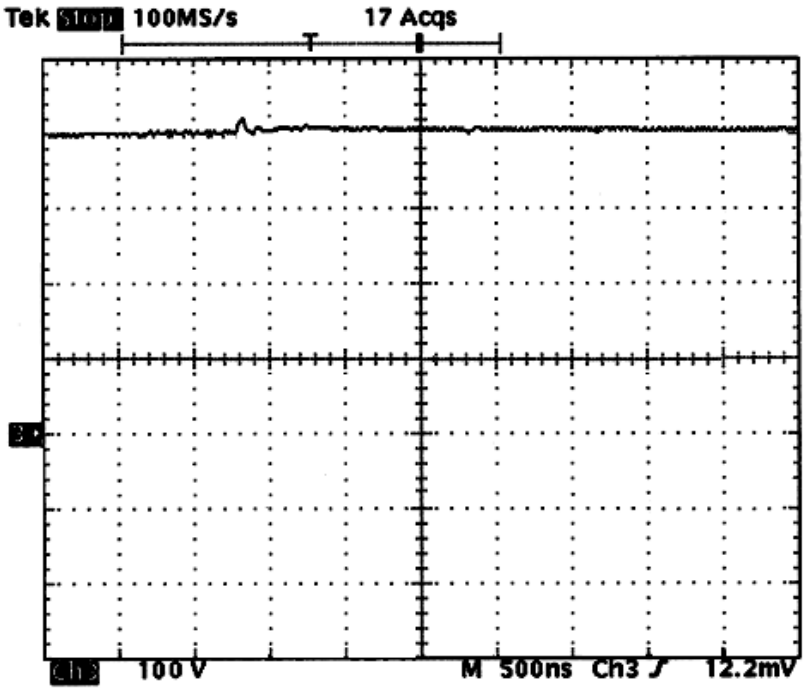
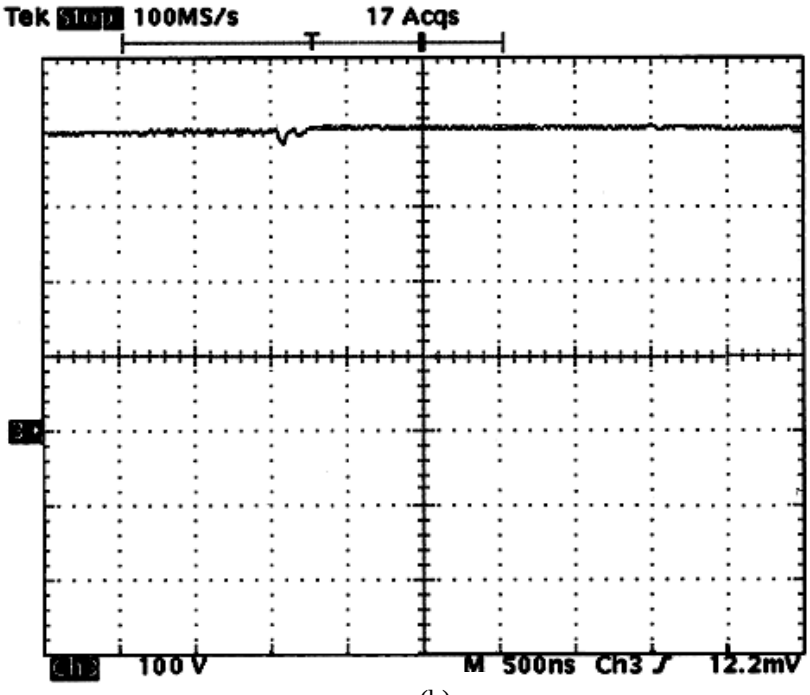


Fig. 5.5 Experimental input currents (i_A, i_B, i_C) at (a) full-load (b) 75% of full-load (c) 50% of full-load and (d) 25% of full-load for an input voltage of 245 V_{RMS}.
Scale: 1 A/div, 3 *ms*/div.



(a)



(b)

Fig. 5.6 Output voltage response of a proposed converter under change in load (a) From full-load to half load (b) From half load to full-load. Scale: 100 *V/div*, 5 *ms/div*.

The comparison of efficiency curves of proposed soft-switched converter and that of three-phase hard-switched converter are shown in Fig. 5.7. From Fig. 5.7 it can be seen that the efficiency of proposed soft-switched converter is higher than that of hard-switched converter, especially at high output power levels. At full-load power level, it is found that, the proposed three-phase soft-switched converter has total losses of around 39% of the total losses of the three-phase hard-switched converter, and so the overall efficiency, which is at about 90.8% in the hard-switched case, increases to 96.2% . Even under, light load condition (25% of full-load), the minimum increase in the efficiency is found to be 3.5%. The developed prototype of proposed three-phase AC-DC PFC soft-switched boost converter with passive snubber circuit is shown in Fig. 5.8.

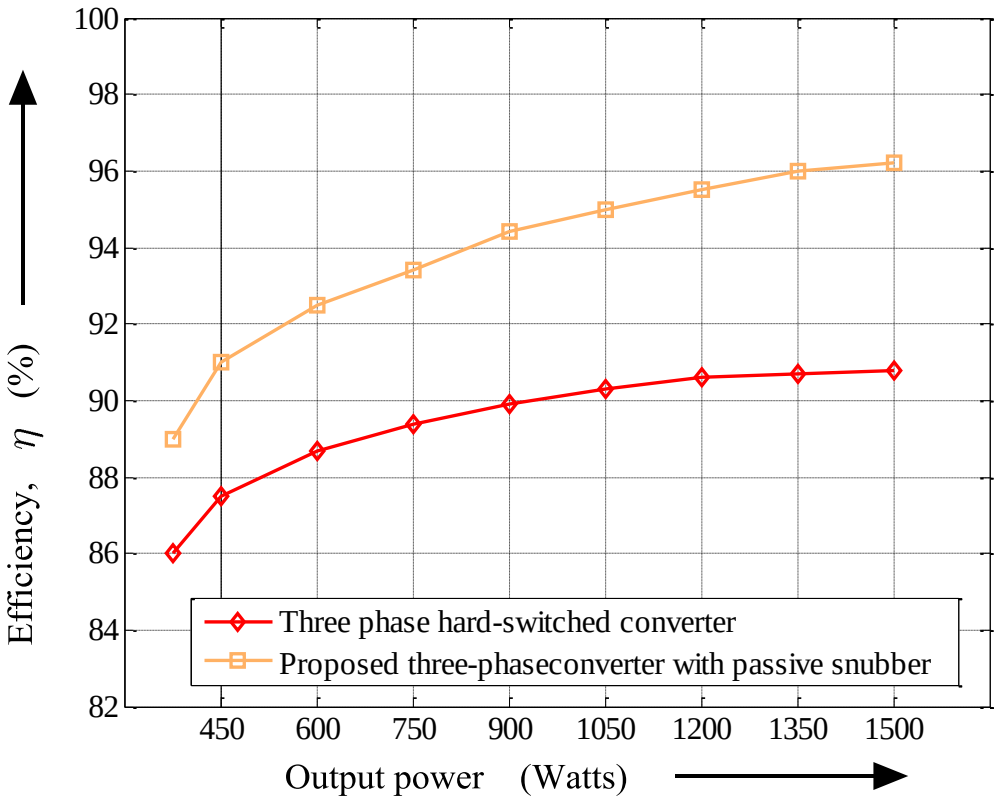


Fig. 5.7 Comparison of efficiency curves of proposed three-phase soft-switched converter with three-phase hard-switched converter

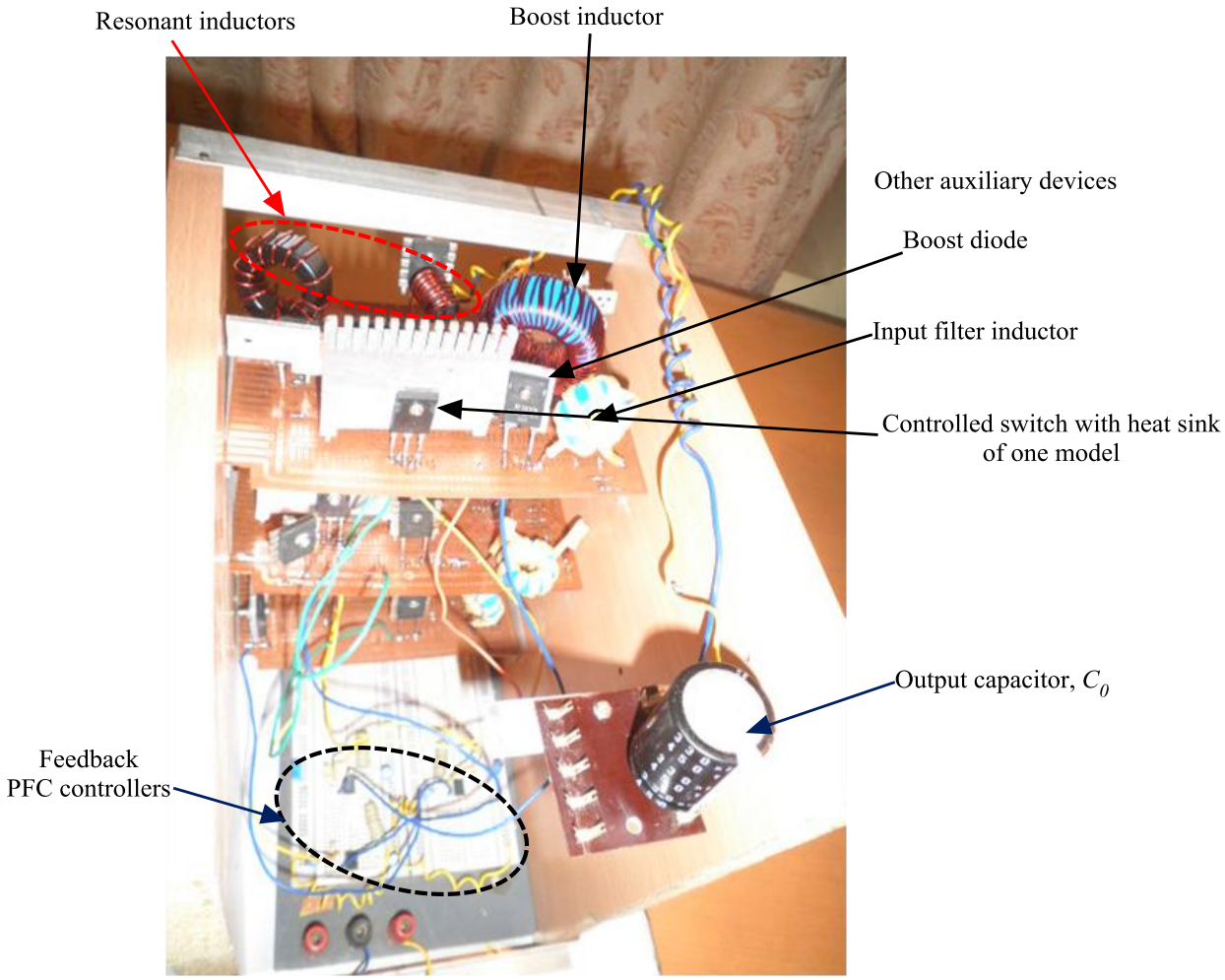


Fig. 5.8 Photograph of proposed 3-phase AC-DC PFC boost converter with passive snubber circuit

5.3 A 1.5 kW three-phase AC-DC PFC boost converter with an active snubber circuit in modular system

A prototype of a proposed three-phase AC-DC PFC boost converter with an active snubber circuit has been developed in the Power Electronics and Drives Laboratory, at NIT, Rourkela. Three identical single-phase AC-DC PFC boost converter with an active snubber proposed in chapter 4 of thesis are connected in modular approach. Regarding the feedback system, as described earlier, PFC IC ICE2PCS01 controller has been employed to each module of the proposed three-phase system.

Fig. 5.9 shows the three-phase AC-DC PFC boost converter with an active snubber circuit schematic with simplified feedback block diagram in modular approach. The output voltage and all three boost inductor currents of power converter are accurately sensed and are fed to the feedback system. The complete feedback system consists of a group of three identical feedback systems and it is connected in such a manner that, one boost converter is connected to one corresponding feedback module.

The technical specifications of the prototype of the proposed three-phase AC-DC PFC converter with an active snubber circuit are identical to that three-phase AC-DC PFC converter with passive snubber circuit described in Table 5.1 of section 5.1.2. This is because; the aim of both prototypes (three-phase AC-DC PFC with passive snubber and three-phase AC-DC PFC with active snubber converters) is to achieve higher efficiency of a converter with the primary objective of accomplishing nearly unity input power factor. The component values and devices of the proposed three-phase AC-DC PFC converter with active snubber circuit are tabulated in Table. 5.3.

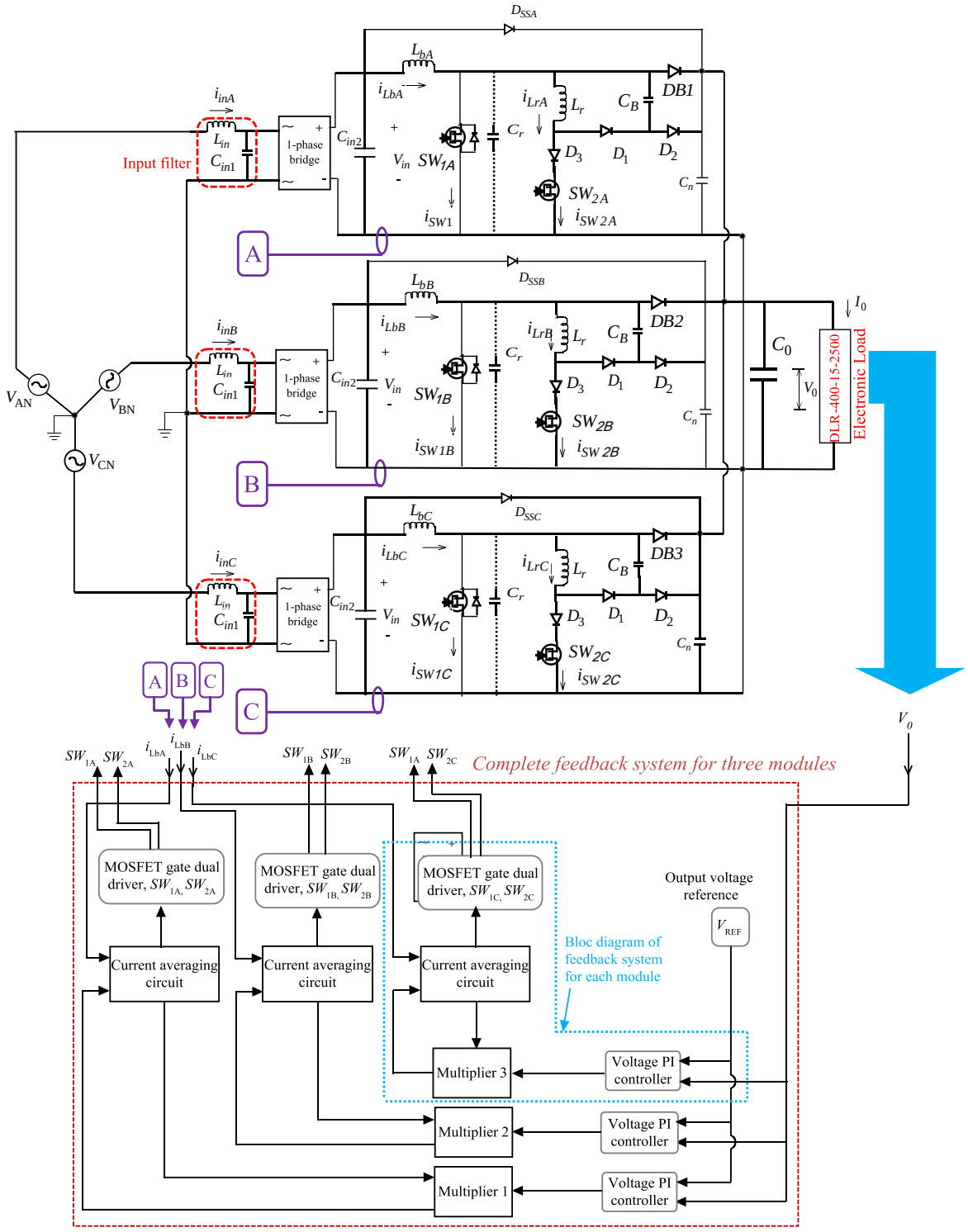


Fig. 5.9 Block schematic of proposed 1.5 kW soft-switched PFC boost converter with active snubber circuit in modular system

Table 5.3 Parameter set employed in the evaluation tests of the 3-ph AC-DC PFC boost converter with an active snubber

Parameter	Simulation	Experimental
Bridge Rectifier IC with heat sink (In each module)	Ideal	GBJ 2506-BP
MOSFETs (SW_{1A}, SW_{2A}, SW_{1B}, SW_{2B}, SW_{1C}, SW_{2C},)	Ideal	IRFP 460
Hyper fast boost diodes (*DB1, DB2 & DB3*)	Ideal	DSEI 30-12A
Auxiliary diodes, (D_1, D_2 & D_3), (In each module)	Ideal	RHRP 3060
Low line filter inductor,(L_{in}), (In each module)	5.6 μH	5.6 μH
Input filter (C_{in1}), (In each module)	0.47 μF, 275 V	0.47 μF, 275 V
Input HF bypass capacitor (C_{in2}), (In each module)	1 μF, 630 V	1 μF, 630 V
Boost inductor (L_{bA}, L_{bB} & L_{bC}), (In each module)	1.5 mH	1.5 mH
Resonant inductor (L_r), (In each module)	10 μH	10 μH
Snubber capacitor (C_B), (In each module)	5.6 nF, 400 V	5.6 nF, 400 V
Output bypass capacitor C_n, (In each module)	1 μF	1 μF
Output capacitor (C_0)	450 μF, 600 V	450 μF, 600 V

5.4 Simulation and experimental results

In simulation, as described in previous section 5.2 the power converter (developed in PSIM) of each phase is linked with its corresponding feedback system (developed in SIMULINK environment) via Sim-coupler. The simulation schematic of proposed three-phase AC-DC PFC boost with an active snubber circuit is shown in Fig. 5.10. The feedback system generates the complementary gate drive pulses with sufficient dead band to both active switches of the proposed PFC boost soft-switched converter.

The simulated three-phase input voltage waveform of A-phase and input currents at low load (25% of full load) are shown in Fig. 5.11 for an input voltage of 215 V_{rms}. It is ascertained that each AC input line current is in phase with its corresponding sinusoidal input voltage; thus, input power factor of a proposed three-phase converter is nearly unity.

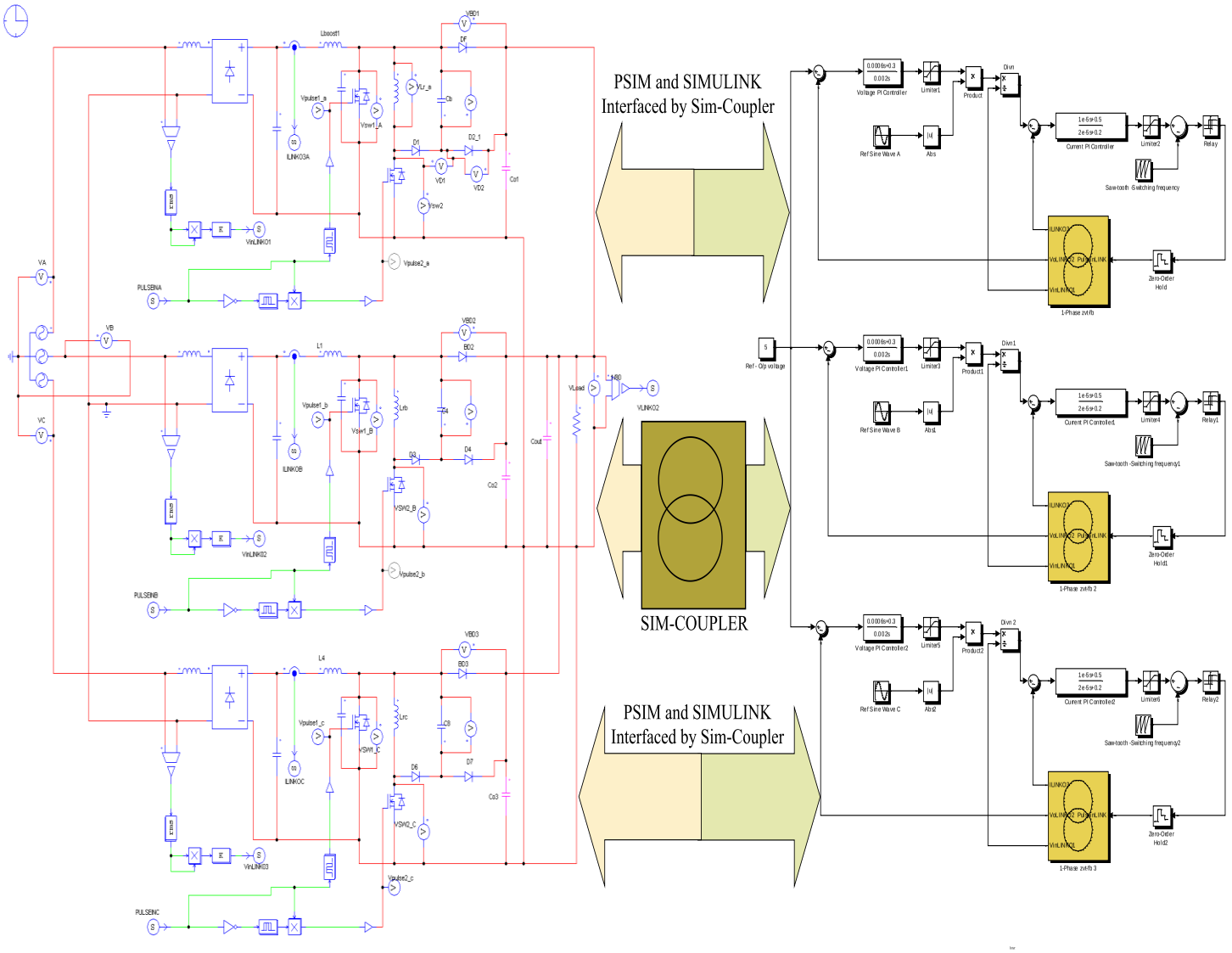


Fig. 5.10 Simulation layout of proposed three-phase AC-DC PFC boost converter with active snubber circuit in modular system (Power converter in PowerSim (PSIM) and feedback system in SIMULINK)

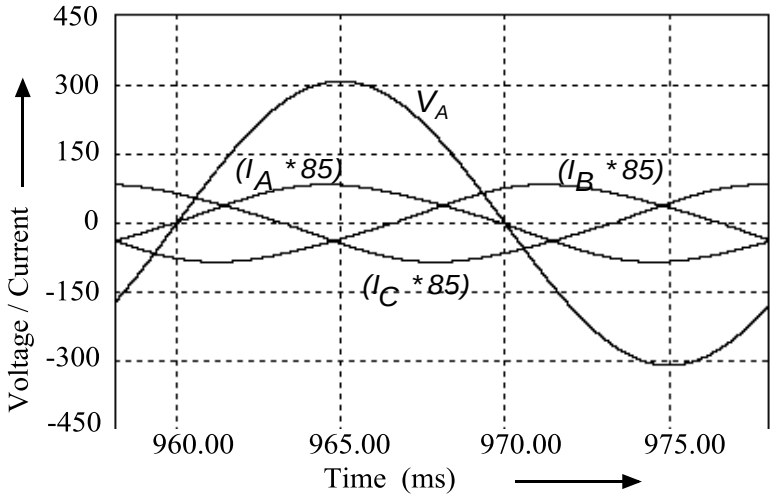


Fig. 5.11 Simulated input current (magnified) i_A, i_B, i_C and input *A*-phase voltage V_A waveforms at 25% of full load for an input voltage of 215 V_{RMS}.

The experimental results shown in Fig. 5.12 are measured and recorded by CW240 Clamp-on Power Meter. The three-phase input current waveforms at a variable load conditions from full load to 25% of full load for an input phase voltage of 215 V_{rms} are shown in Fig. 5.12 (a) – (d). Fig. 5.12(d) represents the input phase voltage V_A as well as three input current waveforms at low load condition. It is observed that, this response is almost closer to that obtained in simulated results shown in Fig. 5.11. From this, it is evident that, the proposed AC-DC soft switched converter operates nearer to the unity power factor even under low load condition.

5.5 Performance characteristics

The THD*i* and PF were calculated from the measured data of the experimental results of the proposed AC-DC soft-switched converter. The variation of THD*i* as a function of the load power of the proposed boost converter with active snubber, PFC converter with passive snubber and the conventional hard switched converter are shown in Fig. 5.13. The THD*i* at full load of the proposed converter is obtained to be around 2.8% and the corresponding PF is equal to 0.9996.

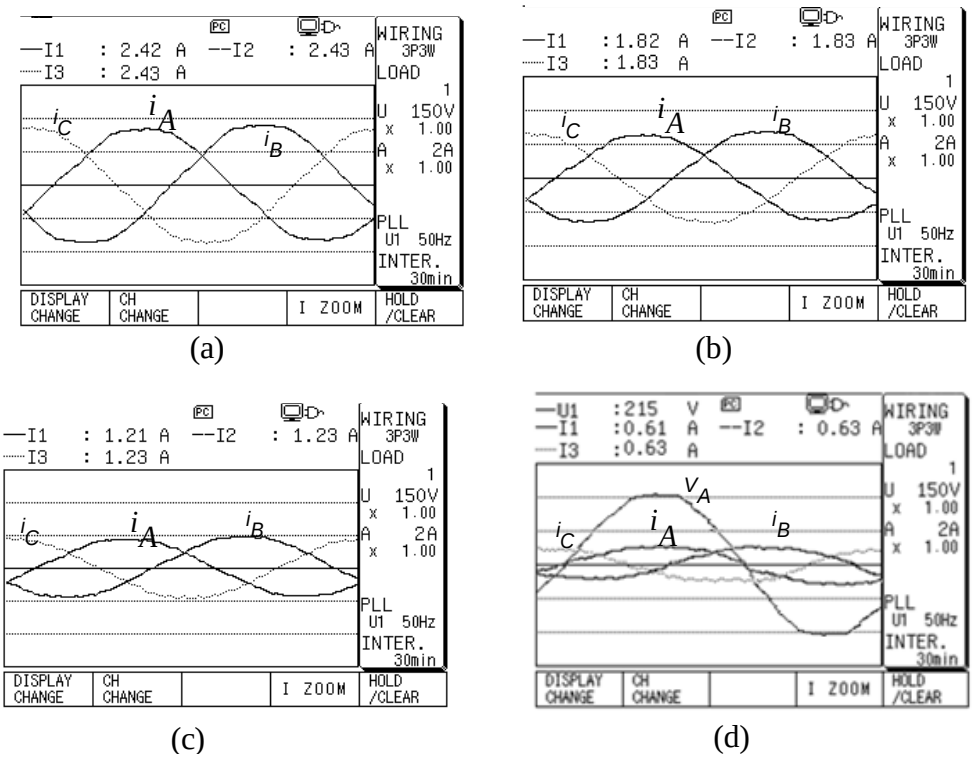


Fig. 5.12 Experimental input voltage and current waveforms. Input currents i_A, i_B and i_C at (a) full load (b) at 75% of full load (c) 50% of full load (e) 25% of full load and input phase voltage V_A.
Scale: on screen.

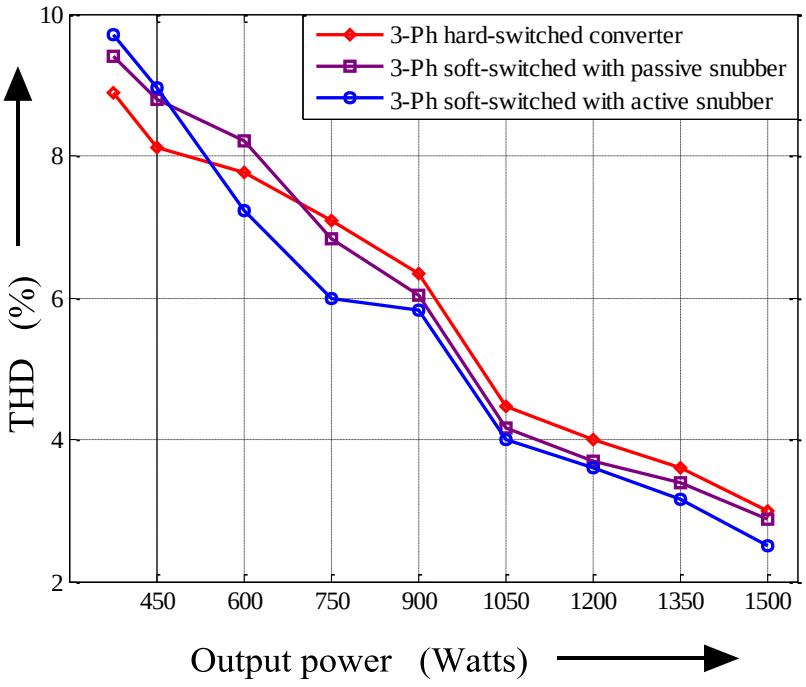


Fig. 5.13 Comparison of variation of THD as a function of load power of three-phase AC-DC PFC boost converters.

The PF variation as a function of load power of the proposed soft-switched boost converter with active snubber, PFC boost converter with passive snubber and conventional hard switched PFC boost converters are shown in Fig. 5.14. It can be seen that, the power factor of the proposed converter is higher than that of the PFC with passive snubber and hard switched converter at higher power levels. At lower power levels, its value is slightly lower than that of conventional PFC converter due to considerable effect of lower order harmonics and higher than the PFC converter with passive snubber circuit. The total THD*i* is well below 10%, hence the proposed soft switched converter exhibits lowest outcome of THD*i*.

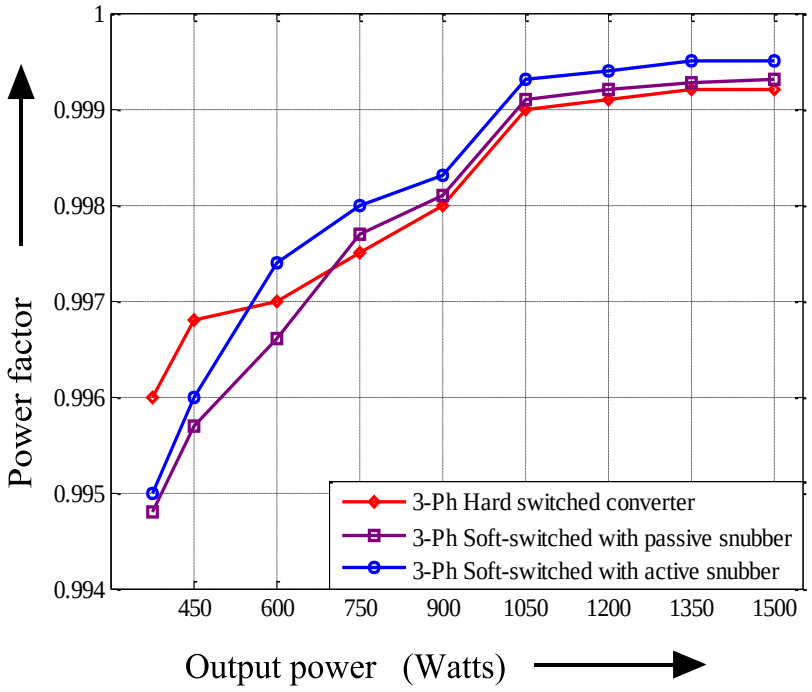


Fig. 5.14 Comparison of variation of PF as a function of load power of three-phase AC-DC PFC boost converters.

The efficiency curves of the proposed three-phase AC-DC soft switched PFC boost converters (both with active snubber and passive snubber) and the conventional three-phase AC-DC hard-switched PFC boost converter with the nominal input voltage 215 V_{rms} are presented in

Fig. 5.15. It is observed that the efficiency of the proposed converter varies from 97.3% to 91.3%. The highest efficiency of the proposed AC-DC PFC converter is obtained at full load power of 1500 W which is around 7.25% higher than that of the conventional hard switched PFC converter. The proposed soft-switched PFC converter with active snubber has higher efficiency of 1.35% with respect to that of PFC converter with passive snubber. The corresponding improvement at the low power level of proposed soft-switching converters (PFC with active and passive snubbers) are also shown in Fig. 5.15. The Fig. 5.16 shows the variation of output voltage under step-change condition of the output load. It is observed that the converter maintains almost constant load voltage.

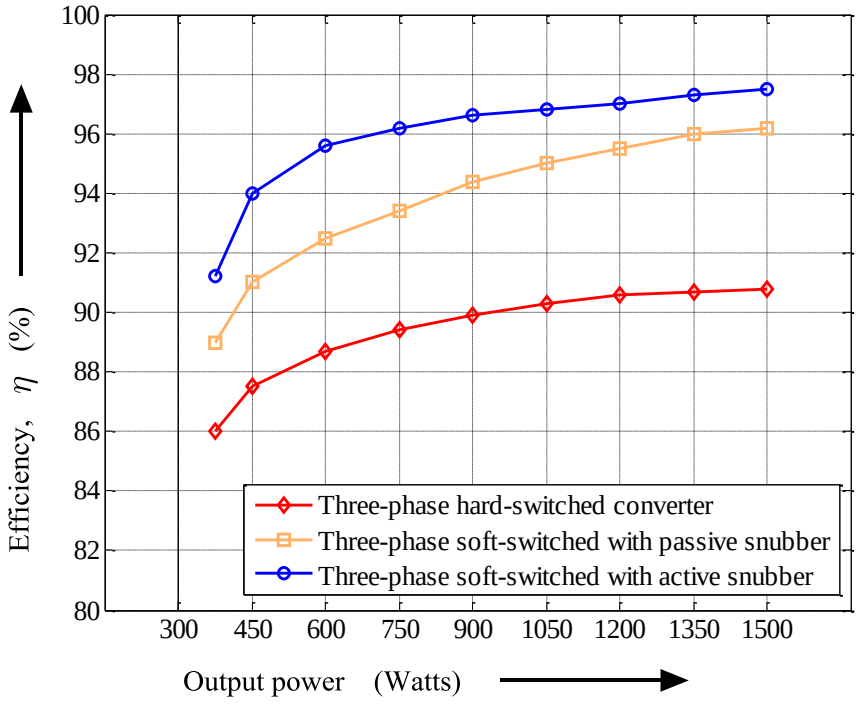


Fig. 5.15 Comparison of efficiency curves of proposed three-phase soft-switched converters with hard switched three-phase AC-DC converter as a function of load power

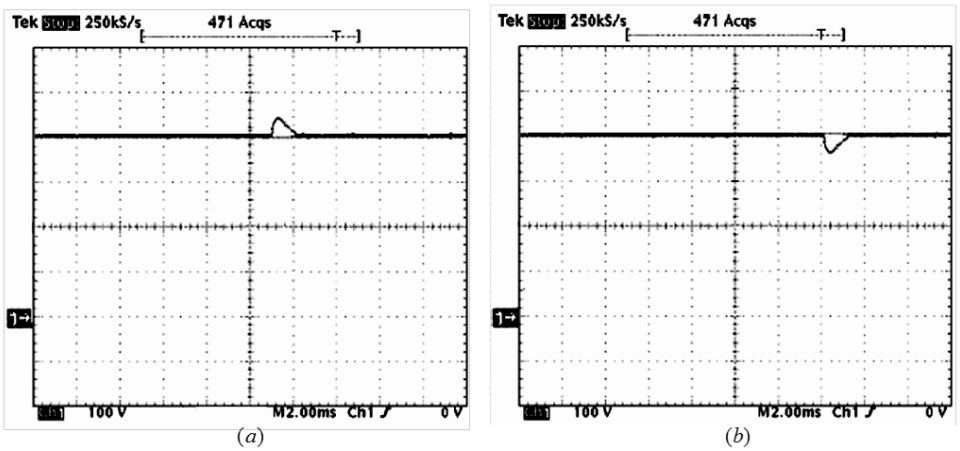


Fig.5.16 Output voltage response under change in load
(a) From full load to half load (b) from half load to full load.
Scale: 100 V/div, 5 ms/div.

The developed prototype of proposed three-phase AC-DC PFC soft-switched boost converter with an active snubber circuit is shown in Fig. 5.17.

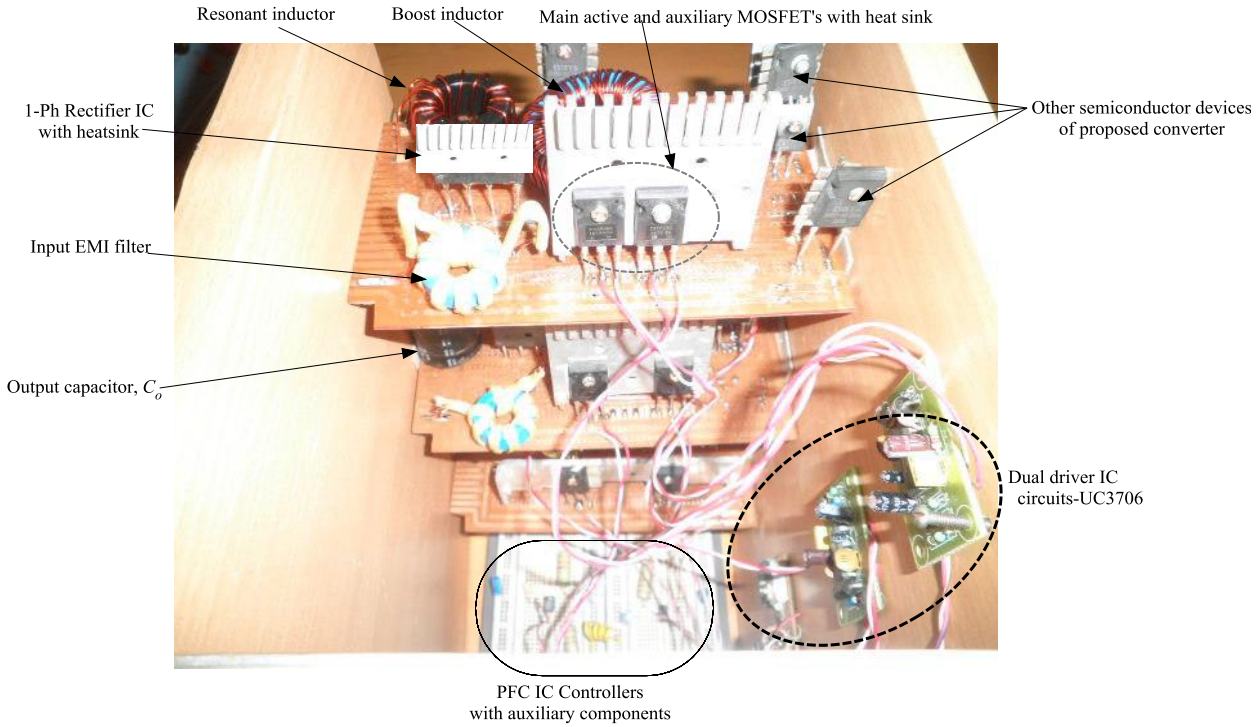


Fig. 5.17 Photograph of proposed 3-phase AC-DC PFC boost converter with active snubber circuit

5.6 Summary

A three-phase modular approach has been proposed for high power expansion of AC-DC PFC converters. Higher efficiency is obtained in these proposed three-phase converters by incorporating soft-switching techniques. Soft switching techniques proposed for single-phase AC-DC PFC boost converters in chapter 3 and chapter 4 are employed for the proposed three-phase AC-DC PFC converters in modular system; to minimize the switching losses with the primary objective of achieving near unity input power factor. For simulation, special features of PSIM and SIMULINK are utilized by interfacing both the environments via Sim-Coupler. The prototypes for all the three converters (hard-switched, soft-switched with passive snubber, and soft-switched with active snubber) are developed in the laboratory for the converter specification of 400 V, 1.5 kW, 100 kHz frequency operation. The performance improvement with respect to efficiency, THD and PF is successfully obtained in the proposed three-phase AC-DC PFC boost soft-switched converters. Through the performance characteristics and graphs of all the three converters presented in section 5.5, it is revealed that, three-phase AC-DC PFC boost converter with active snubber circuit is found to be the superior among the converters with respect to efficiency, THD and power factor.

Chapter 6

Summary and Future Scope

- **Summary**
- **Future scope**

Because of high performance, easy maintainability, and high reliability, DPS systems are widely employed for telecom and computer server applications. In present situation, the exponential increase in the functionality of these applications demands the power management, which provides a large market to DPS systems. Hence, the emergence of front-end AC-DC converters (PFC + DC/DC converter) in these DPS poses many challenges and attracts large research efforts to investigate different solutions such as: high efficiency, fast dynamic response, and high power density. Improved performance of these front-end AC-DC converters in DPS systems must meet these requirements.

6.1 Summary

This dissertation is engaged in researching solutions for PFC boost converters operating at high switching frequency. For PFC stage, conventional single switch PFC boost converter is most suitable topology because of its inherent advantages. However, to meet EMI standards, as well as small filter size, switching frequency of PFC boost converter circuit is usually chosen below 150 kHz. The conventional PFC boost converter with single-sided PWM switching sacrifices the dynamic response of output voltage during load or line voltage change, owing to the fact of low bandwidth filter in the voltage feedback loop. This sluggish transient response problem is further compounded by large voltage overshoots and voltage drops enforcing additional stress on the PFC boost components, as well as on its downstream switch mode power supply load. On the other hand, operating AC-DC PFC boost converter in CCM, with high switching frequency reduces the size of converter (especially magnetic components) and hence the reduction in the overall cost; but this leads to the large switching loss (owing to hard switching) which precludes the circuit operation at higher switching frequency. Hence, the loss minimization in these front-end converters has become a prime issue and can be accomplished by employing soft-switching techniques.

Thus it is important to investigate a suitable soft switching topology that allows the high switching frequency operation of PFC AC-DC boost converter. In addition to these, the DPS demands high power expandability, higher power density and less weight for front-end converters employed for telecom and computer server applications. A systematic modular approach of three-phase system will support the design engineers to achieve these needs of DPSs system. This dissertation brings out some of the solutions to these problems by employing suitable methods and auxiliary soft switching circuits to AC-DC PFC boost converter.

This research presents different topologies with improved performance of PFC AC-DC converters for DPS applications. The specific contributions of this study, based on chapter two to five are summarized as below:

1. For front-end single-phase AC-DC PFC converters, an extended PWM method is proposed to improve the dynamic response during load change or line voltage change. Improved dynamic response is achieved by employing two sided PWM technique by using equal slope triangular signal instead of saw-tooth signal. For PWM switching, the control signal from the feedback system is derived into two signals (of opposite off-sets) which are compared with triangular signal to generate required triggering pulses to drive MOSFET switch of boost converter. To achieve this, two comparators are used in the PWM switching module. However, the increase in the complexity of the PWM switching does not affect the overall performance of the converter. This method essentially improves the dynamic response of the system and reduces the voltage stress on PFC components in comparison with single-sided PWM switching method.

Along with the improved dynamic response, the higher power density can be accomplished with power expandability of three-phase system in modular approach. These single-phase as well as three-phase PFC converters have achieved nearly unity input power

factor even at light load conditions with low THD. The discussed features of the method are authenticated with simulation as well as experimental results.

2. For medium power applications at higher switching frequency, a single-phase AC-DC PFC soft-switched boost converter with a passive snubber circuit has been investigated. The aim is to increase the efficiency of the converter with the primary objective of operating proposed converter at nearly unity power factor. The proposed passive snubber circuit in boost converter serves as an energy recovery turn-on snubber, which greatly reduces the reverse-recovery peak current of the boost diode and turn-on losses of the controlled switch. In addition, this auxiliary passive circuit provides ZVS and/or ZCS condition for all semiconductor switches of the converter. The special feature of this converter is that, the snubber energy is recuperated to the load without the use of main path (through PFC boost diode), hence the reduction in the conduction losses of the boost diode. In the proposed converter, all the semiconductor switches except the boost diode do not have extra voltage or current stress. However, the voltage stress on the boost diode is slightly higher than the output voltage because of the presence of the storage capacitor in the auxiliary passive circuit, but the current in the boost diode is well within the limit. Comparing with the single-phase conventional AC-DC PFC boost converter, this proposed converter achieves higher efficiency for a wide range of output power. The prototype developed in the laboratory of the proposed converter operates at almost unity power factor and provides low THD. The experimental results measured and recorded are authenticated with the simulation results of the proposed converter.

3. For medium power applications, a single-phase AC-DC PFC boost converter with a suitable active auxiliary snubber circuit has been investigated and proposed. This topology with an active auxiliary circuit is designed to achieve ZVT for main switch; its feasibility is tested and verified with prototype developed in the laboratory. The auxiliary

active circuit components require lower ratings than that of the main power circuit components. The proposed auxiliary circuit contributes less power loss because it is connected in parallel to main switch and is active only for very short duration over a switching period. The auxiliary circuit is designed such that main switch turns-on exactly at zero voltage and auxiliary switch turns-on at ZCS; and both the switches are turned off at near ZVS. All the other semiconductor uncontrolled switches are turned on and off at exactly/ ZVS and/or ZCS. In this manner, the proposed ZVT topology minimizes the switching losses of a proposed AC-DC PFC boost converter. There are no extra voltage and current stresses on all semiconductor switches and the drawback of the extra voltage stress of boost diode in the previously proposed passive snubber circuit (chapter 3) has been overcome in this topology.

The proposed ZVT topology is highly efficient as compared with conventional hard-switched and soft-switched passive snubber (proposed in chapter 3) and this is authenticated from efficiency graph. Efficiency graph also shows the wide load range applicability of the operation of the converter. Moreover, the proposed PFC converter with active auxiliary circuit has a simple structure and ease of control because of lesser number of components in comparison to the proposed PFC converter with auxiliary passive circuit presented in chapter 3 of this thesis. A prototype of specification 400 V, 500 W and 100 kHz converter is developed and tested in the Power Electronics and Drives laboratory to verify with the simulation result. The prototype operates at nearly unity input power factor with low THD over a wide range of load power.

4. Besides improving circuit topology and performance for improvement in efficiency, a high power expandability and higher power density could be realized by connecting three identical single-phase PFC boost converters in modular approach. In

addition, this approach also provides higher power density and less weight of PFC converter system.

The topologies of soft-switched converters proposed in chapter 3 and chapter 4 are used to develop prototypes of three-phase system in modular approach. The performance improvement of these three-phase converters (soft-switched with passive snubber and soft-switched with active snubber) is described in chapter 5 of this thesis separately. The features of soft-switching and its performance improvements described in single-phase soft-switched converters (chapter 3 and chapter 4) are retained in the three-phase modular systems (part I and part II respectively) and hence provide higher efficiency with primary objective of operating converters at nearly unity power factor.

This modular approach for a given specification of higher output power can reduce the count of passive components such as output capacitors (bulk in size), size and interconnections. Therefore, three-phase modular system in DPS could result in higher power density, better electrical performance, and easier thermal management. Moreover, due to the modular approach, entire front-end converter could be assembled by placing different integrated power electronics module together. Therefore, automatic manufacturing is possible, which can result in lower cost of the system.

6.2 Future Scope

This dissertation has tried out to break-through some technology barriers for future power management in the field of DPS. It has explored some good ideas and suitable solutions, but further investigation is necessary either for telecom and computer server applications or in related field of power management, which are suggested as follows:

6.2.1 Dynamic response in low power applications

In the chapter 2 of this thesis, it is revealed that faster dynamic response can be achieved for PFC boost converter with two sided PWM technique. This two sided PWM technique can be applied to fly-back (derived from buck-boost) and forward (derived from buck) converters operating as AC-DC PFC converters. These converters are preferred because they provide proper isolation between input and output; moreover any output voltage can be obtained by changing the transformer turns ratio of these converters for low power (<250 W) applications such as power sources to aeronautical and bio-medical equipments.

6.2.2 Design of PFC converter at very high switching frequency

In this thesis, PFC boost converters with auxiliary circuits are designed for switching frequency of 100 kHz in a university/laboratory level of engineering research. A very high power density PFC converters operating at very high switching frequency (hence reduction in size of passive components) has become important in these years.

The high output power density of the PFC converters is experiencing an adverse effect resulted from the applied switching frequency. Thus further improvement on the circuit analysis and printed circuit board (PCB) layout design could help in the improvement of high switching operating frequency. In spite of issues resulted from the very high switching frequency (> 400 kHz) converter design, selection of recently developed semiconductor devices (CoolMOS^{TM} MOSFETs, Silicon Carbide diodes) and PCB layout circuit design are among the important factors to consider, to maximize the capability of frequency-output power product in the very high switching frequency converter applications.

6.2.3 Unbalanced input voltage in modular approach

Continuation of the work described in chapter 5 of this dissertation could be focused on the unbalanced three-phase input voltages and output load conditions. The schemes presented in sections 5.1 and 5.3 of chapter 5 are based on balanced input voltages. Further investigation would also be required during grid disturbance such as voltage sag or swell.

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