TOPOLOGICAL ISSUES IN SINGLE PHASE POWER FACTOR CORRECTION

A THESIS

SUBMITTED IN PARTIAL FULFILLMENT OF THE

REQUIREMENTS FOR THE DEGREE OF

MASTER OF TECHNOLOGY

IN

POWER CONTROL AND DRIVES

By

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CERTIFICATE

This is to certify that the thesis entitled "**Topological issues in single phase power factor correction**" submitted by **Ms. Kurma Sai Mallika**, in partial fulfillment of the requirements for the award of Master of Technology in the Department of Electrical Engineering, with specialization in '**Power Control and Drives'** at National Institute of Technology, Rourkela (Deemed University) is an authentic work carried out by her under my supervision and guidance.

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other University/Institute for the award of any Degree or Diploma.

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Kurma Sai Mallika

M.Tech (Power Control and Drives)

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ABSTRACT

The equipment connected to an electricity distribution network usually needs some kind of power conditioning, typically rectification, which produces a non-sinusoidal line current due to the nonlinear input characteristic. With the steadily increasing use of such equipment, line current harmonics have become a significant problem. Their adverse effects on the power system are well recognized. They include increased magnitudes of neutral currents in three-phase systems, overheating in transformers and induction motors, as well as the degradation of system voltage waveforms. Several international standards now exist, which limit the harmonic content due to line currents of equipment connected to electricity distribution networks. As a result, there is the need for a reduction in line current harmonics, or *Power Factor Correction - PFC*.

There are two types of PFC's. 1) Passive PFC, 2) Active PFC. The active PFC is further classified into low-frequency and high-frequency active PFC depending on the switching frequency. Different techniques in passive PFC and active PFC are presented here.

Among these PFC's we will get better power factor by using high-frequency active PFC circuit. Any DC-DC converters can be used for this purpose, if a suitable control method is used to shape its input current or if it has inherent PFC properties. The DC-DC converters can operate in Continuous Inductor Current Mode – CICM, where the inductor current never reaches zero during one switching cycle or Discontinuous Inductor Current Mode - DICM, where the inductor current is zero during intervals of the switching cycle.

In DICM, the input inductor is no longer a state variable since its state in a given switching cycle is independent on the value in the previous switching cycle. The peak of the inductor current is sampling the line voltage automatically. This property of DICM input circuit can be called "self power factor correction" because no control loop is required from its input side.

In CICM, different control techniques are used to control the inductor current. Some of them are (1) peak current control (2) average current control (3) Hysteresis control (4) borderline control. These control techniques specifically developed for PFC boost converters are analyzed. For each control strategy advantages and drawbacks are highlighted and information on available commercial IC's is given.

This high frequency switching PFC stage also has drawbacks, such as: it introduces additional losses, thus reducing the overall efficiency; it increases the EMI, due to the high-frequency content of the input current.

Some of the EMI requirements are discussed. But the level of high-frequency EMI is much higher with a considerable amount of conduction and switching losses. This high-frequency EMI will be eliminated by introducing an EMI filter in between AC supply and the diode bridge rectifier.

The efficiency will be improved by reducing the losses using soft switching techniques such as 'Zero Voltage Switching'- (ZVS), 'Zero Voltage Transition' (ZVT), and 'Zero Current Switching'- (ZCS).

We study circuit techniques to improve the efficiency of the PFC stage by lowering the conduction losses and/or the switching losses. Operation of a ZVT converter will be discussed, in which the switching losses of the auxiliary switch are minimized by using an additional circuit applied to the auxiliary switch. Besides the main switch ZVS turned-on and turned-off, and the auxiliary switch ZCS turned-on and turned-off near ZVS. Since the active switch is turned-on and turned-off softly, the switching losses are reduced and the higher efficiency of the system is achieved.

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CHAPTER 1

INTRODUCTION

Nonlinear loads and their effects

Standards regulating line current harmonics

Power factor correction

Applications of PFC

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1. INTRODUCTION:

There has been a need to control disturbances to the supply network almost since it was first constructed in the late 19th century. The first of these was the British Lighting Clauses Act of 1899 that prevented uncontrolled arc-lamps from causing flicker on incandescent lamps. With the growth of electronic equipment in the 1970's, it became necessary to control the disturbances caused by these increasing electronic equipment.

The growth of consumer electronics has meant that the average home has a plethora of mains driven electronic devices and not just television sets. Invariably these electronic devices have mains rectification circuits, which is the dominant cause of mains harmonic distortion. Most modern electrical and electronic apparatus use some form of ac to dc power supply within their architecture and it is these supplies that draw pulses of current from the ac network during each half cycle of the supply waveform. The amount of reactive power drawn by a single apparatus (a domestic television for example) may be small, but within a typical street there may be 100 or more TVs drawing reactive power from the same supply phase resulting in a significant amount of reactive current flow and generation of harmonics. Power electronic converters are becoming more popular in industrial, commercial and residential applications for reducing size and weight, as well as for increasing performance and functionality.

The domestic tariff meters do not detect this reactive current and the mismatch between the power generated and that used results in a loss of revenue to the utilities. Furthermore 3-phase unbalance can also be created within a housing scheme since different streets are supplied on different phases. The unbalance current flows in the neutral line of a star configuration causing heating and in extreme cases cause burn out of the conductor. Also the reactive current manifests itself as distortion of the voltage waveform of the ac supply. If an apparatus is sensitive to such voltage distortion, an EMC problem exists. Moreover the harmonic content of this pulsating current causes additional losses and dielectric stresses in capacitors and cables, increasing currents in windings of rotating machinery and transformers and noise emissions in many products, and bringing about early failure of fuses and other safety components.

The major contributor to this problem in electronic apparatus is the mains rectifier. In recent years, the number of rectifiers connected to utilities has increased rapidly, mainly due to the growing use of computers.

1.1 NONLINEAR LOADS AND THEIR EFFECT ON THE ELECTRICITY DISTRIBUTION NETWORK:

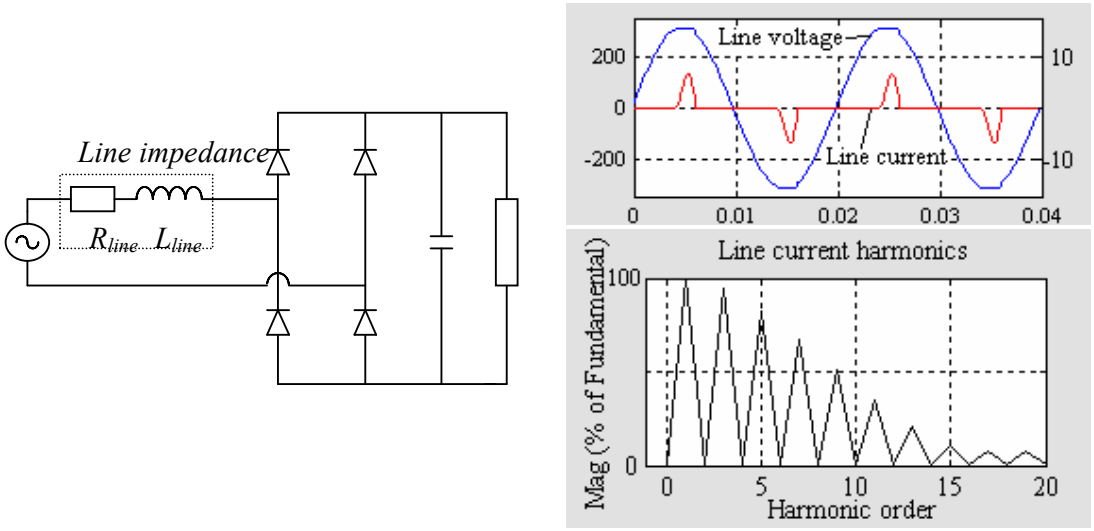
The equipment connected to an electricity distribution network usually needs some kind of power conditioning, typically rectification, which produces a non-sinusoidal line current due to the non-linear input characteristic.

Line-frequency diode rectifiers convert AC input voltage into DC output voltage in an uncontrolled manner. Single-phase diode rectifiers are needed in relatively low power equipment that needs some kind of power conditioning, such as electronic equipment and household appliances. For higher power, three-phase diode rectifiers are used. In both single- and three-phase rectifiers, a large filtering capacitor is connected across the rectifier output to obtain DC output voltage with low ripple. As a consequence, the line current is non-sinusoidal.

In most of these cases, the amplitude of odd harmonics of the line current is considerable with respect to the fundamental. While the effect of a single low power nonlinear load on the network can be considered negligible, the cumulative effect of several nonlinear loads is important. Line current harmonics have a number of undesirable effects on both the distribution network and consumers.

These effects include:

1. Losses and overheating in transformers, shunt capacitors, power cables, AC machines and switchgear, leading to premature aging and failure.
2. Excessive current in the neutral conductor of three-phase four-wire systems, caused by odd triple-n current harmonics (triple-*n*: 3^{rd}, 9^{th}, 15^{th}, etc.). This leads to overheating of the neutral conductor and tripping of the protective relay.
3. Reduced power factor, hence less active power available from a wall outlet having a certain apparent power rating.
4. Electrical resonances in the power system, leading to excessive peak voltages and RMS currents, and causing premature aging and failure of capacitors and insulation.
5. Distortion of the line voltage via the line impedance shown in Fig.1.1 where the typical worst case values: R_{Line}=0.5Ω and L_{Line}=1mH have been considered. The effect is stronger in weaker grids. For example, some electronic equipment is dependent on accurate determination of aspects of the voltage wave shape, such as amplitude, RMS and zero-crossings.



(a) *(b)*

Fig. 1.1: Single-phase diode bridge rectifier: (a) Schematic; (b) Typical line voltage and line current waveforms (upper plot) and odd line current harmonics (lower plot). And the line current has THD=1.5079 and power factor of 0.5475.

6. The distorted line voltage may affect other consumers connected to the electricity distribution network.
7. Telephone interference.
8. Errors in metering equipment.
9. Increased audio noise.
10. Cogging or crawling in induction motors, mechanical oscillation in a turbine-generator combination or in a motor-load system.

1.2 STANDARDS REGULATING LINE CURRENT HARMONICS:

The previously mentioned negative effects of line current distortion have prompted a need for setting limits for the line current harmonics of equipment connected to the electricity distribution network.

Standardization activities in this area have been carried out for many years. As early as 1982, the International Electro-technical Committee-IEC published its standard IEC 555-2, which was also adopted in 1987 as European standard EN 60555-2, by the European Committee for Electro-technical Standardization - CENELEC. Standard IEC 555-2 has been replaced in 1995 by standard IEC 1000-3-2 [1], also adopted by CENELEC as European standard EN 61000-3-2.

1.2.1 Standard IEC 1000-3-2:

1. It applies to equipment with a rated current up to and including $16A_{rms}$ per phase which is to be connected to 50Hz or 60 Hz, 220-240V_{rms} single-phase or 380-415V_{rms} three-phase mains.
2. Electrical equipments are categorized into four classes (A, B, C, and D), for which specific limits are set for the harmonic content of the line current.
3. These limits do not apply for the equipment with rated power less than 75W, other than lighting equipment.

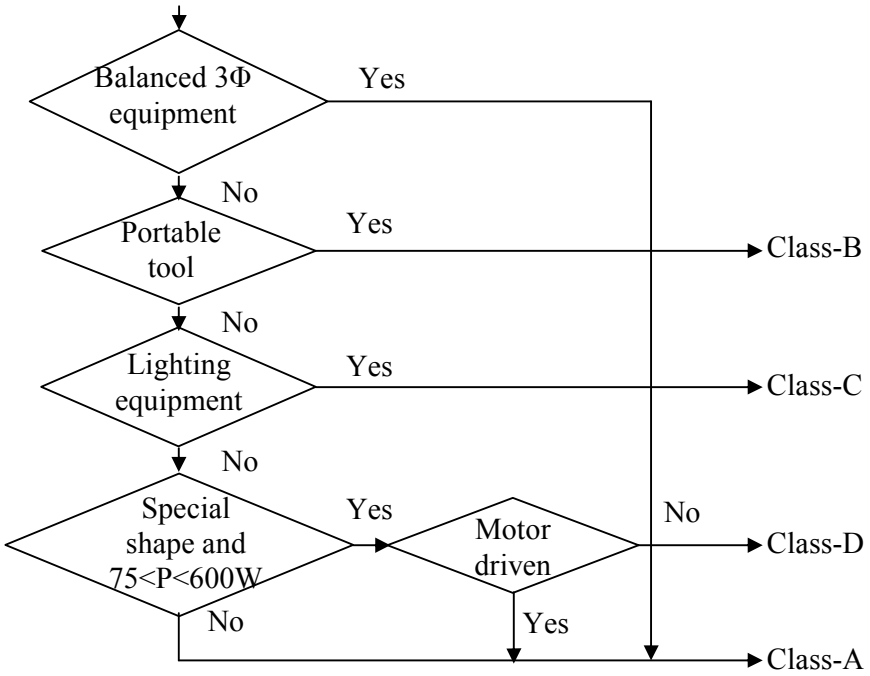


Fig: 1.2. Classification of equipment under Standard IEC 1000-3-2

CLASS-A:

It includes balanced three-phase equipments, household appliances, excluding the equipment identified as class-D. Equipment not specified in one of the other three classes should be considered as class-A equipment.

CLASS-B:

It includes portable tools, and non-professional arc welding equipment.

CLASS-C:

It includes lighting equipment (except for dimmers for incandescent lamps, which belong to class-A).

CLASS-D:

Equipment with special line current shape i.e. includes equipment having an active input power less than or equal to 600w, of the following types:

i. Personal computers.
ii. Personal computer monitors.
iii. Television receivers.

The classification can also be represented using the flowchart: Fig: 1.2

Limits in standard IEC 1000-3-2:

Besides standard IEC 1000-3-2, there are also other documents addressing the control of current harmonics. Standard IEC/TS 61000-3-4 gives recommendations applicable to equipment with rated current greater than $16A_{rms}$ per phase and intended to be connected to 50Hz or 60Hz mains, with nominal voltage up to $240V_{rms}$ single-phase, or up to $600V_{rms}$ three-phase.

Table 1.1(a): Limits for Class-A and Class-D

	Harmonic order	Class-A	Class-D	
		A_{rms}	A_{rms}	*mA/W*
odd harmonics	3	2.30	2.30	3.40
	5	1.14	1.14	1.90
	7	0.77	0.77	1.00
	9	0.40	0.40	0.50
	11	0.33	0.33	0.35
	13	0.21	0.21	0.29
	15 to 39	2.25/n	2.25/n	3.85/n
Even harmonics	2	1.08		
	4	0.43		
	6	0.30		
	8 to 40	1.84/n		

Table 1.1(b): Limits for Class-B and C

	Harmonic order	Class-B	Class-C
		A_{rms}	%
odd harmonics	3	3.45	30*PF
	5	1.71	10
	7	1.15	7
	9	0.60	5
	11	0.49	3
	13	0.31	3
	15 to 39	3.375/n	3
Even harmonics	2	1.62	2
	4	0.64	
	6	0.45	
	8 to 40	2.76/n	

1.2.2 Standard IEEE 519-1992:

Gives recommended practices and requirements for harmonic control in electrical power systems for both individual consumers and utilities [2]. The limits for line current harmonics are given as a percentage of the maximum demand load current I_L at the point of

common coupling-PCC at the utility. They decrease as the ratio I_{SC}/I_L decreases where I_{SC} is the maximum short circuit current at PCC, meaning that the limits are lower in weaker grids. This standard covers also high voltage loads of much higher power.

Limits in standard IEEE 519-1992:

Table 1.2: Odd harmonic limits:

I_{SC}/I_L (%)	h<11	11≤h<17	17≤h<23	23≤h<35	35≤h	TDD*
<20	4.0	2.0	1.5	0.6	0.3	5
20 to 50	7.0	3.5	2.5	1.0	0.5	8
50 to 100	10.0	4.5	4.0	1.5	0.7	12
100 to 1000	12.0	5.5	5.0	2.0	1.0	15
>1000	15.0	7.0	6.0	2.5	1.4	20

*TDD: Total Demand Distortion is the harmonic current distortion in % of a maximum demand load current

The thesis work focuses on methods to achieve compliance with standard IEC 1000-3-2 in single-phase systems.

1.3 POWER FACTOR CORRECTION:

Reduction of line current harmonics is needed in order to comply with the standard. This is commonly referred to as the Power Factor Correction – PFC, which may be misleading.

When an electric load has a *PF* lower than 1, the apparent power delivered to the load is greater than the real power that the load consumes. Only the real power is capable of doing work, but the apparent power determines the amount of current that flows into the load, for a given load voltage.

Power factor correction (PFC) is a technique of counteracting the undesirable effects of electric loads that create a power factor *PF* that is less than 1.

The power factor is defined as the ratio of the active power *P* to the apparent power *S*:

$$PF = P/S \tag{1.1}$$

For purely sinusoidal voltage and current, the classical definition is obtained:

$$PF = \cos\Phi \tag{1.2}$$

where $\cos\Phi$ is the displacement factor of the voltage and current. In classical sense, PFC means compensation of the "*displacement factor*".

The line current is non-sinusoidal when the load is nonlinear. For sinusoidal voltage and non-sinusoidal current the *PF* can be expressed as

$$PF = \frac{V_{rms} I_{1rms}}{V_{rms} I_{rms}} \cos \Phi = \frac{I_{1rms}}{I_{rms}} \cos \Phi = K_P \cos \Phi \quad (1.3)$$

$$K_p = I_{1,rms} / I_{rms} \, , K_p \in [0,1] \quad (1.4)$$

K_p describes the harmonic content of the current with respect to the fundamental. Hence, the power factor depends on both harmonic content and displacement factor. K_p is referred to as purity factor or distortion factor.

The total harmonic distortion factor THD_i is defined as

$$THD_i = \frac{\sqrt{\sum_{n=2}^{\infty} I_{n,rms}^2}}{I_{1,rms}} \quad (1.5)$$

Hence the relation between K_p and THD_i is

$$K_P = \frac{1}{\sqrt{1 + THD_i^2}} \quad (1.6)$$

Standard IEC 1000-3-2 sets limits on the harmonic content of the current but does not specifically regulate the purity factor K_p or the total harmonic distortion of the line current THD_i .The values of K_p and THD_i for which compliance with IEC 1000-3-2 is achieved depend on the power level. For low power level, even a relatively distorted line current may comply with the standard. In addition to this, it can be seen from (1.6) that the distortion factor K_p of a waveform with a moderate THD_i is close to unity (e.g. K_p=0.989 for THD_i=15%). Considering (1.3) as well, the following statements can be made:

1. A high power factor can be achieved even with a substantial harmonic content. The power factor PF is not significantly degraded by harmonics, unless their amplitude is quite large (low K_p, very large THD_i).
2. Low harmonic content does not guarantee high power factor (K_p close to unity, but low $cos\Phi$).

<u>Benefits of high power factor:</u>

1. Voltage distortion is reduced.
2. All the power is active.
3. Smaller RMS current.
4. Higher number of loads can be fed.

Most of the research on PFC for nonlinear loads is actually related to the reduction of the harmonic content of the line current. There are several solutions to achieve PFC [3], [41]. Depending on whether active switches (controllable by an external control input) are used or not, PFC solutions can be categorized as "*Passive*" or "*Active*".

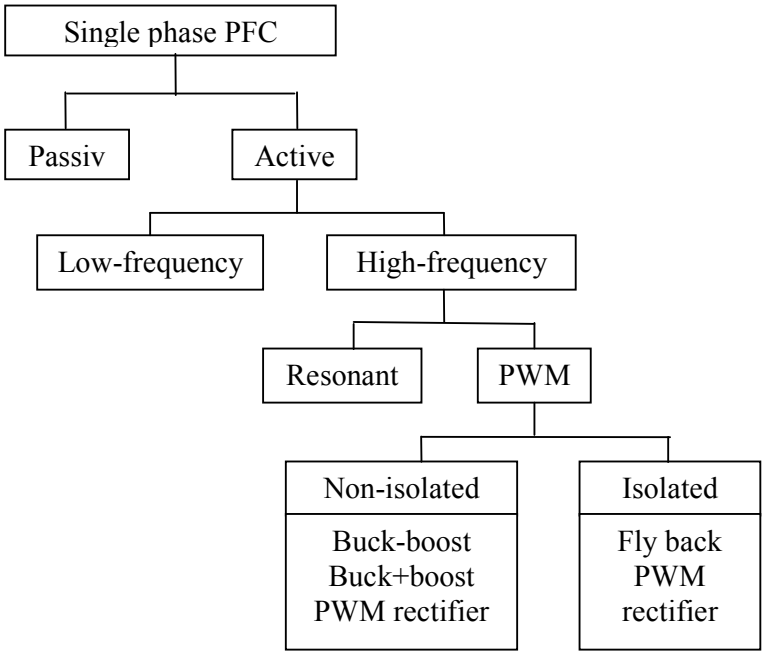


Fig. 1.3 Various Single-Phase off-line PFC topologies

In "*Passive*" PFC, only passive elements are used in addition to the diode bridge rectifier, to improve the shape of the line current. Obviously, the output voltage is not controllable.

For "*Active*" PFC, active switches are used in conjunction with reactive elements in order to increase the effectiveness of the line current shaping and to obtain controllable output voltage. The switching frequency further differentiates the active PFC solutions into two classes.

In "*low-frequency*" active PFC, switching takes place at low-order harmonics of the line-frequency and it is synchronized with the line voltage. In "*high-frequency*" active PFC, the switching frequency is much higher than the line frequency.

1.4 APPLICATIONS OF PFC:

1.4.1 Electricity industry: Power factor correction of linear loads.

Power factor correction is achieved by complementing an inductive or a capacitive circuit with a (locally connected) reactance of opposite phase. For a typical phase lagging *PF*

load, such as a large induction motor, this would consist of a capacitor bank in the form of several parallel capacitors at the power input to the device.

Instead of using a capacitor, it is possible to use an unloaded synchronous motor. This is referred to as a synchronous condenser. It is started and connected to the electrical network. It operates at full leading power factor and puts VARs onto the network as required to support a system's voltage or to maintain the system power factor at a specified level. The condenser's installation and operation are identical to large electric motors.

The reactive power drawn by the synchronous motor is a function of its field excitation. Its principal advantage is the ease with which the amount of correction can be adjusted; it behaves like an electrically variable capacitor.

1.4.2 Switched mode power supply: Power factor correction of non-linear loads.

A typical switched-mode power supply first makes a DC bus, using a bridge rectifier or similar circuit. The output voltage is then derived from this DC bus. The problem with this is that the rectifier is a non-linear device, so the input current is highly non-linear. That means that the input current has energy at harmonics of the frequency of the voltage.

This presents a particular problem for the power companies, because they cannot compensate for the harmonic current by adding capacitors or inductors, as they could for the reactive power drawn by a linear load. Many jurisdictions are beginning to legally require PFC for all power supplies above a certain power level.

The simplest way to control the harmonic current is to use a filter: it is possible to design a filter that passes current only at line frequency (e.g. 50 or 60 Hz). This filter kills the harmonic current, which means that the non-linear device now looks like a linear load. At this point the power factor can be brought to near unity, using capacitors or inductors as required. This filter requires large-value high-current inductors, however, which are bulky and expensive.

It is also possible to perform *active PFC*. In this case, a boost converter is inserted between the bridge rectifier and the main input capacitors. The boost converter attempts to maintain a constant DC bus voltage on its output while drawing a current that is always in phase with and at the same frequency as the line voltage. Another switch-mode converter inside the power supply produces the desired output voltage from the DC bus. This approach requires additional semiconductor switches and control electronics, but permits cheaper and smaller passive components. It is frequently used in practice. Due to their very wide input

voltage range, many power supplies with active PFC can automatically adjust to operate on AC power from about 100 V (Japan) to 240 V (UK). That feature is particularly welcome in power supplies for laptops and cell phones.

1.5 OBJECTIVE OF THIS THESIS WORK:

To better define the scope of this work; let us consider the widely used block diagram of the power supply shown in fig1.4.

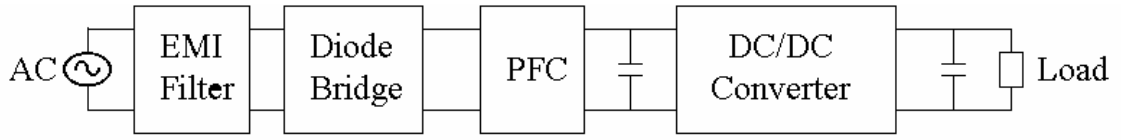


Fig1.4: Block diagram of power supply with active PFC.

Here, the PFC stage can be performed by either *passive* or *active* PFC. But a high-frequency PFC stages shapes input current as close as possible to a sinusoidal waveform which is in phase with the input voltage. Thus, from the electrical point of view, the equipment connected to the line behaves like a resistive load. The voltage on the storage capacitor at the output of the PFC stage has a ripple at twice the line-frequency. Therefore, a second DC/DC switching converter is used to provide a tightly regulated output voltage and, eventually, to provide galvanic isolation. As an example, a typical telecom power supply uses a Forward DC/DC converter to convert the 380-400V_{dc} output voltage of the PFC stage, to 48V_{dc} output voltage, as well as to provide galvanic isolation. The load of the PFC stage can be also an inverter in AC drives applications.

While the high-frequency switching PFC stage reduces the line current harmonics, it also has drawbacks, such as: it introduces additional losses, thus reducing the overall efficiency; it increases the EMI, due to the high-frequency content of the input current; and it increases the complexity of the circuit, with negative effects on the reliability of the equipment, as well as on its size, weight and cost. The general aim of this thesis work is to investigate high-frequency switching circuit topologies and methods to be applied in the PFC stage, which would alleviate some of the aforementioned drawbacks. The thesis addresses several aspects which can be divided as follows.

Different solutions to implement passive PFC, advantages and disadvantages will be discussed in chapter 2. Then active PFC techniques will be discussed in chapter 3.

Among these PFC's we will get better power factor by using high-frequency active PFC circuit. Any DC-DC converters can be used for this purpose, if a suitable control method

is used to shape its input current or if it has inherent PFC properties. The converters can operate in Continuous Inductor Current Mode – CICM, where the inductor current never reaches zero during one switching cycle, which will be discussed in chapter 5 or Discontinuous Inductor Current Mode - DICM, where the inductor current is zero during intervals of the switching cycle, which will be discussed in the chapter 4.

This high frequency switching PFC stage also has drawbacks, such as: it introduces additional losses, thus reducing the overall efficiency; it increases the EMI, due to the high-frequency content of the input current. This high-frequency EMI can be eliminated by introducing one EMI filter in between the input voltage and the diode bridge. Some of the EMI requirements will be discussed in chapter 6.

We studied circuit techniques to improve the efficiency of the PFC stage by lowering the conduction losses and/or the switching losses. Operation of a ZVT converter will be discussed in chapter 7 to improve the efficiency of the PFC stage.

CHAPTER 2

PASSIVE PFC

Diode bridge rectifier

Passive PFC

Advantages of passive PFC

Disadvantages of passive PFC

Summary

2. PASSIVE PFC:

As mentioned in the previous chapter, the diode bridge rectifier, shown again in Fig. 2.1(a), has non-sinusoidal line current. This is because most loads require a supply voltage V_2 with low ripple, which is obtained by using a correspondingly large capacitance of the output capacitor C_f. Consequently, the conduction intervals of the rectifier diodes are short and the line current consists of narrow pulses with an important harmonic content.

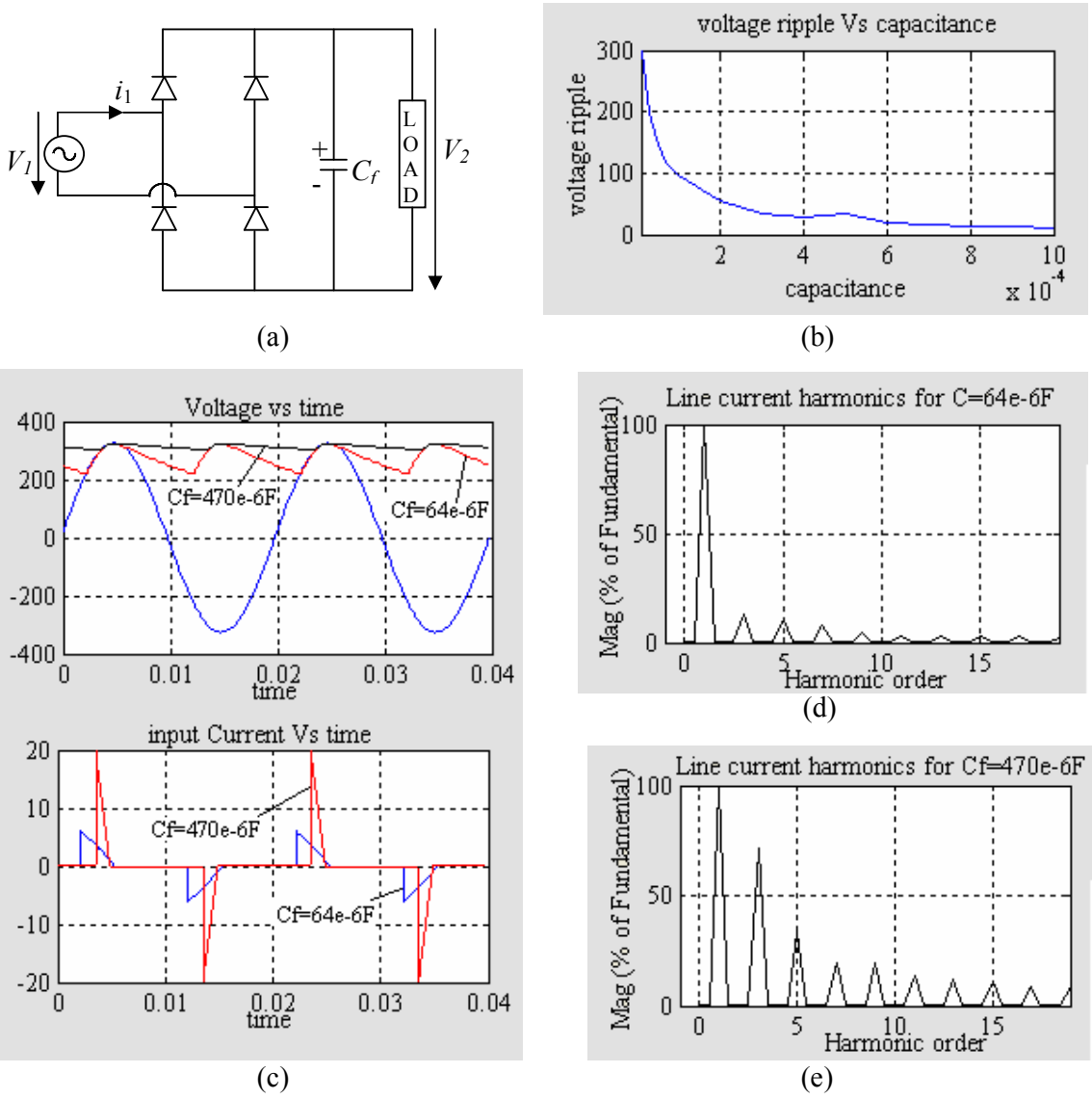


Fig. 2.1 Diode bridge rectifier: (a) Schematic; (b) Voltage ripple as a function of the output filter capacitance; (c) Line voltage and output voltage (upper plot), and input current (lower plot), with V_1=230V_{rms} 50Hz and constant power load P = 200W . With C_f = 470μF, the line current has K_p = 0.4349, cosΦ = 0.9695 and PF =0.4216, and the output voltage ripple is ΔV_2 =25V. With C_f = 64μF, the line current has K_p = 0.6842, cosΦ = 0.8805 and PF = 0.6024, and the output voltage ripple is ΔV_2 =105V; (d) and (e) Line current harmonics with C_f=64μF and C_f=470μF respectively.

2.1 DIODE BRIDGE RECTIFIER:

Before going to *passive PFC*, let us discuss the simplest way to improve the shape of the line current, without adding additional components, is to use a lower capacitance of the output capacitor C_f. When this is done, the ripple of the output voltage increases (shown in fig. 2.1(b)) and the conduction intervals of the rectifier diodes widen. The shape of the input current becomes also dependent on the type of load that the rectifier is supplying, resistive or constant power, as opposed to the case of negligible output voltage ripple where the type of load does not affect the line current. This solution can be applied if the load accepts a largely pulsating DC supply voltage and it is used, for example, in some handheld tools.

The concept is highlighted by the simulated waveforms shown in Fig. 2.1, for two values of the output capacitor and assuming constant power load. The shape of the input current is improved to certain extent with the lower capacitance, at the expense of increased output voltage ripple, as can be seen also from the Fig. 2.1(b).

The method presented above has severe limitations: it does not reduce substantially the harmonic currents and the output voltage ripple is large, which is not acceptable in most of the cases. Several other methods to reduce the harmonic content of the line current in single-phase systems exist, and an overview of the *Passive* PFC is presented next.

2.2 PASSIVE PFC:

Passive PFC methods use only passive elements are used in addition to the diode bridge rectifier, to improve the shape of the line current. Passive Power Factor correction is simply the use of an inductor in the input circuits. We used to call this an inductive input filter earlier. If the inductor is sufficiently large, it stores sufficient energy to maintain the rectifiers in conduction throughout the whole of their half cycle and reduces the harmonic distortion caused by discontinuous conduction of these rectifiers.

2.2.1 Rectifier with AC side inductor:

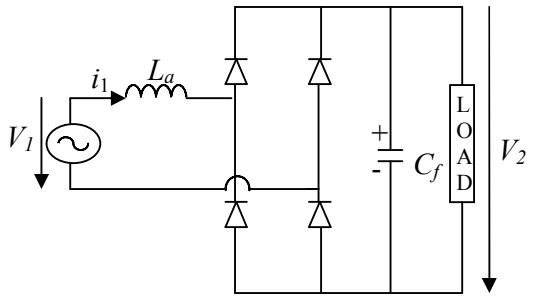


Fig.2.2 Rectifier with AC side inductor. (a) Schematic;

One of the simplest methods is to add an inductor at the AC-side of the diode bridge, in series with the line voltage as shown in Fig.2.2 (a), and to create circuit conditions such that the line current is zero during the zero-crossings of the line voltage [4, pp.91-

94]. The maximum power factor that can be obtained is $PF = 0.78$, with the theoretical assumption of constant DC output voltage. Simulated results for the rectifier with AC-side inductor are presented in Fig.2.2. From the simulation results we can observe that increase in inductance L_a results in improved line current waveform with a lower THD_i, a better distortion factor and a better power factor.

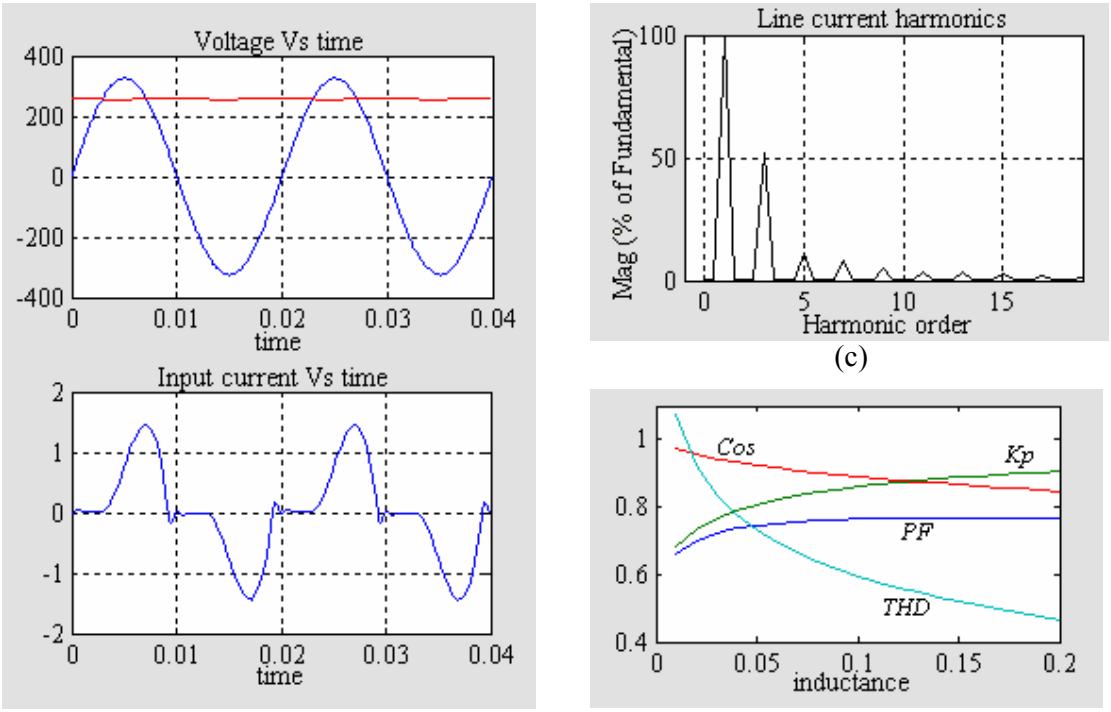


Fig.2.2 (continued...) Rectifier with AC-side inductor. (b)Line voltage, output voltage (upper plot) and line current (lower plot) with V_1=230V_{rms} 50Hz, resistive load R=500Ω, C_f =470μF, and L_a=130mH. The line current has K_p=0.8778, CosΦ =0.8758 and PF =0.7688. The output voltage is V_2 =257V; (c) Line current harmonics; (d) Variation of different parameters as a function of inductance.

2.2.2 Rectifier with DC-side inductor:

The inductor can be also placed at the DC-side, as shown in Fig. 2.3(a) [5]. The

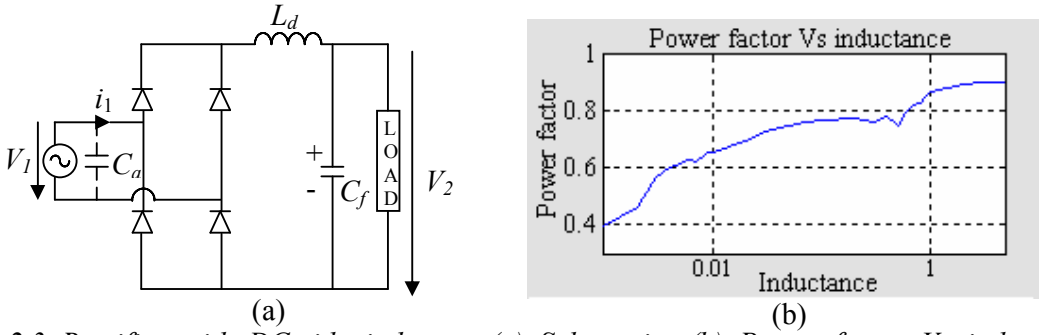
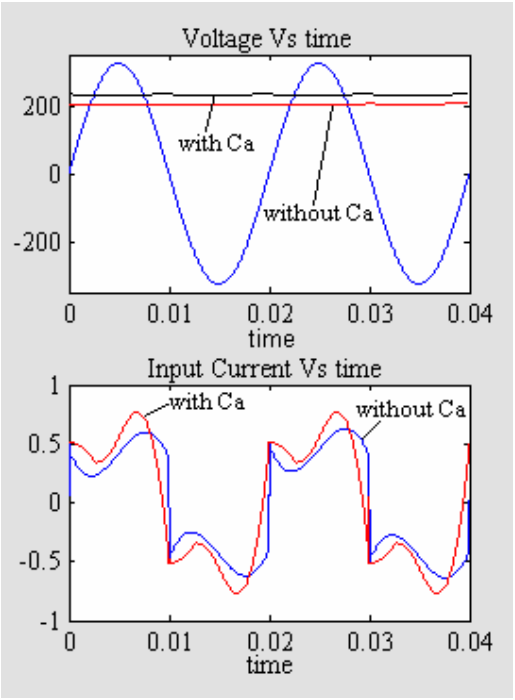
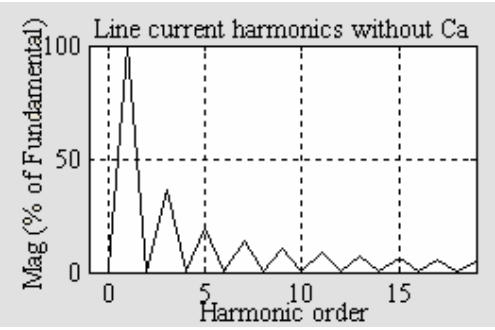


Fig.2.3 Rectifier with DC-side inductor. (a) Schematic; (b) Power factor Vs inductance without C_a;

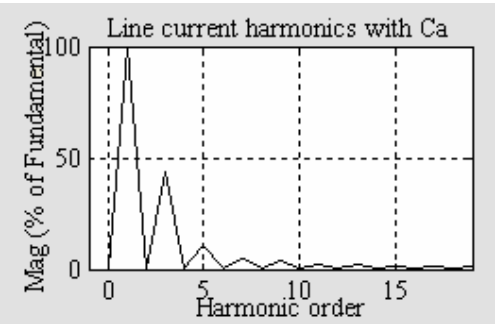
inductor current is continuous for a large enough inductance L_d. In the theoretical case of near infinite inductance, the inductor current is constant, so the input current of the rectifier has a square shape and the power factor is $PF = 0.9$, shown in Fig. 2.3(b). However, operation



(c)



(d)



(e)

Fig. 2.3(continued...) Rectifier with DC-side inductor. (c)Line voltage, output voltage (upper plot) and line current (lower plot) with V_1 = 230V_{rms} 50Hz, resistive load R=500Ω, and C_f =470μF. With L_a=275mH and without C_a, the line current has K_p = 0.8846, cosΦ = 0.9580 and PF = 0.8474, and the output voltage is V_2= 210V. With L_a=275mH and with C_a=4.8μF, the line current has K_p=0.9128, cosΦ=0.9989 and PF=0.9118, and the output voltage is V_2=231V. (d) and (e) Line current harmonics without and with C_a=4.8μF respectively.

close to this condition would require a very large and impractical inductor, as illustrated by the simulated line current waveform for L_d =3H (without C_a), shown in Fig. 2.3(b). For lower inductance L_d, the inductor current becomes discontinuous. The maximum power factor that can be obtained in such a case is $PF = 0.78$, the operating mode being identical to the case of the AC-side inductor previously discussed. An improvement of the power factor can be obtained by adding the capacitor C_a between the bridge rectifier and AC power supply as shown in Fig. 2.3(a), which compensates for the displacement factor $cos\Phi$. A design for maximum purity factor K_p and unity displacement factor $cos\Phi$ is possible, leading to a maximum obtainable power factor $PF = 0.9118$. The simulation results for L_d = 275mH with and without C_a=4.8μF is shown in Fig. 2.3(c).

The shape of the input current can be further improved by using a combination of low pass input and output filters.

2.2.3 Rectifier with series-resonant band-pass filter:

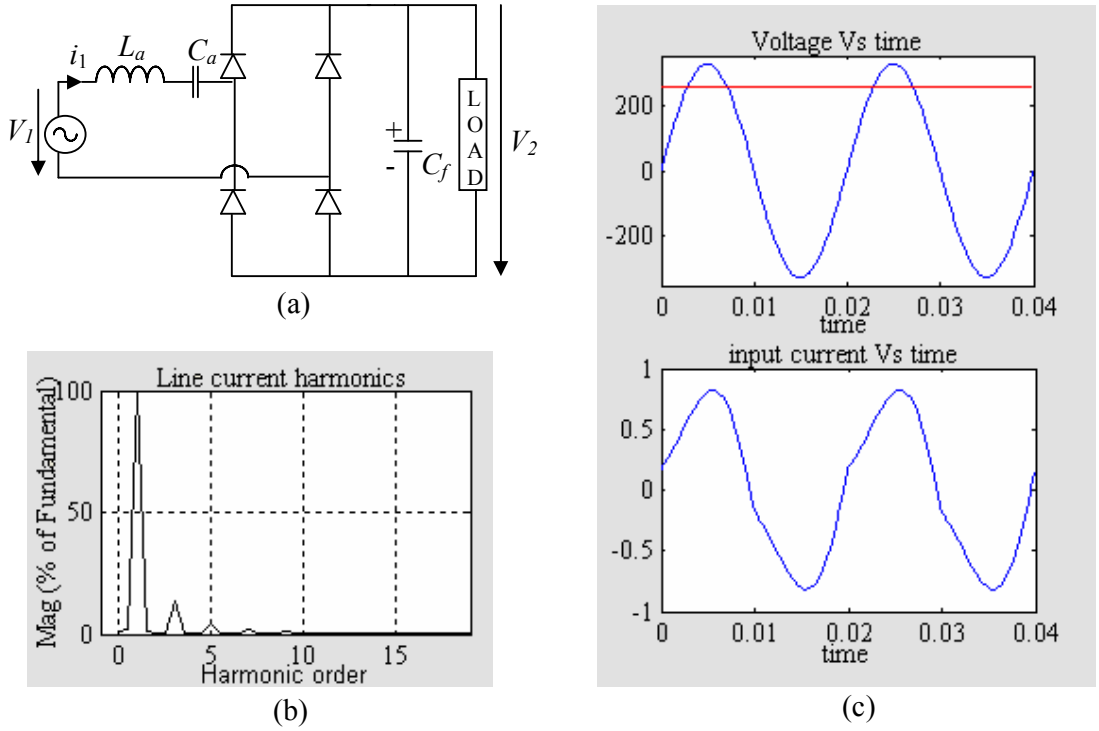


Fig.2.4 Rectifier with series-resonant band-pass filter. (a) Schematic; (b) Line current harmonics; (c) Line voltage, output voltage (upper plot) and line current (lower plot) for V_1=230V_{rms} 50Hz, resistive load R=500Ω, C_f =470μF, L_a=1.5H and C_a=6.75μF. The line current has K_p=0.9937, cosΦ=0.9997 and PF=0.9934. The output voltage is V_2=254V.

A band-pass filter of the series-resonant type, tuned at the line-frequency $1/2\pi\sqrt{L_aC_a}$, is introduced in-between the AC source and the bridge rectifier as shown in Fig. 2.4 together with simulated waveforms [4, pp. 488-489]. By this method we can get almost unity power factor. For 50Hz networks, large values of the reactive elements are needed. Therefore, this solution is more practical for higher frequencies, such as for 400Hz and especially 20 kHz networks.

2.2.4 Rectifier with parallel-resonant band-stop filter:

The solution using a band-stop filter of the parallel-resonant type [6] is presented in Fig. 2.5 together with simulated waveforms. The filter is tuned at the third harmonic, hence it allows for lower values of the reactive elements when compared to the series-resonant band-pass filter. It can be observed from the Fig.2.5 (b); the third harmonic component is completely eliminated. This method maintains high input power factor of 0.9574.

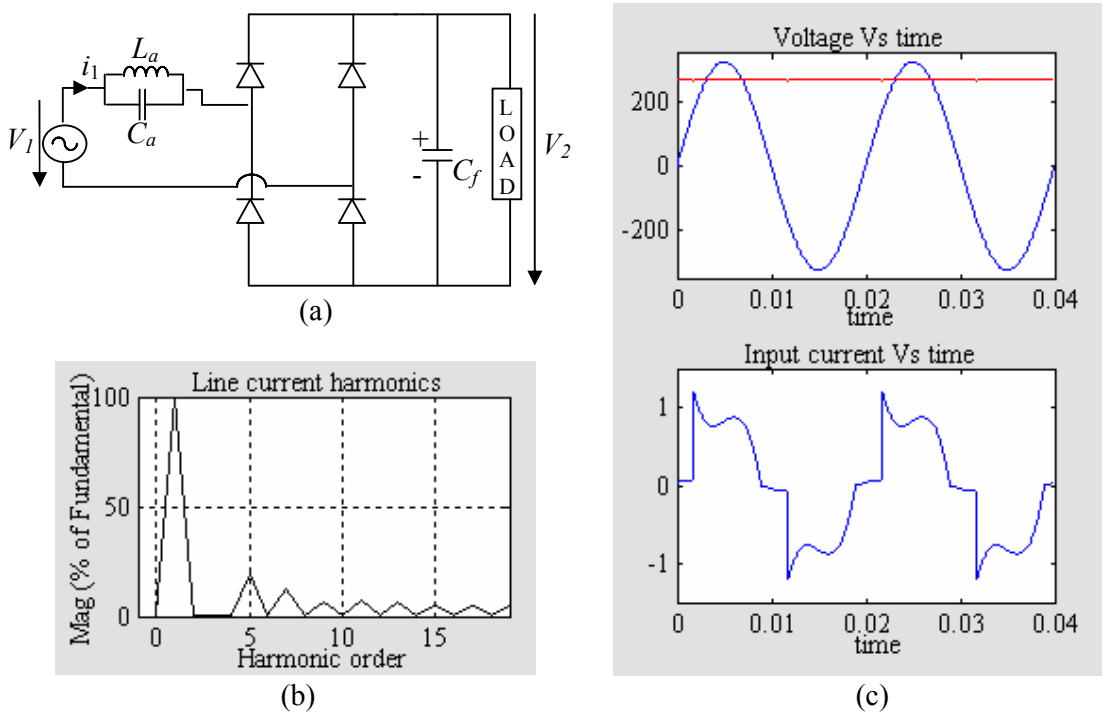


Fig.2.5 Rectifier with parallel-resonant band-stop filter. (a) Schematic; (b) Line current harmonics; (c) Line voltage and output voltage (upper plot) and line current (lower plot) for V_1=230V_{rms} 50Hz, resistive load R=500Ω, filter capacitance C_f=470μF, band-stop filter components L_p=240mH, C_p=470μF tuned at third harmonic. Line current has K_p=0.9586, cosΦ=0.9987, and PF=0.9574. The output voltage is V_2=269V.

2.2.5 Rectifier with harmonic trap filter:

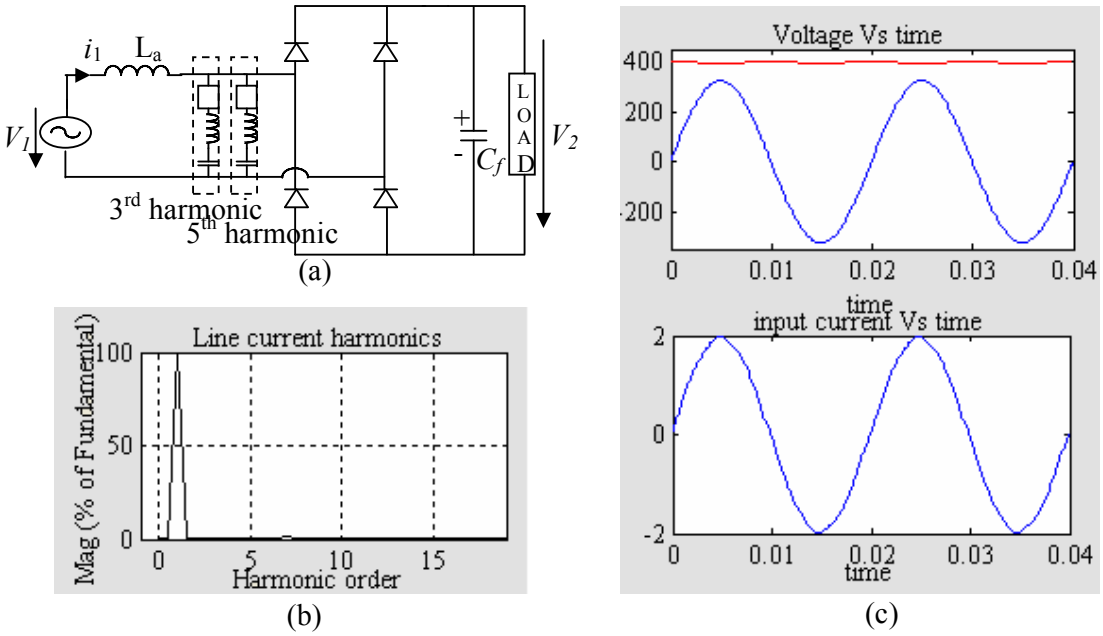


Fig. 2.6 Rectifier with harmonic trap filter: a) Schematic; (b) Line current harmonics; (c) Line voltage, output voltage (upper plot) and line current (lower plot) with V_1=230V_{rms} 50Hz, resistive load R=500Ω, C_f =470μF, and filter values L_a=400mH, L_3=200mH, C_3=5.6μF, R_3=0.1Ω, L_5=100mH, C_5=4.04μF, and R_5=0.1Ω; The line current has K_p= 0.9999, cosΦ=0.9995 and PF=0.9994. The output voltage is V_2=400V.

Another possibility is to use a harmonic trap filter [16, pp. 575-582]. The harmonic trap consists of a series-resonant network, connected in parallel to the AC source and tuned at a harmonic that must be attenuated. For example, the filter shown in Fig. 2.6(a) has two harmonic traps, which are tuned at the 3rd and 5th harmonic respectively. As seen from Fig. 2.6(c), the line current improvement is very good, at the expense of increased circuit complexity. Harmonic traps can be used also in conjunction with other reactive networks, such as a band-stop filter.

2.2.6 Capacitor-fed rectifier:

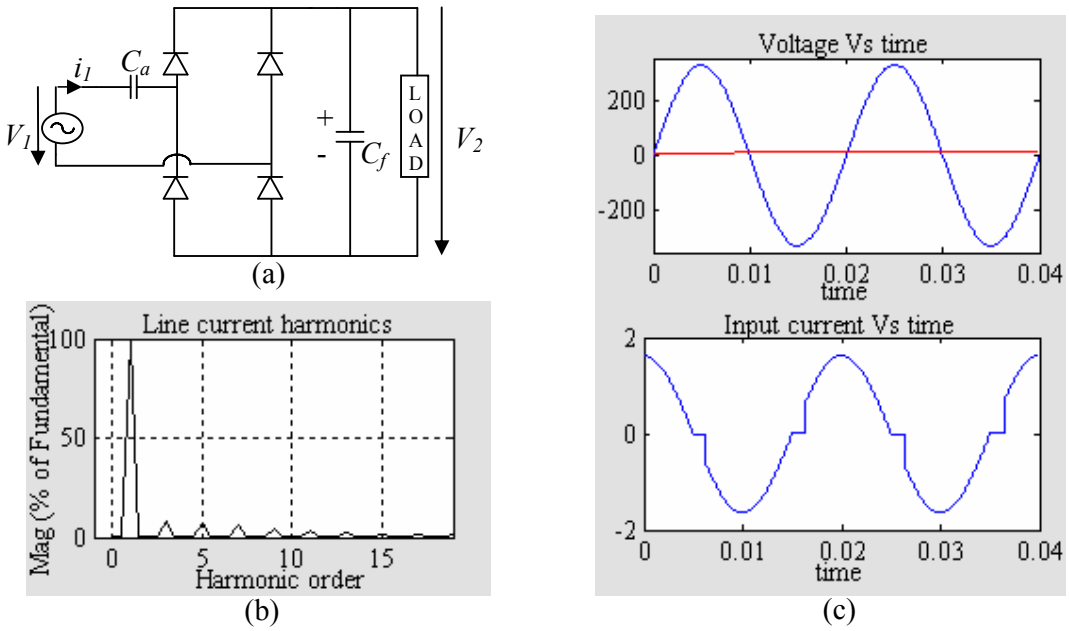


Fig.2.7 Capacitor-fed rectifier. (a) Schematic; (b) Line current harmonics; (c) Line voltage, output voltage (upper plot) and line current (lower plot) with V_1=230V_{rms} 50Hz, resistive load R=500Ω, C_f =4700μF, and C_a=16μF. The line current has K_p=0.9824, cosΦ=0.076 and PF=0.0747. The output voltage is V_2 =12V.

The capacitor-fed rectifier [7], shown in Fig. 2.7 together with simulated waveforms, is a very simple circuit that ensures compliance with standard IEC 1000-3-2 for up to approximately 250W input power at a 230V_{rms} line voltage. The conversion ratio is a function of X_a/R, where $X_a=1/(\omega_L C_a)$. Therefore, it is possible to obtain a specific output voltage, which is nevertheless lower than the amplitude of the line voltage and strongly dependent on the load. Despite the harmonic current reduction, the power factor is extremely low. This is not due to current harmonics, but due to the series-connected capacitor that introduces a leading displacement factor *cosΦ*. An advantage could be that the leading displacement factor *cosΦ* can assist in compensating for lagging displacement factors elsewhere in the power system.

2.2.7 Rectifier with an additional inductor, capacitor and diode (LCD):

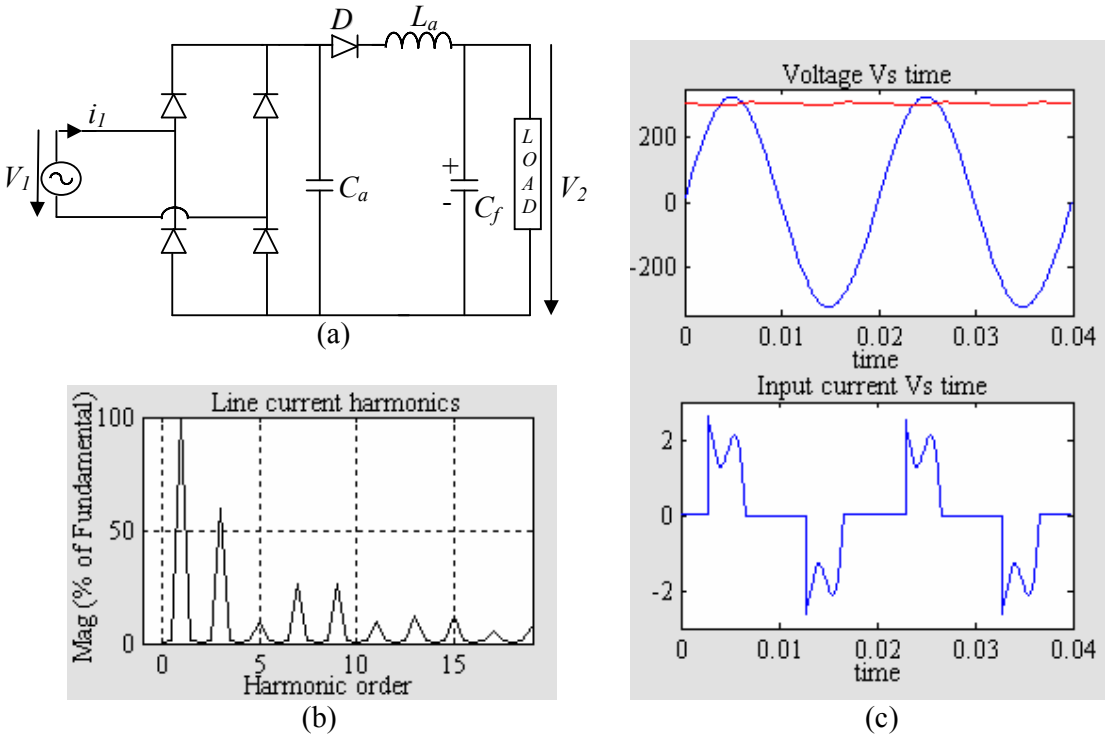


Fig.2.8 Rectifier with an additional inductor, capacitor and diode (LCD). (a) Schematic; (b) Line current harmonics; (c) Line voltage, output voltage (upper plot) and line current (lower plot) with $V_1=230V_{rms}$ *50Hz, resistive load* $R=500\Omega$, $C_f=470\mu F$, $C_a=40\mu F$, *and* $L_a=10mH$. *The line current has* $K_p= 0.7261$, $\cos\Phi=0.9947$ *and* $PF=0.7223$. *The output voltage is* $V_2 = 304V$.

The rectifier with an additional inductor, capacitor, and diode – *LCD* rectifier [8] – is shown in Fig.2.8, together with simulated waveforms. The circuit can be used to about 300W. The added reactive elements have relatively low values. The idea behind the circuit is linked to the previous definition of Class-D of the Standard IEC 1000-3-2. The circuit changes the shape of the input current and, while only a limited reduction of the harmonic currents can be obtained, it was also possible to change the classification of the circuit from Class-D to Class-A. The power-related limits of Class-D were avoided and the absolute limits of Class-A could be met for low power, in spite of the line current being relatively distorted.

2.2.8 Valley-fill rectifier:

Finally, the valley-fill rectifier [9] is shown in Fig.2.9, together with simulated waveforms.

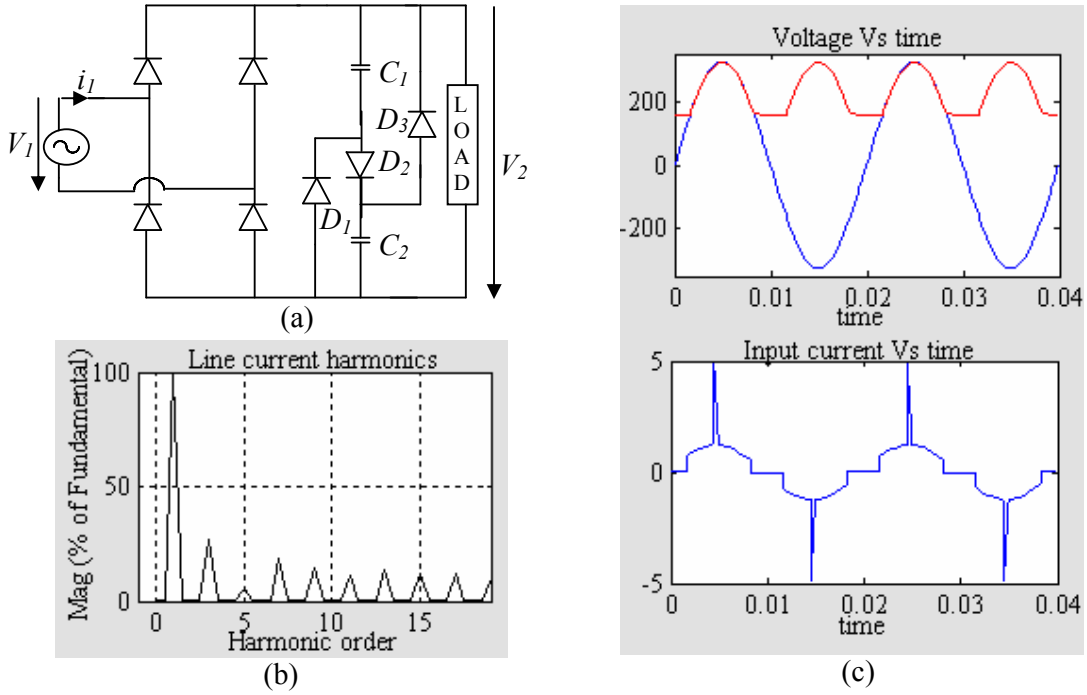


Fig.2.9 Valley-fill rectifier: (a) Schematic; (b) Line current harmonics; (c) Line voltage, output voltage (upper plot), and line current (lower plot) with V_1=230V_{rms} 50Hz, resistive load R=500Ω, and C_1=C_2=470μF. The line current has K_p=0.8724, cosΦ=0.998 and PF=0.8707. The output voltage ripple is ΔV_2=168V.

Much of the input current distortion is caused by the discontinuities which crosses from positive to negative, and then from negative to positive, during each cycle. Due to these discontinuities substantial amount of harmonics were introduced into the input current waveform. If this cross-over distortion can be lessened or eliminated, then the likelihood of using this circuit to meet the IEC specifications would be very high.

To maintain the flow of input current, a voltage doubler is inserted to feed the valley-fill circuit [10]. The current response can further be improved by the insertion of another resistor R_{11}. Insertion of this resistor will remove the charging spike at the cross-over points, and further enhance the quality of the input current.

The valley-fill rectifier with voltage doubler and resistance R_{11} is shown in Fig.2.10, together with simulated waveforms. The circuit reduces the harmonic content of the line current but the output voltage has a large variation and the load of the rectifier must be able to tolerate it.

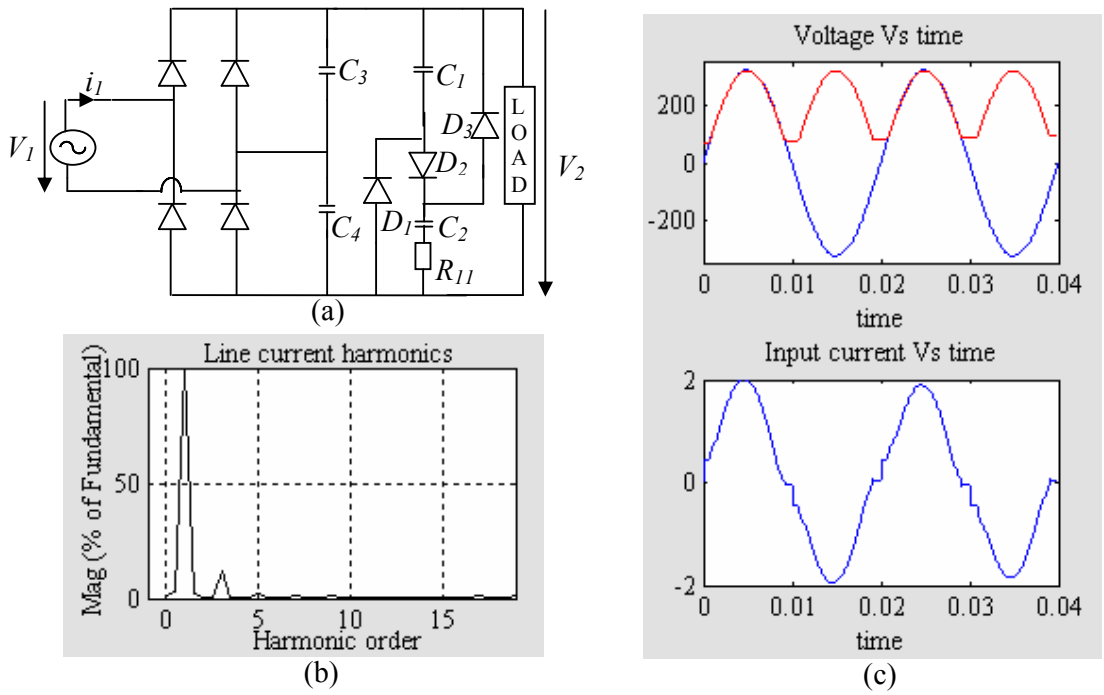


Fig.2.10 Valley-fill rectifier with voltage doubler and resistance R_{11}. (a) Schematic; (b) Line current harmonics; (c) Line voltage, output voltage (upper plot) and line current (lower plot) with V_1=230V_{rms} 50Hz, resistive load R=500Ω, and C_1=C_2=470μF and C_3=C_4=2μF and R_{11}=220Ω . The line current has K_p=0.9866, cosΦ=0.9857 and PF=0.9725. The output voltage ripple is ΔV_2=242V.

2.3 ADVANTAGES OF PASSIVE PFC:

Passive power factor correctors have certain advantages, such as

- Simplicity.
- Reliability.
- Ruggedness.
- Insensitive to noises and surges.
- No generation of high-frequency EMI.
- No high-frequency switching losses.

2.4 DISADVANTAGES OF PASSIVE PFC:

On the other hand, they also have several drawbacks

- Solutions based on filters are heavy and bulky, because line-frequency reactive components are used.
- They have poor dynamic response.
- Lack voltage regulation and the shape of their input current depend on the load. Even though line current harmonics are reduced, the fundamental component may show an excessive phase shift that reduces the power factor.

- Parallel-resonance at different frequencies occurs too, which can amplify other harmonics.

Summary:

Some of the techniques to implement "*Passive PFC*" have been presented in this chapter.

The passive PFC circuit uses low-frequency filter components to reduce harmonics. This approach typically meets EN standards for Class-A equipment up to 250W, at a much lower cost than a comparable switch mode power supply (SMPS) employing active PFC techniques. They typically yield less PF's compared to active topologies; they require a voltage doubler circuit for universal operation on most topologies above 150W.

Better characteristics can be obtained by using "*Active PFC*", which will be discussed in the next chapters.

CHAPTER 3

ACTIVE PFC

3 ACTIVE PFC:

An active PFC is a power electronic system that controls the amount of power drawn by a load in order to obtain a power factor as close as possible to unity. In most applications, the active PFC controls the input current of the load so that the current waveform is proportional to the mains voltage waveform (a sine wave). Active switches are used in conjunction with reactive elements in order to increase the effectiveness of the line current shaping and to obtain controllable output voltage.

The *switching frequency* further differentiates the active PFC solutions into two classes.

- *Low frequency active PFC:*

  Switching takes place at low-order harmonics of the line-frequency and it is synchronized with the line voltage.

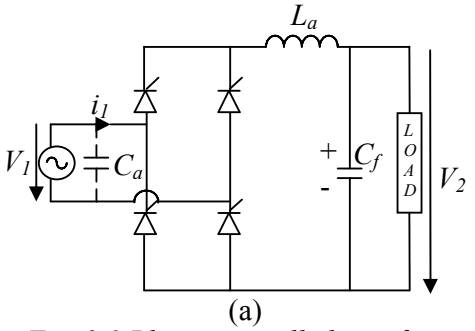
- *High frequency active PFC:*

  The switching frequency is much higher than the line frequency.

3.1 LOW-FREQUENCY ACTIVE PFC:

An active low frequency approach can be implemented up to about 1000 watts. Three representative solutions are presented in the next subchapters.

3.1.1. Phase controlled rectifier with DC-side inductor:

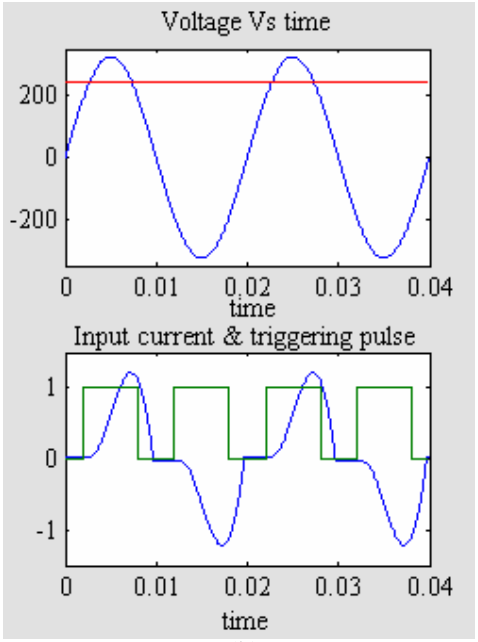


(a)

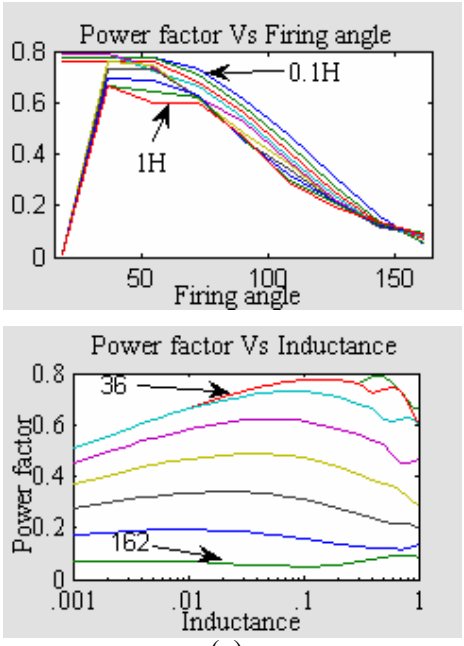
Fig. 3.1 Phase controlled rectifier. (a) Schematic;

The phase-controlled rectifier is shown in Fig. 3.1(a), and its control signals in Fig. 3.1(b). It is derived from the rectifier with a DC-side inductor from Fig. 2.3, where diodes are replaced with thyristors. In this solution, depending on the inductance L_a and the firing-angle α, near-unity purity factor K_p or displacement factor $cos\Phi$ can be obtained [11]. The variation of power factor w.r.t firing angle, for different values of inductance and vice versa are shown in Fig.3.1(c). However, the overall power factor *PF* is always less than 0.8. This implies a lagging displacement factor $cos\Phi$ is compensated for by an additional input capacitance C_a, even

though it increases line current harmonics. This approach is similar to that used for the diode bridge rectifier with a DC-side inductor, and discussed in the previous chapter.

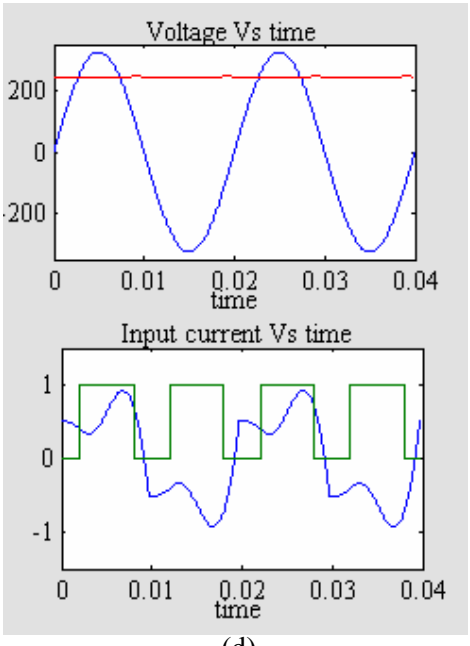


(b)

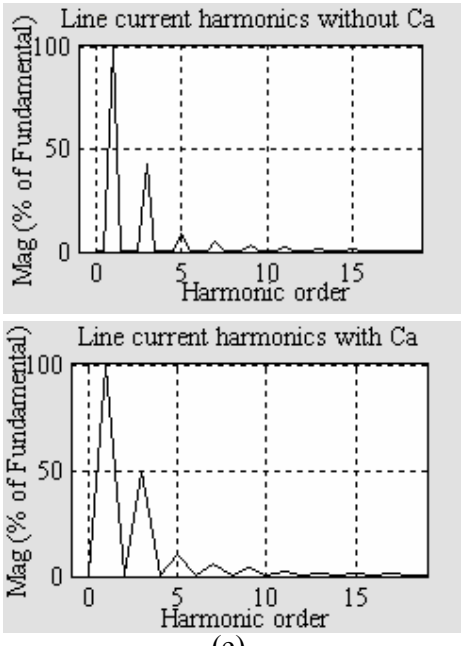


(c)

Fig. 3.1 (continued...) Phase controlled rectifier. (b) Line voltage and output voltage (upper plot) and line current (lower plot); with AC input voltage V_1=230V_{rms} 50Hz, resistive load R=500Ω inductance L_a=200mH, filter Capacitance C_f=470μF and firing angle = 36^0. Line current has Kp=0.9161, cosΦ=0.8490 and power factor=0.7778. (c) Power factor Vs firing angle for different values of inductance (upper plot) and vice versa.



(d)



(e)

Fig. 3.1 (continued...) Phase controlled rectifier. (d) Line voltage and output voltage (upper plot) and line current (lower plot); with additional capacitance C_a. Line current has K_p=0.8892, cosΦ=0.9978 and power factor=0.8873. (e) Line current harmonics without and with capacitance C_a.

This solution offers controllable output voltage, is simple, reliable, and uses low cost thyristors. On the negative side, the output voltage regulation is slow and a relatively large inductance L_a is still required.

The basic DC-DC converters can be used as active PFC. They are mainly used at high switching frequencies. However, it is also possible to use them at low switching frequencies as explained next. In this scheme the switch (SW) is bi-directional and is operated just twice per line period.

3.1.2 Low frequency switching buck converter:

The low-frequency switching Buck converter is shown in Fig. 3.2(a). Theoretically, the inductor current is constant for a near-infinite inductance L_d. The switch is turned on for the time duration T_{on} and the on-time intervals are symmetrical with respect to the zero-crossings of the line voltage, as illustrated in Fig. 3.2(c). In this solution the power factor depends on the firing instance and duty cycle of the active switch *S*. For a lower harmonic content of the line current, multiple switching per line-cycle can be used. However, the required inductance L_d is large and impractical.

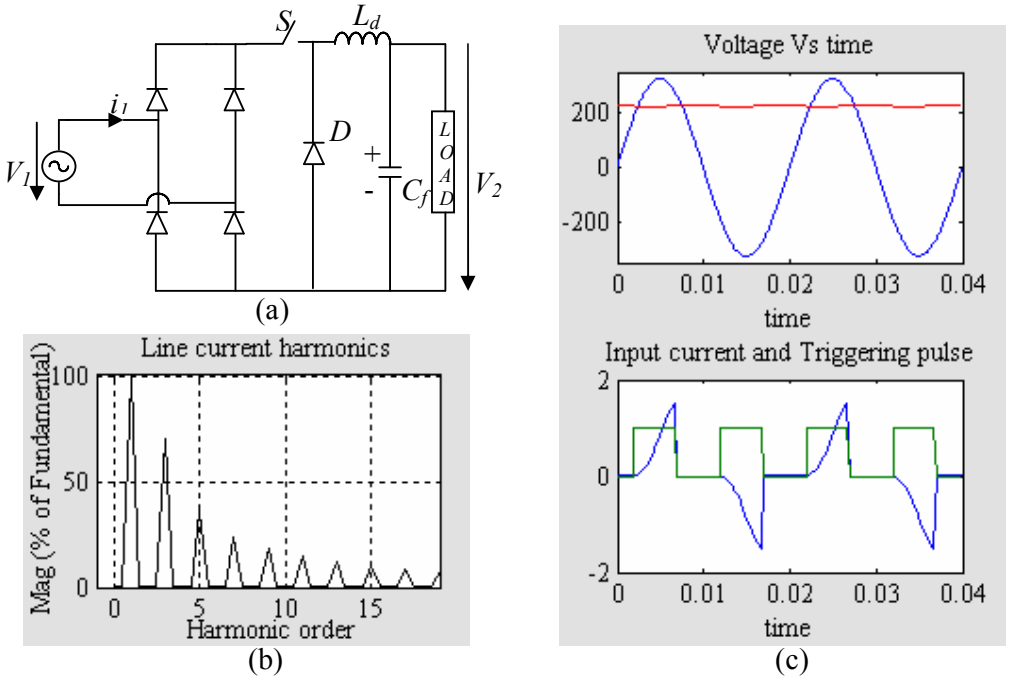
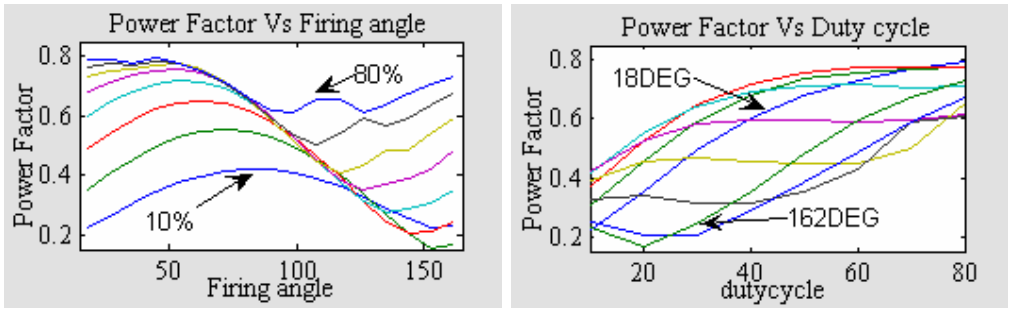


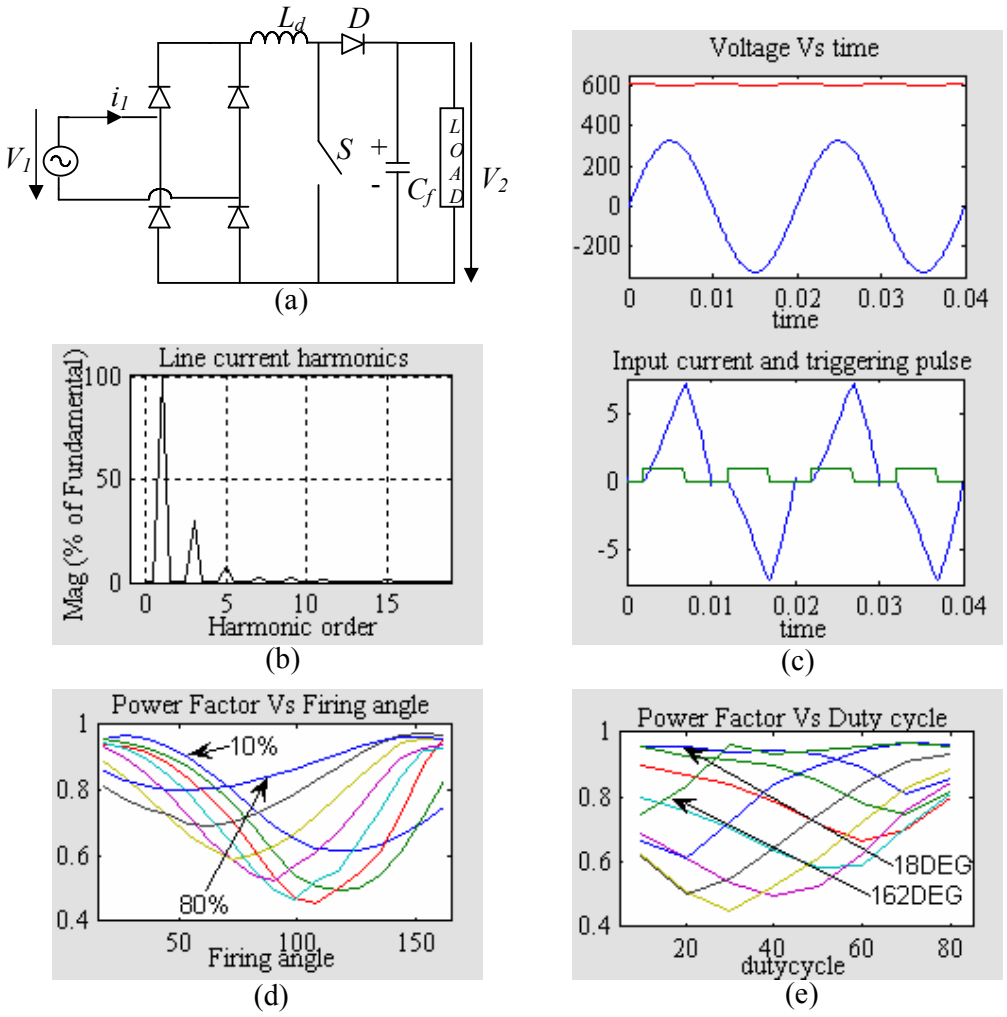
Fig. 3.2 Low-frequency switching buck converter. a) Schematic; b) Line current harmonics; c) Line voltage and output voltage (upper plot), line current and firing pulse (lower plot) for AC input voltage $V_{in}=230V_{rms}$ 50Hz, filter Capacitance $C_f=470\mu F$, resistive load $R=500\Omega$, Inductance $L_d=200mH$. Firing instance 2msec (i.e. 36^0) and duty cycle=50% and the line current has $K_p=0.7468$, $\cos\Phi=0.9870$ and power factor= 0.7371.



(d) (e)

Fig. 3.2(continued...) Low-frequency switching buck converter. (d) & (e) Power factor Vs firing angle for different values of duty cycles and vice versa respectively.

3.1.3. Low-frequency switching boost converter:



(a) (b) (c) (d) (e)

Fig.3.3 Low-frequency switching boost converter. (a) Schematic; (b) Line current harmonics; (c) Line voltage, output voltage (upper plot), line current and firing pulse (lower plot); for AC line voltage V_1=230V_{rms} 50Hz, resistive load R=500Ω, C_f=470μF, L_d=200mH and firing angle 36^0 and duty cycle=50%, the line current has K_p=0.9551, cosΦ=0.8896 and power factor=0.8497; (d) & (e) Power factor Vs firing angle for different values of duty cycles and vice versa respectively.

The low-frequency switching Boost converter is shown in Fig. 3.3. The active switch *S* is turned on for the duration T_{on}, so as to enlarge the conduction interval of the rectifier diodes. It is also possible to have multiple switching per half line-cycle, at low switching frequency, in order to improve the shape of the line current. Nevertheless, the line current has a considerable ripple.

3.1.4 Low frequency switching buck-boost converter:

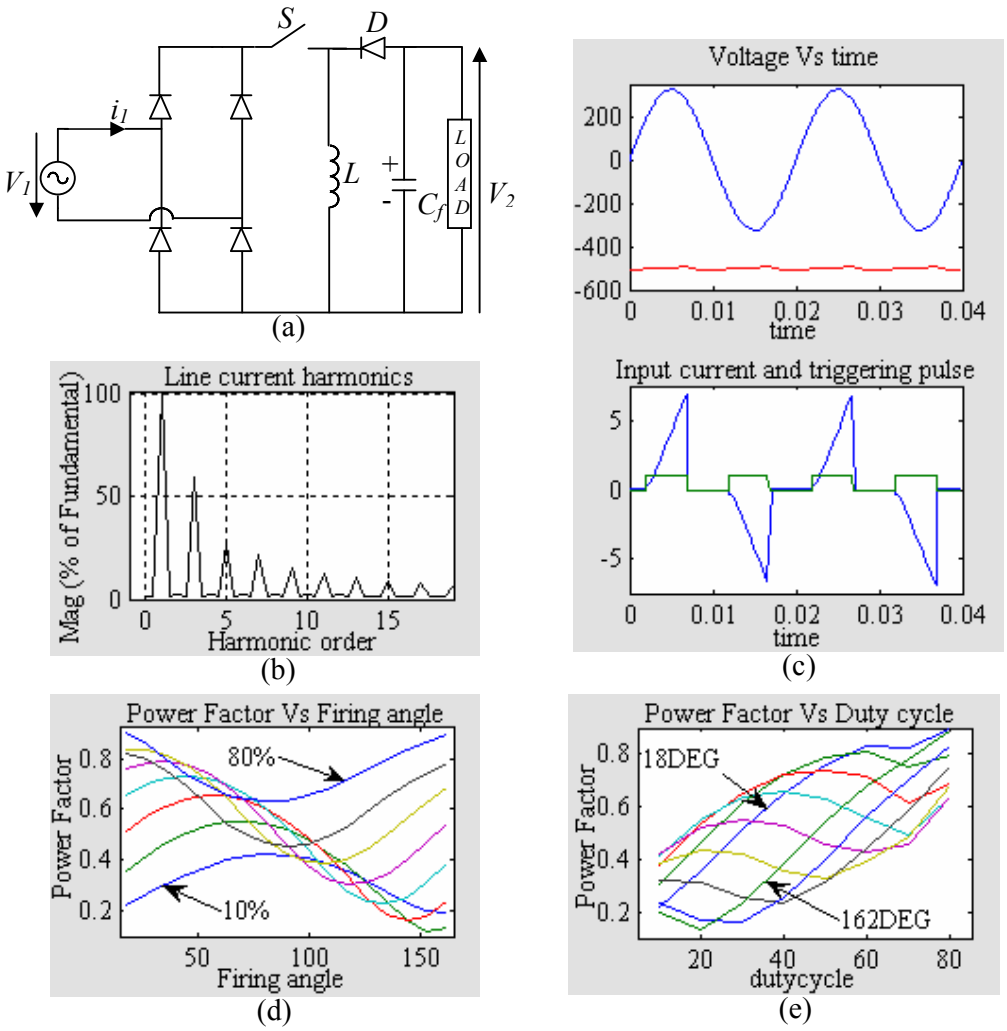


Fig.3.4 Low-frequency switching buck-boost converter. (a) Schematic; (b) Line current harmonics; (c) Line voltage, output voltage (upper plot), line current and firing pulse (lower plot); for AC line voltage V_1=230V_{rms} 50Hz, resistive load R=500Ω, C_f=470μF, L_d=200mH and firing angle 36^0 and duty cycle=50%, the line current has K_p= 0.7938, cosΦ= 0.9924 and power factor= 0.7878; (d) & (e) Power factor Vs firing angle for different values of duty cycles and vice versa respectively.

The low-frequency switching Buck-Boost converter is shown in Fig. 3.4. The active switch *S* is turned on for the duration T_{on}, so as to enlarge the conduction interval of the rectifier diodes. It is also possible to have multiple switching per half line-cycle, at low switching frequency, in order to improve the shape of the line current. Nevertheless, the line current has a considerable ripple.

Low-frequency switching PFC offers the possibility to control the output voltage in certain limits. In such circuits, switching losses and high-frequency EMI are negligible. However, the reactive elements are large and the regulation of the output voltage is slow.

3.2 HIGH-FREQUENCY ACTIVE PFC:

Active high frequency power factor correction makes the load behave like a resistor leading to near unity load power factor and the load generating negligible harmonics. The input current is similar to the input voltage waveform's wave shape.

The PFC stage can be realized by using a diode bridge and a DC/DC converter with a switching frequency much higher than the line-frequency. In principle, any DC/DC converter can be used for this purpose, if a suitable control method is used to shape its input current or if it has inherent PFC properties. Regardless of the particular converter topology that is used, the output voltage carries a ripple on twice the line-frequency. This is because, on the one hand, in a single-phase system the available instantaneous power varies from zero to a maximum, due to the sinusoidal variation of the line voltage. On the other hand, the load power is assumed to be constant. The output capacitor of the PFC stage buffers the difference between the instantaneous available and consumed power, hence the low-frequency ripple. In this thesis, the application of only "*second-order switching converter*" for PFC will be presented.

3.2.1 Second-order switching converters applied to PFC:

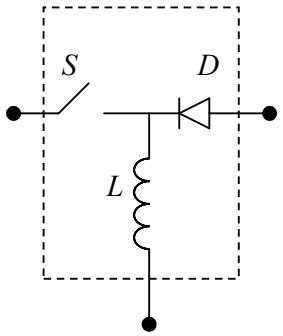


Fig. 3.5 First-order switching cell, from which second-order switching converters are generated.

The first-order switching cell is shown in Fig.3.5. The active switch *S* is controlled by an external control input. In a practical realization, this switch would be implemented, for example, by a MOSFET or an IGBT. The state of the second switch, which is diode *D*,

is indirectly controlled by the state of the active switch and other circuit conditions. The switching cell also contains a storage element, which is the inductor L.

The basic Buck, Boost and Buck-Boost converters are generated from this switching cell. Considering also the output filtering capacitor, they are second-order circuits. The output filtering capacitor can be assimilated to a voltage source. Hence, the ports of the switching cell are connected to voltage sources, a fact which explains why the storage element of the switching cell is an inductor and not a capacitor.

First let us describe three characteristics that are important for a PFC application, which are dependent mainly on the specific topology. In a PFC application, the input voltage is the rectified line voltage

$$v_1(t) = V_1 \left| \sin(\omega_L t) \right|$$

and the output voltage V_2 is assumed to be constant.

The first characteristic, which is determined by the conversion ratio of the converter, is the relation between the obtainable output voltage V_2 and the amplitude V_1 of the sinusoidal input voltage.

The second characteristic refers to the shape of the filtered (line-frequency) input current. If the converter is able to operate throughout the entire line-cycle, a sinusoidal line current can be obtained. Otherwise the line current is distorted, being zero in a region around the zero-crossings of the line voltage where the converter cannot operate.

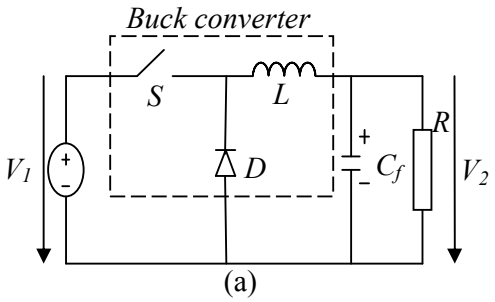
The third characteristic is related to the high-frequency content of the input current. We consider that the input current is continuous if it is not interrupted by a switching action. This means that if the inductor is placed in series at the input, then only the inductor current ripple determines the high-frequency content of the input current. Conversely, the input current is discontinuous if it is periodically interrupted by the switching action of a switch placed in series at the input. In such a case, the high-frequency content of the input current is large.

Now second-order converters will be briefly characterized in the light of these topology-specific characteristics without any feedback controller.

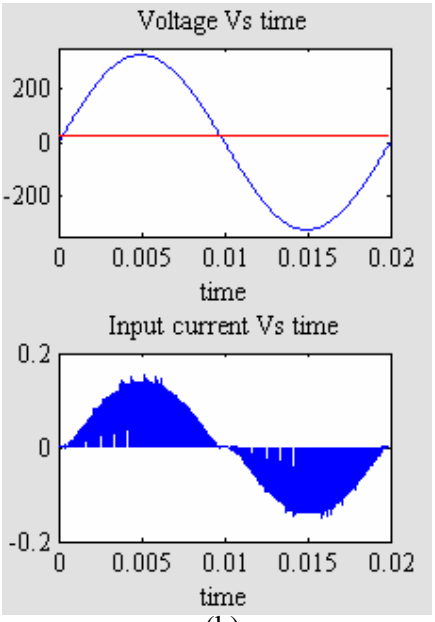
3.2.1.1 Buck converter:

The Buck converter, shown in Fig. 3.6, together with the simulation results has step-down conversion ratio. Therefore, it is possible to obtain an output voltage V_2 lower than the

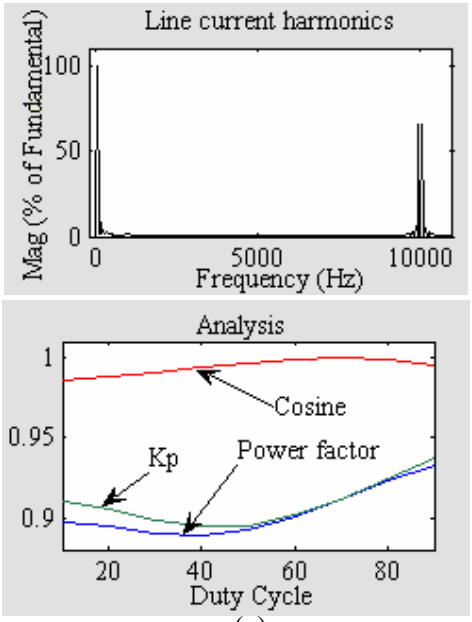
amplitude V_1 of the input voltage. However, the converter can operate only when the instantaneous input voltage v_1 is higher than the output voltage V_2, i.e. only during the interval $\omega_L t \in (\alpha, \pi - \alpha)$, where $\alpha = \sin^{-1}(V_2/V_1)$ Hence, the line current of a power factor corrector based on a Buck converter has crossover distortions. Moreover, the input current of the converter is discontinuous.



(a)



(b)



(c)

Fig.3.6 High-frequency switching buck converter. (a) Schematic; (b) Line voltage, output voltage (upper plot), Line current (lower plot); for AC input voltage $V_{in}=230V_{rms}$, inductance $L_d=200mH$, filter Capacitance $C_f=470\mu F$, resistive load $R=500\Omega$, and triggering pulse: switching frequency $f_s=10$ kHz, Duty cycle=90%. And line current has $K_p=0.9591$, $\cos\Phi=0.9975$ and PF=0.9367. (c) Line current harmonics (upper plot) and Variation of different parameters as a function of duty cycle of active switch (lower plot).

3.2.1.2 Boost converter:

The Boost converter is shown in Fig. 3.6. It has a step-up conversion ratio; hence the output voltage V_2 is always higher than the amplitude V_1 of the input voltage. Operation is possible throughout the line-cycle so the input current does not have

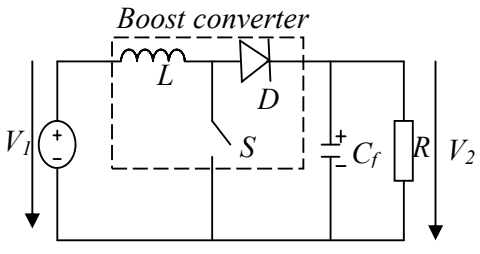
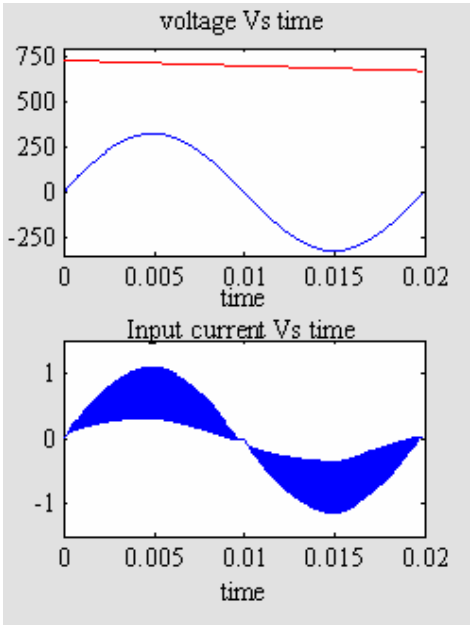
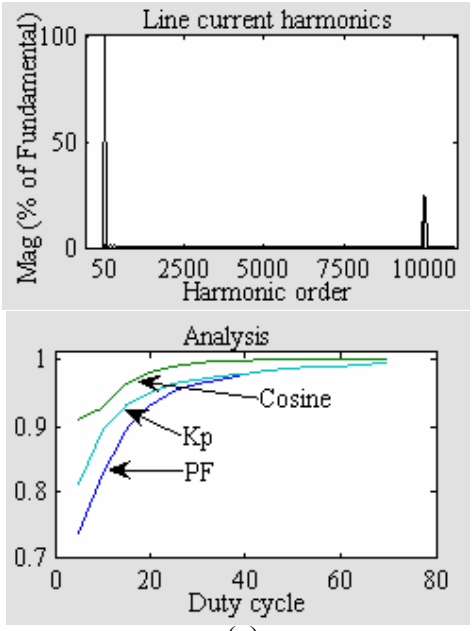


Fig. 3.7 High-frequency switching boost converter. (a) Schematic;

crossover distortions. As illustrated in Fig. 3.7(b), the input current is continuous, because the inductor is placed in series at the input. Hence, an input current with reduced high-frequency content can be obtained when operating in continuous conduction mode. For these reasons, the Boost converter is widely used for PFC.



(b)



(c)

Fig. 3.7 (continued...) High-frequency switching boost converter. (b) Line voltage, output voltage (upper plot) and Line current (lower plot); for AC input voltage V_{in}=230Vrms, inductance L_d=20mH, filter capacitance C_f=470μF, resistive load R=500Ω and triggering pulse: switching frequency f_s=10kHz and duty cycle=50%. Line current has Kp= 0.9857, cosΦ=0.9999 and PF=0.9856. (c) Line current harmonics (upper plot) and variation of different parameters as a function of duty cycle of active switch (lower plot).

3.2.1.3 Buck-boost converter:

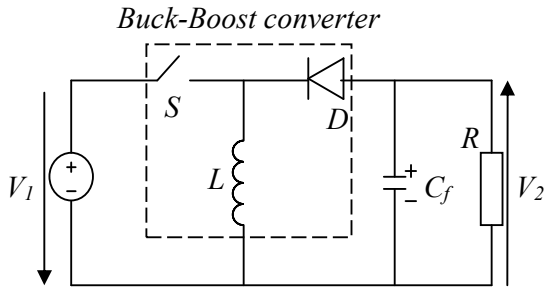
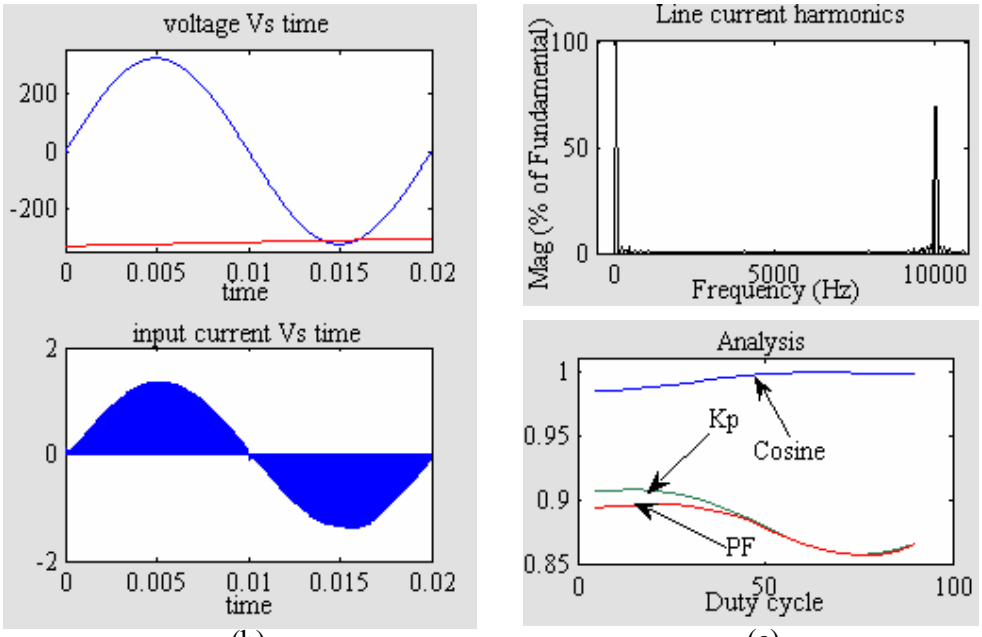


Fig. 3.8 High-frequency switching buck-boost converter. (a) Schematic.

The Buck-Boost converter, shown in Fig.3.8, can operate either as a step-down or a step-up converter. This means that the output voltage V_2 can be higher or lower than the amplitude V_1 of the input voltage, which gives freedom in specifying the output voltage. Operation is possible throughout the line-cycle and a sinusoidal line current can be obtained. However, the output voltage is inverted, which translates into higher voltage stress for the switch. Moreover, similar to the

buck converter, the input current is discontinuous with significant high-frequency content, as illustrated in Fig. 3.8.



(b) (c)

Fig. 3.8 (continued…) High-frequency switching buck-boost converter. (b) Line voltage, output voltage (upper plot) and line current (lower plot); for AC input voltage $V_{in}=230V_{rms}$, inductance L=200mH, filter capacitance $C_f=470\mu F$, resistive load $R=500\Omega$ and Triggering pulse: switching frequency $f_s=10kHz$, duty cycle =50%.Line current has Kp=0.88, cosΦ=0.9989 and PF= 0.8790. (c) Line current harmonics (upper plot) and variation of different parameters as a function of duty cycle of active switch (lower plot).

The topology-specific characteristics are summarized in Table 3.1.

Table 3.1. Topology-specific characteristics.

	Conversion characteristic	Crossover distortion	Input current
Buck converter	Step-down $V_2<V_1$	Yes, because operation is possible only for $\omega_L t \in (\alpha, \pi-\alpha)$ where $\alpha=sin^{-1}(V_2/V_1)$	Discontinuous
Boost converter	Step-up, $V_2>V_1$	No	Continuous
Buck-boost	Step-down/up	No	Discontinuous

The converters can operate in Continuous Inductor Current Mode – CICM, where the inductor current never reaches zero during one switching cycle, or Discontinuous Inductor Current Mode - DICM, where the inductor current is zero during intervals of the switching cycle, which will be discussed in the next chapters.

Summary:

The preferable type of PFC is Active Power Factor Correction (Active PFC) since it provides more efficient power frequency. Because Active PFC uses a circuit to correct power factor, Active PFC is able to generate a theoretical power factor of over 95%. Active Power Factor Correction also markedly diminishes total harmonics, automatically corrects for AC input voltage, and is capable of a full range of input voltage. Since Active PFC is the more complex method of Power Factor Correction, it is more expensive to produce an Active PFC power supply.

Some of the techniques to implement "*Low-frequency switching active PFC*" have been presented in this chapter. An active low frequency approach can be implemented up to about 1000 watts. Power factors as high as 0.95 can be achieved with an active low frequency design. To conclude, low-frequency switching PFC offers the possibility to control the output voltage in certain limits. In such circuits, switching losses and high-frequency EMI are negligible. However, the reactive elements are large and the regulation of the output voltage is slow.

Nearly unity power factor can be obtained by "*high-frequency switching active PFC*", if a suitable control method is used to shape its input current or if it has inherent PFC properties. The converters can operate in Continuous Inductor Current Mode – CICM, where the inductor current never reaches zero during one switching cycle, or Discontinuous Inductor Current Mode - DICM, where the inductor current is zero during intervals of the switching cycle, which will be discussed in the next chapters.

CHAPTER 4

OPERATION IN DISCONTINUOUS INDUCTOR CURRENT MODE – DICM

Average input resistance

Input voltage-current characteristics of basic converter topologies

Design procedure

Simulation results

Summary

4. OPERATION IN DISCONTINUOUS INDUCTOR CURRENT MODE – DICM

Basic types of dc-dc converters, when operating in discontinuous inductor current mode, have self power factor correction (PFC) property, that is, if these converters are connected to the rectified ac line, they have the capability to give higher power factor by the nature of their topologies. Input current feedback is unnecessary when these converters are employed to improve power factor. In this chapter, basic types of dc-dc converter topologies are studied to investigate their self-PFC capabilities [12].

In DICM, the input inductor is no longer a state variable since its state in a given switching cycle is independent on the value in the previous switching cycle. The peak of the inductor current is sampling the line voltage automatically. This property of DICM input circuit can be called "self power factor correction" because no control loop is required from its input side. This is also the main advantage over a CICM power factor correction circuit, in which multi-loop control strategy is essential. However, the input inductor operating in DICM can not hold the excessive input energy because it must release all its stored energy before the end of each switching cycle. As a result, a bulky capacitor is used to balance the instantaneous power between the input and output. In addition, if discontinuous inductor current mode is applied, the input current is normally a train of triangle pulse with nearly constant duty ratio. In this case, an input filter is necessary for smoothing the pulsating input current into a continuous one. Obviously, to ensure high power factor, the average current of the pulsating current should follow the input voltage in both shape and phase.

In this operating mode, for second-order converters shown in Fig.4.1, the inductor current i_L varies from zero to a maximum and returns back to zero before the beginning of the next switching cycle, as presented in Fig. 4.1.

4.1 AVERAGE INPUT RESISTANCE:

In order to examine the self-PFC capabilities of the basic converters, the term 'input resistance' r_I can be used, which is referred as average input resistance calculated as the ratio of the average input voltage and the average input current, over one switching cycle T_s . The input voltage v_1 can be considered to be constant during one switching period T_s, because the switching frequency is much higher than the line-frequency. Hence, as depicted in Fig. 4.1, the input resistance of the analyzed converters can be defined as:

$$r_1(t) = \frac{v_1(t)}{\langle i_1(t) \rangle_{T_S}} \quad \text{.....(4.1)}$$

Where $\langle i_1(t)\rangle_{T_s}$ is the average of the input current i_1 over one switching period T_s [16, 370-381]. Based on the operating principle of the converters and on the waveforms shown in Fig. 4.1, as well as assuming a rectified-sinusoid input voltage v_1 , it is straightforward to calculate the expressions $r_1(t)$ of the input resistance that are presented in Table 4.1.

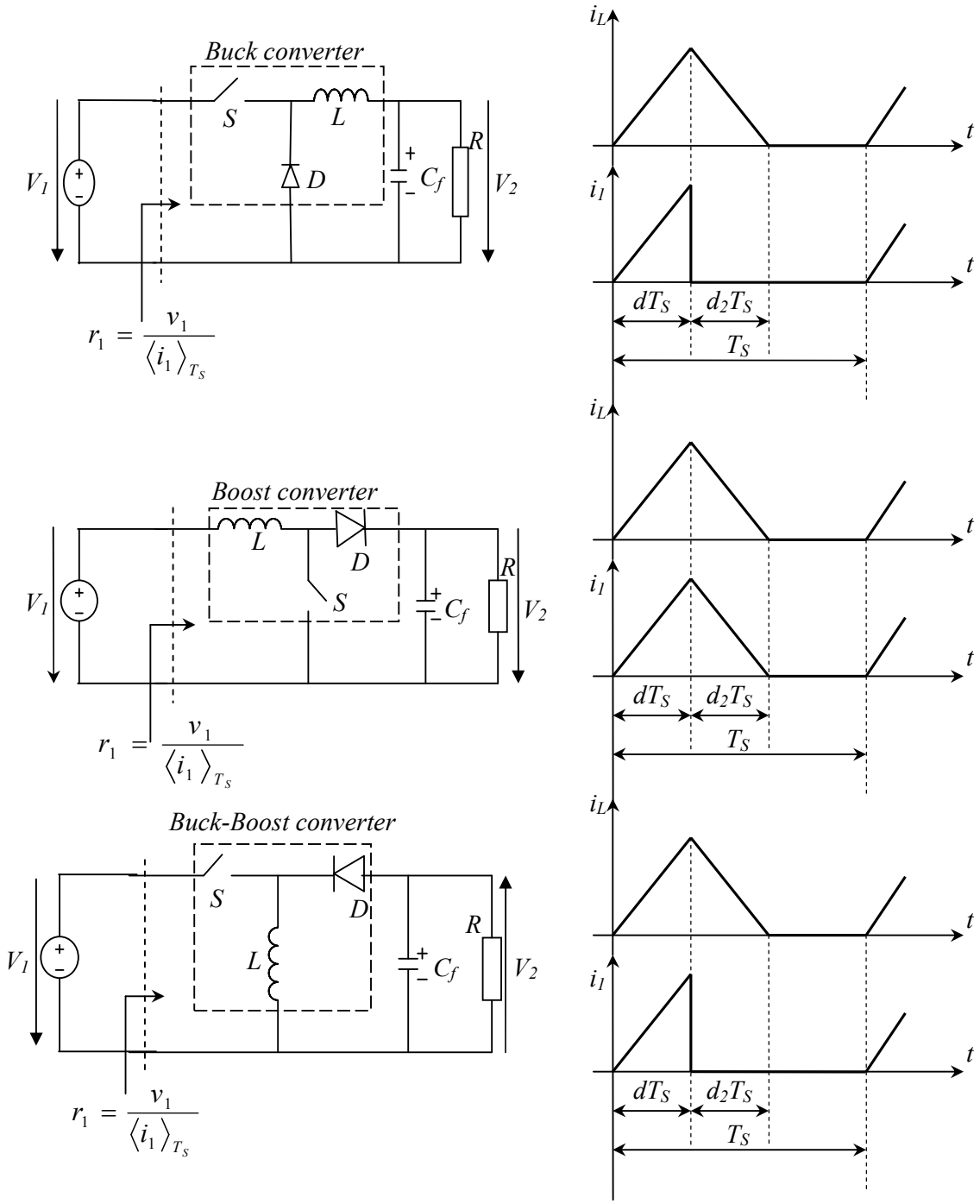


Fig.4.1 Second-order switching converters: a) Definition of the input resistance $r_1(t)$; b) The inductor current $i_L(t)$ and the input current $i_1(t)$, when operating in DICM.

Table 4.1 Inherent PFC properties of second-order switching converters operating in DICM.

Converter	Input resistance $r_1(t)$	Inherent PFC
Buck	$r_1(t)=\frac{2L}{d^2T_S}\left[\frac{1}{1-\frac{V_2}{V_1\sin\omega_L t}}\right], \omega_L t\in(\alpha,\pi-\alpha), \alpha=\arcsin\frac{V_2}{V_1}$	Poor, Improves when V_2/V_1 is decreased
Boost	$r_1(t)=\frac{2L}{d^2T_S}\left[1-\frac{V_1\sin\omega_L t}{V_2}\right], \omega_L t\in(0,\pi)$	Fair , Improves when V_2/V_1 is increased
Buck-boost	$r_1(t)=\frac{2L}{d^2T_S}, \omega_L t\in(0,\pi)$	Excellent.

4.2 INPUT VOLTAGE-CURRENT CHARACTERISTICS OF BASIC CONVERTER TOPOLOGIES:

In order to examine the self-PFC capabilities of the basic converters, we first investigate their input characteristics. Because the input currents of these converters are discrete when they are operating in DICM, only averaged input currents are considered. Since switching frequency is much higher than the line frequency, let's assume the line voltage is constant in a switching cycle. In steady state operation, the output voltage is nearly constant and the variation in duty ratio is slight. Therefore, constant duty ratio is considered in deriving the input characteristics.

4.2.1 Buck converter:

The basic buck converter topology and its input current waveform when operating in DICM are shown in Fig. 4.2(a) and (b), respectively. It can be shown that the average input current in one switching cycle is given by

$$i_{1,avg}(t)=\frac{1}{T_S}\left[\frac{1}{2}DT_S\frac{v_1(t)-V_o}{L}DT_S\right] =\frac{D^2T_S}{2L}v_1(t)-\frac{D^2T_S}{2L}V_o \quad \text{.....(4.2)}$$

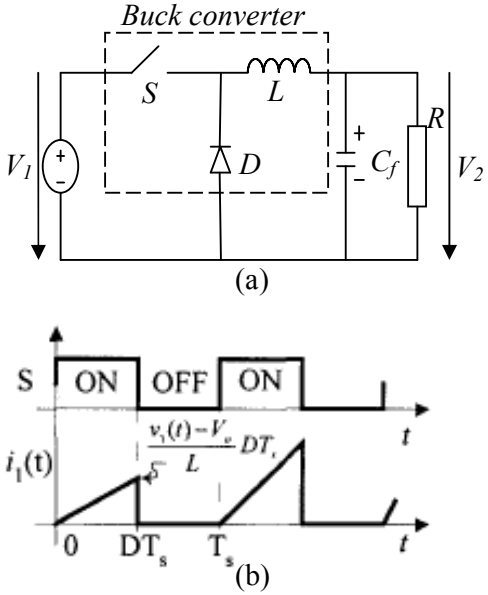


Fig. 4.2 buck converter (a) Schematic; (b) Input current

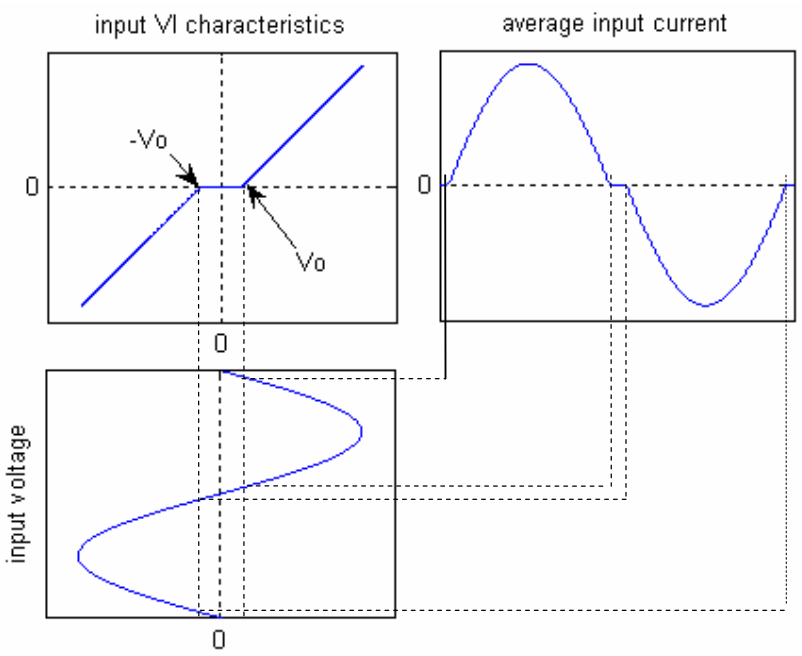


Fig.4.2 (continued…) (c) Input VI Characteristic of basic buck converter operating in DICM.

Figure 4.2(c) shows that the input voltage-input current V-I characteristics is a straight line. It should be note that this straight line does not go through the origin. When the rectified line voltage $v_1(t)$ is less than the output voltage V_o, negative input current would occur. This is not allowed because the bridge rectifier will block the negative current. As a result, the input current is zero near the zero cross point of the line voltage, as shown in Fig.4.2(c). Actually, the input current is distorted simply because the buck converter can work only under the condition that the input voltage is larger than the output voltage.

As can be seen in Table 4.1, the input resistance of the Buck converter is not constant throughout the line-cycle. However, its variation decreases and "*inherent*" PFC property improves, when the ratio V_2/V_1 is decreased. As explained previously, the line current has crossover distortions too, which are however less disturbing when the ratio V_2/V_1 is decreased. However, compliance with standard IEC 1000-3-2 can be obtained up to a relatively high power, when the output voltage V_2 is low enough when compared to the amplitude V_1 of the sinusoidal input voltage

Therefore the basic buck converter is not a good candidate for DICM input power factor correction.

4.2.2 Boost converter:

The basic boost converter and its input current waveform are shown in Fig. 4.3(a) and (b) respectively. The input V-I characteristic can be found as follows:

$$i_{1,avg}(t) = \frac{1}{T_S}\left[\frac{1}{2}(D + D_1)T_S \frac{v_1(t)}{L} DT_S\right] \qquad \text{.....(4.3)}$$
$$= \frac{D^2 T_S}{2L} \frac{v_1(t) V_o}{V_o - v_1(t)}$$

By plotting Eq. (4.3), we obtain the input V-I characteristic curve as given in Fig. 4.3(c). As we can see that as long as the output voltage is larger than the peak value of the line voltage in certain extent (depending on D_1), the relationship between $v_1(t)$ and $i_{1,avg}(t)$ is nearly linear. When the boost converter connected to the line, it will draw almost sinusoidal average input current from the line, shown as in Fig. 4.3(c).

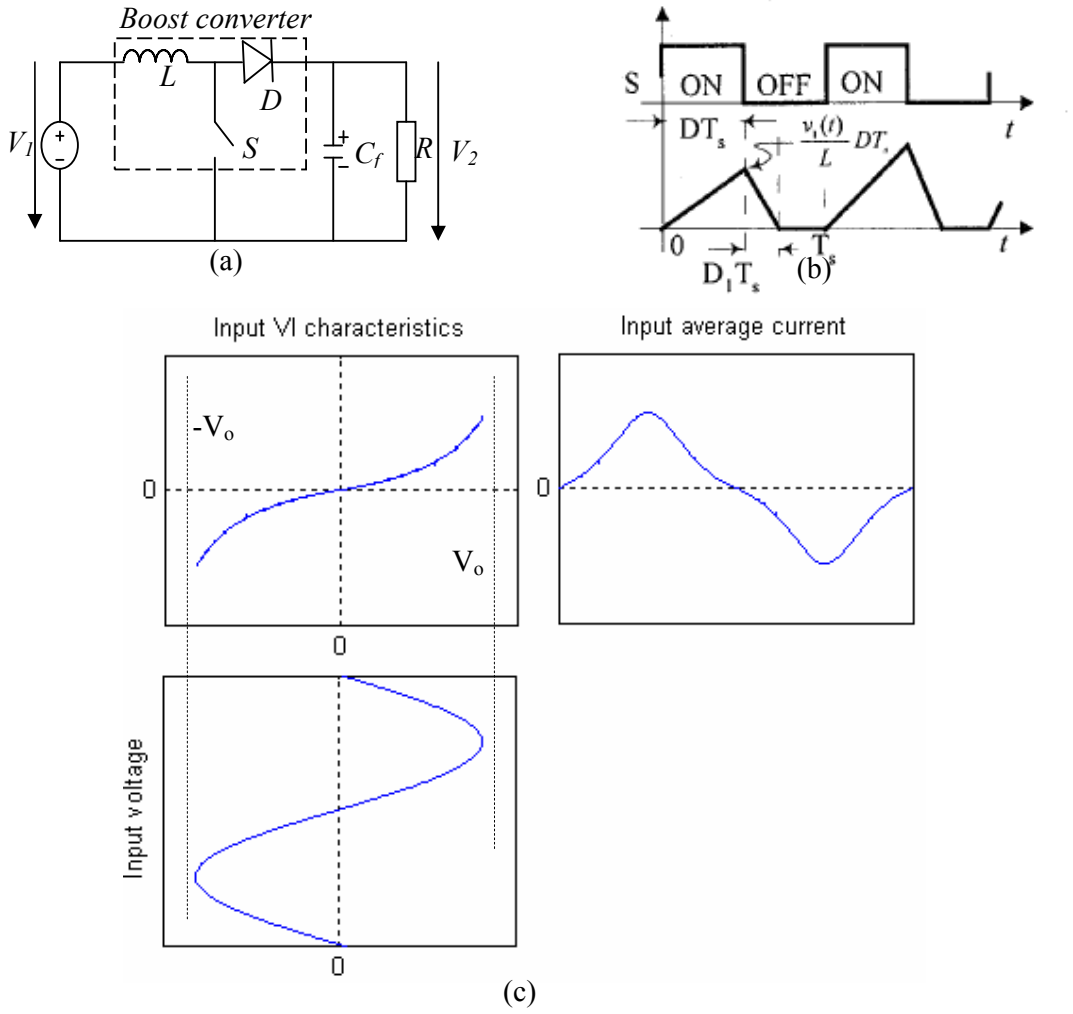


Fig. 4.3 Boost converter. (a) Schematic; (b) Input current; (c) Input V-I Characteristic of basic boost converter operating in DICM

As one might notice from Eq. (4.3) that the main reason to cause the non-linearity is the existence of D_1. Ideally, if $D_1 = 0$, the input V-I characteristic will be a linear one. In practice, to reduce the discharge period D_1, by properly configuring the circuit topology, a higher voltage, instead of V_o, can be created to be applied to the inductor during D_1 to discharge the inductor.

The Boost converter has an imperfect "*inherent*" PFC property, as well. Its input resistance changes throughout the line-cycle, but the variation decreases and inherent PFC property improves when the ratio V_2/V_1 is increased. Taking into account the fact that the line current does not have crossover distortions, compliance with the standard is achieved comfortably.

Because of the above reasons, boost converter is comparably superior to most of the other converters when applied to do PFC [13-15]. However, it should be noted that boost converter can operate properly only when the output voltage is higher than its input voltage. When low voltage output is needed, a step-down dc-dc converter must be cascaded.

4.2.3 Buck-boost converter:

Figure 4.4(a) shows a basic buck-boost converter. The averaged input current of this converter can be found according to its input current waveform, shown in Fig. 4.4(b).

$$i_{1,avg}(t) = \frac{D^2 T_S}{2L} v_1(t) \qquad \text{.....(4.4)}$$

Equation (4.4) gives a perfect linear relationship between $i_{1,avg}(t)$ and $v_1(t)$ which proves that a buck-boost has excellent self-PFC property. This is because the input current of buck-boost converter does not related to the discharging period D_1. Its input V-I characteristics and input voltage and current waveforms are shown in Fig. 4.4(c).

The input resistance of the Buck-Boost converter (presented in table 4.1) depends only on inductance L, switching period T_s and duty-cycle d. If operation in DICM is ensured throughout the line-cycle and if d is kept constant, then the input resistance r_1 is constant. As a consequence, the average input current $\langle i_1(t) \rangle_{T_S}$ tracks the shape of the input voltage and the converter has an "*inherent*" PFC property. In contrast to CICM operation, in DICM there is no need for the controller to adjust the duty-cycle over the line-cycle to perform PFC.

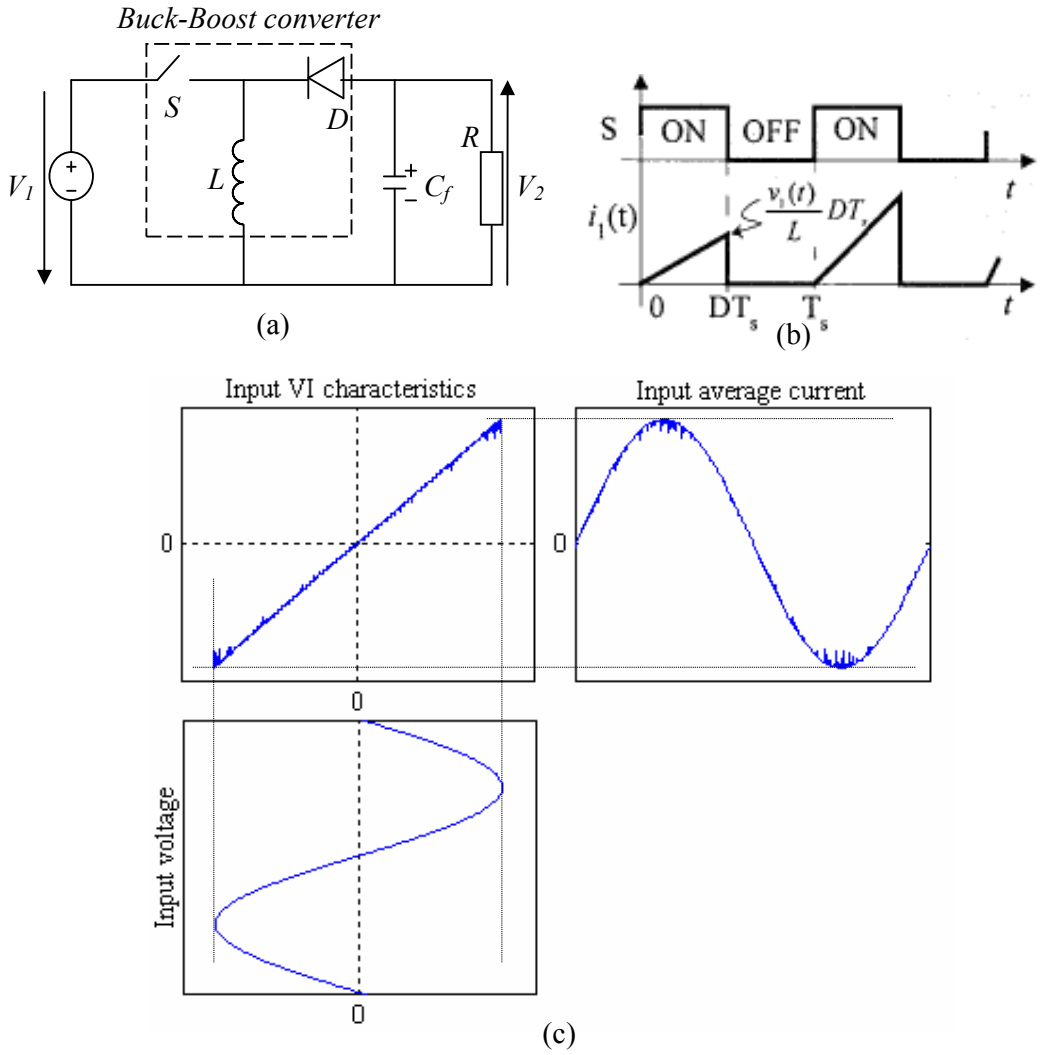


Fig. 4.4 Buck-boost converter. (a) Schematic; (b) Input current; (c) Input V-I Characteristic of basic boost converter operating in DICM

Furthermore, because the output voltage of buck-boost converter can be either larger or smaller than the input voltage, it demonstrates strong availability for DICM input technique to achieve power factor correction. So, theoretically buck-boost converter is a perfect candidate. Unfortunately, this topology has two limitations:

1) The polarity of its output voltage is reversed, i.e., the input voltage and the output voltage don't have a common ground; and

2) It needs floating drive for the power switch. The first limitation circumscribes this circuit into a very narrow scope of applications.

As a result, it is not widely used.

4.3 DESIGN PROCEDURE: [16, chapter5]

Continuous conduction mode

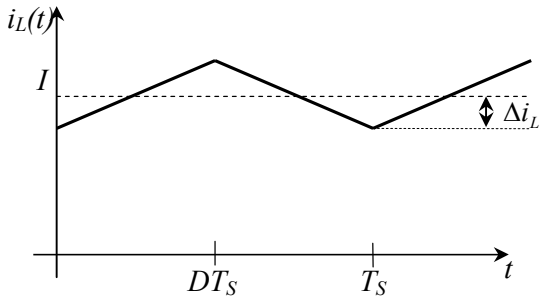


Fig. 4.5 Inductor current of the DC-DC converter.

4.3.1 Design procedure for buck converter:

Minimum diode current is ($I - \Delta i_L$)

DC component $I=V/R$

Current ripple is

$$\Delta i_L = \frac{\left(V_g - V\right)}{2L} DT_S = \frac{V_g DD' T_S}{2L}$$

From the above it can be noted that I depends on load but Δi_L doesn't.

$$I > \Delta i_L(t) \qquad \textit{for CICM}$$
$$I < \Delta i_L(t) \qquad \textit{for DICM}$$

Insert buck converter expressions for I and Δi_L:

$$\frac{DV_g}{R} < \frac{DD' T_S V_g}{2L}$$

$$\frac{2L}{RT_S} < D'$$

This expression is of the form

$$K < K_{crit}(D) \qquad \textit{for DICM}$$

Where $K = \frac{2L}{RT_S}$ *and* $K_{crit}(D) = D'$

Solve K_{crit} equation for load resistance R:

$$R < R_{crit}(D) \qquad \textit{for CICM}$$
$$R > R_{crit}(D) \qquad \textit{for DICM}$$

Where $R_{crit}(D) = \frac{2L}{D'T_S}$

4.3.2 Summary: Mode boundary

$$K > K_{crit}(D) \quad or \quad R < R_{crit}(D) \qquad for\ CICM$$
$$K < K_{crit}(D) \quad or \quad R > R_{crit}(D) \qquad for\ DICM$$

Table 4.2 *CICM-DICM mode boundaries for the buck, boost, and buck-boost converters.*

CONVERTER	$K_{crit}(D)$	$\max_{0 \le D \le 1}(K_{crit})$	$R_{crit}(D)$	$\max_{0 \le D \le 1}(R_{crit})$
Buck	$(1-D)$	1	$\frac{2L}{(1-D)T_S}$	$2\frac{L}{T_S}$
Boost	$D(1-D)^2$	4/27	$\frac{2L}{D(1-D)^2 T_S}$	$\frac{27}{2}\frac{L}{T_S}$
Buck-boost	$(1-D)^2$	1	$\frac{2L}{(1-D)^2 T_S}$	$2\frac{L}{T_S}$

The main advantage of using switching converters operating in DICM for PFC applications is the simplicity of the control method. Since there is no need to continuously adjust the duty-cycle *d* to perform PFC, only a voltage loop is needed to regulate the voltage across the storage capacitor. The bandwidth of the voltage loop has to be low (e.g. 10-15Hz), in order to filter out the output voltage ripple at twice the line-frequency. The simple control of converters with inherent PFC makes them attractive for low-cost applications.

But the main disadvantage of using switching converters operating in DICM for PFC application is the input current is normally a train of triangle pulse with nearly constant duty ratio. As a result the high-frequency EMI is very high. In this case, an input filter is necessary for smoothing the pulsating input current into a continuous one.

4.4 SIMULATION RESULTS:

4.4.1 Buck converter:

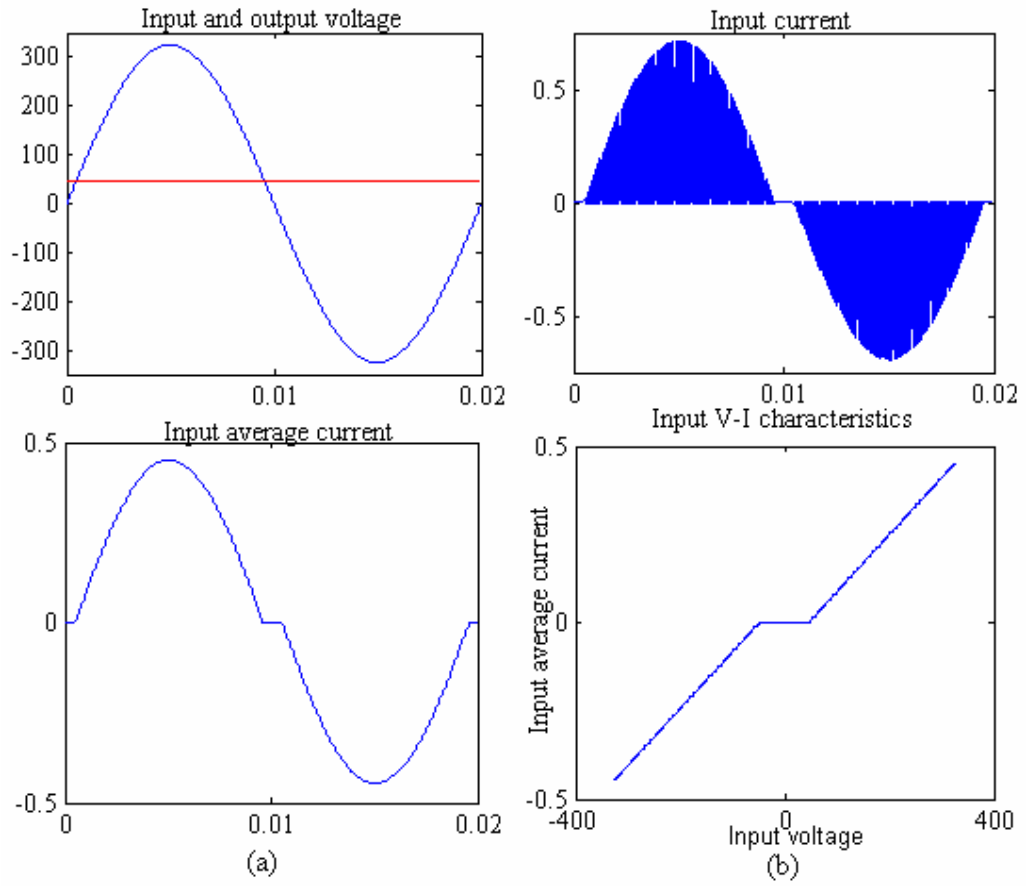


Fig. 4.6 Buck converter operating in DICM. (a) Input voltage and output voltage (upper plot) and Input average current (lower plot); (b) Input current (upper plot) and Input V-I characteristics (lower plot) of buck converter for AC input voltage $V_{in}=230V_{rms}$, inductance $L_d=20mH$, filter Capacitance $C_f=470\mu F$, resistive load $R=500\Omega$.

4.4.2 Boost converter:

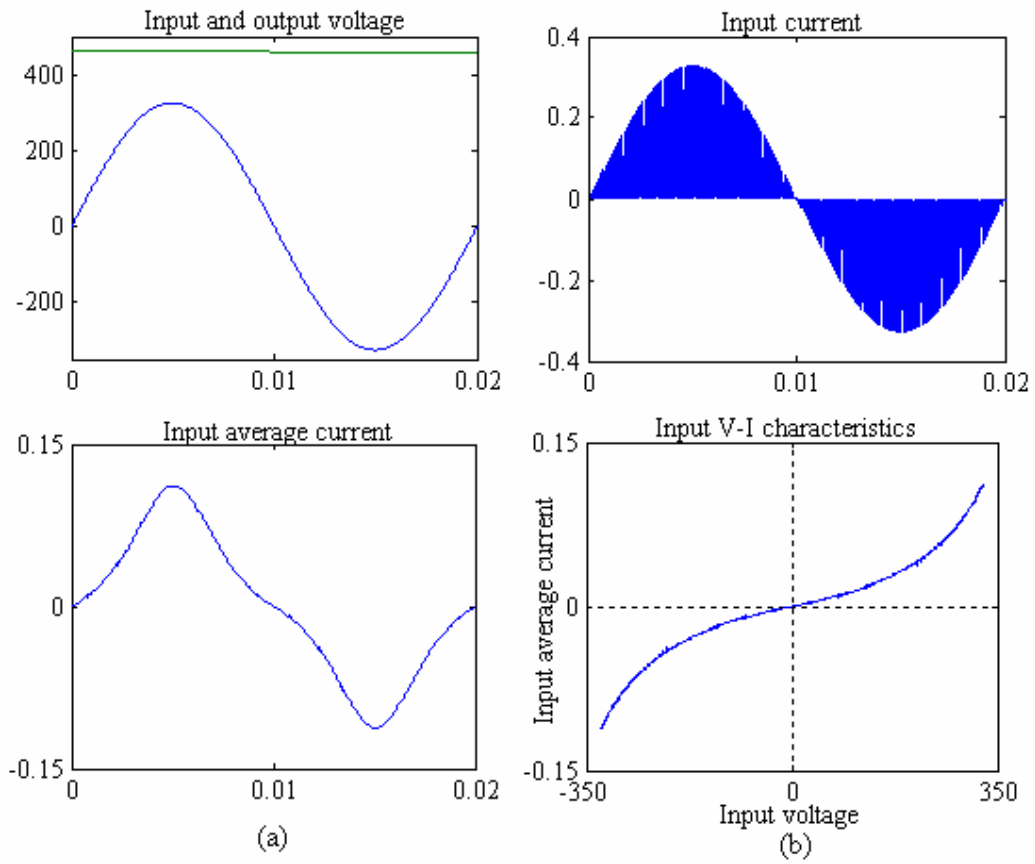


Fig. 4.7 Boost converter operating in DICM. (a) Input voltage and output voltage (upper plot) and Input average current (lower plot); (b) Input current (upper plot) and Input V-I characteristics (lower plot) of boost converter for AC input voltage $V_{in}=230V_{rms}$, inductance $L_d=20mH$, filter Capacitance $C_f=470\mu F$, resistive load $R=3500\Omega$.

4.4.3 Buck-boost converter:

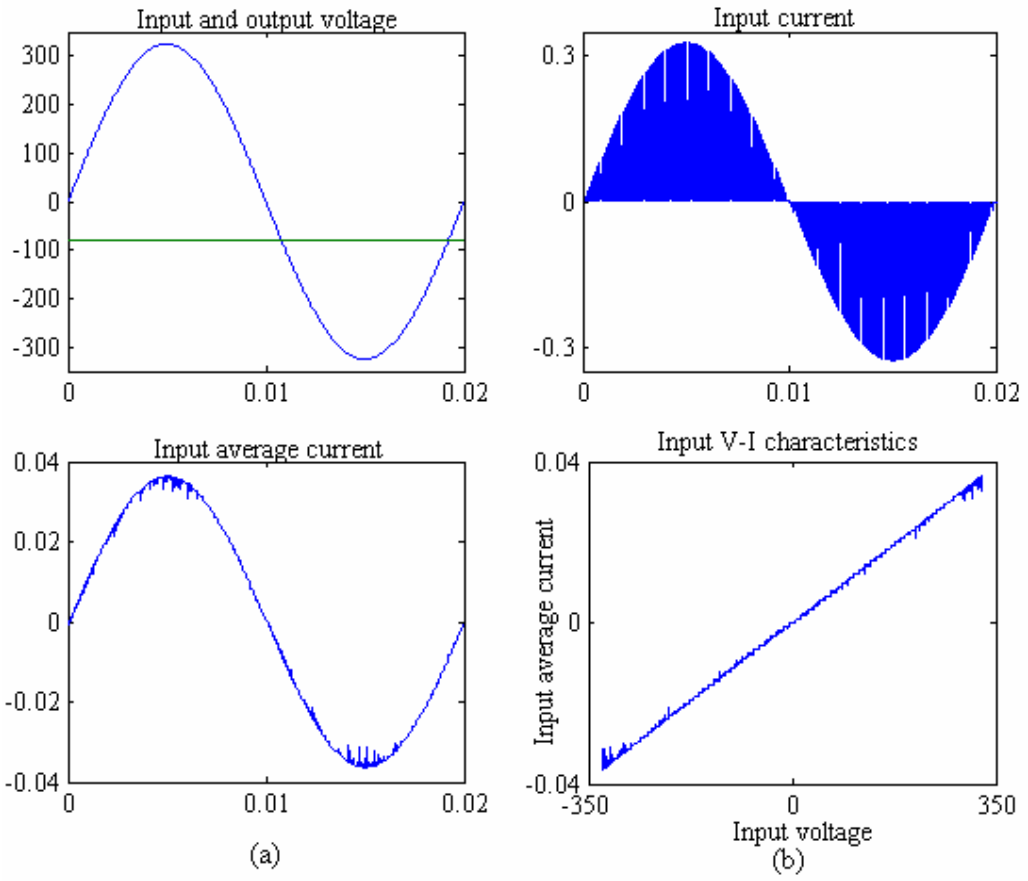


Fig.4.8 Buck-boost converter operating in DICM. (a) Input voltage and output voltage (upper plot) and Input average current (lower plot); (b) Input current (upper plot) and Input V-I characteristics (lower plot) of buck-boost converter for AC input voltage $V_{in}=230V_{rms}$, inductance $L_d=20mH$, filter Capacitance $C_f=470\mu F$, resistive load $R=1000\Omega$.

Summary:

According to the above discussion, we may conclude that the basic boost converter and buck-boost converter have excellent self-PFC capability naturally. Among them, boost converter is especially suitable for DICM PFC usage. Hence, this converter is the most preferable by the designers for power factor correction purpose. Other converters may be used only if their input V-I characteristics have been modified (linearized), or when they operate in continuous inductor conduction mode, which will be discussed in the next chapter.

In addition, if discontinuous inductor current mode is applied, the input current is normally a train of triangle pulse with nearly constant duty ratio. In this case, an input filter is necessary for smoothing the pulsating input current into a continuous one.

CHAPTER 5

OPERATION IN CONTINUOUS INDUCTOR CURRENT MODE – CICM

Control scheme for CICM operation

Peak current control

Average current mode control

Hysteresis control

Borderline control

Control IC's

Simulation results

Summary

5. OPERATION IN CONTINUOUS INDUCTOR CURRENT MODE – CICM:

5.1 CONTROL SCHEME FOR CICM OPERATION:

In this operating mode, the inductor current never reaches zero during one switching cycle and there is always energy stored in the inductor. The *volt-seconds* applied to the inductor must be balanced throughout the line-cycle by continuously changing the duty-cycle of the converter using an appropriate control method.

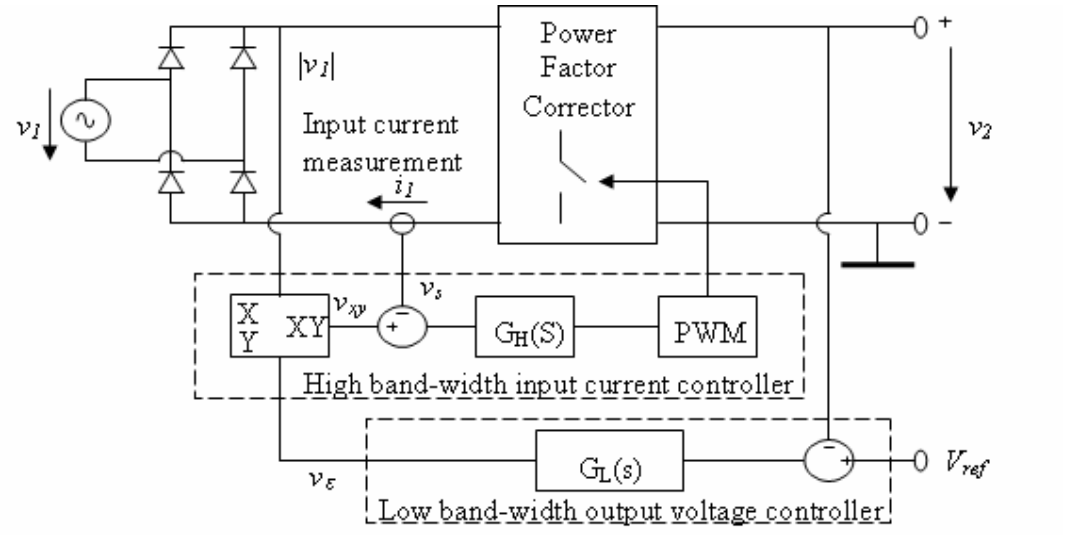


Fig. 5.1 Control scheme for PFC using a switching converter operating in CICM.

An example of a control scheme is shown in Fig. 5.1. The low-bandwidth outer loop with characteristic $G_L(s)$ is used to keep the output voltage of the PFC stage constant and to provide the error signal v_ε. The high-bandwidth inner loop with characteristic $G_H(s)$ is used to control the input current. A multiplier is used to provide a reference v_{xy}, which is proportional to the error signal v_ε and which has a modulating signal with the desired shape for the input current. Fig. 5.1 shows the most common situation, where the modulating signal is the rectified-sinusoid input voltage v_1. Depending on the topology of the PFC stage, it may be beneficial to use as a modulating signal the difference between the input voltage and the output voltage.

The control circuit can be simplified by eliminating the multiplier and the sensing of the line voltage. In this case the modulating signal is $v_{xy} = v_\varepsilon$, and it is essentially constant over the line cycle, because v_ε is the control signal from the low-bandwidth output voltage controller. Therefore, the input current is clamped to a value proportional with v_ε and its shape approaches a square waveform. The simplification of the control circuit leads to a more

distorted line current, but compliance with the standard can be obtained up to approximately 500W for a $230V_{rms}$ input voltage. Furthermore, if the edges of the line current waveform are softened, thus obtaining a nearly trapezoidal waveform, compliance up to several kW can be obtained.

There are several ways to implement the high-bandwidth inner loop [16, pp. 636-639] [5], [17]. Some of them are

1. Peak current control.
2. Average current control.
3. Hysteresis control.
4. Borderline control.

Even though these control techniques can be used for all DC-DC converters, only boost converter has been taken for the study because of the continuous input current.

5.2 PEAK CURRENT CONTROL:

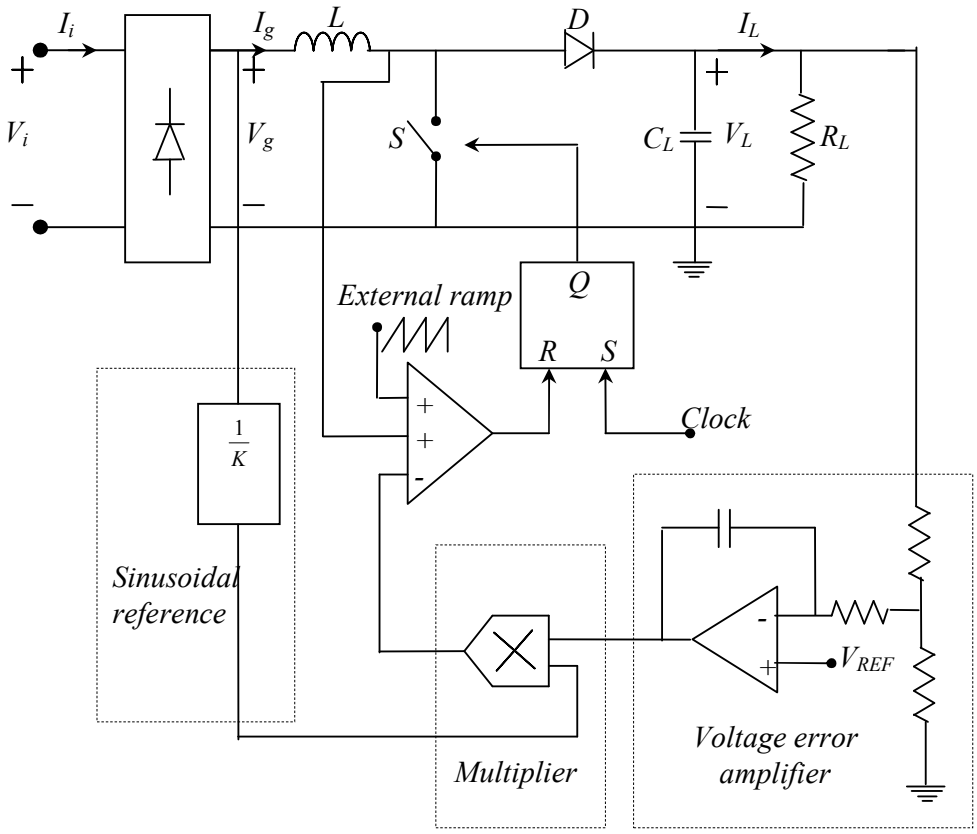
In peak current mode control, well-known from DC/DC converters, the active switch is turned on with constant switching frequency, and turned off when the upslope of the inductor current reaches a level set by the outer loop. This gives instant over-current switch protection, but also makes the control very sensitive to noise. Moreover, the control is inherently unstable at duty-cycles exceeding 0.5 [18]. A compensating ramp must be added to the inductor ramp to solve this problem.

The basic scheme of the peak current controller is shown in Fig. 5.2, together with a typical input current waveform.

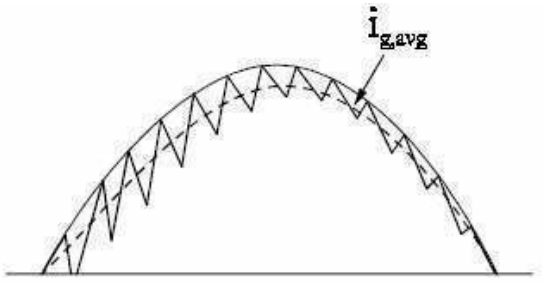
As we can see, the switch is turned on at constant frequency by a clock signal, and is turned off when the sum of the positive ramp of the inductor current (i.e. the switch current) and an external ramp (compensating ramp) reaches the sinusoidal current reference. This reference is usually obtained by multiplying a scaled replica of the rectified line voltage v_g times the output of the voltage error amplifier, which sets the current reference amplitude. In this way, the reference signal is naturally synchronized and always proportional to the line voltage, which is the condition to obtain unity power factor.

As Fig. 5.2 reveals, the converter operates in Continuous Inductor Current Mode (CICM); this means that devices current stress as well as input filter requirements are reduced. Moreover, with continuous input current, the diodes of the bridge can be slow

devices (they operate at line frequency). On the other hand, the hard turn-off of the freewheeling diode increases losses and switching noise, calling for a fast device.



(a)



(b)

Fig. 5.2 Peak current control scheme.

However, if the simplicity of the control circuit is of primary interest, rather than the quality of the line current waveform, then peak current mode control with input current clamping is attractive [19], [20].

The input current distortion can be reduced by changing the current reference wave shape, for example introducing a dc offset, and/or by introducing a soft clamp. These provisions are discussed in [21] and [18]. In [22] it is shown that even with constant current reference, good input current waveforms can be achieved. Moreover, if the PFC is not intended for universal input operation, the duty-cycle can be kept below 50% so avoiding also the compensation ramp.

5.2.1 Advantages:

1. Constant switching frequency.
2. Only the switch current must be sensed and this can be accomplished by a current transformer, thus avoiding the losses due to the sensing resistor.
3. No need of current error amplifier and its compensation network.
4. Possibility of a true switch current limiting.
5. As there is an instantaneous pulse-by-pulse current limit, the reliability is improved and the response speed is increased.

5.2.2 Disadvantages:

1. Presence of sub-harmonic oscillations at duty cycles greater than 50%, so a compensation ramp is needed.
2. Input current distortion which increases at high line voltages and light load and is worsened by the presence of the compensation ramp [21], [18].
3. Control more sensitive to commutation noises.

Available commercial IC's for the peak current control are the ML4812 (Micro Linear) and TK84812 (Toko).

5.2.3 Peak Current Mode Control Problems:

5.2.3.1 Poor noise immunity.

The peak method of inductor current control functions by comparing the upslope of inductor current (or switch current) to a current program level set by the outer loop. The comparator turns the power switch off when the instantaneous current reaches the desired

level. The current ramp is usually quite small compared to the programming level, especially when V_{in} is low. As a result, this method is extremely susceptible to noise. A noise spike is generated each time the switch turns on. A fraction of a volt coupled into the control circuit can cause it to turn off immediately, resulting in a sub-harmonic operating mode with much greater ripple. Circuit layout and bypassing are critically important to successful operation.

5.2.3.2 Slope compensation required:

The peak current mode control method is inherently unstable at duty ratios exceeding 0.5, resulting in sub-harmonic oscillation. A compensating ramp (with slope equal to the inductor current down slope) is usually applied to the comparator input to eliminate this instability. In a buck regulator the inductor current down slope equals V_o/L**.** With V_o constant, as it usually is, the compensating ramp is fixed and easy to calculate-but it does complicate the design. With a boost regulator in a high power factor application, the down slope of inductor current equals $(V_{in}-V_o)/L$ and thus varies considerably as the input voltage follows the rectified sine waveform. A fixed ramp providing adequate compensation will overcompensate much of the time, with resulting performance degradation and increased distortion.

5.2.3.3 Peak to average current error:

The peak to average current error inherent in the peak method of inductor current control is usually not a serious problem in conventional buck derived power supplies. This is because inductor ripple current is usually much smaller than the average full load inductor current, and because the outer voltage control loop soon eliminates this error. In high power factor boost pre-regulators the peak/avg error is very serious because it causes distortion of the input current waveform. While the peak current follows the desired sine wave current program, the average current does not. The peak/avg error becomes much worse at lower current levels, especially when the inductor current becomes discontinuous as the sine wave approaches zero every half cycle. To achieve low distortion, the peak/avg error must be small. This requires a large inductor to make the ripple current small. The resulting shallow inductor current ramp makes the already poor noise immunity much worse.

5.3 AVERAGE CURRENT MODE CONTROL:

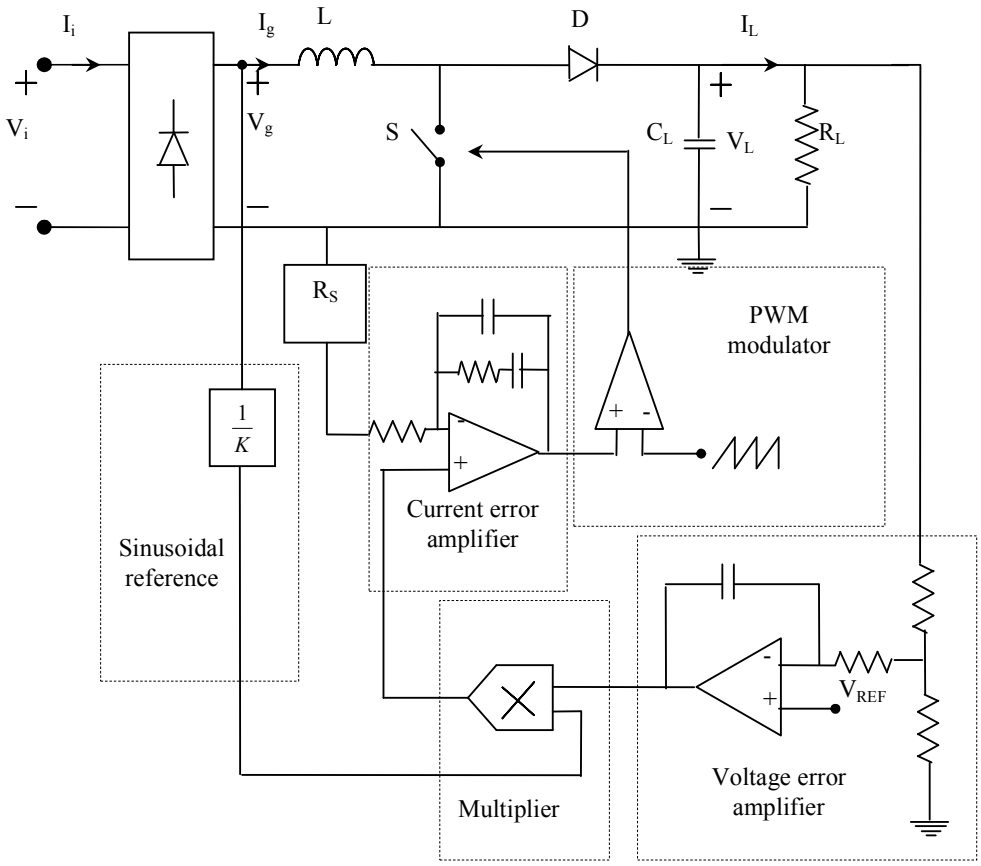
Another control method, which allows a better input current waveform, is the average current control represented in Fig.5.3 [21, 23-25]. Here the inductor current is sensed and filtered by a current error amplifier whose output drives a PWM modulator. In this way the inner current loop tends to minimize the error between the average input current i_g and its reference. This latter is obtained in the same way as in the peak current control.

The converter works in CICM, so the same considerations done with regard to the peak current control can be applied.

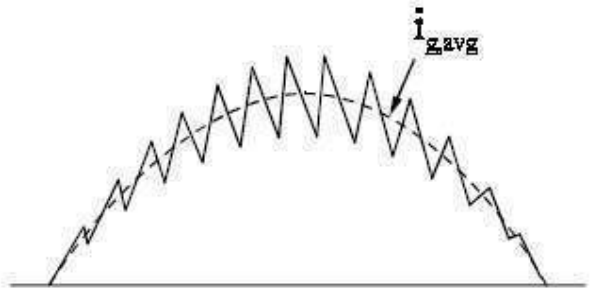
The technique of average current mode control overcomes the problems of peak current mode control by introducing a high gain integrating current error amplifier *(CA)* into the current loop. The gain-bandwidth characteristic of the current loop can be tailored for optimum performance by the compensation network around the *CA*. Compared with peak current mode control, the current loop gain crossover frequency f_c, can be made approximately the same, but the gain will be much greater at lower frequencies.

The result is:

1. Average current tracks the current program with a high degree of accuracy. This is especially important in high power factor pre-regulators, enabling less than 3% harmonic distortion to be achieved with a relatively small inductor. In fact, average current mode control functions well even when the mode boundary is crossed into the discontinuous mode at low current levels. The outer voltage control loop is oblivious to this mode change.
2. Slope compensation is not required, but there is a limit to loop gain at the switching frequency in order to achieve stability.
3. Noise immunity is excellent. When the clock pulse turns the power switch on, the oscillator ramp immediately dives to its lowest level, volts away from the corresponding current error level at the input of the PWM comparator.
4. The average current mode method can be used to sense and control the current in any circuit branch. Thus it can control input current accurately with buck and flyback topologies, and can control output current with boost and flyback topologies.



(a)



(b)

Fig. 5.3 Average current control scheme.

5.3.1 Advantages:

1. Constant switching frequency;
2. No need of compensation ramp;
3. Control is less sensitive to commutation noises, due to current filtering;
4. Better input current waveforms than for the peak current control since, near the zero crossing of the line voltage, the duty cycle is close to one.

5.3.2 Disadvantages:

1. Inductor current must be sensed;
2. A current error amplifier is needed and its compensation network design must take into account the different converter operating points during the line cycle.

Many control IC's are available from different manufacturers: UC1854/A/B family (Unitrode), UC1855 (Unitrode), TK3854A (Toko), ML4821 (Micro Linear), TDA4815, TDA4819 (Siemens), TA8310 (Toshiba), L4981A/B (SGS-Thomson), LT1248, LT1249 (Linear Technology).

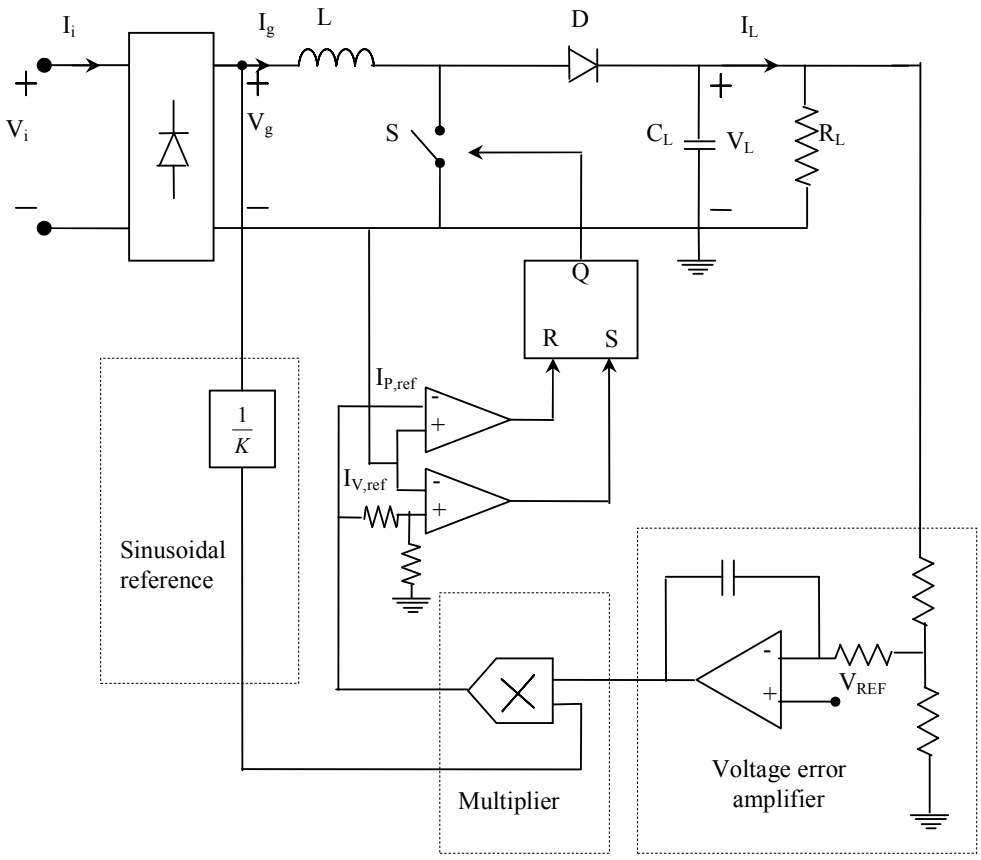
5.4 HYSTERESIS CONTROL:

Fig. 5.4 shows this type of control in which two sinusoidal current references $I_{P,ref}$, $I_{V,ref}$ are generated, one for the peak and the other for the valley of the inductor current. According to this control technique, the switch is turned on when the inductor current goes below the lower reference $I_{V,ref}$ and is turned off when the inductor current goes above the upper reference $I_{P,ref}$, giving rise to a variable frequency control [26-27].

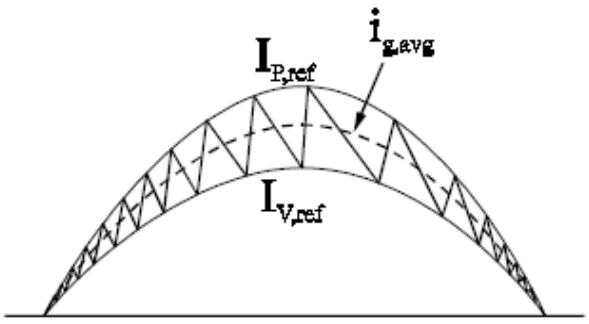
In order to avoid too high switching frequency, the switch can be kept open near the zero crossing of the line voltage so introducing dead times in the line current. An analysis of the power factor as a function of these dead times can be found in [26].

5.4.1 Advantages:

1. No need of compensation ramp;
2. Low distorted input current waveforms.



(a)



(b)

Fig. 5.4 Hysteresis control scheme.

5.4.2 Disadvantages:

1. Variable switching frequency;
2. Inductor current must be sensed;
3. Control sensitive to commutation noises.

A control IC which implements this control technique is the CS3810 (Cherry Semiconductor).

5.5 BORDERLINE CONTROL:

In this control approach the switch on-time is held constant during the line cycle and the switch is turned on when the inductor current falls to zero, so that the converter operates at the boundary between Continuous and Discontinuous Inductor Current Mode (CICM-DICM) [28]. In this way, the freewheeling diode is turned off softly (no recovery losses) and the switch is turned on at zero current, so the commutation losses are reduced. On the other hand the higher current peaks increase device stresses and conduction losses and may call for heavier input filters (for some topologies).

This type of control is a particular case of hysteresis control in which the lower reference $I_{V,ref}$ is zero anywhere. The principle scheme is shown in Fig.5.5. The instantaneous input current is constituted by a sequence of triangles whose peaks are proportional to the line voltage. Thus, the average input current becomes proportional to the line voltage without duty-cycle modulation during the line cycle. This characterizes this control as an "*automatic current shaper*" technique.

Note that the same control strategy can be generated, without using a multiplier, by modulating the switch on-time duration according to the output signal of the voltage error amplifier. In this case switch current sensing can be eliminated.

5.5.1 Advantages:

1. No need of a compensation ramp;
2. No need of a current error amplifier;
3. For controllers using switch current sensing, switch current limitation can be introduced.

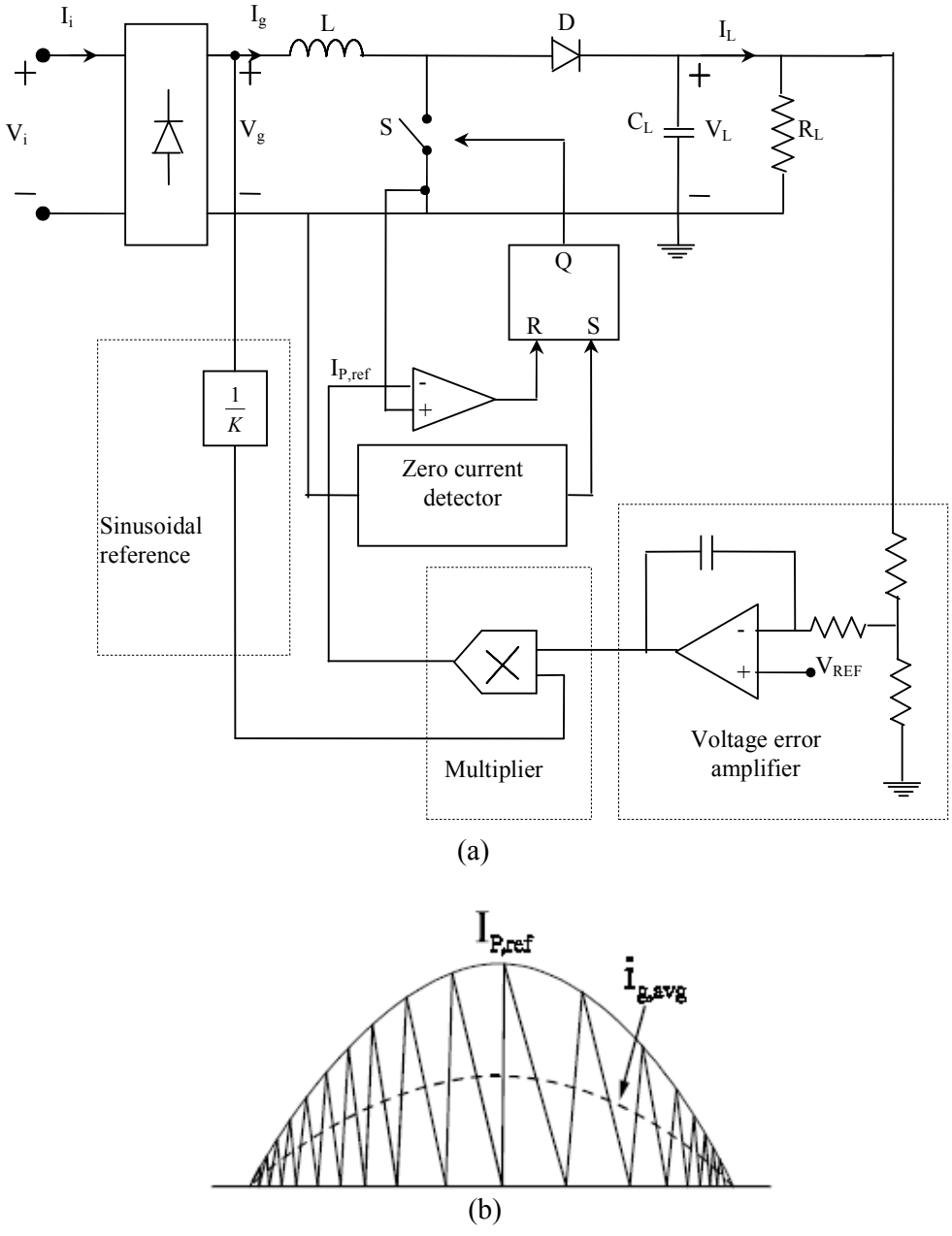


Fig. 5.5 Borderline control scheme.

5.5.2 Disadvantages:

1. Variable switching frequency;
2. Inductor voltage must be sensed in order to detect the zeroing of the inductor current;
3. For controllers in which the switch current is sensed, control is sensitive to commutation noises.

Specific control IC's are: TDA4814, TDA4816, TDA4817, TDA4818 (Siemens), SG3561 (Silicon General), UC1852 (Unitrode), MC33261, MC33262 (Motorola), L6560 (SGS-Thomson).

5.6 CONTROL IC'S:

In table 5.1 commercially available control IC's for PFC applications are summarized.

Table 5.1: available control IC's for PFC applications:

Control technique	Control IC's available
Constant frequency peak current control.	ML4812 (Micro Linear), TK84812 (Toko)
Constant frequency average current control.	UC1854/A/B family (Unitrode), UC1855 (Unitrode), TK3854A (Toko), ML4821 (Micro Linear), TDA4815, TDA4819 (Siemens), TA8310 (Toshiba), L4981A/B (SGS-Thomson), LT1248, LT1249 (Linear Tech.).
Hysteresis control.	CS3810 (Cherry Semic.).
Borderline control.	TDA4814, TDA4816, TDA4817, TDA4818 (Siemens), SG3561 (Silicon General), UC1852 (Unitrode), MC33261, MC33262 (Motorola), L6560 (SGS-Thomson).

5.7 SIMULATION RESULTS:

5.7.1 Peak current control:

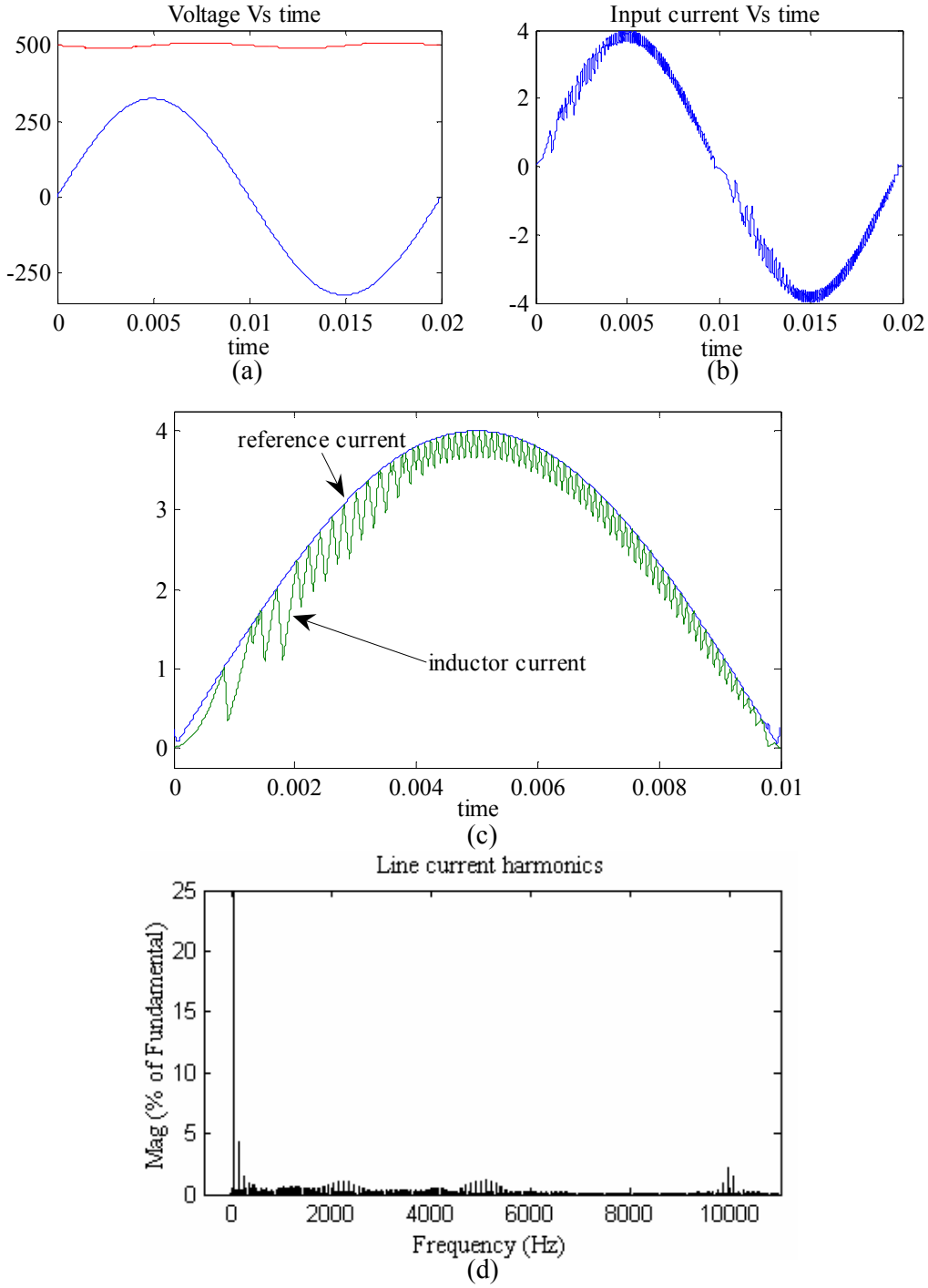


Fig. 5.6 peak current controlled boost converter. (a)Input voltage and output voltage; (b) Input current; (c) Inductor current and reference current; (d) Line current harmonics for AC line voltage $V_1=230V_{rms}$, output voltage $V_0=500V_{dc}$, resistive load $R=500\Omega$, $C_f=470\mu F$, $L_d=200mH$ operating at switching frequency 10kHz, the line current has THD=7.10%, Kp=0.9975, cosΦ=0.9999 and power factor=0.9975.

5.7.2Average current control:

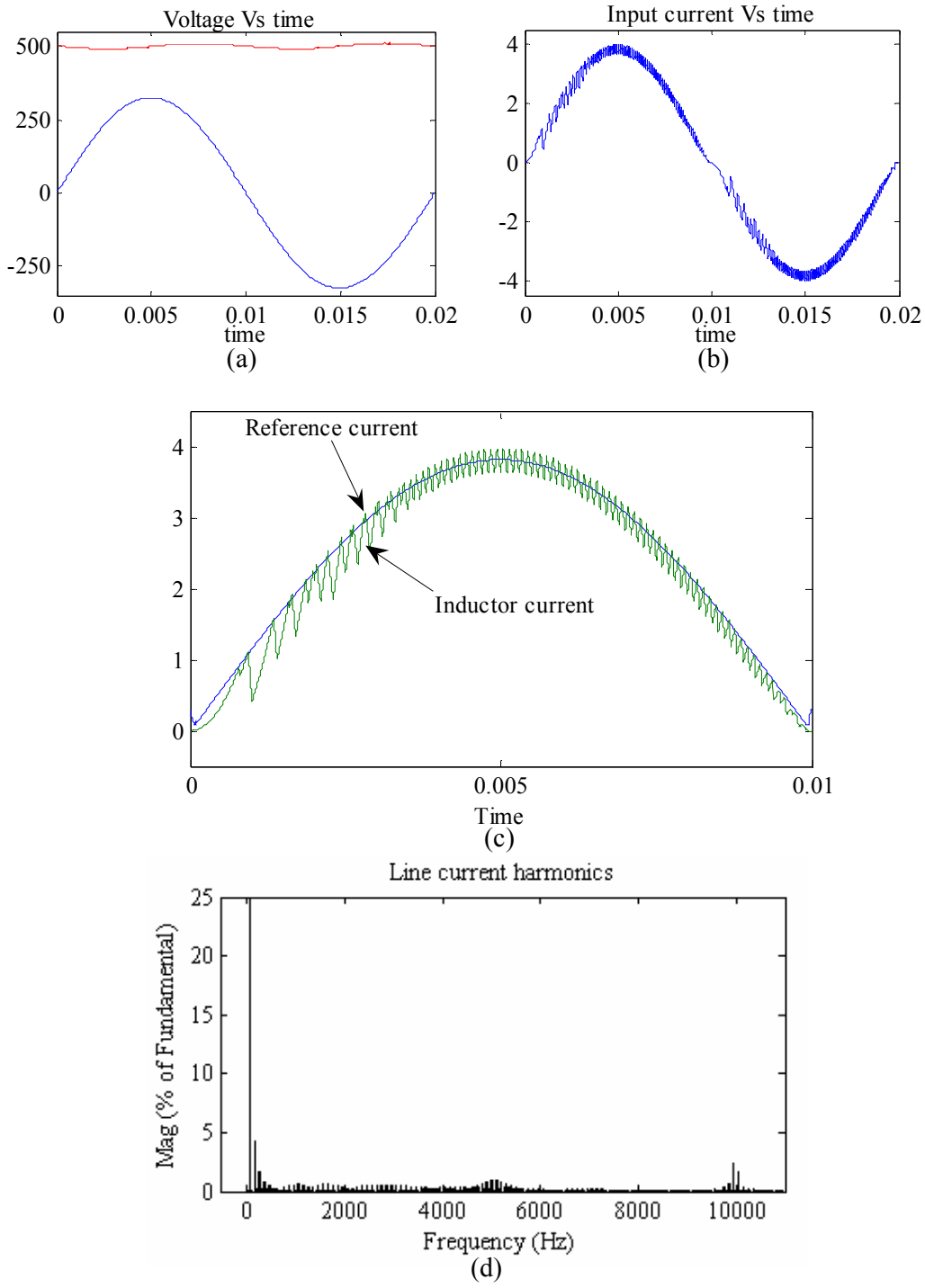


Fig. 5.7 Average current mode controlled boost converter. (a) Input voltage and output voltage; (b) Input current; (c) Inductor current and reference current; (d) Line current harmonics for AC line voltage V_1=230V_{rms}, output voltage V_0=500V_{dc}, resistive load R=500Ω, C_f=470μF, L_d=200mH operating at switching frequency 10kHz, the line current has THD= 6.8175%, Kp= 0.99768, cosΦ=0.9999 and power factor= 0.99768.

5.7.3 Hysteresis control:

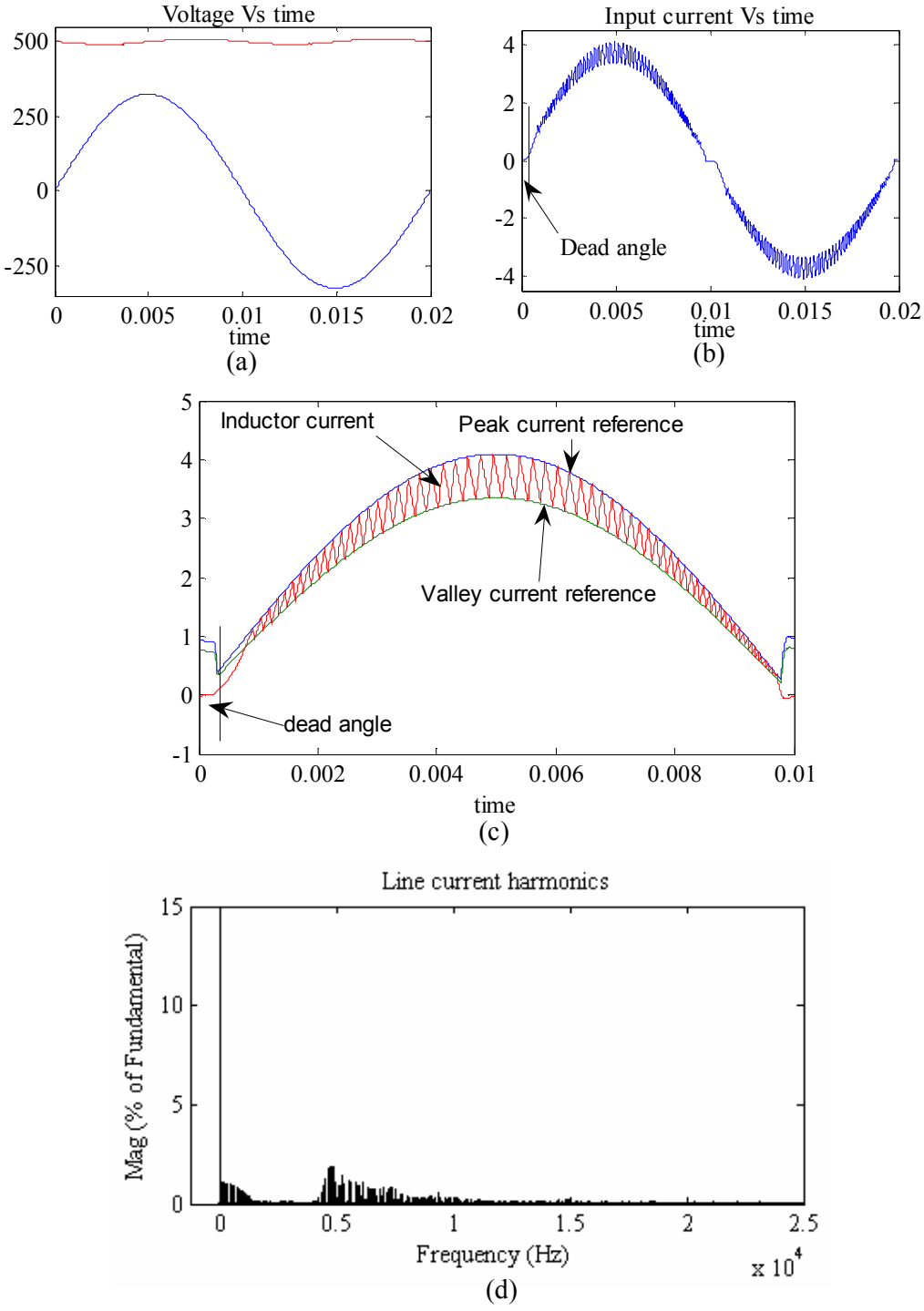


Fig. 5.8 Hysteresis controlled boost converter. (a) Input voltage and output voltage; (b)Input current; (c) Inductor current and reference current; (d) Line current harmonics for AC line voltage $V_1=230V_{rms}$, output voltage $V_0=500V_{dc}$, resistive load $R=500\Omega$, $C_f=470\mu F$, $L_d=200mH$, dead angle $\theta=5^0$, current ripple 20% and the line current has THD= 6.4967%, Kp= 0.9979, cosΦ=0.99999 and power factor= 0.99788.

5.7.3 Hysteresis control:

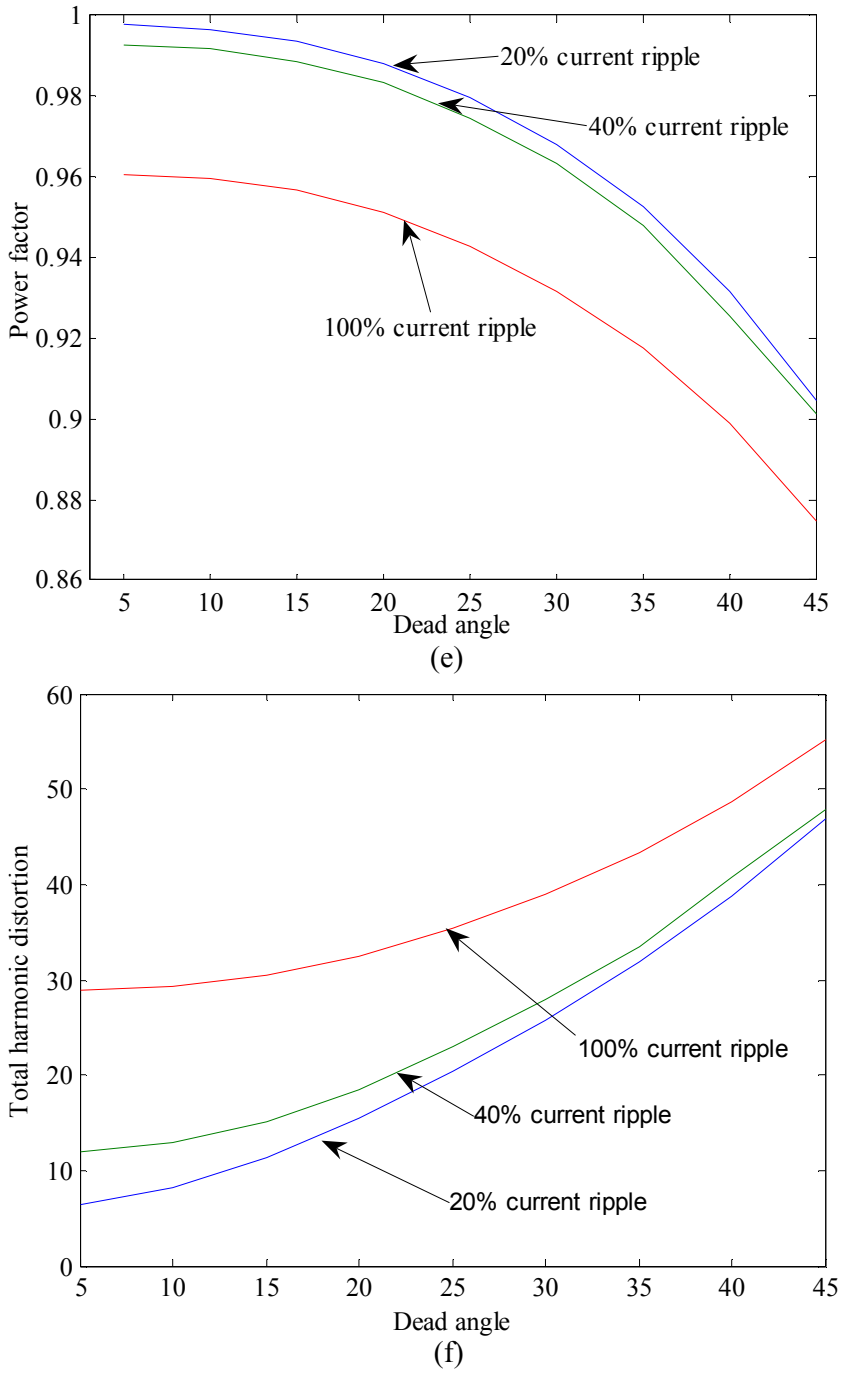


Fig. 5.8 (continued...) Hysteresis controlled boost converter. (e) Power factor at various dead angles for different current ripples; (f) Total harmonic distortion versus dead angle.

5.7.4 Borderline control:

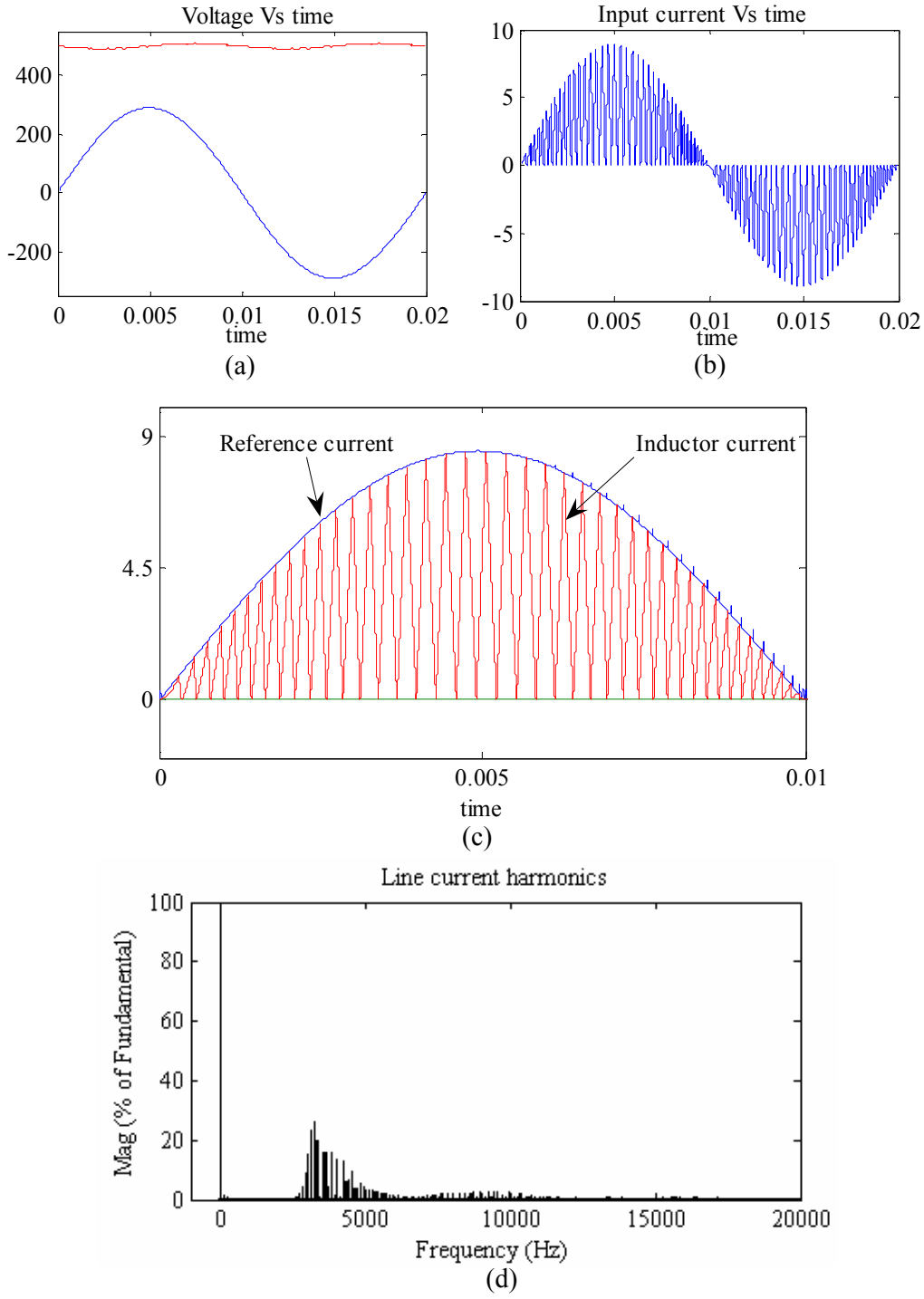


Fig. 5.9 Borderline controlled boost converter. (a) Input voltage and output voltage; (b)Input current; (c) Inductor current and reference current; (d) Line current harmonics for AC line voltage V_1=230V_{rms}, output voltage V_0=500V_{dc}, resistive load R=500Ω, C_f=470μF, L_d=5mH and the line current has THD=0.5892, Kp=0.8615, cosΦ=0.9999 and power factor=0.8615.

Summary:

In this chapter, several control techniques specifically developed for PFC boost converters are analyzed. For each control strategy advantages and drawbacks are highlighted and information on available commercial IC's is given.

Even though peak current control gives better characteristics, it has several drawbacks, such as: poor noise immunity, need of slope compensation, peak to average current error. These problems can be eliminated by average current control at the cost of increased circuit complexity.

Hysteresis control and borderline control leads to variable frequency operation which may create sub-harmonic components. In borderline control, due to the presence of high current ripple it has high harmonic distortion. Hence the maximum power factor obtained will be limited to 0.87.

Hence, peak and average current control techniques are the most preferable control techniques.

These converters operating in CICM reduces the line current harmonics, it also has drawbacks, such as:

1) It increases the EMI, due to the high-frequency content of the input current.

2) It introduces additional losses, thus reducing the overall efficiency and

3) It increases the complexity of the circuit, with negative effects on the reliability of the equipment, as well as on its size, weight and cost.

The high frequency EMI can be eliminated by introducing an EMI filter between AC supply and diode bridge rectifier. The additional losses will be reduced by using soft switching techniques such as ‘ZVS’, ‘ZCS’ and ‘ZVT’.

Some of the basic EMI filter requirements and a novel Zero Voltage Transition – ZVT technique, which can be applied to boost converter used in the PFC stage will be discussed in the next chapters.

CHAPTER 6

EMI FILTER REQUIREMENTS

One stage LC filter for attenuating differential-mode EMI

First requirement

Second requirement

Third requirement

6. EMI FILTER REQUIREMENTS

The high-frequency ripple of the input current of switching converters generates differential-mode EMI, while the common-mode EMI is a result of secondary, usually parasitic, effects. Typically, the differential-mode EMI is dominant below 2MHz, while the common-mode EMI is dominant above 2MHz [29].

6.1 One stage LC filter for attenuating differential-mode EMI:

A high-frequency active PFC stage significantly increases the differential-mode EMI, typically by 30dB to 60dB according to [30] and an EMI filter must be used to comply with EMI standards. There are three main requirements concerning the design of the EMI filter for a PFC stage [31]. To discuss them, let us consider a one-stage LC filter, as shown in Fig. 6.1 (a).

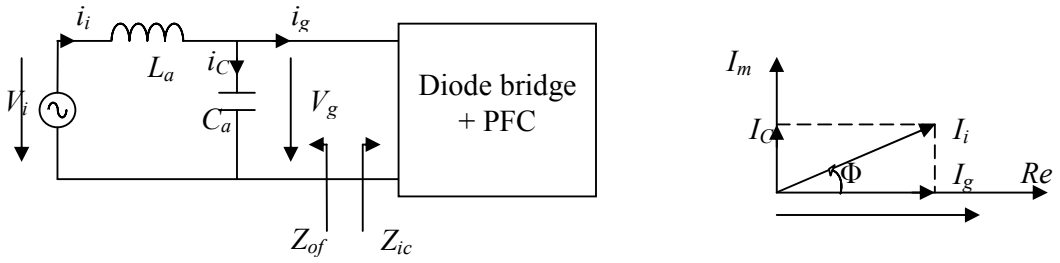


Fig. 6.1 One-stage LC filter for attenuating differential-mode EMI: a) Schematic; b) Phasor diagram of line-frequency components of the system currents and voltages.

6.1.1 First requirement:

The first requirement for the EMI filter is to provide the required attenuation, in order to ensure compliance with the EMI standards.

6.1.2 Second requirement:

Fig. 6.1(b) shows the phasor diagram of the line-frequency components of the system currents and voltages. We assume that the input current i_g of the PFC stage is sinusoidal and in phase with the input voltage v_g which, assuming that the voltage drop across the filter inductor L_a is very small at line-frequency, is essentially equal to the line voltage vi . The capacitive current I_C which is proportional to C_a, introduces a displacement angle Φ between the line current I_i and the line voltage V_i, which degrades the power factor.

This leads to the second requirement for the EMI filter: the displacement angle Φ must be kept low. Hence, the capacitance C_a that can be used is upper limited.

$$C_a < C_{max},$$

As a consequence, the inductance L_a is lower limited

$$L_a > L_{min}$$

In order to have a product L_aC_a that gives the required attenuation.

6.1.3 Third requirement:

The third requirement is related to the overall stability of the system. It is known that unstable operation may occur due to the interaction between the EMI filter and the power stage. This phenomenon is analyzed in several publications, including [32] for peak current mode controlled DC/DC converters, and [33] and [34] for power factor correctors with average current mode control. To explain it, let us consider the thevenin equivalent circuit shown in Fig. 6.2, of the EMI filter/PFC stage interconnection from Fig.6.1 (a). H_f is the transfer function of the filter, Z_{of} is the output impedance of the EMI filter and Z_{ic} is the input impedance of the PFC stage.

From the equivalent circuit, we can write:

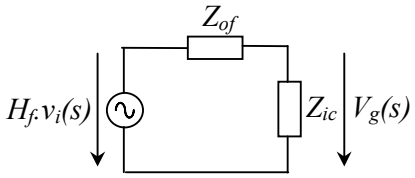


Fig.6.2 Thevenin's equivalent circuit

$$\frac{v_g(s)}{v_i(s)} = \frac{H_f(s)}{1+\dfrac{Z_{of}(s)}{Z_{ic}(s)}} = \frac{H_f(s)}{1+T_f(s)}$$

Where $T_f = Z_{of}/Z_{ic}$ can be considered as a loop gain that must satisfy the Nyquist criterion for stability. The interaction between the EMI filter and the power converter is minimized and no instabilities can arise in the system, if $|T_f|<<1$. This means that the modulus of the output impedance of the EMI filter must be much lower than the modulus of the input impedance of the power converter, $|Z_{of}|<<|Z_{ic}|$. The aforementioned condition may be difficult to fulfill in a PFC application. This is because, at the resonant frequency of the EMI filter, the modulus of the output impedance Z_{of} has a maximum that is proportional to $\sqrt{L_a/C_a}$, which cannot be set arbitrarily low since C_a is upper limited and L_a is lower limited. Hence, in a PFC application it is possible to have $|T_f|>1$, especially at low Z_{ic}, i.e. at low line voltage and high load current. Therefore, if the input impedance Z_{ic} shows an excessive positive phase shift, then $T_f = Z_{of}/Z_{ic}$ may not satisfy the Nyquist criterion for stability and instabilities

occur. For this reason, it is important to know the input impedance Z_{ic} of the PFC stage, in order to be able to perform the stability analysis.

CHAPTER 7

METHODS FOR IMPROVING THE EFFICIENCY

Reduction of conduction losses

Reduction of switching losses

An improved ZVT technique

Simulation results

Summary

7. METHODS FOR IMPROVING THE EFFICIENCY:

The PFC stage performs an additional power processing operation, and therefore it has a negative impact on the overall efficiency of the power supply. We can improve the efficiency by reducing the switch conduction losses in the combined diode bridge and PFC stage, as well as on circuit techniques for reducing the switching losses.

7.1 REDUCTION OF CONDUCTION LOSSES:

Conduction losses are caused by the current flowing through a non-ideal switching device in the on-state, which determines a certain voltage drop on the device. A static model of the switching device is useful for estimating the conduction losses. Static models are presented in Fig. 7.1, for on-state diode and MOSFET.

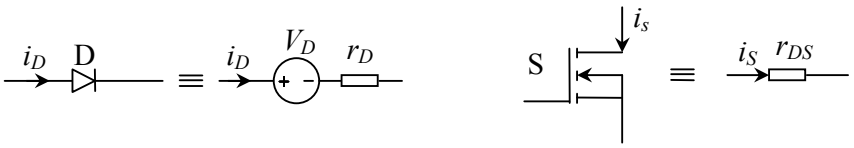


Fig. 7.1 Static models for an on-state switching device: a) Diode; b) MOSFET.

As shown in Fig. 7.1, the static characteristic of the on-state diode can be modeled as a voltage source V_D in series with a resistor r_D. On the other hand, the appropriate static model for the on-state MOSFET is just resistor r_{DS}. With these models, it is straightforward to calculate the conduction losses of diode D:

$$P_{D,cond} = V_D I_{D,av} + r_D I_{D,rms}^2 \qquad \text{..... (7.1)}$$

Where $I_{D,av}$ and $I_{D,rms}$ are the average and RMS diode currents, respectively. Similarly, the conduction losses of switch S (MOSFET) are expressed as:

$$P_{D,cond} = r_{DS} I_{S,rms}^2 \qquad \text{.....(7.2)}$$

Where $I_{S,rms}$ is the RMS switch current.

Naturally, the total conduction losses of the combined diode bridge and PFC stage are the sum of the individual conduction losses of the switches. Considering also (7.1) and (7.2), we can conclude that one way to diminish the total conduction losses is to reduce the number of switches that are in the power path and/or to reduce the average/RMS currents flowing through the switches, assuming that the r_{DS} of MOSFETs and the V_D and r_D of diodes remain unchanged.

7.2 REDUCTION OF SWITCHING LOSSES:

The commutation process of real switching devices takes a certain time, during which the instantaneous power dissipated in the device can be very large. Therefore, switching losses are a major reason for decreased efficiency in converters.

The source of the switching losses [16, pp.94-104]:

1. During turn-on and turn-off of the active switch S, the switch voltage V_S and the switch current i_S has simultaneously non-negligible values, so a significant instantaneous power $P_S=V_S i_S$ is dissipated in the switch. The energy lost at turn-off is particularly significant in IGBTs, due to the current tailing that occurs during this transition.
2. Some amount of minority charge is stored in diode D while it is conducting. When the diode turns off, the stored charge must be removed during the reverse recovery process, before it can establish a reverse biased operating point. While some of the charge is removed by recombination within the diode, a part Q_r is recovered through a negative current i_D, which flows through the active switch as well. On the other hand, while this process takes place, the active switch voltage is practically $v_S=V_1$, because the diode remains forward biased. As a consequence, the reverse recovery process of the diode induces switching losses in the active switch *S*.
3. When the active switch *S* is turned-on, its parasitic capacitance, e.g. For a MOSFET the drain-source capacitance C_{DS}, is shunted and the energy stored in it is dissipated in the switch.
4. When a switch is conducting, inductances effectively in series with it, store energy which is dissipated at turn-off.

The switching losses reduced using soft-switching techniques.

7.2.1 Losses in diode:

1. Switching losses induced by the diode reverse recovery are proportional to the stored charge Q_r.
2. Q_r depends on the on-state diode current i_D=I, as well as on the rate of variation of di_D/dt.
3. Q_r is reduced if di_D/dt is limited, typically $di_D/dt < 100\text{A}/\mu\text{s}$ [35].

4. This technique is used in some passive snubbers.

7.2.2 Capacitive losses:

1. The capacitive turn-on losses can be theoretically eliminated.

7.2.3 Losses in active switch:

1. The overlap of non-negligible active switch voltage and current can be avoided at turn-on by using the "Zero Voltage Switching" (ZVS) technique.
2. This technique consists of forcing the active switch voltage to zero, prior to its turn-on, by creating a resonance between an inductor and a capacitor
3. The inductor also limits the rate of variation of the diode current, so the losses due to the reverse recovery are reduced as well.

Better characteristics are obtained in Zero Voltage Transition – ZVT topologies, at the expense of increased complexity. Several ZVT topologies have been published, e.g. in [36], [37], [38], [35] and [39].

Here, to achieve ZVS, switch voltage and current waveforms are changed only during commutation intervals, the behavior of the ZVT converter being otherwise identical to that of the hard-switching converter. In converter topologies having only one active switch, the ZVT technique is implemented with an auxiliary circuit, which consists of an additional active switch, an auxiliary inductor, for the resonant process that discharges the drain-source capacitance of the switch and for limiting the rate of change of the diode current at turn-off, as well as a few other passive components.

While having increased complexity as a main drawback, ZVT and ZCT topologies have also clear advantages. The switching losses are reduced, without the need to alter the switch waveforms during the conduction intervals of the main switches. In addition to this, because the operation of the original hard-switching converter is altered only during switching intervals, the design of the converter itself and of its control circuit can be made in a similar manner as for the original hard switching converter.

An improved Zero-Voltage-Transition Technique (ZVT-Technique) [40] in a single-phase active power factor correction circuit based on a dc-dc boost converter topology and operated in a continuous-inductor-current mode with fixed-switching frequency control is discussed in the next sub-chapter.

7.3 AN IMPROVED ZVT TECHNIQUE:

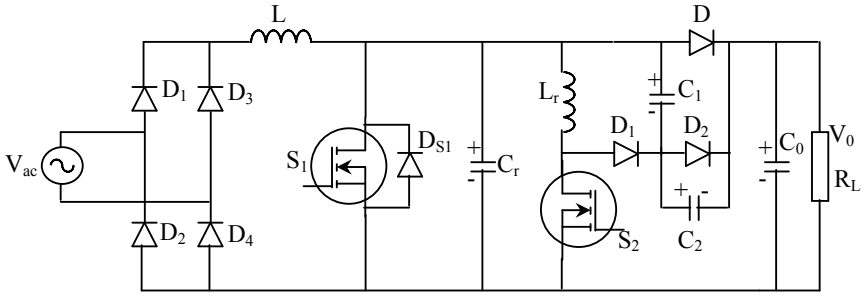


Fig.7.2 ZVT PWM boost PFC converter.

7.3.1 Circuit description and operation:

The power stage of the converter [40] is shown in Fig. 7.2. The additional circuitry of the converter is consisted of a diode (D_2) and two capacitors (C_1, C_2).The converter operates in a continuous current mode with fixed frequency controlled by peak current control technique. By inserting additional circuit, all of the switches, including auxiliary switches, are only turned-on and off at soft-switching.

The ZVT converter has eight operating modes. The ideal waveform and equivalent circuit of each mode are shown in fig. 7.3 and fig. 7.4, respectively. To analyze the steady state operation, all components and devices are assumed to be ideal and the boost inductor (L) and output capacitor (C_O) are assumed to be large enough to treat as a current source and a voltage source, respectively.

7.3.1.1 Mode of Operation:

The operations of each mode are explained as follows:

Mode 1 [t_o-t_1]:

Prior to $t = t_o$, the main switch S_1 and the auxiliary switch S_2 are turned-off, and main diode D is conducting. At $t = t_o$, S_2 is turned-on, the resonant inductor current i_{Lr} linearly ramp up until it reaches I_{in} at t_1, where main diode D is turned-off with soft-switching. The voltage and current expressions which govern this circuit mode are given by:

$$i_{Lr} = \frac{V_0}{L_r} t \quad and$$

$$V_{Cr} = V_{Lr} = V_0$$

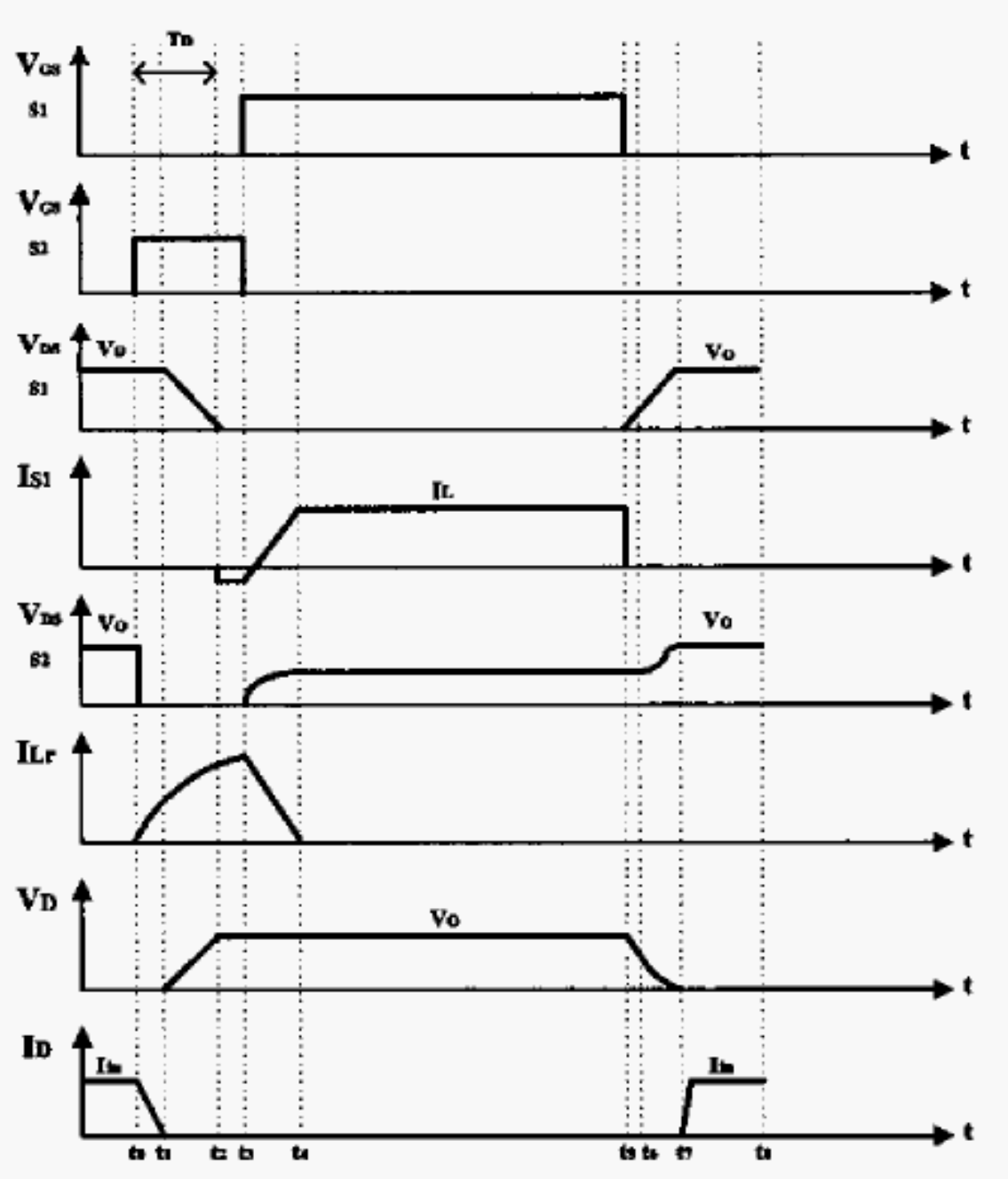


Fig. 7.3 Theoretical waveforms of the ZVT converter.

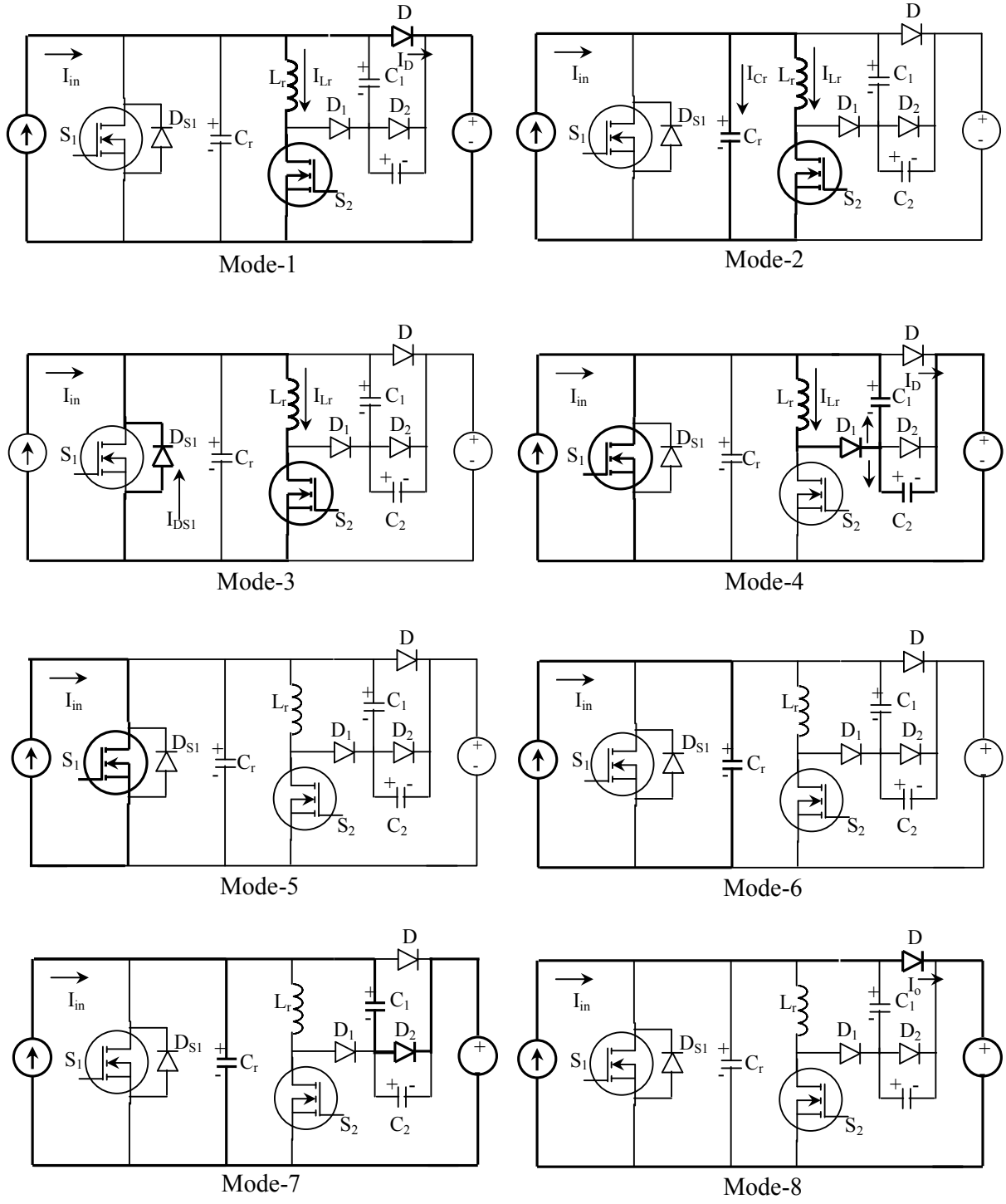


Fig. 7.4 Equivalent circuit of each operating mode.

Mode 2[t_1 - t_2]:

At t_1, the resonant inductor current i_{Lr} reaches I_{in}, L_r, and C_r begin to resonate. The resonant capacitor voltage V_{Cr} is equal to V_0 .The voltage and current expressions are given by:

$$I_{Lr} = I_{in} + \frac{V_0}{Z_n}\sin\omega_n(t - t_1)$$

$$V_{Cr} = V_0\cos\omega_n(t - t_1)$$

Where $Z_n = \sqrt{\frac{L_r}{C_r}}$ *and* $\omega_n = \frac{1}{\sqrt{L_r C_r}}$.

Mode 3 [$t_2 - t_3$]:

When V_{Cr} reaches zero the body diode D_{S1} of the main switch conducts providing a freewheeling way for I_{Lr}. At this instant, main switch S_1 can be turned on at zero voltage. The current I_{DS1} is given by

$$I_{DS1} = \left[I_{in} + \frac{V_0}{Z_n}\right] - I_{in} = \frac{V_0}{Z_n}$$

Mode 4 [$t_3 - t_4$]:

Auxiliary switch S_2 is turned off with near ZVS at t=t_3. The energy stored in the resonant inductor L_r is transferred to the capacitor C_1 to C_2. Then the voltage polarity of the capacitor C_1 is reversed to negative. During this period, the capacitor C_1 is acting as a turn-off snubber of the auxiliary switch. The energy stored in the capacitor C_2 will be recycled and used to suppress the turn-off voltage spike of the main switch S_1. The voltage and the current expressions of this mode are given by

$$I_{Lr} = I_{Lr}(t_2)\cos\omega_n(t - t_3)$$

$$V_{C1} = Z_n I_{Lr}(t_2)\sin\omega_n(t - t_3)$$

where $Z_n = \sqrt{\frac{L_r}{C_1 + C_2}}$ $\omega_n = \frac{1}{\sqrt{L_r(C_1 + C_2)}}$

Mode 5 [$t_4 - t_5$]:

During this period, the inductor L is charged by the input dc voltage source v_{in} while the main switch S_1 continues to be turned on and the auxiliary switch S_2 is turned off.

Mode 6 [$t_5 - t_6$]:

At t_5, the main switch S_1 begins to turn off, the inductor L charges the resonant capacitor C_r and the voltage across the capacitor increases. The current through L_r equals to zero and the voltage across C_r is given by

$$V_{Cr} = \frac{I_{in}}{C_r} t = \frac{I_L}{C_r} t$$

Mode 7 [$t_6 - t_7$]:

When the increasing voltage across C_r is greater than (V_0+V_{C1}) the capacitor C_1 begins to discharge through the diode D_2. This discharge of C_1 can slow down the rising voltage slope of the rising voltage across C_r or the main switch S_1. Therefore, the capacitor is performing as a tuned off snubber for the main switch to suppress the turned off voltage spike and the turned off voltage slope of the main switch S_1. The voltage across C_r is given by

$$V_{Cr} = V_0 + V_{C1}$$

Mode 8 [$t_7 - t_8$]:

This stage begins when the diode D is turned on under ZVS. The operation of the circuit at this stage is identical to the normal turned off operation of a PWM boost converter. It ends at the moment that S_2 is turned on to begin a new switching cycle.

7.3.1.2 Delay time:

To ensure proper operation of the ZVT soft switching boost PFC converter, a minimum delay time (t_D) of the auxiliary switch S_2 is required. This delay time t_D must satisfy the following condition:

$$t_D \geq \frac{I_{in} L_r}{V_0} + \frac{\pi}{2} \sqrt{L_r C_r}$$

Design procedure can be found in [40].

7.4 SIMULATION RESULTS:

7.4.1 Switching of the main switch:

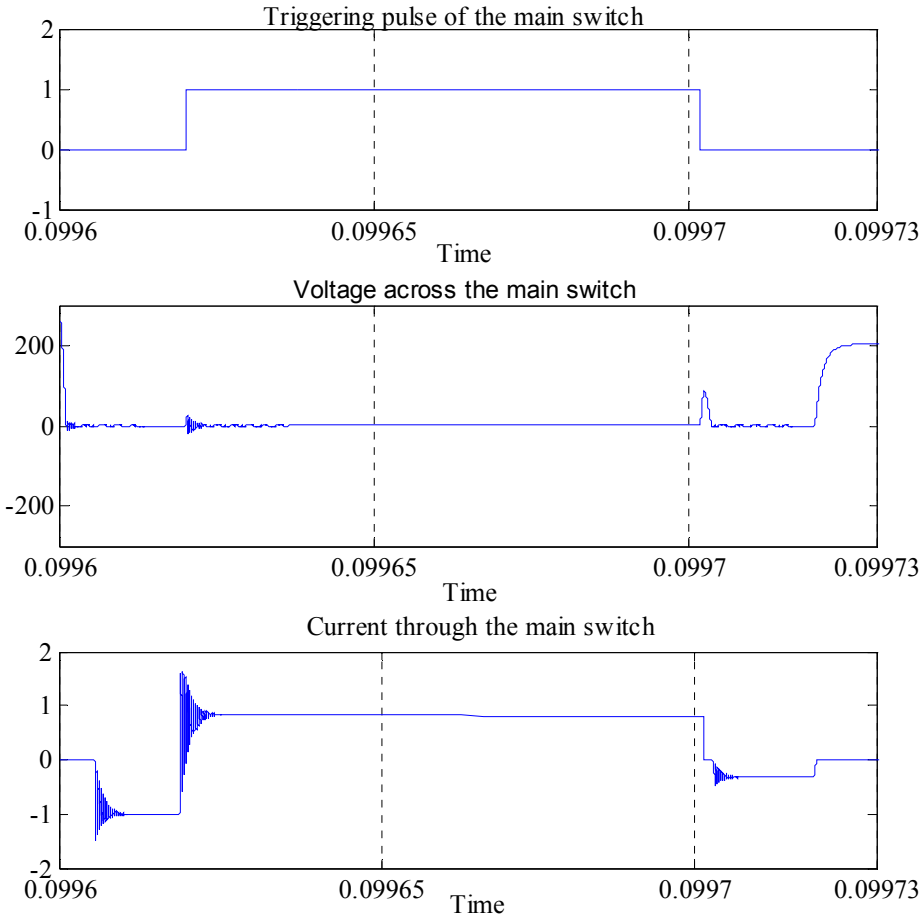


Fig. 7.5 Triggering pulse of the main switch, the voltage across it and the current through the main switch present in ZVT converter during one switching cycle.

From this fig.7.5 we can clearly observe the zero of voltage switching of the main switch S_1 present in the ZVT converter.

7.4.2 Switching of the auxiliary switch:

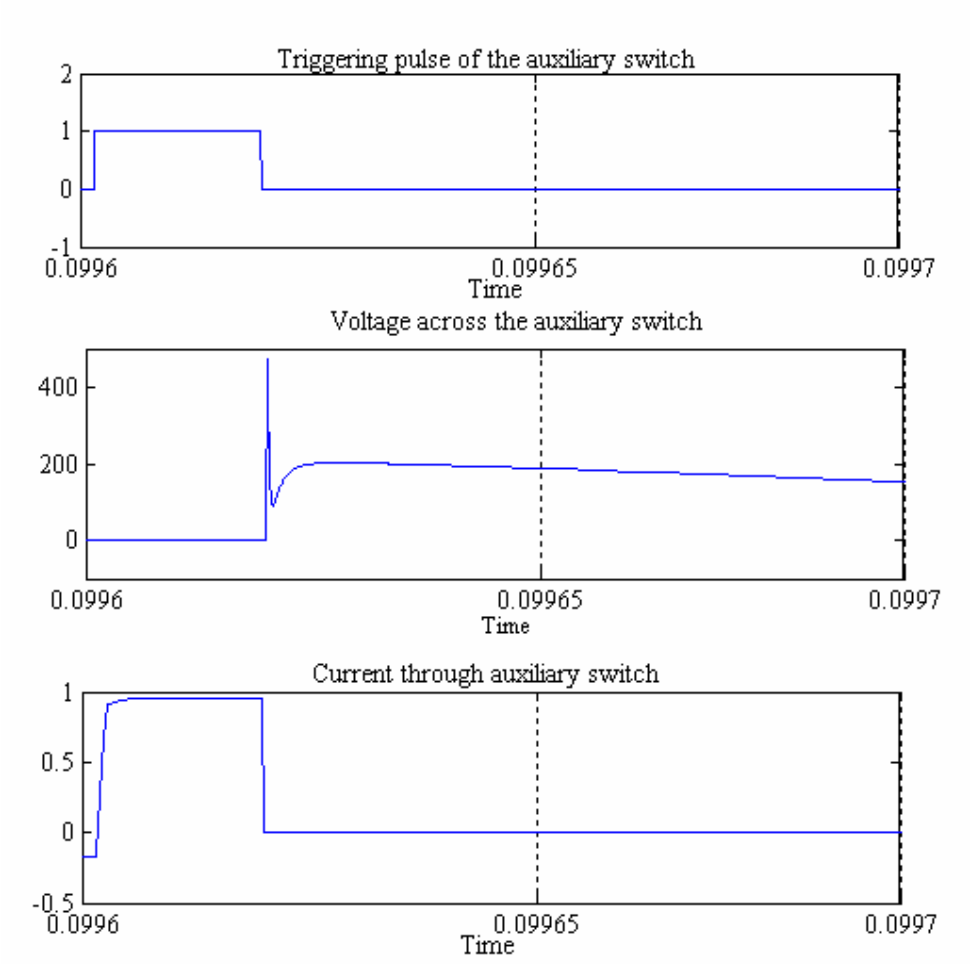


Fig. 7.6 triggering pulse of auxiliary switch and the voltage across it and the current through the auxiliary switch present in ZVT converter during one switching cycle.

From this Fig.7.6 we can clearly observe the zero voltage switching of the auxiliary switch S_2 present in the ZVT converter.

7.4.3 Switching of diode:

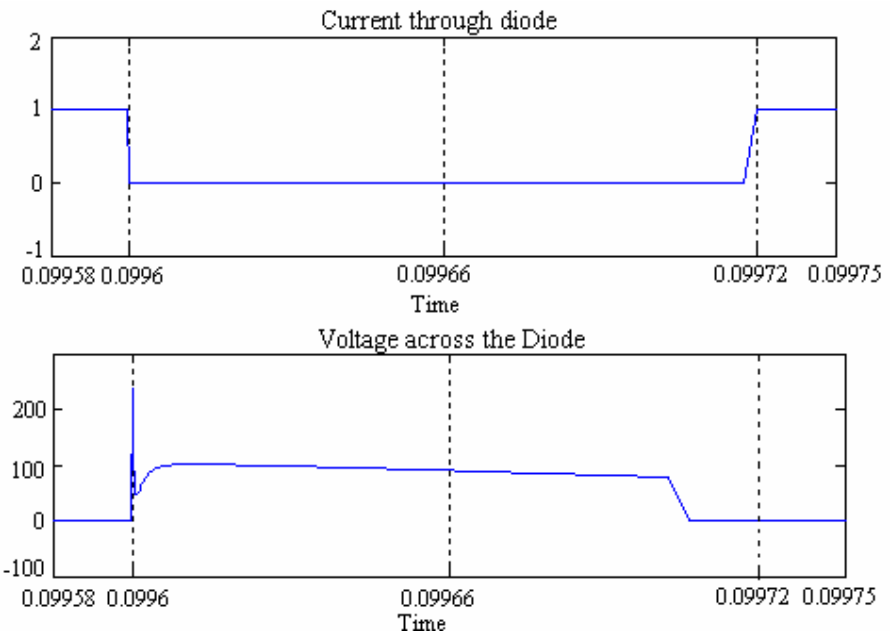


Fig. 7.7 Current through the diode and voltage across the diode during one switching cycle.

From this fig 7.7 we can observe the soft switching of the diode present in the ZVT converter.

7.4.4 Input and output wave forms of the ZVT converter:

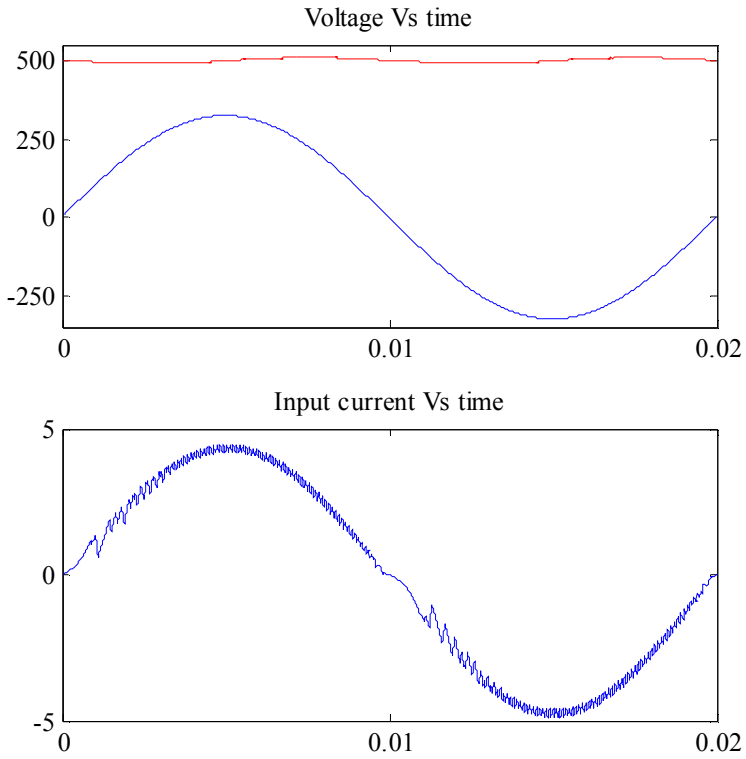


Fig. 7.8 ZVT converter. Input voltage and the output voltage (upper plot) and input current (lower plot) for AC line voltage V_1=230V_{rms}, output voltage V_0=500V_{dc}, resistive load R=500Ω, C_f=470μF, L=33.79mH, L_r=80μH, C_r=1.8nF, C_1=4.7nF and C_2=1.5nF operating at switching frequency 10kHz, the line current has THD= 7.22%, Kp= 0.9974, cosΦ=0.9999 and power factor= 0.9974.

7.4.5 Comparison of different parameters without and with soft-switching.

Table 7.1 comparison of different parameters with and without soft-switching.

Parameters	Without ZVT	With ZVT
THD	0.0669	0.0722
K_P	0.9978	0.9974
cosΦ	1.0000	1.0000
Power factor	0.9977	0.9974
P_{ac}	575.4819W	518.2205W
P_{dc}	499.7793W	499.8873W
Efficiency	86.84%	96.46%

Summary:

The switching losses of the auxiliary switch are minimized by using an additional circuit applied to the auxiliary switch. Besides the main switch ZVS turned-on and turned-off and the auxiliary switch turned-on and turned-off near ZVS. Since the active switch is turned-on and turned-off softly, the switching losses are reduced and the higher efficiency of the system is achieved. The results have been compared with the PFC stage with hard switching.

CHAPTER 8

CONCLUSION

Conclusion

Future work

8 CONCLUSION.

8.1 CONCLUSION.

Reduction of line current harmonics is needed in order to comply with the standard. This is commonly referred to as the Power Factor Correction – PFC.

Power factor correction (PFC) is a technique of counteracting the undesirable effects of electric loads that create a power factor *PF* that is less than 1.

There are several solutions to achieve PFC. Depending on whether active switches (controllable by an external control input) are used or not, PFC solutions can be categorized as "*Passive*" or "*Active*".

Passive PFC:

The passive PFC circuit uses low-frequency filter components to reduce harmonics. This approach typically meets EN standards for Class-A equipment up to 250W, at a much lower cost than a comparable switch mode power supply (SMPS) employing active PFC techniques. They typically yield less PF's compared to active topologies; they require a voltage doubler circuit for universal operation on most topologies above 150W.

First different techniques to implement "*Passive PFC*" have been discussed.

Active PFC:

The preferable type of PFC is Active Power Factor Correction (Active PFC) since it provides more efficient power frequency. Because Active PFC uses a circuit to correct power factor, Active PFC is able to generate a theoretical power factor of over 95%. Active Power Factor Correction also markedly diminishes total harmonics, automatically corrects for AC input voltage, and is capable of a full range of input voltage. Since Active PFC is the more complex method of Power Factor Correction, it is more expensive to produce an Active PFC power supply.

Low-frequency active PFC:

Some of the techniques to implement "*Low-frequency switching active PFC*" have been presented. An active low frequency approach can be implemented up to about 1000 watts. Power factors as high as 0.95 can be achieved with an active low frequency design. To conclude, low-frequency switching PFC offers the possibility to control the output voltage in certain limits. In such circuits, switching losses and high-frequency EMI are negligible. However, the reactive elements are large and the regulation of the output voltage is slow.

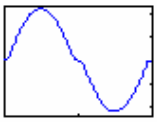
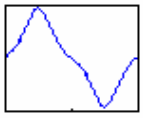
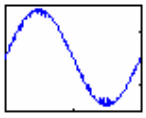
High-frequency active PFC:

Nearly unity power factor can be obtained by "*high-frequency switching active PFC*", if a suitable control method is used to shape its input current or if it has inherent PFC properties. The converters can operate in Continuous Inductor Current Mode – CICM, where the inductor current never reaches zero during one switching cycle, or Discontinuous Inductor Current Mode - DICM, where the inductor current is zero during intervals of the switching cycle.

Operation in discontinuous inductor current mode – DICM:

In DICM, the input inductor is no longer a state variable since its state in a given switching cycle is independent on the value in the previous switching cycle. The peak of the inductor current is sampling the line voltage automatically. This property of DICM input circuit can be called "self power factor correction" because no control loop is required from its input side.

We can conclude that the basic boost converter and buck-boost converter have excellent self-PFC capability naturally. Among them, boost converter is especially suitable for DCM PFC usage and buck-boost is not widely used because of the drawbacks such as: the input voltage and the output voltage don't have a common ground due to the reversed output voltage polarity, etc. Hence, this converter is the most preferable by the designers for power factor correction purpose. Other converters may be used only if their input V-I characteristics have been modified (linearized), or when they operate in continuous inductor conduction mode.

Basic converter	Line current waveform	DICM self PFC	Power level
Buck		Poor	Low to medium
Boost		Fair	Low to medium
Buck-boost		Excellent	Low to medium

In addition, if discontinuous inductor current mode is applied, the input current is normally a train of triangle pulse with nearly constant duty ratio. In this case, an input filter is necessary for smoothing the pulsating input current into a continuous one.

Operation in continuous inductor current mode – CICM:

In CICM, different control techniques are used to convert the non-sinusoidal input current into sinusoidal. Some of them are (1) peak current control (2) average current control (3) Hysteresis control (4) borderline control. Even though these control techniques can be used for all DC-DC converters, only boost converter has been taken for the study because of the continuous input current. These control techniques specifically developed for PFC boost converters are analyzed. For each control strategy advantages and drawbacks are highlighted and information on available commercial IC's is given.

Even though peak current control gives better characteristics, it has several drawbacks, such as: poor noise immunity, need of slope compensation, peak to average current error. These problems can be eliminated by average current control at the cost of increased circuit complexity.

Hysteresis control and borderline control leads to variable frequency operation which may create sub-harmonic components. In borderline control, due to the presence of high current ripple it has high harmonic distortion. Hence the maximum power factor obtained will be limited to 0.87.

Hence, peak and average current control techniques are the most preferable control techniques.

This high frequency switching PFC stage also has drawbacks, such as: it introduces additional losses, thus reducing the overall efficiency; it increases the EMI, due to the high-frequency content of the input current.

Some of the EMI requirements have discussed. But the level of high-frequency EMI is much higher with a considerable amount of conduction and switching losses. This high-frequency EMI will be eliminated by introducing an EMI filter in between AC supply and the diode bridge rectifier.

Finally, to improve the efficiency of the PFC stage, operation of ZVT converter has been discussed, in which the switching losses of the auxiliary switch are minimized by using an additional circuit applied to the auxiliary switch. Besides the main switch ZVS turned-on and turned-off, and the auxiliary switch ZCS turned-on and turned-off near ZVS. Since the active switch is turned-on and turned-off softly, the switching losses are reduced and the higher efficiency of the system is achieved. The results have been compared with the PFC stage with hard switching.

Finally to conclude, the high-frequency active PFC with a suitable control scheme and the soft-switching techniques gives around 0.9976 (almost unity) power factor with an efficiency of around 96%.

8.2 FUTURE WORK:

Throughout this thesis work, we have discussed only the second order converters applied for PFC. Better characteristics can be obtained by using fourth-order converters for PFC.

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