DESIGN OF A 4GHz PROGRAMABLE FREQUENCY SYNTHESIZER FOR IEEE-802.11a STANDERD

A THESIS SUBMITTED IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF

Master of Technology
In
VLSI Design & Embedded System
By

Ashutosh Abhishek
210EC2062

Under the Guidance of
Prof. Debiprasad Priyabrata Acharya

Department of Electronics and Communication Engineering

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CERTIFICATE

This is to certify that the thesis entitled, **"DESIGN OF A 4GHz PROGRAMABLE FREQUENCY SYNTHESIZER FOR IEEE-802.11a STANDERD"** submitted by **ASHUTOSH ABHISHEK** (210EC2062) in partial fulfilment of the requirements for the award of Master of Technology degree in Electronics and Communication Engineering with specialization in "VLSI Design and Embedded Systems" at National Institute of Technology, Rourkela (Deemed University) and is an authentic study analysis work carried out by him under my supervision.

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other university/institute for the award of any Degree or Diploma.

Date:

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Abstract

Frequency synthesizer is one of the most versatile component and heart of any system. It is used to correct the phase & frequency error so that the signal coming from the different part of the circuit or from the wireless medium does not cause any attenuation or distortion due to frequency dependent or phase dependent error. Present days the Frequency Synthesizer is also used for the wireless communication in the GHz range to correct the phase and frequency error as well as provide synchronization with low locking time, reduced skew and jitter. The frequency synthesizer is used inside a processor to provide the clock synchronization, clock recovery. Due to all above important application in the Analog and mixed signal as well as in digital signal analysis there is a necessity of a Frequency synthesizer with higher Capture range low lock time and with a low settling time. The design of given Frequency synthesizer is done in the 90nm (GPDK 090) process technology in CADANCE virtuoso Analog design environment. To detect the phase and frequency error for any unsymmetrical pulse the voltage based phase frequency detector is used in the design.

Voltage controlled oscillator is also a very important part which decide the range of frequency synthesizer. The VCO used here is a current starved Ring oscillator which consumes a very low power. The loop filter is an important component that decides the Dynamic response of the frequency synthesizer. The rise time damping ratio, settling time, bandwidth and output signal to noise ratio of the circuit. The loop filter used here is a passive lead lag filter which is designed with the resistor and capacitor. The layout of the frequency synthesizer is done in the CADANCE virtuoso XL layout editor and different type of simulation is done in the spectre simulator. The power consumed in the frequency synthesizer is 0.22091 m watt at 1.2 V supply voltage and the lock time is 220 ns. The divider is a very important part which made the frequency synthesizer circuit tuneable in a wide range of input frequency so for this purpose we designed it programmable which divide in N/N+1 ratio.

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CHAPTER 1

INTRODUCTION

1.1 Motivation

The Frequency synthesizer [1-5] is a very important component of any digital circuit and it is the part of the circuit which is used to perform the clock synchronization in the wireless medium when the signal travel a long distance its axis of symmetry change with the axis at the time of transmission of signal so at the time of receiving the signal phase error occurred which finally affect the output of the circuit and it gives frequency offset to the desired output of the circuit

Now a days in the wireless communication the frequency requirements is as high as 4GHz for orthogonal frequency division multiplexing (OFDM) based system for this high frequency the data rate is very high but it is always very sensitive to the multipath fading and phase and frequency error. The noise coming at the input terminal due to phase and frequency error cause the output frequency to deviate so that the output will always produce the deviated frequency response

In recent year there are a lot of researches conducted to provide a Frequency synthesizer which can produce low lock time low settling time, moderate value of damping factor to provide the efficient frequency response at the output.

The Frequency synthesizer is first invented in the year 1932 during the reduction of the reduction of the noise in the radio received signal and it was observed that the signal coming from the distance source is producing some noise if it is not properly tuned and latter it observed that the noise is produced due to mismatch of phase and frequency at the receiver input and a circuit was designed to reduce the phase and frequency error at the receiver side .with the time passes the frequency of operation increases and the requirement of fast loop locking is required

This Frequency synthesizer contains five block phase frequency detector (PFD), charge pump (CP), low pass loop filter (LPF), Voltage controlled oscillator (VCO) and a N/N+1 frequency divider. The requirement for the IEEE 802.11a standard is that operating frequency must lie in between the 3.4 GHz to 4GHz. The operation of this Frequency synthesizer in such a way that it divide the given frequency in the fractional ratio with the help of the N/N+1 frequency divider Performing the entire task with a good frequency precision and in a very low locking time is the difficulty and the division of the VCO output in fractional ratio with the help of N/N+1 is also a motivation to take this project

1.2 Organization of Thesis

The detailed description of the frequency synthesizer is given in the next section but in the first chapter I have described the motivation behind this project in the chapter 1. The chapter 2 consist detailed description of frequency synthesizer system where the Phase frequency detector has been described in. The section 2.2 described about the charge pump and calculation of phase error through the charge pump .the current starved VCO has been explained in section 2.3 where how current is affecting the frequency of the circuit is described. The term which is commonly used in frequency synthesizer to describe about its dynamic behaviour is given in section 2.4. The loop filter has been explained in section 2.5. The multi modulus divider has been explained in section 2.6 of the thesis.

Chapter 3 of the thesis explains about the analysis of the parameter and extraction of parameter from the response curve, it also explains about the various design parameters which can affect the dynamic response of the system. The section 3.2 described the key parameter of the frequency synthesizer which is very important during design and how it is depending upon the various part of frequency synthesizer.

The chapter 4 explains about the simulation results and discussions of the frequency synthesizer circuit. The section 4.2 discusses the effect of parallel shunt capacitor on the control voltage performance of the circuit

Finally the thesis has been concluded in chapter 5 where the scope for future work has also been specified

CHAPTER 2

FREQUENCY SYNTHESIZER

2.1 Introduction

The frequency synthesizer is a circuit which synthesize and generate clocks from given clock frequency. It uses the negative feedback to correct the phase and frequency error so that the recovered signal is free from this error. Frequency synthesizer is also used as frequency multiplier which multiplies by a factor to low frequency input F_{ref} to convert it into high frequency outputF_{out}.

The main objective of frequency synthesizer is to recover the signal without phase and frequency error and this process is completed after many iterations inside the system

The main component of the frequency synthesizer is

i) phase frequency detector

ii) charge pump

iii) low pass filter

iv) voltage controlled oscillator

v) multi-modulus divider

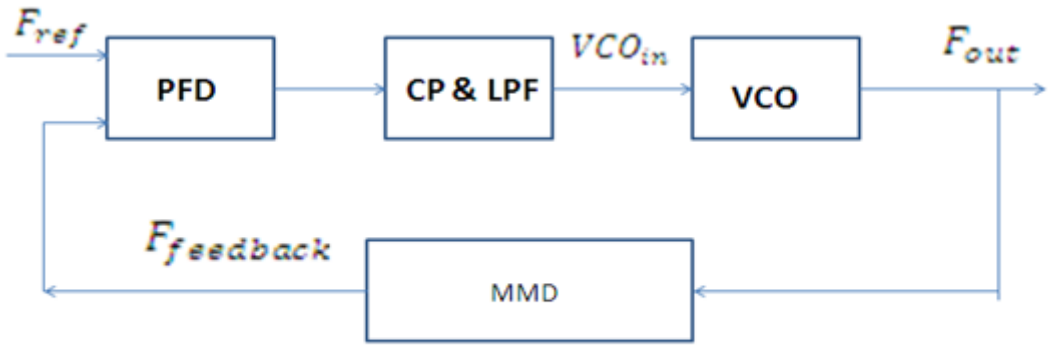

Figure 1: Frequency Synthesizer Block Diagram

2.2 Frequency Synthesizer Architecture

2.2.1 Phase frequency detector

The phase frequency detector [6-7] is a very first component of Frequency synthesizer whose work is to minimize the phase error introduces by the reference signal. The phase frequency detector has two inputs one is from the input of the Frequency synthesizer and other is from the output of divider circuit which divide the output frequency to bring it within the lock range to the reference frequency.it is used to minimize the phase as well as frequency error of the incoming signal.in phase frequency detector we generally used four type of phase frequency detector.

The Frequency synthesizer circuit contain five block phase frequency detector, charge pump, Loop filter, current starved VCO, Multi-modulus Divider

(A) Multiplier phase detector

(B) EXOR phase detector

(C) J-K flip-flop phase detector

(D) Phase frequency detector with voltage output

The selection of phase frequency detector is very important in the Frequency synthesizer circuit because the type of the PFD used in the circuit decide the error detection capability of the frequency synthesizer. In this section first we see all type of PFD and then we choose one of them

2.2.1.1 Multiplier phase detector

The multiplier phase detector [1] is mainly used for the linier input in the frequency synthesizer and provides a phase error at the output of the Phase detector circuit.

Basically the input to the Phase detector is a sine wave of zero phase error or with a constant phase error .suppose the two inputs is

$$S_1 = A_1 \sin(\omega_1 t + \theta_1) \quad 1$$

And second signal is

$$S_2 = A_2 \sin(\omega_2 t + \theta_2) \quad 2$$

Where ω is radian frequency and θ is phase of the signal .so when the two input is applied to the circuit the output is a signal with constant phase error

Suppose at some point of time when the radian frequency $\omega_1 = \omega_2$ then in that case phase error is

$$\varphi' = A_1 A_2 \sin(\theta_1 - \theta_2) \quad 3$$

So that the output value is dependent upon the phase error of the two signals .but the disadvantage of this type of PFD is that the phase detection process is very slow and it finally makes the whole circuit very slow. Another problem with this type of PFD is that due to ac input the output signal of the PFD is also AC and its average is zero so that so many times the VCO control voltage will also be zero and it does not acquire the lock state.

2.2.1.2 EXOR phase detector

The performance of the EXOR phase detector [1] is same as that of the multiplier phase detector for the linear input signal .the EXOR phase detector is normally used in the digital Frequency synthesizer and input to the EXOR phase detector is a digital pulse and in normal condition when the phase error between the two input signal is zero in that case the phase error between the two signal is out of phase by 90^0 .the phase error detection capability of the EXOR phase detector is in the range of $-90^o < \theta_e < 90^o$ .if any signal have phase error outside this range than in that case

the EXOR phase detector cannot detect the error. Another problem with this phase detector is that it is also very slow same like the multiplier phase detector whose pull in frequency is very slow. The acquisition of the signal can only be realized if the frequency difference is $\Delta\omega_p = \omega_1 - \omega_2'$ where $\Delta\omega_p$ is pull in frequency, ω_1 is the input frequency and ω_2' is the feedback frequency of the circuit

2.2.1.3 J-K flip-flop phase detector

The behaviour of J-K flip-flop phase detector [1] is same as that of the EXOR gate phase detector in the absence of clock in the flip-flop because in the absence of clock it changes its state with the change in the level of the input pulse. When the J-K flip-flop is clocked the transition in output is due to the change in the input level with the clock transition so that it can give the output with the unsymmetrical input pulse also and the maximum phase error obtained when the two input S_1 and S_2 are opposite to each other by 180^o phase. The output of the phase detector is mini mum when phase error obtained due to -180^o asymmetry and the maximum value at the output is obtained when the input has 180^o phase difference .from the above analysis we can say that the J-K flip-flop based phase detector is tracking the phase when it is in the range of $-\pi < \theta_e < \pi$.

2.2.1.4 Voltage Based phase Frequency Detector

The voltage based phase frequency detector [1,5] circuit has a very good option that the given circuit not only detect the phase error but it also detect the frequency error between the two incoming signal have any phase or frequency mismatch. The voltage based PFD is designed with the help of two D flip-flop in this case the output of the PFD is maximum when the input signals are 360^o apart or asymmetrical so the

tracking of the phase can be done in the range of phase error of $-2\pi < \theta_e < 2\pi$ and the pull in frequency is infinity

From the analysis of these four type of Phase frequency detector we see that the voltage based Phase frequency detector is best one because this PFD can detect the phase error in the range of $-2\pi < \theta_e < 2\pi$ so that if two incoming wave are 360^o asymmetrical then in that case also PFD will detect the error.

The voltage based phase frequency detector is a combination of two D latch with the combination of an AND gate in a way that the output of the two latch are connected to the input of the AND gate and the two data input are connected to the supply voltage or biasing voltage of the circuit .the clock input of the two D-latch are connected to the input frequency and the feedback frequency of the circuit. The output of the phase frequency detector is the phase error introduced due to the variation in the input frequency of the circuit .the main function of the PFD is to compare the two inputs and produced an output which is the resultant of the frequency mismatch which causes the phase error. Suppose that the A and B are the two D-latches whose input frequencies are ω_A and ω_B respectively then in that case if the input frequency ω_A is greater than the ω_B then in that case the output Q_A is high for the time in which the phase error is detected at the output and the case when the ω_A is less than the frequency ω_B than in that case the output at the terminal Q_B is high and produce the phase error. When both the input i.e. ω_A and ω_B are at the same frequency than in that case both the output are at high at the same time and these output are fed to the AND gate at its two input terminal, the output of the AND gate are fed to the RESET pin of the D-latch and both the latch are RESET simultaneously so that the output are RESET at the same time and produce no phase error at the output of PFD. From above description we can conclude that if $\omega_A > \omega_B$ in that case the phase error produced at the Q_A and fed to the charge pump which start conducting for the period of the pulse producing phase error and start charging the

capacitor of LPF .in the second case when the $\omega_A < \omega_B$ in that case the output at Q_B is high and it make N-MOS of the charge pump conducting and the voltage across the capacitor of loop filter decreases and the output frequency will reduces.

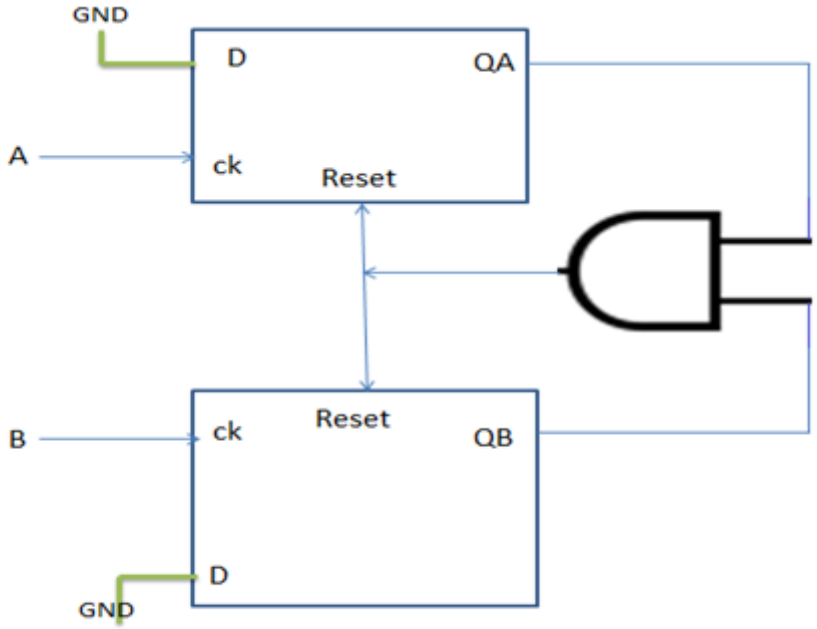

Figure 2: Block Diagram of phase frequency Detector [5]

2.2.2 CHARGE PUMP

Charge pump [1,5] of the frequency synthesizer is the part which connected at the output terminal of the phase frequency detector and the working of the charge pump depends upon the output of the PFD that send the phase error as input to the charge pump.

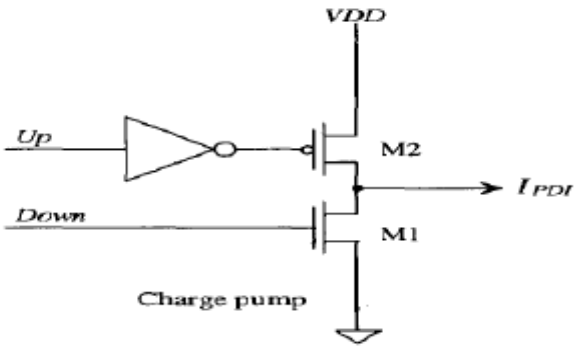

Figure3: Charge Pump

The working of the charge pump is that when the output Q_A is low then in that case the P-MOS will conduct and in the case when the PFD output Q_B is high in that case the N-MOS will conduct. The output current I_{PDI} of the charge pump must be insensitive to the voltage variation [8].

2.2.2.1 Calculation of phase error

If the PFD output Q_A is high for time Δt in that case the total phase error at the output of the PFD is [5]

$$\Delta\varphi = \frac{\Delta t}{T_{clock}}.2\pi\ (radians) \qquad 4$$

Where $\Delta\varphi$ is the phase error of the two input at PFD and the value of phase error are given in radians and the value of output voltage of charge pump is

$$V_{charge\ pump} = \frac{V_{DD} - 0}{4\pi}.\Delta\varphi = K_{cp}.\Delta\varphi \qquad 5$$

Where the gain of the charge pump is

$$K_{cp} = \frac{V_{DD}}{4\pi} \quad (6)$$

2.2.3 CURRENT STARVED VCO

The current starved VCO [3] is a simple ring oscillator with for number of stages in which the oscillation frequency is controlled by the help of current conduction through the circuit. The voltage controlled oscillator contain a cascade of inverter stage through which the voltage transfer from one stage to another stage of the circuit and finally feedback to the input terminal of the VCO so that oscillation in the circuit obtained because of transition time taken by the voltage to travel from input to output and finally feedback to the input terminal of the circuit. The design of CSVCO is done in the usual manner [3, 10, 11].

If the time taken by the voltage for the charging and discharging of load capacitor is τ then frequency of oscillation of the CSVCO is

$$f = \frac{1}{2N\tau} \quad (7)$$

Where N=no. of inverter stage

$$\tau = t_1 + t_2$$

The voltage propagation time period τ is a function of current so that if we are able to control the value of current in the circuit then we can control the frequency of oscillation also.in current starved voltage controlled ring oscillator P-MOS are always in the saturation region and with the help of control voltage V_{crtl} we are controlling the current through the N-MOS and finally controlling the frequency of oscillation.

The design of current starved VCO has the design procedure

1) Determine the total capacitor of the VCO

$$C_{tot} = C_{in} + C_{out}$$

$$C_{tot} = \frac{5}{2} C_{ox}\left(W_p L_p + W_n L_n\right) \quad (8)$$

2) Determine the charging and discharging time of the capacitor

$$t_1 = C_{tot}.\frac{V_{sp}}{I_D} \quad (9)$$

$$t_2 = C_{tot}.\frac{V_{DD} - V_{sp}}{I_D} \quad (10)$$

In this design the value of all current is taken equivalent so that

$$\tau = t_1 + t_2 = C_{tot}.\frac{V_{DD}}{I_D} \quad (11)$$

Then the oscillation frequency of the VCO of N stage is

$$f_{osc} = \frac{1}{N(t_1 + t_2)} = \frac{I_D}{C_{tot} V_{DD}} \quad (12)$$

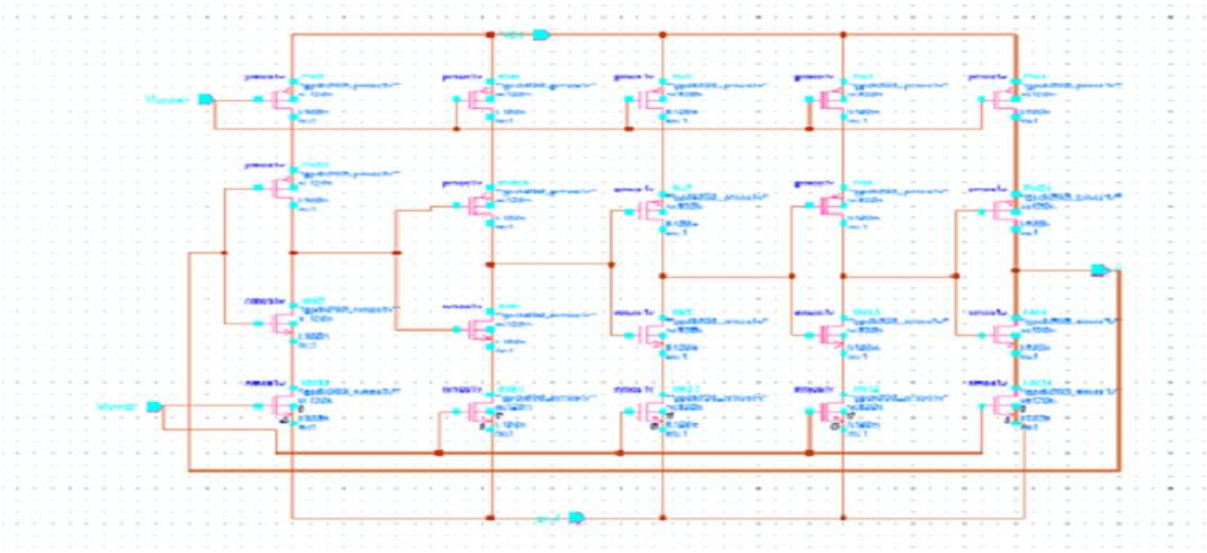

Figure4: Circuit Diagram of Current Starved VCO

In current starved VCO the PMOS M_P is always set in the saturation region and the controlling of current I_D is done with the help of control voltage V_{crtl} in the NMOSM_N. The

control voltage is used here as the gate voltage and the conduction of current follow the equation

$$I_D = K_n(V_{GS} - V_T)^2 \qquad 13$$

Where

$$K_n = \frac{\mu_n C_{ox}}{2}\frac{W}{L}$$

$V_T =$ Threshold voltage

The frequency of oscillation of the voltage controlled oscillator is directly proportional to the current through the circuit

2.2.4 LOOP FILTER

Loop filter of a frequency synthesizer is one of the most important component and it affect the dynamic characteristics of the frequency synthesizer like rise time, settling time ,peak overshoot, damping ratio, damping factor, bandwidth and noise performance of a Frequency synthesizer. In this part of the thesis first of all we see the dynamic parameter and its effect on the system. We are using here a passive phase lead-lag filter having one pole and one zero.

The transfer function of the given Frequency synthesizer is

$$H(s) = \frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)} \qquad 14$$

Where $\tau_1 = R_1 C$ and $\tau_2 = R_2 C$

In this given filter the $\tau_2 = R_2 C$ has strong influence on the damping ratio

2.2.5 Multi-Modulus Divider

The multi-modulus divider [23] is a programmable architecture of generic chain of N/N+1 divider in which one divider is connected to other in the cascaded manner so that every divider divides the output of the previous divider in a controlled way of division. The N/N+1 divider represent here as the 2/3 divider in which the same divider circuit divide the input either by 2 or by 3 depending upon the programmable input of the divider. The 2/3 divider circuit is the combination of four D-latch which are arranged by the combination of AND gate and NOT gate with them in which the input frequency is given to the clock point in each latch .The 2/3 divider contain two external pin P and M_i which is used to control the divide ratio of the divider. The two condition e ,one condition is that when the external input is set at zero means in this case P=0 and $M_i = 0$ then only the combination of two D-latch i.e. latch-1 and latch -2 will work and divide the input by 2 .

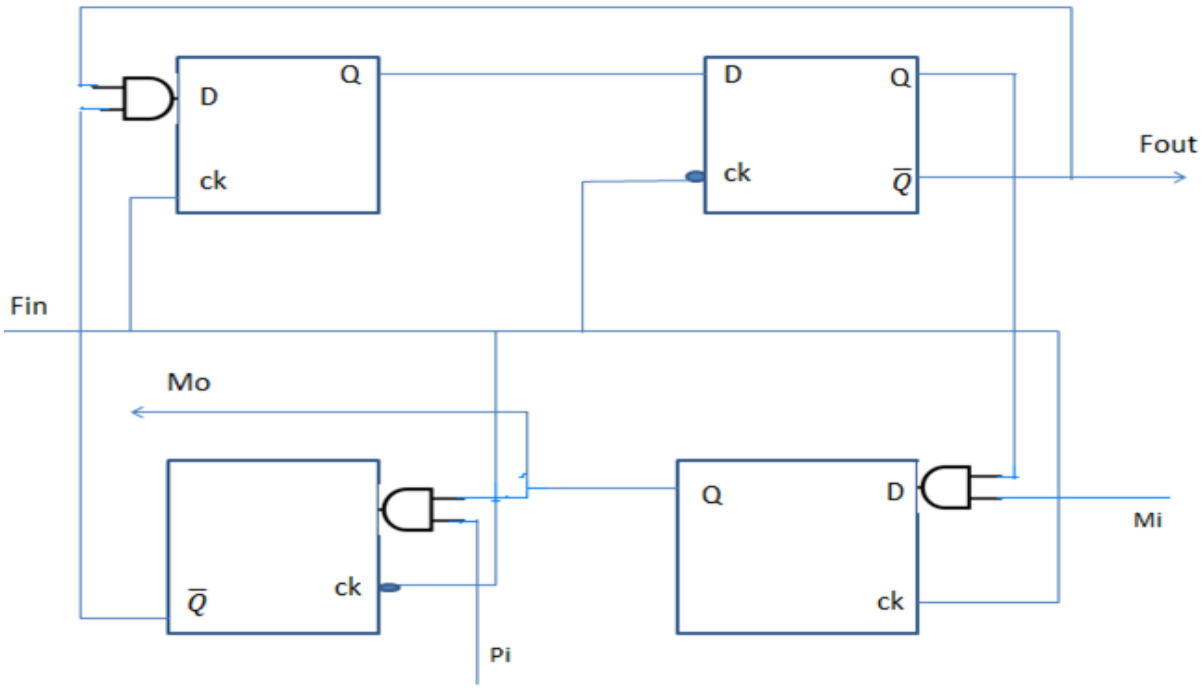

Figure5: Block Diagram of MMD

when the external control pin P=1 and M_i =1 the divider divide the input in the ratio of 3 .the process of division is that in the divide by 2 process, the output adds a cycle of time to the input but in the case of divide by three the divider divide the input once by three in a cycle means one extra cycle of frequency is added at the output.

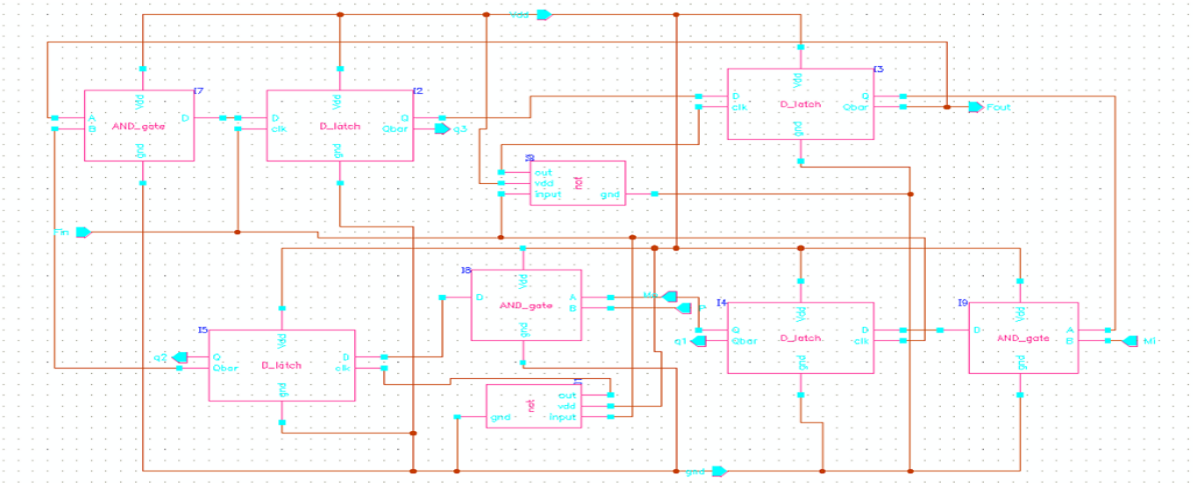

Figure6: Circuit Diagram of Current MMD

$$T_{out} = 2^n T_{in} + 2^{n-1} T_{in} P_{n-1} + 2^{n-2} T_{in} P_{n-2} + \cdots \ldots \ldots \ldots \ldots . \quad 15$$

$$T_{out} = (2^n + 2^{n-1} P_{n-1} + 2^{n-2} P_{n-2} + \cdots \ldots \ldots \ldots \ldots .) T_{in}$$

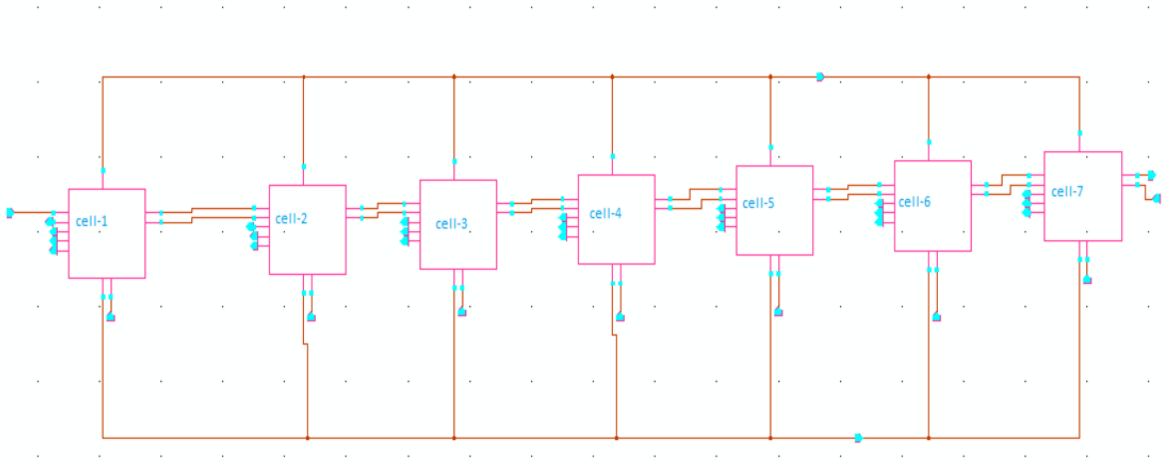

Figure7: Generic chain of MMD

To understand better the process of division we take an example of frequency input of 4GHz the time period is 0.25 ns and when the circuit divide the input in the ratio of 2 in that case the divider adds an extra cycle of time period to the input and it becomes 0.5 ns but the case when the divider divide the input by 3 in that case the divider adds one extra cycle of 0.25ns and the period of output frequency become 0.75ns. in this way the divider divide the input frequency .one another advantage of use of this circuit as divide circuit is that it reduce the hardware component to get a particular divide ratio .suppose that we have to divide the given input frequency by 82 then in that case the divide ratio of the circuit is in between $64 < 82 < 128$ so that if we are using the divide by two circuit we will require a total of 7 divider to get this divide ratio but the case if we are using a divide by three circuit then in that case it require total of 6 divider and the calculation can be completed by the eq.(1)

$$T_{out} = (2^6 + 2^{6-1} \times 0 + 2^{6-2} \times 1 + 2^{6-3} \times 0 + 2^{6-4} \times 0 + 2^{6-5} \times 1 + 2^{6-6} \times 0)T_{in}$$

$$T_{out} = (2^6 + 2^{6-2} \times 1 + +2^{6-5} \times 1)T_{in}$$

$$T_{out} = (64 + 16 + +2)T_{in}$$

$$T_{out} = 82T_{in}$$

So hat from above example we can say that the no. of divider required is 5

2.3 Noises in frequency synthesizer

The output of the practical system deviates from the desired response. This is because of the imperfections and noises in the system. The supply noise also affects the output noise of the frequency synthesizer system. There are mainly 4 types of noises. They are explained below.

2.3.1 Phase Noise

The phase noise is the very important parameter in the frequency synthesizer which is mostly affected by the random frequency variation and oscillator frequency stability. Oscillator noise, PFD and frequency divider circuit inside the Frequency synthesizer is the main cause of phase noise [12-15].

2.3.2 Jitter

A jitter is a variation of the reference signal with respect to ideal position in time [16-19] the jitter and phase noise is related to each other and by calculating one you can get the idea about other [18]. The jitter impacts the data transmission quality. The deviation of the signal from the ideal position can cause the increases in bit error rate (BER) of communication signal [19]

CHAPTER 3

DESIGN & ANALYSIS

3.1 Analysis of the frequency synthesizer System

In the Frequency synthesizer if we are taking each block as a separate component and transferring each component in the Laplace domain the we get a system which can be described mathematically the frequency synthesizer and analysis is easy and in the mathematical point of view it describe each and every parameter of the frequency synthesizer .since we are able to describe every parameter so controlling parameter is very easy

$$H(s) = \frac{\frac{K_0 K_d F(s)}{N}}{s + \frac{K_0 K_d F(s)}{N}} \qquad 16$$

If we are using the passive lead-lag filter then in that case the transfer function is

$$H(s) = \frac{\frac{K_0 K_d}{N}\frac{1 + s\tau_1}{\tau_1 + \tau_2}}{s^2 + s\frac{1 + \frac{K_0 K_d \tau_2}{N}}{\tau_1 + \tau_2} + \frac{\frac{K_0 K_d}{N}}{\tau_1 + \tau_2}} \qquad 17$$

From the equation of the second order closed loop system we get the value of characteristics equation as

$$C.E. = s^2 + 2\delta\omega_n + {\omega_n}^2 \qquad 18$$

Putting the value we get the value of damping ratio of the circuit

$$\delta = \frac{\omega_n}{2}\left(\tau_2 + \frac{N}{K_0 K_d}\right) \qquad 19$$

The natural frequency of oscillation is

$$\omega_n = \frac{K_0 K_d}{N(\tau_1 + \tau_2)} \qquad 20$$

3.2 Term in Frequency Synthesizer

3.2.1 Rise time

The rise time is the time taken by the output to reach from 10% to 90% of the final value of the output and it is controlled by the damping ratio of the low pass filter.

3.2.2 Peak overshoot

in the case of under damped system at the first instance when the transient overshoot occur over the settled value is known as the peak overshoot normally in the circuit the under damped system provide a fast output response but due to high peak overshoot it may damage the output response of the circuit so that the peak overshoot must be within some reasonable value. Since The damping ratio decide the peak overshoot of the circuit

$$M_p = e^{-\frac{\delta\pi}{\sqrt{1-\delta^2}}} \qquad 21$$

Where

M_p=peak overshoot

δ=damping ratio

3.2.3 Settling time

This is the total time taken by the circuit to reach at the steady state output response and it is related by the equation

$$t_s = \frac{3.2}{\delta\omega_n} \quad 0 < \delta < 0.69 \qquad 22$$

$$t_s = \frac{4.5\delta}{\omega_n} \qquad \delta > 0.69 \qquad 23$$

3.2.4 Bandwidth

the bandwidth of the frequency synthesizer is the range of frequency under which if any signal is coming at the input terminal of the circuit the circuit will produce the undistorted output in other words it reflect the reproducibility of the circuit

$$B.W. = \omega_n \sqrt{\left[(1 - 2\delta^2) + \sqrt{\delta^4 - 4\delta^2 + 2}\right]} \qquad 24$$

3.2.5 Noise performance

The noise performance of the frequency synthesizer is just inversely proportional to that bandwidth of the frequency synthesizer because if the bandwidth is higher, than the noise present over that bandwidth is also receipted by the frequency synthesizer and finally reduce the output signal to noise ratio

3.3 Key Parameter of the Frequency Synthesizer [1]

3.3.1 Lock range

This is the range of frequency for the locking of the frequency synthesizer. If any signal has the frequency in this range then it will lock to that frequency.

3.3.2 Lock time

The minimum time required for a frequency synthesizer to get locked is known as the lock in time .after this time the frequency synthesizer is locked permanently to the fix output frequency.

3.3.3 Pull-in time

This is the time required to pull in the signal in the fast locking state when the signal are locking or acquisition time is very slow .once the signal comes in the fast locking state then it will lock very fast. Generally pull-in process is slow.

3.3.4 Hold range

The lock range is the frequency range in which a frequency synthesizer is able to maintain lock statically. If a signal frequency is beyond the hold range frequency then the frequency synthesizer lost is locking permanently .the calculation of hold range is done at the point where the phase error is maximum. Since the maximum phase error can be obtained at different value of angle so that it is different for different PFD. The detection of phase error is decided by the PFD so the selection of PFD is very important for the hold range. In our circuit the phase detection capability is $-2\pi < \theta_e < 2\pi$ so that

$$\Delta\omega_H = \frac{K_0 K_d F(0) 2\pi}{N} \qquad 25$$

The value also depends upon the DC gain of the filter $F(0)$ but the value here is $F(0) = 1$

Lock range

$$\Delta\omega_L = 4\pi\delta\omega_n \qquad 26$$

3.3.5 Pull-in range

It is the range of frequency in which if the input signal is present then the frequency synthesizer can track and lock the signal very easily the pull-in range of the frequency synthesizer depends upon the PFD chosen so in the case when we are using the voltage based

phase frequency detector and passive lead-lag filter so in that case the theoretical gain of the loop-filter is infinity and in the same way the pull-in range is also infinity

$$\Delta\omega_L = \infty$$

3.3.6 Pull-in time

It is the time taken by signal in pull-in process so that it also depends upon the PFD and Loop filter

$$T_p = 2(\tau_1 + \tau_2)\ \ln\frac{1}{1-\left(\frac{2N\Delta\omega_0}{U_B K_0}\right)} \qquad 27$$

Where

$\frac{U_B}{2} = \frac{V_{DC^+} - V_{DC^-}}{2}$

3.3.7 Pull-out range

This is a frequency step which cause the a lock-out if applied to the reference frequency [1].the value of pull-out frequency range is in between lock range and pull-in range

$$\Delta\omega_{PO} = 11.55\omega_n(\delta + 0.5) \qquad 28$$

3.4 DESIGN SYNTHESIS & PARAMETER EXTRACTION

Calculation of various parameters in the circuit is done through the dynamic response of the control voltage which is actually an output of the second order closed loop system so that the calculation is done with this response. From the given figure we can see that the circuit is producing an overshoot at some point of time so that from that figure take the value of maximum over shoot and also calculate the peak time on which the maximum overshoot is

coming.by taking this two value calculate the value of damping ratio and natural frequency of oscillation .

$$M_p = e^{-\frac{\delta\pi}{\sqrt{1-\delta^2}}}$$

Now put the value of maximum overshoot and we get

$$max.overshoot = 659.2 - 600 = 59.2\,mV$$

The from the equation we get

$$59.2 = e^{-\frac{\delta\pi}{\sqrt{1-\delta^2}}} \times 100$$

$$e^{-\frac{\delta\pi}{\sqrt{1-\delta^2}}} = 0.09867$$

$$\frac{\delta\pi}{\sqrt{1-\delta^2}} = 2.316$$

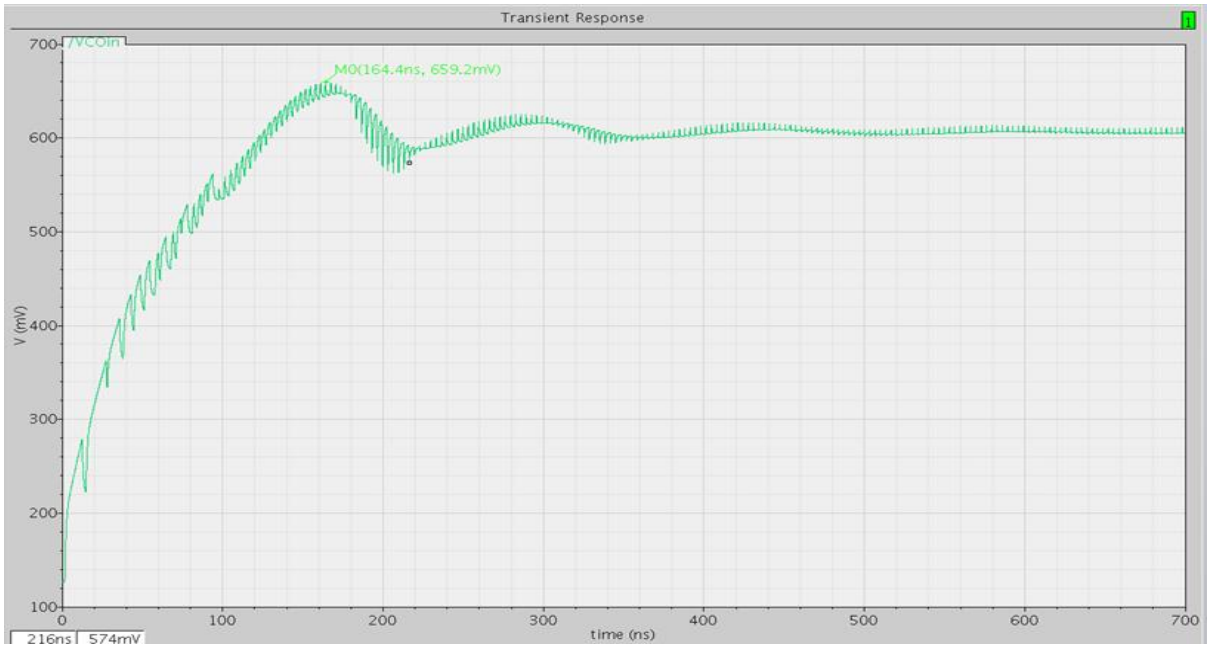

Figure 8: output of Loop filter

$$\frac{\delta^2}{1-\delta^2} = 0.5435$$

$$\delta^2 = 0.3521$$

$$\delta = 0.5934$$

For the closed loop system if the value of δ is in the range of $0.45 < \delta < 2$ then in that case the system perform properly and this circuit satisfying this condition.

The natural frequency of oscillation can be calculated with the help of peak time of the response so that

$$t_P = \frac{\pi}{\omega_n\sqrt{1-\delta^2}} \qquad 29$$

The peak time is in the graph is 164.4 ns so that

$$164.4\ ns = \frac{\pi}{\omega_n\sqrt{1-\delta^2}}$$

$$\omega_n\sqrt{1-\delta^2} = 19.11 \times 10^6\ rad$$

$$\omega_n = 23.74 \times 10^6\ rad$$

Now after getting the value of natural frequency and damping ratio we will calculate the value of bandwidth of the frequency synthesizer

3.5 Design Specifications

3.5.1 VCO Design Specification

The current starved VCO design Specification is given below

Table 1: VCO specification

Parameter	Value
Centre Frequency	4 GHz
No. of stage	5
Inverter Delay	25 ps
Supply Voltage	1.2 V

Table 2: VCO design parameter

Parameter	Value
Width of the PMOS	165nm
Width of the NMOS	120nm
$L_{PM} = L_{NM}$	100nm

Table 3: Frequency synthesizer specification

Parameter	Value
Reference frequency(F_{ref})	280 MHz
Output frequency(F_{out})	4 GHz
Bandwidth	20-30 MHz
Supply Voltage	1.2 V
Divide Ratio	10.5
Damping ratio	0.45-1.5
Lock-in time	200 -250 ns

CHAPTER 4

SIMULATION RESULT AND DISCUSION

4.1 Phase Frequency Detector

The phase frequency detector used here is the combination of NOR gate and the AND gate, the working of the PFD is when there are no input phase error both flip-flop will gives the output high which makes the PMOS and NMOS of the charge pump conduct and the AND gate RESET both flip-flop and VCO will run at constant frequency until the new phase error will detect. When the error detect due to high input frequency F_{in} the output of the flip-flop A is high makes the charge pump to charge the voltage across the loop filter capacitor and rise the output frequency of VCO. The error due to feedback frequency cause flip-flop B to rise to high and NMOS will conduct and discharge the capacitor and frequency will lower down

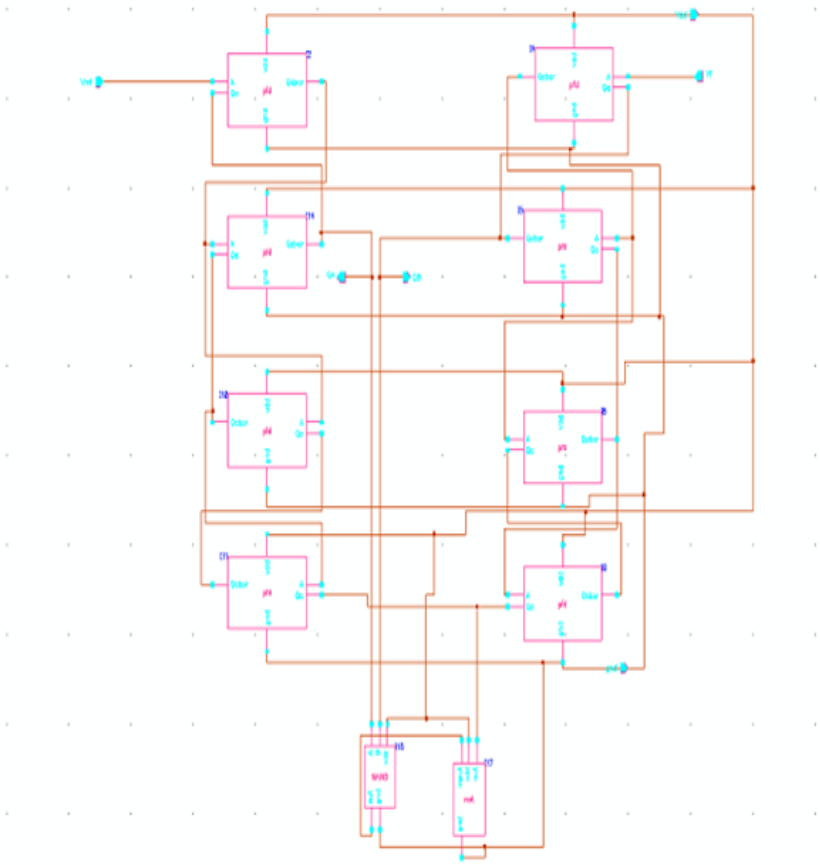

Figure 9: Circuit Diagram of PFD

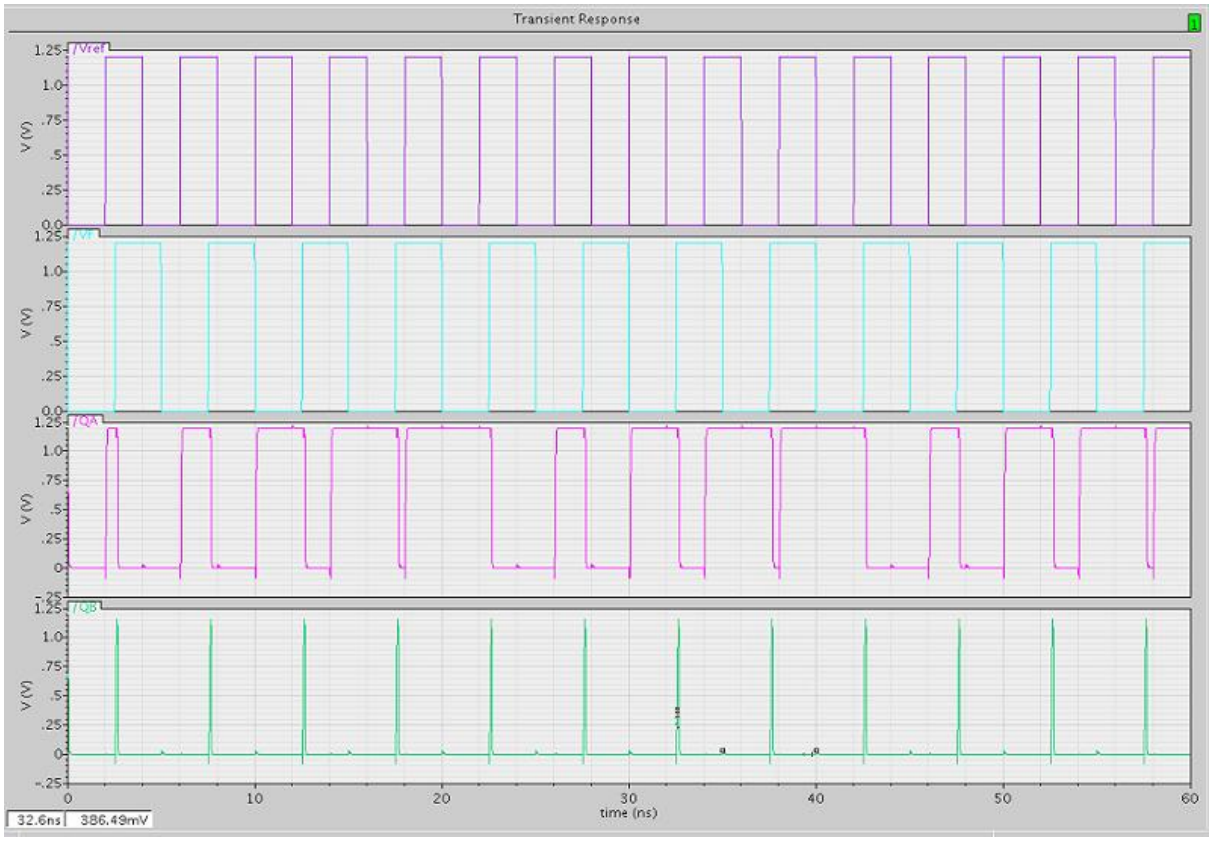

Figure 10: The output of PFD When the input F_in rising edge leads F_feedback Rising Edge

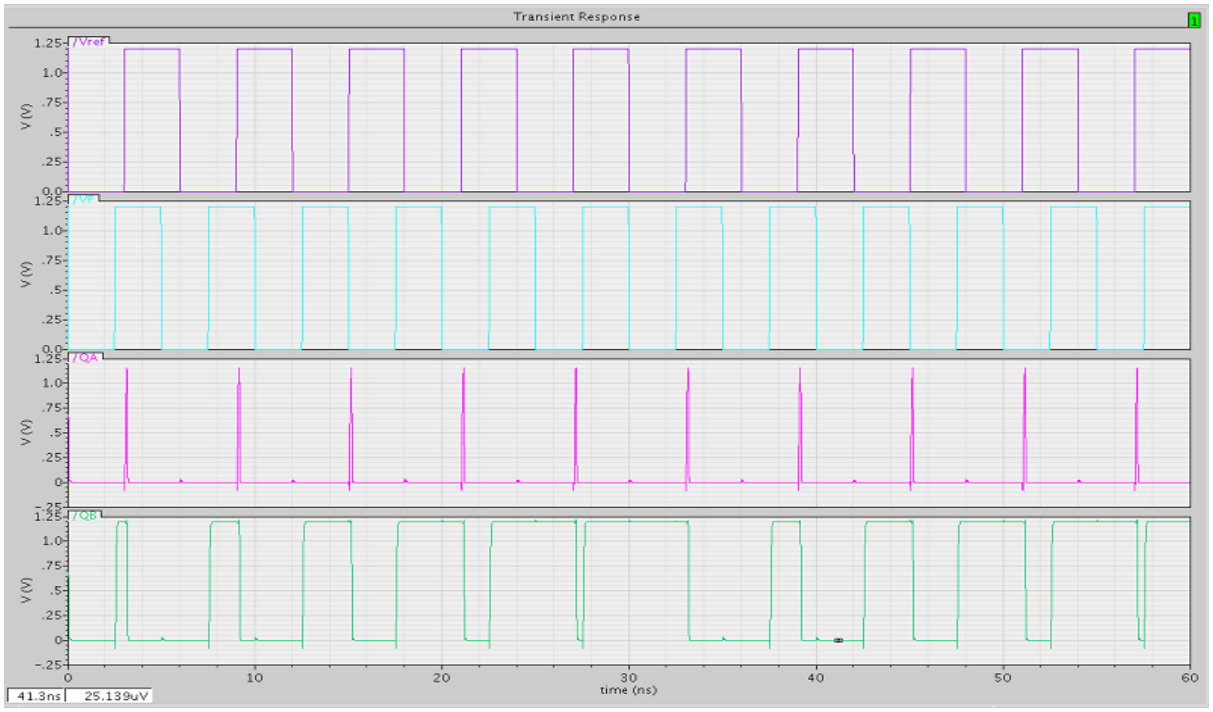

Figure 11: The output of PFD When the input F_feedback rising edge leads F_in Rising Edge

4.2 Loop Filter

Loop filter is a low pass filter which is connected at the output of the charge pump and it behave like integrators which convert the phase and frequency error in to equivalent voltage signal which finally drive the VCO for the frequency output. The output of loop filter is shown in the figure which describes the behaviour of the loop filter output with respect to the frequency of input as well as the feedback signal. The figure shows that when input frequency F_{in} is greater than in that case the UP node of the PFD is high and it start charging the capacitor of the loop filter. But in the case when feedback signals is high than the DOWN point is high and makes a path between output capacitor to the GND. The conducting path between capacitor and ground start discharging the capacitor to zero value potential.

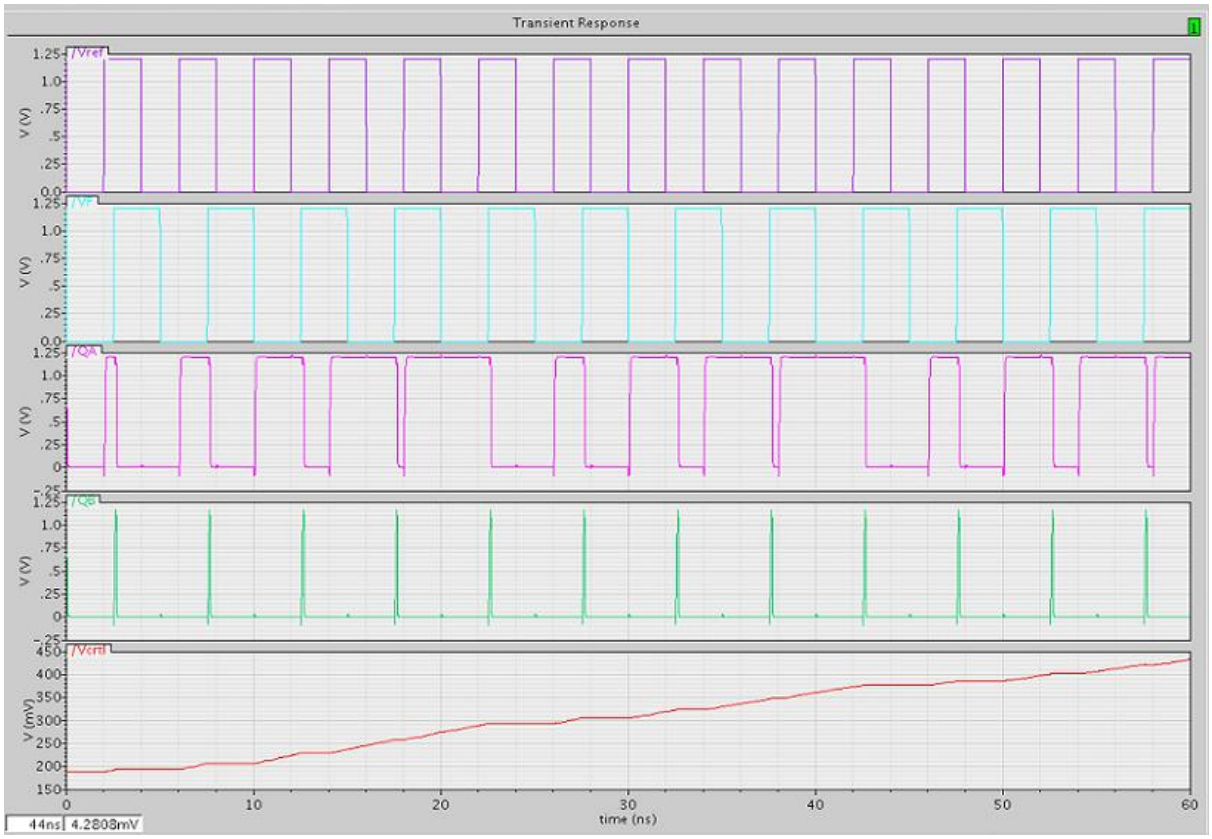

Figure 12: The output capacitor of loop filter is charging

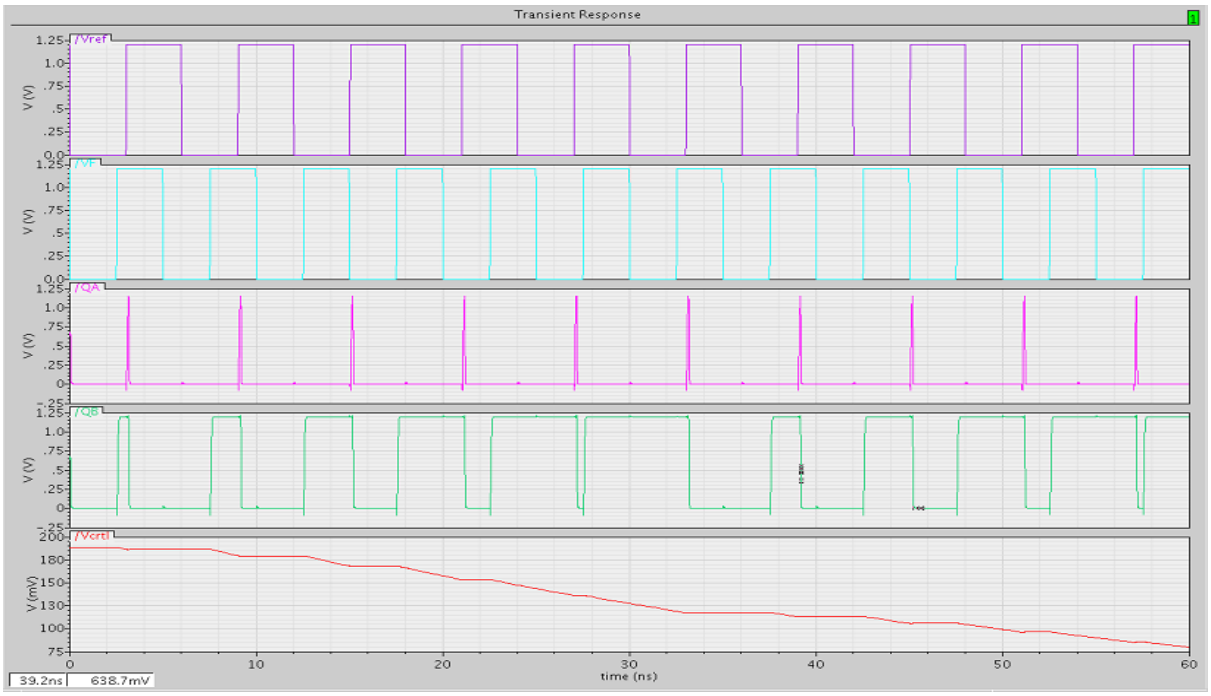

Figure 13: The output capacitor of loop filter is discharging

The charging and discharging of capacitor will control the output frequency.

4.3 Effect of shunt cap on Loop filter

Since the loop filter is very important part of the frequency synthesizer so the design of loop filter will decide the overall performance of the circuit. The loop filter with a capacitor and two resistors as given in the Fig 14 gives the output voltage across the capacitor which is distorted due to transient spikes in the waveform. The transient spikes in capacitor come because of the quick change of voltage across the capacitor. The distortion is removed by introducing a capacitor in parallel of the capacitor of loop filter. This capacitor removes the distortion introduced in the output. The Fig 15 show he output of modified filter and the distortion is removed because the introduction of capacitor gives sufficient time to the voltage to charge the capacitor of the loop filter. The output after modification is given in the Fig 15 and the value of parallel capacitor is 10 % of the filter capacitor.

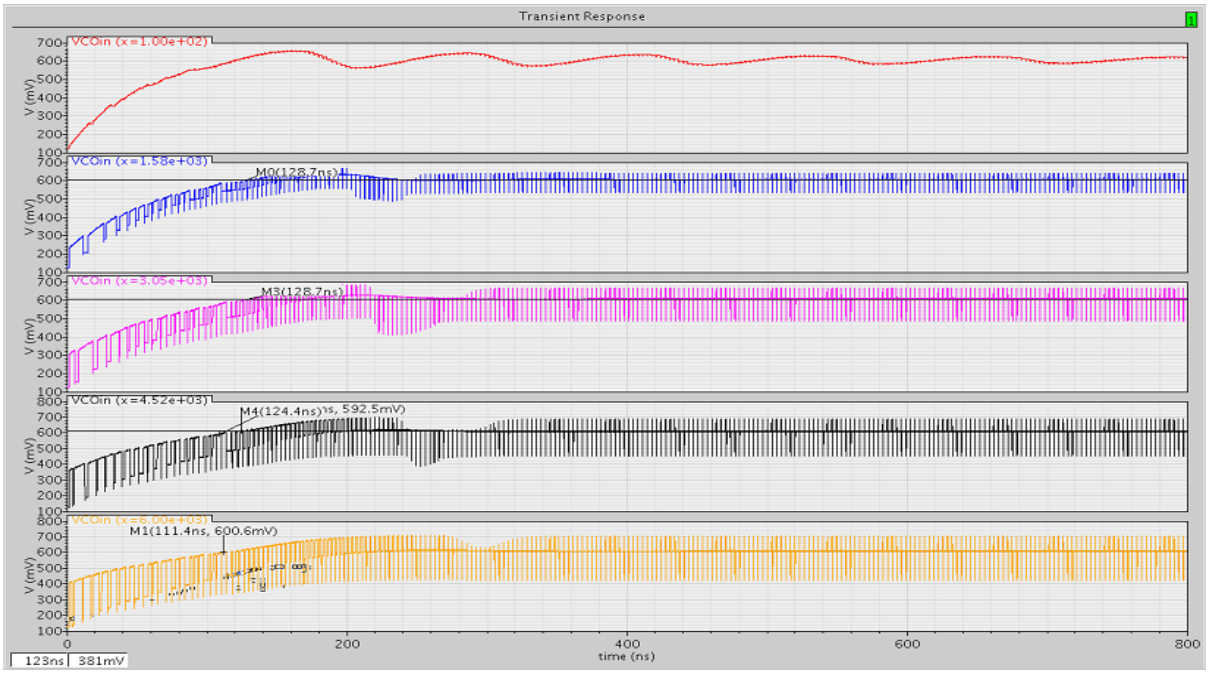

Figure 14: The output of loop filter without parallel capacitor

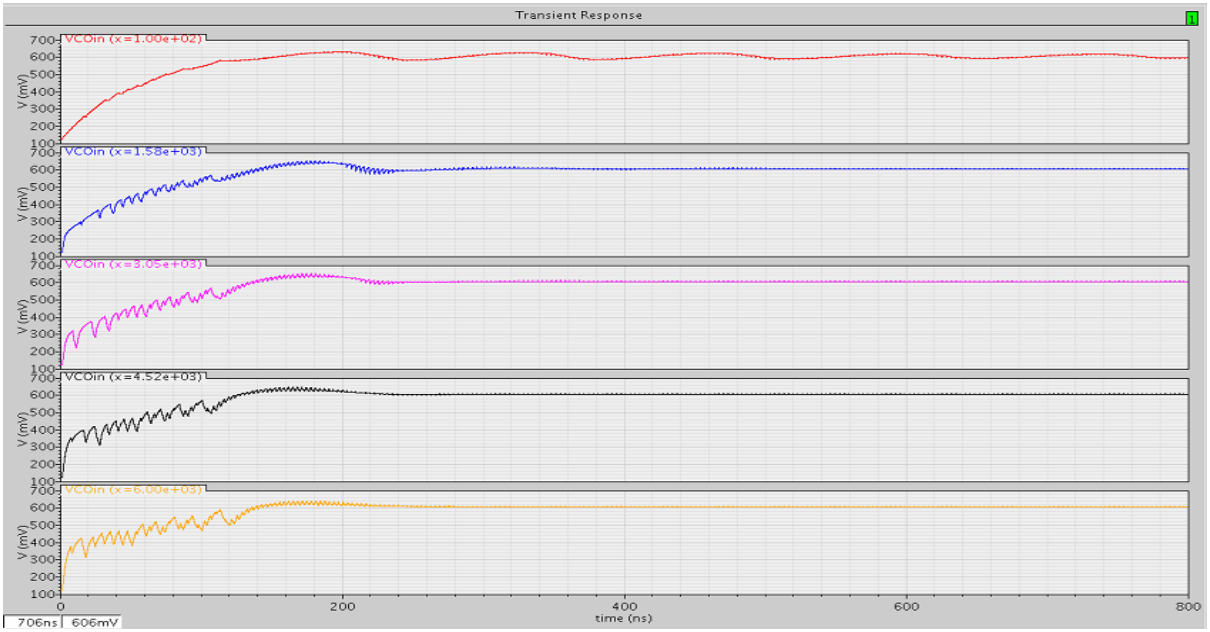

Figure 15: The output of loop filter with parallel capacitor

The introduction of capacitor stabilized the control voltage and reduced the rise time of the circuit because the introduction of capacitor is an introduction of open loop pole in the forward path of a closed system which is responsible for it

4.4 Voltage controlled oscillator

The voltage controlled oscillator is a 5 stage current starved voltage controlled oscillator that is oscillating at the frequency of 4GHz as the centre frequency. The centre frequency in this VCO is obtained at the controlled voltage of$\frac{V_{DD}}{2}$. The V_{DD} in this circuit 1.2 volt so the centre frequency is obtained at the controlled voltage of 600 mV

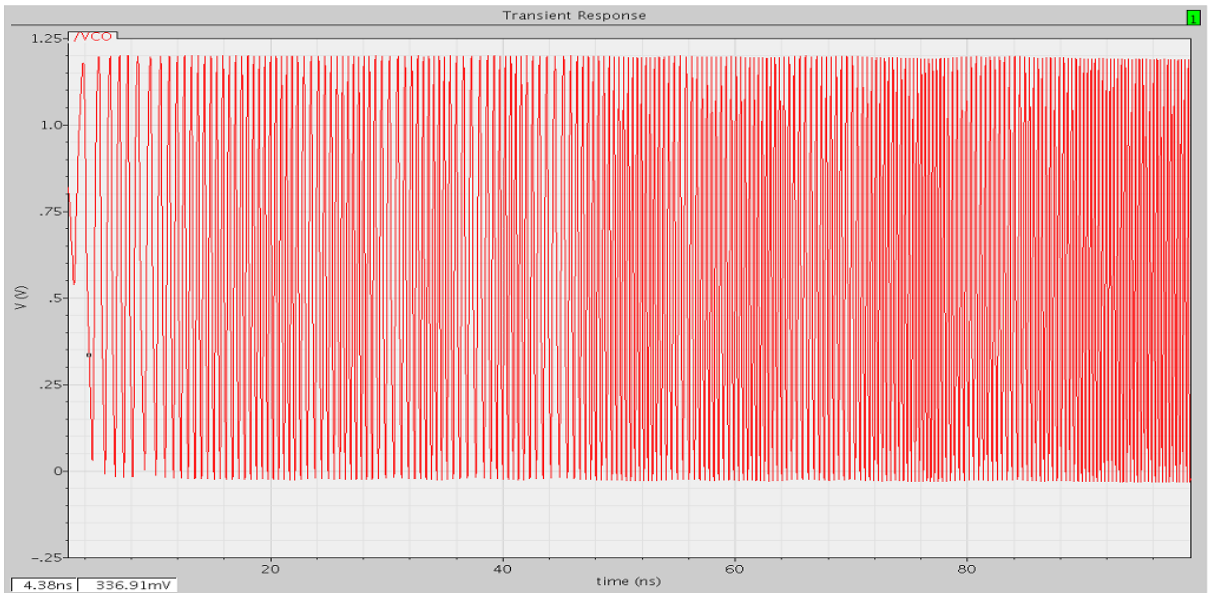

Figure 16: The output frequency of Ring Oscillator

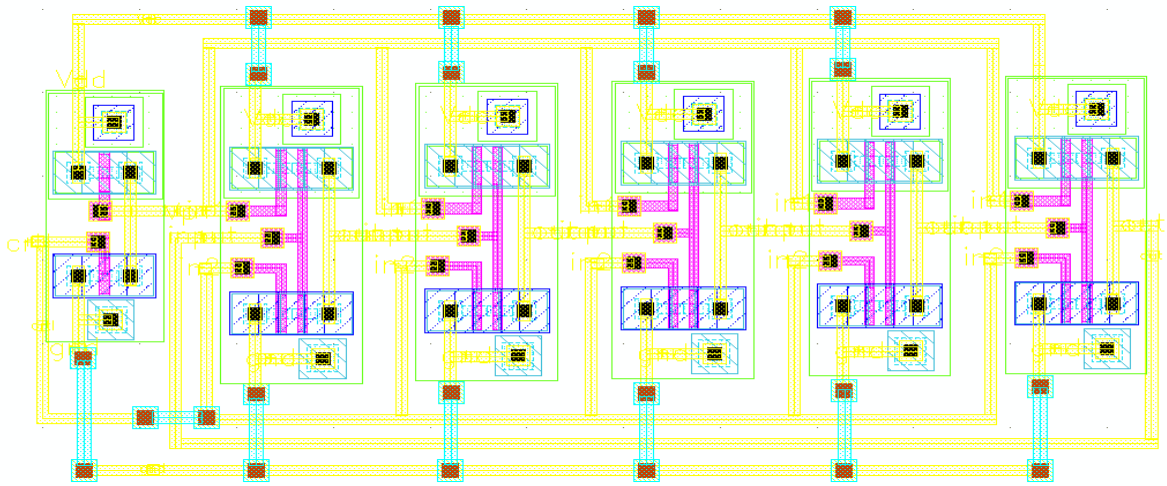

Figure 17: The Layout of the Current Starved VCO

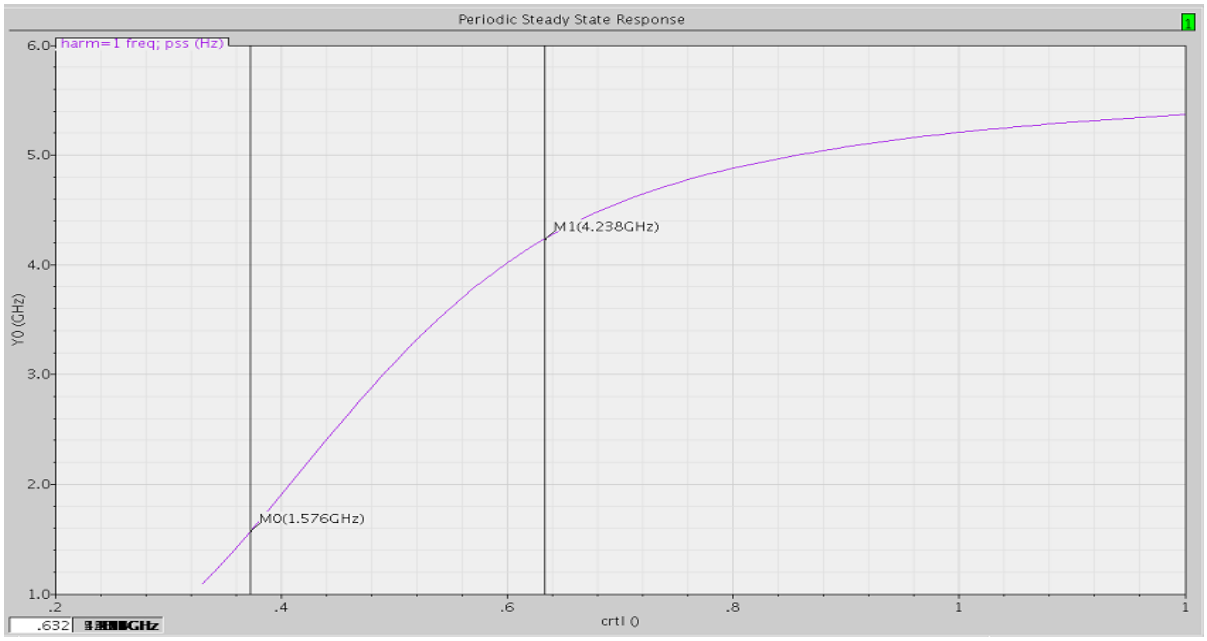

Figure 18: The output of PSS generated oscillator characteristics

The phase noise of the VCO is shown in the fig and its value is -76.7 dBc/HZ and it is shown in fig 19

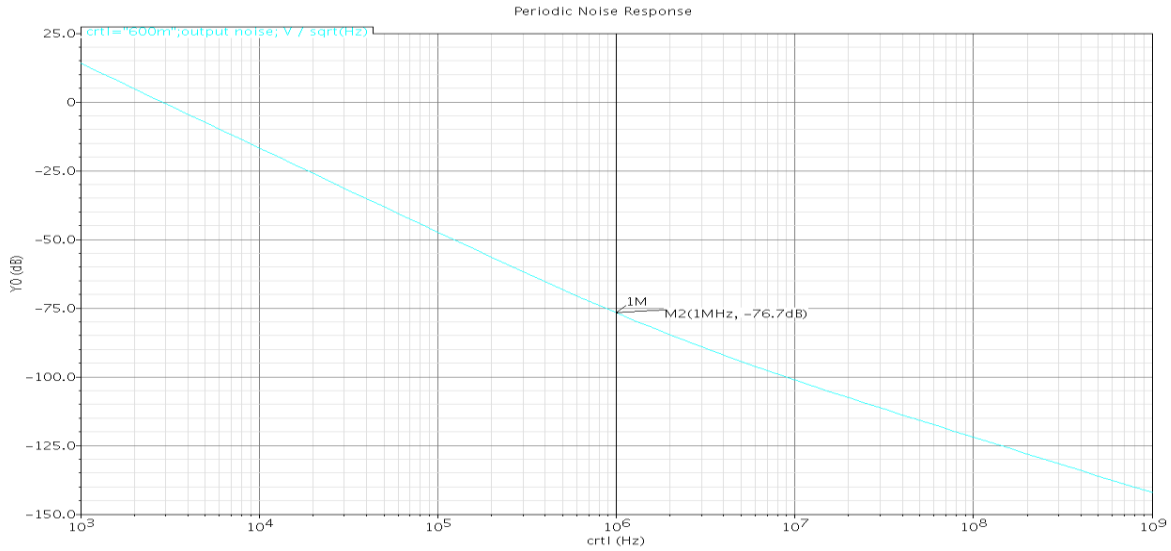

Figure 19: Phase Noise of the VCO

The ac gain of the VCO is very important parameter which is used to determine the transfer function of the circuit and we are seeing from the result that it is constant up to 10GHz of frequency

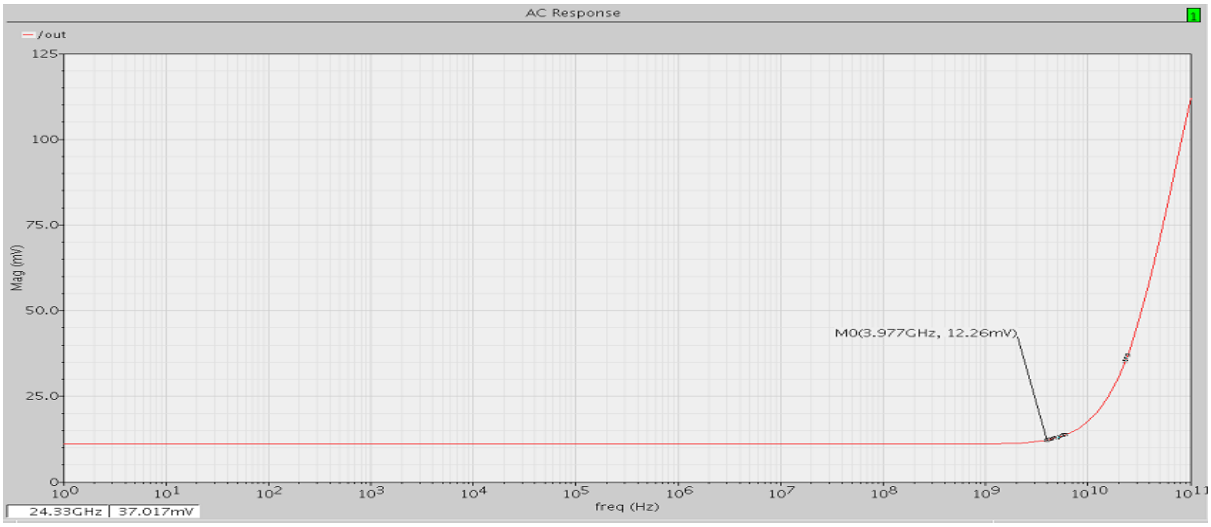

Figure 20: The small signal gain or ac signal gain of VCO

4.5 Multi-Modulus Divider

The multi-modulus divider is a programmable divider that is used in the design to divide the VCO frequency in N/N+1.

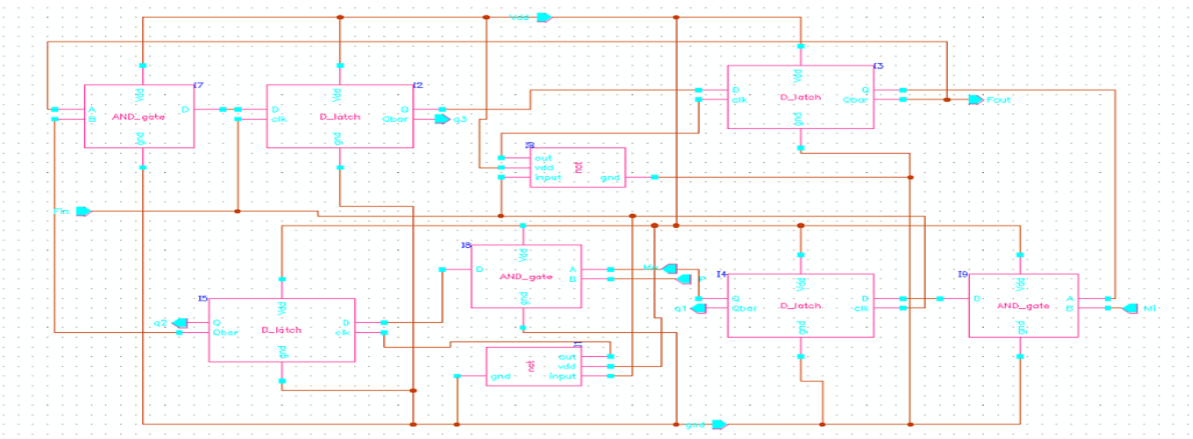

Figure 21: Circuit Diagram of MMD-Cell

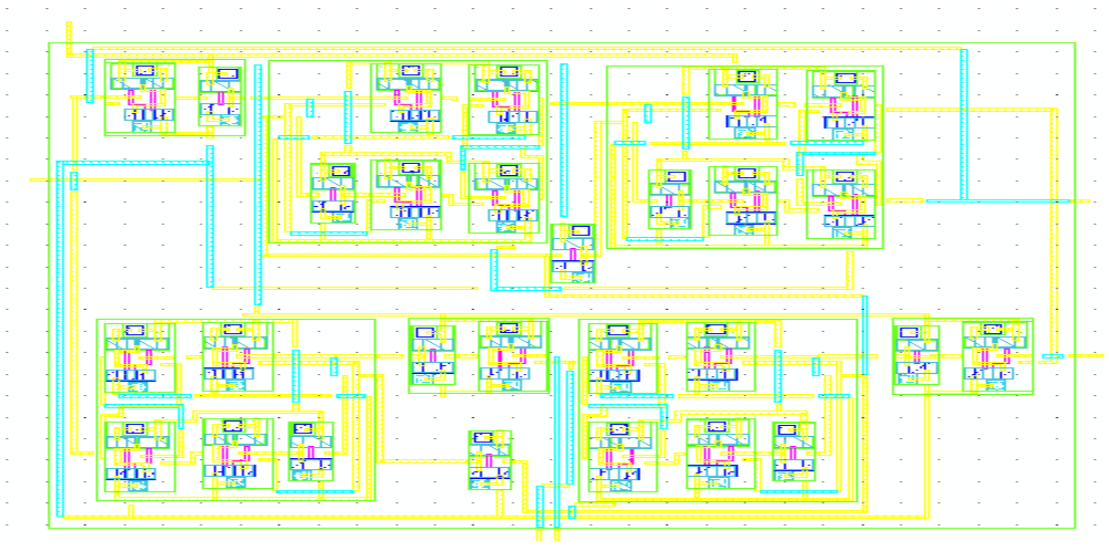

Figure 22: Layout of MMD Cell

The division ratio is controlled by a voltage pulse which provide a fixe divide ratio for a given duty cycle and divide the incoming signal in the range of 2 to 3 because in normal condition the divider is dividing in the divide ratio of 2/3 the circuit diagram of the multi modulus divider cell is given in fig 21and its Layout in fig 22.

The voltage pulse produces a certain divide ratio when we connect it to the terminal P of the MMD and simultaneously connecting the input pin M_i toV_{DD}. The divide ratio decided by this voltage pulse follow a pattern that is given in the fig 23

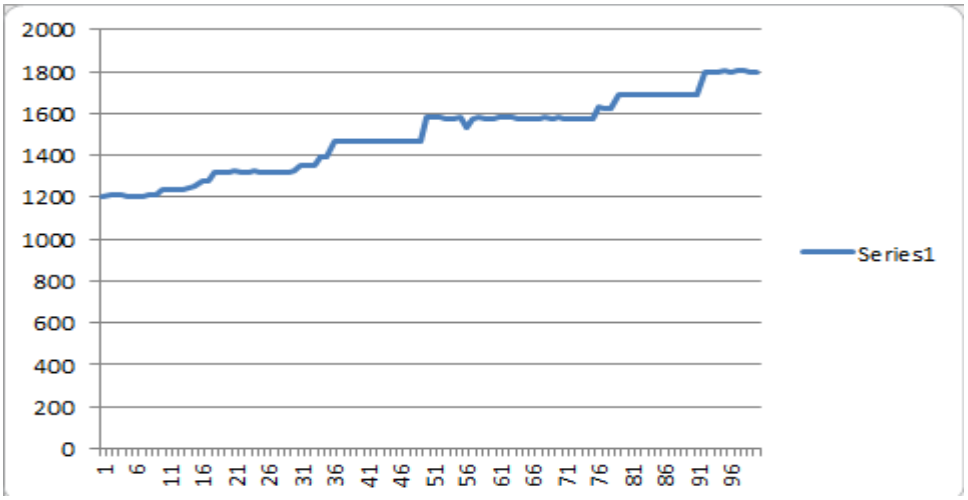

Figure 23: Pattern of division by Voltage Pulse

The division by a cell is done in either 2 or 3 and the it depends upon the pin P as well as M_i

When both the pin is at high then it divide by 3 and when both are at low it divide by 2

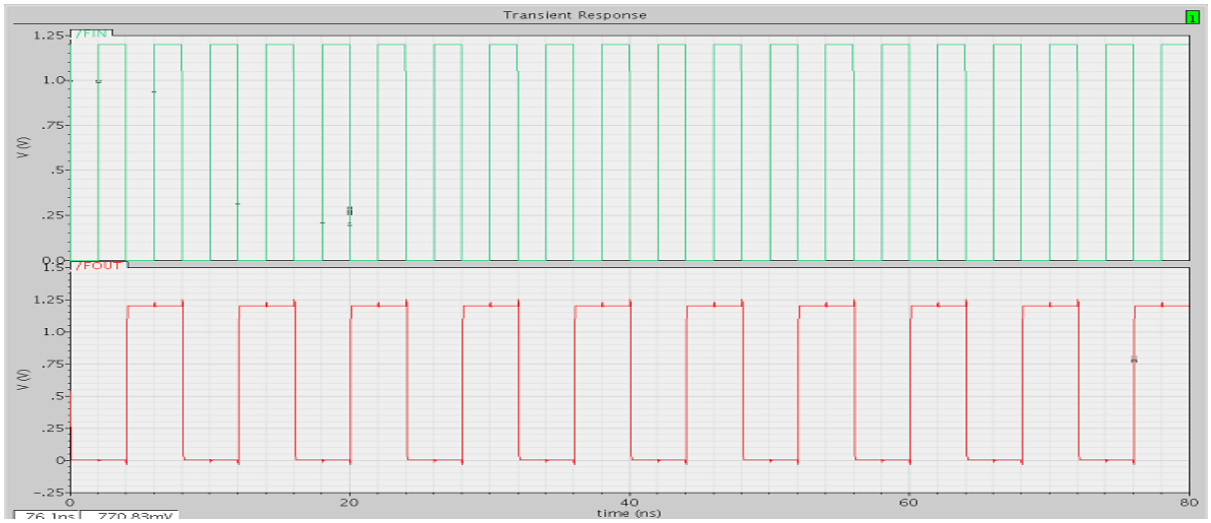

Figure 24: The MMD Cell Divide by 2 output

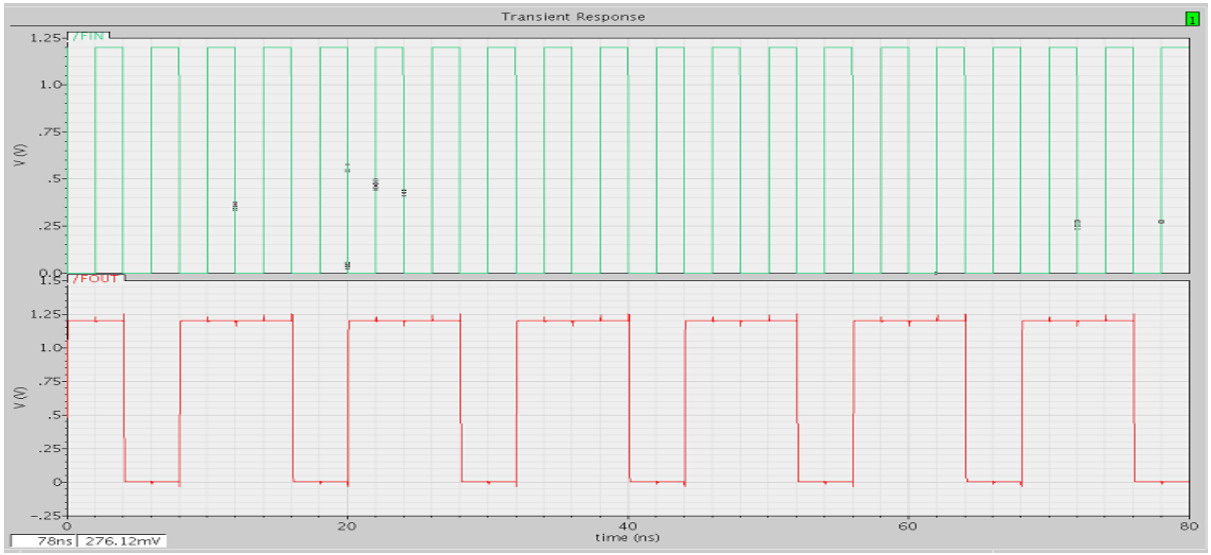

Figure 25: The MMD Cell Divide by 3 output

4.6 Frequency synthesizer

The Frequency synthesizer is a circuit whose output frequency is a function of the input control voltage of the CSVCO so that whenever the control voltage is constant then in that

case it produce a constant output .in this design of the circuit the control voltage is in the stable condition after 220ns so that the lock time is 220ns

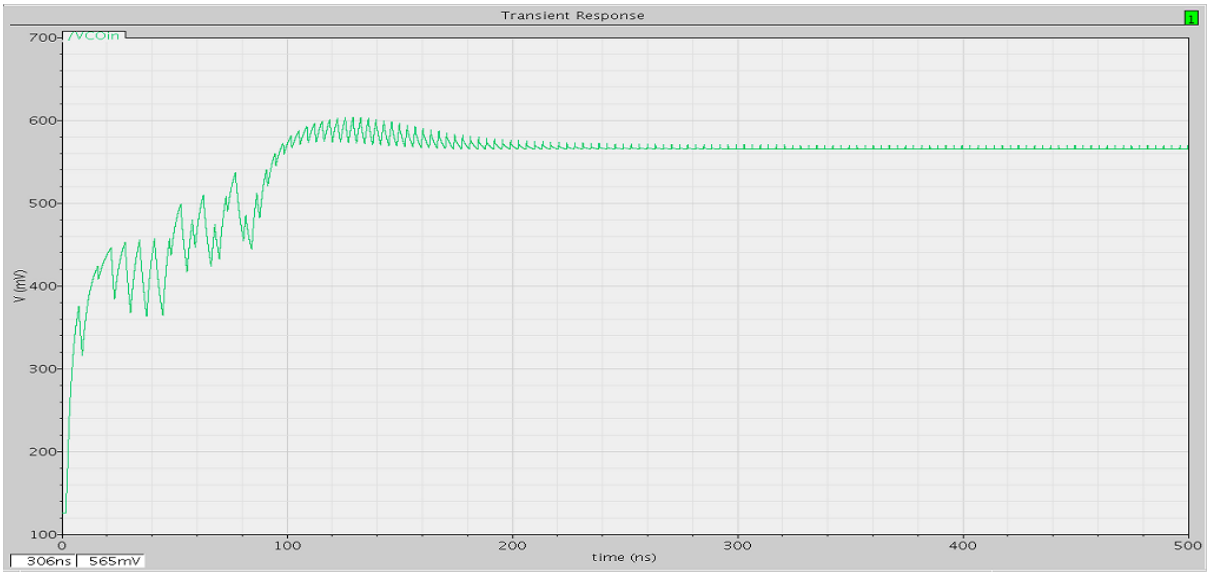

Figure 26: Control voltage of VCO

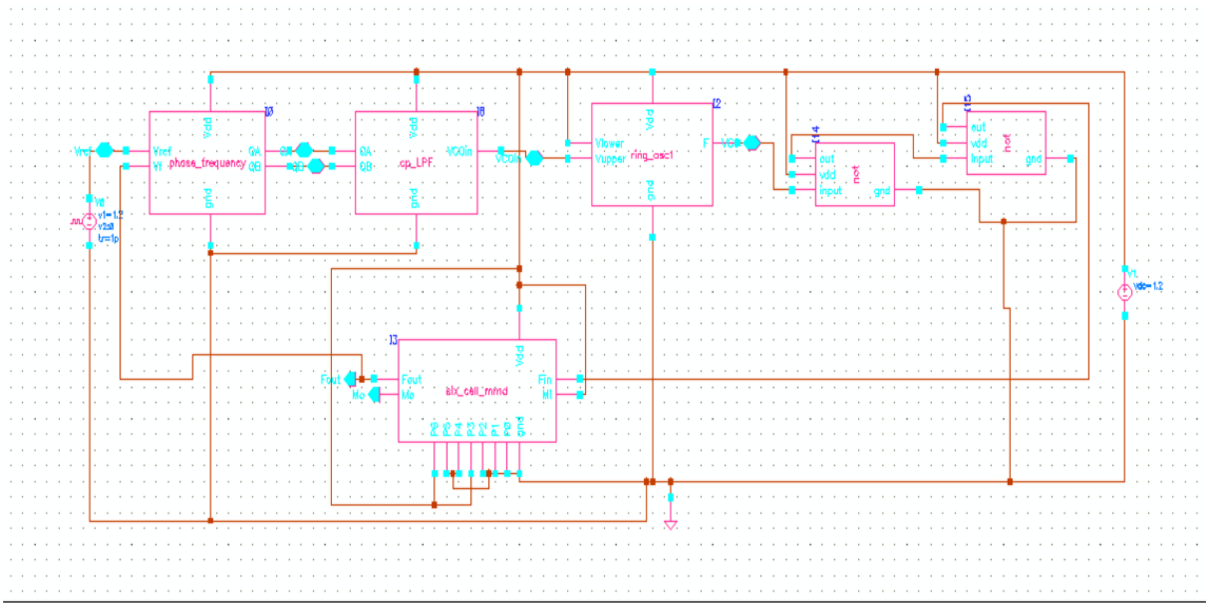

Figure 27: Circuit Diagram of frequency synthesizer

The frequency synthesizer has five major block and except this five block it also contain two inverter as the buffer which is used here to eliminate the loading effect on the CSVCO so that it the whole circuit will work in their respective manner

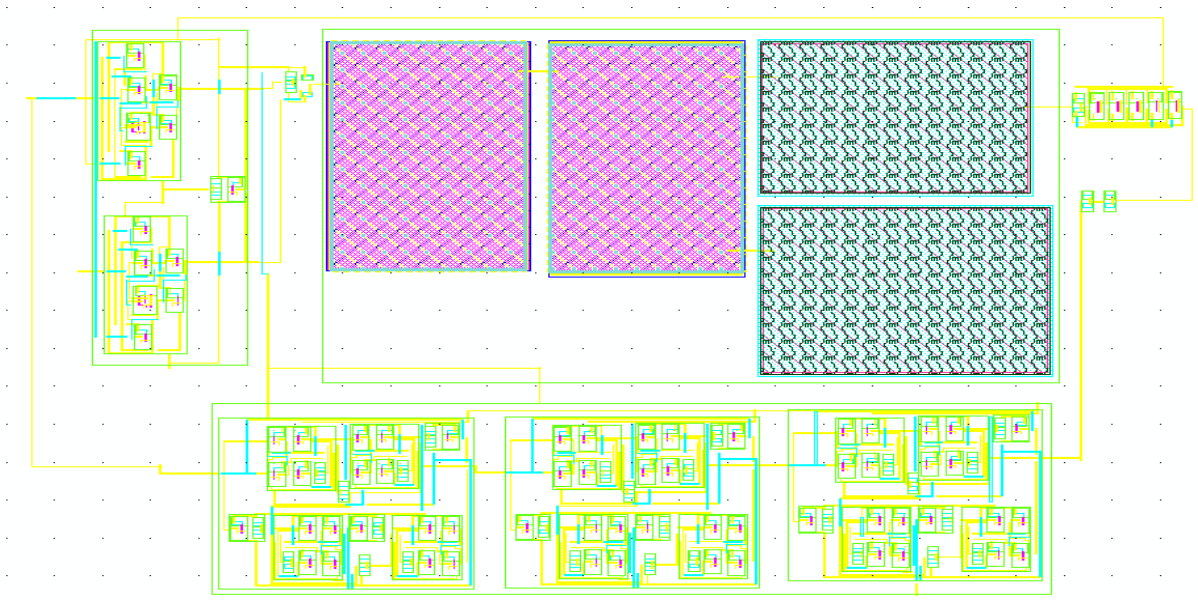

Figure 28: Lay-out of Frequency synthesizer

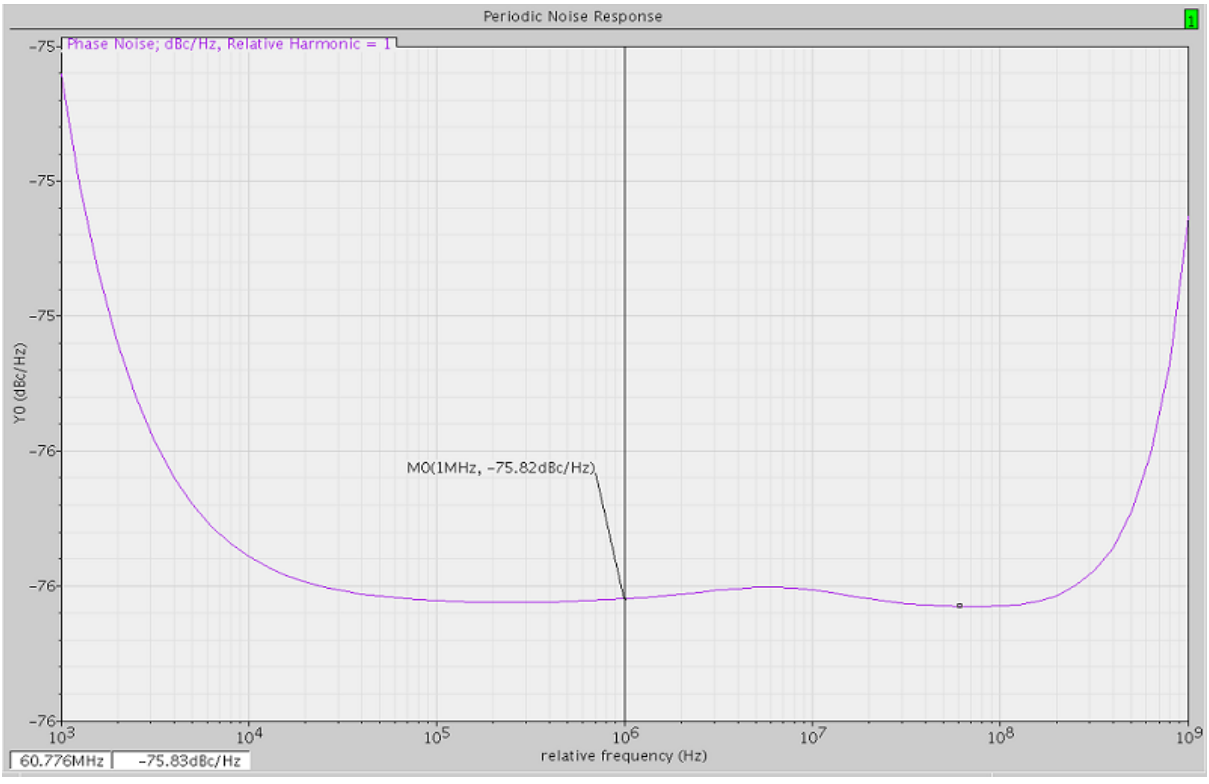

Figure 29: Phase noise of Frequency synthesizer

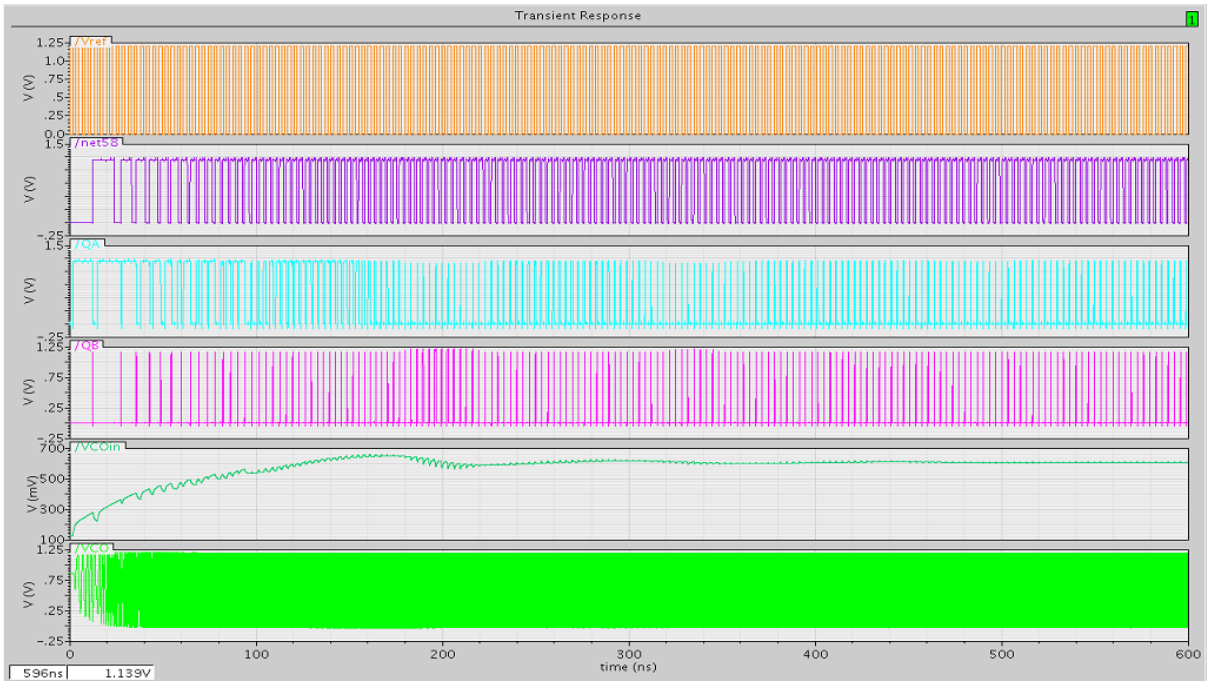

Figure 30: Output of Frequency synthesizer schematic level

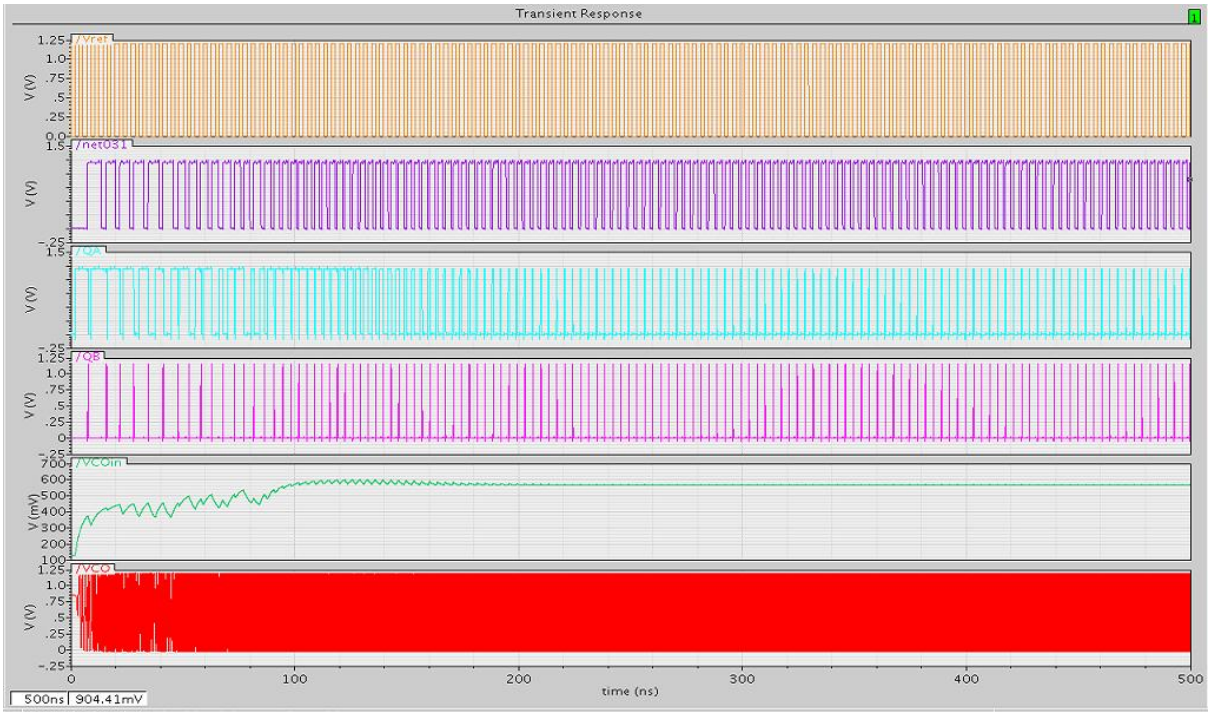

Figure 31: Output of Frequency synthesizer Layout level

The phase noise of the frequency synthesizer is -75dBc/Hz at the frequency of 1 MHz and the power consumption is 0.2091 m watt at the given centre frequency. From the given diagram

of power calculation we see that the power is constant at the time of 220ns so it can be the conclusion that output frequency is also constant at this time.

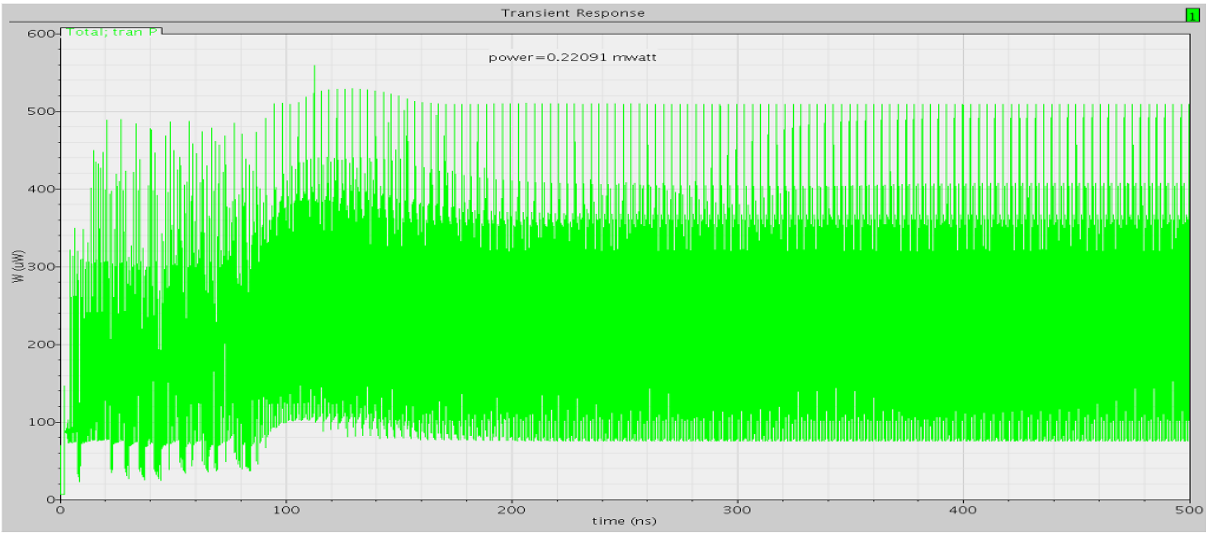

Figure 32: Power consumption in frequency synthesizer

The comparison of schematic level and post lay-out level result

Table 4: comparison of schematic and post lay-out result

parameter	Schematic level Result	Post –layout Result
Lock-in time	220ns	255ns
Power consumption	0.2091m watt	0.4032m watt
VCO Frequency	3.99901 GHz	3.95032 GHz
Natural frequency of frequency synthesizer	23.11 MHz	27.11 MHz
Bandwidth	5.93 MHz	3.98MHz
Pull-in time	∞	∞

CHAPTER 5

CONCLUSION AND FUTURE WORK

Conclusion & Future Work

1) The given frequency synthesizer is giving a lock in time is 220ns which is a better performance.
2) The power consumption of the frequency synthesizer is 0.209 m watt at 1.2 V power supply voltage.
3) The CSVCO frequency depends upon the current through the inverter and it is finally depending upon the size of transistor so proper value of transistor size will control the centre frequency of CSVCO
4) The loop filter is very important for dynamic behaviour of the frequency synthesizer therefore the selection of proper value of resistor and capacitor will decide the speed and behaviour of the frequency synthesizer circuit.
5) The phase frequency detector will decide the linearity and the pull-in range of the frequency synthesizer therefore the selection of PFD is very important in the design.
6) For fractional frequency divider the design of divider circuit is very important and it will decide the range of frequency which can be applied in the frequency synthesizer.

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