Realizing a Signature Verification System using Single Electron Transport Devices

A Project Thesis submitted for the partial fulfillment of the requirements for the degree of

Bachelor of Technology
in
Electrical Engineering

By

Anuja Singh
108EE003

Under Supervision of

Prof P.K. Sahu

Department of Electrical Engineering
National Institute of Technology, Rourkela
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DECLARATION

This is to certify that the work done in this Thesis Report entitled "Realizing a Signature Verification System using Single Electron Transport Devices" by Anuja Singh has been carried out under my supervision in partial fulfillment of the requirements for the degree of *Bachelor of Technology*, during session 2011-2012 in the department of Electrical Engineering, National Institute of Technology, NIT Rourkela, and this work has not been duplicated as far as my knowledge goes.

Place: Rourkela

Date: 7th May, 2012

Prof. P. K. Sahu

Department of Electrical Engineering

NIT Rourkela

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Further, I would like to thank all the administrative staff members of Department of Electrical Engineering for their humble cooperation and support. I would also take this opportunity to give thanks to all others who have helped us throughout my project and study at my institute.

Anuja Singh

(Roll No. 108EE003)

ABSTRACT

The need for developing faster systems is a trend today. Binary decision devices, working on the principle of single electrons are much faster and low time consuming. This paper aims at realizing a system of signature verification using single electron transistors. Single electron transistors can be used as binary decision devices to create logic gates, flip-flops etc. These logic circuit components will be employed to realize a signature verification system. The advantage of single electron transistor is its compact size and low power requirement. Also, single electron transistors have a much faster switching speed. Hence, SETs can be said to be the electronic equipments of the future. Their application in an offline signature verification device would help create a system that is fast, robust and low power consuming. Signature is an important tool to validate one's identity. This project would help in creating a device that would verify the authenticity of a signature using the SETs.

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CHAPTER I: Introduction

Signatures have been widely accepted as the behavioral biometric used to declare someone's identity. Many documents require a signature in order to be validated. Hence methods of auto signature verification techniques are required to be developed so that signature verification can be carried out at such a regular basis. Signature verification can be categorized on the basis of mode of data acquisition - On line and Off line. On-line data records the motion of the stylus while the signature is produced, and includes location, and possibly speed and direction, acceleration and pen pressure, as functions of time. Online systems use this information secured during acquisition. These dynamic characteristics are characteristic to each individual and sufficiently stable as well as repetitive. Off-line data is a 2 dimensional image of the signature. Processing Off-line is more complex due to the lack of stable dynamic characteristics. Difficulty also lies in the fact that it is hard to segment the signature strokes due to highly stylish and unconventional writing styles. The non-repetitive nature of discrepancies of the signatures, because of age, health, geographic location and perhaps at some level the emotional state of the person, aggravates the problem. All these reasons together cause large intra-personal variation. A robust system has to be designed that should not only be able to take into account these factors but also detect various types of forgeries.

We will be using single electron transistors to create a signature identification system. The single electron devices are promising candidates because of the unique principle of operation, quantized nature of carrier transport, high switching speed, ultra small size, and low power dissipation. The single electron transistors exploit the quantum effect of tunneling to control and measure the

movement of single electrons. The single electron transistors are so sensitive to charge that they can be used as extremely precise electrometers. The SETs can be used as binary decision devices. The electron will follow a particular path depending if the input given to it is a 0 or a 1.

However, these applications of the SET cannot be physically realized yet, because of certain constraints. The SETs which have been developed so far can only be operated at zero temperatures, and two identical SETs cannot be created.

CHAPTER II: Background and Literature Review

The Single Electron Transistors

Single electron transistors are based on the quantum tunneling of electrons. Given in the figure below is a schematic diagram of the SETs.

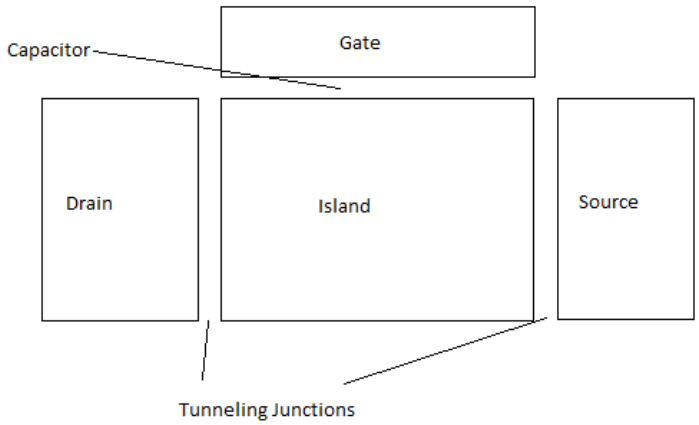


fig1: Schematic diagram showing main parts of an SET.

Working Principle

Let a small conductor, called an island, be initially electroneutral. There is no appreciable electric field beyond its border in this state, but it has a weak external force F, that may bring in an additional electron from outside. This is usually carried by tunneling through an energy barrier created by a thin insulating layer. Thus, the net charge of the island becomes -e, which creates an electric field E that repulses the following electrons that might be added. Even though charge e is very small, its corresponding electric field is quite large for sub nanostructures. If C is the capacitance of the island, then, in order to avoid thermally induced random temperature movements the following inequality should be satisfied:

$$e^2/C >> kT \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(1)$$

where, k is the Boltzmann constant.

Theoretical Background

Orthodox Theory

The orthodox theory has been a guiding principle for single electronics. It has been based on certain assumptions:

- The electron energy quantization inside the conductors is overlooked, i.e. the electron energy spectrum is treated as continuous. To be stringent, this assumption is valid only if $Ek << k_BT$, but it frequently gives an adequate description of observations as soon as $E_k << E_c$.

- The time τ_t of electron tunneling through the barrier is assumed to be negligibly small in comparison with other time scales (including the interval between neighboring tunneling events). This assumption is valid for tunnel barriers used in single-electron devices of practical interest, where $\tau_t \sim 10^{-15}$ s.

- Coherent quantum processes consisting of several simultaneous tunneling events ("*cotunneling*") are ignored. This assumption is valid if the resistance R of all the tunnel barriers of the system is much higher than the quantum unit of resistance R_Q:

$$R >> R_Q,\ R_Q = h/4e^2 \approx 6.5\ \text{k}\Omega \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ (2)$$

The latter relation is of principal importance for single-electronics as a whole.

Despite the limitations listed above, the orthodox theory is in quantitative agreement with almost all the experimental data for systems with metallic conductors (with their negligible values of the electron wavelength on the Fermi surface, λ_F) and gives at least a qualitative description of the majority results for most semiconductor structures (where the quantization effects are more noticeable, due to larger λ_F).

The main result of the theory can be put together as follows: the tunneling of a single electron through a specific tunnel barrier is always a random event, with a certain rate Γ (i.e. probability per unit time) which depends solely on the reduction ΔW of the free (electrostatic) energy of the system on account of this tunneling event. Within the orthodox theory this dependence may be articulated with a universal formula

$$\Gamma(\Delta W) = (1/-e)\, I(\Delta W/e)\, [1 - \exp\{-\Delta W/k_B T\}]^{-1}, \quad \text{(3)}$$

where $I(V)$ is the "seed" dc I-V curve of the tunnel barrier in the absence of single-electron charging effects. (In many cases, the Ohmic approximation $I(V) = V/R$ is quite acceptable.) ΔW may be readily found from the system's electrostatics.

Effects beyond Orthodox theory

Cotunneling- The essence of the effect is that the tunneling of several(N>1) electrons through different barriers at the same time is possible as a single coherent quantum-mechanical process. The rate of this process is crudely $(R_Q/R)^{N-1}$ times less than that for the single-electron tunneling described by Eq. (3) of the orthodox theory. If the condition expressed by Eq. (2) is satisfied, this ratio is rather small; cotunneling can nevertheless be clearly observed within the Coulomb blockade range where orthodox tunneling is suppressed.

Discrete Energy levels- For very small islands, the quantum splitting E_k between electron energy levels may become larger than E_c and $k_B T$ if the tunneling barriers are not extremely thin, i.e. their seed tunneling rate Γ_0 is not too large ($h\Gamma_0 < k_B T$),

$$\Gamma(\Delta W) = \Gamma_0 [1 + \exp\{-\Delta W/k_B T\}]^{-1} \quad \text{(4)}$$

Binary Decision Diagram

A BDD is a graphical representation suitable for large digital functions. BDD represents digital functions as directed acyclic graphs, with each node labeled as a variable. It provides a complete and concise representation for most digital functions encountered in logic design.

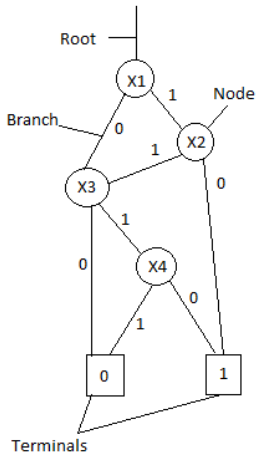


fig 2

The figure above shows the BDD for logic of $X1\overline{X2} + X3\overline{X4}$. Following a node, that branch is traversed that gives the correct value of the variable at the node. Following these branches, we reach the terminals BDD and obtain either 1 or 0 as the final value.

BDD Devices

A BDD is composed of many identical interconnected nodes. Hence, the node is a unit element of the BDD. These unit elements are called BDD devices. Each BDD device receives a messenger from a preceding device through the entry branch, and sends it to the next device through the exit branch corresponding to the binary value of the input.

Messenger- A messenger is a signal that travels through the path to reach the terminal value. The value of the signal is determined by observing which terminal the messenger reaches. Various media, like light or electrons can be used as messengers.

Advantage of BDD devices- In BDD devices, the messenger simply enters through one of the branch and doesn't need to drive the inputs of the other devices. This creates an advantage because, unlike in other traditional devices, a voltage level need not be maintained. Also, the messengers need not be electrical at all; they can be physical effects too. Such physical effects are useless for the transistor type devices.

SETs as BDD Devices

It is possible for the BDD to use a single electron as a messenger. If the BDD is implemented by using single electron circuits, then an electron travels along the path and reaches either a 0 or 1 terminal; the value of the digital function is determined by observing which terminal the electron reaches.

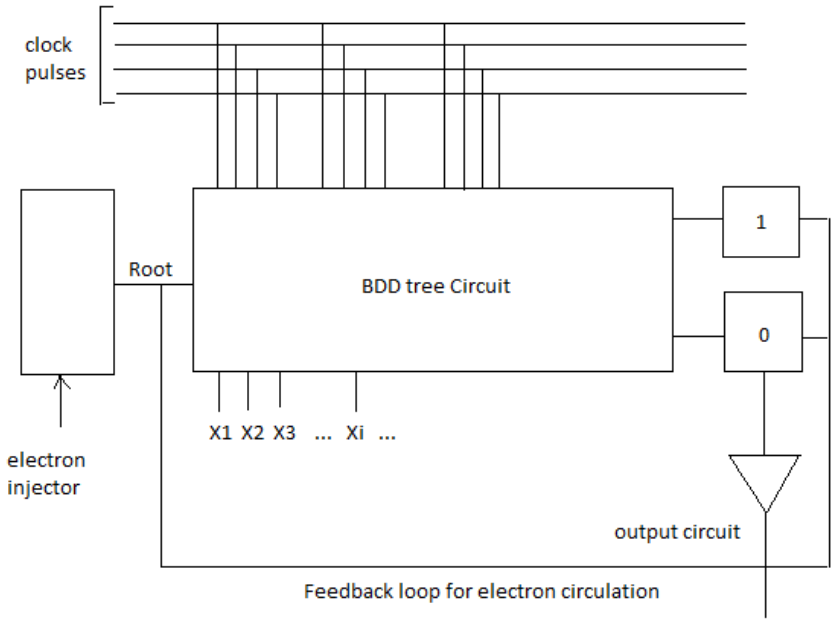


fig 3: BDD Circuit Block

Given above is a schematic view of a BDD circuit block, consisting of a BDD tree circuit, an output circuit, and an electron injector.

The BDD circuit is constructed of a number of unit devices, which is driven by clock pulses and accepts variable inputs (X1, X2,…)

The output circuit detects the arrival of the messenger electron at the 0 or 1 terminals of the BDD circuit and produces the corresponding binary output signal.

The electron injector supplies a messenger electron into the root of the BDD circuit.

Signature Verification System

A handwritten signature as a behavioral biometric is the mean accepted method to declare someone's identity. Signature Verification systems are used by corporations to identify customers, courts to establish identities etc. There are two ways to process a signature sample. The first is where the image is captured directly as handwriting trajectory, and the second is in which digitisers are used in order to acquire a digital image. We will be utilizing the second process of image generation. Contour coding is done on the signature sample and local features such as discontinuities, tangents, end points, curvatures are obtained. These information are compared to the already present signature information, and the verification of signature is done.

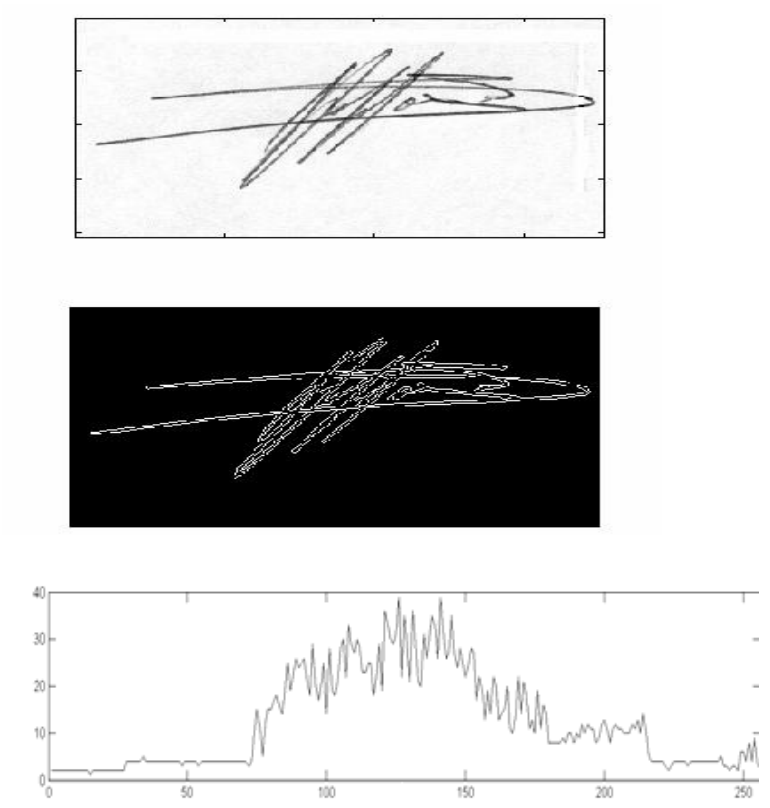


Figure 4: a) Original image. b) The final binary image. c) Corresponding projection of the binary image. The vertical axis corresponds to the number of white pixels of each abscissa.

CHAPTER III: METHODOLOGY

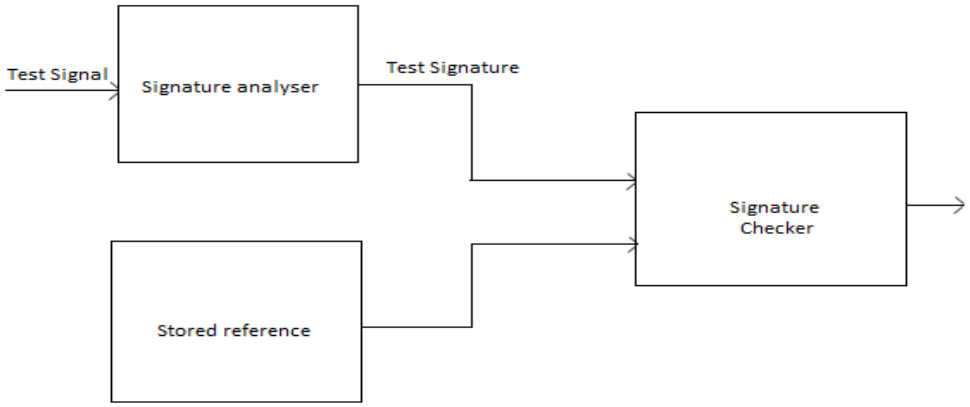


Fig 5: Block level diagram of a Signature Identification System

A compact, low power consuming signature Identification system has to be designed, based on logic gates, that will be used in the system.

Signature analyser- Converts a RGB (coloured) image into a grayscale image and then from grayscale to a binary image. The binary image is then converted to a matrix.

Stored reference- Has the matrix of the original signature stored.

Signature checker- This is basically logic gates used to compare the signature sample fed and the already existing sample of signature.

The conventional signature verification system

The conventional signature verification systems using C-MOS is developed using the EX-OR gate and the D-Flip Flop.

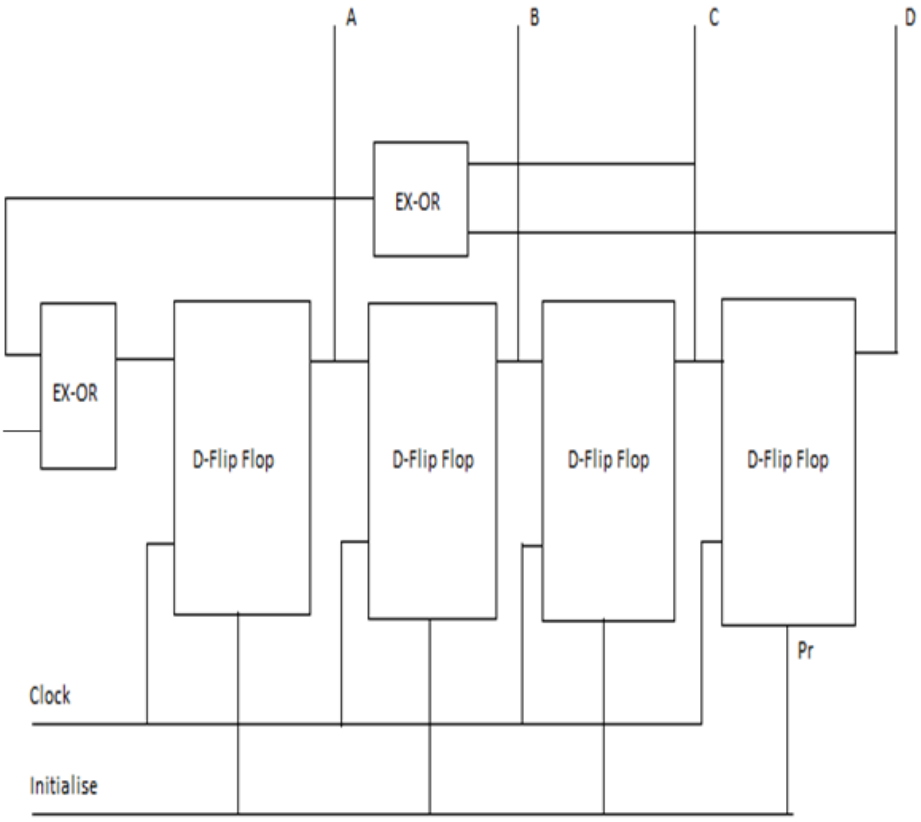


Fig 6- Logic Diagram of Conventional Signature Verification System

Hardware Implementation

Since SETs have not been developed as yet that could function at room temperature, the hardware implementation of the circuit has been done using conventional logic gates.

The ICs used for the implementation are 7474 Dual D-Flipflop and 7486 Quad 2-input Xor Gate

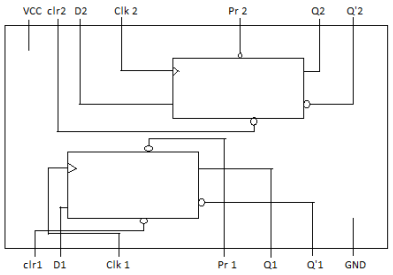


Fig7 :- 7474 Dual D- Flipflops

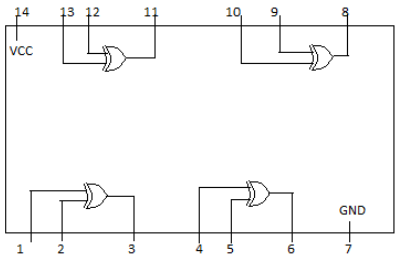


Fig 8:- IC 7486 Quad 2-input XOR gates

The signature inverted binary image should be burned onto a hardware and converted to voltage levels. The voltage form is then given as input. The output of the signature is compared with the output of the stored reference and decision is taken.

Image Inversion

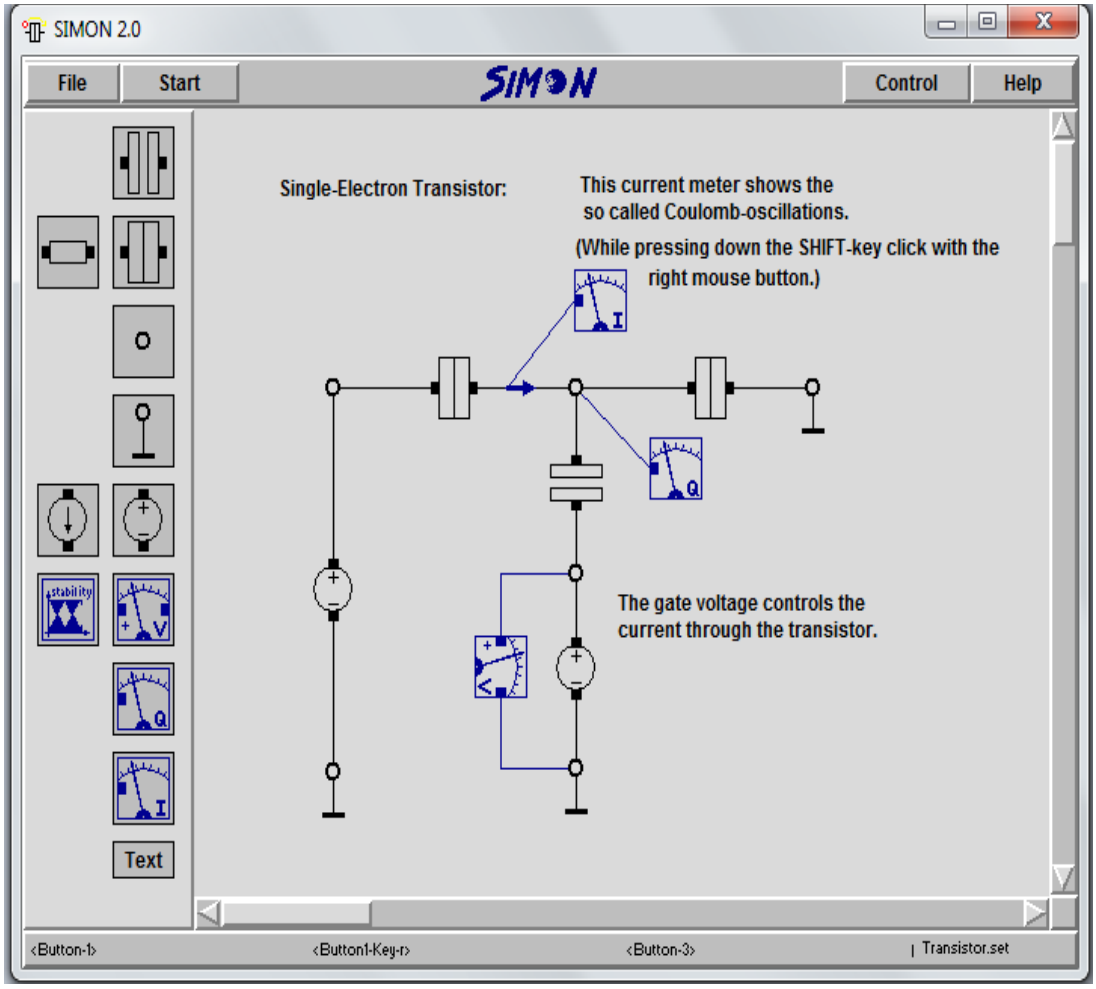
Matlab programming has been used to convert an RGB imaged to an inverted black and white image.

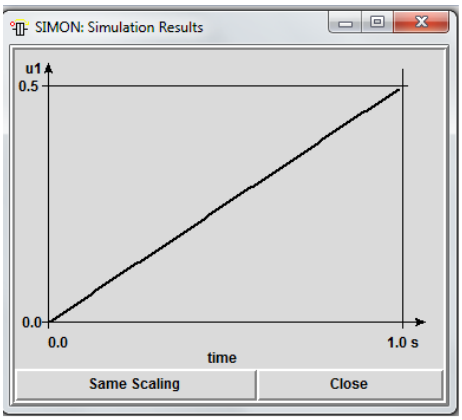
The corresponding matrix for the logical image was created. All the positions in the matrix that was not zero, were saved in a matrix. This matrix has been attached.

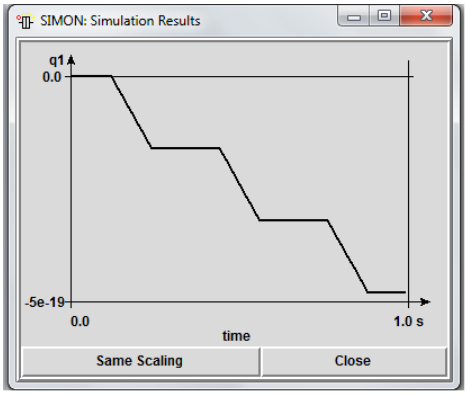
The matrix of the logical image will be used as reference when used for signature verification purposes. The 0s denote black and the 1s denote white.

CHAPTER IV: RESULTS

Given below is the circuit for simulation of the Single Electron Transistor and the results of the simulation showing the voltage, charge and current. The single electron transistor circuit has been simulated using the SIMON software, which was developed by C. Wasshuber and his collaborators at the Technical University of Vienna, Austria. SIMON software is used for simulation of circuits having single electron devices. It provides a graphical interface to the user and an approximate account of co-tunneling.







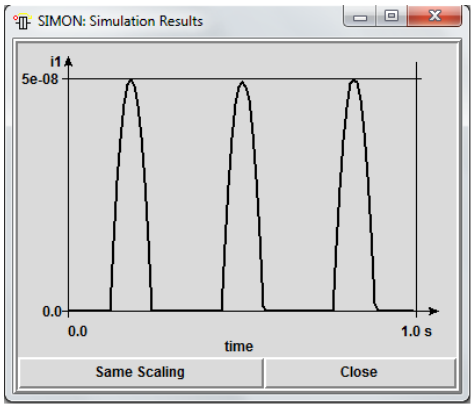


Fig 9: The simulation circuit for an SET. The following graphs show the stationary simulated voltage charge and current for the circuit

Forming the signature verification system requires flip-flops, Ex-OR gates and other logic gates.

Given below is the simulation of the EX-OR gate using SIMON software.

-

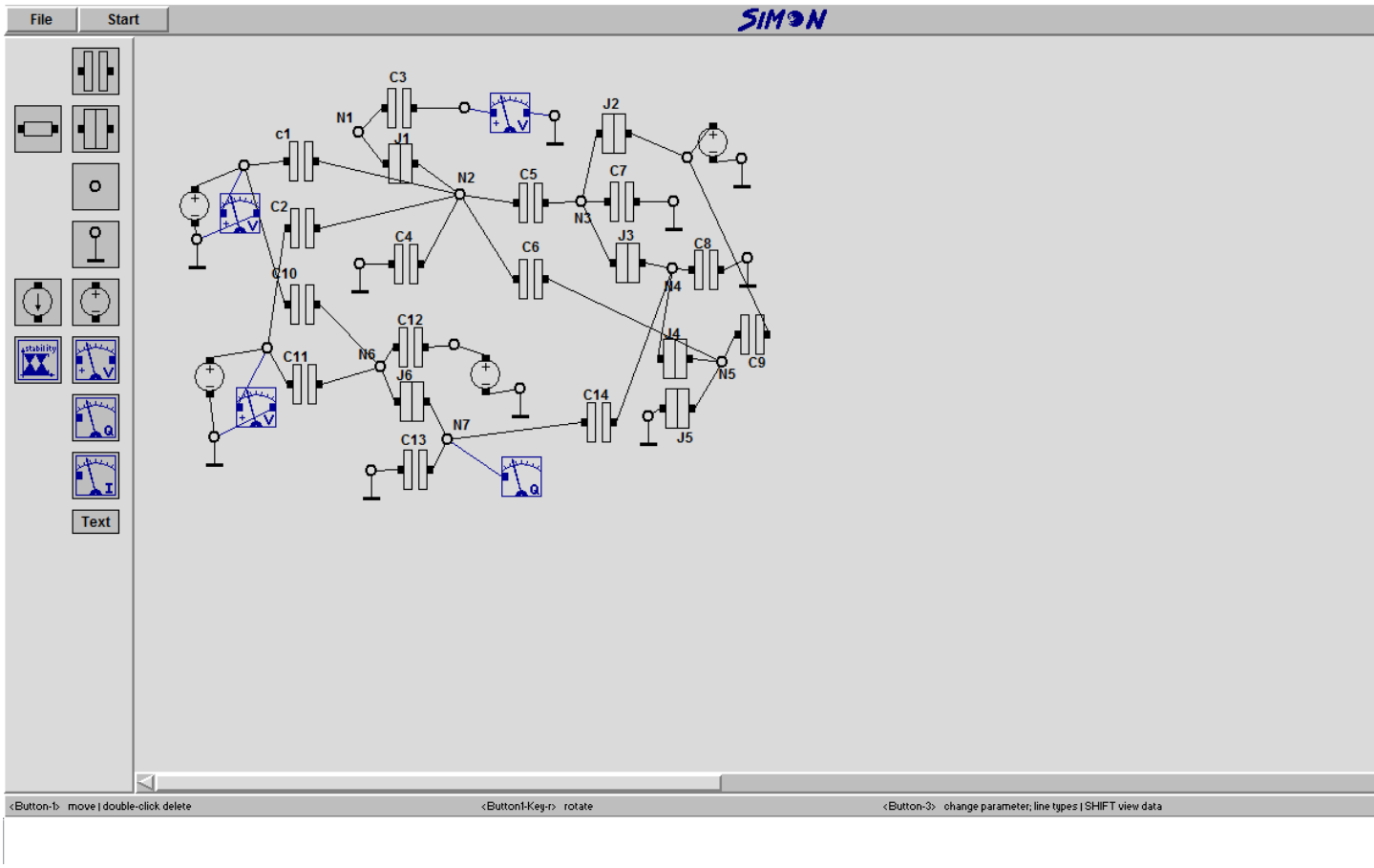


Fig 10- EX-OR circuit using SETs

The results of the simulation of this ex-or circuit are given

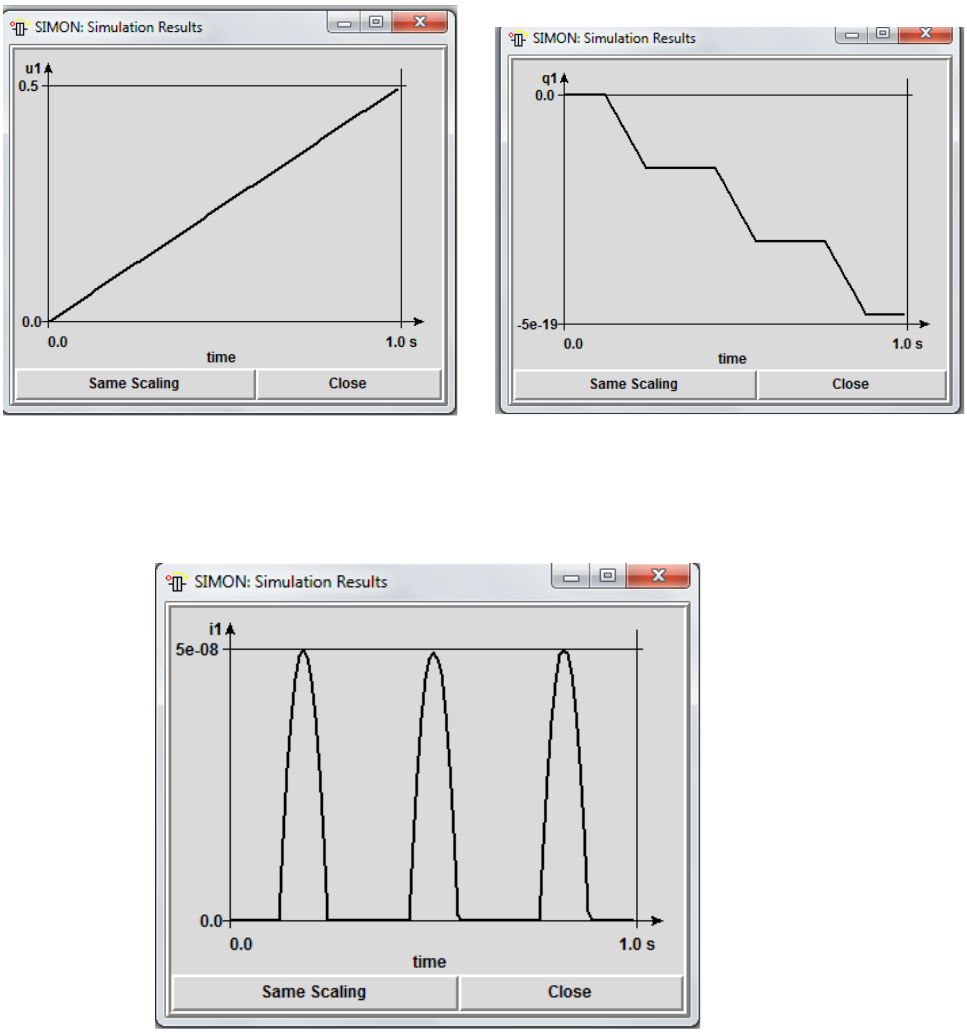
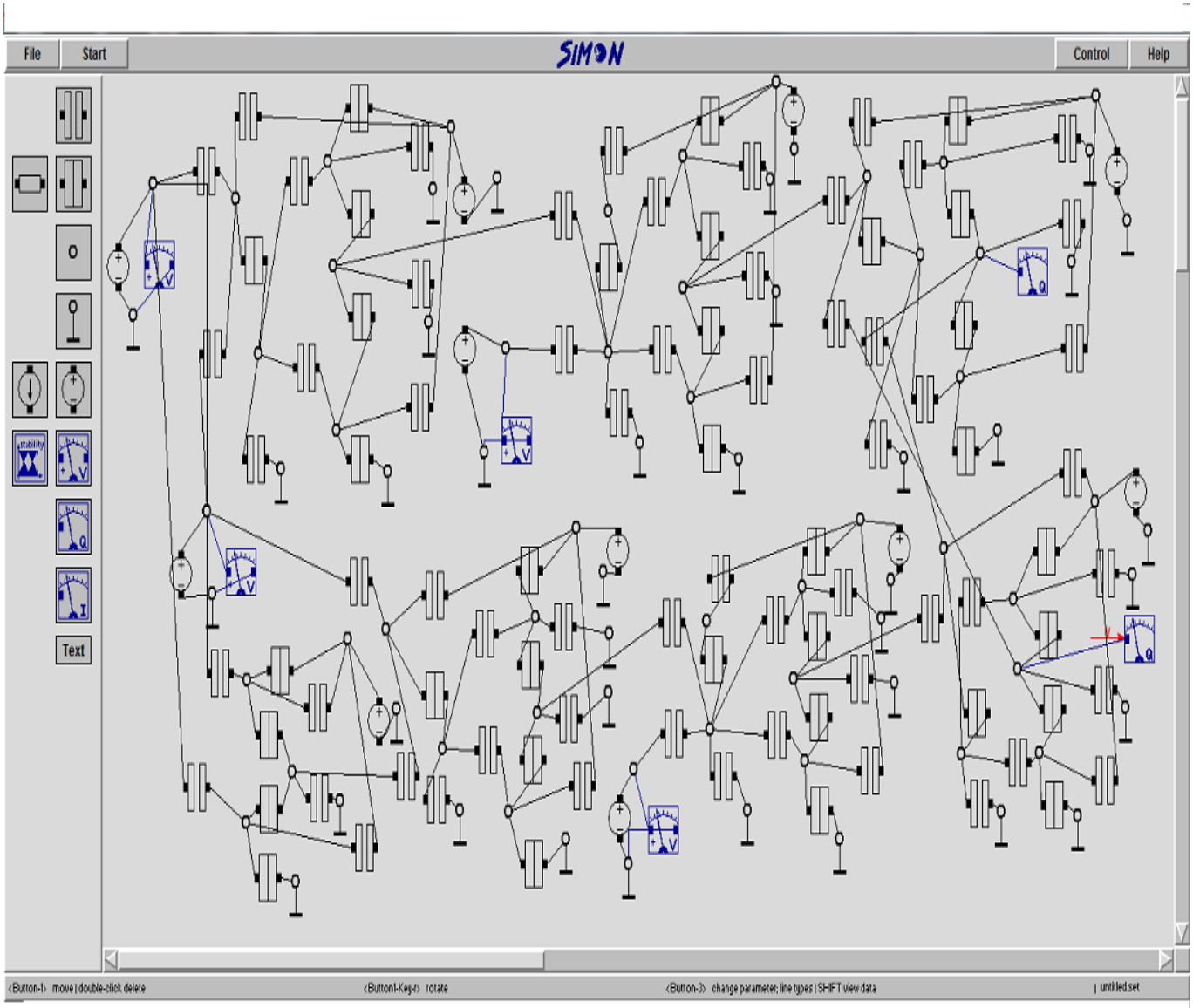
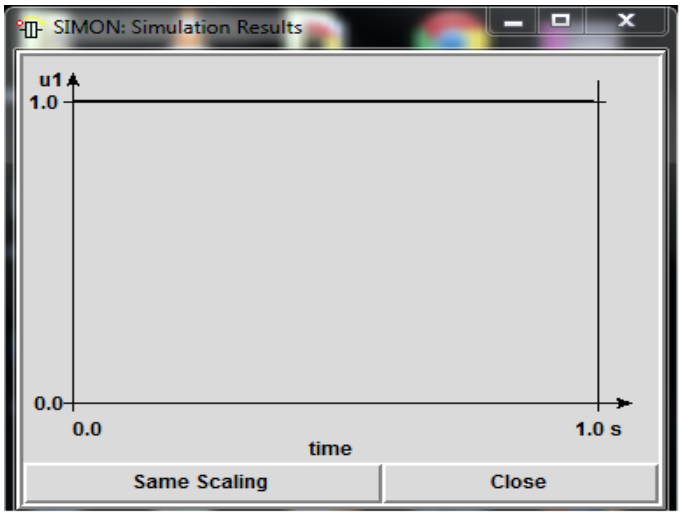
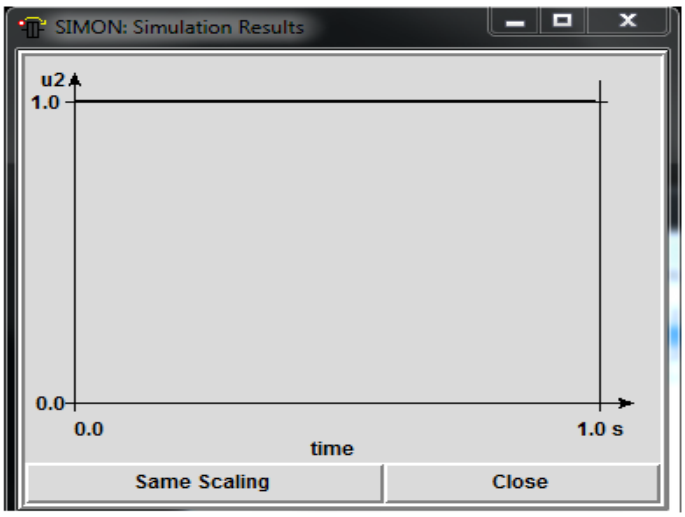


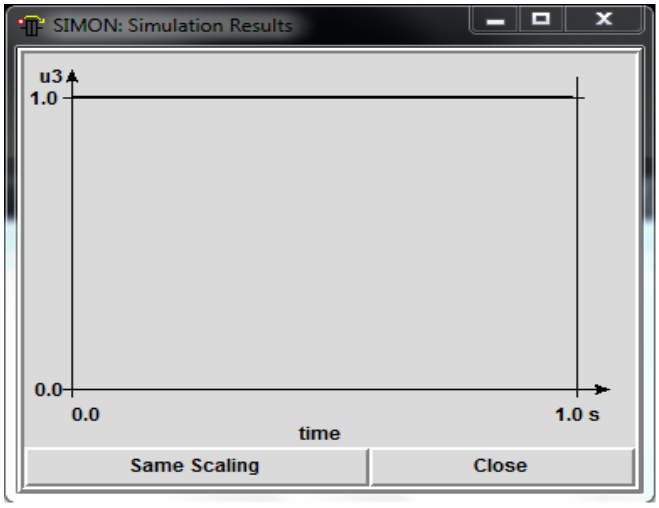
Fig 11: The simulation results show the potential, charge and current variation of an Xor gate using SETs with time respectively.

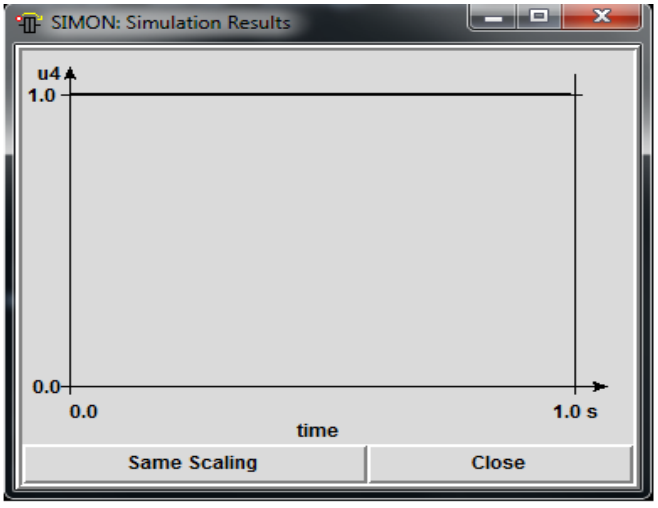
The D-Flip Flop circuit has been simulated using the SIMON software and the circuit and the results of the simulation have been attached herewith.




SIMON: Simulation Results
u1
1.0
0.0
0.0
1.0 s
time
Same Scaling
Close


SIMON: Simulation Results
u2
1.0
0.0
0.0
1.0 s
time
Same Scaling
Close


SIMON: Simulation Results
u3
1.0
0.0
0.0
1.0 s
time
Same Scaling
Close


SIMON: Simulation Results
u4
1.0
0.0
0.0
1.0 s
time
Same Scaling
Close

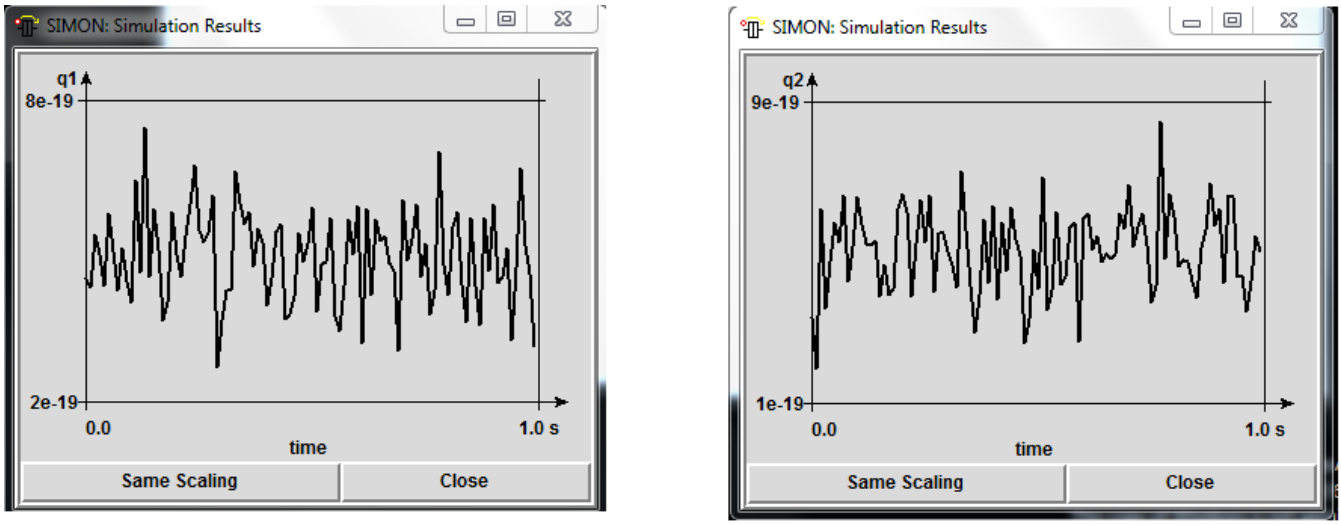


Fig 12- The above shows the D-Flip Flop circuit and the results of the simulation.

The results for the image inversion from rgb to black and white, or binary is given below

The matrix form of the above binary image has been attached herewith.

11	64	31	219	40	233	50	236	56	86	59	130	61	172	69	66	95	158
11	65	31	220	41	25	50	237	56	88	59	131	61	173	69	76	95	165
11	66	32	30	41	26	50	238	56	89	59	132	61	174	69	77	95	169
11	67	32	31	41	52	50	239	56	90	59	133	61	175	69	78	96	110
11	68	32	69	41	53	50	243	56	100	59	134	61	185	69	79	96	115
11	69	32	70	41	54	50	244	56	101	59	135	61	186	69	80	96	116
11	70	32	71	41	55	50	245	56	102	59	136	61	218	69	81	96	121
11	71	32	72	41	56	50	246	56	106	59	137	61	219	69	191	96	122
12	61	32	219	41	57	51	24	56	107	59	138	61	233	69	192	96	129
12	62	32	220	41	195	51	25	56	108	59	139	61	234	69	193	96	133
12	63	33	29	41	196	51	83	56	109	59	140	61	235	69	194	96	134
12	64	33	30	41	197	51	84	56	110	59	141	61	286	69	218	96	140
12	65	33	67	41	218	51	85	56	111	59	142	61	287	69	219	96	141
12	66	33	68	41	219	51	86	56	112	59	143	61	288	69	220	96	146
12	67	33	69	41	220	51	94	56	113	59	150	61	289	69	221	96	149
12	68	33	70	41	232	51	95	56	114	59	151	61	290	69	222	96	150
12	69	33	71	41	233	51	96	56	115	59	152	61	291	69	223	96	151
12	70	33	219	41	234	51	97	56	116	59	153	61	292	69	224	96	157
12	71	33	220	42	25	51	98	56	117	59	158	61	293	69	225	96	158
12	72	34	28	42	26	51	99	56	118	59	159	61	294	70	35	96	165
12	73	34	29	42	52	51	100	56	119	59	160	61	295	70	36	96	166
12	74	34	30	42	53	51	101	56	120	59	175	61	296	70	37	96	169
12	75	34	65	42	54	51	102	56	121	59	176	61	297	70	38	96	171
13	58	34	66	42	55	51	103	56	122	59	177	62	27	70	65	96	172
13	59	34	67	42	56	51	104	56	123	59	178	62	28	70	66	96	178
13	60	34	68	42	57	51	105	56	124	59	179	62	69	70	67	96	179
13	61	34	69	42	58	51	106	56	154	59	180	62	70	70	72	96	187
13	62	34	207	42	59	51	107	56	155	59	181	62	71	70	73	96	191
13	63	34	208	42	60	51	159	56	156	59	182	62	72	70	74	96	197
13	64	34	209	42	61	51	160	56	157	59	183	62	88	70	75	96	198
13	71	34	210	42	62	51	161	56	158	59	184	62	89	70	76	97	110
13	72	34	211	42	63	51	187	56	159	59	185	62	90	70	77	97	111
13	73	34	212	42	64	51	188	56	160	59	186	62	141	70	78	97	114
13	74	34	213	42	65	51	218	56	185	59	187	62	142	70	79	97	115
13	75	34	214	42	66	51	219	56	186	59	188	62	143	70	193	97	120
13	76	34	215	42	67	51	225	56	187	59	189	62	144	70	194	97	123
13	77	34	216	42	68	51	226	56	218	59	190	62	145	70	195	97	126

13	78	34	217	42	69	51	227	56	219	59	191	62	146	70	196	97	127
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14	77	35	63	42	220	51	239	56	264	59	219	62	218	70	220	97	149
14	78	35	64	42	234	51	245	56	265	59	235	62	219	70	221	97	157
14	79	35	65	42	235	51	246	56	266	59	236	62	232	70	222	97	158
14	80	35	66	43	24	52	24	56	267	59	237	62	233	71	37	97	165
15	54	35	67	43	25	52	25	57	25	59	247	62	234	71	38	97	166
15	55	35	199	43	52	52	84	57	26	59	248	62	292	71	39	97	169
15	56	35	200	43	53	52	85	57	78	59	249	62	293	71	66	97	173
15	57	35	201	43	54	52	86	57	79	59	250	62	294	71	67	97	176
15	58	35	202	43	55	52	87	57	80	59	251	62	295	71	68	97	177
15	79	35	203	43	56	52	91	57	81	59	252	62	296	71	69	97	180
15	80	35	204	43	57	52	92	57	82	59	253	62	297	71	70	97	183
15	81	35	205	43	58	52	93	57	83	59	254	62	298	71	71	97	184
15	82	35	206	43	59	52	94	57	89	59	255	62	299	71	72	97	188
16	52	35	207	43	60	52	95	57	90	59	256	62	300	71	73	97	192
16	53	35	208	43	61	52	96	57	100	59	257	62	301	71	74	97	196
16	54	35	209	43	62	52	97	57	101	59	258	62	302	71	75	97	199
16	55	35	210	43	63	52	98	57	102	59	259	63	28	71	76	98	110
16	56	35	211	43	64	52	99	57	104	59	260	63	29	71	195	98	111
16	81	35	212	43	65	52	100	57	105	59	261	63	68	71	196	98	114
16	82	35	213	43	66	52	101	57	106	59	262	63	69	71	197	98	115
16	83	35	214	43	67	52	106	57	107	59	263	63	70	71	198	98	123
17	50	35	215	43	68	52	107	57	108	59	264	63	71	71	199	98	127
17	51	35	216	43	69	52	108	57	109	59	265	63	88	71	200	98	135
17	52	35	217	43	70	52	109	57	110	59	266	63	89	71	201	98	136
17	53	35	218	43	71	52	158	57	111	59	267	63	142	71	202	98	138
17	54	35	219	43	72	52	159	57	112	59	268	63	143	71	203	98	143
17	82	35	220	43	193	52	160	57	113	59	269	63	144	71	204	98	146
17	83	35	221	43	194	52	161	57	114	59	270	63	145	71	205	98	157
17	84	35	222	43	195	52	186	57	115	59	271	63	146	71	206	98	158
18	48	35	223	43	218	52	187	57	116	59	272	63	186	71	207	98	165
18	49	35	224	43	219	52	188	57	117	59	273	63	187	71	208	98	166
18	50	36	27	43	220	52	218	57	118	59	274	63	218	71	209	98	169
18	51	36	28	43	234	52	219	57	119	59	275	63	219	71	210	98	173
18	52	36	61	43	235	52	222	57	120	59	276	63	231	71	211	98	174

18	83	36	62	43	236	52	223	57	121	59	277	63	232	71	212	98	180
18	84	36	63	44	24	52	224	57	122	59	278	63	233	71	213	98	184
18	85	36	64	44	25	52	225	57	123	59	279	63	297	71	214	98	188
19	46	36	65	44	66	52	226	57	124	59	280	63	298	71	215	98	192
19	47	36	192	44	67	52	227	57	142	59	281	63	299	71	216	98	199
19	48	36	193	44	68	52	228	57	143	59	282	63	300	71	217	99	110
19	49	36	194	44	69	52	238	57	153	59	283	63	301	71	218	99	115
19	50	36	195	44	70	52	239	57	154	59	284	63	302	71	219	99	116
19	84	36	196	44	71	52	245	57	155	59	285	63	303	71	220	99	121
19	85	36	197	44	72	52	246	57	158	60	26	63	304	72	38	99	123
19	221	36	198	44	73	52	247	57	159	60	27	63	305	72	39	99	127
20	45	36	199	44	74	53	24	57	185	60	72	64	29	72	40	99	135
20	46	36	200	44	75	53	25	57	186	60	73	64	30	72	41	99	138
20	47	36	201	44	192	53	86	57	187	60	74	64	67	72	67	99	146
20	48	36	202	44	193	53	87	57	218	60	75	64	68	72	68	99	147
20	84	36	203	44	194	53	88	57	219	60	76	64	69	72	69	99	148
20	85	36	204	44	218	53	89	57	236	60	89	64	86	72	70	99	157
20	220	36	205	44	219	53	90	57	237	60	90	64	87	72	71	99	158
20	221	36	206	44	235	53	91	57	238	60	124	64	88	72	72	99	165
20	222	36	207	44	236	53	92	57	246	60	125	64	89	72	73	99	166
21	43	36	208	44	237	53	93	57	247	60	126	64	186	72	198	99	169
21	44	36	209	45	24	53	94	57	261	60	127	64	187	72	199	99	174
21	45	36	213	45	25	53	95	57	262	60	128	64	218	72	200	99	178
21	46	36	214	45	73	53	103	57	263	60	129	64	219	72	201	99	180
21	84	36	215	45	74	53	104	57	264	60	130	64	229	72	202	99	184
21	85	36	216	45	75	53	105	57	265	60	131	64	230	72	203	99	188
21	220	36	217	45	76	53	106	57	266	60	139	64	231	72	204	99	192
21	221	36	218	45	77	53	107	57	267	60	140	64	232	72	205	99	199
21	222	36	219	45	191	53	108	58	26	60	141	64	303	72	206	100	110
21	223	36	220	45	192	53	109	58	76	60	142	64	304	72	207	100	116
22	41	36	221	45	193	53	110	58	77	60	148	64	305	72	208	100	120
22	42	36	222	45	218	53	157	58	78	60	149	64	306	72	209	100	123
22	43	36	223	45	219	53	158	58	79	60	150	64	307	72	210	100	127
22	44	36	224	45	236	53	159	58	80	60	151	64	308	72	211	100	132
22	45	36	225	45	237	53	160	58	81	60	159	64	309	72	212	100	135
22	84	36	226	46	24	53	186	58	89	60	160	65	30	72	213	100	136
22	85	36	227	46	25	53	187	58	90	60	161	65	31	72	214	100	138
22	220	37	26	46	75	53	218	58	100	60	162	65	66	72	215	100	146
22	221	37	27	46	76	53	219	58	101	60	163	65	67	72	216	100	148
22	222	37	28	46	77	53	221	58	102	60	164	65	68	72	217	100	149
22	223	37	59	46	78	53	222	58	103	60	165	65	85	72	218	100	158

23	40	37	60	46	190	53	223	58	104	60	166	65	86	72	219	100	165
23	41	37	61	46	191	53	224	58	105	60	167	65	87	73	40	100	169
23	42	37	62	46	192	53	225	58	106	60	168	65	88	73	41	100	174
23	43	37	63	46	218	53	238	58	122	60	169	65	187	73	42	100	177
23	83	37	190	46	219	53	239	58	123	60	170	65	188	73	43	100	180
23	84	37	191	46	236	53	245	58	130	60	171	65	218	73	218	100	183
23	85	37	192	46	237	53	246	58	131	60	172	65	219	73	219	100	184
23	220	37	193	46	238	53	247	58	132	60	173	65	228	74	42	100	188
23	221	37	194	47	24	54	24	58	133	60	174	65	229	74	43	100	192
24	39	37	195	47	25	54	25	58	134	60	175	65	230	74	44	100	196
24	40	37	196	47	77	54	86	58	135	60	176	65	231	74	45	100	199
24	41	37	197	47	78	54	87	58	136	60	177	65	306	74	218	101	110
24	82	37	198	47	79	54	88	58	137	60	178	65	307	74	219	101	115
24	83	37	199	47	80	54	89	58	138	60	179	65	308	75	44	101	116
24	84	37	200	47	189	54	90	58	139	60	180	65	309	75	45	101	119
24	220	37	201	47	190	54	91	58	140	60	181	65	310	75	46	101	123
24	221	37	202	47	191	54	92	58	141	60	185	65	311	75	47	101	127
25	37	37	203	47	218	54	102	58	142	60	186	66	31	75	48	101	131
25	38	37	204	47	219	54	103	58	143	60	218	66	32	75	49	101	132
25	39	37	216	47	237	54	104	58	151	60	219	66	66	75	50	101	135
25	40	37	217	47	238	54	105	58	152	60	234	66	67	75	218	101	138
25	80	37	218	48	24	54	106	58	153	60	235	66	83	75	219	101	139
25	81	37	219	48	25	54	107	58	154	60	236	66	84	76	45	101	146
25	82	37	220	48	79	54	108	58	158	60	249	66	85	76	46	101	149
25	83	37	225	48	80	54	109	58	159	60	250	66	86	76	47	101	158
25	220	37	226	48	81	54	110	58	180	60	251	66	87	76	48	101	164
25	221	37	227	48	189	54	156	58	181	60	252	66	187	76	49	101	165
26	36	37	228	48	190	54	157	58	182	60	253	66	188	76	50	101	169
26	37	37	229	48	218	54	158	58	183	60	254	66	189	76	51	101	173
26	38	38	26	48	219	54	159	58	184	60	255	66	218	76	218	101	176
26	39	38	27	48	235	54	160	58	185	60	256	66	219	76	219	101	180
26	79	38	58	48	236	54	186	58	186	60	264	66	226	77	47	101	184
26	80	38	59	48	237	54	187	58	187	60	265	66	227	77	48	101	188
26	81	38	60	48	238	54	218	58	188	60	266	66	228	77	49	101	192
26	82	38	61	48	239	54	219	58	189	60	267	66	229	77	50	101	195
26	219	38	62	48	240	54	221	58	190	60	268	66	230	77	51	101	199
26	220	38	190	48	241	54	222	58	191	60	269	66	310	77	218	102	109
26	221	38	191	48	242	54	223	58	192	60	270	66	311	77	219	102	110
27	35	38	192	49	24	54	237	58	193	60	271	66	312	78	50	102	111
27	36	38	193	49	81	54	238	58	194	60	272	67	32	78	219	102	114
27	37	38	194	49	82	54	239	58	195	60	273	67	33	78	220	102	115

27	77	38	198	49	83	54	246	58	196	60	274	67	65	79	219	102	119
27	78	38	199	49	188	54	247	58	218	60	275	67	66	79	220	102	120
27	79	38	200	49	189	55	25	58	219	60	276	67	67	80	219	102	123
27	80	38	201	49	190	55	26	58	236	60	277	67	81	80	220	102	124
27	219	38	202	49	218	55	83	58	237	60	278	67	82	81	219	102	126
27	220	38	217	49	219	55	84	58	246	60	279	67	83	81	220	102	127
27	221	38	218	49	232	55	85	58	247	60	280	67	84	82	219	102	132
28	34	38	219	49	233	55	86	58	248	60	281	67	85	82	220	102	135
28	35	38	220	49	234	55	87	58	249	60	282	67	188	82	221	102	136
28	36	38	227	49	235	55	88	58	254	60	283	67	189	83	220	102	139
28	75	38	228	49	236	55	89	58	255	60	284	67	190	83	221	102	140
28	76	38	229	49	237	55	90	58	257	60	285	67	218	83	222	102	141
28	77	38	230	49	238	55	101	58	258	60	286	67	219	83	223	102	142
28	78	38	231	49	239	55	102	58	259	60	287	67	224	83	224	102	145
28	79	39	26	49	240	55	103	58	260	60	288	67	225	84	220	102	146
28	219	39	56	49	241	55	104	58	261	60	289	67	226	84	221	102	147
28	220	39	57	49	242	55	107	58	262	60	290	67	227	84	222	102	149
28	221	39	58	49	243	55	108	58	263	60	291	67	228	84	223	102	150
29	33	39	59	49	244	55	109	58	264	61	27	67	310	84	224	102	151
29	34	39	60	49	245	55	120	58	265	61	28	67	311	85	221	102	159
29	35	39	197	50	24	55	121	58	266	61	70	68	33	85	222	102	160
29	74	39	198	50	25	55	122	58	267	61	71	68	34	85	223	102	163
29	75	39	199	50	82	55	155	58	268	61	72	68	65	93	110	102	169
29	76	39	200	50	83	55	156	59	26	61	73	68	66	93	111	102	170
29	77	39	217	50	84	55	157	59	27	61	74	68	79	93	114	102	172
29	78	39	218	50	99	55	158	59	74	61	89	68	80	93	115	102	173
29	219	39	219	50	100	55	159	59	75	61	90	68	81	93	145	102	176
29	220	39	220	50	101	55	160	59	76	61	141	68	82	93	146	102	177
30	31	39	229	50	102	55	186	59	77	61	142	68	83	93	159	102	180
30	32	39	230	50	103	55	187	59	78	61	145	68	84	93	160	102	183
30	33	39	231	50	104	55	218	59	79	61	146	68	189	93	163	102	184
30	34	39	232	50	105	55	219	59	89	61	147	68	190	93	164	102	187
30	72	40	25	50	106	55	237	59	90	61	148	68	191	93	168	102	188
30	73	40	26	50	160	55	238	59	91	61	149	68	192	93	169	102	189
30	74	40	55	50	187	55	239	59	100	61	150	68	218	94	110	102	192
30	75	40	56	50	188	55	246	59	101	61	160	68	219	94	115	102	193
30	76	40	57	50	189	55	247	59	102	61	161	68	222	94	116	102	195
30	219	40	58	50	218	55	264	59	103	61	162	68	223	94	146	102	196
30	220	40	196	50	219	55	265	59	104	61	163	68	224	94	158	102	199
31	31	40	197	50	228	55	266	59	122	61	164	68	225	94	164	102	200
31	32	40	198	50	229	56	25	59	123	61	165	68	226	94	165	0	0

31	33	40	199	50	230	56	26	59	124	61	166	68	310	94	169	0	0
31	70	40	218	50	231	56	81	59	125	61	167	68	311	95	110	0	0
31	71	40	219	50	232	56	82	59	126	61	168	69	34	95	115	0	0
31	72	40	220	50	233	56	83	59	127	61	169	69	35	95	116	0	0
31	73	40	231	50	234	56	84	59	128	61	170	69	36	95	146	0	0
31	74	40	232	50	235	56	85	59	129	61	171	69	65	95	157	0	0

Table 1- Matrix showing the non-zero positions in the matrix of the signature given above.

The image and inversions of another signature is given below

The output when different signatures were fed

348

The signatures are not the same

The output when the same signature was fed

0

The signatures are the same

The truth table for the hardware model of the device

Preset	Input	A	B	C	D
0	0	0	1	1	1
		1	1	1	1
		0	1	1	1…
0	1	0	0	1	1
		0	1	1	1
		1	0	1	1
		0	1	1	1
		1	1	1	1
		0	1	1	1…
1	0	0	1	0	0
		1	1	0	0
		0	1	0	0…
1	1	1	1	1	1…

Table 2- Truth table of the logic circuit of the SVS

CHAPTER V: CONCLUSION

The single electron devices are promising candidates for the elements of future because of the unique principle of operation, quantized nature of carrier transport, high switching speed, ultra small size, and low power dissipation. They are the future of the integrated circuits. Use of single electron transistor will help develop a signature verification system that would be low power consuming, compact and fast. The verification system would be designed using the MATLAB software, as SIMON 2.0 does not have a command to input desired inputs. Because of the limitations of SIMON 2.0, MATLAB will be used to devise a signature verification system. The need for a hardware implementation of the verification device arises from the fact that it would be more robust, compact and easy to use in comparison to a software implementation of it.

LIST OF FIGURES

LIST OF TABLES

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