GRID SYNCHRONIZATION ALGORITHM FOR DISTRIBUTED GENERATION SYSTEM DURING GRID ABNORMALITIES

A Thesis submitted in partial fulfillment of the requirements for the degree of

Bachelor of Technology in "Electrical Engineering"

By

BINITA SEN (108EE036)

DUSHYANT SHARMA (108EE046)

Department of Electrical Engineering
National Institute of Technology
Rourkela-769008 (ODISHA)
May-2012

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Under guidance of

Prof. B.CHITTI BABU

Department of Electrical Engineering
National Institute of Technology
Rourkela-769008 (ODISHA)
May-2012

DEPARTMENT OF ELECTRICAL ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY, ROURKELA

ODISHA, INDIA-769008

CERTIFICATE

This is to certify that the thesis entitled "**GRID SYNCHRONIZATION ALGORITHM FOR DISTRIBUTED GENERATION SYSTEM DURING GRID ABNORMALITIES**", submitted by **Binita Sen (Roll. No. 108EE036) and Dushyant Sharma (Roll. No. 108EE046)** in partial fulfillment of the requirements for the award of **Bachelor of Technology** in **Electrical Engineering** during session 2011-2012 at National Institute of Technology, Rourkela. A bonafide record of research work carried out by them under my supervision and guidance.

The candidates have fulfilled all the prescribed requirements.

The thesis which is based on candidates' own work, has not been submitted elsewhere for a degree/diploma.

In my opinion, the thesis is of standard required for the award of a Bachelor of Technology degree in Electrical Engineering.

Place: Rourkela

Dept. of Electrical Engineering
National institute of Technology
Rourkela-769008

Prof. B.Chitti Babu
Assistant Professor

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Binita Sen

Dushyant Sharma

B.Tech (Electrical Engineering)

Dedicated to

Our beloved parents

ABSTRACT

Distributed Generation (DG) System is a small scale (less than 20 MW) electric or shaft power generation at or near the user's facility as opposed to the normal mode of centralized power generation. DGs include wind energy, photo voltaic system, fuel cell and combined heat and power (CHP) generation etc. To ensure safe and reliable operation of power system based on DG system, usually power plant operators should satisfy the grid code requirements such as grid stability, fault ride through, power quality improvement, grid synchronization and power control etc. Number of synchronizing algorithms has been discussed in the literature to track the phase angle of the grid voltage or current to synchronize DG system with the grid. One of the earliest introduced methods for tracking the phase angle is Zero Crossing Detector (ZCD) and it gives better response during balanced grid conditions. But the occurrence of power quality problems, especially in weak grid, leads to malfunctioning of the controllers based on ZCDs. An alternative to ZCD is the Phase Locked Loops (PLLs) for grid synchronization which provides better response with accuracy. Different PLLs have also been proposed and are studied extensively in the available literature starting from Charge Pump PLL to Linear PLL and Synchronous Reference Frame (SRF) PLL which can very well track the phase angle and frequency during balanced conditions. But during abnormal conditions like frequency deviations, voltage unbalances and power quality problems such as voltage flicker, voltage dip, voltage sag, distorted grid voltages, these PLLs fails to track the phase angle and frequency with good accuracy. These shortcomings are overcome by Double Synchronous Reference Frame (DSRF) PLL and a PLL based on Second Order Generalized Integrator (SOGI).

In this work the above mentioned PLLs are analysed for different abnormal grid condition which is followed by the comparative study between two advanced PLL techniques (DSRF PLL and SOGI based PLL). The analysis is carried out in MATLAB/SIMULINK environment and the obtained results are discussed for effectiveness of the study.

CONTENTS

Abstract i

Contents ii

List of Figures v

CHAPTER-1

INTRODUCTION

1.1 Motivation 2

1.2 Literature Review 2

1.3 Thesis Objective 3

1.4 Organization of the Thesis 4

1.5 Project Contribution 5

CHAPTER-2

GRID SYNCHRONIZATION ALGORITHM FOR POWER CONVERTERS

2.1 Introduction 7

2.2 Grid Connection Requirements 7

2.3 Grid Synchronization Algorithms 9

2.3. 1 Zero Crossing Detector 9

2.3. 2 Phase Locked Loop 9

A. Linear PLL 10

B. Synchronous Reference Frame PLL 11

C. Double Synchronous Reference Frame (DSRF) PLL 12

D. Second Order Generalized Integrator (SOGI) based PLL 14

2.4 Conclusion 15

CHAPTER-3

GRID SYNCHRONIZATION USING DOUBLE SYNCHRONOUS REFERENCE FRAME (DSRF) PLL

3.1 Introduction 17

3.2 Analysis of Synchronous Reference Frame (SRF) PLL 17

3.3 Analysis of Double Synchronous Reference Frame (DSRF) PLL 20

3.4 Simulation Results and Discussions 22

3.4.1 Dynamic Response of DSRF PLL during Unbalanced Grid Voltages 22

3.4.2 Response of DSRF PLL under Line to Ground Fault 24

3.4.3 Response of DSRF PLL during Voltage Sag 26

3.4.4 Response of DSRF PLL during Frequency Deviation 28

3.4.5 Response of DSRF PLL during Voltage Flicker 30

3.4.6 Response of DSRF PLL during Harmonic Injection 32

3.4.7 Response of DSRF PLL during Voltage Dip 34

3.5 Conclusion 36

CHAPTER-4

ANALYSIS OF SECOND ORDER GENERALIZED INTEGRATOR (SOGI) BASED PLL

4.1 Introduction 38

4.2 Analysis of Second Order Generalized Integrator (SOGI) based PLL 38

4.3 Simulation Results and Discussions 39

4.3. 1 Response of SOGI based PLL under Line to Ground Fault 41

4.3. 2 Response of SOGI based PLL during Frequency Deviation 43

4.3. 3 Response of SOGI based PLL during Harmonic Injection 45

4.3. 4 Response of SOGI based PLL during Voltage Dip 47

4.3. 5 Response of SOGI based PLL during Voltage Flicker 49

4.3. 6 Response of SOGI based PLL during Voltage Sag 50

4.4 Comparative Study 52

4.4. 1 Comparison of SOGI based PLL and DSRF PLL under Line to Ground Fault 52

4.4. 2 Comparison of SOGI based PLL and DSRF PLL during Frequency Deviation 54

4.4. 3 Comparison of SOGI based PLL and DSRF PLL during Voltage Sag 56

4.4. 4 Comparison of SOGI based PLL and DSRF PLL during Voltage Dip 58

4.4. 5 Comparison of SOGI based PLL and DSRF PLL during Voltage Flicker 60

4.4. 6 Comparison of SOGI based PLL and DSRF PLL during Harmonic Injection 62

4.5 Conclusion 64

CHAPTER-5

CONCLUSIONS AND FUTURE WORK

5.1 Conclusions 66

5.2 Future Work 66

References 67

Research Publications 69

LIST OF FIGURES

Fig. No.	Name of the Figure	Page. No.
2.1	Block Diagram of a PLL	10
2.2	Block Diagram of a LPLL	11
2.3	Block Diagram of a SRF PLL	12
2.4	Synthesis Circuit used in DSRF PLL	13
2.5	Voltage Vector Decomposition (Unbalanced Voltage)	13
2.6	Block Diagram of DSRF PLL	13
2.7	SOGI based Quadrature Signal Generation (QSG)	14
2.8	Block Diagram of SOGI based PLL	14
3.1	Simulink Results for SRF PLL during Unbalanced Grid Conditions	19
3.2	Simulink Model of a DSRF PLL	22
3.3	Dynamic Response of DSRF PLL during Unbalanced Grid Conditions	23
3.4	Response of DSRF PLL under Line to Ground Fault	25
3.5	Response of DSRF PLL during Voltage Sag	27
3.6	Response of DSRF PLL during Frequency Deviation	29
3.7	Response of DSRF PLL during Voltage Flicker	31
3.8	Response of DSRF PLL during Harmonic Injection	33
3.9	Response of DSRF PLL during Voltage Dip	35
4.1	Simulink model of SOGI based PLL	40
4.2	Frequency Response for SOGI-QSG	41
4.3	Response of SOGI based PLL under Line to Ground Fault	42
4.4	Response of SOGI based PLL during frequency Deviation	44
4.5	Response of SOGI based PLL during Harmonic Injection	46
4.6	Response of SOGI based PLL during Voltage Dip	48
4.7	Response of SOGI based PLL during Voltage Flicker	49
4.8	Response of SOGI based PLL during Voltage Sag	51
4.9	Comparison of SOGI based PLL and DSRF PLL under Line to Ground Fault	53
4.10	Comparison of SOGI based PLL and DSRF PLL during Frequency Deviation	55
4.11	Comparison of SOGI based PLL and DSRF PLL during Voltage Sag	57

4.12 Comparison of SOGI based PLL and DSRF PLL during Voltage Dip 59
4.13 Comparison of SOGI based PLL and DSRF PLL during Voltage Flicker 61
4.14 Comparison of SOGI based PLL and DSRF PLL during Harmonic Injection 63

CHAPTER 1

Introduction

1.1 MOTIVATION:

The use of fossil fuels for electric power generation has imposed several problems on the environment including global warming and greenhouse effect. This has led to an era in which the increasing power demand will be met by Distributed Generation (DG) system which are based on renewable energy sources such as solar power, wind power, small hydro power etc. [1]-[2].

The DG systems are distributed near the user's facility. These systems are mainly small scale generations having capacity less than 20MW. These Distributed Generation (DG) systems need to be controlled properly in order to ensure sinusoidal current injection into the grid. However, they have a poor controllability due to their intermittent characteristics [3]. Grid connected inverter is the key element to maintain voltage at the point of common coupling (PCC) constant and to ensure power quality improvements. For safe and reliable operation of power system based on DG system, usually power plant operators should satisfy the grid code requirements such as grid stability, fault ride through, power quality improvement, grid synchronization and power control etc. The major issue associated with DG system is their synchronization with utility voltage vector [4]. The information about the phase angle of utility voltage vector is accurately tracked in order to control the flow of active and reactive power and to turn on and off power devices.

1.2 LITERATURE REVIEW:

Few of the earliest known synchronization algorithms include Zero Crossing Detectors (ZCDs). The performance of ZCDs is badly affected by power quality problems, especially in the case of weak grid. The use of Phase Locked Loops (PLLs) for grid synchronization provides better response and it has been discussed in [5]. The Linear PLL is mainly used to detect phase for single phase supply. For balanced three phase supply, Synchronous Reference Frame (SRF) PLL is used. The PLL based on Synchronous Reference Frame uses Park's Transformation which takes two orthogonal signals as inputs and generates constant voltages. To generate orthogonal components Clarke's transformation is employed. But it is found that, this PLL fails

to detect the phase for unbalanced grid condition [6]. Hence Decoupled Double Synchronous Reference Frame (DDSRF) PLL was proposed to deal with unbalanced grid conditions like voltage unbalance [7]. DDSRF PLL can detect the positive sequence phase angle in such conditions. Double Synchronous Reference Frame (DSRF) PLL based on synthesis circuit was proposed in [6] which is more frequency adaptive and can be easily implemented. Other PLL techniques used for grid synchronization include Enhanced PLL (EPLL) which does not use Synchronous Reference Frame but rather synchronizes each phase of a 3-phase system independently [8]. Other method used for detection of positive sequence is the use of Second Order Generalized Integrator (SOGI). The harmonic rejection capacity of this method is very high. The use of SOGI was proposed as an alternative of Clarke's transformation to generate orthogonal signals and then to use it for grid synchronization. Dual Second Order Generalized Integrator – Frequency Locked Loop (FLL) was proposed as an advanced method for grid synchronization [9]-[10]. Other than orthogonal signal generation SOGIs can be used as current controller, to eliminate harmonics [11] and to detect multiple grid frequencies. Multiple Second Order Generalized Integrator – Frequency Locked Loop (MSOGI FLL) was proposed in [12] which estimate not only the positive and negative sequence components at fundamental frequency but also other sequence components at multiple frequencies.

1.3 THESIS OBJECTIVES:

The following objectives have been achieved at the end of the project.

1) To analyse various grid synchronization algorithms available for phase angle tracking.
2) To study the conventional SRF Phase Locked Loops (PLL) and observe its response during grid unbalances.
3) To study the advanced PLL techniques (DSRF PLL and SOGI based PLL) and their response during abnormal grid conditions such as line to ground fault and various power quality problems. The power quality problems include voltage unbalances, voltage sag, voltage dip, voltage flicker, harmonic injection, frequency deviation etc.
4) To study the frequency response of the SOGI based PLL in order to analyse the stability of the system.

5) To observe the comparative analysis between DSRF PLL and SOGI based PLL to detect the phase angle during various abnormal grid conditions and power quality problems.

1.4 ORGANIZATION OF THESIS:

The thesis is organised into five chapters including the introduction. Each of these is summarized below.

Chapter 2 deals with the introduction of various grid synchronization algorithms used for power converters. First, a brief idea is given about various grid code requirements that need to be satisfied for proper operation of the DG system. This is followed by the analysis of various grid synchronization algorithms including Zero Crossing Detector (ZCD), Linear PLL (LPLL), Synchronous Reference Frame (SRF) PLL, Double Synchronous Reference Frame (DSRF) PLL and Second Order Generalized Integrator (SOGI) based PLL.

Chapter 3 describes the analysis and response of DSRF PLL. At first, it gives a brief idea of SRF PLL, its mathematical analysis, working and response during unbalanced grid condition and shows how it fails to track the phase angle for unbalanced condition. This is followed by the detailed mathematical analysis of DSRF PLL to show how it decouples the positive and negative sequence components and track the phase angle even in abnormal grid conditions. Finally, the simulation results showing the response of DSRF PLL under various abnormal grid conditions as obtained by simulations in MATLAB/SIMULINK environment are shown and discussed.

Chapter 4 describes the analysis and response of SOGI based PLL. It starts with a brief introduction about the SOGI based PLL, its mathematical analysis and working. Further, it shows the frequency response of the SOGI in order to study its stability. This is followed by the response of SOGI based PLL during abnormal grid conditions and illustrates how it tracks the phase angle of the positive and negative sequence components. Finally, the DSRF PLL and SOGI based PLL are compared in terms of phase tracking under various abnormal grid conditions and the results obtained MATLAB/SIMULINK environment are shown and discussed.

Chapter 5 reveals the general conclusions of the work done, followed by the references.

1.5 PROJECT CONTRIBUTION:

This project tests the different PLL techniques to track the phase angle of the positive sequence of a 3 phase system during abnormal grid conditions. With the help of simulations in MATLAB/SIMULINK environment, this research work tests the SRF PLL for unbalanced grid voltage. As it fails to track the phase angle properly during unbalanced conditions, the other advanced PLL schemes (DSRF PLL and SOGI based PLL) are tested for abnormal grid conditions. This project work concludes with a comparison of these two PLLs in terms of phase angle tracking for suitability of operation during abnormal grid conditions.

CHAPTER 2

Grid Synchronization Algorithm for Power Converters

2.1 INTRODUCTION:

The DG systems are highly intermittent power generation system and their power output depends heavily on the natural conditions. To connect the DG systems with the utility grid various grid code requirements must be met. But as DG system are fragile power generation systems and their characteristics are highly intermittent, power electronics converter plays a very vital role.

Whenever a DG system is required to be connected to the utility grid, two types of converter comes into picture. First is the Source-side converter which helps to ensure maximum power point tracking (MPPT) and the other is Grid-side converter which helps to maintain the grid connections standards.

The proper operation of grid connected inverter system is determined by grid voltage conditions such as phase, amplitude and frequency. In such applications, an accurate and fast detection of the phase angle, amplitude and frequency of the grid voltage is essential.

Various grid synchronization algorithms for phase tracking of the 3-phase system are proposed in literature, which are explained in brief in this chapter.

2.2. GRID CONNECTION REQUIREMENTS:

To investigate the dynamic behaviour of DG systems, the general grid code requirements are revisited in this section. Grid codes have been enforced for countries like USA, Germany, Spain, Denmark, China and Canada which have substantial generation. The major requirements of typical grid codes for operation and grid connection of DG systems are summarized as follows [13].

2.2.1 *Voltage regulation:*

This means by the connection of DG, the voltage at the PCC shall not go outside a specified range.

2.2.2 *System Frequency:*

Likewise, the frequency deviations shall also not go outside a specified range.

2.2.3 *Synchronization:*

While synchronizing a DG with an area electric power system (EPS) it shall not cause a voltage fluctuation of more than ± 5% of the prevailing voltage level at the PCC.

2.2.4 *Monitoring provisions:*

A DG system of rating 250 kW or larger shall have provisions for the monitoring of connection status and real and reactive power output at the point of DG connection.

2.2.5 *Isolation device*

Whenever required by area EPS operating practice, an isolation device shall be located between the DG unit and the area EPS.

2.2.6 *Grounding*

There should be a proper coordination among the grounding scheme and the grounding fault protection of DGs with the EPS operators.

2.2.7 *Voltage disturbances*

During any abnormal voltage condition, a DG shall cease to energize the EPS within a specified clearing time.

2.2.8 *Frequency disturbances*

Likewise, if the frequency is outside the normal range a DG shall cease to energize the EPS within a specified time.

2.2.9 *Loss of synchronization*

A DG of 250 kW or larger shall be equipped with loss of synchronism protection functions to disconnect the DG from the area EPS without intentional time delay.

2.2.10 *Reconnection*

After an out-of-bounds disturbance, a DG shall cease to energize the area EPS, and shall remain disconnected until the area EPS voltage and frequency have returned to and maintained normal ranges for 5 minutes.

2.2.11 *Anti-Islanding*

A DG shall detect the island condition and cease to energize the area EPS within 2 seconds of the formation of an island.

2.2.12 *Harmonics*

The allowable voltage harmonic distortion is specified at the PCC. It is normally required that the maximum voltage total harmonic distortion is 5**%** and maximum individual frequency voltage harmonic is 3% of the fundamental component.

2.2.13 *DC current injection*

A DG and its interconnection system shall not inject dc current greater than 0.5% of its rated output current into the area EPS at the PCC.

2.2.14 *Flicker*

A DG shall not create objectionable flicker for customers on the area EPS.

2.3. GRID SYNCHRONIZATION ALGORITHMS:

Few of the various grid synchronization algorithms that are proposed in literature are:-

2.3.1 *Zero Crossing Detector*

A zero crossing detector (ZCD) is a circuit that detects a transition of ac voltage from one polarity to another. Whenever a transition from positive to negative occurs a pulse is generated showing 0 degree and likewise 180 degree for the reverse case.

The performance of ZCD is badly affected by power quality phenomena [5].

2.3.2 *Phase Locked Loop*

A phase locked loop (PLL) is a system which synchronizes its output signal with a given input signal or reference signal both in frequency and in phase. It is a non-linear closed loop control which automatically changes the frequency of a controlled oscillator depending on the frequency and phase of the input signal such that the output is matched both in frequency and phase with the reference or the input signal.

The main components of a PLL are

i) A phase detector which compares the input/reference signal and the output signal and generates an error signal.

ii) A loop filter which removes unwanted harmonics terms from the error signal.

iii) A voltage controlled oscillator (VCO) which generates the output signal whose frequency varies around a central frequency depending on the output of the loop filter [5].

The block diagram of a PLL is shown below in Figure 2.1.

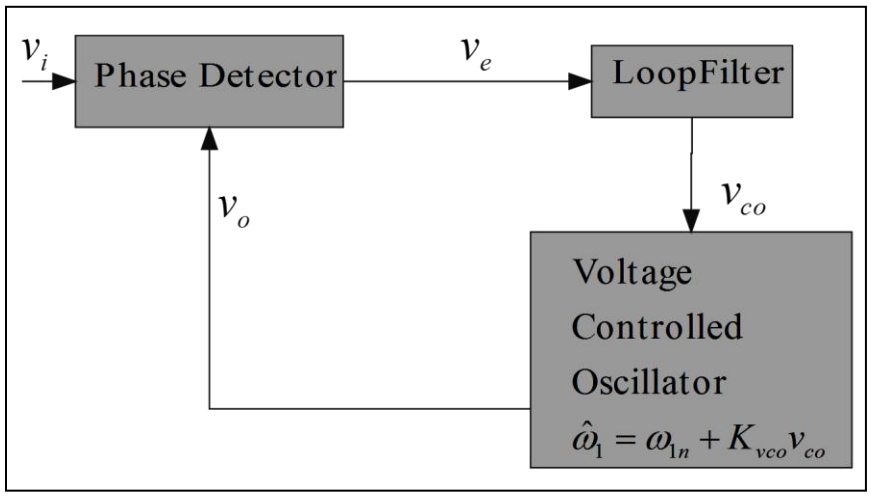


Figure 2.1: Block Diagram of a PLL

The various kinds of PLL techniques are:-

A. Linear PLL

Linear PLL (LPLL) is mainly used for single phase voltage. It has a mixer which is used as a phase differentiator which gives a signal proportional to the difference between the phases of the input and the output signal. This error signal also contains components at frequencies which are even multiples of the input frequency. The loop filter removes the harmonic components and only the proportional component is passed on to the voltage controlled oscillator according to which the VCO output is generated [5].

The whole model is shown by a block diagram in Figure 2.2.

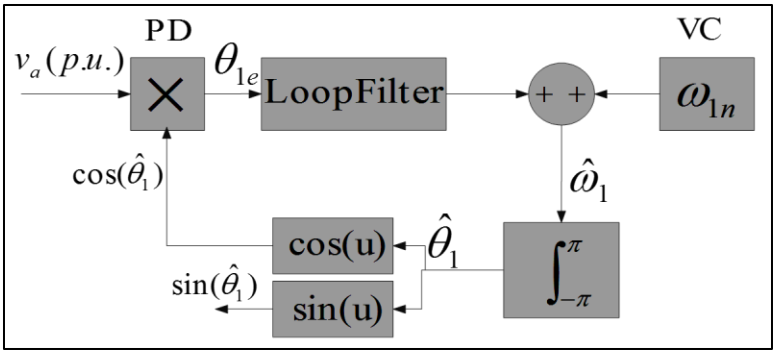


Figure 2.2: Block Diagram of a LPLL

The phase differentiator output is:-

$$v \times \underbrace{\cos(\hat{\theta}_1)}_{\text{Feedback wave}} = \frac{V_{1max}}{2} \times \left(\sin(\theta_1 - \hat{\theta}_1) + \sin(\theta_1 + \hat{\theta}_1)\right) + f(2\omega_i, 4\omega_i, 6\omega_i, \dots) \tag{2.1}$$

Now assuming that the PLL is locked in steady state $\omega_1 = \hat{\omega}_1$ and $\varphi_1 \approx \hat{\varphi}_1$

$$v \times \cos(\hat{\theta}_1) \approx \underbrace{\frac{V_{1max}}{2}\sin(\varphi_1 - \hat{\varphi}_1)}_{\approx \varphi_1 - \hat{\varphi}_1 = \theta_{1e}} + \underbrace{\frac{V_{1max}}{2}\sin(2\omega_1 t + 2\varphi_1)}_{\text{Generated Second harmonic}} + \underbrace{f(2\omega_i, 4\omega_i, 6\omega_i, \dots)}_{\text{Other harmonics}} \tag{2.2}$$

where v is the input signal, ω_1 is the input frequency, and the terms with (^) represent the output signal.

This equation shows that the result has information about the phase error along with some other harmonic components which are removed by the Loop Filter [5].

B. Synchronous Reference Frame PLL

A synchronous Reference Frame PLL (SRF PLL) is mainly used for tracking the phase angle in case of 3-phase signals which works in a similar way as a linear PLL with only difference in the Phase Detector (PD) block. It uses ***Park's Transformation*** of a 3-phase signal as the PD.

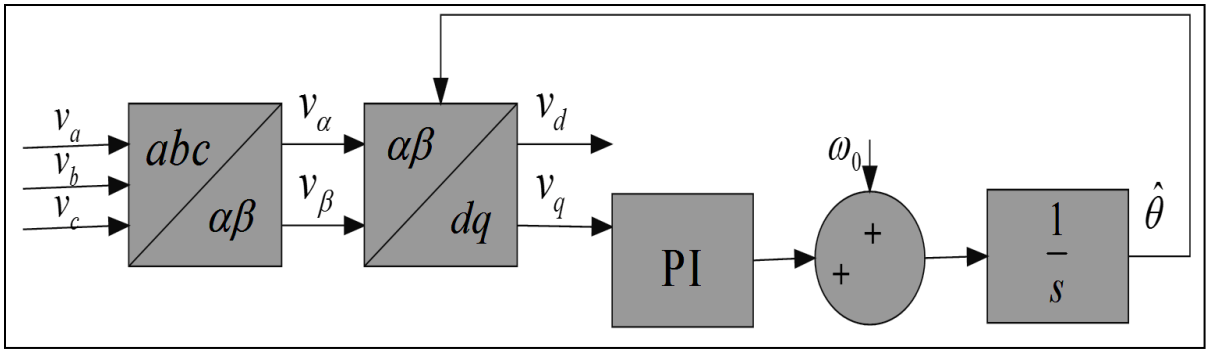


Figure 2.3: Block Diagram of a SRF PLL

Figure 2.3 shows the block diagram of a SRF PLL in which v_a, v_b, v_c are the components of a 3-phase signal. First block in the figure is ***Clarke's Transformation*** which translates a 3-phase voltage vector from the *abc* natural reference frame to the αβ stationary reference frame. The second block is the ***Park's Transformation*** which translates the αβ stationary reference frame to rotating frame. A ***Proportional Integrator (PI)*** controller is used as loop filter [5].

C. Double Synchronous Reference Frame (DSRF) PLL

The DSRF PLL is a combination of two conventional SRF PLLs. These two frames are separated by a synthesis circuit which is shown in figure 2.4. The voltage vector v is decomposed into positive and negative sequence vectors and these components are denoted by v_+ and v_- respectively as shown in figure 2.5. The block diagram of DSRF PLL, shown in figure 2.6 shows that the α and β axis components both contain the information of the positive sequence and negative sequence which makes it difficult to detect the positive sequence component. The two PLLs work independently, rotating with positive direction and negative direction respectively and detect the positive sequence and negative sequence simultaneously [6].

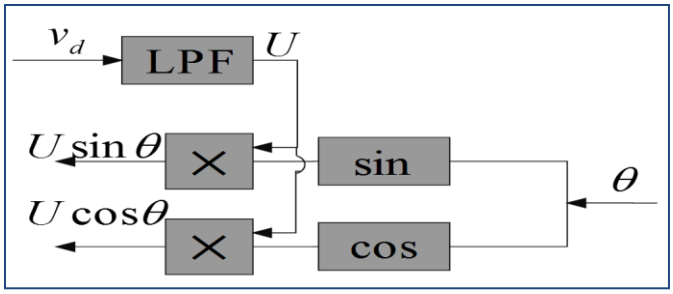


Figure 2.4: Synthesis Circuit used in DSRF PLL

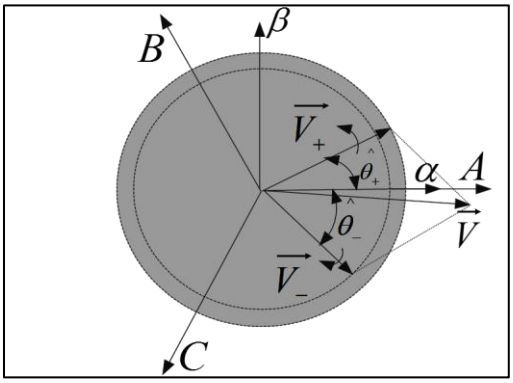


Figure 2.5: Voltage Vector Decomposition (Unbalanced Voltage)

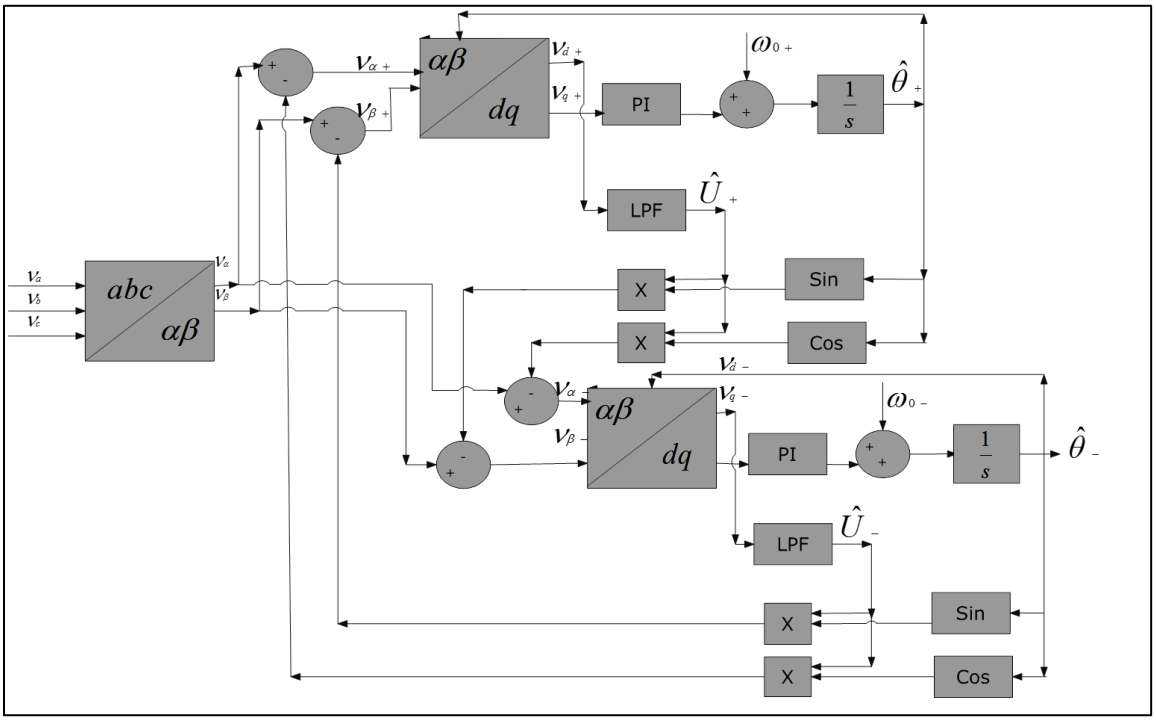


Figure 2.6: Block Diagram of DSRF PLL

D. Second Order Generalized Integrator (SOGI) based PLL

The PLL based on Second Order Generalized Integrator (SOGI) also separates and perfectly detects the phase angle of positive and negative sequence components but involves Quadrature Signal Generation (QSG) with the use of SOGI as shown in figure 2.7. Two SOGI based QSGs are used to obtain the in phase and quadrature components of the α axis (represented by v'_{α} and qv'_{α} respectively) and β axis (represented by v'_{β} and qv'_{β} respectively) voltages. The α and β axis voltages of the positive and negative sequence components so obtained are fed to two separate conventional SRF PLLs which separately obtain the d and q axis voltages of the two sequence components and hence the corresponding phase angles are properly detected. The block diagram of the algorithm is shown in figure 2.8 [9,10,14].

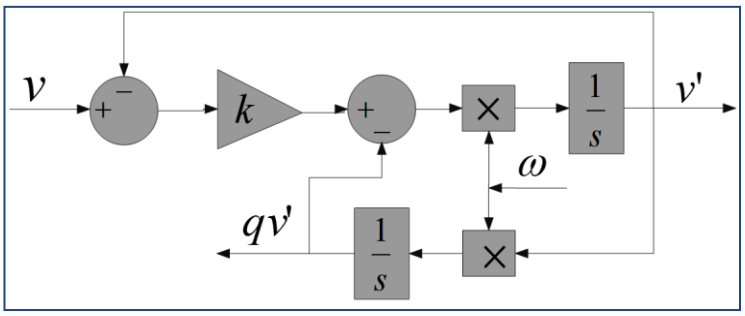


Figure 2.7: SOGI Based Quadrature Signal Generation (QSG)

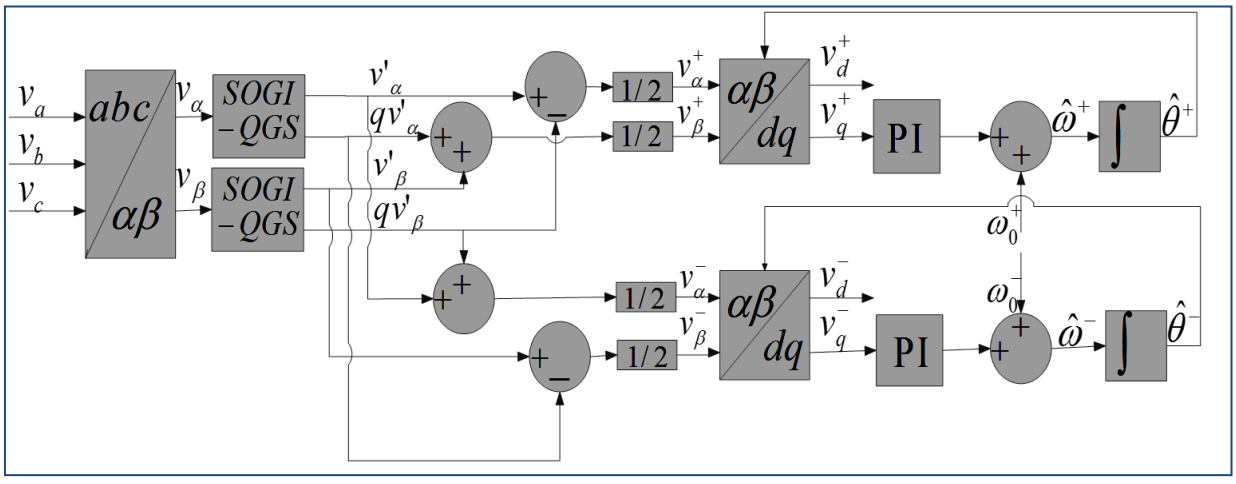


Figure 2.8: Block Diagram of SOGI based PLL

2.4 CONCLUSION:

The various grid synchronization algorithms have been studied. The earliest used phase detection method involves the concept of Zero Crossing Detector. The use of PLLs has shown better results for phase detection especially during grid abnormalities. Various kinds of PLL techniques are seen by their circuit models. The LPLL is mainly used for single phase synchronization while the SRF PLL is used to detect the phase angle in case of 3-phase system. The DSRF PLL and SOGI based PLL are used to decouple the positive and negative sequence components and to track the phase angle for both the sequence components separately. The mathematical model of the PLLs and the corresponding phase detection results as obtained from MATLAB/SIMULINK environment are shown in the further chapters for better understanding.

CHAPTER 3

Grid Synchronization using Double Synchronous Reference Frame (DSRF) PLL

3.1 INTRODUCTION:

The DSRF PLL, as described in section 2.3.2 (C), is a combination of two conventional SRF PLLs, separated by a synthesis circuit. It tracks the phase angle of the positive and the negative sequence separately. This chapter gives a detailed mathematical analysis of the DSRF PLL and its response to abnormal grid conditions. The chapter begins with the analysis of SRF PLL and its response to unbalanced grid voltages. It further explains how the conventional SRF fails to track the phase angle properly when the grid is under unbalanced conditions and illustrates the way in which DSRF PLL solves the problem by decoupling the positive and the negative sequence components.

3.2 ANALYSIS OF SYNCHRONOUS REFERENCE FRAME (SRF) PLL:

The SRF PLL explained in section 2.3.2(B) and showed in the figure 2.3 can be mathematically described by the following equations [6]:-

For a balanced 3-phase input, the d and q components can be obtained by the following relationship: -

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos(\hat{\theta}) & \sin(\hat{\theta}) \\ -\sin(\hat{\theta}) & \cos(\hat{\theta}) \end{bmatrix} \begin{bmatrix} U\cos\theta \\ U\sin\theta \end{bmatrix} = \begin{bmatrix} U\cos(\theta-\hat{\theta}) \\ U\sin(\theta-\hat{\theta}) \end{bmatrix} \quad (3.1)$$

where θ and $\hat{\theta}$ represent the phase of input signal and output of PLL respectively; U is the amplitude of input signal; v_d, v_q are the d- and q-axis components respectively.

Under unbalance utility conditions, the voltage vector can be expressed as:

$$v = v_+ + v_- + v_0 \quad (3.2)$$

where subscripts +, – and 0 define the vector for the positive, negative and zero sequence components.

Using Clarke's transformation, the voltage vector in the αβ plane is given by: -

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} U_+\cos(\theta_+) + U_-\cos(\theta_-) \\ U_+\sin(\theta_+) + U_-\sin(\theta_-) \end{bmatrix} \quad (3.3)$$

By Park's Transformation

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos(\hat{\theta}) & \sin(\hat{\theta}) \\ -\sin(\hat{\theta}) & \cos(\hat{\theta}) \end{bmatrix} \begin{bmatrix} U_+ \cos(\theta_+) + U_- \cos(\theta_-) \\ U_+ \sin(\theta_+) + U_- \sin(\theta_-) \end{bmatrix}$$

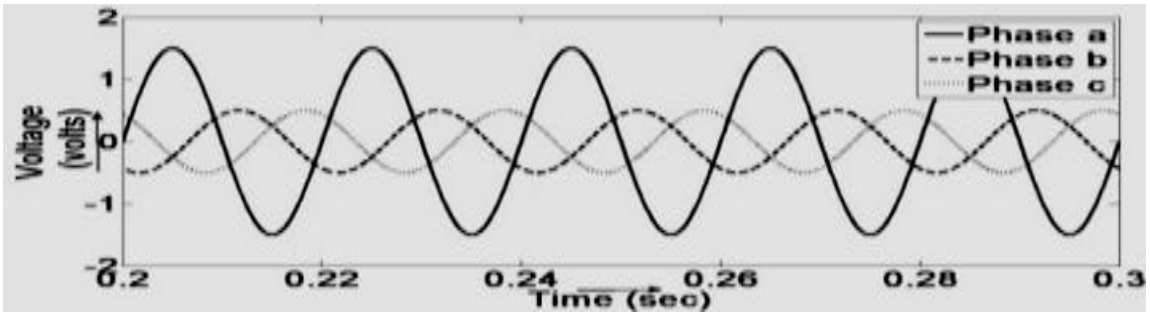
$$= \begin{bmatrix} U_+ \cos(\theta_+ - \hat{\theta}) + U_- \cos(\theta_- - \hat{\theta}) \\ U_+ \sin(\theta_+ - \hat{\theta}) + U_- \sin(\theta_- - \hat{\theta}) \end{bmatrix}$$

$$= \begin{bmatrix} U_+ + U_- \cos(2\omega t) \\ U_+ - U_- \sin(2\omega t) \end{bmatrix} \tag{3.4}$$

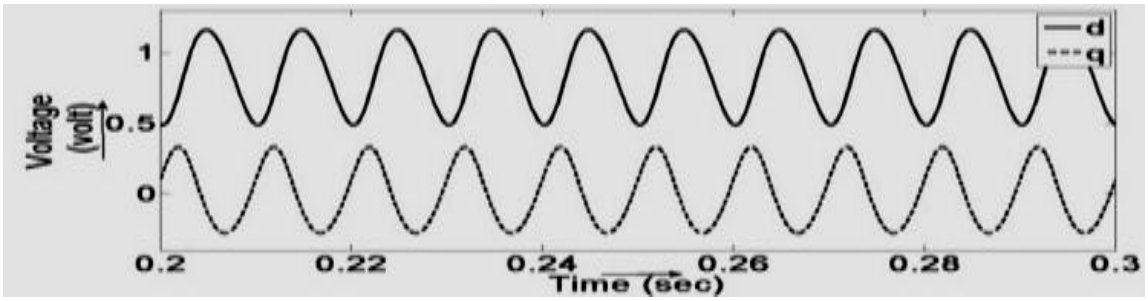
where ω is the angular frequency of voltage vector and $\hat{\theta} \approx \theta_+ = -\theta_- = \omega t$ in the steady state. So if the conventional SRF PLL is used during unbalanced grid conditions the second harmonic ripples are so high that makes it difficult to get the information of phase angle and amplitude.

The results obtained from simulation of SRF PLL during unbalanced grid voltage are shown in Fig. 3.1. Fig. 3.1 (a) shows the 3-phase unbalanced grid voltage such that phase a magnitude is greater than the other 2 phases. As described in equation 3.4, the d and q axis voltages are not constant, rather contains second harmonic ripples. Fig. 3.1 (b) shows these second harmonic components in d axis and q axis voltages. This sinusoidal nature in q axis voltage affects the output of PI controller and generates sinusoidal error signal and hence sinusoidal angular frequency (at central frequency ω_0 which is 100π in this case). This is shown in Fig. 3.1 (c). From Fig. 3.1 (d), it can be seen that, the detected phase obtained by the time integration of angular frequency is not perfectly triangular but rather contains sinusoidal variations. Thus it can be seen from the graph that SRF PLL fails to track the phase angle properly during unbalanced grid conditions.

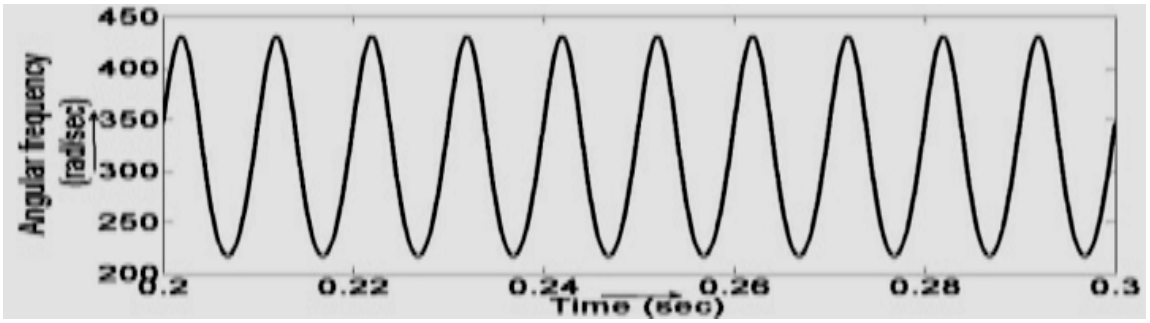
(a)



(b)



(c)



(d)

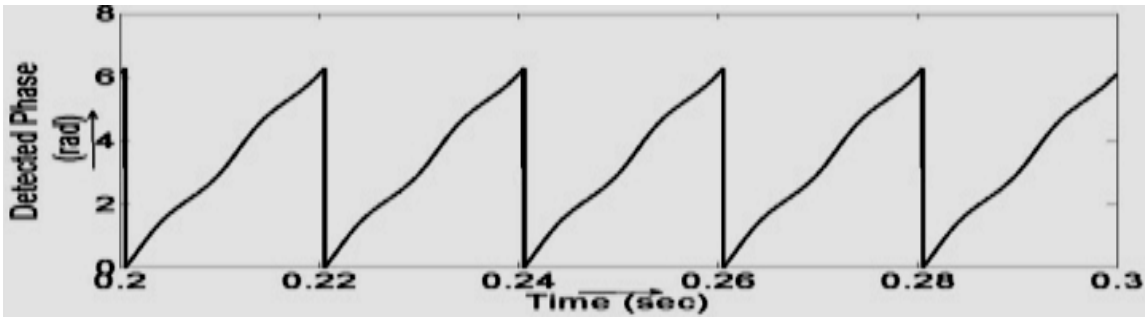


Figure 3.1: Simulation Results for SRF PLL during Unbalanced Grid Conditions (a) Grid Voltage Waveform (b) d-q Components of Grid Voltage (c) Detected Angular Frequency (d) Detected Phase Angle

3.3 ANALYSIS OF DOUBLE SYNCHRONOUS REFERENCE FRAME (DSRF) PLL:

In a DSRF PLL, as shown in figure 2.6, the d-axis component from the Park's transformation is fed to the synthesis circuit. This signal is actually the voltage amplitude in steady state. The synthesis circuit consists of a Low Pass Filter (L.P.F.), two multipliers, and two orthogonal trigonometric functions as shown in figure 2.4. The main objective of the orthogonal functions is to create orthogonal and in-phase signals with respect to the input signal, multiplying them with the amplitude. These signals are used as decoupling signals as shown in the figure 2.6. The two PLLs are required to detect the positive and negative sequence at the same time. The signals generated by the synthesis circuit are used as feedback for the unbalanced input signal. The input to the Park's transformation, v_α and $v_\beta$is the difference of actual v_α and $v_\beta$and the generated signals from the other PLL. As the process goes on the input to the PLL cleans up and the distortion at the output is cancelled. The positive sequence is detected by the PLL with ω_{0+} as the initial angular frequency and the negative sequence is detected by the one with ω_{0-}as the initial angular frequency. The detailed mathematical analysis is given below [6].

At initial state v_d= 0, $\hat{\theta}$ =$\omega_0 t$. Hence the output of the synthesis circuit is zero and decoupling circuit has no effect. Each PLL contains both positive and negative sequence information. In rotating reference frame, rotating with positive direction, the Park's transformation output is,

$$\begin{bmatrix} v_{d+} \\ v_{q+} \end{bmatrix} = U_+ \begin{bmatrix} \cos(\theta_+ - \hat{\theta}_+) \\ \sin(\theta_+ - \hat{\theta}_+) \end{bmatrix} + U_- \begin{bmatrix} \cos(\theta_- - \hat{\theta}_+) \\ \sin(\theta_- - \hat{\theta}_+) \end{bmatrix} \tag{3.5}$$

$\hat{\theta}_+ = \omega_{0+} t$ at initial state, which is the approximate center angular frequency of positive sequence component. Then (3.5) becomes

$$\begin{bmatrix} v_{d+} \\ v_{q+} \end{bmatrix} = \begin{bmatrix} U_+ + U_- \cos(-2\omega_{0+} t) \\ U_- \sin(-2\omega_{0+} t) \end{bmatrix} \tag{3.6}$$

As it can be seen, there are some 2ω ripples in the *d*-axis component which is attenuated using a low pass filter. This makes the PLL more stable. The LPF is defined as

$$LPF(s) = \frac{\omega_c}{s+\omega_c} \tag{3.7}$$

where $\omega_c$is the cut off frequency of the LPF.

The PLL behaviour is analysed by using state variable model. The state equations can be derived as (taking 2 state variables, $x_1$and x_2 as the state vectors):-

$$\begin{cases}\dot{x}_1 = \omega_c(U_+ - \mathcal{X}_1 + (U_- - x_2)\cos(\theta_+ - \theta_-)) \\ \dot{x}_2 = \omega_c(U_- - \mathcal{X}_2 + (U_+ - x_1)\cos(\theta_+ - \theta_-))\end{cases} \tag{3.8}$$

where$\begin{cases}\dot{x}_1 = \widehat{U}_+ \\ \dot{x}_2 = \widehat{U}_-\end{cases}$

At steady state $x_1 = U_+$and$x_2 = U_-$. This implies that the *d*- axis component will converge to input voltage vector amplitude after sometime, and the decoupling of signals by the synthesis circuit begins.

So each PLL input will be:

$$\begin{cases}v_{\alpha+} = v_\alpha - U_- \cos\theta_- = U_+ \cos\theta_+ \\ v_{\beta+} = v_\beta - U_- \sin\theta_- = U_+ \sin\theta_+\end{cases} \tag{3.9}$$

and

$$\begin{cases}v_{\alpha-} = v_\alpha - U_+ \cos\theta_+ = U_- \cos\theta_- \\ v_{\beta-} = v_\beta - U_+ \sin\theta_+ = U_- \sin\theta_-\end{cases} \tag{3.10}$$

Thus it can be seen that at steady state the two sequence components are perfectly decoupled and hence the PLL can perfectly track the phase angle for both the sequence components even in unbalanced grid conditions.

3.4 SIMULATION RESULTS AND DISCUSSIONS:

The Simulink Model for DSRF PLL as described by equations (3.5) to (3.10) is shown in figure 3.2.

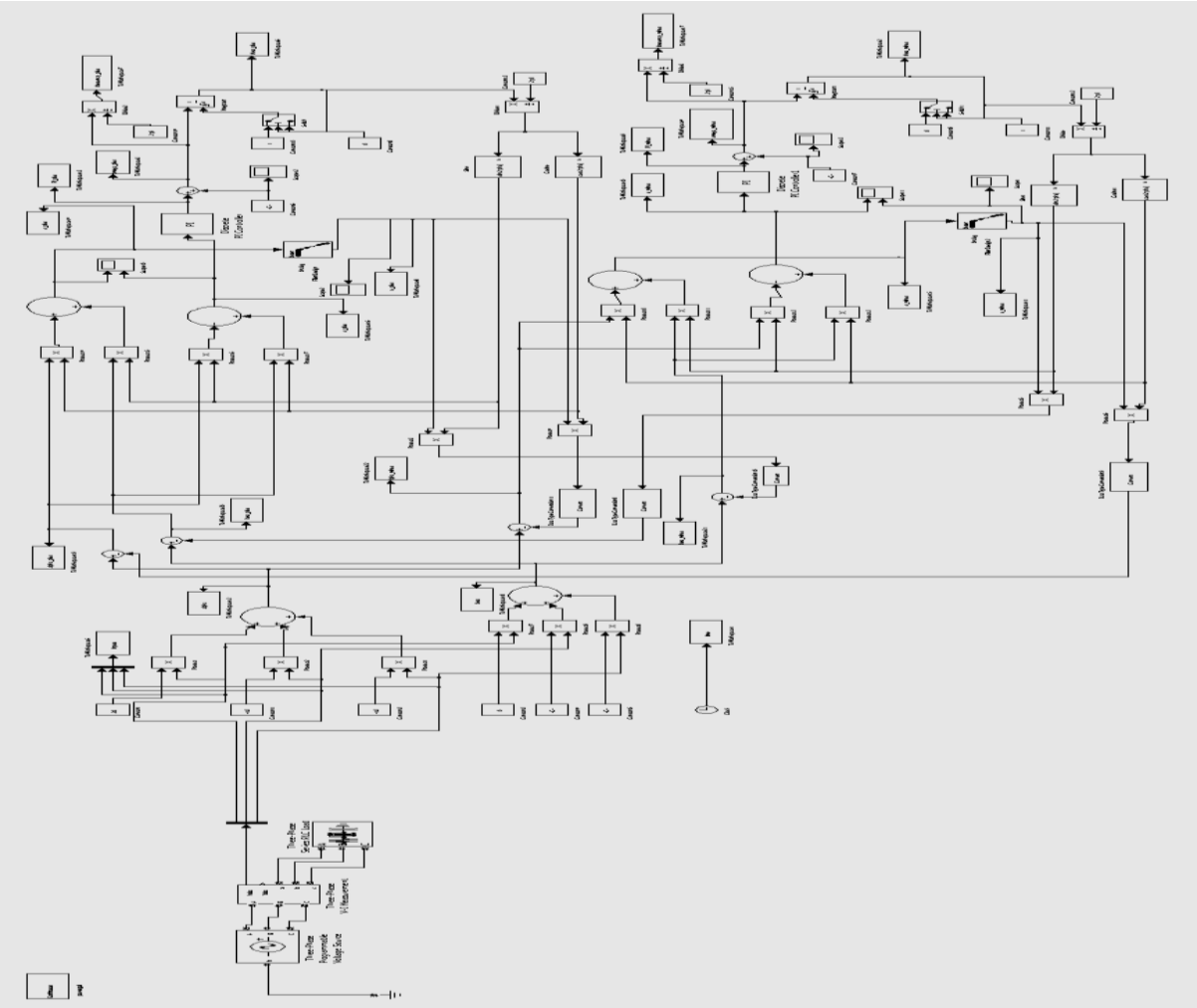


Figure 3.2: Simulink Model of a DSRF PLL

The MATLAB/SIMULINK results obtained for DSRF PLL under various abnormal grid conditions are discussed in this section.

3.4.1 *Dynamic Response of DSRF PLL During Unbalanced Grid Voltages*

The dynamic responses obtained from simulation for DSRF PLL during unbalance grid voltage are shown in Fig. 3.3. The PI tuning used for these results are K_p=67.5 and K_i=100.

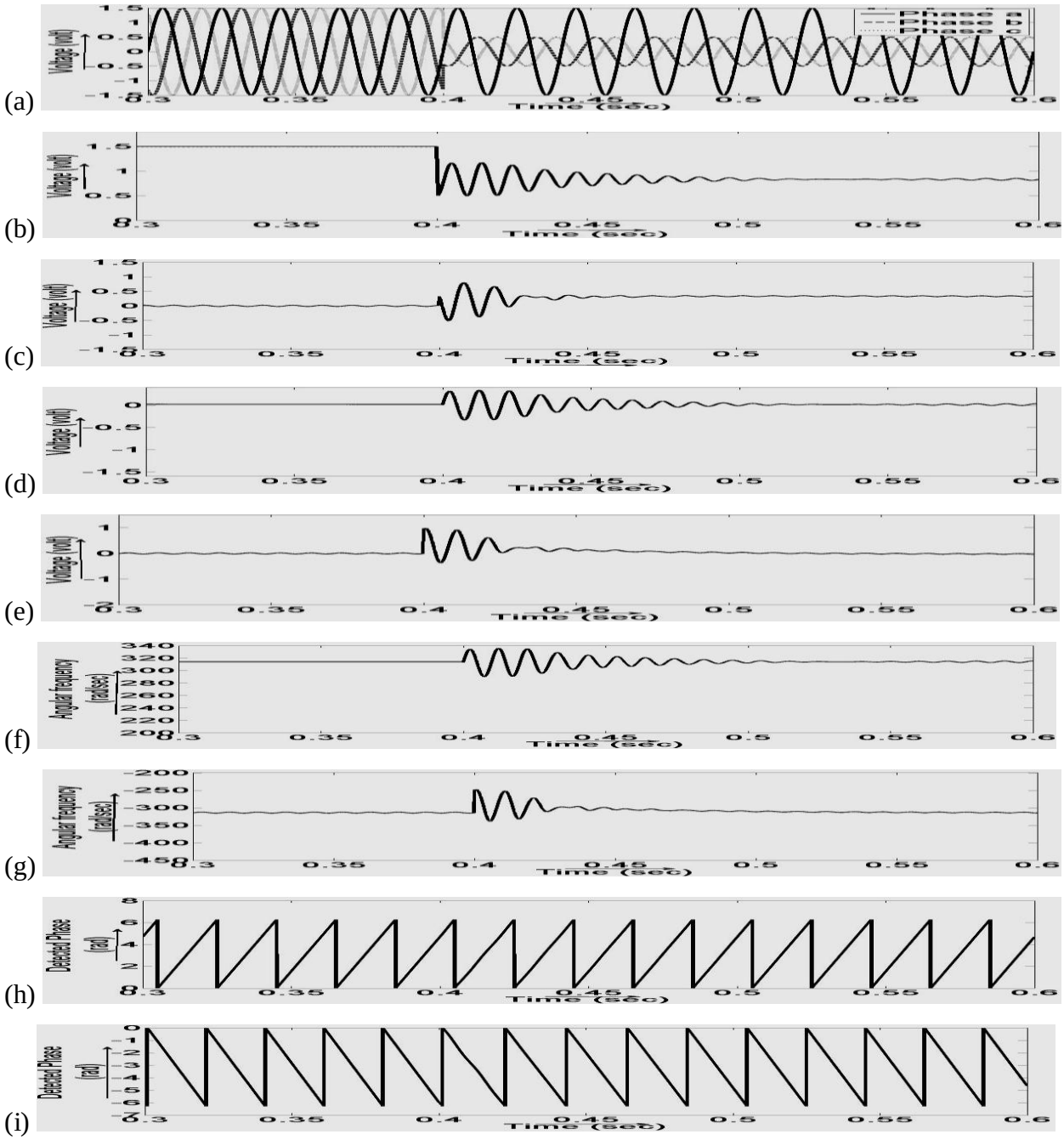


Figure 3.3: Dynamic Response of DSRF PLL during Unbalanced Grid Conditions (a) Grid Voltage Waveforms (b) d axis Voltage of Positive Sequence Component (c) d axis Voltage of Negative Sequence Component (d) q axis Voltage of Positive Sequence Component (e) q axis Voltage of Negative Sequence Component (f) Detected Angular Frequency of Positive Sequence Component (g) Detected Angular Frequency of Negative Sequence Component (h) Detected Phase Angle of Positive Sequence Component (i) Detected Phase Angle of Negative Sequence Component

Fig. 3.3 (a) shows a 3-phase signal which is balanced upto time t=0.4 sec and then voltage amplitude of 2 of the phases reduces to 0.5 from their initial value of 1.5. With this kind of input the dynamic responses are observed.

The positive and negative sequence components are separately observed in case of DSRF PLL. As shown in Fig. 3.3 (b) d axis voltage of positive sequence component is almost constant both during balanced and unbalanced period and negligible sinusoidal variations are observed during the transient period (from t=0.4 to 0.5 sec). Similarly as shown in Fig. 3.3 (c) the d axis voltage of negative sequence component is also almost constant having negligible variations. As shown is Fig. 3.3 (d) the q axis voltage of the positive sequence component maintains a constant value both in balanced and unbalanced conditions. The transients are observed when there is sudden change in input voltage (at t=0.4 sec). The transient vanishes to give a nearly constant value (nearly at zero) for q axis voltage of positive sequence component. A similar nature is observed for q axis voltage of negative sequence component as can be seen in Fig. 3.3 (e).

The angular frequencies of positive and negative sequence components are both similar to their respective q axis voltages and hence a nearly constant angular frequency is observed for positive and negative sequence components (Fig. 3.3 (f) and Fig. 3.3 (g) respectively). For these constant angular frequencies we observe perfectly triangular phase angle detection for positive sequence (Fig. 3.3 (h)) and negative sequence (Fig. 3.3 (i)). The detected phase angle varies linearly every cycle from 0 to 2π for positive sequence and 0 to -2π for negative sequence.

3.4.2 *Response of DSRF PLL Under Line to Ground Fault*

The results obtained from simulation of DSRF PLL under line to ground fault are shown in Fig. 3.4. The PI tuning used for these results are K_p=67.5 and K_i=100.

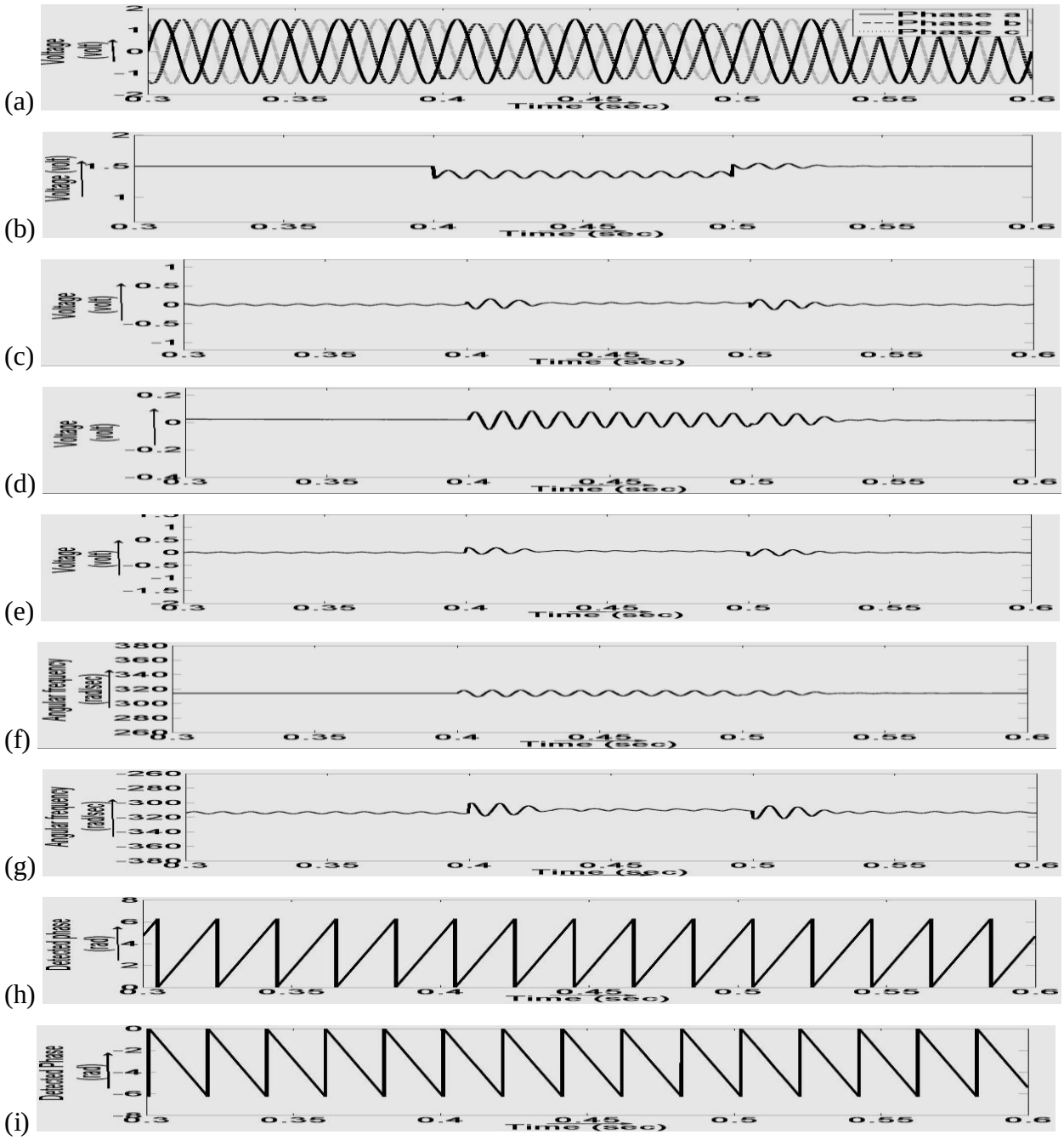


Figure 3.4: Response of DSRF PLL under Line to Ground Fault (a) Grid Voltage Waveforms (b) d axis Voltage of Positive Sequence Component (c) d axis Voltage of Negative Sequence Component (d) q axis Voltage of Positive Sequence Component (e) q axis Voltage of Negative Sequence Component (f) Detected Angular Frequency of Positive Sequence Component (g) Detected Angular Frequency of Negative Sequence Component (h) Detected Phase Angle of Positive Sequence Component (i) Detected Phase Angle of Negative Sequence Component

Fig. 3.4 (a) shows the voltage waveform when line to ground fault occurs. The system was initially in balanced condition (having amplitude 1.5V). Line to ground fault occurs at time, t = 0.4sec. At this instant the phase voltage of 2 of the phases reduces and remains at an amplitude of 1.3V. The system regains its balanced state at time, t = 0.5 sec. The d axis voltage of positive sequence component shown in Fig. 3.4 (b) is constant at the amplitude of the signals during balanced input. During line to ground fault, the d axis voltage reduces and some oscillations with very small amplitude are observed. The d axis voltage of negative sequence component (Fig. 3.4 (c)) also maintains its constant value other than very small transients that occur at time t = 0.4 sec and 0.5 sec. The q axis voltages of positive sequence (Fig. 3.4 (d)) and negative sequence (Fig. 3.4 (e)) maintains their near zero value at all instants, with some oscillations at the instants when switching of voltages occur. The angular frequencies of positive sequence and negative sequence components maintain their constant value at 100π and -100π (Fig. 3.4 (f) and Fig. 3.4 (g) respectively).Therefore the detected phase angle is perfectly triangular for both positive (Fig. 3.4 (h)) and negative sequence (Fig. 3.4 (i)).

3.4.3 *Response of DSRF PLL During Voltage Sag*

The simulation results obtained for DSRF PLL during voltage sag are shown in Fig. 3.5. The PI tuning used for these results are K_p=67.5 and K_i=100.

As shown in Fig. 3.5(a), voltage sag occurs at time t = 0.3 sec when all the three phase voltages reduces to 0.45V from their initial voltage of 0.5V. The three phases regain their original value of 0.5V at time t = 0.4 sec. This kind of sudden reduction in voltage for small period (2 and half cycles in this case) is known as voltage sag. Fig. 3.5 (b) illustrates the d axis voltage of positive sequence component, which is constant at the amplitude of the input signal. In the duration when voltage sag occurs, the d axis voltage remains constant but its value changes to the new amplitude. Similarly as shown in Fig. 3.5 (c) the d axis voltage of negative sequence component also maintains its constant zero value. The q axis voltage of positive sequence component remains constant at a value very close to zero and some slight transients are observed at the time of switching (Fig. 3.5 (d)). The same holds good for q axis voltage of negative sequence component which remains constant at zero in both the periods (Fig. 3.5 (e)). As q axis voltages are constant the corresponding angular frequency for both positive and negative components maintains their constant value at 100π and -100π (Fig. 3.5 (f) and Fig. 3.5

(g)).The detected phase for both the sequence components is perfectly triangular because of the constant angular frequency observed (Fig. 3.5 (h) and Fig. 3.5 (i)).

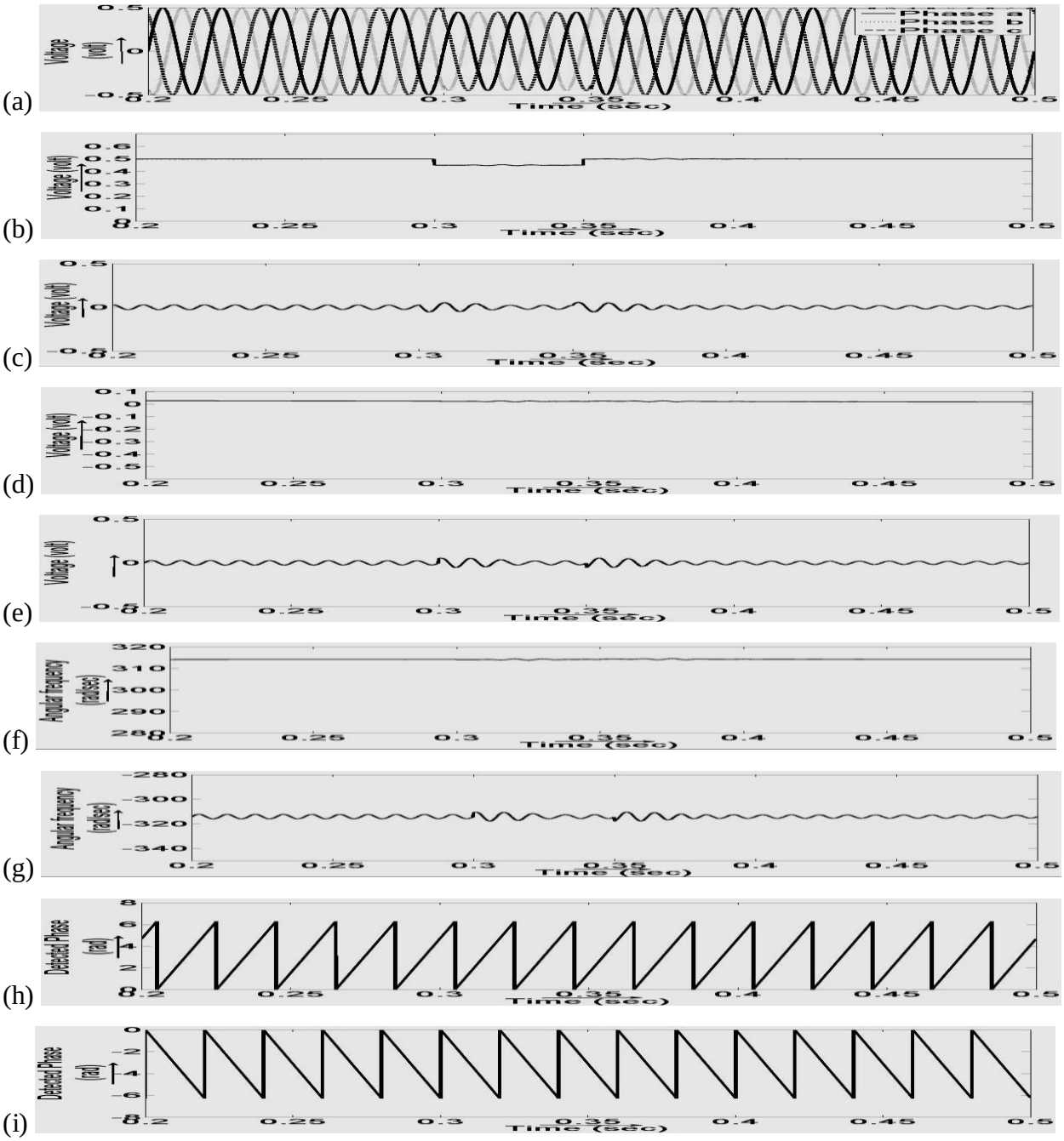


Figure 3.5: Response of DSRF PLL during Voltage Sag (a) Grid Voltage Waveforms (b) d axis Voltage of Positive Sequence Component (c) d axis Voltage of Negative Sequence Component (d) q axis Voltage of Positive Sequence Component (e) q axis Voltage of Negative Sequence Component (f) Detected Angular Frequency of Positive Sequence Component (g) Detected Angular Frequency of Negative Sequence Component (h) Detected Phase Angle of Positive Sequence Component (i) Detected Phase Angle of Negative Sequence Component

3.4.4 *Response of DSRF PLL During Frequency Deviation*

The simulation results obtained for DSRF PLL during frequency deviation are shown in Fig. 3.6. The PI tuning used for these results are K_p=67.5 and K_i=100.

As shown in Fig. 3.6(a), frequency deviation occurs at time t = 0.3 sec when the frequency of the 3-phase voltage changes to 52 Hz from its initial value of 50Hz. Fig. 3.6 (b) illustrates the d axis voltage of positive sequence component, which is constant at the amplitude of the input signal (=0.8V). Whenever frequency deviation occurs, the d axis voltage deviates slightly but still remains constant at almost the same value i.e. 0.8V. Similarly as shown in Fig. 3.6 (c) the d axis voltage of negative sequence component also maintains its constant zero value but some slight oscillations are obtained when frequency deviation occurs. The q axis voltage of positive sequence component remains constant at a value very close to zero and increases slightly as frequency is increased (Fig. 3.6 (d)). The q axis voltage of negative sequence component also remains at almost zero volt both before and after the frequency deviation occurs, but contains some oscillations which increases as soon as the frequency deviates (Fig. 3.6 (e)). Similar characteristics are reflected in the corresponding angular frequencies for both positive (Fig. 3.6 (f)) and negative (Fig. 3.6 (g)) components; the positive sequence angular frequency changes from 100π to 104π. The detected phase for both the sequence components is perfectly triangular because of the constant angular frequency observed with a very small reduction in the time period corresponding to the slight change in the frequency (Fig. 3.6 (h) and Fig. 3.6 (i)).

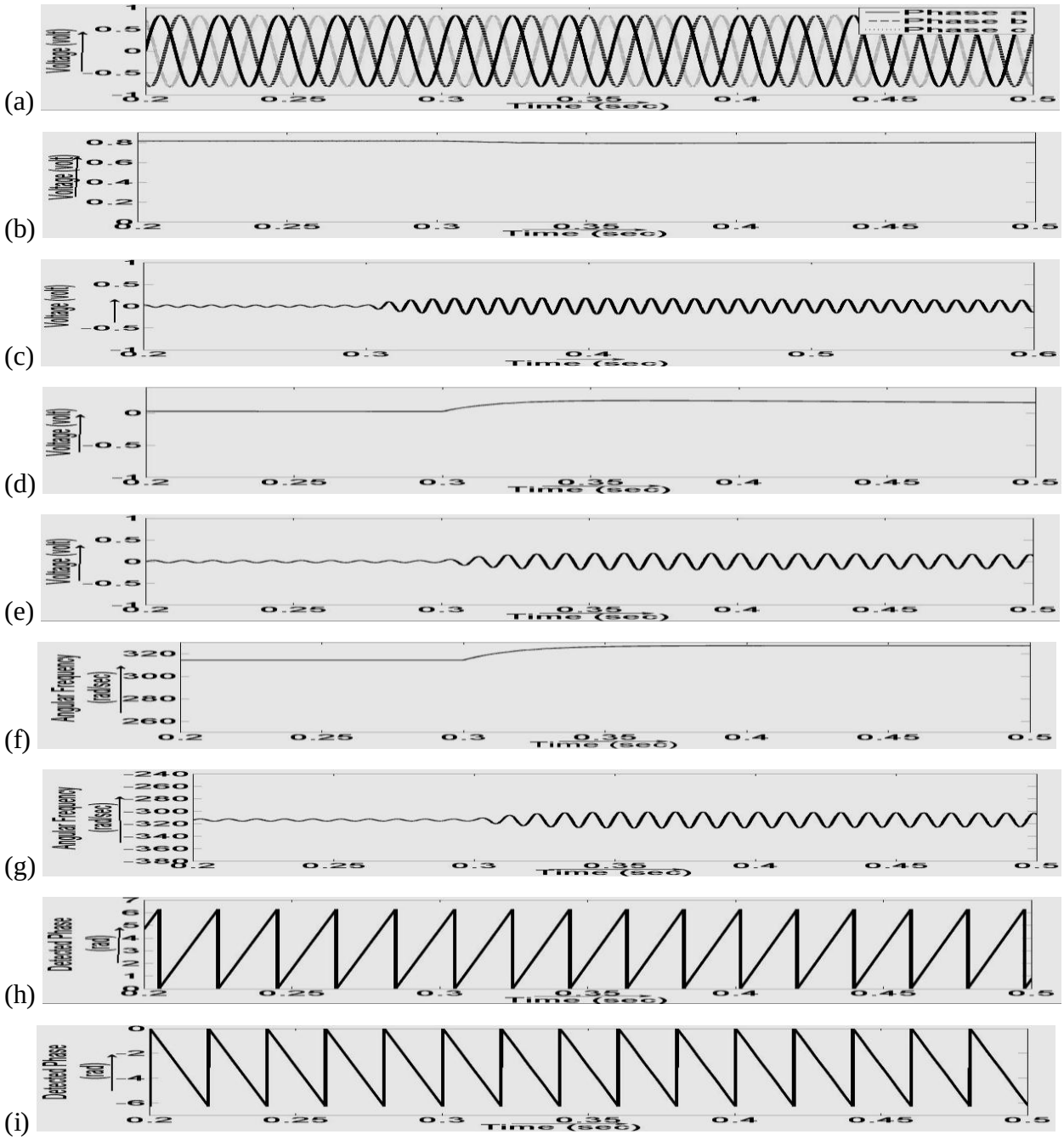


Figure 3.6: Response of DSRF PLL during Frequency Deviation (a) Grid Voltage Waveforms (b) d axis Voltage of Positive Sequence Component (c) d axis Voltage of Negative Sequence Component (d) q axis Voltage of Positive Sequence Component (e) q axis Voltage of Negative Sequence Component (f) Detected Angular Frequency of Positive Sequence Component (g) Detected Angular Frequency of Negative Sequence Component (h) Detected Phase Angle of Positive Sequence Component (i) Detected Phase Angle of Negative Sequence Component

3.4.5 *Response of DSRF PLL During Voltage Flicker*

The simulation results obtained for DSRF PLL during voltage flicker are shown in Fig. 3.7. The PI tuning used for these results are K_p=67.5 and K_i=100.

As shown in Fig. 3.7(a), voltage flicker occurs at time t = 0.3 sec when the balanced 3-phase voltage having magnitude 0.5V becomes unbalanced. The magnitude of all three phases increases but not by same amount. The unbalance remains for a period of 0.05 sec, after which the system regains its balanced state. Fig. 3.7 (b) illustrates the d axis voltage of positive sequence component, which is constant at the amplitude of the input signal (=0.5V). During flicker as the magnitude of all 3-phases increases; the d axis voltage also increases and regains its original value of 0.5V; after a small transient period when the system becomes balanced again. Similarly as shown in Fig. 3.7 (c) the d axis voltage of negative sequence component also maintains its constant zero value but some slight oscillations are obtained when flicker occurs. The q axis voltage of positive sequence component remains constant at a value very close to zero but shows certain oscillations during the unbalanced state (Fig. 3.7 (d)). The q axis voltage of negative sequence component also remains at almost zero volt both before and after the flicker as well as during the flicker but with slight transient at the instant when voltage changes. It consists of oscillations which are constant in magnitude even in steady state (Fig. 3.7 (e)). Similar characteristics are reflected in the corresponding angular frequencies for both positive (Fig. 3.7 (f)) and negative (Fig. 3.7 (g)) components; the positive sequence angular frequency remains constant at 100π while the negative sequence angular frequency remains constant at -100π. The oscillations in angular frequencies are similar to that in corresponding q axis voltage. The detected phase for both the sequence components is perfectly triangular, changing from 0 to 2π in each cycle, because of the constant angular frequencies observed (Fig. 3.7 (h) and Fig. 3.7 (i)).

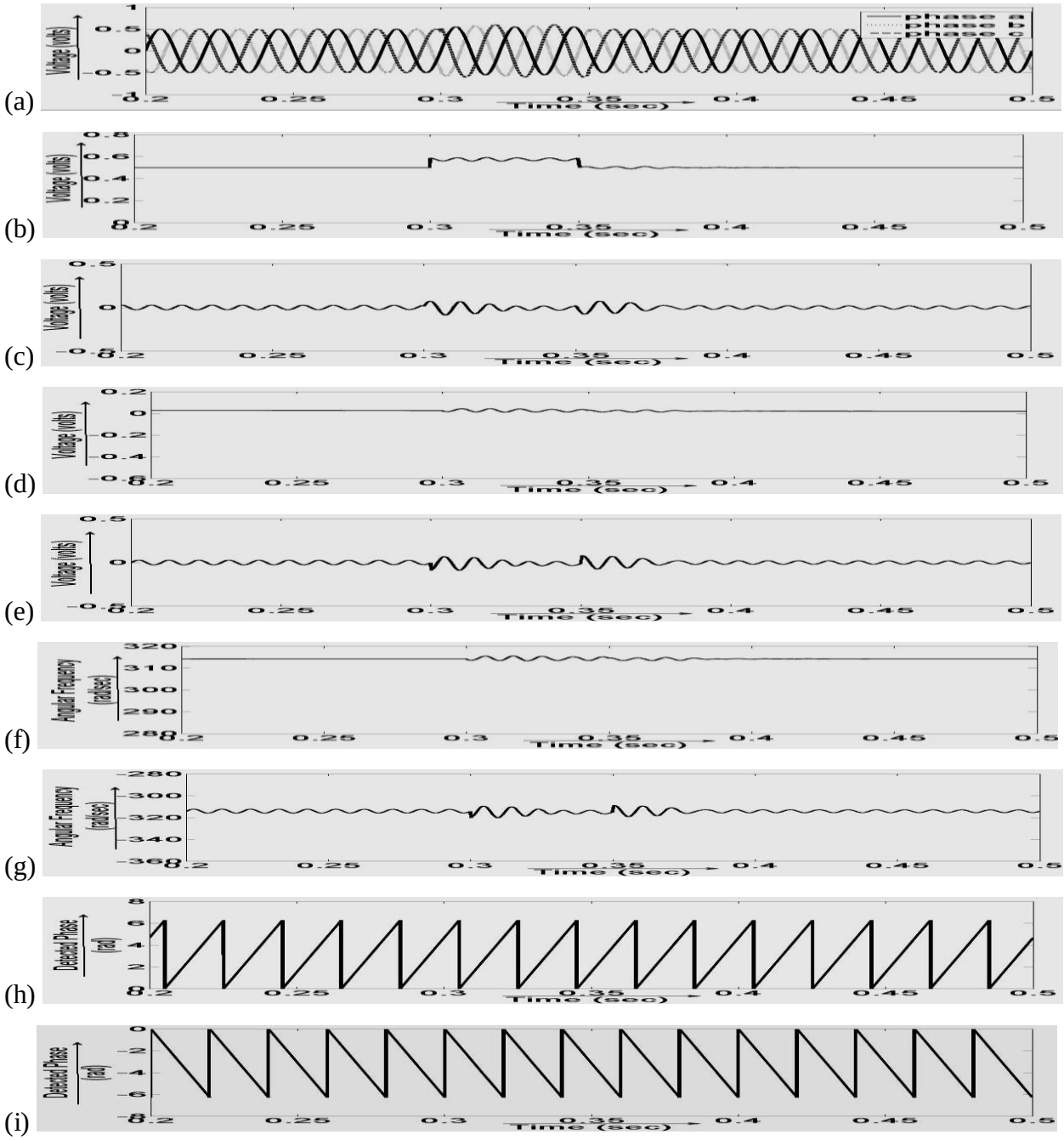


Figure 3.7: Response of DSRF PLL during Voltage Flicker (a) Grid Voltage Waveforms (b) d axis Voltage of Positive Sequence Component (c) d axis Voltage of Negative Sequence Component (d) q axis Voltage of Positive Sequence Component (e) q axis Voltage of Negative Sequence Component (f) Detected Angular Frequency of Positive Sequence Component (g) Detected Angular Frequency of Negative Sequence Component (h) Detected Phase Angle of Positive Sequence Component (i) Detected Phase Angle of Negative Sequence Component

3.4.6 *Response of DSRF PLL During Harmonic Injection*

The simulation results obtained for DSRF PLL during harmonic injection are shown in Fig. 3.8. The PI tuning used for these results are K_p=67.5 and K_i=100.

Fig. 3.8(a) shows a balanced 3-phase voltage having a magnitude of 1V to which 5^{th} and 7^{th} harmonics are injected at time t = 0.3 sec and the 3-phase voltage becomes distorted. Fig. 3.8 (b) illustrates the d axis voltage of positive sequence component, which is constant at the amplitude of the input signal (=1V) but due to the presence of harmonics in the systems after 0.3 sec, the d axis voltage shows some oscillations as different frequency components comes into picture during Clarke's transformation and Park's transformation. Similarly as shown in Fig. 3.8 (c) the d axis voltage of negative sequence component also maintains its constant zero value but the consistent oscillations increases as the voltage becomes distorted. The q axis voltage of positive sequence component remains constant at a value very close to zero but shows consistent oscillations due to the presence of more than 1 frequency components (Fig. 3.8 (d)). The q axis voltage of negative sequence component also remains almost at zero volt but the oscillations increases as the harmonics are injected because the voltage is now affected by more than 1 frequency components. (Fig. 3.8 (e)). Similar characteristics are reflected in the corresponding angular frequencies for both positive (Fig. 3.8 (f)) and negative (Fig. 3.8 (g)) sequence components; the positive sequence angular frequency oscillates about 100π while the negative sequence angular frequency oscillates about -100π. This is because the fundamental frequency has the maximum amplitude, which leads to the constant values of 100π and -100π respectively in the detected angular frequencies and the remaining frequency components causes the oscillations. The detected phase for both the sequence components is perfectly triangular, changing from 0 to 2π in each cycle, because of the dominant fundamental angular frequencies and the integration of the harmonics due to the remaining frequencies does not lay much effect on the detected phase (Fig. 3.8 (h) and Fig. 3.8 (i)).

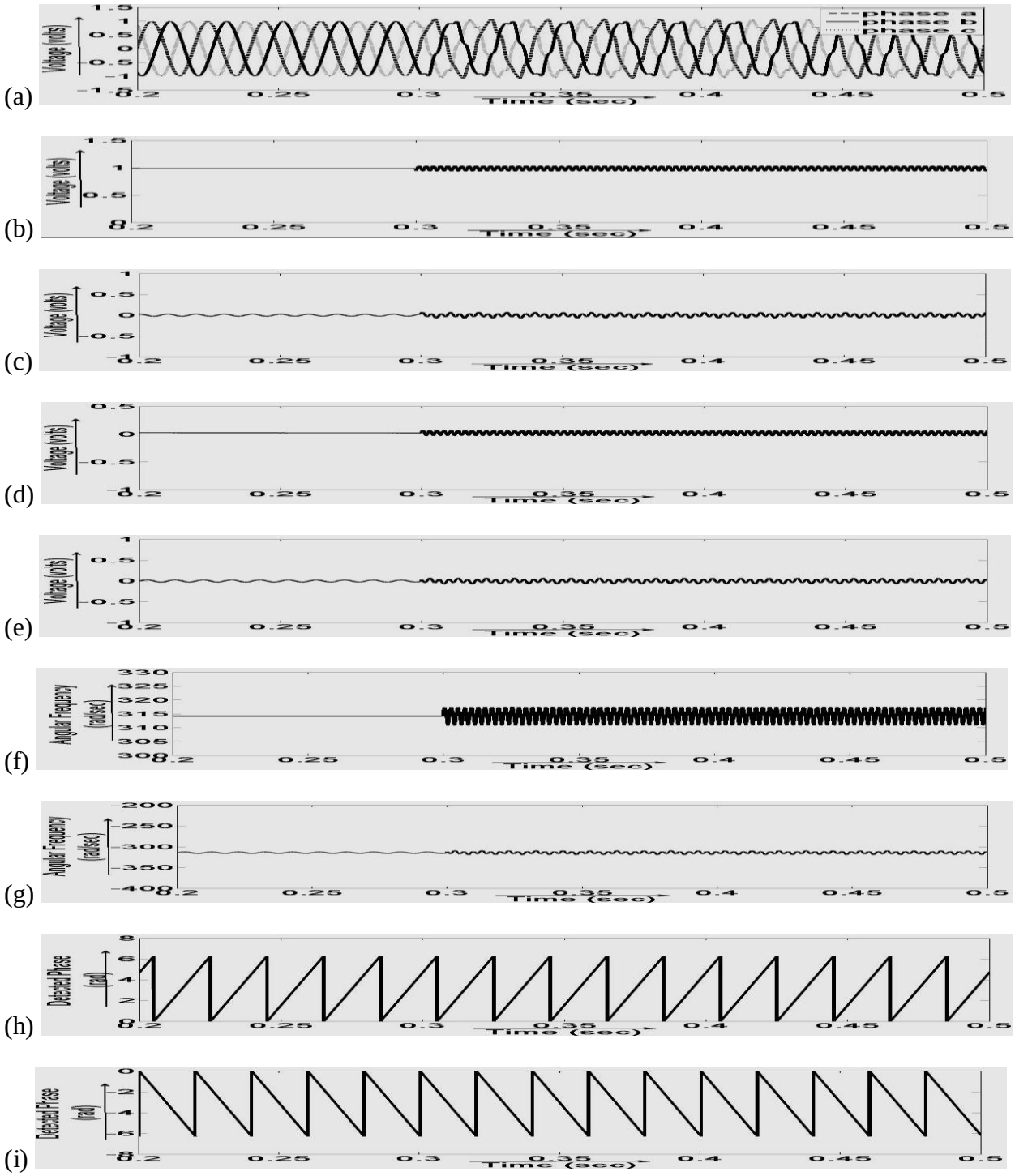


Figure 3.8: Response of DSRF PLL during Harmonic Injection (a) Grid Voltage Waveforms (b) d axis Voltage of Positive Sequence Component (c) d axis Voltage of Negative Sequence Component (d) q axis Voltage of Positive Sequence Component (e) q axis Voltage of Negative Sequence Component (f) Detected Angular Frequency of Positive Sequence Component (g) Detected Angular Frequency of Negative Sequence Component (h) Detected Phase Angle of Positive Sequence Component (i) Detected Phase Angle of Negative Sequence Component

3.4.7 *Response of DSRF PLL During Voltage Dip*

The simulation results obtained for DSRF PLL during voltage dip are shown in Fig. 3.9. The PI tuning used for these results are K_p=67.5 and K_i=100.

As shown in Fig. 3.9 (a), voltage dip occurs at time t = 0.3 sec when the balanced 3-phase voltage having magnitude 0.5V becomes unbalanced. The magnitude of phases becomes 0.45, 0.475 and 0.55V. The unbalance remains for a period of 0.05 sec, after which the system regains its balanced state. This kind of power quality problem is called voltage dip. Fig. 3.9 (b) illustrates the d axis voltage of positive sequence component, which is constant at the amplitude of the input signal (=0.5V). During dip as the magnitude of all three phases changes; the d axis voltage oscillates and regains its original value of 0.5V; after a small transient period when the system becomes balanced again. Similarly as shown in Fig. 3.9 (c) the d axis voltage of negative sequence component also maintains its constant zero value but some slight oscillations are obtained when dip occurs. The q axis voltage of positive sequence component remains constant at a value very close to zero but shows certain oscillations during the unbalanced state (Fig. 3.9 (d)). The q axis voltage of negative sequence component also remains at almost zero volt both before and after the dip as well as during the voltage dip but with slight transient at the instant when voltage changes. The q axis voltage consists of oscillations which are constant in magnitude even in steady state (Fig. 3.9 (e)). Similar characteristics are reflected in the corresponding angular frequencies for both positive (Fig. 3.9 (f)) and negative (Fig. 3.9 (g)) sequence components; the positive sequence angular frequency remains at 100π while the negative sequence angular frequency remains constant at -100π. The oscillations in angular frequencies are similar to that in corresponding q axis voltage. The detected phase for both the sequence components is perfectly triangular, changing from 0 to 2π in each cycle, because of the constant angular frequencies observed (Fig. 3.9 (h) and Fig. 3.9 (i)).

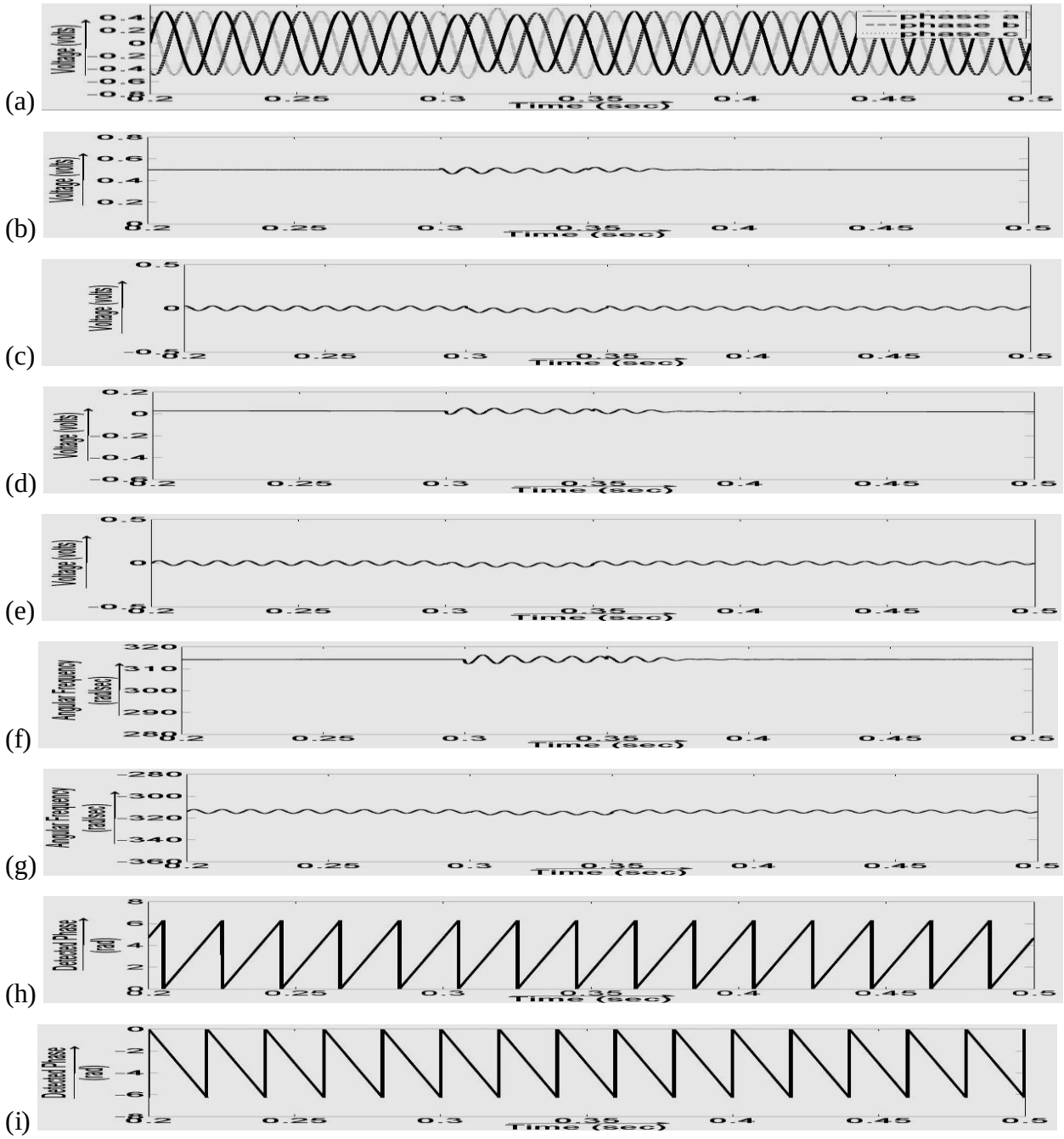


Figure 3.9: Response of DSRF PLL during Voltage Dip (a) Grid Voltage Waveforms (b) d axis Voltage of Positive Sequence Component (c) d axis Voltage of Negative Sequence Component (d) q axis Voltage of Positive Sequence Component (e) q axis Voltage of Negative Sequence Component (f) Detected Angular Frequency of Positive Sequence Component (g) Detected Angular Frequency of Negative Sequence Component (h) Detected Phase Angle of Positive Sequence Component (i) Detected Phase Angle of Negative Sequence Component

3.4. CONCLUSION:

The chapter presents the performance of Double Synchronous Reference Frame (DSRF) PLL for phase detection under abnormal grid conditions and power quality problems. The abnormal grid conditions include line to ground fault and the various quality problems include voltage unbalance, voltage sag, frequency deviation, voltage flicker, harmonic injection and voltage dip. From the above discussions, one can observe that, the studied DSRF PLL can accurately detect the phase irrespective of the grid conditions. Moreover, the DSRF PLL can also decouple the positive and negative sequence components of grid voltages in order to ensure sinusoidal current injection into the grid. Further, the obtained results clearly show that the DSRF PLL gives better response to track the positive sequence component over conventional SRF PLL which fails to track the phase angle whenever there is an unbalance in the grid

CHAPTER 4

Analysis of Second Order Generalized Integrator (SOGI) based PLL

4.1 INTRODUCTION:

A brief introduction to the SOGI based PLL has already been mentioned in section 2.3.2(D). The detailed mathematical analysis of this PLL has been done in this chapter. The response of this PLL is studied for different abnormal grid conditions like line to ground fault and power quality problems such as voltage sag, frequency deviations, harmonic injection, voltage flicker and voltage dip. With the help of these results the perfect tracking of phase angle by SOGI based PLL is shown and explained. After this, the response of this PLL is compared with that of DSRF PLL. This comparative study well illustrates the superiority of SOGI based PLL over DSRF PLL.

4.2 ANALYSIS OF SECOND ORDER GENERALIZED INTEGRATOR(SOGI) BASED PLL:

The SOGI based PLL is shown in figure 2.7. As can be seen, the α and β axis voltages of the positive and negative sequence components so obtained are fed to two separate conventional SRF PLLs which separately obtain the d and q axis voltages of the two sequence components and hence the corresponding phase angles are properly detected. The decoupling of alpha and beta voltages into positive and negative sequences is done with the help of SOGI, as can be seen in figure 2.7.

The α and β axis voltages for positive and negative sequence components are calculated by the following equations [9,15]:

$$\begin{cases} v_{\alpha+} = \frac{1}{2} \times (v'_{\alpha} - qv'_{\beta}) \\ v_{\beta+} = \frac{1}{2} \times (qv'_{\alpha} + v'_{\beta}) \end{cases} \tag{4.1}$$

$$\begin{cases} v_{\alpha-} = \frac{1}{2} \times (v'_{\alpha} + qv'_{\beta}) \\ v_{\beta-} = \frac{1}{2} \times (-qv'_{\alpha} + v'_{\beta}) \end{cases} \tag{4.2}$$

The d and q axis voltages of positive sequence components are given by (4.3).

$$\begin{bmatrix} v_{d+} \\ v_{q+} \end{bmatrix} = \begin{bmatrix} \cos(\hat{\theta}_+) & \sin(\hat{\theta}_+) \\ -\sin(\hat{\theta}_+) & \cos(\hat{\theta}_+) \end{bmatrix} \begin{bmatrix} U_+ \cos(\theta_+) \\ U_+ \sin(\theta_+) \end{bmatrix}$$

$$= \begin{bmatrix} U_+ \cos(\theta_+ - \hat{\theta}_+) \\ U_+ \sin(\theta_+ - \hat{\theta}_+) \end{bmatrix} \tag{4.3}$$

Same relationship holds good for negative sequence.

After this the positive and negative sequence alpha and beta components are operated in similar way as SRF PLL and the positive and negative sequence phase angles are tracked separately. Hence SOGI based PLL can track the phase angle perfectly even for unbalanced grid.

4.3 SIMULATION RESULTS AND DISCUSSIONS:

The Simulink Model for SOGI based PLL as described by equations (4.1) to (4.3) is shown in figure 4.1.

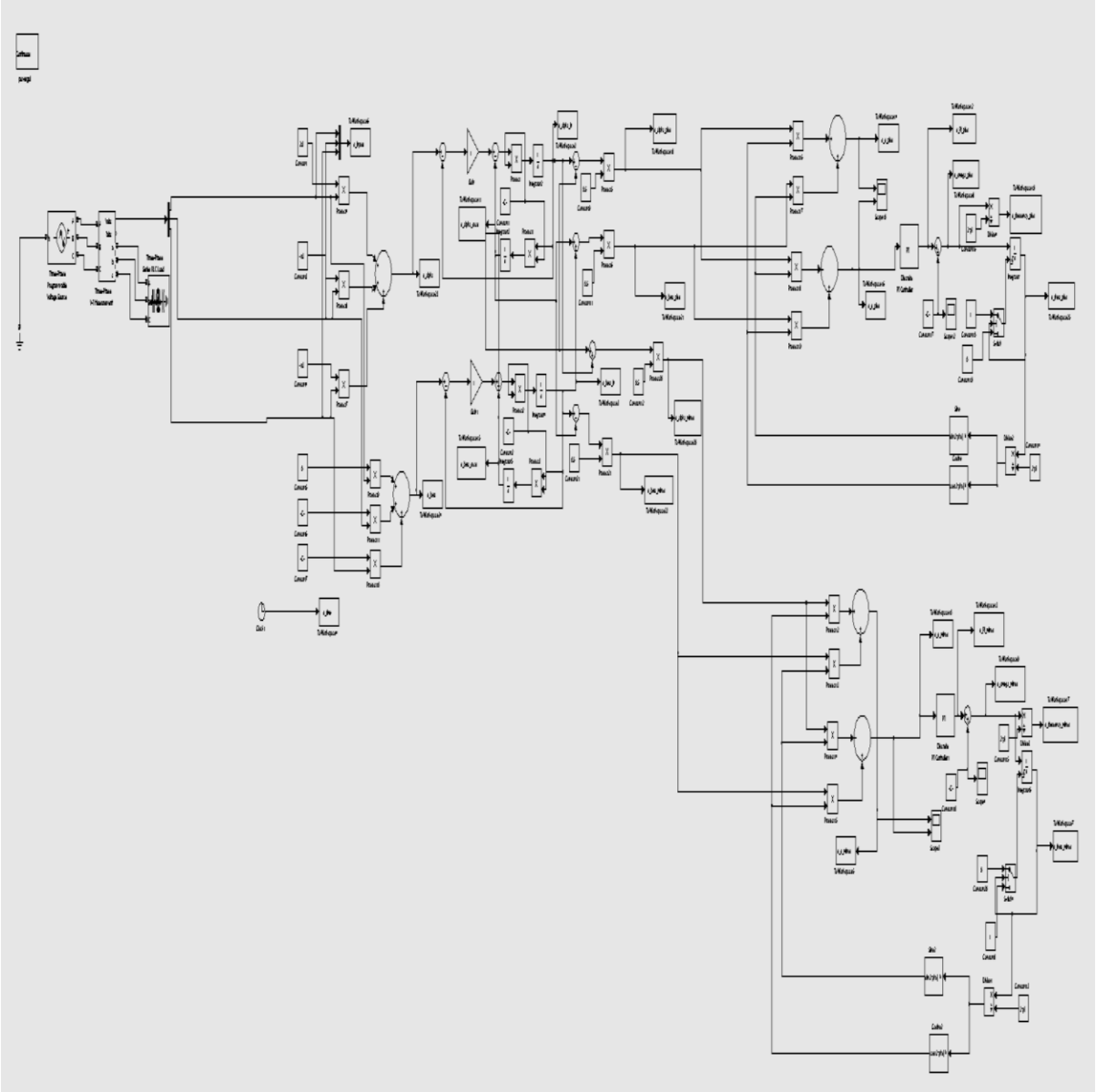
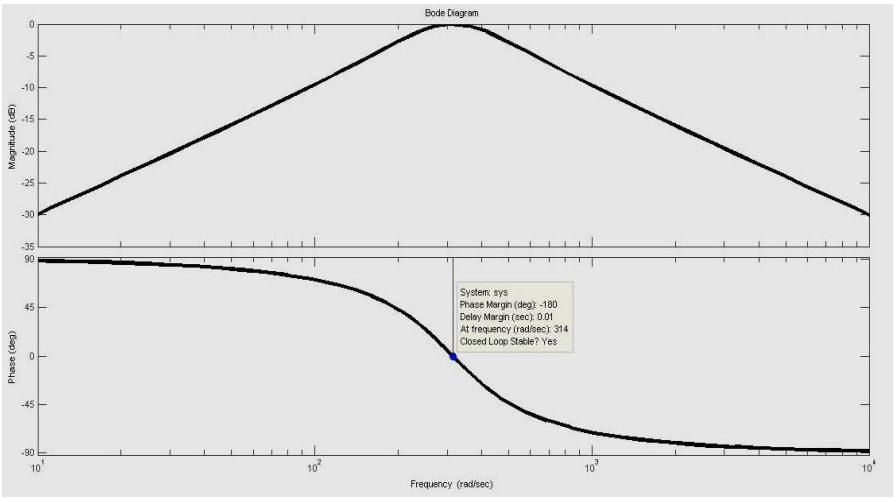


Figure 4.1: Simulink Model of SOGI based PLL

The frequency response for the SOGI was obtained from the transfer function obtained in [10] as shown in figure 4.2.

As can be seen from the Bode plots, the two systems i.e. for the in phase output (shown in figure 4.2 (a)) and for the quadrature phase output (shown in figure 4.2 (b)), are closed loop stable.

(a)



(b)

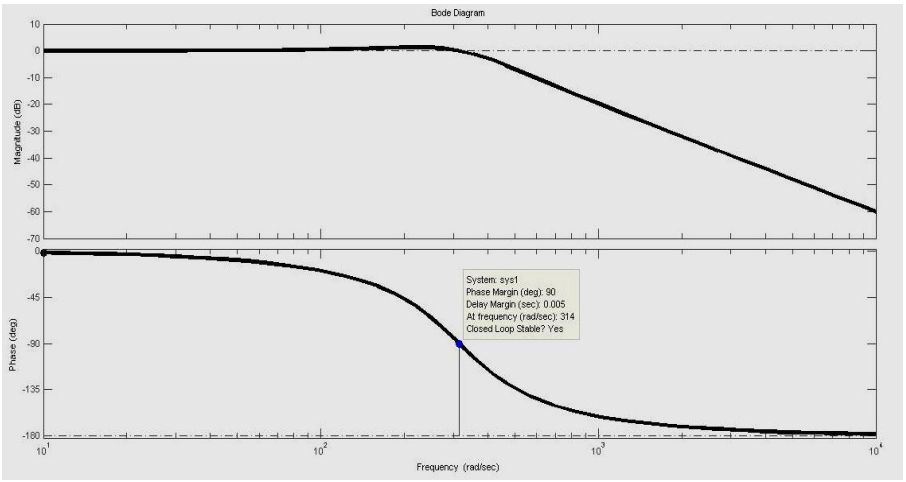


Figure 4.2: Frequency Response for SOGI-QSG (a) Bode Plot for In Phase Component (b) Bode Plot for Quadrature Component

The MATLAB/SIMULINK results obtained for SOGI based PLL under various abnormal grid conditions are discussed in this section.

4.3.1 Response of SOGI based PLL Under Line to Ground Fault:

The responses obtained from simulation for SOGI based PLL under line to ground fault are shown in Fig. 4.3. The PI tuning used for these results are K_p=67.5 and K_i=100. The gain for QSG was taken as 1.

Fig. 4.3(a) shows a 3-phase signal which is balanced up to time t=0.4 sec and then voltage amplitude of two of the phases reduces to 1 from their initial value of 1.5. With this kind of input the dynamic responses are observed.

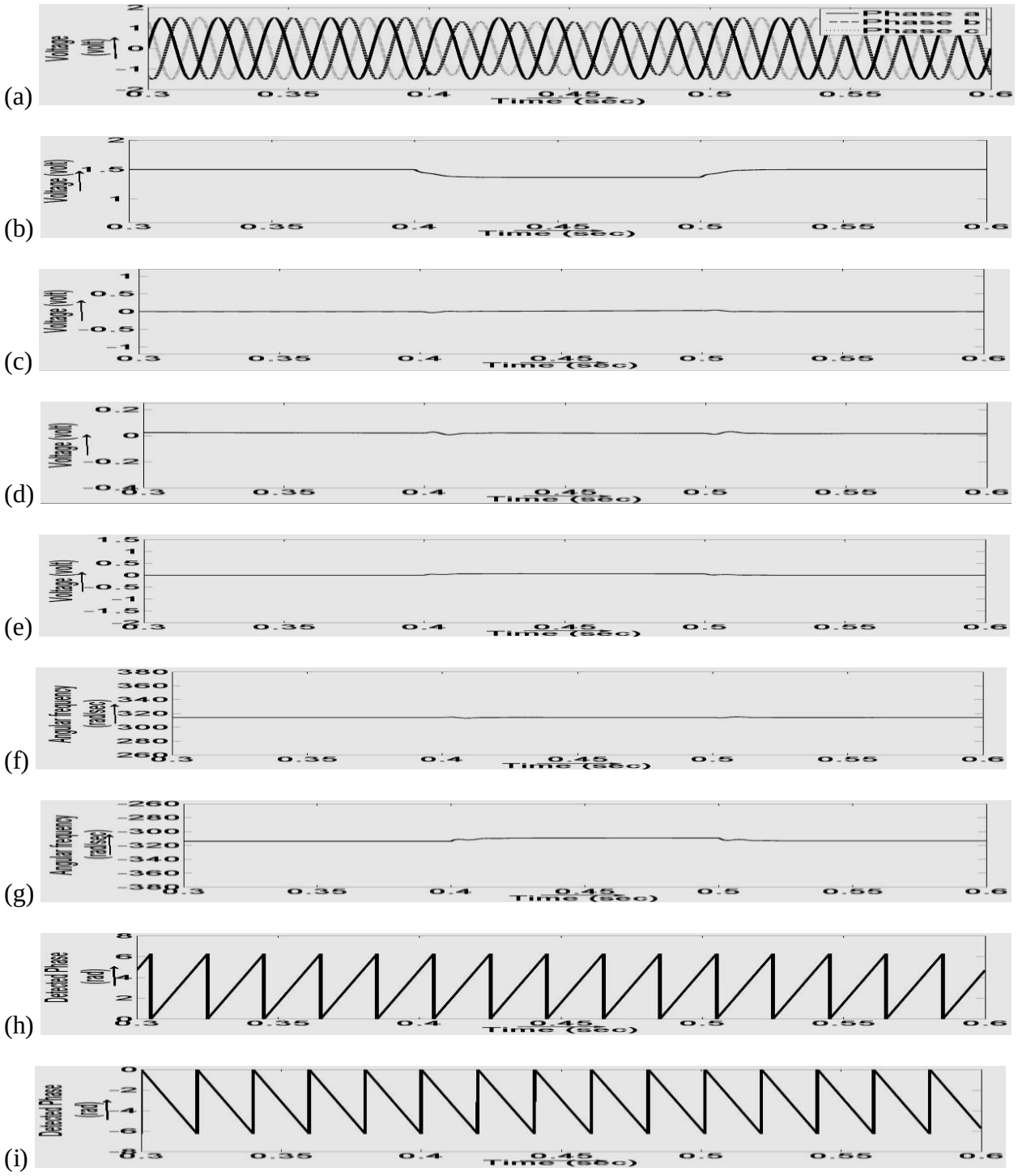


Figure 4.3: Response of SOGI based PLL under Line To Ground Fault (a) Grid Voltage Waveforms (b) d axis Voltage of Positive Sequence Component (c) d axis Voltage of Negative Sequence Component (d) q axis Voltage of Positive Sequence Component (e) q axis Voltage of Negative Sequence Component (f) Detected Angular Frequency of Positive Sequence Component (g) Detected Angular Frequency of Negative Sequence Component (h) Detected Phase Angle of Positive Sequence Component (i) Detected Phase Angle of Negative Sequence Component

The positive and negative sequence components are separately observed in case of SOGI based PLL. As shown in Fig. 4.3(b), d axis voltage of positive sequence component is almost constant except during the fault period when the voltage level decreases a bit through transient response. Similarly as shown in Fig. 4.3(c) the d axis voltage of negative sequence component is also almost constant having negligible variations at the beginning and end of the fault. As shown is Fig. 4.3(d) the q axis voltage of the positive sequence component maintains a constant value throughout except the fault period when instantaneous transients are obtained at the two ends. A similar nature is observed for q axis voltage for negative sequence component as can be seen in Fig. 4.3(e).

The angular frequencies of positive and negative sequence components are both similar to their respective q axis voltages and hence a nearly constant angular frequency is observed for positive and negative sequence components (Fig. 4.3(f) and Fig. 4.3(g) respectively). For these constant angular frequencies we observe perfectly triangular phase angle detection for positive sequence (Fig. 4.3(h)) and negative sequence (Fig. 4.3(i)). The detected phase angle varies linearly every cycle from 0 to 2π for positive sequence and 0 to -2π for negative sequence.

4.3.2 Response of SOGI based PLL During Frequency Deviation:

The responses obtained from simulation for SOGI based PLL during frequency deviation are shown in Fig. 4.4. The PI tuning used for these results are K_p=67.5 and K_i=100. The gain for QSG was taken as 1.

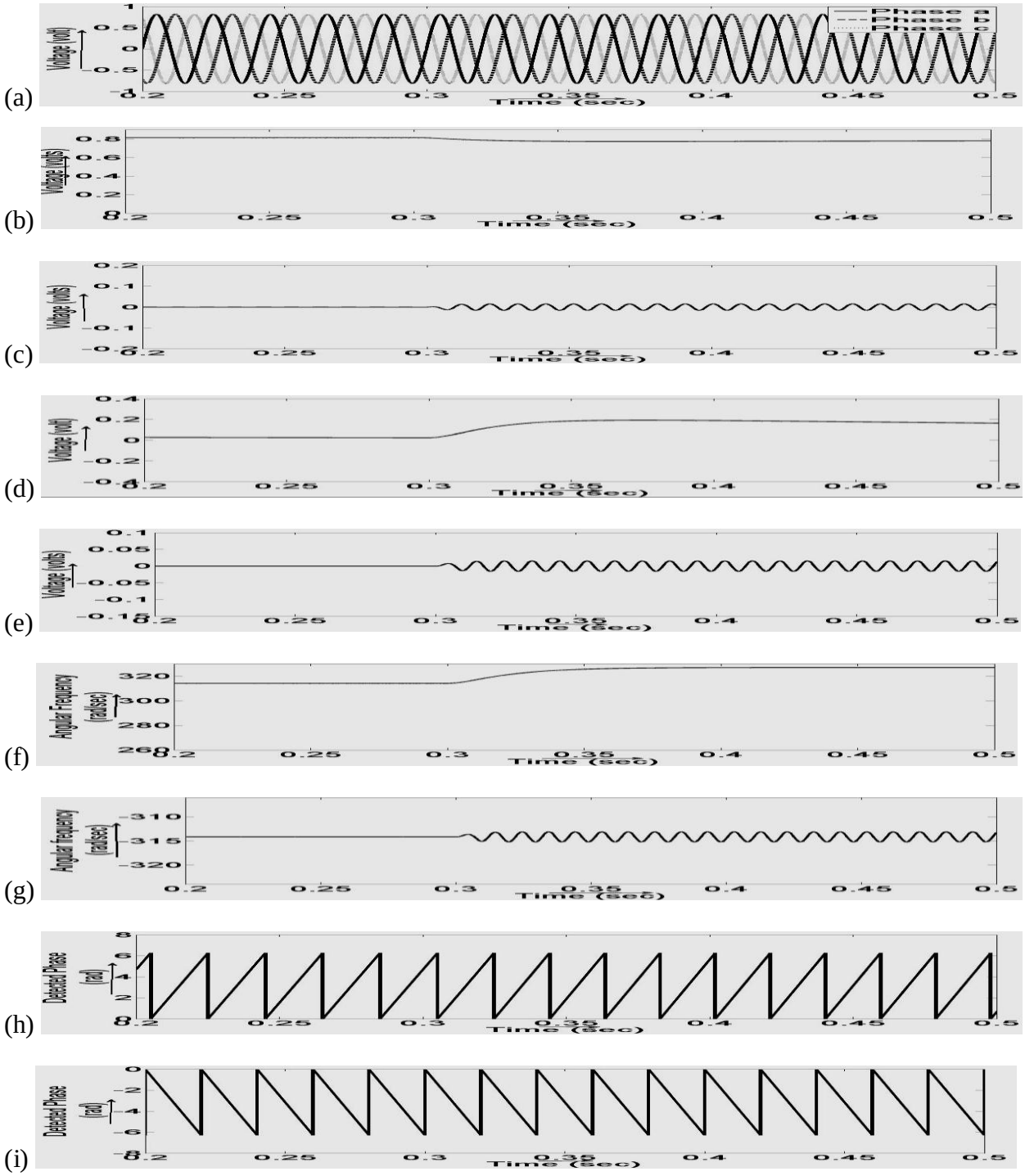


Figure 4.4: Response of SOGI based PLL during Frequency Deviation (a) Grid Voltage Waveforms (b) d axis Voltage of Positive Sequence Component (c) d axis Voltage of Negative Sequence Component (d) q axis Voltage of Positive Sequence Component (e) q axis Voltage of Negative Sequence Component (f) Detected Angular Frequency of Positive Sequence Component (g) Detected Angular Frequency of Negative Sequence Component (h) Detected Phase Angle of Positive Sequence Component (i) Detected Phase Angle of Negative Sequence Component

Fig. 4.4(a) shows the grid voltage when frequency deviation occurs. During this fault the frequency of the system suddenly increases to 52 Hz from 50 Hz at 0.3 sec, keeping the amplitude constant and remains so till the end. The d axis voltage of positive sequence component shown in Fig. 4.4(b) is constant at the amplitude of the signals during balanced input but when the frequency increases, this voltage component decreases to a low value. The d axis voltage for negative sequence component (Fig. 4.4(c)) also maintains its constant value other than very small constant oscillations that occur as soon as the frequency increases. The q axis voltages for positive sequence (Fig. 4.4(d)) and negative sequence (Fig. 4.4(e)) maintains their near zero value during normal frequency. But when the frequency increases the positive sequence increases to a higher value whereas the negative sequence shows behaviour similar to d-axis component. The angular frequencies of positive sequence and negative sequence components maintain their constant value at 100π and -100π (Fig. 4.4(f) and Fig.4.4(g) respectively) except when the frequency increases, when they start oscillating across the same value. Therefore the detected phase angle is perfectly triangular for both positive (Fig. 4.4(h)) and negative sequence (Fig. 4.4(i)).

4.3.3 Response of SOGI based PLL During Harmonic Injection:

The responses obtained from simulation for SOGI based PLL during harmonic injection are shown in Fig. 4.5. The PI tuning used for these results are K_p=67.5 and K_i=100. The gain for QSG was taken as 1.

As shown in Fig. 4.5(a), 5^{th} and 7^{th} harmonics are injected into the system at t=0.3 sec, rest everything remaining the same. Fig. 4.5(b) illustrates the d axis voltage of positive sequence component, which is constant at the amplitude of the input signal. As soon as the harmonics are injected, the voltage starts oscillating across the same value and remains so till the end. Similarly as shown in Fig. 4.5(c) the d axis voltage of negative sequence component also maintains its constant zero value except when harmonics are injected during which the component oscillates around zero.

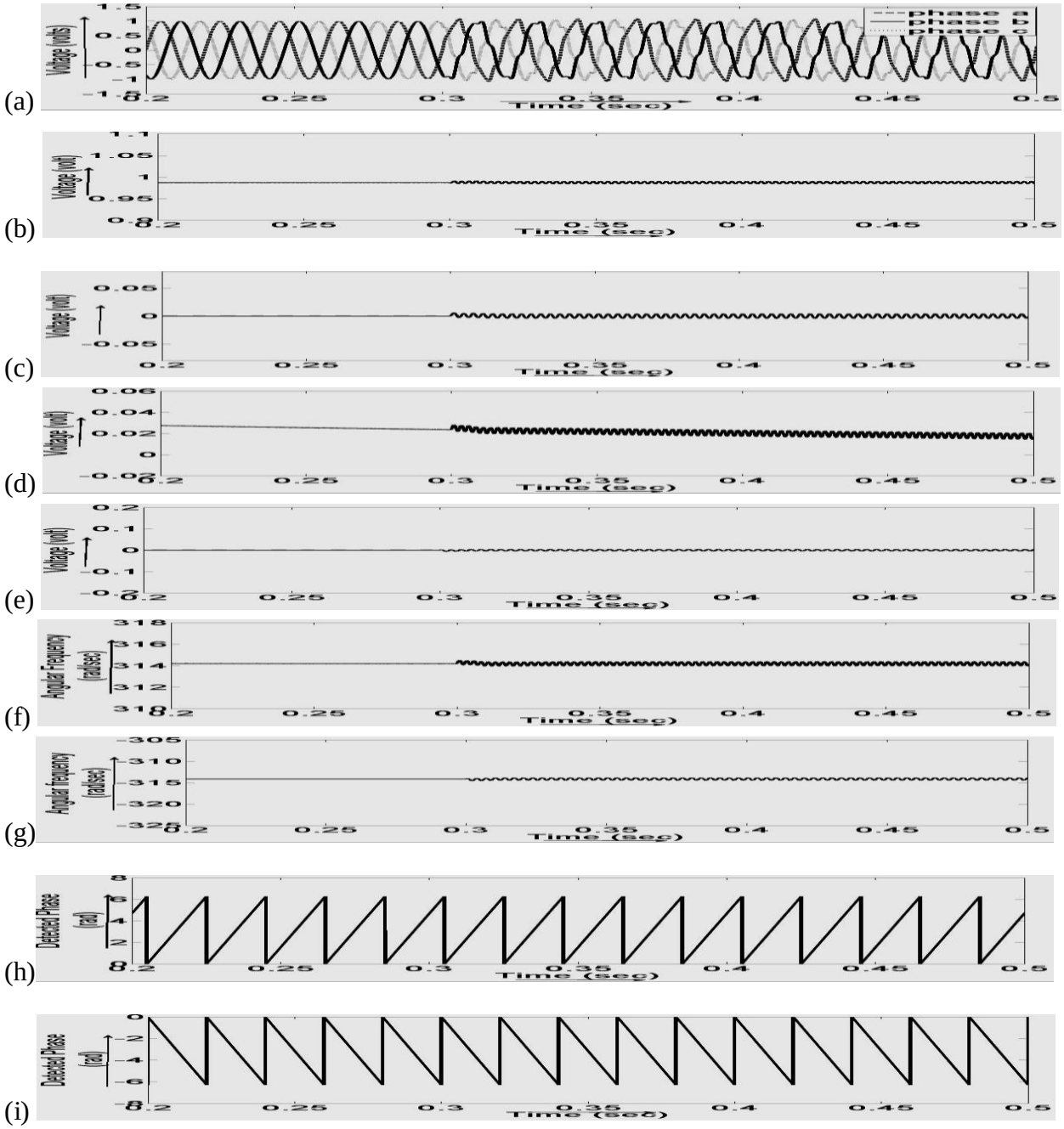


Figure 4.5: Response of SOGI based PLL during Harmonic Injection (a) Grid Voltage Waveforms (b) d axis Voltage of Positive Sequence Component (c) d axis Voltage of Negative Sequence Component (d) q axis Voltage of Positive Sequence Component (e) q axis Voltage of Negative Sequence Component (f) Detected Angular Frequency of Positive Sequence Component (g) Detected Angular Frequency of Negative Sequence Component (h) Detected Phase Angle of Positive Sequence Component (i) Detected Phase Angle of Negative Sequence Component

The q axis voltage of positive sequence component remains constant at a value very close to zero and with the input of harmonics, it starts oscillating and the average value gradually decreases towards zero (Fig. 4.5(d)). The same holds good for q axis voltage of negative sequence component which remains constant at zero, but oscillates throughout when harmonics are injected (Fig. 4.5(e)). As q axis voltages are constant the corresponding angular frequency for both positive and negative sequence components maintains their constant value at 100π and -100π till the system is operating at 50 Hz, but when harmonics are injected, these quantities oscillate around the same value (Fig. 4.5(f) and Fig. 4.5(g)).The detected phase for both the sequence components is perfectly triangular because of the constant angular frequency observed (Fig. 4.5(h) and Fig. 4.5(i)).

4.3.4 Response of SOGI based PLL During Voltage Dip:

The responses obtained from simulation for SOGI based PLL during voltage dip are shown in Fig. 4.6. The PI tuning used for these results are K_p=67.5 and K_i=100. The gain K for the QSG was taken as 1.

Fig. 4.6(a) shows a 3-phase signal which is balanced up to time t=0.3 sec and then voltage amplitudes of the three phases change to 0.45, 0.475 and 0.55V from their initial value of 0.5V. After 0.05 sec the voltage returns back to its original value.

As shown in Fig. 4.6(b) d axis voltage of positive sequence component is almost constant except during the transient period (from t=0.3 to 0.35 sec). Similarly as shown in Fig. 4.6(c) the d axis voltage of negative sequence component is almost constant having a dip during the fault period. As shown is Fig. 4.6(d) the q axis voltage of the positive sequence component maintains a constant value and the transients are observed during the voltage dip. The q axis voltage for negative sequence component behaves in a similar way as the d axis voltage for negative sequence as can be seen in Fig. 4.6(e).

The angular frequencies of positive and negative sequence components are both similar to their respective q axis voltages and hence a nearly constant angular frequency is observed for positive and negative sequence components (Fig. 4.6(f) and Fig. 4.6(g) respectively). For these constant angular frequencies we observe perfectly triangular phase angle detection for positive sequence (Fig. 4.6(h)) and negative sequence (Fig. 4.6(i)). The detected phase angle varies

linearly every cycle from 0 to 2π for positive sequence and 0 to -2π for negative sequence.

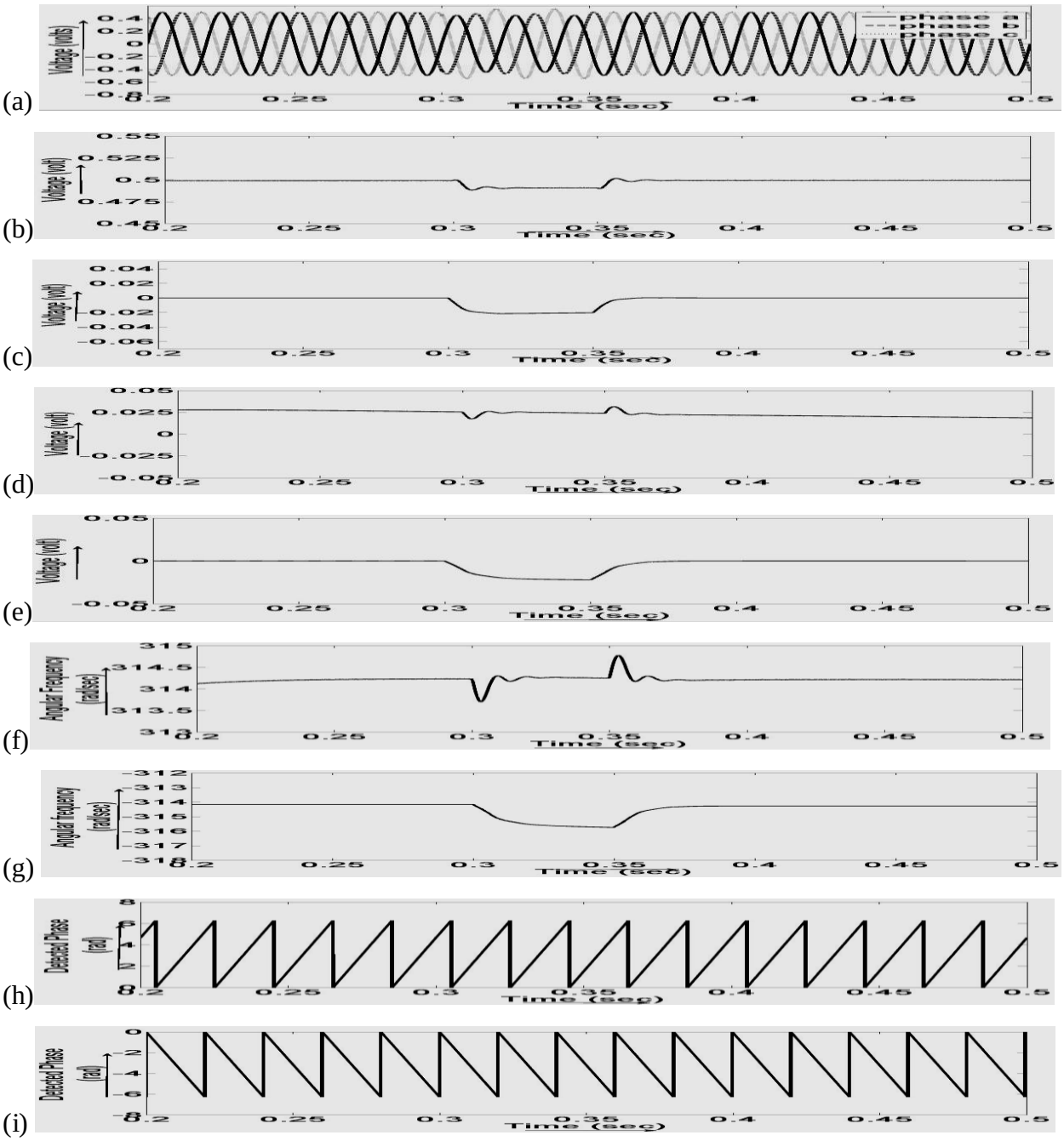


Figure 4.6: Response of SOGI based PLL during Voltage Dip (a) Grid Voltage Waveforms (b) d axis Voltage of Positive Sequence Component (c) d axis Voltage of Negative Sequence Component (d) q axis Voltage of Positive Sequence Component (e) q axis Voltage of Negative Sequence Component (f) Detected Angular Frequency of Positive Sequence Component (g) Detected Angular Frequency of Negative Sequence Component (h) Detected Phase Angle of Positive Sequence Component (i) Detected Phase Angle of Negative Sequence Component

4.3.5 Response of SOGI based PLL During Voltage Flicker:

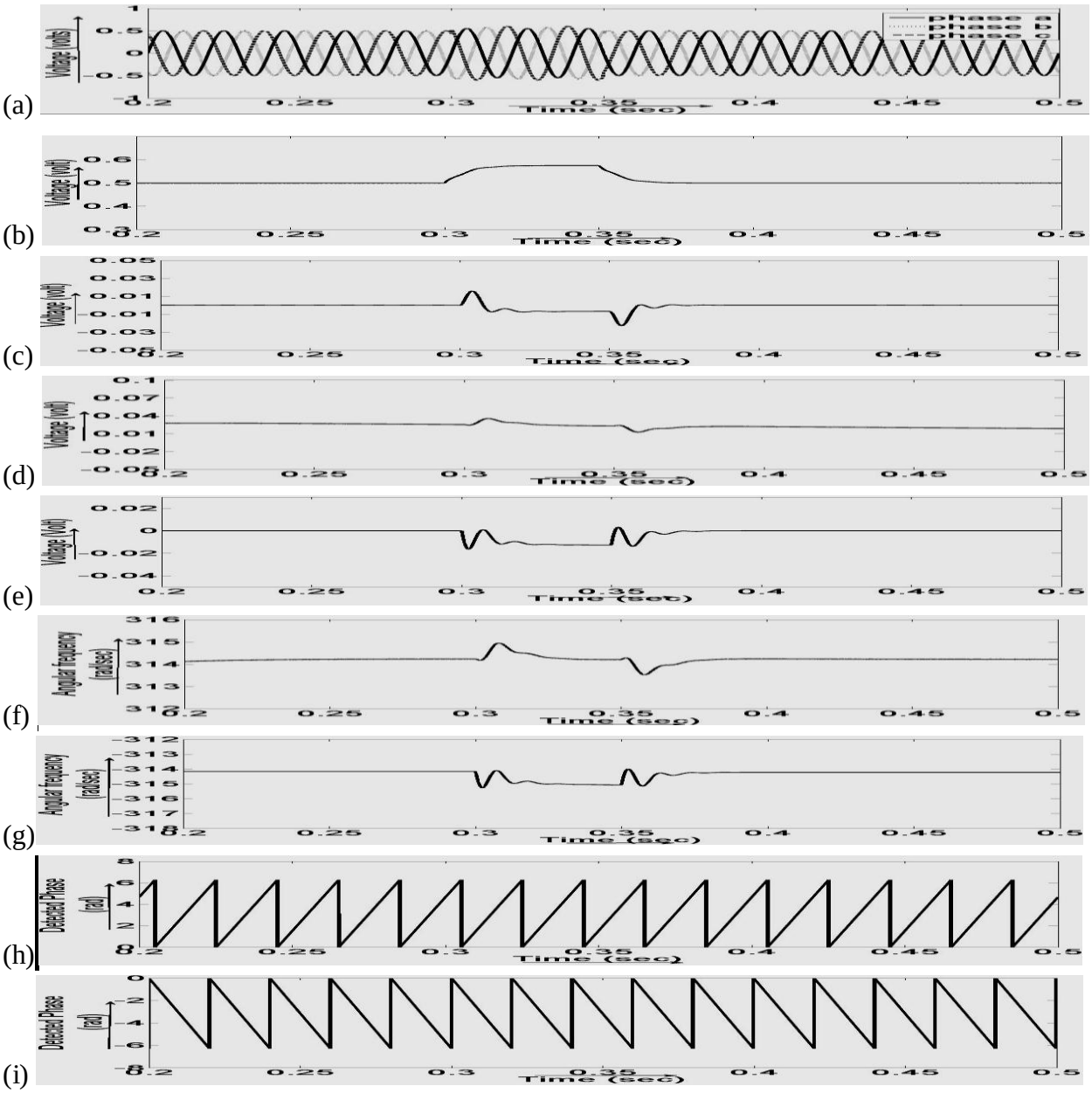


Figure 4.7: Response of SOGI based PLL during Voltage Flicker (a) Grid Voltage Waveforms (b) d axis Voltage of Positive Sequence Component (c) d axis Voltage of Negative Sequence Component (d) q axis Voltage of Positive Sequence Component (e) q axis Voltage of Negative Sequence Component (f) Detected Angular Frequency of Positive Sequence Component (g) Detected Angular Frequency of Negative Sequence Component (h) Detected Phase Angle of Positive Sequence Component (i) Detected Phase Angle of Negative Sequence Component

The responses obtained from simulation of SOGI based PLL during voltage flicker are shown in Fig. 4.7. The PI tuning used for these results are K_p=67.5 and K_i=100. The gain K for the QSG was taken as 1.

Fig. 4.7(a) shows the input to the system when voltage flicker occurs. The system was initially in balanced condition (having amplitude 0.5V). At t=0.3 sec, the phase voltage of all the phases increases randomly to 0.55V, 0.6V and 0.65V respectively. The system regains its balanced state at time, t = 0.35 sec. The d axis voltage of positive sequence component shown in Fig. 4.7(b) is constant at the amplitude of the signals during the entire period except when flicker occurs, when the voltage increases to a new value. The d axis voltage for negative sequence component (Fig. 4.7(c)) also maintains its constant value other than very small transients that occur at time t = 0.3 sec and 0.35 sec and these two are opposite in nature. The q axis voltages for positive sequence (Fig. 4.7(d)) remains constant before flicker occurs, experiences transients during the event, and reduces to a low value after the flicker is over. The q axis voltage for negative sequence (Fig. 4.7(e)) maintains its zero value at all instants, with reduced value during the flicker. The angular frequencies of positive sequence and negative sequence components maintain their constant value at 100π and -100π (Fig. 4.7(f) and Fig.4.7(g) respectively).Therefore the detected phase angle is perfectly triangular for both positive (Fig. 4.7(h)) and negative sequence (Fig. 4.7(i)).

4.3.6 Response of SOGI based PLL During Voltage Sag:

The responses obtained from simulation for SOGI based PLL during voltage sag are shown in Fig. 4.8. The PI tuning used for these results are K_p=67.5 and K_i=100. The gain K for the QSG was taken as 1.

As shown in Fig. 4.8(a), voltage sag occurs at time t = 0.3 sec when all the three phase voltages reduces to 0.45V from their initial voltage of 0.5V. The three phases regain their original value of 0.5V at time t = 0.35 sec. Fig. 4.8(b) illustrates the d axis voltage of positive sequence component, which is constant at the amplitude of the input signal.

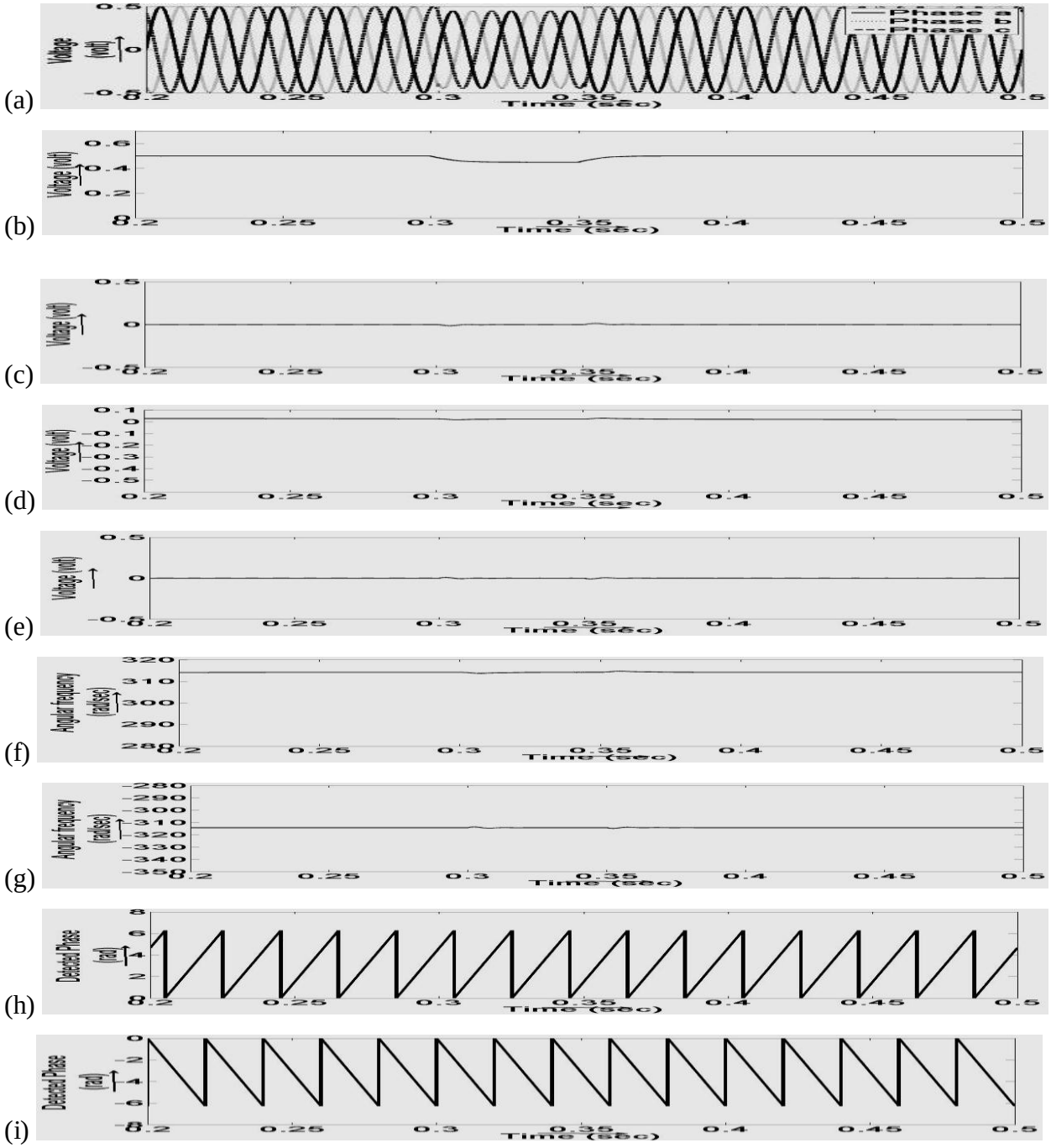


Figure 4.8: Response of SOGI based PLL during Voltage Sag (a) Grid Voltage Waveforms (b) d axis Voltage of Positive Sequence Component (c) d axis Voltage of Negative Sequence Component (d) q axis Voltage of Positive Sequence Component (e) q axis Voltage of Negative Sequence Component (f) Detected Angular Frequency of Positive Sequence Component (g) Detected Angular Frequency of Negative Sequence Component (h) Detected Phase Angle of Positive Sequence Component (i) Detected Phase Angle of Negative Sequence Component

In the duration when voltage sag occurs, the d axis voltage remains constant but its value changes to the new amplitude. Similarly as shown in Fig. 4.8(c) the d axis voltage of negative sequence component also maintains its constant zero value. The q axis voltage of positive sequence component remains constant at a value very close to zero and some slight transients are observed at the time of switching (Fig. 4.8(d)). The same holds good for q axis voltage of negative sequence component which remains constant at zero in both the periods (Fig. 4.8(e)). As q axis voltages are constant the corresponding angular frequency for both positive and negative sequence components maintains their constant value at 100π (Fig. 4.8(f)) and -100π (Fig. 4.8(g)) respectively. The detected phase for both the sequence components is perfectly triangular because of the constant angular frequency observed (Fig. 4.8(h) and Fig. 4.8(i)).

4.4 COMPARATIVE STUDY:

A comparative analysis was carried out between SOGI based PLL and DSRF PLL. The comparison was done on the basis of their performance during different grid abnormalities. The results so obtained are shown in the following sections.

4.4.1 Comparison of SOGI based PLL and DSRF PLL Under Line to Ground Fault:

The results obtained from simulation for DSRF PLL and SOGI based PLL under line to ground fault are shown in Fig. 4.9. For this study, the gain of PI controller was taken as K_p=67.5 and K_i=100. The K value for QSG of SOGI was taken as 1. The explanation for the study is given as follows.

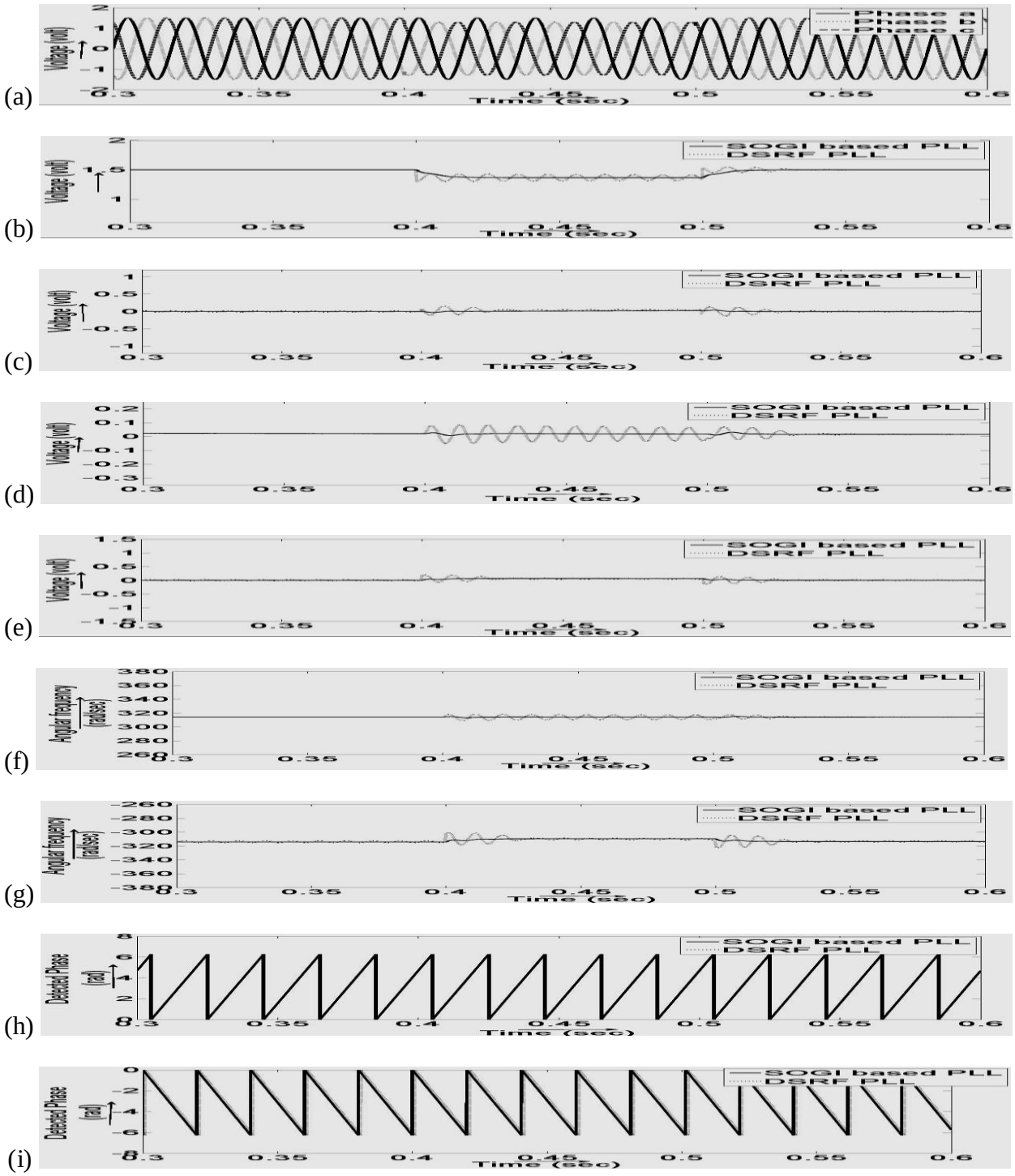


Figure 4.9: Comparison of SOGI based PLL and DSRF PLL under Line To Ground Fault (a) Grid Voltage Waveforms (b) d axis Voltage of Positive Sequence Component (c) d axis Voltage of Negative Sequence Component (d) q axis Voltage of Positive Sequence Component (e) q axis Voltage of Negative Sequence Component (f) Detected Angular Frequency of Positive Sequence Component (g) Detected Angular Frequency of Negative Sequence Component (h) Detected Phase Angle of Positive Sequence Component (i) Detected Phase Angle of Negative Sequence Component

Fig. 4.9(a) shows the grid voltage (input to the system) when line to ground fault occurs. The system was initially in balanced condition (having amplitude 1.5V). Line to ground fault occurs at time, t = 0.4sec. At this instant the phase voltage of two of the phases reduces and remains at an amplitude of 1.3V. The system regains its balanced state at time, t = 0.5 sec. Fig. 4.9(b) shows the d axis voltage of positive sequence component. For both DSRF PLL and SOGI based PLL the d axis voltages are constant at the amplitude of the input signal during balanced input but during unbalance the voltage reduces slightly. Even in this case the voltage given by SOGI based PLL is constant but the voltage given by DSRF PLL has got some negligible oscillations. The transients are observed with DSRF PLL when input voltage changes but with the SOGI based PLL the transient oscillations are absent and the d axis voltage achieves its final value smoothly. For both the PLLs the final value is same. The d axis voltage for negative sequence component (Fig. 4.9(c)) also maintains its constant value other than very small transients that occur for DSRF PLL at time t = 0.4 sec and 0.5 sec. The q axis voltages for positive sequence (Fig. 4.9(d)) and negative sequence (Fig. 4.9(e)) maintain a value which is almost equal to zero value at all instants but some oscillations are observed in case of DSRF PLL. Similar nature is observed for angular frequencies of positive sequence and negative sequence components which maintain their constant value at 100π (Fig. 4.9(f)) and -100π (Fig. 4.9(g)) respectively with some oscillations in the case of DSRF PLL and almost no oscillations in case of SOGI based PLL. As a result of constant angular frequencies the detected phase angle is perfectly triangular for both positive (Fig. 4.9(h)) and negative sequence (Fig. 4.9(i)) for both the PLLs. The detected phase changes linearly from 0 to 2π in each cycle for positive sequence and 0 to -2π for negative sequence.

4.4.2 Comparison of SOGI based PLL and DSRF PLL During Frequency Deviation:

This section explains the response of two PLLs during frequency deviation and the corresponding results are shown in Fig. 4.10.

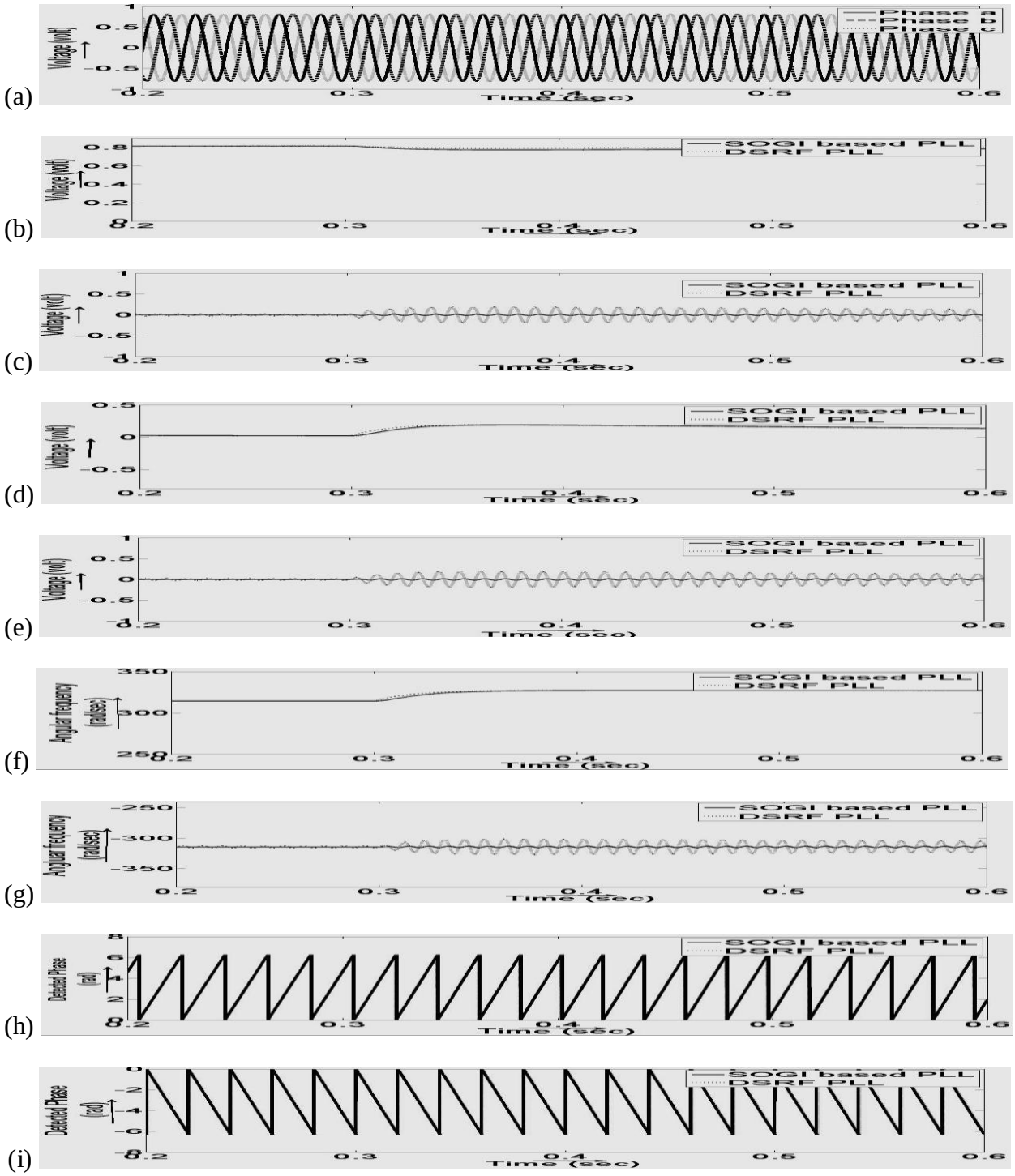


Figure 4.10: Comparison of SOGI based PLL and DSRF PLL during Frequency Deviation (a) Grid Voltage Waveforms (b) d axis Voltage of Positive Sequence Component (c) d axis Voltage of Negative Sequence Component (d) q axis Voltage of Positive Sequence Component (e) q axis Voltage of Negative Sequence Component (f) Detected Angular Frequency of Positive Sequence Component (g) Detected Angular Frequency of Negative Sequence Component (h) Detected Phase Angle of Positive Sequence Component (i) Detected Phase Angle of Negative Sequence Component

To study the response of frequency deviation, the frequency of the input signal is changed from 50 Hz to 52 Hz at 0.3 sec as shown in Fig. 4.10(a). Fig. 4.10(b) and Fig. 4.10(c) illustrates the d axis voltages of the two sequence components. The d axis voltage of positive sequence is almost same for both the PLLs but the d axis voltage of negative sequence contains oscillations in case of DSRF PLL when frequency changes while the oscillations are very less in the case of SOGI based PLL. The same nature is observed for q axis voltages (Fig. 4.10(d) and Fig. 4.10(e)) and hence for the angular frequencies (Fig. 4.10(f) and Fig. 4.10(g)) of the two components too. The angular frequencies are almost constant at 100π and -100π. Though negligible, but the harmonic oscillations in case of DSRF PLL are more than the SOGI based PLL. The almost constant nature of angular frequencies result in the perfect triangular detection of phase angles (Fig. 4.10(h) and Fig. 4.10(i)).

4.4.3 Comparison of SOGI based PLL and DSRF PLL During Voltage Sag:

The simulation results of two PLLs during voltage sag are explained in this section and are illustrated in Fig. 4.11.

As shown in Fig. 4.11(a), voltage sag occurs at time t = 0.3 sec when voltage amplitude of all three phases reduces to 0.45V from their initial amplitude of 0.5V. The original value of amplitude is regained at 0.4 sec. The d axis voltage of positive sequence component, equal to the amplitude of input signal is shown in Fig. 4.11(b). Smooth change is observed for SOGI based PLL as compared to oscillations in DSRF PLL, whereas the time taken to achieve new value after switching is less in case of DSRF PLL. Similarly the d axis voltage of negative sequence component, as shown in Fig. 4.11(c) maintains its constant zero value but oscillations are observed for DSRF PLL. The q axis voltage of positive sequence component (Fig. 4.11(d)) remains constant at a value very close to zero. Likewise the q axis voltage of negative sequence component remains constant at zero (Fig. 4.11(e)). The DSRF waveform for both the q axis voltages contain some oscillations, while in the other case it is almost straight line and oscillations are very less. The angular frequencies for both the components have same nature as the q axis components. The values are almost constant at 100π and -100π (Fig. 4.11(f) and Fig. 4.11(g)) respectively with some small oscillations observed in case of DSRF PLL. As a result of constant angular frequencies, the detected phase for both the sequence components is perfectly triangular (Fig. 4.11(h) and Fig. 4.11(i)) for both the PLLs.

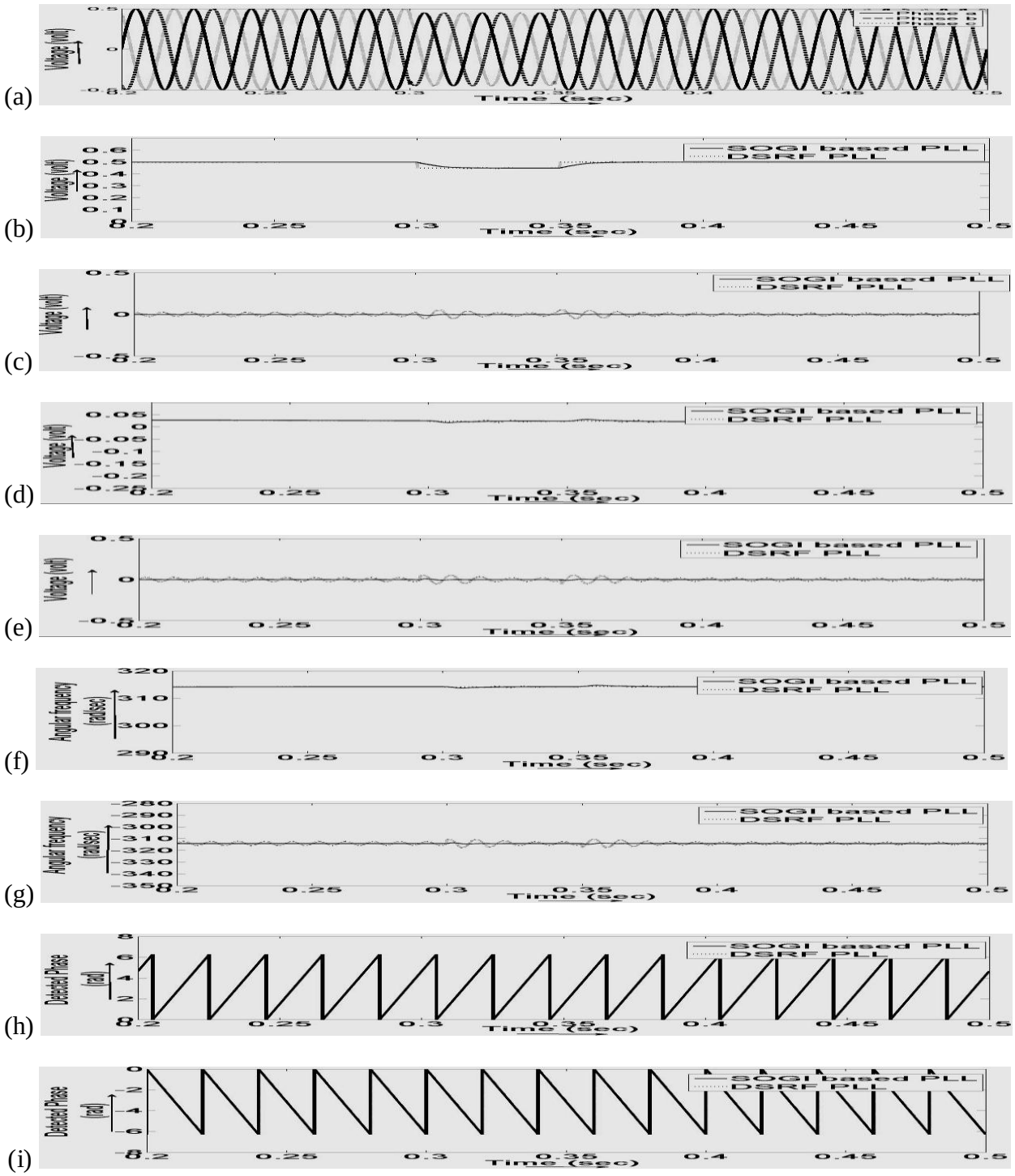


Figure 4.11: Comparison of SOGI based PLL and DSRF PLL during Voltage Sag (a) Grid Voltage Waveforms (b) d axis Voltage of Positive Sequence Component (c) d axis Voltage of Negative Sequence Component (d) q axis Voltage of Positive Sequence Component (e) q axis Voltage of Negative Sequence Component (f) Detected Angular Frequency of Positive Sequence Component (g) Detected Angular Frequency of Negative Sequence Component (h) Detected Phase Angle of Positive Sequence Component (i) Detected Phase Angle of Negative Sequence Component

4.4.4 Comparison of SOGI based PLL and DSRF PLL During Voltage Dip:

The simulation results of two PLLs during voltage dip are explained in this section and are illustrated in Fig. 4.12.

As shown in Fig. 4.12 (a), voltage dip occurs at time t = 0.3 sec when voltage amplitude of the three phases change to 0.45, 0.475 and 0.55V and system becomes unbalanced. The system regains its balanced state at 0.35 sec. The d axis voltage of positive sequence component, equal to the amplitude of input signal is shown in Fig. 4.12 (b). While for SOGI based PLL, the d axis voltage is observed to be almost constant; the DSRF PLL shows some oscillations especially during the unbalanced voltage. Similarly the d axis voltage of negative sequence component, as shown in Fig. 4.12 (c) maintains its constant zero value but oscillations are observed for DSRF PLL. The q axis voltage of positive sequence component (Fig. 4.12 (d)) remains constant at a value very close to zero. Likewise the q axis voltage of negative sequence component remains constant at zero (Fig. 4.12 (e)). The DSRF waveform for both the q axis voltages contain some oscillations, while in the other case it is almost straight line and oscillations are very less. The angular frequencies for both the components have same nature as the q axis components. The values are almost constant at 100π and -100π (Fig. 4.12 (f) and Fig. 4.12 (g)) respectively with some small oscillations observed in case of DSRF PLL. For positive sequence component, these oscillations are much observable during the abnormal condition but for the negative sequence component, the oscillations can be seen even in normal balanced operating condition. As a result of constant angular frequencies, the detected phase for both the sequence components is perfectly triangular (Fig. 4.12 (h) and Fig. 4.12 (i)) for both the PLLs.

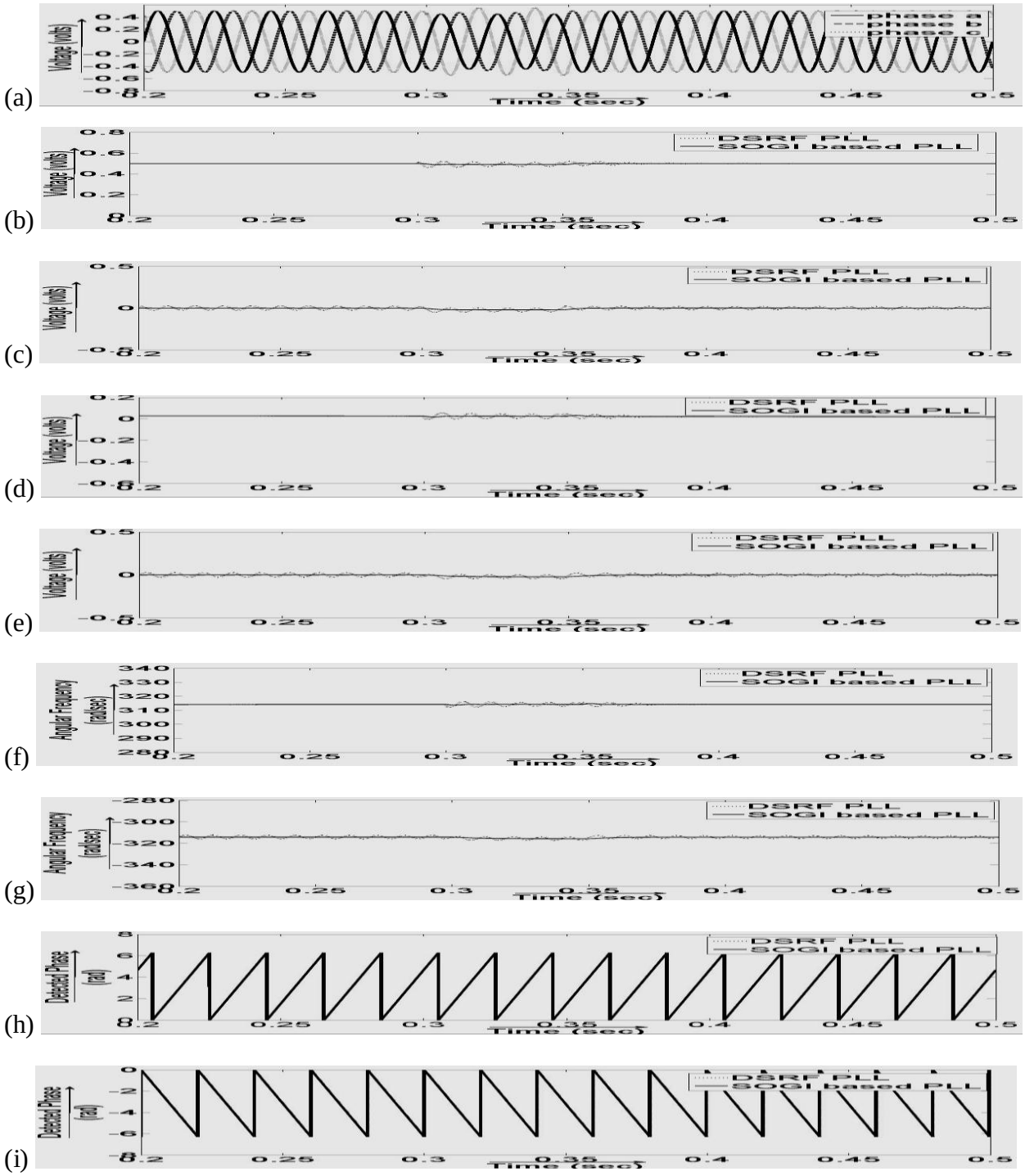


Figure 4.12: Comparison of SOGI based PLL and DSRF PLL during Voltage Dip (a) Grid Voltage Waveforms (b) d axis Voltage of Positive Sequence Component (c) d axis Voltage of Negative Sequence Component (d) q axis Voltage of Positive Sequence Component (e) q axis Voltage of Negative Sequence Component (f) Detected Angular Frequency of Positive Sequence Component (g) Detected Angular Frequency of Negative Sequence Component (h) Detected Phase Angle of Positive Sequence Component (i) Detected Phase Angle of Negative Sequence Component

4.4.5 Comparison of SOGI based PLL and DSRF PLL During Voltage Flicker:

The simulation results of two PLLs during voltage flicker are explained in this section and are illustrated in Fig. 4.13.

As shown in Fig. 4.13 (a), voltage flicker occurs at time t = 0.3 sec when voltage amplitude of all three phases increases and system becomes unbalanced. The system regains its balanced state at 0.35 sec. The d axis voltage of positive sequence component, equal to the amplitude of input signal is shown in Fig. 4.13 (b). While for SOGI based PLL, the d axis voltage is observed to be almost constant, the DSRF PLL shows some oscillations especially at the instants when voltage changes. During the unbalanced voltage condition, the SOGI based PLL smoothly obtains its new value while oscillatory behaviour is observed for the DSRF PLL. Similarly the d axis voltage of negative sequence component, as shown in Fig. 4.13 (c) maintains its constant zero value but oscillations are observed for DSRF PLL. The q axis voltage of positive sequence component (Fig. 4.13 (d)) remains constant at a value very close to zero. Likewise the q axis voltage of negative sequence component remains constant at zero (Fig. 4.13 (e)). The DSRF PLL waveform for both the q axis voltages contain some oscillations, while in the other case it is almost straight line and oscillations are very less. The angular frequencies for both the components have same nature as the q axis components. The values are almost constant at 100π and -100π (Fig. 4.13 (f) and Fig. 4.13 (g)) respectively with some small oscillations observed in case of DSRF PLL. For positive sequence component, these oscillations are much observable during the abnormal condition but for the negative sequence component, the oscillations can be seen even in normal balanced operating condition. As a result of constant angular frequencies, the detected phase for both the sequence components is perfectly triangular (Fig. 4.13 (h) and Fig. 4.13 (i)) for both the PLLs.

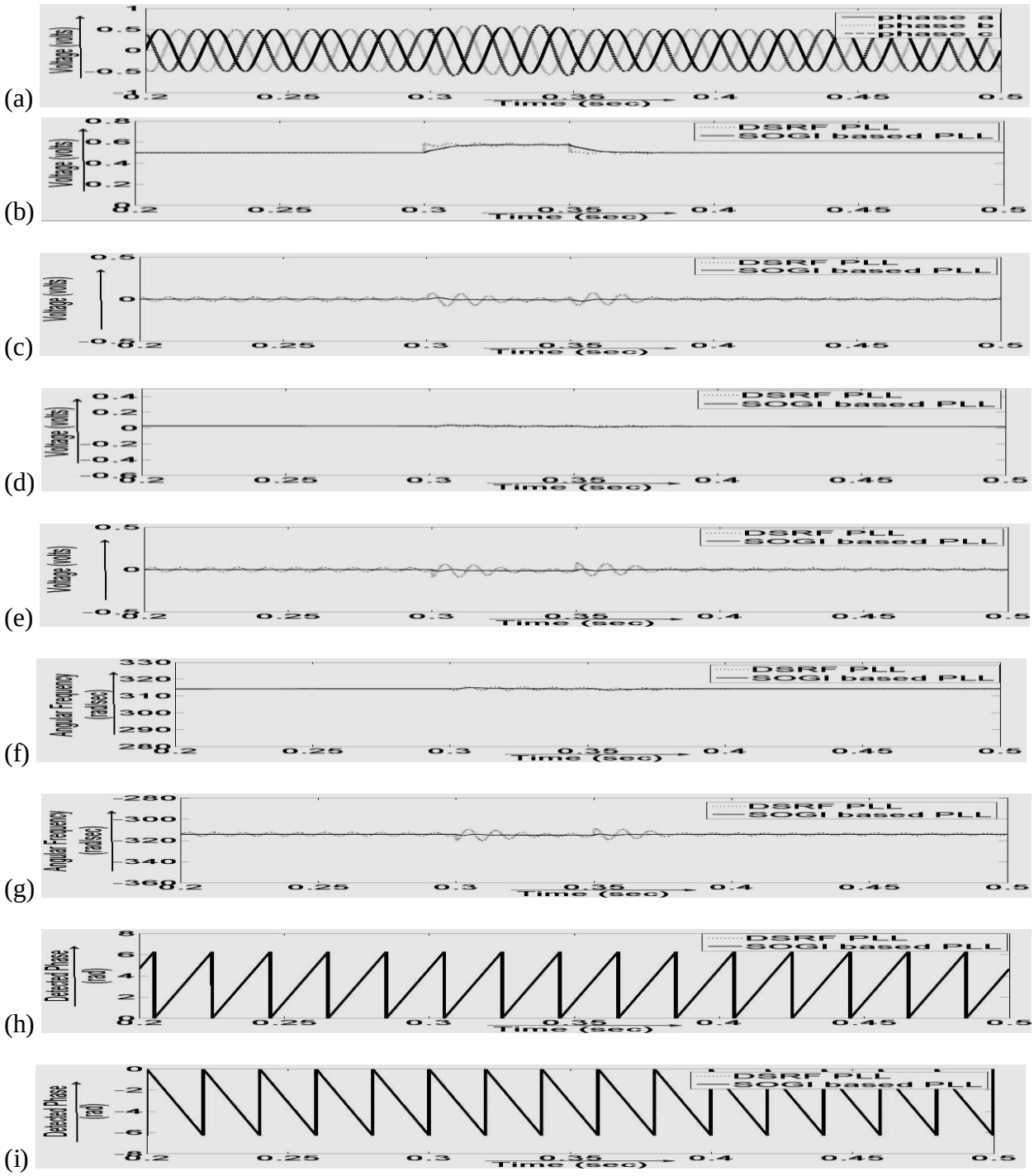


Figure 4.13: Comparison of SOGI based PLL and DSRF PLL during Voltage Flicker (a) Grid Voltage Waveforms (b) d axis Voltage of Positive Sequence Component (c) d axis Voltage of Negative Sequence Component (d) q axis Voltage of Positive Sequence Component (e) q axis Voltage of Negative Sequence Component (f) Detected Angular Frequency of Positive Sequence Component (g) Detected Angular Frequency of Negative Sequence Component (h) Detected Phase Angle of Positive Sequence Component (i) Detected Phase Angle of Negative Sequence Component

4.4.6 Comparison of SOGI based PLL and DSRF PLL During Harmonic Injection:

The simulation results of two PLLs during harmonic injection are explained in this section and are illustrated in Fig. 4.14.

As shown in Fig. 4.14 (a), the system is operating at balanced 3-phase voltage upto 0.3 sec and then 5^{th} and 7^{th} harmonics are injected as a result of which the 3-phase voltage waveforms get distorted. The d axis voltage of positive sequence component, equal to the amplitude of input signal is shown in Fig. 4.14 (b). While for SOGI based PLL, the d axis voltage is observed to be almost constant, the DSRF PLL shows much oscillations that are consistent throughout the duration when grid voltage contains harmonic distortions. Similarly the d axis voltage of negative sequence component, as shown in Fig. 4.14 (c) maintains its constant zero value but oscillations are observed for DSRF PLL. The oscillations are observable even in normal operating condition. The q axis voltage of positive sequence component (Fig. 4.14 (d)) remains constant at a value very close to zero. Likewise the q axis voltage of negative sequence component remains constant at zero (Fig. 4.14 (e)). Though slight oscillations are observed when system gets distorted due to multiple frequency components, the oscillations observed in case of SOGI based PLL are very less while oscillations in the case of DSRF PLL are clearly noticeable. The angular frequencies for both the components have same nature as the q axis components. The values are almost constant at 100π and -100π (Fig. 4.14 (f) and Fig. 4.14 (g)) respectively but the effect of harmonics can be easily seen in case of DSRF PLL as the detected angular frequency oscillates between two different values especially for the positive sequence component, while the oscillations in case of SOGI based PLL are hardly noticeable. The oscillations in case of DSRF PLL though visible, do not make much impact on the detected phase angle because the range of oscillation is very small and the integration of such oscillatory values give negligible effect. As a result of constant angular frequencies, the detected phase for both the sequence components is perfectly triangular (Fig. 4.14 (h) and Fig. 4.14 (i)) for both the PLLs (ranging from 0 to 2π and 0 to -2π for the positive sequence and the negative sequence respectively).

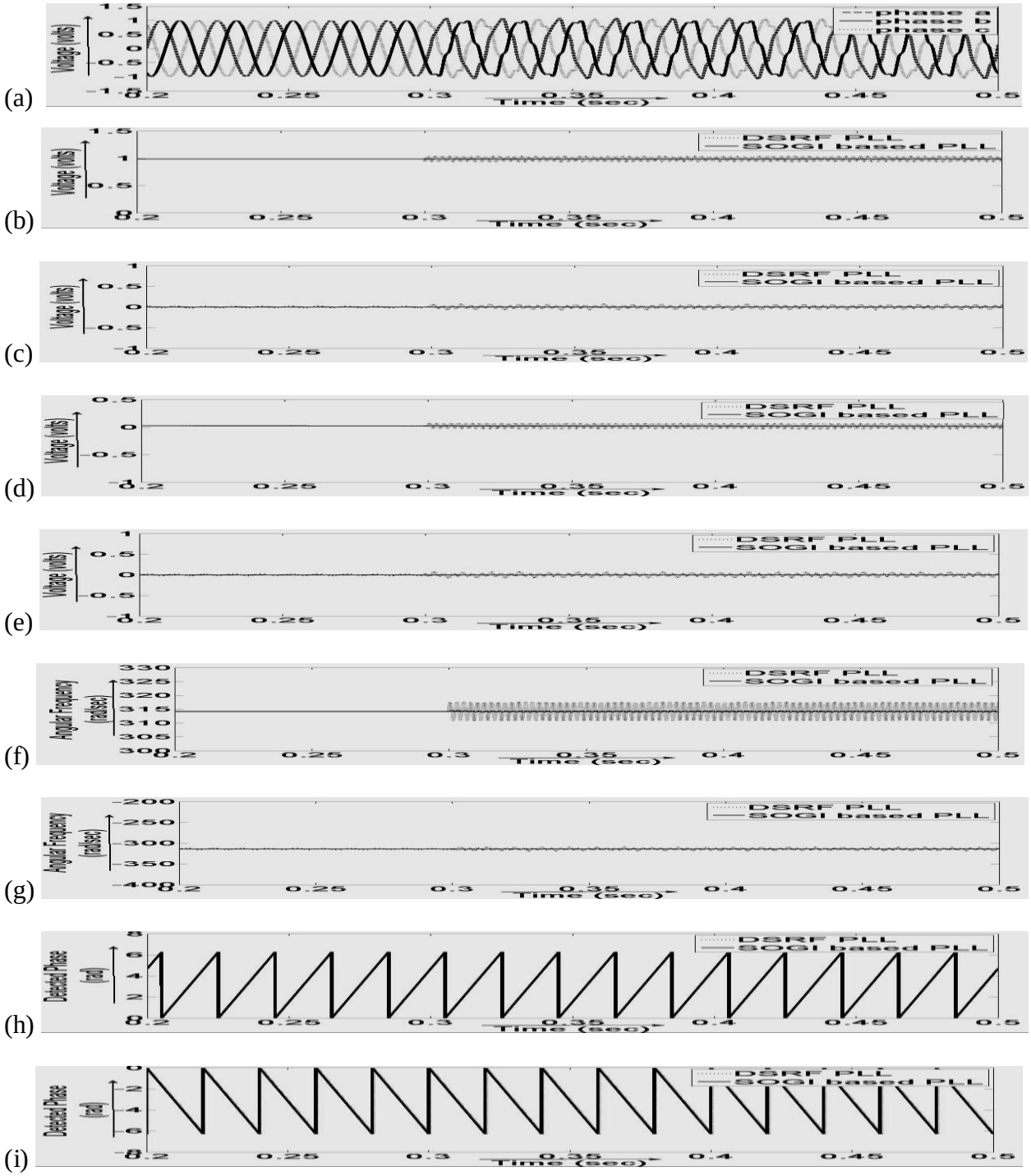


Figure 4.14: Comparison of SOGI based PLL and DSRF PLL during Harmonic Injection (a) Grid Voltage Waveforms (b) d axis Voltage of Positive Sequence Component (c) d axis Voltage of Negative Sequence Component (d) q axis Voltage of Positive Sequence Component (e) q axis Voltage of Negative Sequence Component (f) Detected Angular Frequency of Positive Sequence Component (g) Detected Angular Frequency of Negative Sequence Component (h) Detected Phase Angle of Positive Sequence Component (i) Detected Phase Angle of Negative Sequence Component

4.5 CONCLUSION:

From the study it can be easily concluded the SOGI based PLL, which uses a SOGI to generate quadrature signals easily decouple the positive and the negative sequence components and hence can handle major abnormalities and track the phase angle of the positive as well as negative sequence components perfectly and with a very good dynamic response. The stability of the PLL depends on the stability of the SOGI, which is tested by plotting the Bode plot for the SOGI. With the gain values taken for the study, the Bode plot showed that the system is stable. In comparison to DSRF PLL, SOGI based PLL gives much better response in the sense that dynamic response in all kinds of abnormalities is better for SOGI based PLL as the DSRF PLL showed many oscillations, especially for negative sequence component and at the instant when system changes its operating condition.

CHAPTER 5

Conclusions and Future work

5.1 CONCLUSIONS:

The various grid synchronization algorithms were analysed in this thesis and the following conclusions are drawn.

A. A Linear PLL (LPLL) can be used for synchronization for single phase signals with acceptable results and a Synchronous Reference Frame (SRF) PLL can be used for 3-phase balanced signals. But it cannot be used for unbalanced utility conditions as the detected phase angle contains 2^{nd} harmonic oscillations.
B. Double SRF PLL solves the above problem by decomposing the input voltage vectors into their positive and negative sequence components. By this, this PLL detects the phase angle separately for each of the two components. The response of this PLL has slight oscillations which makes the response sluggish in nature.
C. The shortcomings of DSRF PLL are overcome by the SOGI based PLL. This model uses Quadrature Signal Generation (QSG) followed by separate tracking of positive and negative sequence components. Unlike the former one, for the later model the positive and negative sequences are independent to each other. Further, the transient response of SOGI based PLL during grid abnormalities is better than DSRF PLL, even though both the PLLs can detect the phase angles accurately.
D. However, the phase angle detection of the two sequence components is more accurate as in the case of SOGI based PLL due to less harmonic oscillations during the steady state and transient conditions. This is due to the fact that, the estimated phase *(sin(wt) and cos(wt))* by SOGI based PLL is perfectly sinusoidal.
E. The stability of the PLL depends on the stability of SOGI-QSG. The Bode plot observed for the SOGI-QSG shows that the system taken for study is closed loop stable.

5.2 FUTURE WORK:

The algorithms studied in this work are to be realized in FPGA environment for their real time analysis. This will also help in better understanding and analysing how fast these algorithms can accurately track the phase angle during abnormal grid conditions.

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RESEARCH PUBLICATIONS:

1. **Binita Sen, Dushyant Sharma**, B.Chitti Babu, "DSRF and SOGI based PLL-Two Viable Scheme for Grid Synchronization of DG Systems during Grid Abnormalities", *Proc. of IEEE Students' Conference on Engineering & Systems (SCES 2012), MNNIT, Allahabad, Mar/2012*.
2. **Dushyant Sharma, Binita Sen**, B.Chitti Babu, "Improved Grid Synchronization Algorithm for DG System using DSRF PLL under Grid Disturbances", *Proc. of IEEE Students' Conference on Engineering & Systems (SCES 2012), MNNIT, Allahabad, Mar/2012*.