DESIGN OF A DUAL OPAMP LOW OFFSET INTEGRATOR SYSTEM FOR PLASMA REACTOR

A thesis submitted in partial fulfilment of the

requirements for the degree of

Bachelor of Technology

In

Electronics and Instrumentation Engineering

By

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and
Suman Sourav Dikshit
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Department of Electronics and Communication Engineering
National Institute of Technology, Rourkela

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NATIONAL INSTITUTE OF TECHNOLOGY ROURKELA

CERTIFICATE

This is to certify that the thesis entitled **"DESIGN OF A DUAL OPAMP LOW OFFSET INTEGRATOR SYSTEM FOR PLASMA REACTOR"** submitted by Omkar Prasad Mishra (108EI031) and Suman Sourav Dikshit(108EI020) in partial fulfilment of the requirements for the award of the Degree of BACHELOR OF TECHNOLOGY in Electronics and Instrumentation Engineering at National Institute of Technology, Rourkela (Deemed University) is an authentic work carried out by them under my supervision and guidance.

Date: 14th May, 2012

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NATIONAL INSTITUTE OF TECHNOLOGY ROURKELA

DECLARATION

We hereby declare that the project work entitled **"DESIGN OF A DUAL OPAMP LOW OFFSET INTEGRATOR SYSTEM FOR PLASMA REACTOR"** is a record of our original work done under Prof Sarat Kumar Patra, Professor, National Institute of Technology, Rourkela. Throughout this documentation wherever contributions of others are involved, every endeavour was made to acknowledge this clearly with due reference to literature. This work is being submitted in the partial fulfilment of the requirements for the degree of Bachelor of Technology in Electronics and Instrumentation Engineering at National Institute of Technology, Rourkela for the academic session 2008 – 2012.

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ABSTRACT

In a fusion reactor, where tokamaks are used to confine the plasma using toroidal and poloidal magnetic fields, highly accurate magnetic measurements are a necessity for automatic control. However, due to extremities in temperature, acquiring uncorrupted signals become a challenging task. Presented in this thesis is a design of a twin operational amplifier based low offset integrating system to eliminate any error in measurement due to temperature dependent DC offset. This integrator system comprises mainly three stages after the inductive sensor. The first stage consists of a dual integrator in which the output signal from the sensor was fed to one integrator and the input terminals of the other integrator were grounded. An instrumentation amplifier which has a very high common mode rejection ratio and large input impedance was implemented in the second stage to find the differential signal between the outputs of the two integrators. Any noise arising in the environment was eliminated in the next stage by a Digital Signal Processor based Finite Impulse Response Low-Pass Filter. The first two stages of the design were simulated by using Multisim Circuit Design Suite. The low-pass filtering stage was realized on a Texas Instruments TMS320C6713 starter kit using Kaiser Windowing technique to achieve a sharp cut-off at 780Hz. To obtain a full layout of the operational amplifier based design Cadence Electronic Design Automation UMC_180 nm tool was used. The primary objective of DC offset elimination was verified through the results.

KEY WORDS:

Inductive Sensor, Operational Amplifier, Integrator, Instrumentation Amplifier, Low-pass Filter

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Chapter 1

INTRODUCTION

1.1 Plasma State

Plasma is the fourth state of matter after solid, liquid and gaseous states. This state of matter has similarities with the gaseous state but the particles are ionised. The ionised gas consists of nearly same number of negatively and positively charged particles. The characteristics of plasma are different to that of a normal gas. Being composed of charged particles, plasma is strongly affected by electric and magnetic field. In addition to that they are also affected by the magnetic field of the earth.

1.2 Tokamaks

A tokamak is a torus (doughnut) shaped device using powerful magnetic fields to confine the plasma. It is used to study the reactions of plasma which take place at very high temperatures. To get a stable equilibrium of the plasma, magnetic field lines moving around

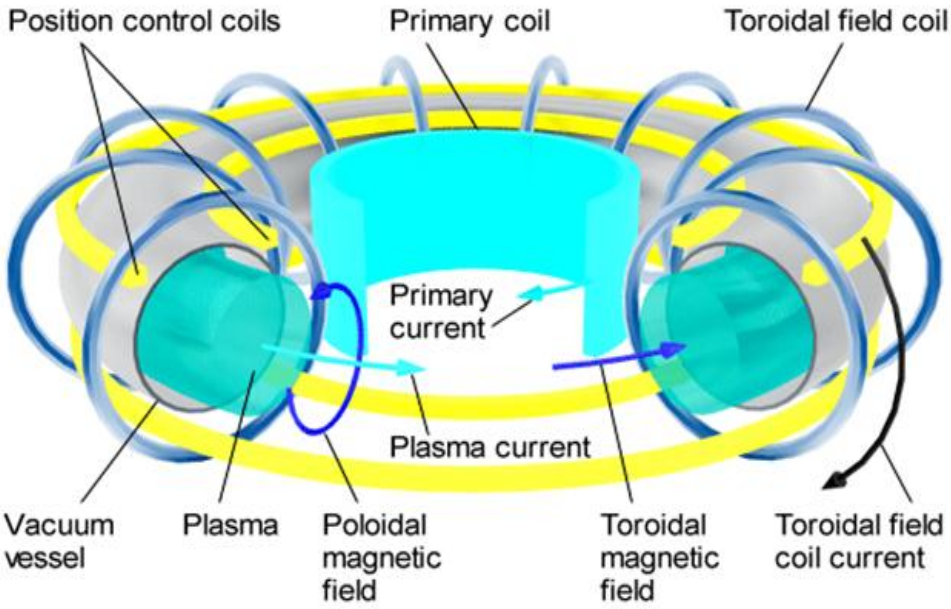

Figure 1.1 (Magnetic Fields in a Tokamak)

the torus shaped confinement helically are required. Such a field is generated by adding two individual magnetic field components. One is a toroidal field which moves in circle throughout the torus and the poloidal field is perpendicular to the toroidal field. The toroidal field is produced by the electromagnets around the tokamaks and the poloidal field is generated by the plasma current flowing in the torus. In a nuclear fusion, such a method of magnetic confinement is used because no other methods of solid confinements can withstand such high temperatures of the plasma.

1.3 Need of an Integrating System

Magnetic pick-up or induction coil circuits are used to measure magnetic fields. Any change in the magnetic flux produces a current whose direction opposes the change. The induced voltage is equal to the rate of change of flux (N = $\oint_S B.ndS$) in Webers per second.

$$\text{E.M.F E} = \frac{dN}{dt}$$

The change in shape of the plasma, change of strength of the magnetic field or movement in the circuit causes a change in the flux. The required flux is measured by integrating the output signal with respect to time.

1.4 Importance of Integrator in Plasma Reactor

The output of the pick-up coil can be integrated digitally or in analog circuit to obtain the value of magnetic field **B**. An easy integration method is to use passive elements like a resistor (R) and a capacitor (C).

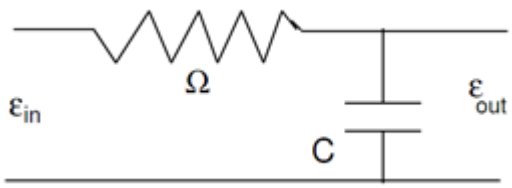

Figure 2.2 (Passive Integrator)

The output voltage can be expressed as

$$\frac{d\epsilon_{out}}{dt} + \frac{\epsilon_{out}}{\tau} = \frac{\epsilon_{in}}{\tau} \quad \text{..... (1.1)}$$

where $\tau = \Omega C$ is time constant. The solution of this equation gives the integration of the input signal.

Another method is to use an opamp based active integrator. The circuit is as shown below:

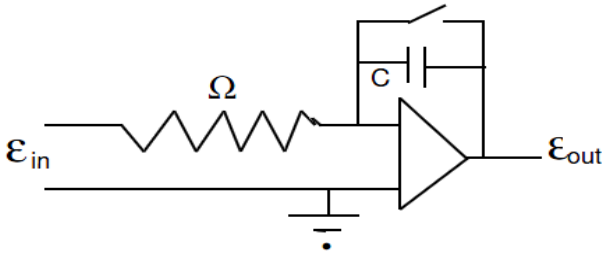

Figure 1.3 (Active Integrator)

The output voltage is given by the following equation:

$$\varepsilon_{out} = \frac{1}{\Omega C}\int_{t1}^{t} \varepsilon_{in} dt \quad \text{..... (1.2)}$$

1.5 Methods of Integration

Various methods of integration used in different tokamaks are:

1. Analog integration technique using an A/D-register-D/A(A/D: analog to digital converter, D/A: digital to analog converter).
2. The mixed analog digital integrator using DSP with a fast ADC.
3. The alternating analog integrator consisting of two individual integration modules.
4. The digital integrator with tri VFC-UDC units (VFC: Voltage to frequency converter, UDC: up down counter)

1.6 Literature Review

1.6.1 Existing References

The purpose of this survey is to give us a prerequisite knowledge on the topic undertaken in this thesis and to stress the significance of the present study.

An analog integrator is generally used in a plasma control system to integrate the output signals of the induction coil sensors and find the magnetic field values. In many tokamaks several types of digital integrators have been devised for measuring the magnetic field with accuracy. Bak et al. [1] have developed an automatic integrating drift compensating analog integrator for KSTAR tokamaks. A couple of differential amplifiers added to the signal path between the magnetic sensors and the integrator enhance the performance of the integrator. The analog integrator which has ADC- register- DAC (ADC- Analog-to-Digital Converter, DAC- Digital-to-Analog Converter) stages in the integrator makes up for the integration drift. The resolution is moderately high at 16-bits. The integrator system is

controlled by a PC (Personal Computer) through a serial interface. With proper calibration, the value of the drift is no more than around 10^{-7} Webers per second.

Another digital integrator based on a VFC-UDC (VFC- Voltage-to-Frequency Converter, UDC- Up-Down Counter) has been devised for the tokamak's long pulse integration of magnetic signals. Kurihara and Kawamata [2] devised three trial boards. The first trial board eliminated the technical cause of drift. The precision of the integration was enhanced by the second board. The third board was used for drift suppression. This integrator system is built up on a simple concept of conversion of the voltage signal into frequency so as to reduce any drift in frequency by employing a PLL (Phase Locked Loop). The PLL used is a digital system which counts the frequency from the UDC (Up-Down Counter).

Zhang et al. [3] presented a method to compensate totally for the DC offset and compensate the steady-state error in voltage model flux in a torque control system. This proposed method used a low pass filter and then a high pass filter in series to realise an integrator. To work in different situations, these low pass filter have adaptive cut-off frequencies. Time phasor method is used to derive an error compensation formula, thus making it more convenient for this integrator to be implemented in a digital control system. The new integrator with error compensation also estimates accurate values of steady state flux.

Michael D. Bryant et al. [4] suggested a hybrid signal (analog and digital) approach. Integration is in analog but data is stored and manipulated both in digital and analog. Whenever an analog integrator voltage equals or surpasses an onset voltage, a quantity of charge equal to the onset voltage is cleared from the feedback capacitor of the analog integrator. Then, the counter is incremented or decremented as required. This integrator

system works with voltage even greater than the saturation level without the operational amplifier entering into saturation and avoids drifts arising out of low pass filtering.

A different version of the analog integrator implemented in Tore Supra for the purpose of magnetic measurements was designed by Defrasne et al. [5]. Though established on the identical principles, this proposed integrator was upgraded in order to fulfil the long duration of pulses, with time period up to 1000 s, for ITER (International Thermo-nuclear Experimental Reactor). The automatic compensation scheme, usually a sample and hold amplifier, is also established on an integrator amplifier. Hence, the identical care must be taken with its outer capacitor. Modifications have been made to the thermal drift of the compensation system. When the sample and hold is in hold mode, there is no feedback on the input amplifier, so when differential input voltage increases, during the measurement phase, the amplifier soaks and temperature and the drift rises. Now a switch to ground the S/H input has been implemented and, as a result, the temperature of components has reduced.

1.6.2 Objective of the Present Thesis

The exhaustive literature analysis suggests different methods for integrating the output signal from the magnetic pick-up in tokamaks. Still there needs to be improved methods for handling long pulse plasma discharges. The main challenges to be dealt with are designing of long time constant integrator system which can eliminate the effects of offset induced integration drifts, occurring due to very high temperatures in the confinement during the discharge. In our thesis, we have implemented a different approach to tackle the offsets by utilizing twin OPAMP single IC integrating platforms followed by subsequent stages to deal with low level signals and environmental noise effects.

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Chapter 2

INTEGRATOR SYSTEM DESIGN

2.1 Block Diagram

The basic block diagram of the proposed integrator system as presented in this thesis looks as follows:

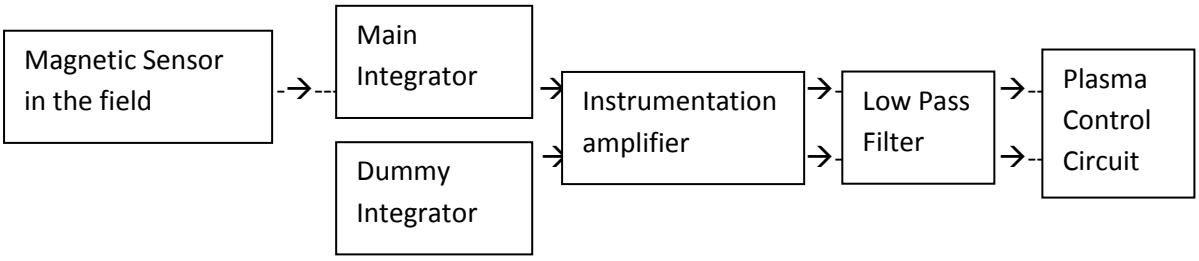

Figure 2.1 (Block Diagram of the Integrator System)

The circuit diagram of the integrator system is given as shown in Figure 3.2. A dual operational amplifier is used to design the two integrators. The input of the main integrator is connected to the coil and the input of the dummy integrator is grounded. Then, the instrumentation amplifier (INAMP) is used to subtract the output signal of the dummy integrator from the output signal of the main integrator, so the output of the instrumentation amplifier is the integration signal which compensates the drift. By using these techniques, the integration drift caused by the DC offset and temperature related drift of the operational amplifier can be eliminated in real time integration [6].

2.2 Circuit Design Considerations

Let's consider the initial conditions to be $v_0(t)$=0 at t_o=0. The output of the simple integrator can be written as

$$v_0(t) = -\frac{1}{RC}\int_{to}^{t}(v_i(t) + RI_{OS} - V_{OS})\,dt \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (2.1)$$

where $v_i(t)$ is the input signal, V_{OS} is the input offset voltage and I_{OS} is the input offset current. As the expression suggests the integration drift is a combined effect of voltage and offset currents. The main integrator integrates the input signal, whereas the dummy one has 0mV as input as both the terminals are grounded. Taking the input offset voltages and currents to be V_{OS1}, V_{OS2} and I_{OS1}, I_{OS2}, respectively.

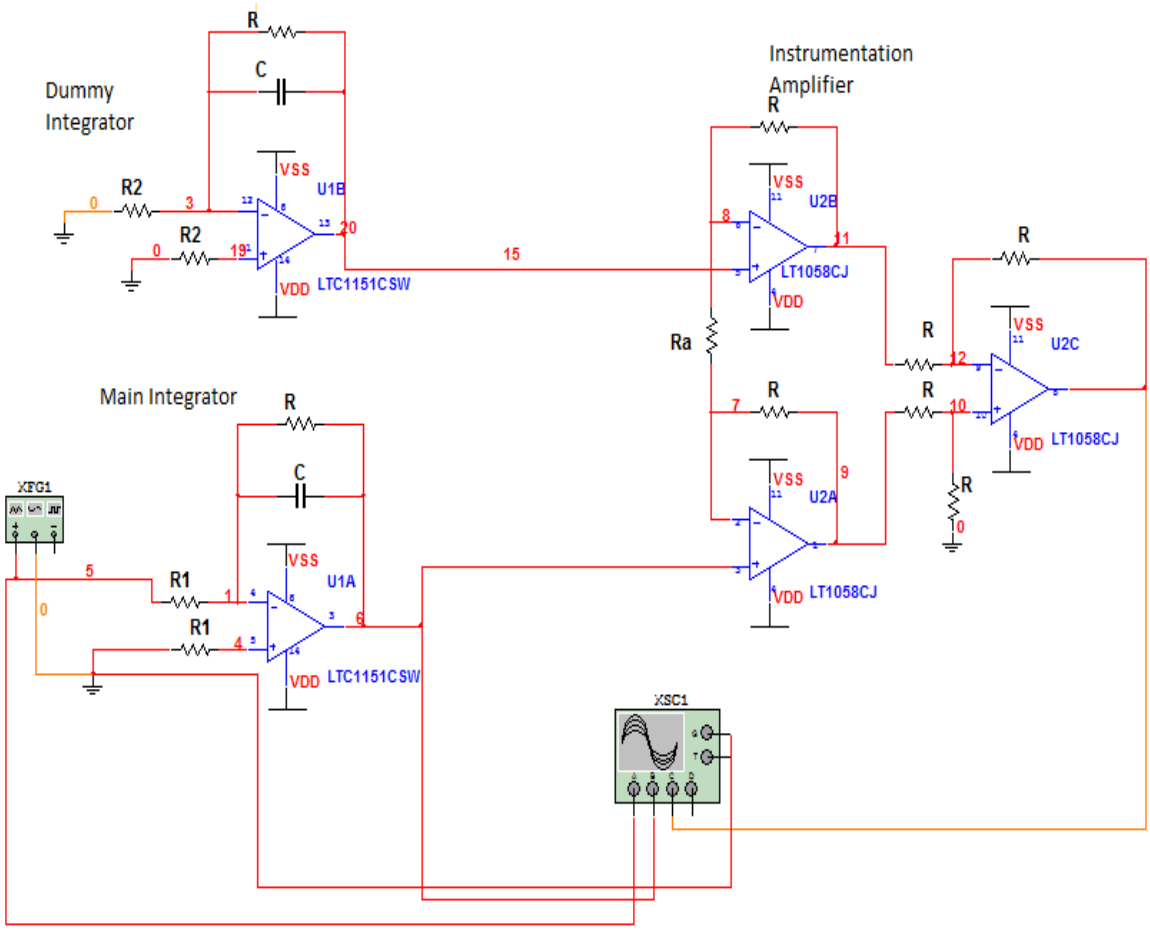

Figure 2.2 (Circuit Diagram of the Integral Module)

The difference between outputs of both the integrators is given by

$$v_0(t) = v_{01}(t) - v_{02}(t)$$

$$= -\frac{1}{R_1C}\int_{to}^{t}(v_i(t) + RI_{OS1} - V_{OS1})\,dt + \frac{1}{R_2C}\int_{to}^{t}(RI_{OS2} - V_{OS2})\,dt$$

This gives:

$$v_0(t) = -\frac{1}{R_1C}\int_{to}^{t}(Vi(t))dt + (t\text{-}t_0)\left[\frac{(R_2\, I_{OS2}) - V_{OS2}}{R_2C} - \frac{(R_1\, I_{OS1}) - V_{OS1}}{R_1C}\right] \quad \ldots\ldots\ldots\ldots\ldots (2.2)$$

To eliminate integration drift the second term should be zero, i.e.

$$\frac{(R_2\, I_{OS2}) - V_{OS2}}{R_2C} = \frac{(R_1 I_{OS1}) - V_{OS1}}{R_1C} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2.2)$$

The above equation can be easily met by varying the resistor R_2 of the dummy integrator. Moreover, for a dual operational amplifier fabricated on an IC (Integrated Circuit) the values of offset voltages and offset currents of the two operational amplifiers closely match each other.

2.3 Parameter Analysis of the Tokamak

Table 2.1 (Required Parameters in Tokamak)

a.	Long pulses are up to 1000 seconds or longer.
b.	Time constant RC is 20ms.
c.	Total integration drift should be less than 20mv.
d.	The typical offset should be 0.5 uV and offset current 20pA.
e.	And an average input offset drift needs to be 0.01 uV/ °C.
f.	The low pass filter at the output stage has a cutoff frequency of 800Hz

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Chapter 3

INTEGRAL MODULE

3.1 Integrator Design Using OPAMP

3.1.1 Derivation of Integration Expression

By placing a capacitor in the feedback path of an inverting configuration of an operational amplifier, we can realize the mathematical operation of integration. Let us apply a time varying input $v_i(t)$ to the negative input terminal of an operational amplifier with a feedback configuration, as shown in Figure 3.1. This applied voltage appears across the resistor (R) due to the virtual ground and a current $i_1(t)$ equal to $v_i(t)/R$ flows through the feedback path, thus charging the capacitor C.

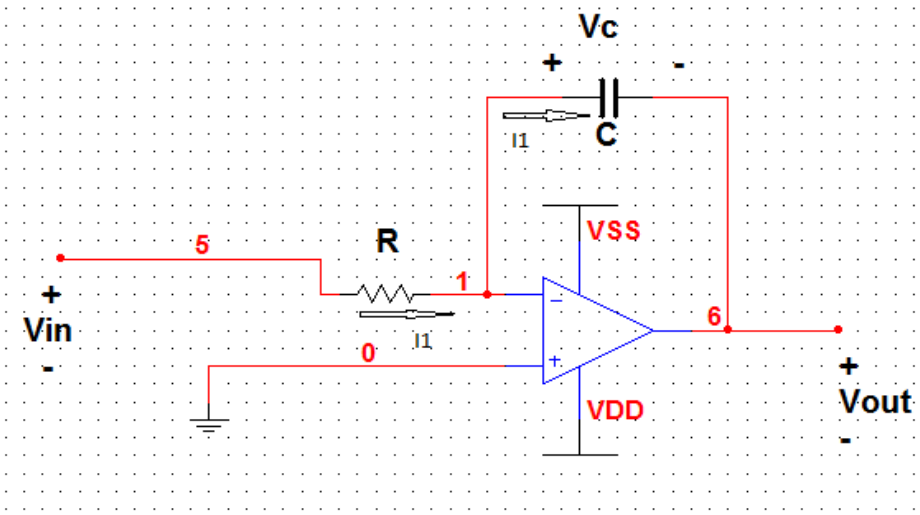

Figure 3.1 (Integrating Operational Amplifier)

The output voltage is $v_o(t)$. Considering in Laplace Domain,

$$X_c = \frac{1}{j\omega C} = \frac{1}{sC}$$

$\frac{Vo(s)}{Vi(s)} = -\frac{1}{sCR}$. Converting back to the time domain we get the expression,

$$v_o(t) = -\frac{1}{RC}\int_{t0}^{t} v_i(t)\,.\,dt \quad \text{.....(3.1)}$$

3.1.2 Miller Integrator

The above integrator works fine with AC voltage input of high frequencies. But with input frequencies which are very low or DC inputs the capacitive reactance is very high, hence no current flows through the feedback path and we get no output. To avoid this effect, we add a resistor (R) in parallel with the capacitor. This helps us to achieve a constant DC gain at very low frequency.

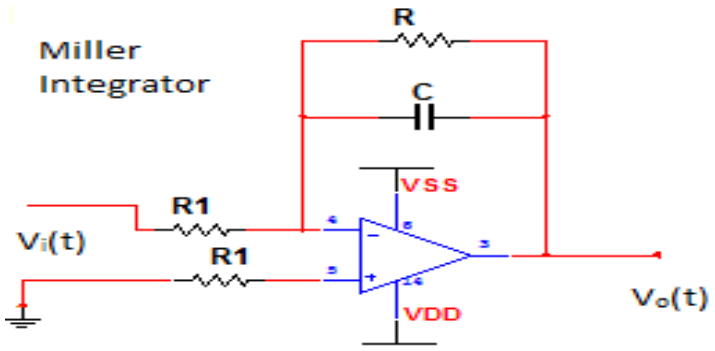

Figure 3.2 (Miller Integrator)

The DC gain is given by - $\frac{R}{R1}$. The time constant is given by R_1C. At any frequency other than DC the feedback path impedance is given as

$$Z_f = \frac{R}{1+sCR}$$

3.1.3 Effect of DC Offset in Integration

DC offset is a serious problem which has to be accounted for in almost all operational amplifiers. If the two inputs of the amplifier are grounded. It will be found that a finite DC offset voltage exists at the output. This is because an error offset voltage at the input stage is amplified due to the large open loop gain of the operational amplifier. Such a phenomenon often corrupts the amplified signal.

During integration DC offset causes serious problems as much as saturating the output. If a finite DC offset exists at the input stage of the integrator, any long time integration of the signal produces a ramp voltage output which if continued for a long time rises to the rail voltage level. This seriously corrupts or even loses the actual input signal to be integrated. This effect can be mathematically shown as:

$$V_o(t) = -\frac{1}{RC}\int_{t0}^{t} v_i(t).dt$$

where $v_i(t) = V_{os,}$

V_{os}, being constant with respect to time can be brought out of the limits of integration. This gives $V_o(t) = -\frac{1}{RC} Vos \int_{t0}^{t} dt = -\frac{1}{RC} Vos(t-t_o)$ (which is a ramp function).

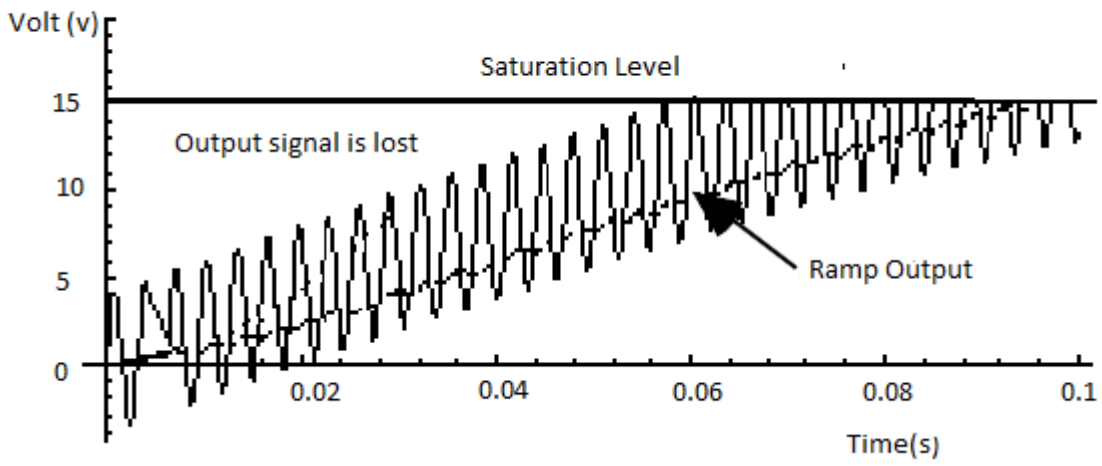

Figure 3.3 (Effects of DC offset)

3.2 Instrumentation Amplifier Design

Instrumentation amplifiers (INAMP) are used in many applications like automotive and various data acquisition systems. The INAMP is a closed loop gain block which has very high input impedance in the order of several mega-ohms and low output impedance. It also has a property to neglect common mode signals.

3.2.1 Basic Differential Amplifier

The differences between two input signals are amplified by the basic differential amplifier. The figure below shows the circuit diagram of the differential amplifier:

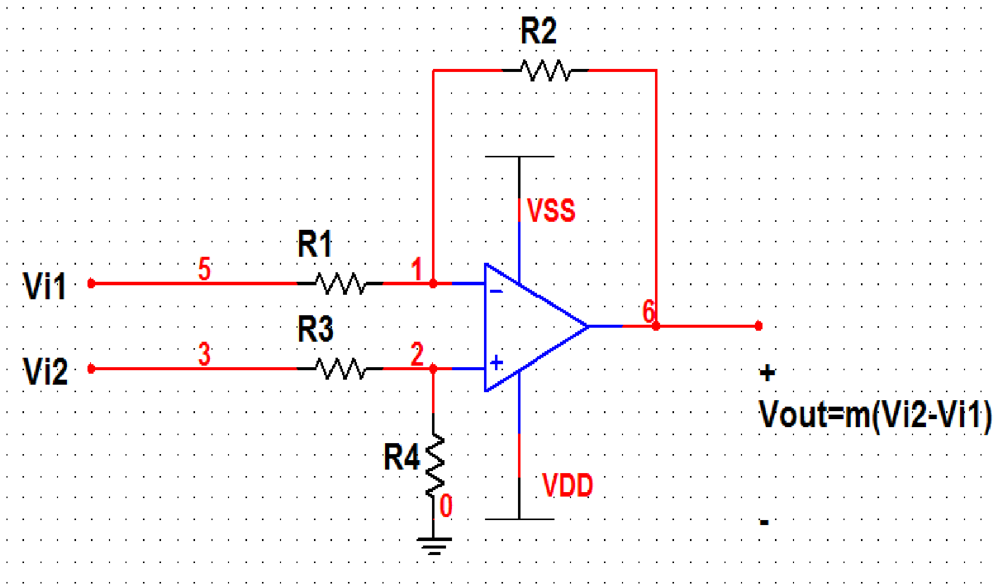

Figure 3.4 (Basic differential amplifier circuit)

To obtain the differential signal, the inverting and non-inverting gains needs to be equalized, where

$$\text{Inverting gain} = -\frac{R_2}{R_1}$$

$$\text{And the non-inverting gain} = \left(1 + \frac{R_2}{R_1}\right)\left(\frac{R_4}{R_3+R_4}\right).$$

Now balancing both the gains, we get

$$\left(1 + \frac{R_2}{R_1}\right)\left(\frac{R_4}{R_3+R_4}\right) = .-\frac{R_2}{R_1} \quad \text{(3.2)}$$

$$\Longrightarrow \quad \frac{R_4}{R_3+R_4} = \frac{R_2}{R_1+R_2}$$

$$\Longrightarrow \quad \frac{R_4}{R_3} = \frac{R_2}{R_1} \quad \text{.....(3.3)}$$

Proceeding with these conditions, the output voltage equations can be written as follows

$$v_{o2} = \frac{R_4}{R_3+R_4}\left(1+\frac{R_2}{R_1}\right)v_{i2} = \frac{R_2}{R_1}v_{i2}$$

$$v_{o1} = -\frac{R_2}{R_1}v_{i1}$$

Using superposition principle, the output voltage can be written as

$$v_o = v_{o1} + v_{o2} = \frac{R_2}{R_1}(v_{i2} - v_{i1}) = \frac{R_2}{R_1}v_{id} \quad \text{..... (3.4)}$$

The following circuit is used to determine the common mode rejection of the differential amplifier

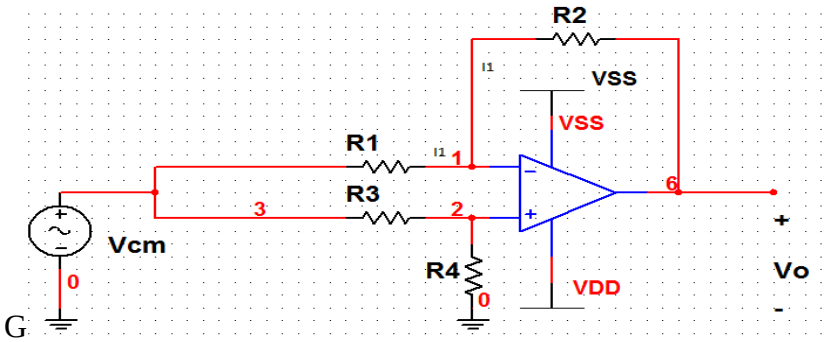

Figure 3.5 (Circuit for determination of common mode rejection)

The current i_1 is given by:

$$i_1 = \frac{1}{R_1}(V_{icm} - \frac{R_4}{R_3+R_4}V_{icm})$$

$$= V_{icm}\cdot\frac{R_4}{R_3+R_4}\cdot\frac{1}{R_1} \quad \text{..... (3.5)}$$

Therefore the common mode output voltage will be:

$$v_o = V_{icm} \cdot \frac{R_4}{R_3+R_4} - i_1 R_2$$

$$= \frac{R_4}{R_3+R_4}\left(1 - \frac{R_2}{R_1}.\frac{R_3}{R_4}\right)V_{icm} \quad \text{..... (3.6)}$$

If the condition $\frac{R_4}{R_3} = \frac{R_2}{R_1}$ is satisfied, then v_o, i.e. common mode output voltage becomes zero.

3.2.2 Issues in Common Differential Amplifiers

- A slight mismatch in resistors can change the CMR drastically. Because of loading effect, the effective resistances $R_3$and R_1 are changed
- To minimize the loading effects, the differential amplifier should possess a very high input impedance. But in this configuration, the $R_{id} = 2R_1$only.
- If we need high gain $\frac{R_2}{R_1}$, R_1should be low, which in turn will minimize the input impedance.

3.2.3 Instrumentation Amplifier

The shortcomings of a common differential amplifier can be overcome by using an instrumentation amplifier [7], whose circuit diagram is shown below

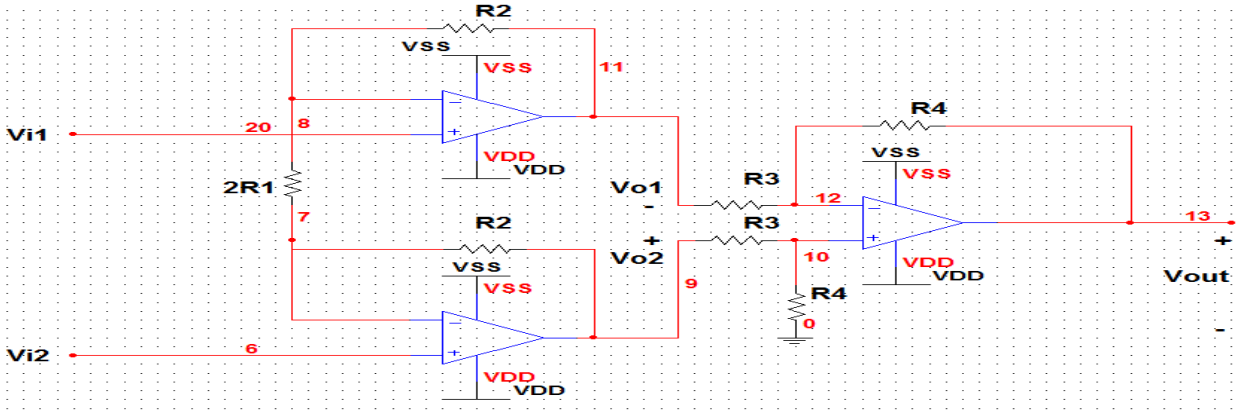

Figure 3.6 (Instrumentation amplifier circuit)

Here, $$v_{id} = v_{i2} - v_{i1}$$

$$v_{o2} - v_{o1} = \frac{v_{id}R_2}{2R_1} + v_{id}.\frac{2R_1}{2R_1} + v_{id}.\frac{R_2}{2R_1}$$

$$= v_{id}\left(1 + \frac{2R_2}{2R_1}\right) \quad \text{..... (3.6)}$$

So, the output voltage is: $$v_o = v_{id}\left(1 + \frac{2R_2}{2R_1}\right) \quad \text{..... (3.7)}$$

Let a common mode voltage v_{icm} be applied to both the input terminals which appears in the negative terminals of the OPAMPs in the first stage. So the differential voltage across $2R_1$ will be zero, thus no current flows through R_2. Hence, the first stage doesn't amplify v_{icm} rather it simply propagates v_{icm} to the next stage where this value is subtracted. Only, the differential voltage is amplified. Again, it is easier to change the gain by varying R_1.

3.3 Results and Discussions

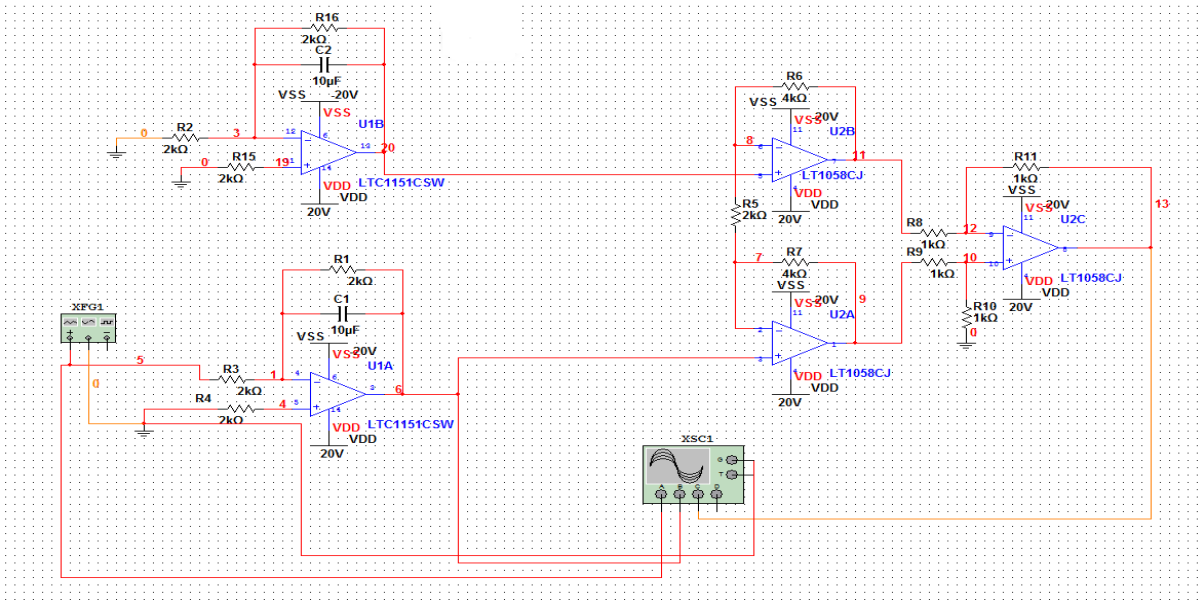

Figure 3.7 (Integral Module Circuit)

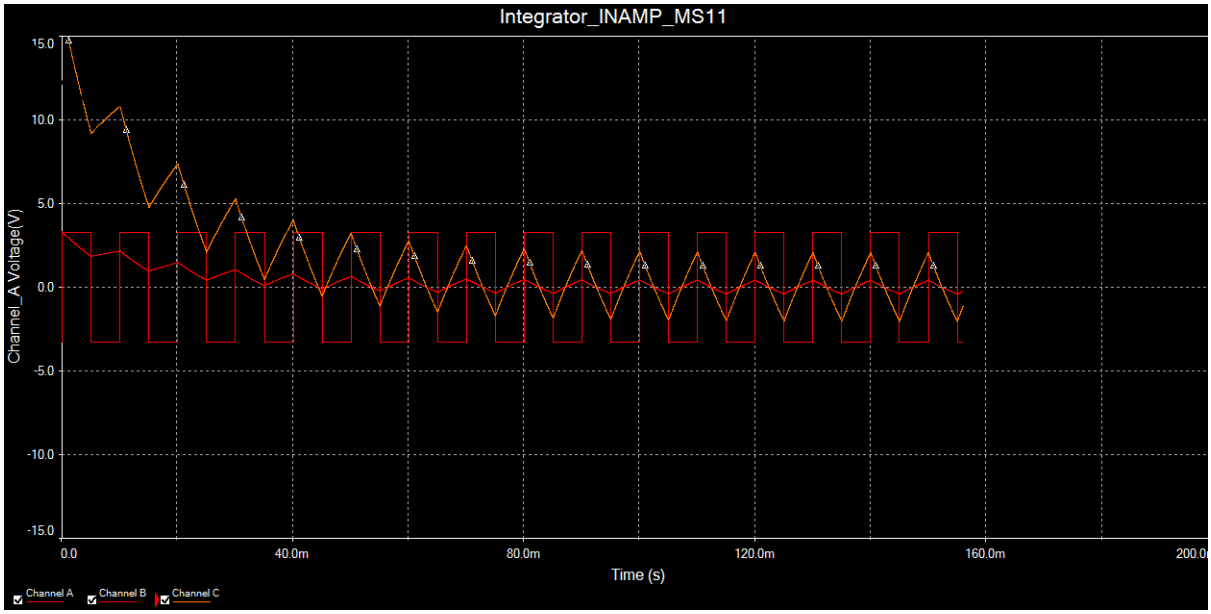

Figure 3.8 (Test Signal Response)

The entire integral module was designed for the tokamak using Multisim Circuit Simulator. The dual opamp IC used is LTC1151 which has typical offset of 0.5 uV, an input offset current of 20pA and an average input offset current of 20pA. The above characteristics are ideal for realizing a low drift integrator. For low frequency operations, miller effect and compensation was used, which involved a resistor to be connected in parallel to the feedback capacitor. The instrumentation amplifier having a gain of 5 was built by using the quad-opamp LT1058 IC package. The above circuit was simulated and tested by giving bipolar square wave voltage of amplitude 3.3V and frequency 30Hz.

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Chapter 4

DIGITAL FILTER DESIGN

4.1 Filter Basics

A filter is a digital circuit which allows signal of a specific range of frequency to pass through it while blocking the signals with frequency outside the range. Based on the components used filters can be passive or active filters. Passive filters are composed of passive elements like capacitors (C) inductors (L) and resistors(R). They don't need any external power sources to operate, nor do they contain any transistors. Whereas active filters contain active elements like operational amplifiers. They need external power sources to operate. Based on the frequency selectivity, filters are of many types. A high pass filter passes signals of frequency larger than a cut-off frequency. A low pass filter does the exact opposite. It passes the signals with frequency less than the cut-off frequency. A band pass filter passes certain range of frequency. It has two cut-off frequencies- a lower cut-off and a higher cut-off frequency. A band stop filter rejects a certain range of frequency specified within the two cut-off frequencies. Analog filters and digital filters are classified on the basis of the domain in which signal processing is done. Analog filters are simple to implement but digital filters are flexible and versatile.

Noises from the instrumentation amplifier and other environmental noises need to be filtered. A low pass filter with cut-off frequency of 780Hz is used. A digital filter was designed for this purpose. Digital was chosen over analog because of many advantages digital signal processing offers over analog signals.

4.2 Comparison of Analog and Digital Filter

Digital filters are less prone to errors compared to analog filters because of absence of passive elements which change their value with respect to factors like temperature. Digital filter are more accurate and have a sharper fall rate compared to their analog counterparts of the same order. Flexibility and re-configurability are the advantages of digital filters over

analog filters. Depending on the speed of the processor, digital processors have a very high speed of processing. For some of these reasons, we designed a digital low pass finite impulse response filter for our integrator system.

4.3 Impulse Response of Filters

The terms finite impulse response (FIR) and infinite impulse response (IIR) are used to distinguish various filter types. The FIR filters are of non-recursive type, whereby the present output sample is dependent on present and past input samples whereas IIR filters are recursive type, where the output at time t is dependent on the present input and past output and input samples. In most of the cases, a finite impulse response filter is preferred over and infinite impulse response filter. This is so because, Finite Impulse Response filters are always stable, easily realisable and provide a linear phase response under specific conditions. Once the filtering stage coefficients are generated, the response is precisely predictable. Since no poles lie outside the unit circle, FIR filters are always stable.[8]

4.4 FIR Low Pass Filter Design

A causal FIR filter of order N is characterised by the transfer function

$$H(z) = \sum_{n=0}^{N} h(n).z^{-n}$$

Such a filter requires N+1 multipliers and N two input addresses as shown as in the figure4.1.

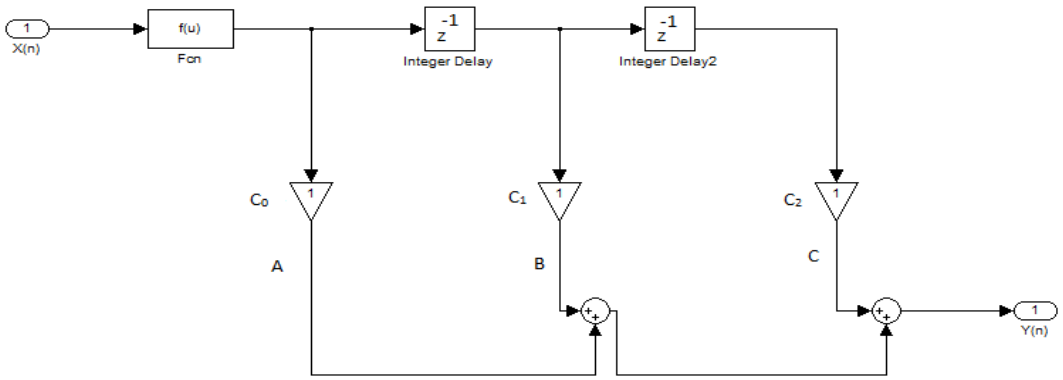

Figure 4.1 (Second Order FIR Filter)

For example, if we take a second order filter, the N = 2. The number of coefficients M = N+1 = 3. Let the three coefficients be C_0, C_1, C_2.

Table 4.1 (Coefficients of Second Order FIR Filter)

Time (t)	A	B	C	Output(Y)
0	C_0	0	0	C_0
1	$2C_0$	C_1	0	$2C_0 + C_1$
2	$3C_0$	$2C_1$	C_2	$3C_0 + 2C_1 + C_2$
3	$4C_0$	$3C_1$	$2C_2$	$4C_0 + 3C_1 + 2C_2$
4	0	C_1	$3C_2$	$C_1 + 3C_2$
5	0	0	$4C_2$	$4C_2$
6	0	0	0	0

Let after appending the zeroes the impulse inputs are I = {1, 2, 3, 4, 0, 0, 0}

We get six samples of output which has been shown in Table 4.1 above.

The Windowing technique used here is the Kaiser Window. It is a finite sequence to truncate any infinite impulse input samples to a finite length one. Kaiser Window is given by the following expression:

$$\omega_0(n) = \frac{I_0 * \alpha * \sqrt{1-\left(\frac{2*n}{N-1}\right)^2}}{I_0(\alpha)} \text{ ,for } |n| <= \frac{(N-1)}{2}$$

$$0 \quad , \quad \text{otherwise}$$

where, α is an adjustable parameter and $I_0(x)$ is the modified zeroth order Bessel filter of 1st kind, N is the total number of samples in the window and the n refers to the nth sample.

The total finite impulse response low pass filter transfer function in the z domain is obtained by cascading the window sequence $\omega_0(z)$ with a filtering sequence h(z). The resulting Kaiser Window is superior to other windows because for a given specification, its transition width is very small. By varying α, we can vary the main lobe amplitude. By varying N the main lobe width can be changed. Such a filter is easily customisable using any Digital Signal Processor.

4.5 Results and Discussion

For the design of the filter a DSP starter kit (TMS320C6713) from Texas Instruments was used. First, the desired filter responses were characterised and the filter parameters were calculated. Calculation of the gain amplitude and phase response was set. Next, the coefficient values were calculated. These coefficient values are used with sampled data from an ADC to perform the filter calculation. The block diagram of the entire set-up looked as shown in Figure 4.2.

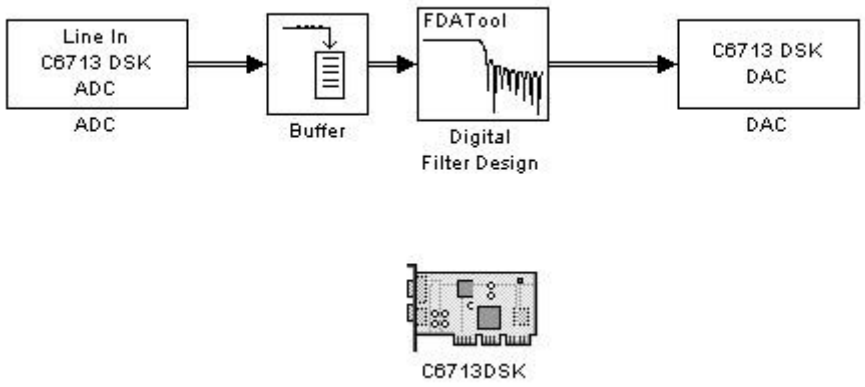

Figure 4.2 (Filter Design in Simulink)

The intended cut-off frequency was 800Hz. So sampling frequency had to be at least 1600Hz (Nyquist's Criteria). We sampled the input signal at a frequency of 3200 Hz. For a sharp fall-off rate, the order of the filter was set at 32. Kaiser Windowing was used. Using Code Composer Studio, the corresponding C code was generated and was dumped on the C6713 kit. Table 5.2 contains the list of all the coefficients of the intended FIR Filter.

Table 4.2 (Numerator and Denominator Coefficients)

sl.no	Numerator:	Denominator:
1	0.0034718191924937953	1
2	-0.037338622329960561	-5.6182561467182763
3	0.13963361872738039	15.289201031785465
4	-0.27871341879444267	-26.843327398512553
5	0.3534955707068696	34.168499886694271
6	-0.32706613836414949	-33.594292289698508
7	0.25117950439234832	26.541750818144411
8	-0.15934699165813471	-17.308380453778234
9	0.073291139881891482	9.4963784056814546
10	-0.033797335698494316	-4.44609052910688
11	0.021739788862581249	1.7953854225389847
12	0.001651469631588832	-0.63043344911925303
13	-0.0030397740504490185	0.19369965784591675
14	-0.011573208634188202	-0.052319917947598535
15	-0.0059179212156750694	0.012466489534582452
16	0.006690780589167682	-0.0026264974295875116
17	0.013353933863004696	0.0004899564464414777
18	0.0066907805891678633	-0.00008096178873070817 3
19	-0.0059179212156743261	0.00011845418416291873
20	-0.011573208634186302	-0.00001532415012481816

21	-0.0030397740504492527	0.00000017488047003373642
22	0.0016514696315886325	-0.00000001754505849478609 8
23	0.021739788862581252	0.00000000154019738645099 63
24	-0.033797335698494371	-0.00000000011757097056505082
25	0.073291139881891773	0.00000000000774074798499293 81
26	-0.15934699165813437	-0.00000000000043489504946883722
27	0.25117950439234826	0.00000000000002055704626681 4324
28	-0.32706613836414955	-0.00000000000000080204688574 23726
29	0.35349557070686966	0.00000000000000002514567436260234
30	-0.27871341879444272	-0.00000000000000000060894327392 7011
31	0.13963361872738042	0.00000000000000000001069124778 66974
32	-0.037338622329960582	-0.00000000000000000000012110114635826
33	0.0034718191924937958	0.00000000000000000000000664430917873 02

The frequency response was plotted as shown in Figure 4.3.

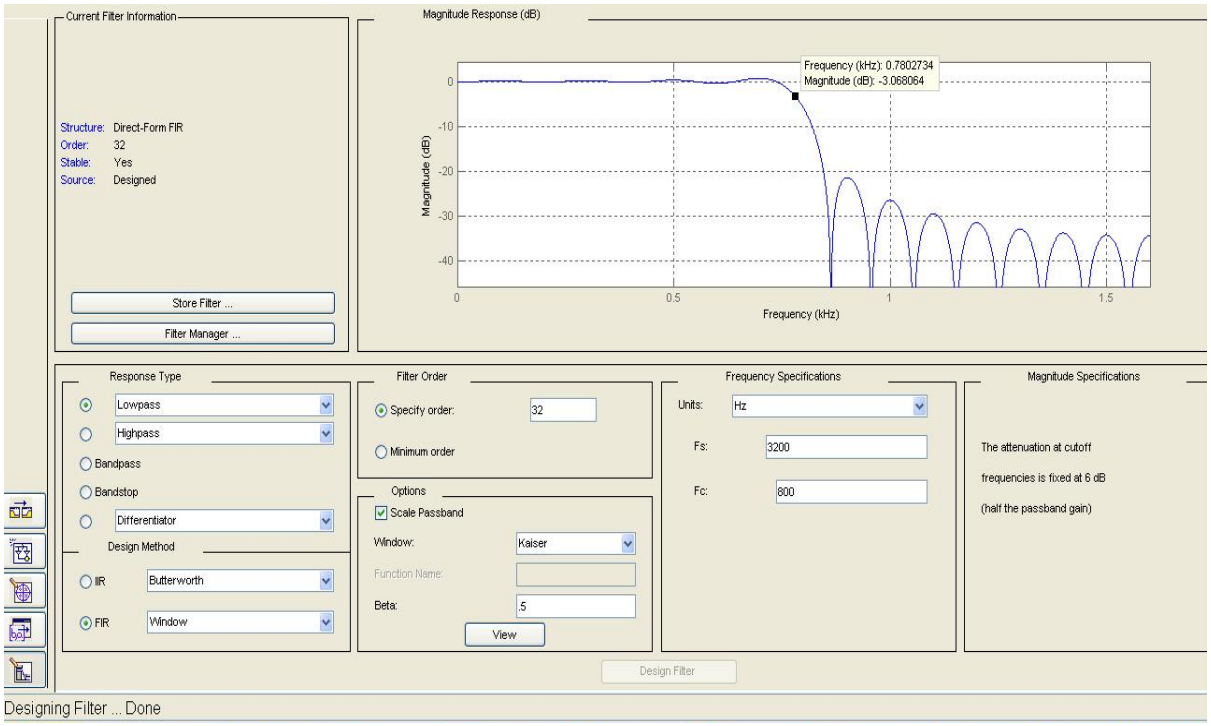

Figure 4.3 (Frequency Response of the designed FIR Filter)

The 3 dB cut-off frequency was obtained at 780 Hz. We observed that the fall rate was steeply high at 400 dB/Hz centred around the cut-off frequency. Although side lobes are present, they are below the main lobe in amplitude by more than 20 dB and they won't be considered. Due to unavailability of information about actual signal from the plasma reactor, we took an audio signal as input as it contained the same order of frequency components as a

noise signal from a plasma control circuit would contain. This filter could be safely applied to tokamak applications.

The pole zero plot of the designed filter was found as given by Figure 4.4

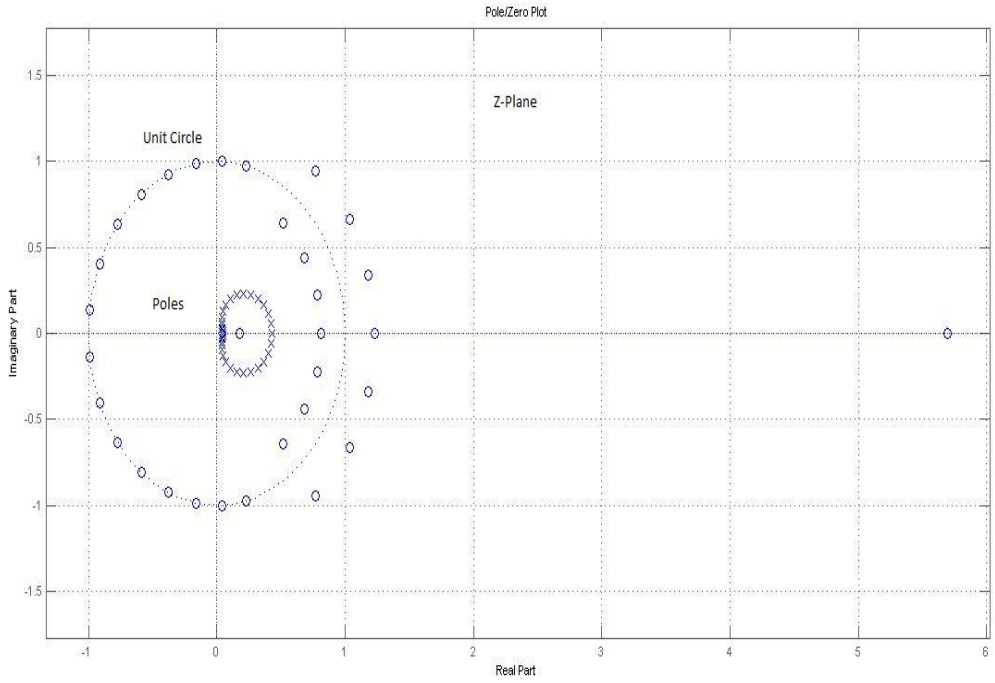

Figure 4.4 (Pole Zero plot of the designed FIR Filter)

A digital filter is deemed stable if all its poles lie within the unit circle. Our results confirm the fact. As always, the FIR filter was found to be very stable for noise elimination applications in a tokamak.

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Chapter 5

OPAMP AND INAMP DESIGN USING CADENCE

Cadence design tool, a product of cadence design system, consists of different platforms to design full custom ICs, digital ICs and mixed signal circuits. In this thesis, we have used cadence to get a layout-ready circuit for our proposed integrator system.

5.1 Basic OPAMP Design

The operational amplifiers are controlled sources which have very high forward gain; such that the closed loop gain becomes insensitive to gain of the opamp when negative feedback is applied. The opamp forms the building block of many circuits. CMOS opamps involve two or more gain stages to improve the overall amplification. There are four stages in a basic opamp-

1. Current mirror
2. Differential amplifier
3. Differential to single ended stage
4. Output Buffer

The general block diagram of the opamp is shown below:

The differential transconductance stage acts as the input of the opamp and sometimes converts the differential signal to single ended output. This stage also provides substantial differential gain improving noise and offset performance. In case, the single ended

conversion is not performed, it is done in the following stage which involves an inverter. For driving the low resistance load, an output buffer is provided in the final stage.

5.2 Specifications of OPAMP Design

- A_v> 5000 V/V ICMR = -1 to 2V
- V_{DD}= 2.5V V_{SS}= -2.5V
- SR>10V/μs BW= 20 KHz
- $C_{L=}$ 15 pF

5.3 Simulations and Results

A two stage operational amplifier was designed meeting the above conditions [9] using cadence 180nm technology. Different circuits were made to determine the characteristics of the opamp. An instrumentation amplifier circuit was done in cadence using the designed opamp and the results and characteristics were verified for different gains.

5.3.1 Two Stage OPAMP Design Using Cadence

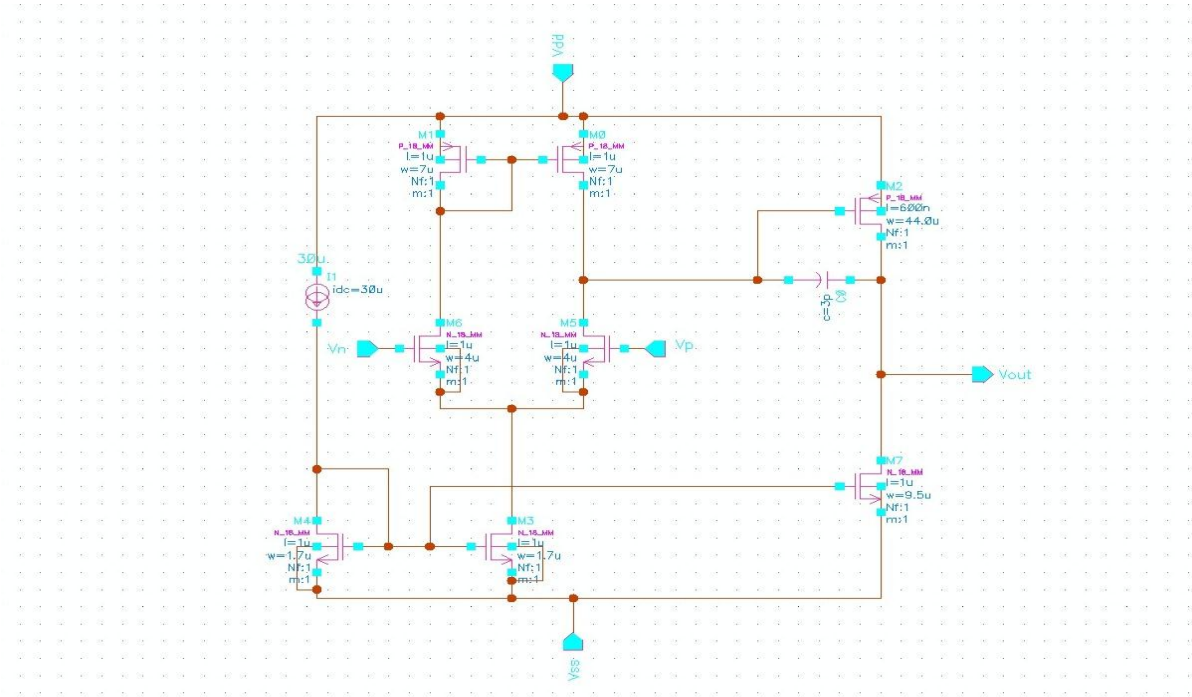

Figure 5.1 (Two Stage OPAMP Circuit)

5.3.2 AC Response of Designed OPAMP

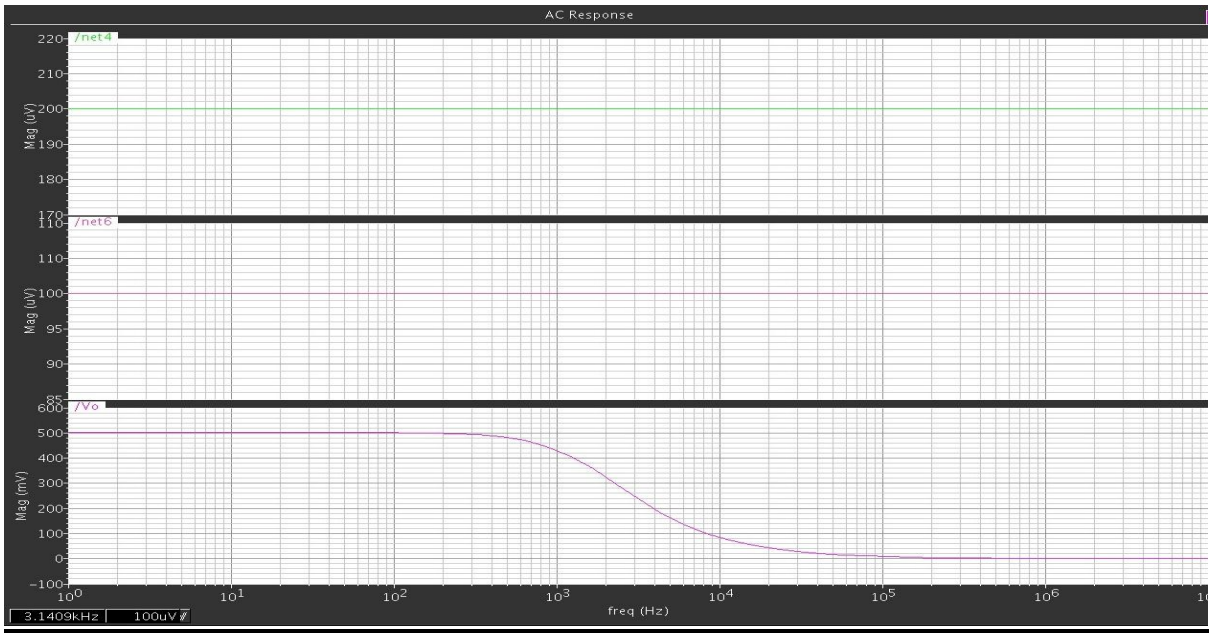

Figure 5.2 (AC Response of OPAMP)

The differential ac inputs of 100uV and 200 uV were applied to the input terminals of the designed opamp. The output obtained was 500 mV. So open loop gain was 5000V/V for lower frequencies.

5.3.3 Differential Gain vs. Frequency

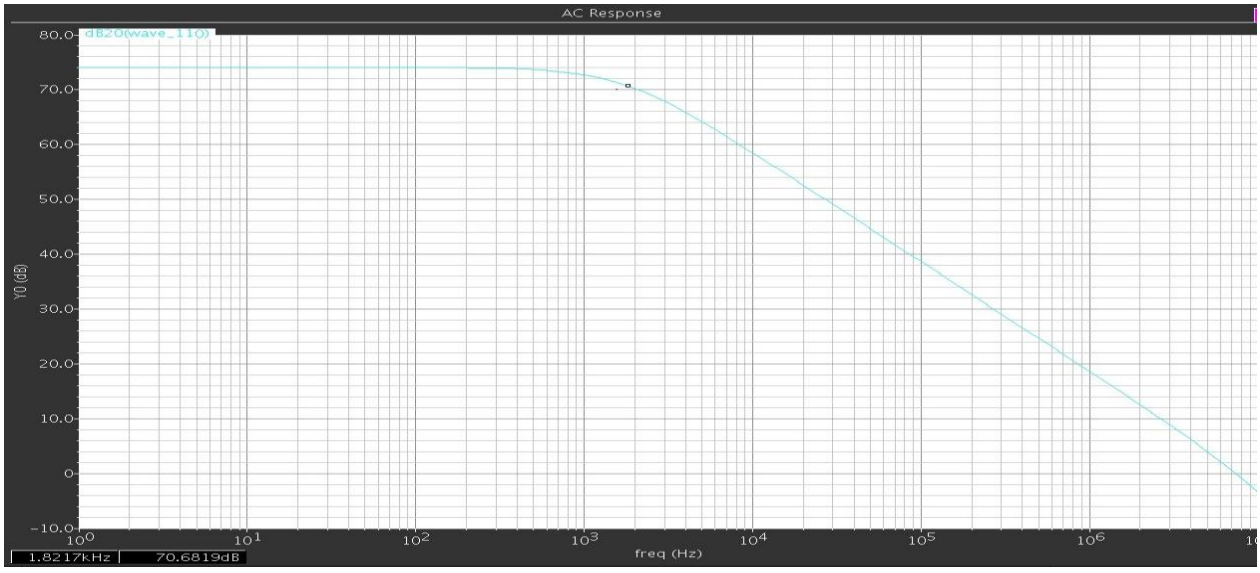

Figure 5.3 (Differential Gain vs. Frequency)

5.3.4 CMRR vs. Frequency

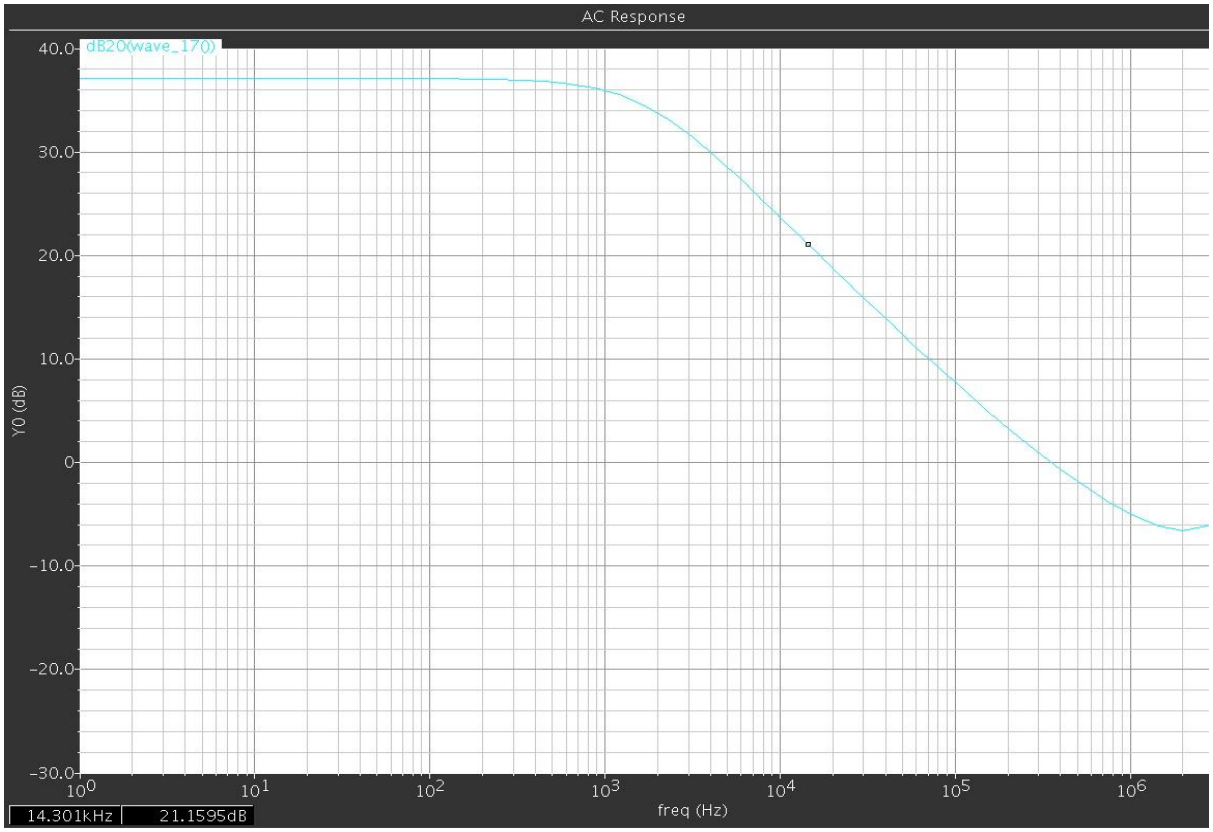

Figure 5.4 (CMRR vs. Frequency)

The Common Mode Rejection Ratio is defined as the ratio of the differential voltage gain to the common mode voltage gain. Here, the CMRR (Common Mode Rejection Ratio) is found to be 40 dB.

5.3.5 Slew Rate Determination

Slew Rate is defined as the maximum rate of change of output voltage. It is expressed by the following formula.

$$SR = \frac{dv_0}{dt}$$

In our design the slew rate was found to be equal to11 μV/sec.

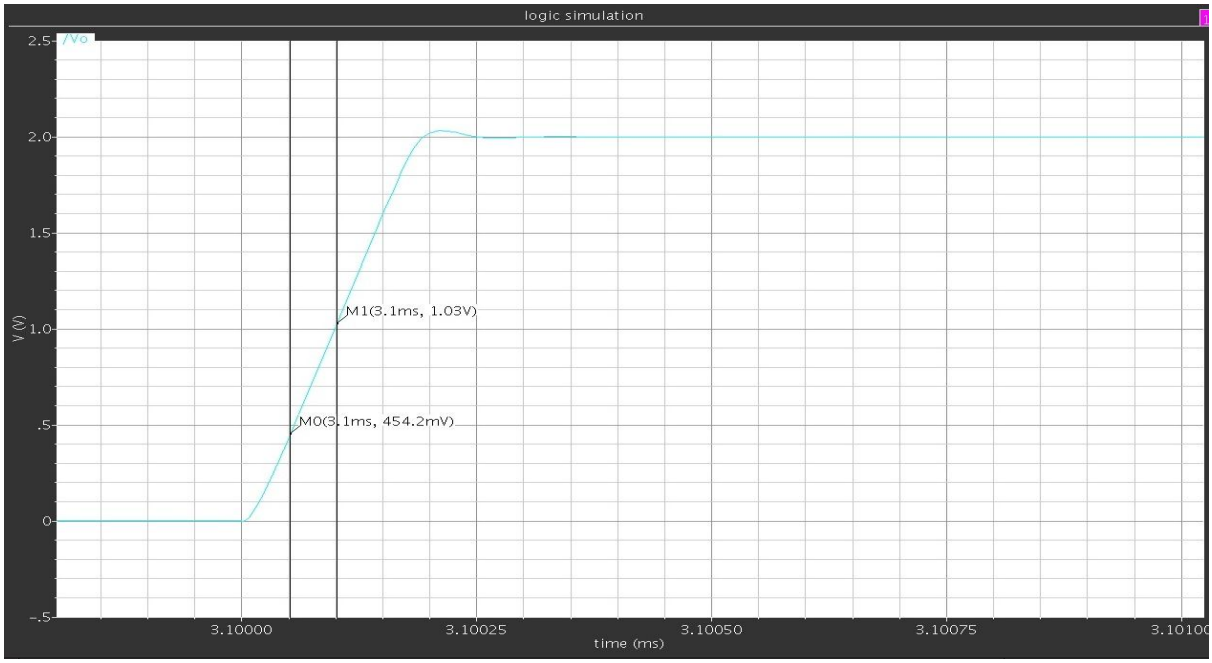

Figure 5.5 (Slew Rate Determination of opamp)

5.3.6 INAMP Circuit Design Using OPAMP

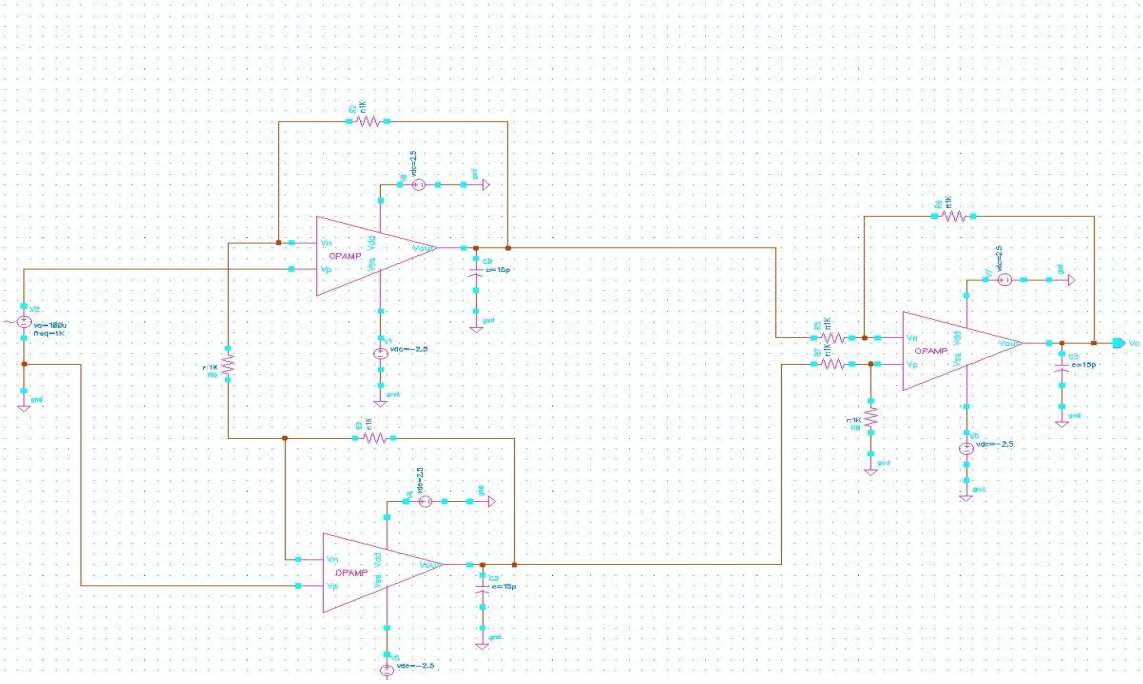

Figure 5.6 (INAMP Circuit Using OPAMP)

The designed opamp block was used in the circuit shown in Figure 5.6 to implement the instrumentation amplifier.

5.3.7 Transient Characteristics of the INAMP

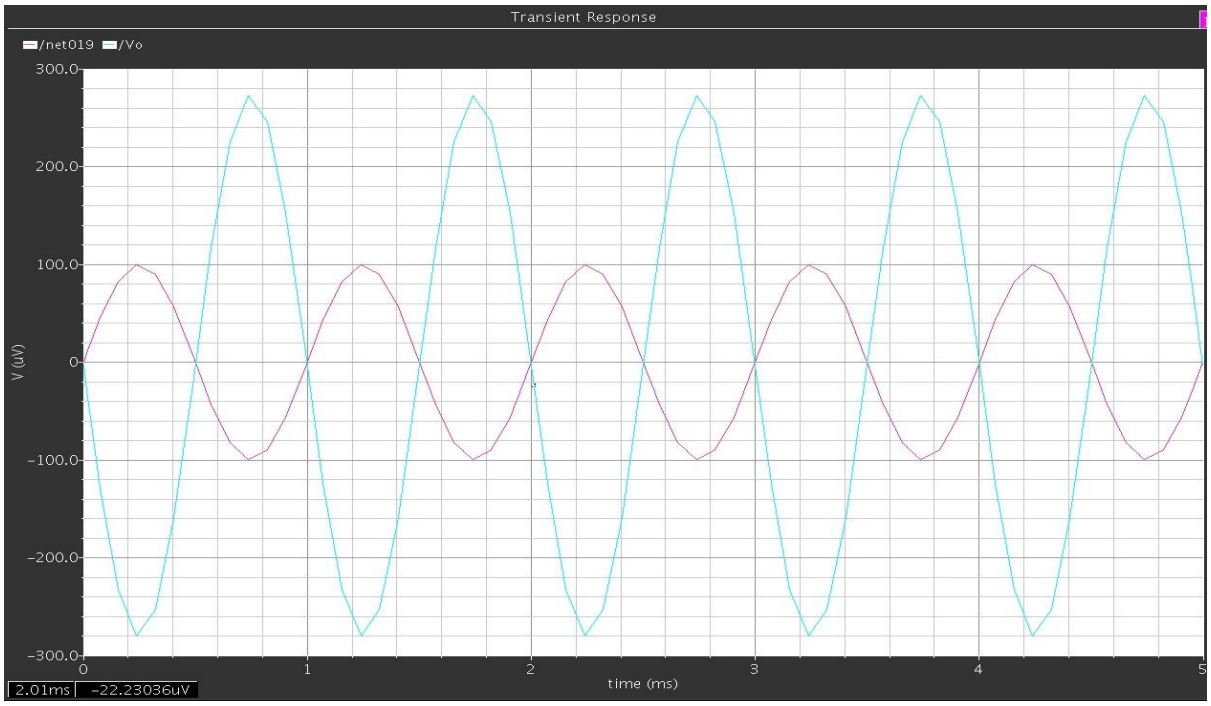

Figure 5.7 (Transient Characteristics of Designed INAMP)

The resistances values used in this circuit were 1 kΩ for all the resistors. The maximum gain for the instrumentation amplifier is given by the following formula.

$$gain = (1 + \frac{2R_2}{2R_1})\frac{R_4}{R_3}$$

Calculating the value from the results obtained in Figure 6.7 the gain was found to be nearly equal to 3 which is same compared to the gain calculated by using the formula.

5.3.8 CMRR vs. Frequency Response of INAMP

Common Mode Rejection Ratio is defined as the ratio of the common mode voltage gain to the differential voltage gain. It is generally expressed in logarithmic scale.

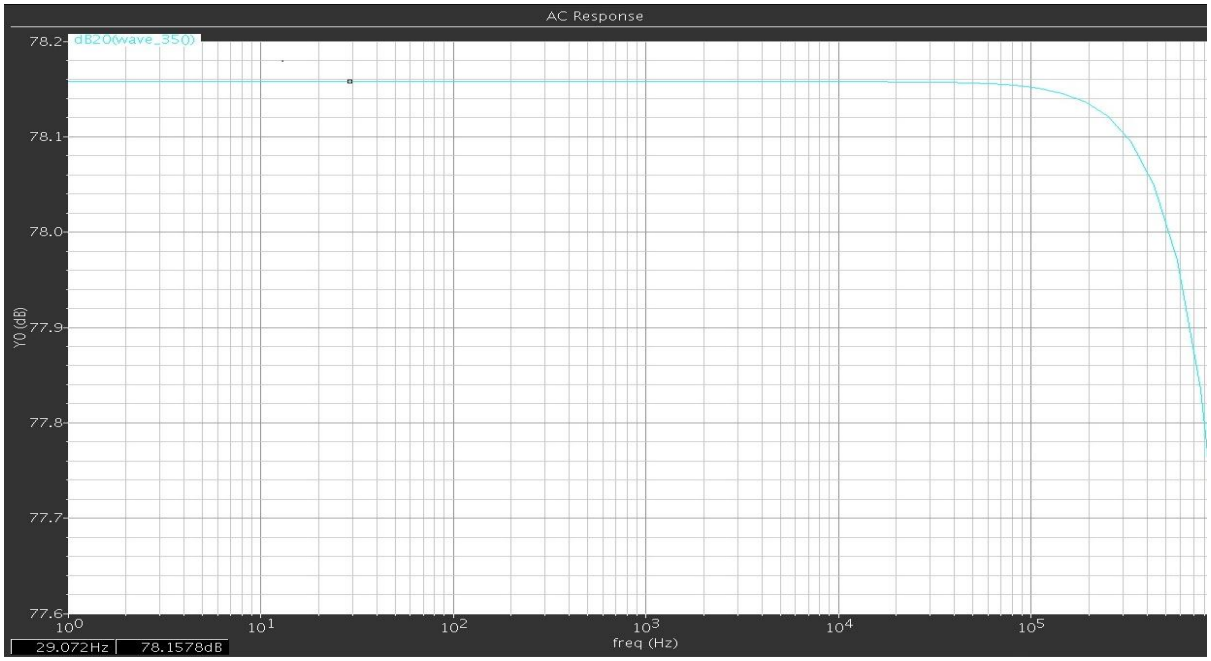

Figure 5.8 (CMRR vs. Frequency of INAMP)

The CMRR of the instrumentation amplifier was found out to be more than 75 dB which is clearly greater than the CMRR value of a normal operational amplifier. Due to this property of the high CMRR, instrumentation amplifier is generally useful in supressing common mode signals arising out of noise and DC offset.

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Chapter 6

CONCLUSIONS

6.1 Contributions

In our thesis, the integrator system whose model has been developed not only helps in reducing DC offset effects but also it enables a mixed signal approach for removing any unwanted noises. For low frequency operations the miller compensation technique was proposed and simulated. The instrumentation amplifier stage was designed for avoiding loading effects and for required amplification during subsequent processing. Here the pulse frequencies are assumed to be very low so that a low pass filter with cut off frequency 780Hz can remove the unwanted signals present during data acquisition. The filter was a digital filter for providing better accuracy, flexible operations, higher order design implementations and faster response. The FIR filter which was realised on a Texas Instruments TMS320C6713 starter kit involving a Digital Signal Processor (DSP) was based on Kaiser Windowing technique. The Kaiser Window is superior to other windows because for a given specification, its transition width is very small and amplitude of main lobe is easily variable by changing the value of α.

The basic stage of opamp design was done using Cadence 180 nm technology. The characteristics graphs which were obtained gave desired results. The main objective was to develop the complete lay-out-oriented circuit for the designed integrator. The opamp was used in realizing the basic INAMP for verifications of results. The cadence tools can be used to produce low power, high efficiency integrator system layouts which can be effectively used in tokamaks.

6.2 Scope for Future Work

The design is part analog and part digital, hence, it should be integrated to be laid out on a chip. This design needs to be tried out on a real IC to test its robustness and real time

response. Since capacitors are involved in the feedback, leakage effects need to be taken into account. In the analog design 20V supply voltage sources have been used, but for an IC layout supply voltages compatible with the nanometer technology of the design need to be used. Test signals consisting of bipolar pulses occurring at regular but long time intervals could be developed to simulate the actual signals-on the-field and then the response of the circuit could be checked for low frequency signals. The complete integrator system can be implemented using CMOS technology in Cadence and one can have an optimized and drift compensating ‘dual integrator IC’, instead of a ‘dual opamp IC’ to build the integrators.

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