National Institute of Technology
Rourkela

HCS12 based embedded PWM Controller for battery charger application

A thesis submitted in partial fulfillment of the requirements for the degree of

Bachelor of Technology in
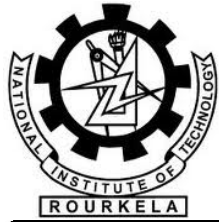### Electronics & Communication Engineering

By:

Darshani Rautray

(108EC032)

Under supervision of:

Dr. Kamala Kanta Mahapatra

CERTIFICATE

This is to certify that the thesis titled "*HCS12based embedded Pulse Width Modulation Controller for battery charging application*", submitted to the National Institute of Technology, Rourkela by **Ms. DarshaniRautray**, Roll No**. 108EC032**for the award of the degree of Bachelor of Technology in Electronics & Communication Engineering, is a bona fide record of research work carried out by her under my supervision and guidance.The candidate has fulfilled all the prescribed requirements. The thesis, which is based on candidate's own work, has not been submitted elsewhere for a degree/diploma.

In my opinion, the thesis is of standard required for the award of a Bachelor of Technology degree in Electronics & Communication Engineering.

To the best of my knowledge, she bears a good moral character and decent behavior.

Prof. K. K. Mahapatra

Department of Electronics & Communication Engineering

National Institute of Technology

Rourkela ‑ 769 008 (INDIA)

ACKNOWLEDGEMENTS

DECLARATION

I hereby declare that the project work entitled "HCS12 based embedded PWM controller for battery charger application" is a record of my original work done under Dr. Kamala KantaMahaPatra, Professor, National Institute of Technology, Rourkela. Throughout this documentation wherever contributions of others are involved, every endeavor was made to acknowledge this clearly with due reference to literature. This work is being submitted in the partial fulfillment of the requirements for the degree of Bachelor of Technology in Electronics and Communication Engineering at National Institute of Technology, Rourkela for the academic session 2008 – 2012. The results embodied in this thesis have not been submitted to any other University or Institute for the award of any degree or diploma.

Darshani Rautray

CONTENTS

Figures and Tables

Tables

ABSTRACT:

With present wireless communication revolution, possession of mobile phones, MP3 walkmans, Ipods, Ipadsthe convenience of quick and easy communication, information storage and search, the situation has also brought to concern certain issues regarding their operation.

Every cell phone comes with a rechargeable battery and battery charger. The devices like PDA, MP3 Walkman, and digital cameras all require batteries to operate, adding to the importance of rechargeable batteries.

The cellphone batteries get damaged due to overcharge and subsequent signal deterioration due to absence of charge. Overcharging the battery will lead to lessening the battery life.

Li-ion and Ni-Cd batteries are well suited to portable devices like cell phones, walkmans, by virtue of their small size and weight. However, life cycles of the batteries are easily affected due to overcharging and undercharging.The reason being that overcharging damages the physical components of the battery. On the other hand undercharging reduces the energy capacity of a battery.

Thus,arises the need for an intelligent voltage and current controlled PWM microcontroller based battery charger to prevent the overcharging. The battery charger application will include an electromagnetic interference filter,bridge rectifier,transformer,switching that operates with the help of a microcontroller unit of a PWM controller.A current detection block,voltage detection block and a temperature detection block are feedback through differential amplifiers into the Analog to Digital conversion unit of the microcontroller. Microcontroller facilitates advanced user interface.

The application aims at efficient battery performance, safety and cost.

1

Battery Charging Characteristics

INTRODUCTION

Before heading to the design, we must thoroughly understand the charging cycle of a battery to design the charger according to the specifications. At different stages of charging, the process undergoes certain changes .The batteries are applied an initial charge,followed by a regime of full charge/discharge cycle. Most of thepopulationofbatteries used in portable devices are namely the**nickel–cadmium**, **nickel-metal-hydride** and **lithium–ion**.
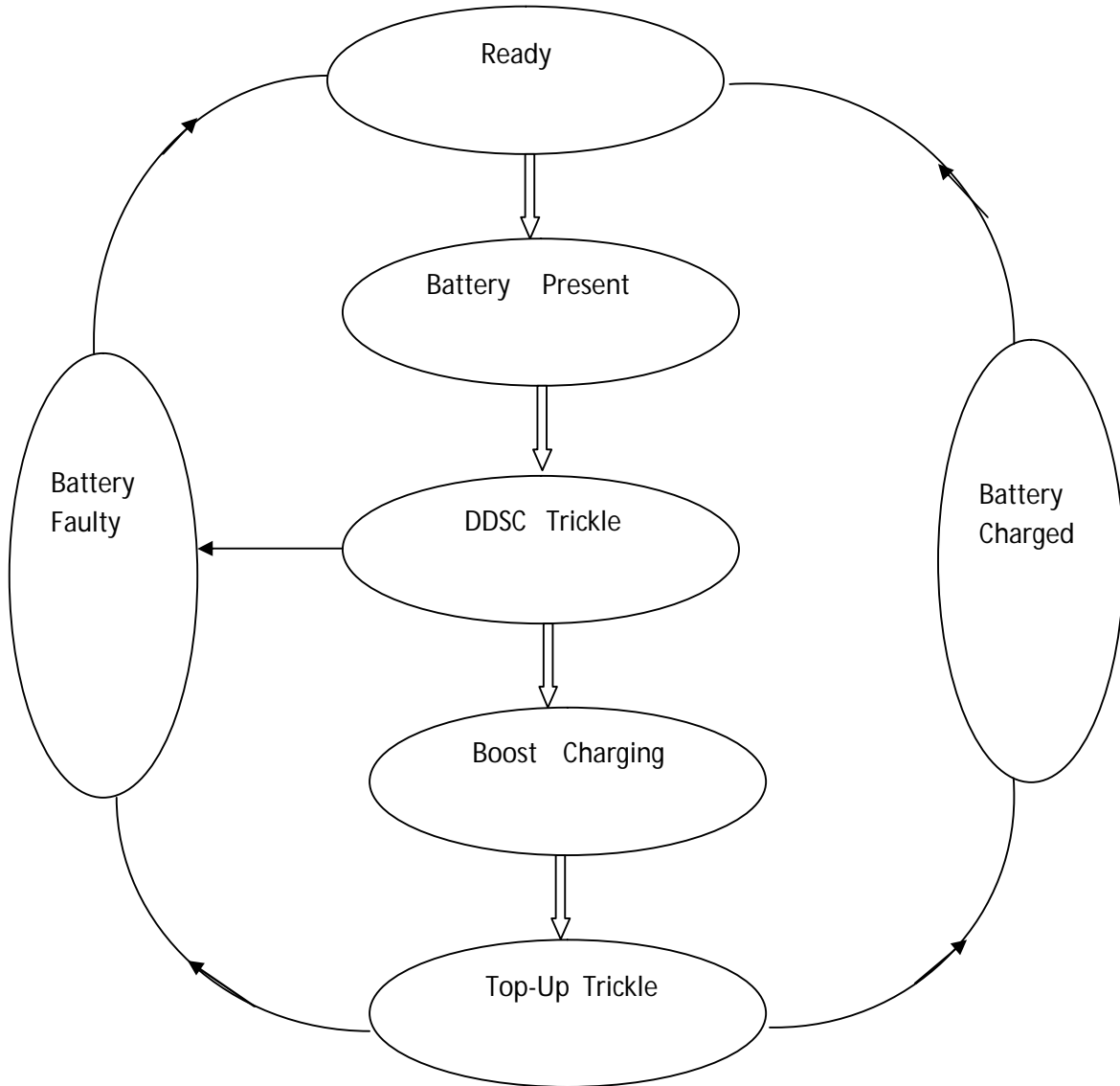
1.1 The Charging Cycle

Fig 1.1

The high density batteries like Ni-MH and Ni-Cd get charged rather rapidly in 1 to 2 hours,if a proper charging method is used. It is essential to monitor the allowed operating conditions so that they are not violated.

- Capacity:
  - ❖ This value indicates the amount of current a battery is able to supply for a certain period of time.
    For example: A battery with capacity 500 mAh, supplying 500 mA continuously for 1 hour, this charging current of 500 mA is called 1C. Larger the battery capacity measured in mAh implies longer supply of current by the battery.

- Trickle Charging:
  - ❖ The fixed charging of 0.1 C, C standing for the rated battery capacity is applied to the battery. It charges the battery typically through 16 to 18 hours. Charging beyond this limit however can damage the battery.
  - ❖ Ni-MH cells are observed to be more vulnerable to damage as compared to Ni-Cd cells, and they get damaged when exposed extended trickle charging at rate greater than 0.1 C. The trickle charging current for Ni-MH should be limited to the bounds of 0.033 C to 0.05 C to the damage that may occur to the battery with the upper limit of 18-20 hours.
- Boost Charging:
  - ❖ If a fixed charging current of 0.3 C or 0.5 C is applied and the charging time is typically 3 to 4 hours. On completing the boost cycle, the charger steps down to a trickle charge to top up.
  - ❖ A fixed charging current of 1C or 1.5 C is applied with a charging time of typically 1 to 2 hours followed by top up at low current.
    The procedure of charging is continuously monitored to check the battery temperature to avoid any damage caused by overcharging.
- Determination of End of Charge Condition :
  - ❖ With the increase in the charging rate, probability of battery damage due to overcharging increases. Hence, it is important for the accurate termination of the fast charging when the battery is fully charged. The deciding parameters for the termination of battery charging are the rate of change of battery temperature (dT/dt) and the battery voltage (dV/dt) with time.
- Detection of the dV/dt Point:
  - ❖ Ni-MHhave charging characteristics which show small fall in voltage towards end of the boost charging cycle. This is determined as the dV/dt (also called -Δ V) point. At this point the charger shifts from boost charging to trickle charging. The phenomenon is more pronounced for NiCd batteries. In the case of NiMH battery , the voltage drop of 5-10 mV/cell from peak is observed at the end of charge condition.

- Detecting the dT/dt Point:
  - ❖ As the battery reaches near completion of charge, a gas is produced which creates an internal pressure and sudden temperature rise.

❖ The temperature rise is acceptable reaching the peak of 50°C to 60°C in Ni-MH batteries. Such sudden rise in temperature can be used to terminate the charging. As ΔV is not easily detected, the overcharging can happen.

❖ Thus dT/dt termination has to be followed.NiMH/Ni-Cd batteries can be charged at higher rates of 1C to 1.5 C followed by the rise in temperature of1^0C/min to 2^0C/minute is observed at the end of charge condition.The temperature rise observed is more abrupt in NiMH batteries as compared toNi-Cd batteries .

.

1.2 The Charge Detection

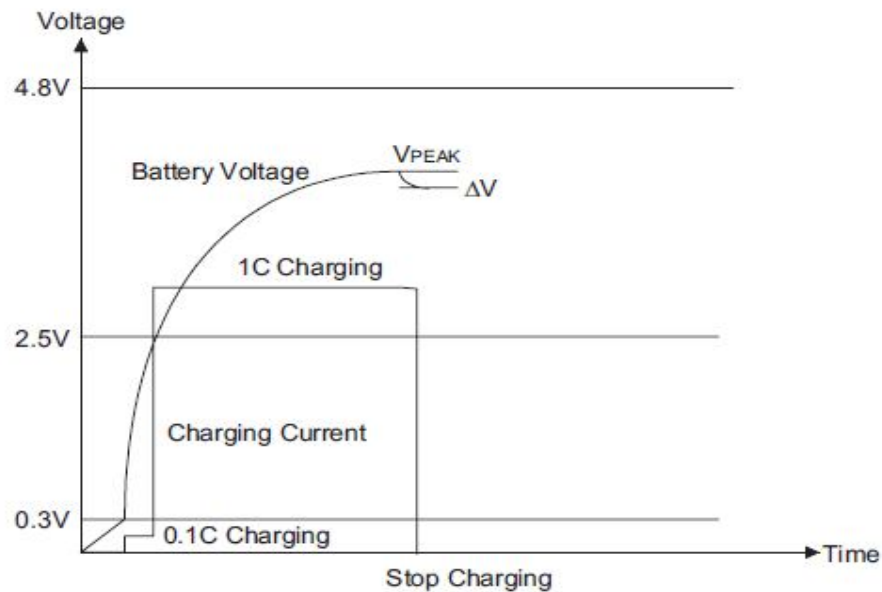Charging curve for Ni-Cd and Ni-NH batteries.

Fig 1.2

Terms and definitions:

- Vbat: Battery voltage, the immediate measured value is averaged with previous three measurements .
- Vmax: The safest highest battery voltage allowed.
- VPeak: Max value of Vbat.
- △V : VPeak-Vbat

- Charging methods observed for the Ni-NH and Ni-Cd batteries are the same.The following describes several methods involved in charge detection when full charge condition has been obtained.

    1) V measurement: The battery voltage falls in fully charged condition. When successive reductions of 10mV is detected 8 times ($\triangle$V>10mV for 8 times), the battery will be taken as being in fully charged state.

    2) Vpeak measurement: If Vbat is found to be less than Vpeak after a considered time period of one minute, then the battery is assumed to be fully charged. If Vbat happens to be greater than or equal to Vpeak after one minute should be reset and after a similar period of time the value should be measured.

    3) Vmax measurement: When the battery is fully charged, it reaches Vmax.

    4) Use of safe timing method: When the charging time happens to be greater than the set up time, the battery can be considered to be fully charged.

    5) Battery Temperature measurement: The temperature will continuously rise, if the charging continues after battery reaches the fully charged condition.This provides a fully charged measurement parameter.

    6) Battery detection: The charger checks voltage on the battery holder from time to time; if this measured voltage exceeds 0.3V then it is assumed that battery has been placed in the charger. If the voltage detected falls below 0.3V then it is assumed that no battery is placed in the holder.

The charging of Ni-Cd battery can be done only after measured voltage on the rechargeable battery exceeds 0.3V. This is inferred as per the above mentioned condition of battery detection.While the fast charging of the battery can only be done after the battery voltage exceeds 2.5V.Until this point has been reached, the battery is charged at a current of 0.1C,after the battery voltage exceeds 2.5V , a fast charging current of 1C can be applied.

When the battery is detected, it is placed in standby condition ready for charging.If after charging,the battery is not removed, it will stay in the standby condition.

1.3 Limitations

Overcharging :

Overcharging, which is the attempt to charge a battery beyond its electrical capacity can cause battery explosion along with possibilities of leakage or irreversible damage.It may also cause damage to the charger that carries out the charging process. When the battery is recharged excessively, a gaseous mixture of hydrogen and oxygen may be produced leading to the pressure build up and the possibility of the bursting.

Memory Effect :

When the Ni-Cd or Ni-NH batteries are recharged without first undergoing full discharging, they will suffer from a reduction in the overall battery capacity called the **Memory Effect.** When voltage falls below 2.2V, the charger will stop the battery discharging and begin the charging cycle automatically.

The Memory effect is also known as **battery effect**, **lazy battery effect** or **battery memory**, that causes the batteries to hold less charge. It describes that Ni-Cd batteries gradually lose their maximum energy capacity because of repeated recharging after being only partially discharged. The battery appears to "remember" the smaller capacity. The result of the effect causes changes in the characteristics of the underused active materials of the cell.

Reverse Charging: Batteries should never be recharged in the reverse. This can lead to leakage or heating of the battery. Extreme cases are when the battery bursts due to reverse charging.

<u>Voltage depression due to long term overcharging:</u>

In this problem, the peak voltage of the battery drops at rate faster than normal as it used to, inspite of the total energy remaining almost the same.The battery is observed to be draining very quickly. The effect is ascribed to the memory effect because it appears that the battery is not holding its full charge.

Voltage depression is caused by repeated over-charging of the battery causing rapid discharge, and fall of battery voltage all of a sudden. The effect is observed to be very common in trickle chargers.

<u>Deep Discharge:</u>

Battery can be damaged due to repeated deep discharge.The cell with the smallest capacity may discharge to zero and will then'reverse charge'. This results in loss of capacity which is also often ascribed to memory effect.

Chapter

2
PWM Control

INTRODUCTION

Pulse-width modulation (PWM), or **pulse-duration modulation (PDM),** is a techniqueused for controlling power to inertial electrical devices, which are made practical by modern electronic power switches.

The PWM output necessary to regulate the switching, is obtained here by comparison of the actual value of the parameter under control with its corresponding set point. In the constant voltage mode, the converter voltage is compared with the voltage set point, whereas in the constant current mode, comparison is done between the voltage developed by the charging current across a sense resistor and the current set point.

2.1HCS12 Pulse Width Modulator

The HCS12 microcontroller has a pulse-width modulation module which is capable of giving upto six independent pulse-width modulated waveforms. Once the PWM module is initialized, the outputs will be output automatically without any further action required by the program.

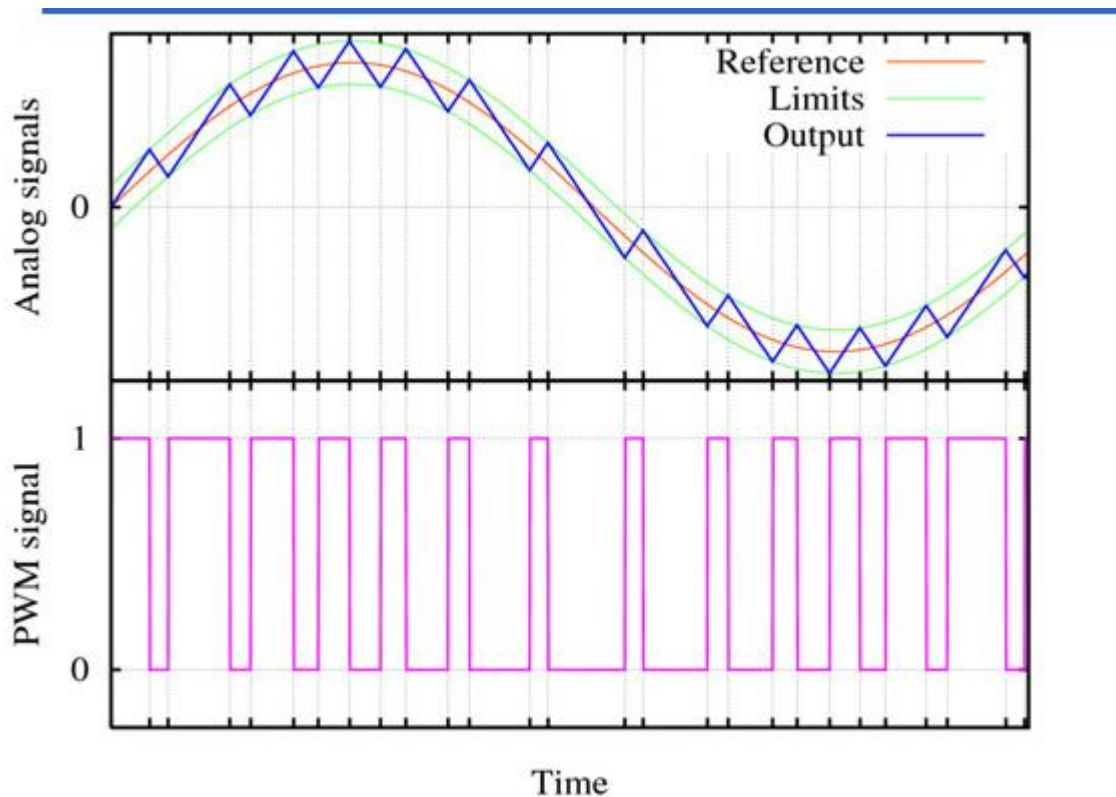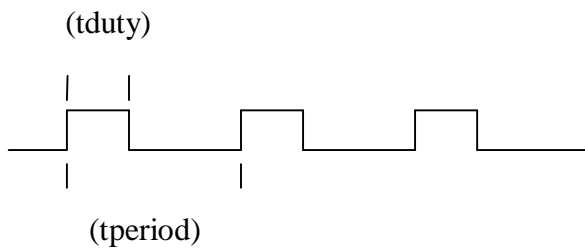There are two time intervals that need to be specified and controlled. These are the following:

Fig 2.1

PWM wave

(tduty)

(tperiod)

1) Period (*tperiod*): Time period of the specified PWM wave frequency.

2) Duty (*tduty*): The time that the output is high.

3) Duty Cycle : Ratio of the*tduty* to *tperiod* and given as a percent.

Duty cycle=(tduty/tperiod)*100%

The pulse width modulation module in the HCS12 comprises of an 8-bit (or 16-bit) **PWMCNTn,** clocked by a clock signal. This clock has been derived by dividing the system bus clock by a prescalar and other division logic and there are upto two clock choices for each PWM channel. There are registers which control the period **PWMPERn** and the duty cycle is controlled by the register **PWMDTYn**. The system is initialized through values in these registers and the clock frequency is selected. When the **PWMCNTn** register is reset, the pulse width modulator output **PWMn**is set high (or low depending on the polarity control bit set in the *.PPoln*register). **PWMCNTn** counts up and once it matches up to the value initialized in the **PWMDTYn** register , the 8-bit *duty cyle comparator* causes the output to go low (or high). As **PWMCNTn** continues to count, it eventually matches up to the value initialized in the 8-bit *period comparator* that sets the output value high (or low) again and resets **PWMCNTn**, to start the process all over again.
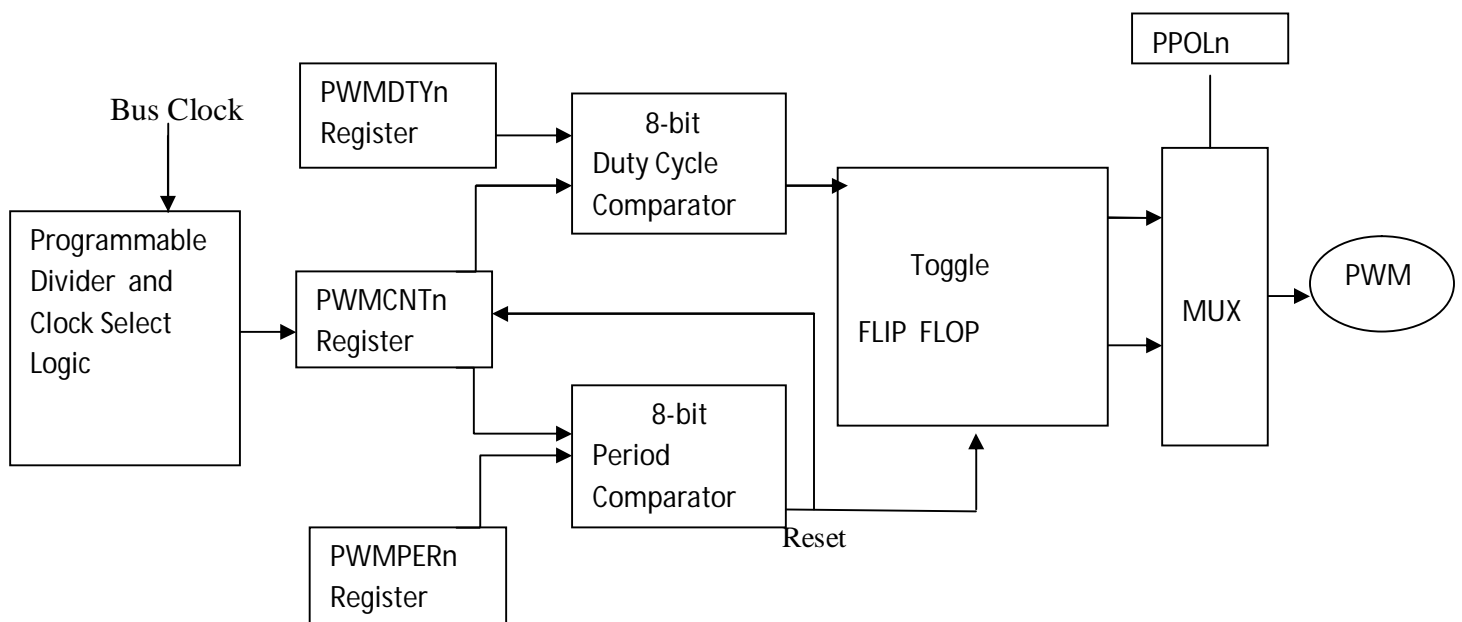

Fig 2.2

The pulse-width modulation registers and the counter register can be concatenated in pairs to obtain 16-bit timing resolution. This results in a longer period and higher duty cycle resolution than can be achieved with the normal 8-bit operation.

2.2 Pulse width Clock Control

The initialization of the PWM module involves the clock select rate, polarity of the output and left or center alignment of the pulses.

The four clock sources derived from system bus clock are the **Clock A, Clock B , Clock SA , Clock SB.** Divider stages for the Clock A and Clock B are controlled by the PWM Prescale Clock Register (*PWMPRCLK).* These two independent clocks may be slower than the bus clock by factor of 1,2,4,8,16,32,64 or 128.

Clock SA and Clock SB are scaled versions of clocks A and B which are produced by the further division of Clock A and Clock B by twice the value in *PWMSCLA* (for clock SA) and *PWMSCLB* (for clock SB) . Clocks SA and SB range from ½ to $1/512^{th}$ the frequency of the clocks A and B.

One of the four clocks is selected through the clock select logic to be used by the PWM channels 0 through 5. This is done by bits in the PWM Clock Select Register (*PWMCLK)* and each channel comes with the choice of two clocks.

PWMPRCLK: PWM Prescale Clock Register Select

0	PCKB2	PCKB1	PCKB0	0	PCKA2	PCKA1	PCKA0

Fig 2.3

PCKB2 PCKA2	PCKB1 PCKA1	PCKB0 PCKA0	Value B Value A
0	0	0	Bus clock (default)
0	0	1	Bus clock/2
0	1	0	Bus clock/2
0	1	1	Bus clock/2
1	0	0	Bus clock/2
1	0	1	Bus clock/2
1	1	0	Bus clock/2
1	1	1	Bus clock/2

Table 2.1

PWMCLK : PWM Clock Select Register

0	0	PCLK5	PCLK4	PCLK3	PCLK2	PCLK1	PCLK0

Fig 2.4

PWM Channel	PCLKn	Clock Source
5	0	Clock A (default)
	1	Clock SA
4	0	Clock A (default)
	1	Clock SA
3	0	Clock B (default)
	1	Clock SB
2	0	Clock B (default)
	1	Clock SB
1	0	Clock A (default)
	1	Clock SA
0	0	Clock A (default)
	1	Clock SA

Table 2.2

2.3 Pulse width Modulator Control Registers

2.3.1 PWM Channel Enable

PWM Channel enable bits *PWMEN5-PWMEN0* in the PWME facilitate the gating of the selected clock signal to be gated to the PWM. The clock prescaler shuts off to reduce power consumption when all channels are disabled.

When the PWM channel is enabled, the output bit gets the signal when the clock source begins its next cycle.

0	0	PWME5	PWME4	PWME3	PWME2	PWME1	PWME0

Fig 2.5

2.3.2 PWM Polarity control

PPOLn bits control the starting polarity of each of the channels, in the PWMPOL register. The output is high at the beginning of the cycle if the polarity bit is 1 and then comes down to low by end of the duty time.

Vice Versa for the PPOLn bit 0.

0	0	PPOL5	PPOL4	PPOL3	PPOL2	PPOL1	PPOL0

Fig 2.6

2.3.3   PWM Centre Alignment Control

The left aligned and centre aligned pulse-width modulated waveforms differ by the fact that the centre-aligned pulse have twice the period value given by the PWMPER register. This alignment is controlled by the PWMCAE register.

0	0	CAE5	CAE4	CAE3	CAE2	CAE1	CAE0

Fig 2.7

2.3.4   PWM Concatenate Control Register

Channels 4 and 5, 2 and 3, 0 and 1 can be concatenated if the requirement is of 16-bit PWMs.

0	CON45	CON23	CON01	PSWAI	PFRZ	0	0

Fig 2.8

PSWAI : stops in wait mode

PFRZ: counters stop in freeze mode

2.3.5   PWM Channel Counter Registers

Each channel is associated with a dedicated 8-bit up down counter for itself, which runs at the selected clock source rate. The counter allows itself to be read at any time without any changes to the PWM waveform.

In the left aligned mode , the counter starts at $00 and counts up to the value set in the Period register -1 (PWMPERn-1). In the centre aligned mode, the counter counts up from $00 up to the value stored in the period register and then back down to $00.

PWMCNT5-PWMCNT0

7	6	5	4	3	2	1	0

Fig 2.9

The channel counters have values which are compared with the values set in the channel period registers and the duty cycle registers. A counter is set to $00 and it is directed to set anytime that it is written to. The duty and polarity registers are loaded at this time and the output is changed according to specified polarity bit. When a counter channel is disabled, the counter register does not count. The PWMCNTn register should be written to when the counter is disabled otherwise the period may get truncated.

2.3.6   PWM Period and Duty Registers

PWM Channel Period Registers

The count specifying the end of the period is contained in the channel period registers. When the PWMPERn register is written to while the PWM is enabled, until the existing period has terminated, the new value does not take effect.

Left-aligned Waveform (CAEn=0):Period= Channel_clock_period*PWMPERn

Centre-aligned Waveform (CAEn=1):Period= Channel_clock_period*2*PWMPERn

PWMPER0-PWMPER5

7	6	5	4	3	2	1	0

Fig 2.10

PWM Channel Duty Registers

When the PWMDTYn register is written while the PWM is enabled, it does not take effect until the existing period terminates or the channel is disabled or the PWMCNTn channel is written to.

There is no pulse generated if the PWMDTYn is greater than or equal to the period specified in the PWMPERn.

PWMDTY0-PWMDTY5

7	6	5	4	3	2	1	0

Fig 2.11

2.4 Determination of Pulse width modulation Counter Pre-scaler andScaler values.

PWM value below 20kHz can cause objectionable noise whereas if the frequency is too high some components may not be able to follow the rate of change.

1) Choose the PWM period for PWMPERn to be 255. This provides the best time resolution while choosing the duty cycle count to be set in PWMCTYn.

2) Divide the t_{period} by 255 , to obtain the period of the PWMCNTn clock.
$$T_{PWMCNT} = t_{period}/255$$

3) The total divisor needed is obtained by dividing the PWMCNTn period by the bus clock period.
$$\text{Total Divisor} = T_{PWMCNT} / \text{Bus clock period}$$

4) Recalculation of PWMCNTn followed by PWMPERn
$$T_{PWMCNT} = \text{Total Divisor} * \text{Bus clock period}$$
$$PWMPER = t_{period} / T_{PWMCNT}$$

5) PWMDTYn register countis calculated based on the PWMCNTn period.
$$PWMDTY = t_{duty}/T_{PWMCNT}$$

6) The Total divisor chosen must be rounded to the next highest even integer value.

2.5   PWM generation by circuit components

When a comparator is fed with a saw tooth carrier, it can turn a sinusoidal command to the pulse width modulated output. Larger command signal, results in wider pulse.
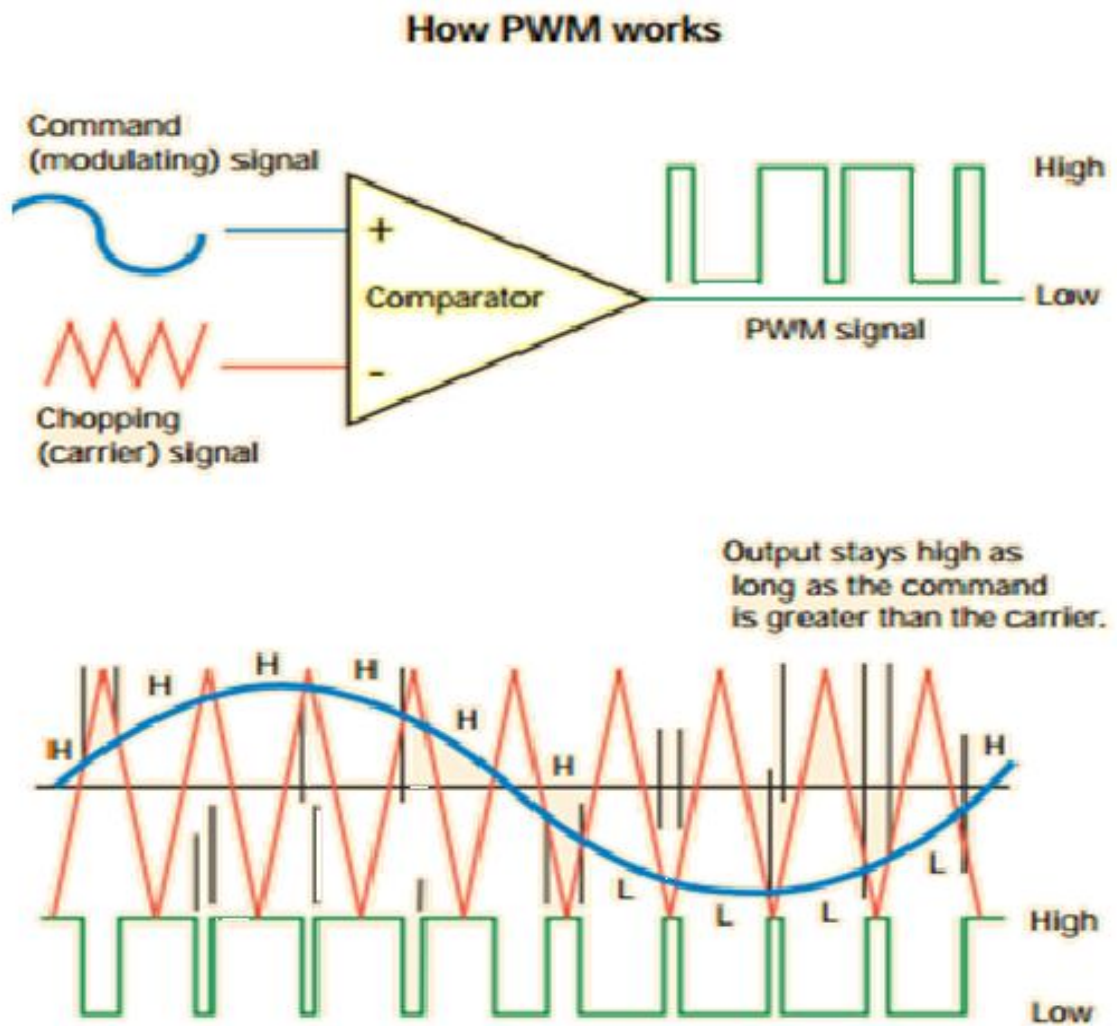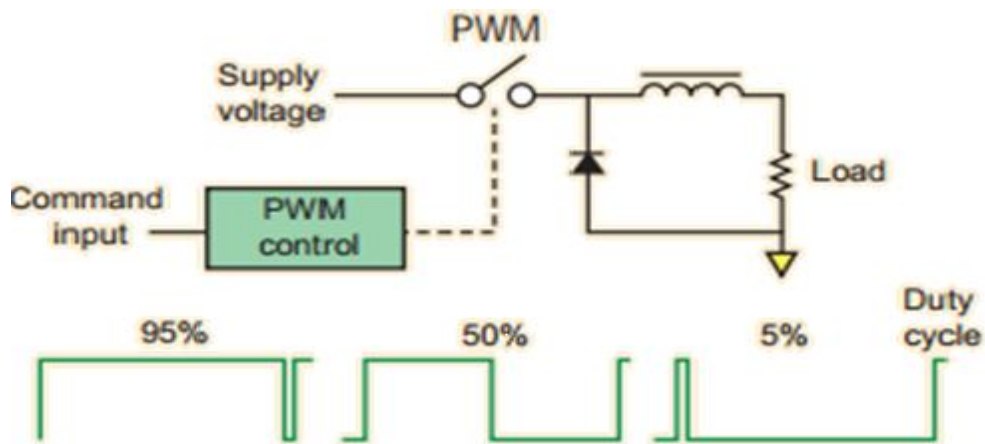
Fig 2.12

Fig 2.13

2.6 Control Algorithm

The PWM output which is obtained by comparing the actual parameter value and the corresponding set point. Controllers are differentiated based on method of regulation of parameters in accordance with the corresponding set point.

The value that results with the comparison of the actual value and set value is the error value that is used. By the addition of an integral component to the control algorithm this error is eliminated.

3

ADC   Interfacing
Through HCS12

INTRODUCTION

An analog to digital converter can be defined as a device that converts a continuous quantity to a discrete time digital representation.

Analog to Digital Conversion is the transformation of an analog signal (voltage) to a binary number and eventually to a digital number to be read on a monitor, chart or meter. The resolution of the A2D converter is determined by the number of bits(binary digits) that represent the digital number.Theoretically specified resolution is that an n-bit ADC has a resolution one part in 2^n.

3.1 HCS12 A/D Converter
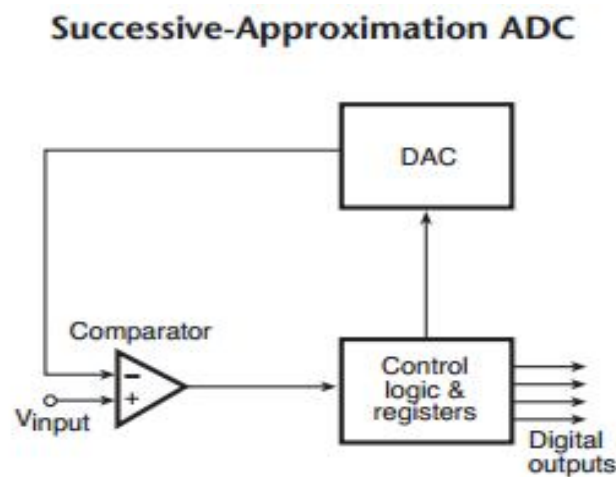
Successive-Approximation ADC

Fig 3.1

The HCS12 A/D converter, is a successive approximation one. Testing of each bit in the successive approximation register takes place; starting with the most significant bit moving towards the least significant bit. The output from the Digital to Analog converter is compared with the input as each bit is set. The bit remains set if the D/A output is lower than the input signal and the next bit is tried. Bits which make the D/A output higher than the analog input are reset.

The A/D converter is a 8-channel, multiplexed, 8-bit or 10-bit, successive approximation one with +-1LSB accuracy.

The conversion is started by either an external trigger signal or by writing into the control register .The port AD bits *AN0/PAD0-PAD7/AN7*are the input pins .The input multiplexer is controlled by A/D Control register *ATDCTL5*. When the conversion is started, the capacitor charges upto the input signal and is held constant for the duration of the A/D conversion. The conversion is optimized by use of V_{RH} and V_{RL} over the input signal range. The outputs from the A/D conversions are placed into 8   16-bit data registers *ATDDR0-ATDDR7*
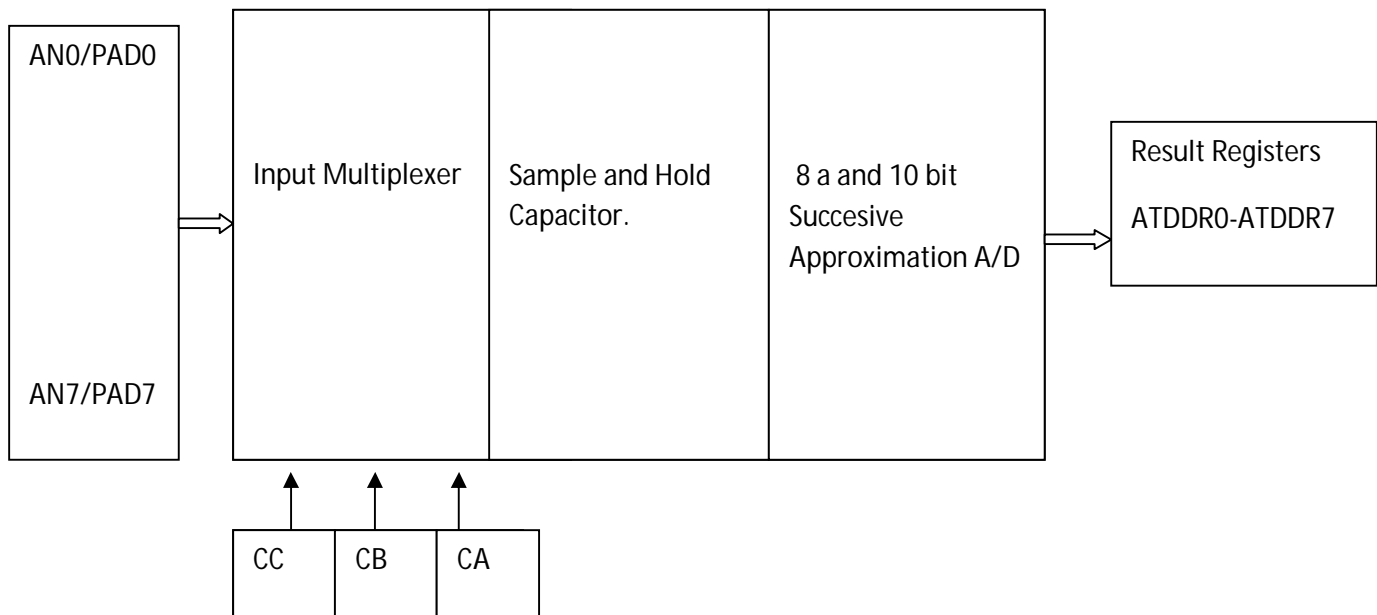
Fig 3.2

3.2   ATD Control Registers

3.2.1   ATDCTL2

A short delay of 20 µs is to be observed before using the A/D after it has been powered up.

ADPU	AFFC	AWAI	ETRIGLE	ETRIGP	ETRIGE	ASCIE	ASCIF

Fig 3.3

ADPU: On/Off control for the ATD is set by this bit.

AFFC: ATD Fast Flag Clear:Enables fast flag clear operation.Any access to the result register will clear the associated flag.

AWAI: ATD Power Down in Wait Mode. The ATD powers down in wait mode to reduce power consumption by setting this bit.

ETRIGLE: External Trigger/Level Control: This bit sets the external trigger signal to be a rising or falling edge.

ETRIGP: Polarity defined for the trigger signal

ETRIGE: Enables the external trigger mode.

ASCIE: ATD Sequence Complete Interrupt Enable

3.2.2 ATDCTL3

0	S8C	S4C	S2C	SIC	FIFO	FRZ1	FRZ0

Fig 3.4

S8:S1C: Conversion Sequence Length: Number of conversions per sequence is controlled by these bits. S4C is set to 1 to maintain software continuity with earlier members of the HCS12 family.

FIFO: Result Register First In First Out: The conversion sequences defines how the ATD conversions are placed into the result register (ATDDR0). If the FIFO mode is on, the conversion counter is not reset at the beginning or end of the conversion sequence and conversion results are placed in the consecutive result registers. The result register counter wraps up when it reaches the end of the result register file.

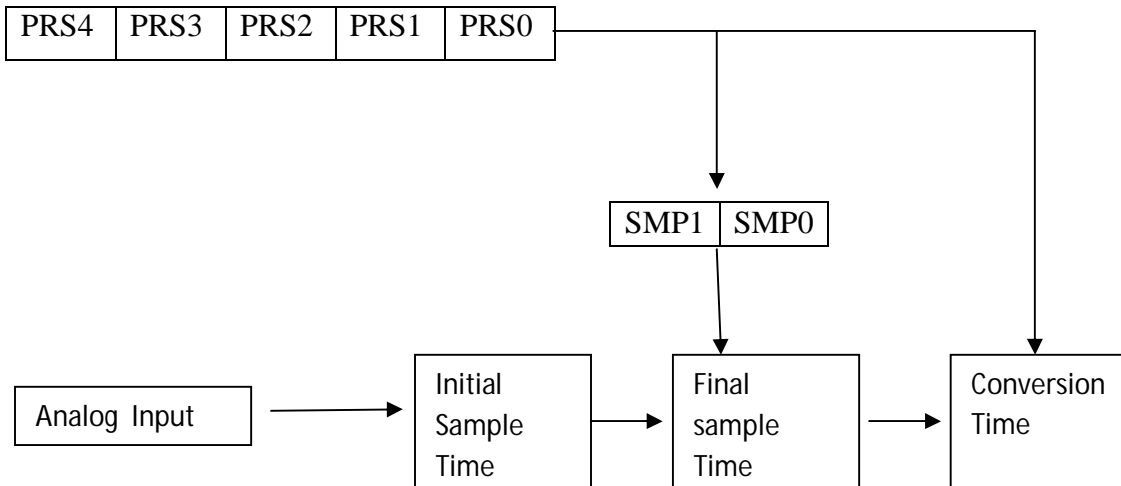### 3.2.3 ATDCTL4

ATD Clock (500 kHz to 2MHz)

Fig 3.5

The ATDCTL4 controls the feature of sampling time, prescaler bits PRS4-PRS0 are chosen to generate to appropriate A/D clock frequency.

In the initial sample stage, the input is connected through unity gain buffer amplifier to sample capacitor. The input pin is connected directly to sampling capacitor in the second part which is then charged to final input value. Finally 8 or 10 bit A/D clocks to complete the conversion.\

Nyquist Frequency: The maximum frequency which can be sampled without the effect of aliasing and which is the resultant of two samples per period of input signal.

Aliasing: When the input signal changes ata much fasterrate than the sample rate, then spurious signals or aliases are produced. The frequency of this signal is the difference between the signal frequency and the sampling rate.

SMP2	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0

Fig 3.6

SRES8: for resolution select: 8 bit or 10 bit.

SMP1:SMP0: Sample Time select: the 2 bits are needed to select the second phase of the sample time in units of conversion cycles. The external analog signal is directly attached to the storage capacitor for final charging by the second phase.

3.2.4 ATDCTL5

The ATDCTL5 register enables the ATD conversion. After each conversion, the A/D waits for the ATDCTL5 register to be written to again.

DJM	DSGN	SCAN	MULT	O	CC	CB	CA

Fig 3.7

DJM: the bit defines whether it is right or left justified data.

DSGN:This bit selects the signed or unsigned representation in data registers.

SCAN: Continuous conversion Sequence Mode.This bit checks whether conversion sequences are performed continuously or only once.

MULT: This bit signifies if the sampling is from the specified analog input channel or subsequent channels also.

CC,CB,CA: These bits are helpful in selecting the input channels .This selection code determines the first channel to be selected and subsequent channels are determined by incrementing the code.

The ADC measures the output voltages and output current by the Dc-Dc converter which is feedback to the controller. The ADC measures voltage at the battery terminals to determine the termination of charge.
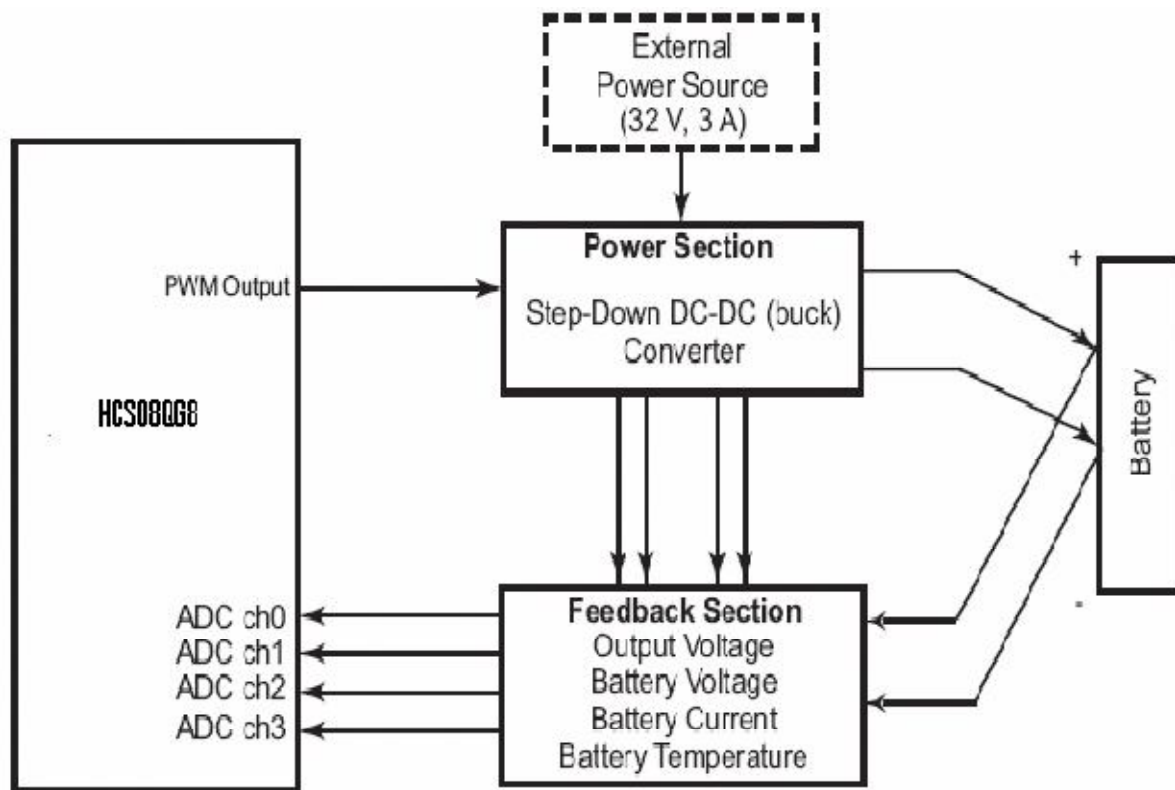
4

Circuit Simulation & Results

Fig 4.1

The buck converter is used for modulation of higher voltage from an external source with a PWM method for the generation of lower voltage. Control algorithm controls the pulse width based on values which have been obtained through the feedback section which consists of four differential amplifiers.
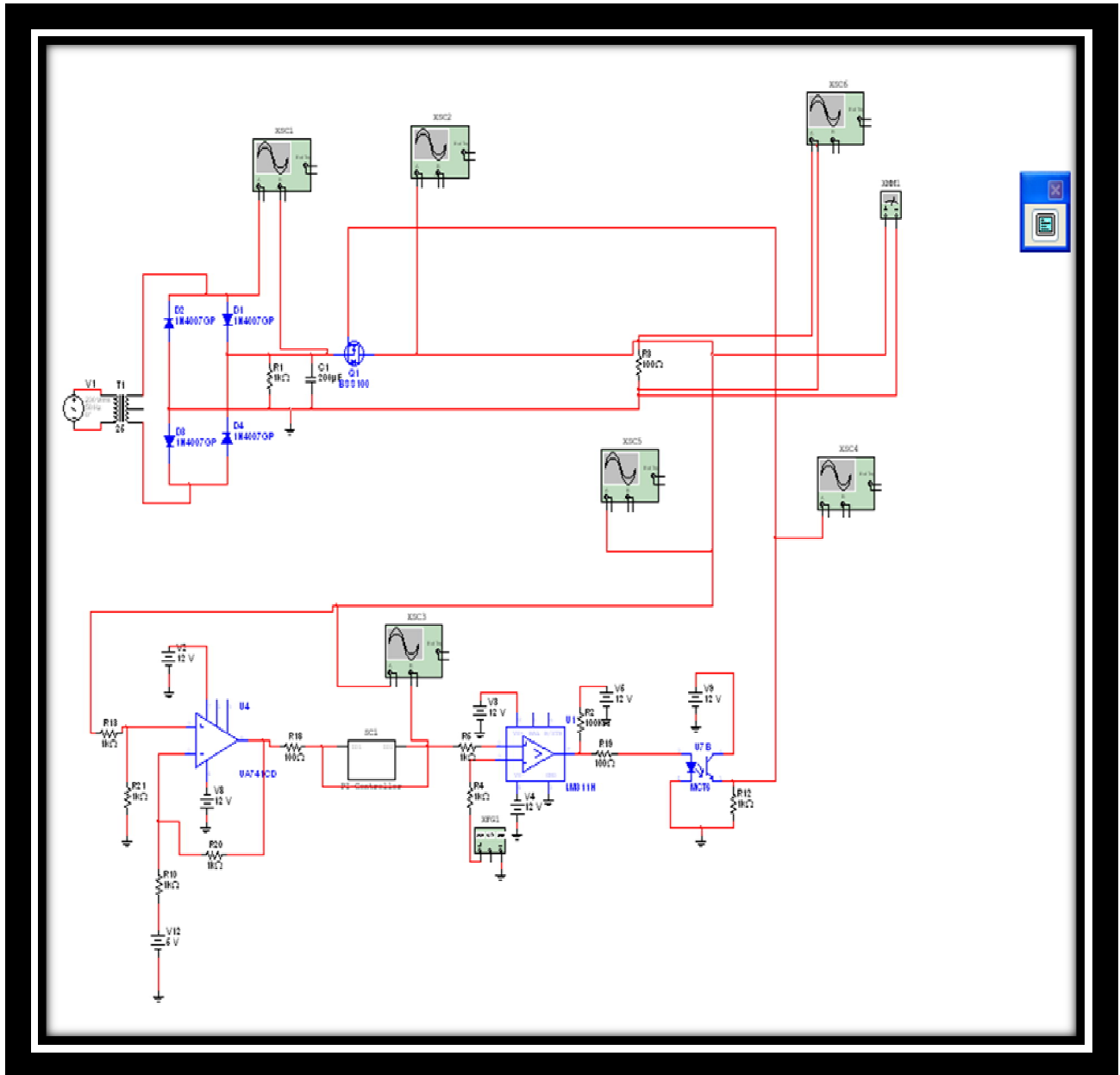
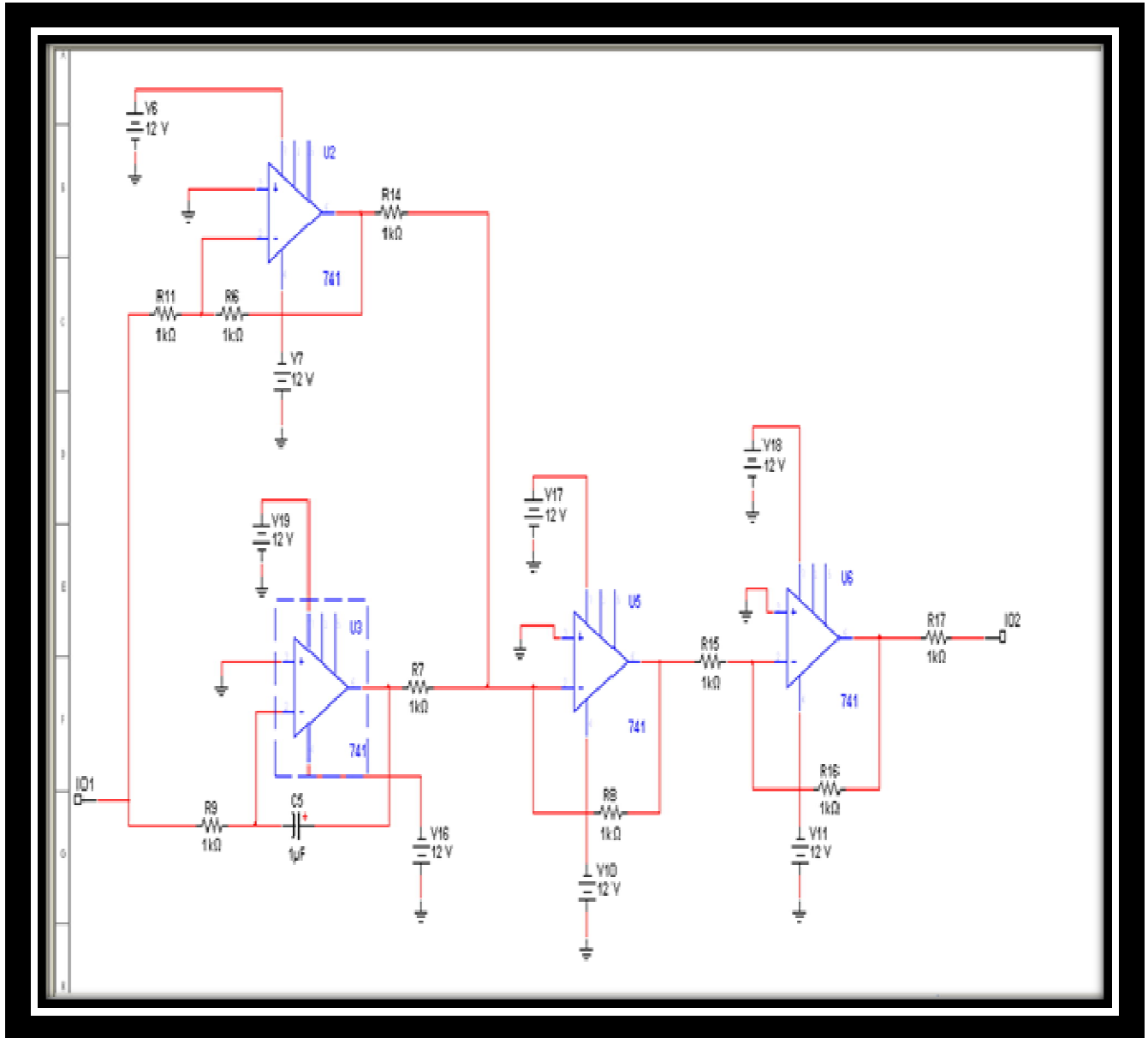# Model of the Working Circuit

Fig 4.2

PID Controller Circuit

Fig 4.3

Rectified output
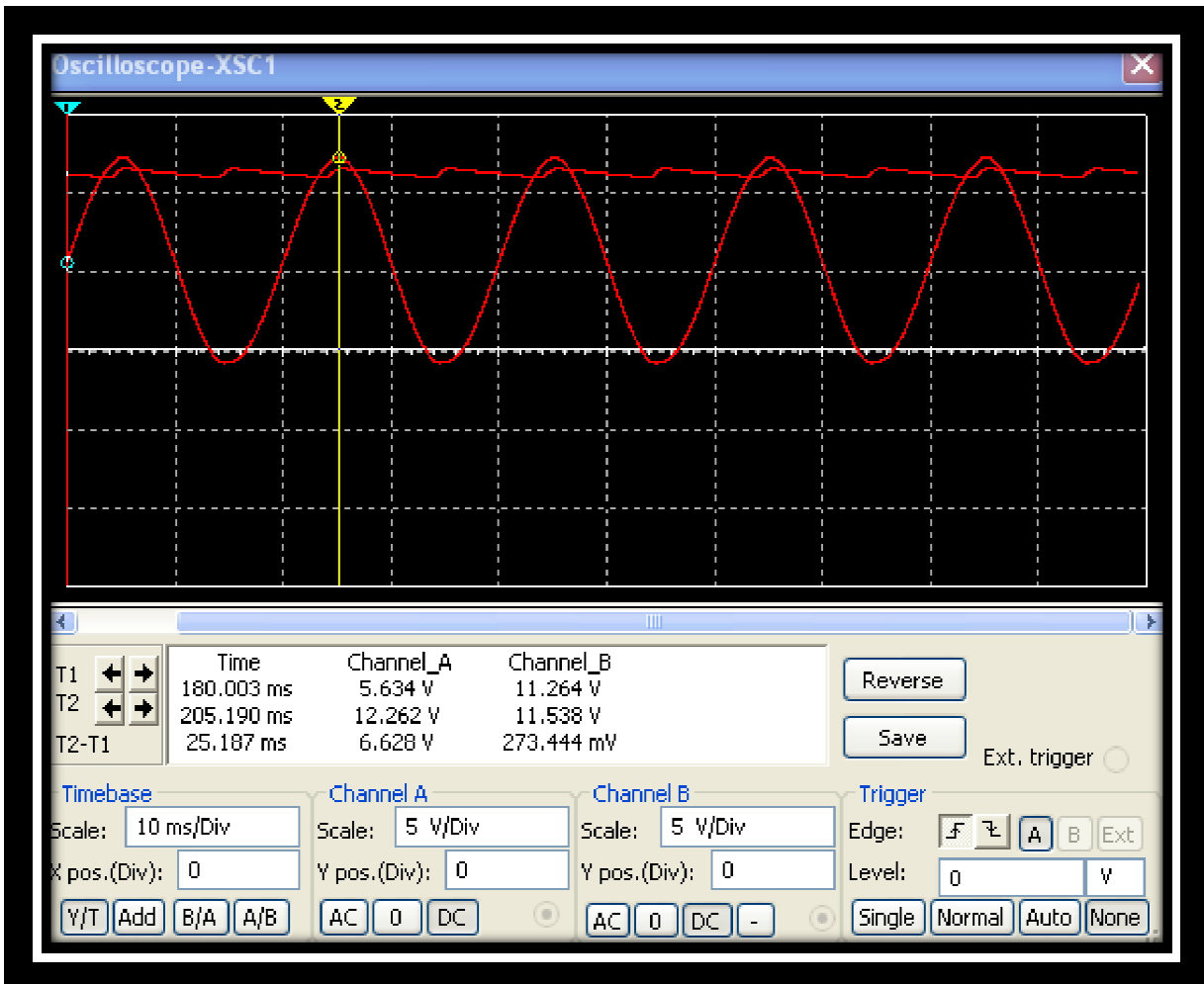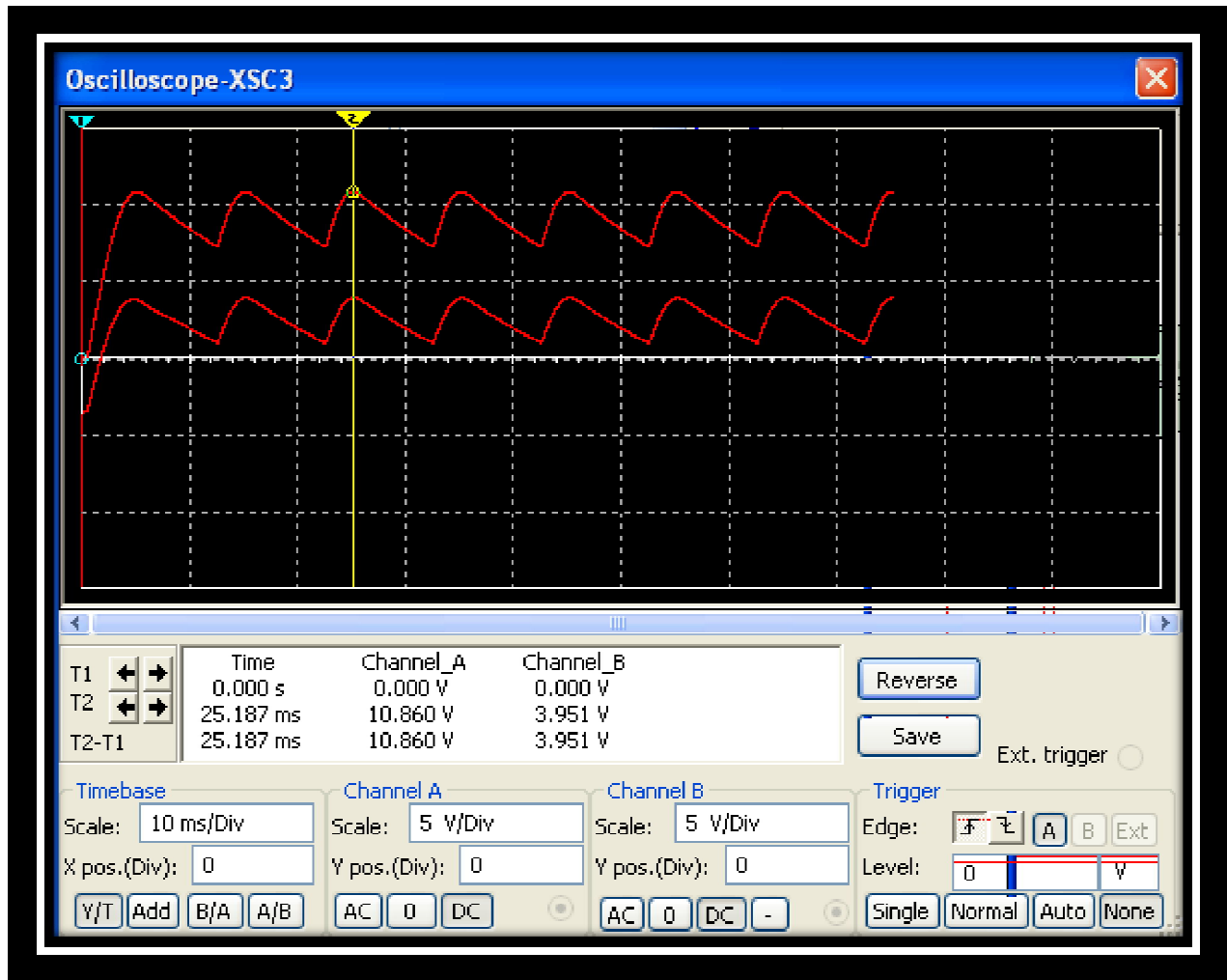

Fig 4.4

Differential Amplifier Output
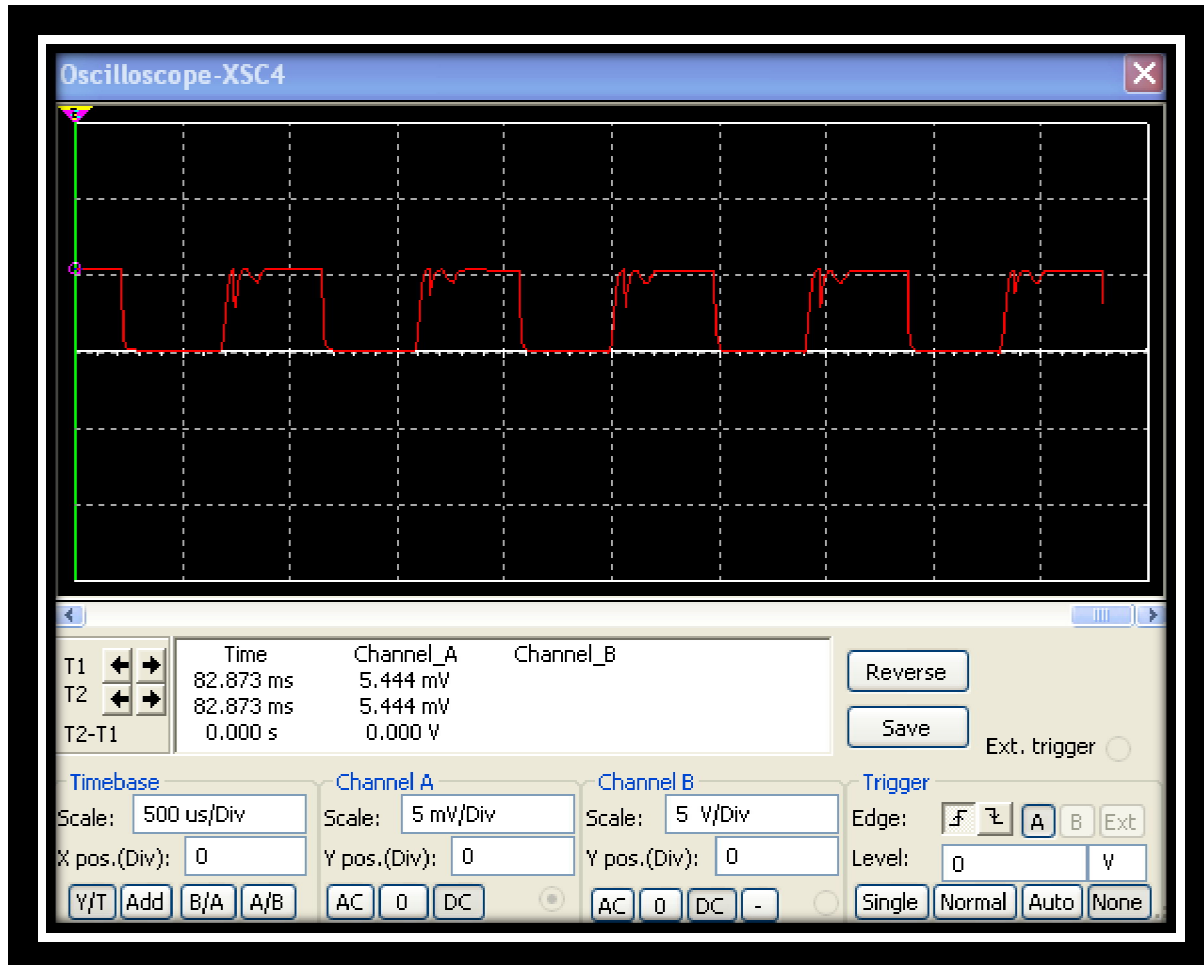

Fig 4.5

PWM   signal generation
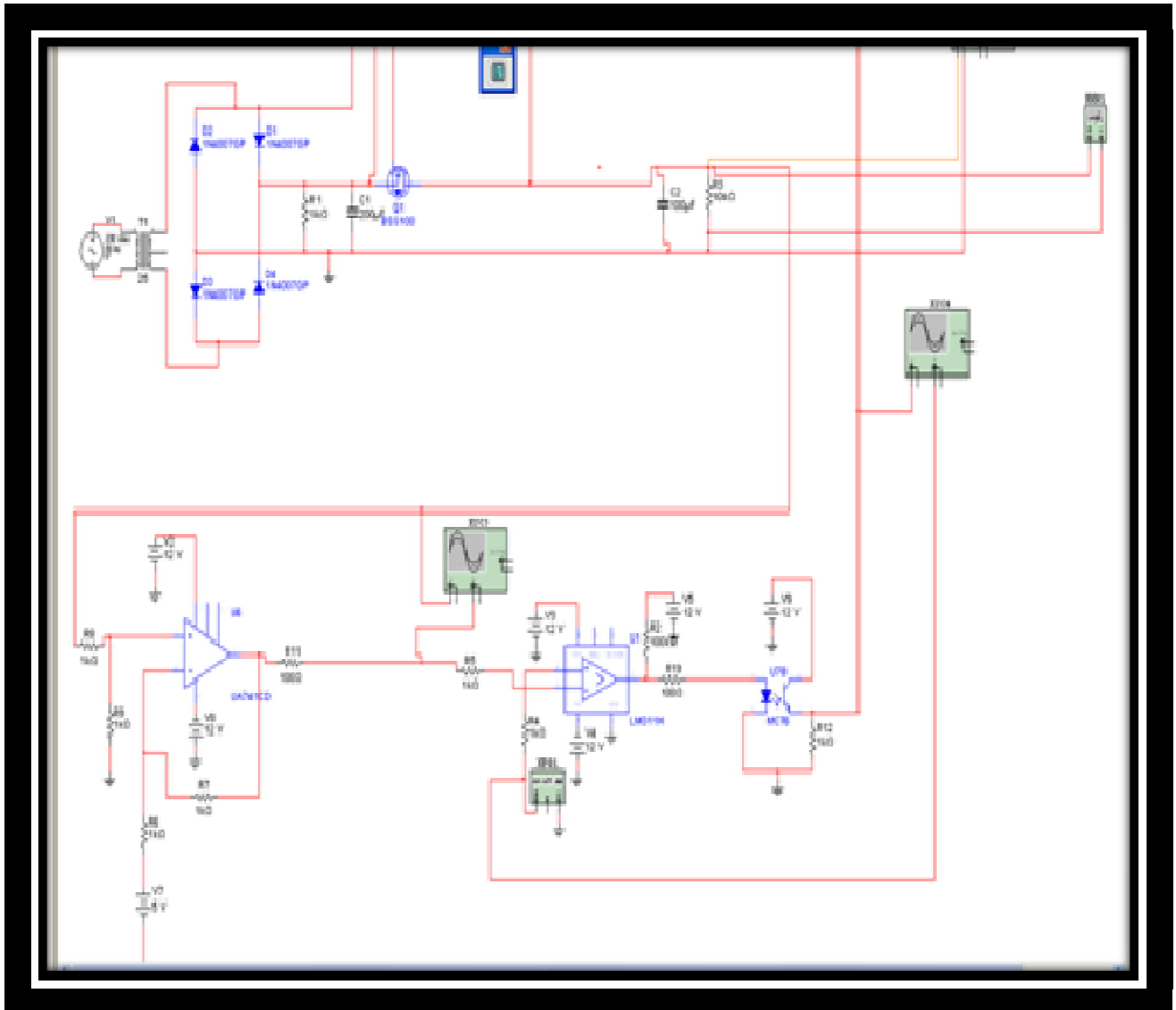

Fig 4.6

PWM generation without the PID controller

Fig 4.7
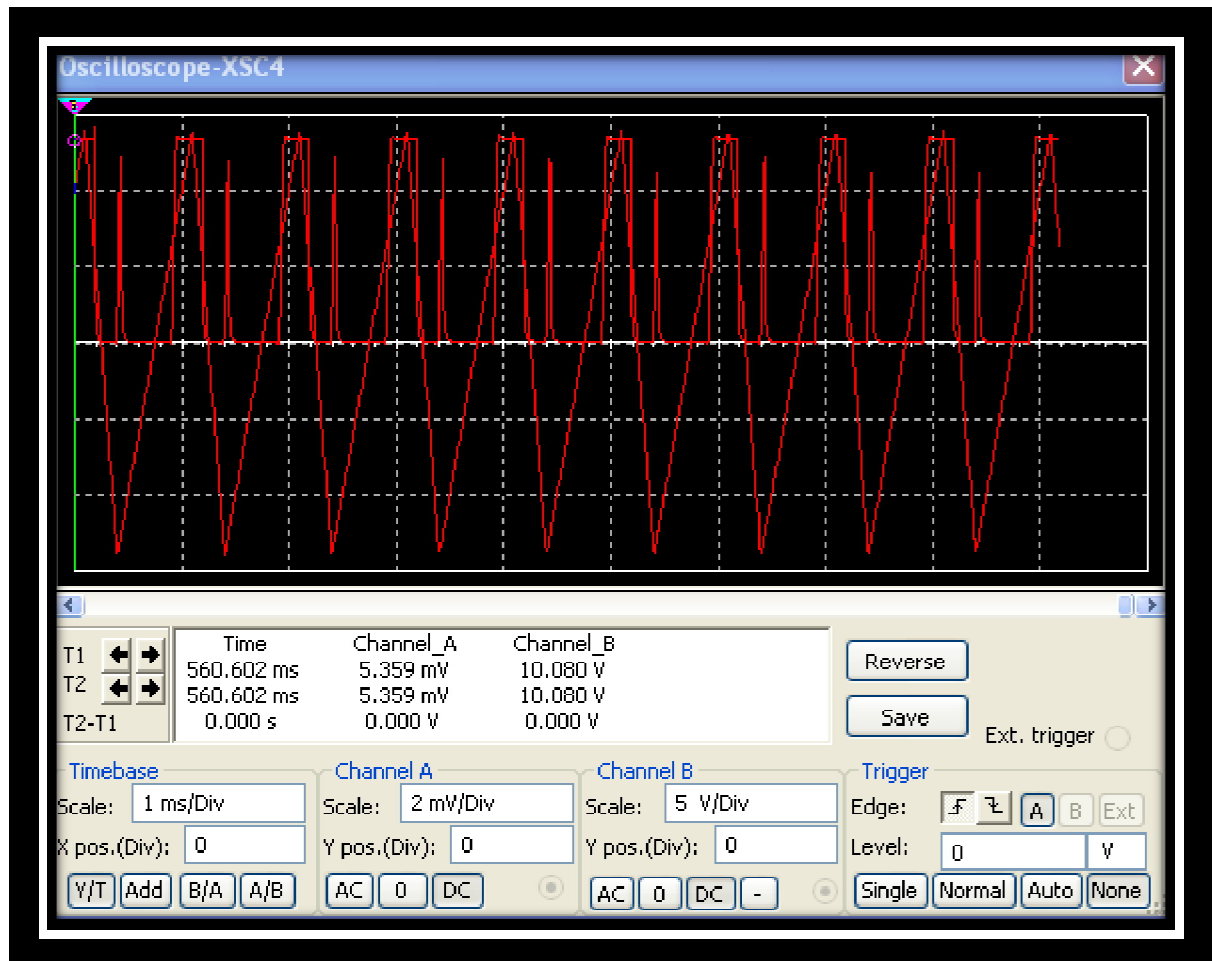
Fig 4.8

4.2 HCS12 Code Output

4.2.1 PWM Wave Generation

The code outputs a 20 kHz waveform with a high duty time that varies with 10μs to 50μs.The output is port T, bit 1.
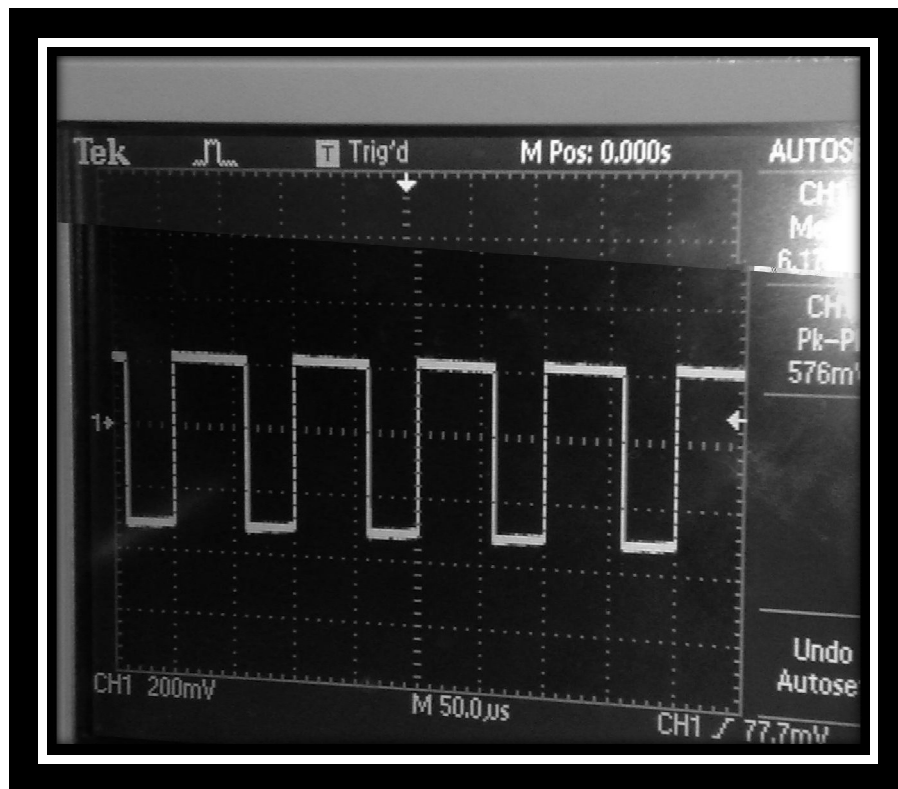

Fig 4.9

4.2.2   ADC

The code converts the analog input on channel one four times and calculates the average.

Voltage Detected(analog value in volts)	Values observed after A2D conversion
4.84	249
4.46	E4
3.66	BB
3.13	A0
2.78	80
2.13	6B
1.96	63
1.71	57
1.33	44
0.99	32
0.5	0Xa1
0.02	0

Table 4.1

Conclusion

A novel circuit based on HCS12 is designed for battery charging application. This circuit includes PWM circuit, ADC interface and circuit is designed so that it is compatible to battery characteristics.

Individual circuit components are investigated through simulations using MULTISIM package.

Through these simulations and outputs we get a thorough understanding of the battery characteristics and the factors that influence the charging process.

Prior to design using microcontroller we conducted a circuit level simulation that includes PWM circuit, PID controller etc. The results through either approach complement each other thus validating our concept.

A novel microcontroller technology is implemented that facilitates controlled charging of the battery to increase battery efficiency, safety at a reduced cost.

References

1) HCS08 Microcontroller based novel PWM controller for battery charger application. S.K Pattnaik, SudeendraKumar, A.K Swain, K.K Mohapatra, IEEE March 2008
2) HoltekMicrocontroller Application – Battery Charger D/N: HA0052E Application Note .
3) Intelligent and Universal Fast Charger for Ni-Cd and Ni-MH Batteries in Portable Applications-Juan Díaz, Juan A. Martín-Ramos, Alberto *M. Pernía, Member,* IEEE Transactions on Industrial Electronics, Vol. 51, No. 4, August 2004
4) T. H. Liu, D. F. Chen, and C. C. Fang, "Design and implementation of a batterycharger with state-of-charge estimator". *Int. J. Electron.,* pp.211-226, vol. 87,no. 2, Feb., 2000.
5) M. González, M. A. Perez, J. Díaz, and F. J. Ferrero, "Ni-Cd and Ni-MH batteryoptimized fast-charge method for portable tele-communication applications"*Proc. INTELEC'96,* pp.522-529, 1996.
6) An Innovative Charger for Safe charging of NiCd batteries. Tanvir S Mundra& Ajay Kumar IEEE Transaction on Consumer Electronics August 2007
7) M. González, M. A. Perez, J. Díaz, J. C. Campo, and S. Horta "New intelligent Ni-Cd and Ni-MH battery fast-charger" *Proc. IEEE ISIE'97*, pp. 501-506,1997.
8) C. B. Falcon, "Methods of controlling the application and termination of charge to a rechargeable battery", *US Patent*: *5600226*, Feb 4, 1997.