VLSI Implementation of a Demand mode Dual Chamber Rate Responsive Cardiac Pacemaker

A Thesis submitted in partial fulfilment of the requirements for the degree of

Bachelor of Technology
in
Electronics and Instrumentation Engineering

Submitted by:

Abhipsa Panda
108EI007

Under the supervision of
Prof. Kamalakanta Mahapatra

Department of Electronics and Communication Engineering,

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C E R T I F I C A T E

This is to certify that the Thesis entitled, '**VLSI Implementation of a Demand mode Dual Chamber Rate Responsive Cardiac Pacemaker**' submitted by **Abhipsa Panda** in partial fulfilment of the requirements for the award of **Bachelor of Technology Degree** in **Electronics and Instrumentation Engineering** at the **National Institute of Technology Rourkela** is an authentic work carried out by her under my supervision. To the best of my knowledge and belief the matter embodied in the Thesis has not been submitted by her to any other University/Institute for the award of any Degree/Diploma.

Prof. Kamalakanta Mahapatra
Department of Electronics and Communication Engineering,
National Institute of Technology Rourkela.

A C K N O W L E D G E M E N T

This is a Research Project and I would never have been able to complete it successfully without some people. I would always be grateful to the following for their help and guidance throughout the project.

Firstly, my heartfelt thanks to Prof. Kamalakanta Mahapatra for his incessant support and motivation throughout the project. His provision for an independent environment throughout the two semesters was a boost to creativity. His experience and ideas proved to be priceless breakthroughs, forming a significant part of the project.

I would like to thank Prof S. K. Meher, Head of the Department Electronics and Communication Engineering, for approving my project whole-heartedly.

Mr Ayaskanta Swain, who has been of immense help during the initial phases of the project, deserves a special mention for his never-ending efforts to answer queries and find a light in the intermittent dark ends.

Also thanks to Mr Jagannath Mohanty, Mr Vijay Sharma and Mr Bhubaneshwar Das for extending a helping hand with the technical difficulties and provision of adequate requirements for the project. Thanks Mr Satyaki Mascharak and Mr Arghyapriya Choudhury for helping me with the hardware implementation of the project.

Finally, a word of thanks to God, all my friends, everyone associated with this project directly or indirectly to make it a success.

Abhipsa Panda

A B S T R A C T

This project is aimed to design a dual chamber rate responsive cardiac pacemaker, implement it in VLSI and improvise on it for real time safety critical environments.

A state machine approach has been followed to achieve the desired purpose. The heart of the pacemaker system rests in the pulse generator which forms the major portion of the project. It has been developed using VHDL and implemented in hardware using FPGA. In the FSM, first an input event is detected. Once this input is detected a timer is set for approximately 0.8 sec, which will be the time between heartbeats, thus giving us 72 heartbeats per minute. Once the timer expires we check to see if a new event is detected. If one is detected we repeat the process of detection and waiting. If one has not been received we need to stimulate the heart and then repeat the process of detection and waiting.

The code has been optimized and modified for different pacemaker modes. Adequate effort has been put in for designing a sensing circuit and other peripherals like memory, data compression techniques and remote monitoring equipment, culminating in suggestions for improvement in respective areas. It closes with pacemaker testing for real life applications and scope for further work in the field.

C O N T E N T S

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C H A P T E R 1

I N T R O D U C T I O N

1. INTRODUCTION

1.1 Motivation

I have always believed in the philosophy of the greatest contribution we Engineers can do to the betterment of the human race is by giving it a healthier and safer life, rather than a more comfortable and luxurious one. Most of engineering sciences focus on the latter perspective. Whilst amidst all the apparent so-called technological gifts, from this community to the rest of the humanity have made life better and easier to lead, I emphasize on making life better with improved health of the general masses, and the best an engineer can give in this respect is through the fusion of engineering and medical sciences. Thanks to forums like IEEE EMB (IEEE Engineering in Medicine and Biology) this field has seen peaks of success unimaginable a few decades back. This has been my strongest motivation to choose the aforesaid project.

An ever increasing rate of cardiovascular diseases causing untimely deaths has made pacemaker technology the need of the hour. With the advent of the sixth decade of implantable cardiac pacemakers, two trends have become increasingly apparent. These are: the demand for automaticity in pacers and the greater reliance upon programmers in the care of the patient. This is where we Engineers come into the picture.

The recent developments in the VLSI forefront have indeed made high speed, low area, and low power devices carry the day. Pacemaker is a life critical device with hard deadlines, severely restricted power supply and space availability. So trend to shift to the VLSI domain is dominant.

This is an effort from the Engineering community in contributing to global healthcare for a better and beautiful tomorrow.

1.2 Problem Statement

The primary objective of this project is to design a dual chamber rate responsive cardiac pacemaker, implement it in VLSI and improvise on it for real time safety critical environments.

1.3 Organization of the Thesis

The Thesis has been divided into eight chapters including this one. The first chapter serves as an introduction and gives an overview of the project. The second Chapter explains the basic concepts with regards to pacemaker and the functioning of the heart. The third chapter shows the design of a pulse generator in VHDL and its gradual improvement to the pacing machine of a rate responsive pacemaker. The different pacing modes and types of pacemakers were also explained in this chapter. Chapter four deals with the sensing circuit and its schematic design in Multisim. Chapter five concerns with the peripherals associated with the pacemaker with respect to memory and telemetry considerations and provides suggestions for improvement. Chapter six shows the closed loop testing of the pacemaker machine using VHM. Chapter seven explains the various methodologies for hardware implementation. Chapter eight gives the concluding remarks and scope for further research in the field.

C H A P T E R 2

B A C K G R O U N D

I N F O R M A T I O N

2. Background Information

2.1 Basics of Pacemaker

The pacemaker is a device implanted inside human body to correct improper functioning of the heart. It consists of three components: the pulse generator, the pacing leads, and the sensing circuit.

The pulse generator contains the pacemaker's power source and digital circuitry. A lithium/silver vanadium oxide battery having a 10yr shelf life is the main power source. The digital circuitry is bifurcated into a microcontroller that handles high-level control and manipulation, and a sequencer for handling routine pacing function. In this project both the components are encompassed in the VHDL code written and dumped into the FPGA board which controls the execution of pacing considering the inputs from the other components of the device.

The pulse generator receives its inputs as an electrical pulse through a sensing circuit from the heart, via electrodes or electrodes. The pulse generator senses the heart's own electrical activity and responds according to the way it has been pre-programmed. Electrical stimulus from the pulse generator move through the pacing leads into the electrode tip. The leads for a pacemaker are used to stimulate the atrium or the ventricle on the right side of the heart. As such the leads perform the dual function of transmitting signals to and fro the pulse generator.

The sensing circuit performs the needed signal conditioning on the signals from the heart and processes them to convert into a form more acceptable to the pulse generator. It acts as an interface between the leads and the generator.

2.2 Brief functioning of the heart

The main function of the Heart is to pump blood to the entire body. It gets the deoxygenated blood from the entire body via veins into its left atria, pumps it into its ventricles, which is then sent to the lungs for oxygenation. The oxygenated blood returns to the right side of the heart and the same process is followed to pump the blood to the entire body.

It has a Sino-atrial node (SA node); called natural pacemaker. It generates electrical impulses, which are responsible for the contraction and expansion of heart muscles. These electrical impulses synchronize the heart muscles and hence blood pumping. Although, all the heart cells can generate electrical impulses or action potentials, SA node is the major node of generation of the pulses.

After contraction of the atria, the impulse makes its way to the Atrio-venticular (AV) node. The impulse slows down at the node, which gives time for contraction of the atria. Just below the AV node, the impulse runs quickly through the bundle of His, the right and left branches of the bundle and the Purkinje fibres and lead to ventricular contraction. In case of damage of the intrinsic conduction system, an artificial device, pacemaker, is implanted within the heart. This device monitors the heart rate stimulating the heart when it beats too slow or skips beats. Main goal of cardiac pacing is to artificial stimulation of a diseased heart to operate at the normal rate.

2.2.1 Cardiac Cycle

The pressure changes in the major blood vessels and the four chambers cause the valves to open and close and directly affect the flow of blood through the heart. The following phases of atrial, ventricular, and aortic pressure take place over one cycle.

2.2.2 Atrial Systole

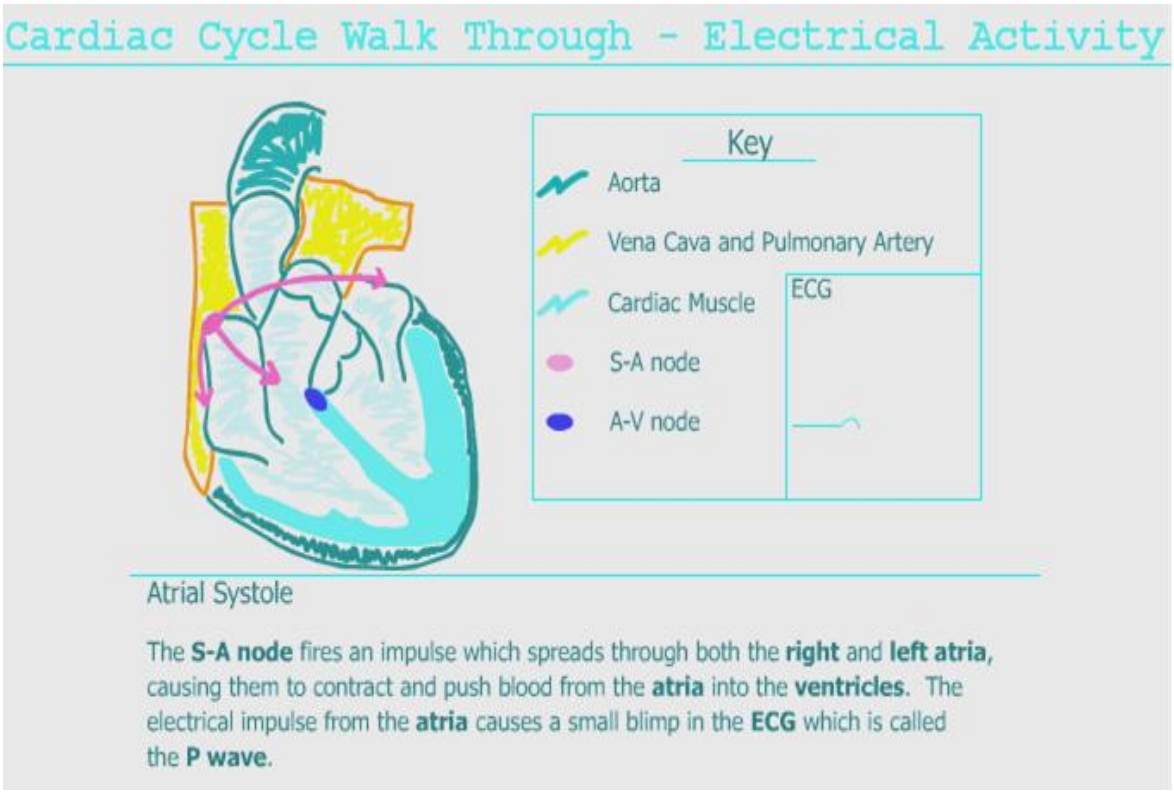

FIG. 2.1 Atrial Systole

2.2.3 Ventricular Systole

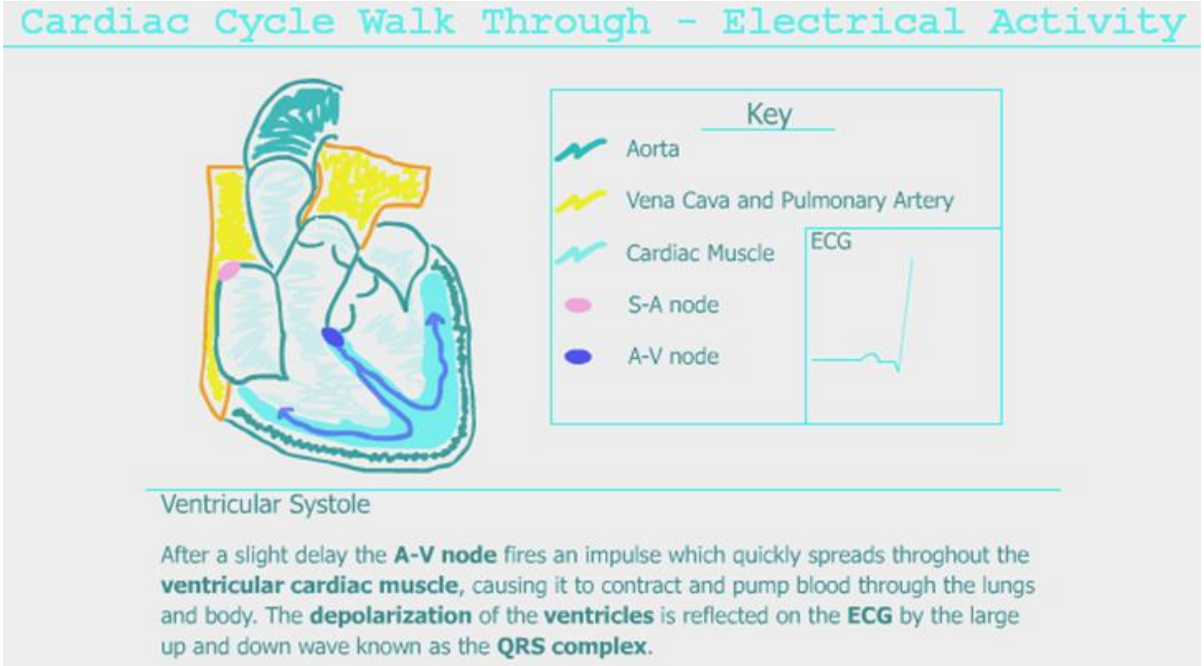

FIG. 2.2 Ventricular Systole

2.2.4 Late Diastole

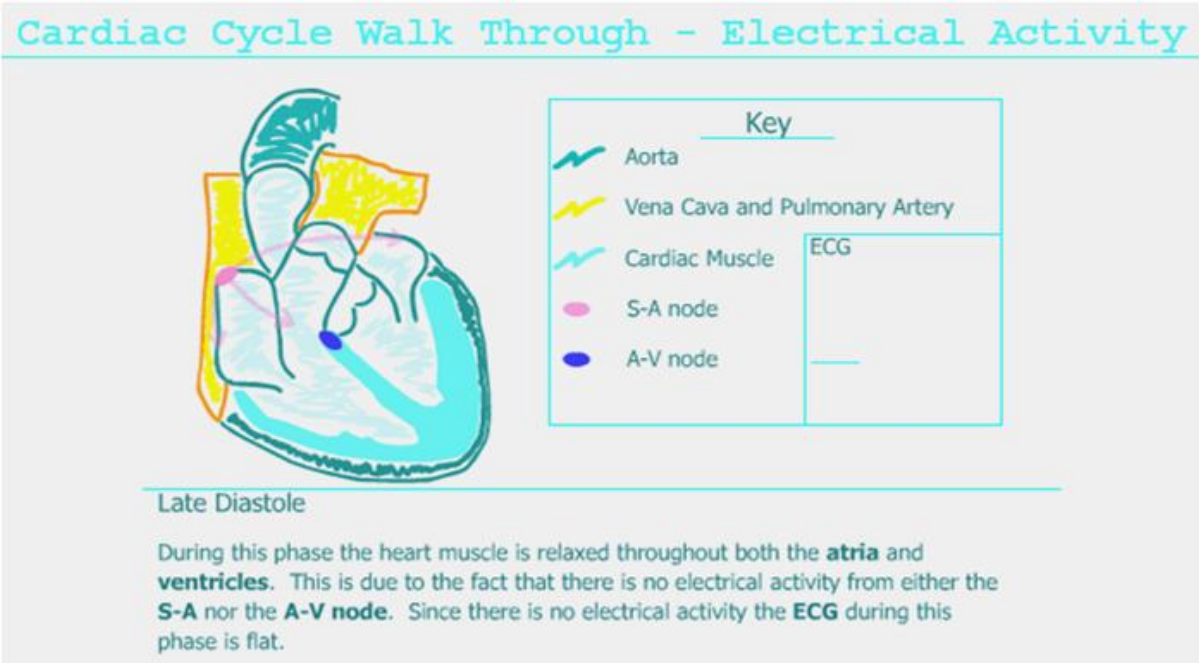

FIG. 2.3 Late Diastole

2.2.5 Early Diastole

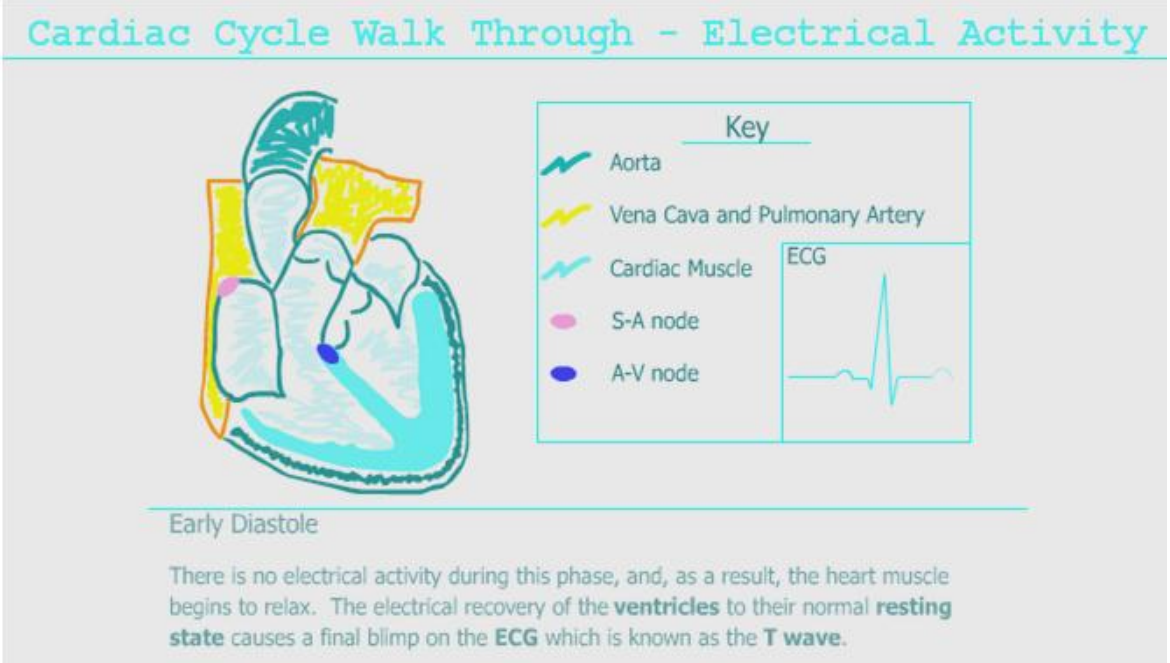

FIG. 2.4 Early Diastole

The above illustrations suitably explain the functioning of the heart that was described in the earlier portions of the chapter. The different phases of the cardiac cycle culminate in finally enabling the blood to be pumped throughout the body.

Each part of the cycle has its special significance: some like the late diastole occurs non visible by most electrocardiograms. Yet it is registered under certain special conditions giving a hint about the improper working of the heart. The discussion of implication of each of the phases is beyond the scope of our discussion. A brief idea about the cycles would suffice our purpose.

C H A P T E R 3

P U L S E G E N E R A T O R - T H E H E A R T O F T H E P A C E M A K E R

3. Pulse Generator: the heart of the Pacemaker

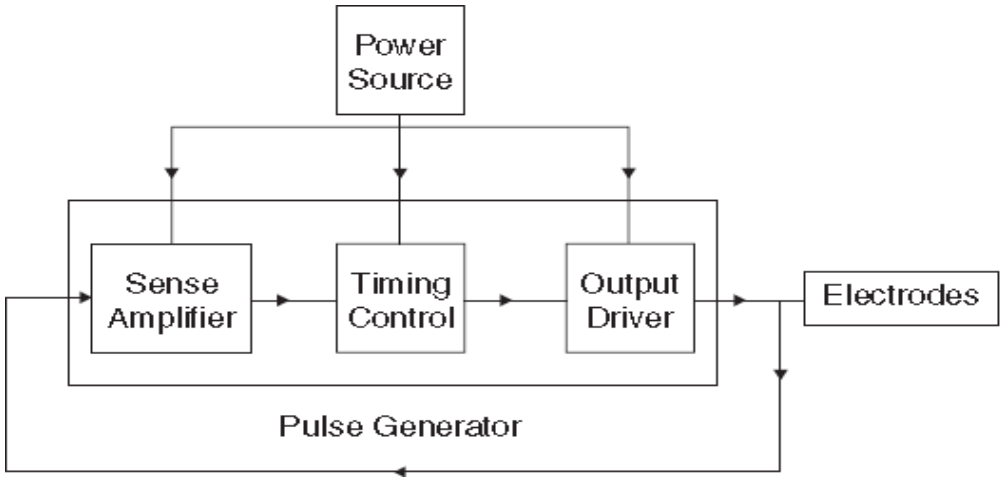

Fig. 3.1 Block Diagram of a Pacemaker

As mentioned beforehand, the most important part of the pacemaker is the pulse generator (denoted as timing control in the diagram), and hence, the major portion of the project concentrates on this topic. This chapter presents the different kinds of pulse generators available and that has been designed in the due course of this project. Various constraints have been considered and a cumulative approach has been followed in designing the end result.

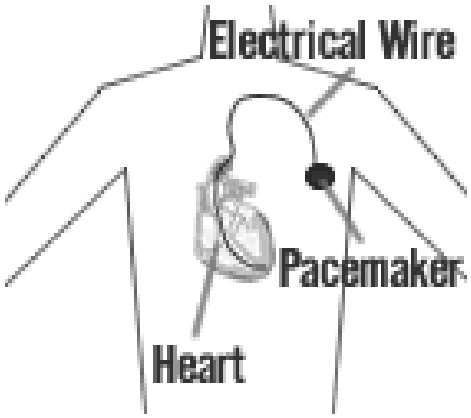

Fig. 3.2 The physical placement of an Implanted Cardiac Pacemaker

3.1 Approach

In this project a finite state machine is used to implement a simple demand pacemaker. A demand pacemaker is one in which there is no competition between the intrinsic pacing of the heart and the artificial pacing of the device. In other words, the pacer paces only in the absence of an R wave and so there is no competition between the two pacemakers. Had this not been the case, both of them would have had a competitive approach culminating in over-pacing of the heart at times.

Depending on the number of chambers involved the number of states of the machine changes. A Mealy model of the machine has been used for the purpose. Depending on the present state and the current input (sensed intrinsic pace) the output and next state changes at every state. The basic process of pacing is described below.

First an event is detected, in this case an R-wave. Once the R-wave is detected a timer is set for approximately .83 sec, which will be the time between heartbeats, thus giving us 72 beats per minute. Once the timer expires it is checked to see if a new R-wave is detected. If yes, the process of detection and waiting is repeated. If no, the heart is stimulated then the process of detection and waiting is repeated.

It was first done for a single chamber model (assuming pacing is needed just by the ventricles, atria functioning properly) and extend it to dual chamber (where both atria and ventricles are paced) Later the Rate Responsive pacemaker is designed considering a more practical design for the device. Finally the pacemaker is extended to different modes of working and results are observed.

3.2 Single Chamber Pacemaker

A Single Chamber Pacemaker is one in which only one of the two chambers of the heart-atrium and ventricle is paced. Since there are, in total four chambers, we consider each side of the heart separately. As such, there are two chambers to be considered. Now, if in a pacemaker, one of the two is paced, it is called as a single chamber pacemaker. Usually it is the ventricles that are paced because they have stronger muscles and hence, a more powerful contraction owing to the fact that they have to pump the blood to a longer distance as compared to the atria.

Depending on the mode of pacemaker operation the chambers sensed and chambers paced can be configured. In single chamber pacemaker typically there is one chamber sensed. But in specific cases there can be multiple i.e. dual chamber sensing and single chamber pacing too. Additionally they can have Rate Responsive behaviour which is going to be discussed in the subsequent sections.

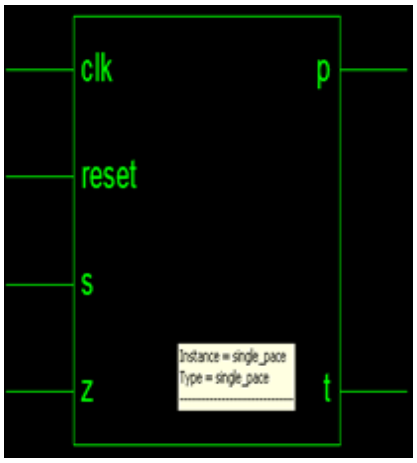

FIG. 3.3 RTL schematic of Single Chamber Pacemaker

3.2.1 State Machine

The state machine designed for this pacemaker consists of three states: Reset Timer, Wait and Pace. The machine gets the input ‘s’ from the sensor if a pace is sensed or not. Depending on ‘s’, it stays in the ‘wait’ state for 0.8 seconds (if intrinsic pacing is present) or goes to the ‘pace’ state to pace the heart artificially(if intrinsic pacing is absent). Depending on the input received from the timer i.e. if the timer has completed waiting 0.8 seconds (in case of wait state) the current state changes to ‘Reset Timer’ and the timer is reset. After every pacing operation the machine invariably goes to the ‘Reset Timer’ state to continue the process repetitively.

When the Pacemaker is being implanted in the body, the Reset timer state is triggered, and the rest of the operation follows. The following is the FSM diagram and component obtained after simulation and FPGA implementation of the VHDL code for implementation of a single chamber pacemaker.

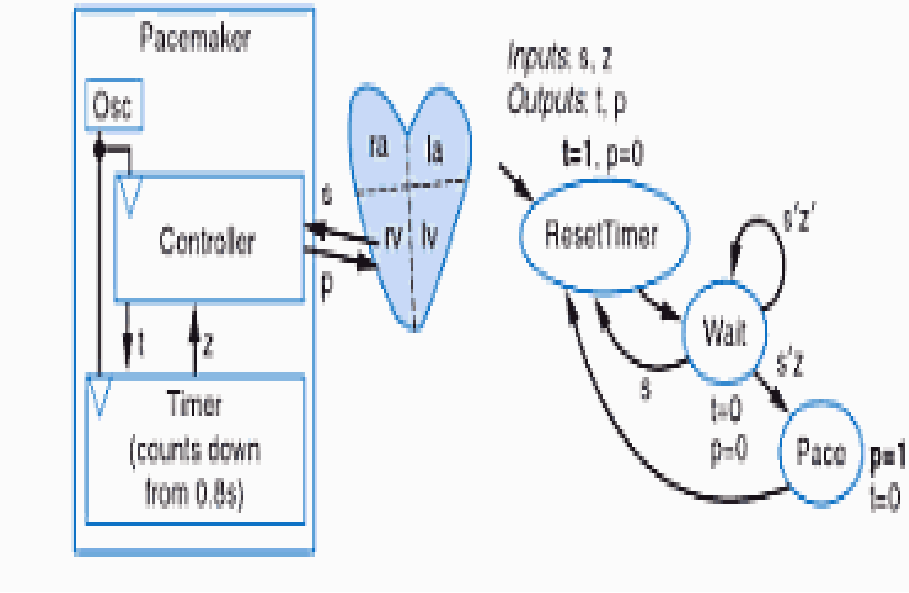

FIG.3.4 State Diagram of Single chamber pacemaker

3.2.2 State Table:

Inputs:

s: sensing parameter: 1 if contraction is sensed.

z: timer output: 1 if timer reaches 0.

Outputs:

t: output to timer: 1 if timer is to be reset.

p: output to heart : 1 if pacing needs to be done.

State	Functionality	Inputs	Inputs	Outputs	Outputs
		s	z	p	t
A	Wait	0	0	0	0
B	Pace	0	1	1	0
C	Reset	1	0	0	1
	Timer	1	1	0	1

Table 3.1 State Table of Single Chamber Pacemaker

3.3 Dual Chamber Pacemaker:

A dual-chamber pacemaker typically calls for two pacing leads: one placed in the right auricle and the other in the right ventricle. A dual-chamber pacemaker monitors (i.e. senses) electrical activity in the atrium and the ventricle to see the need of pacing. If need be, the pacing pulses of the atrium and ventricle are timed so that they mimic the heart's natural way of pumping. The atrial-stimulating impulse is generated first, and, after a predetermined time interval (200 milliseconds), the ventricular-stimulating impulse is generated.

The same logic can be applied to the left side of the heart in case of its improper functioning. Sometimes the dual chamber pacemaker can also be programmed to behave as a single chamber pacemaker depending on the excitation inputs and corresponding outputs.

Following figure gives a black box representation of the dual chamber pacemaker designed in the project.

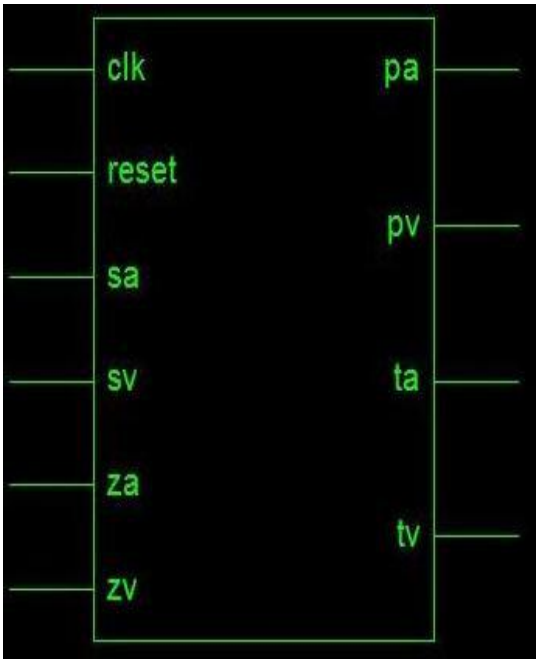

FIG 3.5 RTL schematic of Dual chamber pacemaker

3.3.1 State Machine

This is an extension of the single chamber to dual chamber pacemaker. The basic working principle is the same. Just that after the pacing of atrium, the state changes to the 'Reset Timer' state of the ventricle and not the 'Reset Timer' state of the atrium. So basically the general flow of a complete cycle of the pacemaker goes in the following path:

Reset Timer A → Wait A → Pace A →

Reset Timer V → Wait V → Pace V.

Then the process continues in a cyclic manner again.

The following is the state diagram.

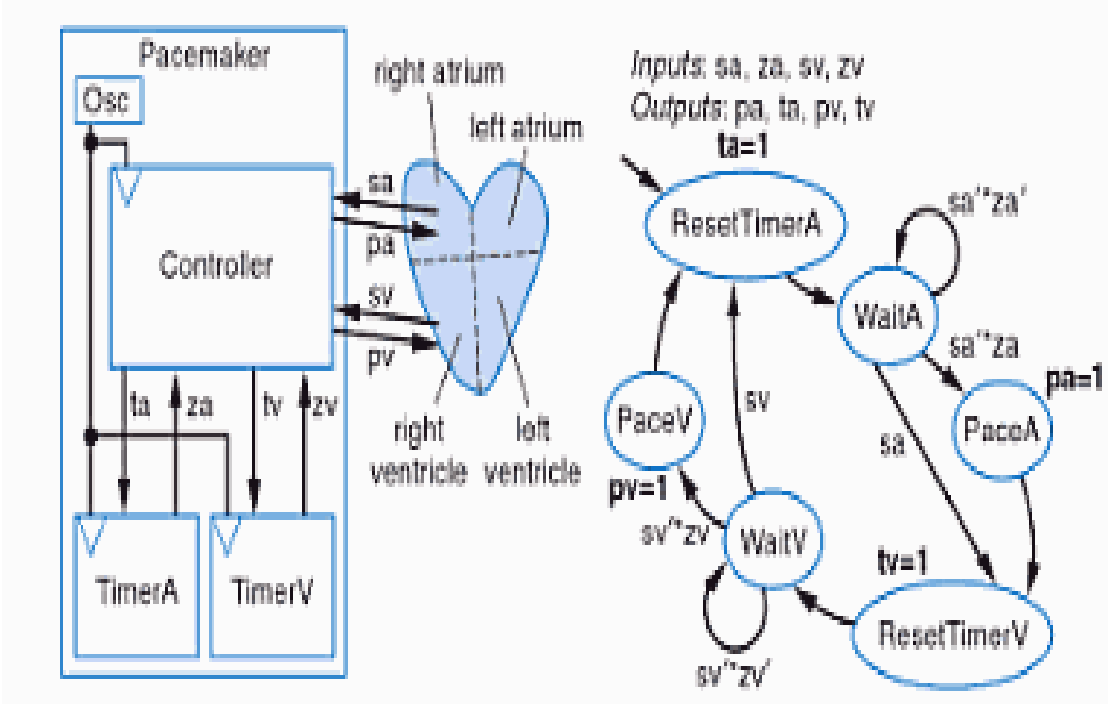

FIG.3.6 State Diagram of Dual chamber pacemaker.

3.3.2 State Table:

The inputs and outputs hold the same significance; ‘a’ suffix stands for atria, and ‘v’ suffix sands for ventricle. E.g.

Inputs:

sv: sensing parameter: 1 if contraction is sensed in the ventricle.

zv: timer output: 1 if timer reaches 0 for ventricle wait state.

Outputs:

tv: output to timer: 1 if timer for the ventricle is to be reset.

pv: output to heart : 1 if pacing needs to be done in the ventricle.

State	Function	Input	Input	Input	Input	Output	Output	Output	Output
		sa	za	sv	zv	pa	pv	ta	tv
A	Wait A	0	0	x	x	0	0	0	0
B	Pace A	0	1	x	x	1	0	0	0
C	Reset A	1	0	x	x	0	0	1	0
	Timer A	1	1	x	x	0	0	1	0
D	Wait V	x	x	0	0	0	0	0	0
E	Pace V	x	x	0	1	0	1	0	0
F	Reset V	x	x	1	0	0	1	0	0
	Timer V	x	x	1	1	0	0	0	1

Table 3.2 State Table of Dual Chamber Pacemaker

3.4 Rate Responsive Pacemaker

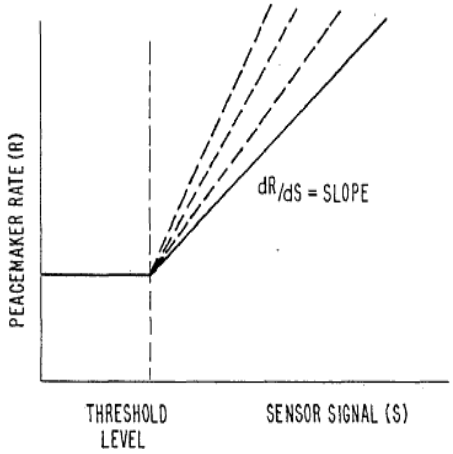

Fig 3.7 Relation between sensing and pacing rate in a rate responsive pacemaker

A rate-responsive pacemaker contains one or more special sensors to detect changes in the body indicative of the need for more oxygen. With the detection of a change, the pacing rate is increased according to the programming of the pacemaker.

It helps in case of abnormalities like Chronotropic Incompetence even with the proper functioning of heart where pacemaker is not required. Commercial Rate Responsive Pacemakers make use of a software called PRPS- Pacing Rate Profile Software. It is an Algorithm computing the best correlation between heart rate & metabolic needs,

The common types of sensors used in this class of pacemakers are:

Activity sensor -A rate-responsive pacemaker with such a sensor allows the heart rate to vary in response to various levels of physical activity. The sensor, which is attached to the inside of the pacemaker's case (metallic), registers pressure waves owing to the muscle movement or movement of the body. The pacemaker's circuitry converts these pressure waves into electrical signals to adjust the rate of pacing. The broad classifications of activity sensors are

- Accelerometers
- Vibration Sensors

Physiological sensor – This is a component of some rate-responsive pacemakers that detect variations in the frequency, speed and depth of breathing. This allows the pacemaker to ascertain if the heart rate is adequate for the activity one is involved in and if additional pacing help is required. Some examples are sensors involving

- Minute ventilation
- QT Intervals
- Myocardial Vibrations
- Temperature
- pH Indications

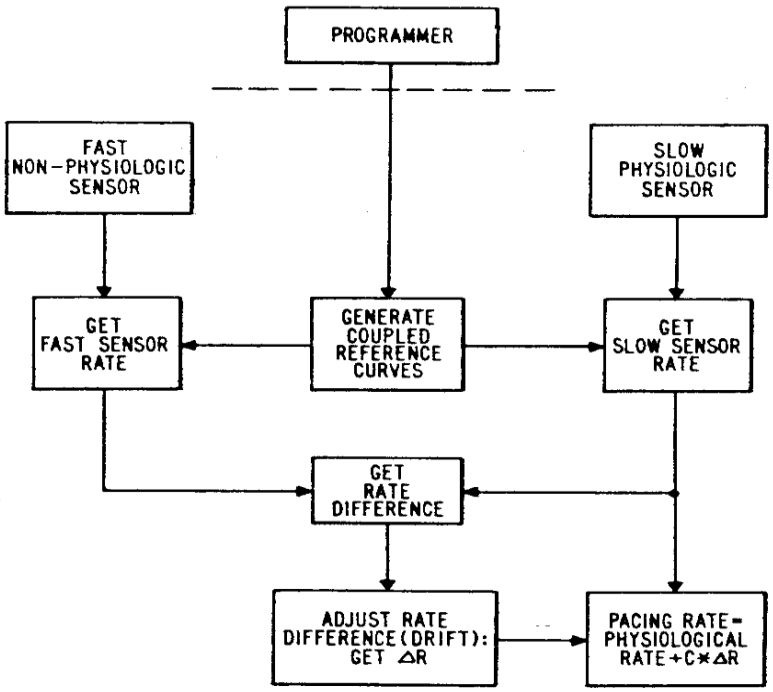

Fig 3.8 Block diagram showing the mutual working of sensors in a rate responsive pacemaker

3.5 VHDL Programming

The general method of coding remains same in principle: a Mealy State Machine coding in VHDL using the usual coding practices. It is ultimately optimised in terms of time taken for execution and other constraints for best results

. Considering the clock frequency and constraints of programming the 0.8 seconds wait state could not be incorporated in the code. Instead the main frame of the process rested on the coding of a single chamber demand mode cardiac pacemaker to verify the correct response of the machine to the inputs via the outputs and next state changes. This was further extended to the Dual chamber pacemaker.

Then an experimental value of delay was given which was restricted to a few nanoseconds and the single camber pacemaker code was tested on it to verify the results if the incorporation of the delay in 'wait' state could give the desired results. A timer was used for the delay process. The code was then extended for a dual chamber pacemaker.

Finally the rate response concept was put in the code to take a value corresponding to the body requirements of oxygen, and hence the pacing rate and give the pacing pulses corresponding to the changing values. Here the timer input and output were confined to be internal signals and structural style of modelling was used giving output only the pacing pulses.

Conclusively the coding was found out to be a cumulative process with gradual development through levels to culminate at the end results.

3.6 Pacemaker Modes

Pacemakers pulse generators can be of various types depending on the modes of pacing. The human body has different requirements and those vary form one person to another. Accordingly the pacemaker used for one person cannot be generalised for all. Depending on the needs of the patient and the programmability options, the pacing pulse can be sensed as inhibited or triggered by the R wave of the ECG. Also there are competitive or non-competitive modes of pacing depending on if the intrinsic pacing of the heart is sensed by the pacemaker or not. Pacemakers can be:

Demand: if the pacemaker senses the presence of an R wave and paces only if the R wave is not present.

Non Demand: if the pacemaker paces the heart irrespective of the presence of an intrinsic R wave.

Triggered: if the pacemaker paces the heart every time a R wave is detected i.e the pacing function is triggered by the R wave.

Inhibited: if the pacemaker paces the heart every time a R wave is skipped i.e the pacing function inhibited by the R wave.

As examples, the DDDR, VVI and DDI modes have been specifically programmed and results were observed. The following table shows the different working modes.

I	II	III	IV	V
Chamber(s) paced	Chamber(s) sensed	Response to sensing	Rate modulation	Multisite pacing
O = None	O = None	O = None	O = None	O = None
A = Atrium	A = Atrium	T = Triggered	R = Rate modulation	A = Atrium
V = Ventricle	V = Ventricle	I = Inhibited		V = Ventricle
D = Dual (A+V)	D = Dual (A+V)	D = Dual (T+I)		D = Dual (A+V)

Table 3.3 Pacemaker modes

3.7 Simulation Results

3.7.1 Single Chamber Pacemaker

3.7.1.1 Single Chamber Demand mode Pacemaker without Delay

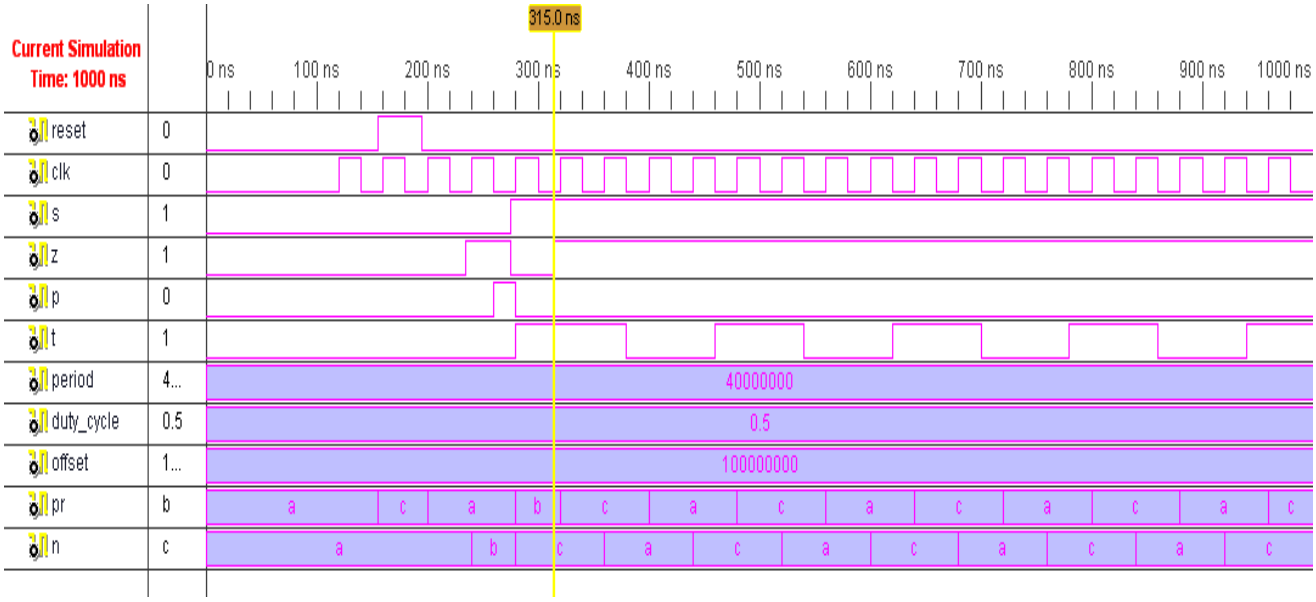

FIG 3.9 Test Bench Waveform for Single Chamber Pacemaker without Delay

3.7.1.2 Single Chamber Demand mode Pacemaker with Delay

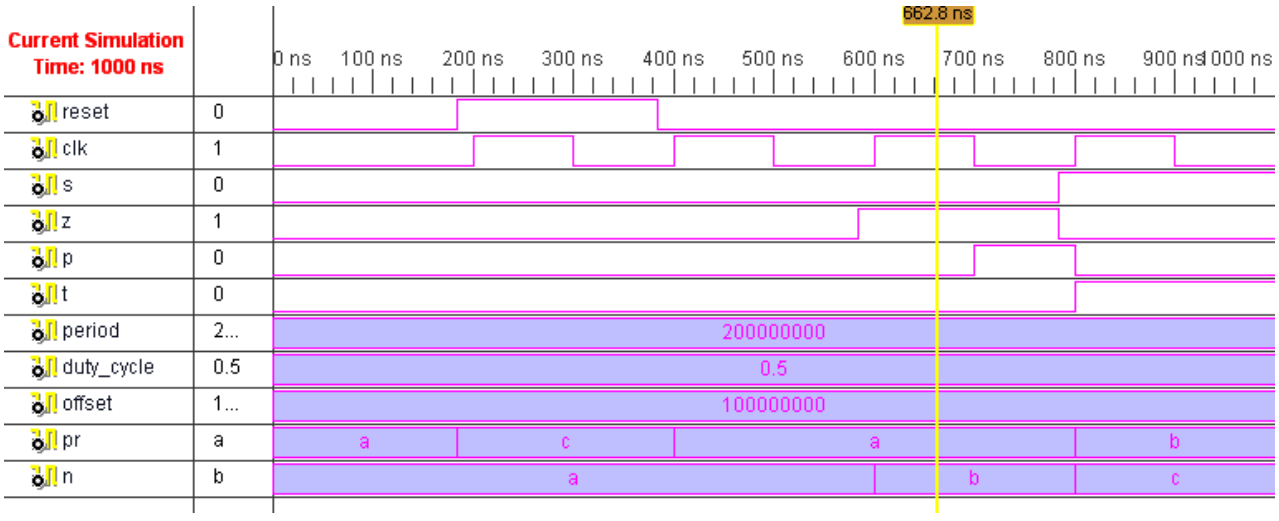

FIG 3.10 Test Bench Waveform for Single Chamber Pacemaker with Delay

3.7.2 Dual Chamber Pacemaker

3.7.2.1 Dual Chamber Demand mode Pacemaker without Delay

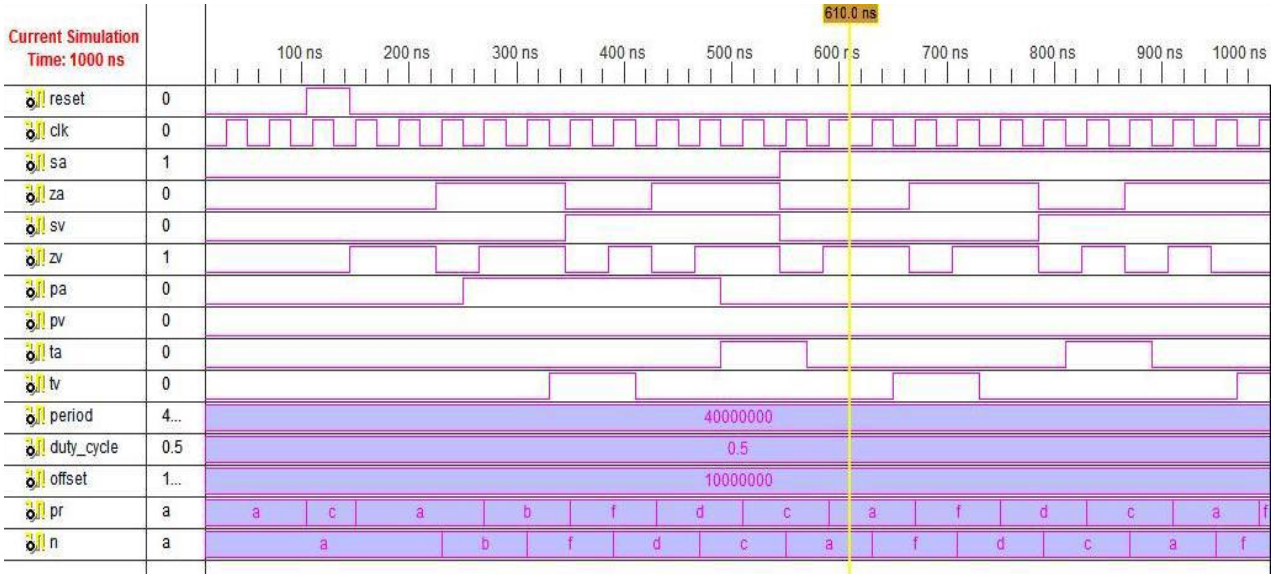

FIG 3.11 Test Bench Waveform for Dual Chamber Pacemaker without Delay

3.7.2.2 Dual Chamber Demand mode Pacemaker with Delay

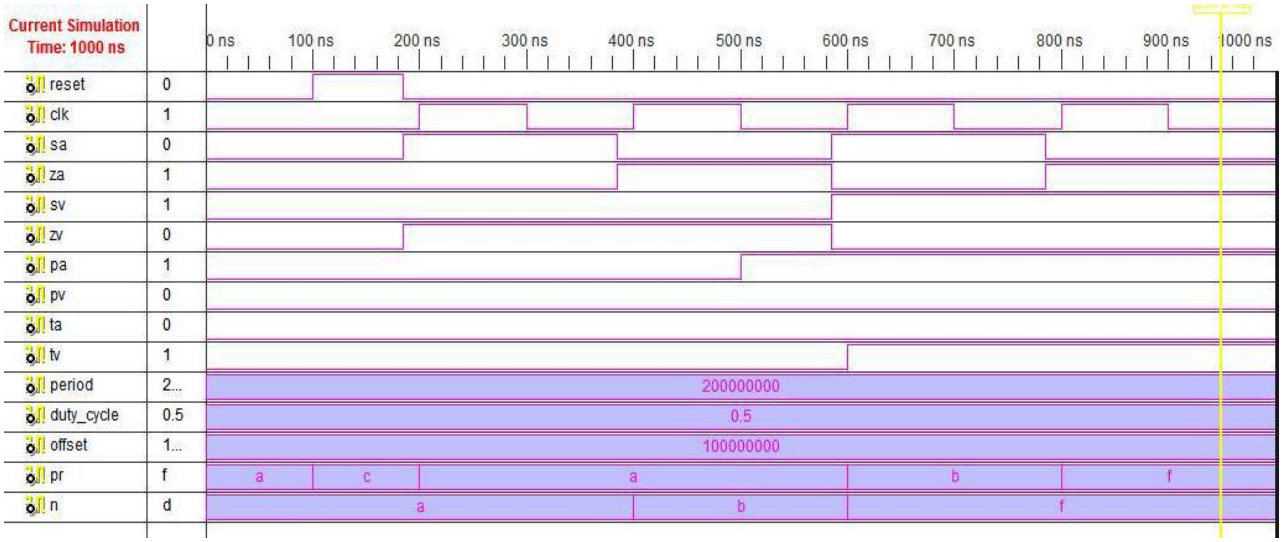

FIG 3.12 Test Bench Waveform for Dual Chamber Pacemaker with Delay

3.7.3 Rate Responsive Pacemaker

3.7.3.1 Single Chamber Rate Responsive Pacemaker

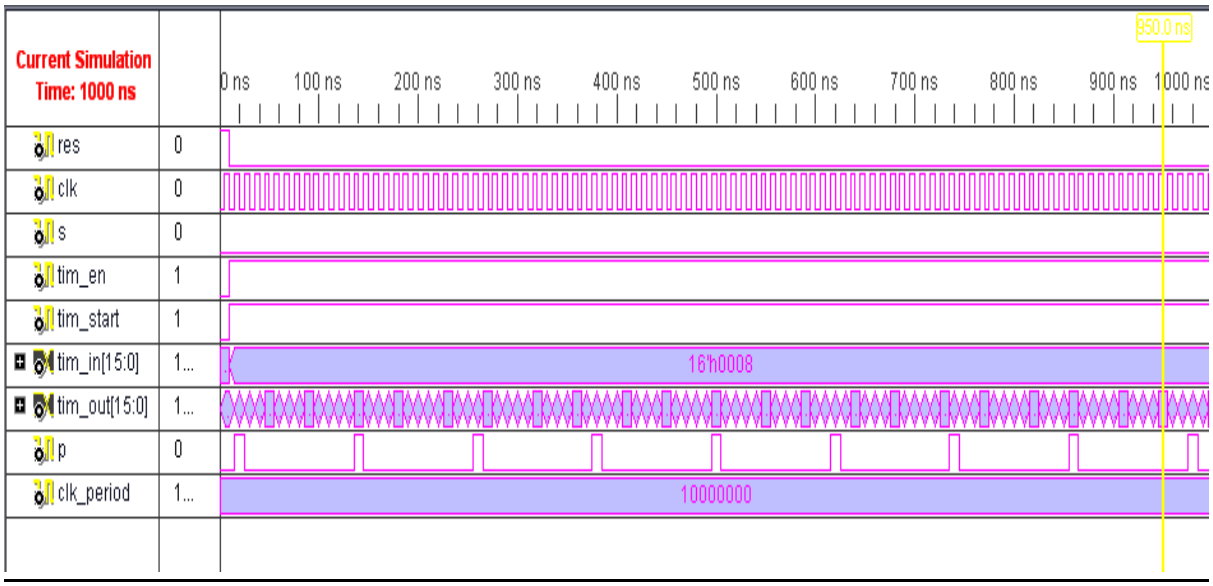

FIG 3.13 Test Bench Waveform for Rate Responsive Single Chamber Pacemaker

3.7.3.2 Dual Chamber Rate Responsive Pacemaker

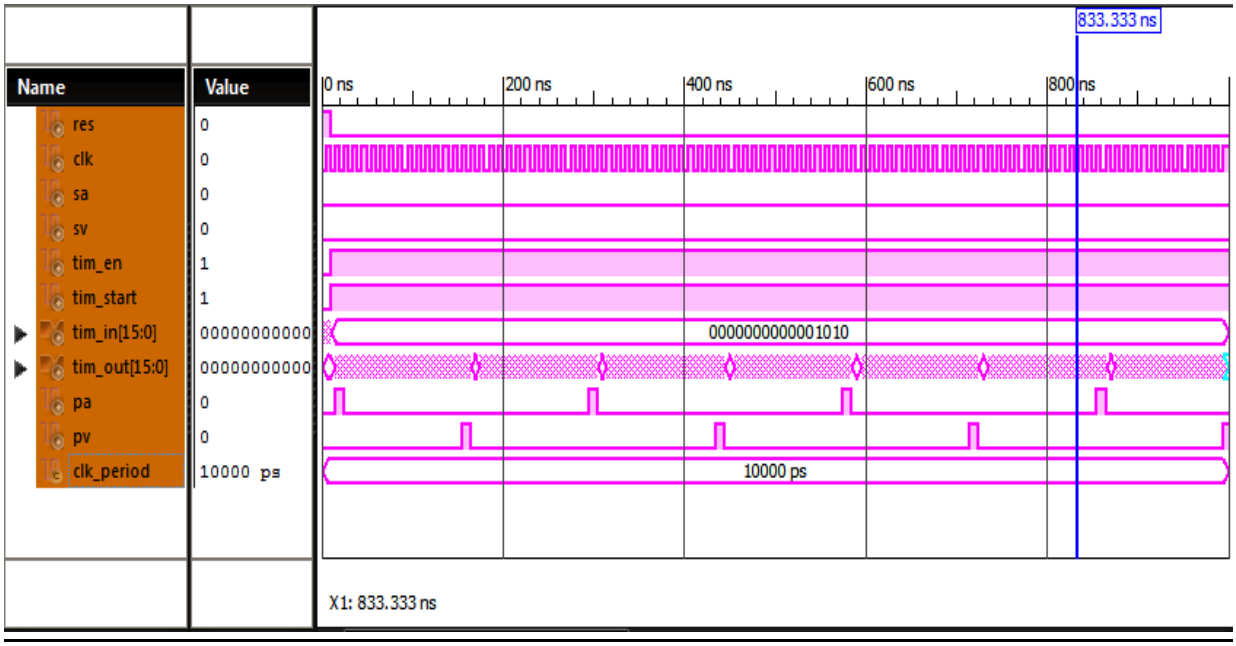

FIG 3.14 Test Bench Waveform for Rate Responsive Dual Chamber Pacemaker

3.7.4 Pacing Modes

3.7.4.1 VVI

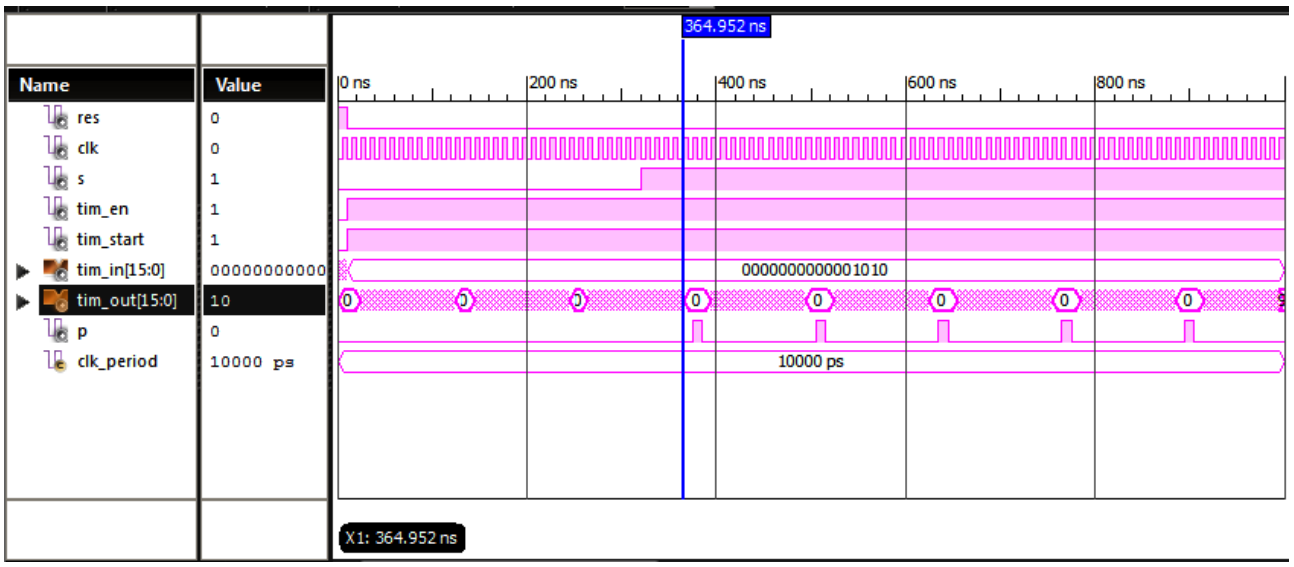

FIG 3.15 VVI mode

3.7.4.2 DDI

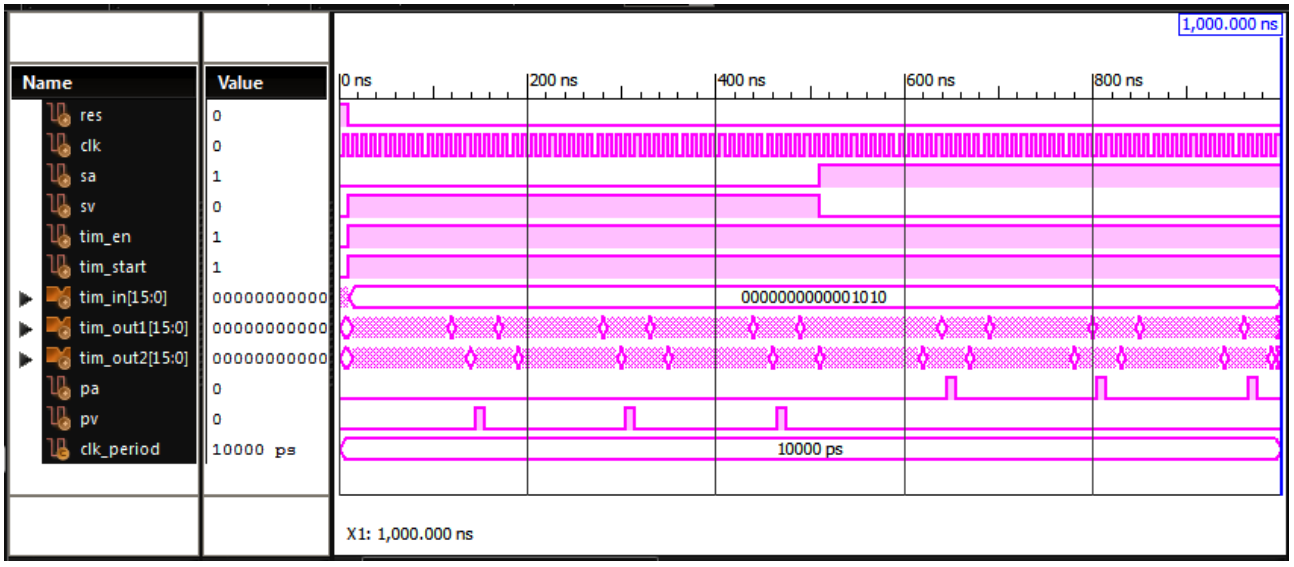

FIG 3.16 DDI mode

3.7.4.3 DDTR

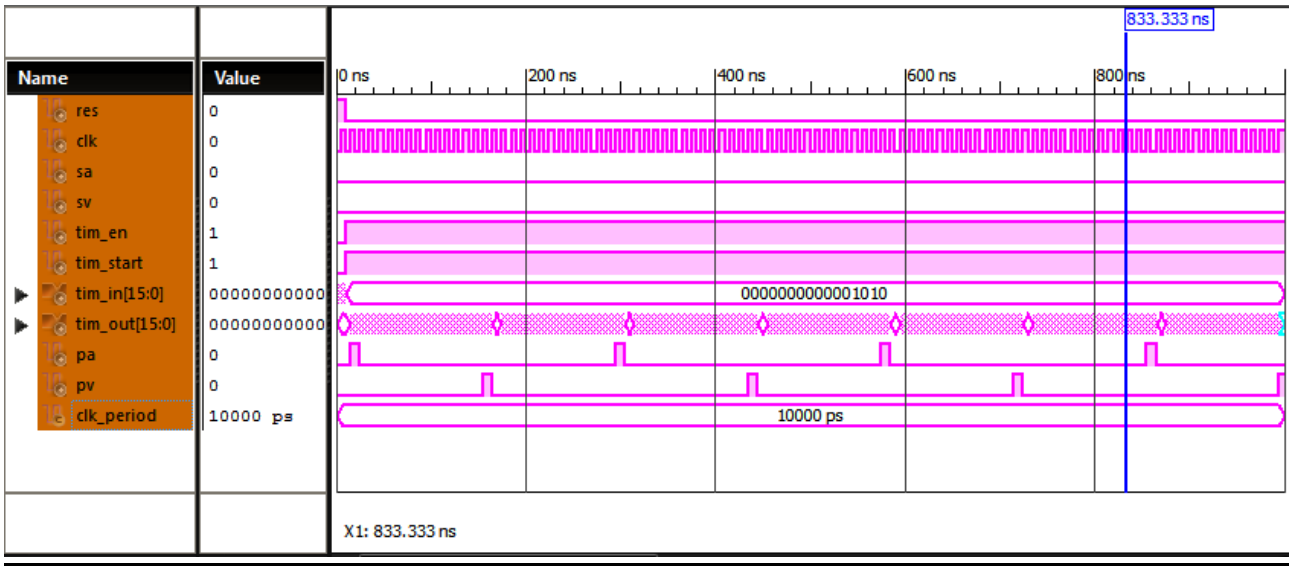

FIG 3.17 DDTR mode

CHAPTER 4

SENSING CIRCUIT

4. Sensing circuit

The next most important part of the Pacemaker after pulse generator is the Sensing circuit. It forms the portion between the dual purpose (pacing and sensing) leads and the pulse generator. Its primary function is to tap the real time signals from the heart coming from the sensing leads and provide input to the pulse generator in a form more suitable to the pulse generator.

The sensing circuit takes up the signals from the patient and performs adequate signal conditioning to get a pulse at every sensed or non-sensed contraction of heart depending on it is in the triggered or inhibited mode. The basic design consists of first tapping out the ECG signal from the heart, then detecting the R wave of the signal and generating a pulse which can act like the input to the pulse generator corresponding to the R wave so that the routing pacing operation may proceed thenceforth.

The leads of the pacemaker, the third component of the device are generally of direct contact type. They work as transducers converting the ionic flow in the body to electron current and then to an electric potential. Ag/AgCl electrode and electrolyte pair is used. A half cell potential is created at the interface with a Nernst potential is generated at the electrolyte-skin interface. Two electrodes can be used to measure the potential differences between two skin surfaces. Since not much design concept is involved here and most of the requirements are readily available, not much importance has been given to this part.

The circuit has been designed in Multisim by first generating an ECG signal from the heart connected via leads. Then the R wave is detected from the wave by using a 555 timer. Subsequently it produces a pulse of required width to be fed into the digital circuitry through an ADC. The further process of pacing continues through the pulse generator. The following sections describe the individual circuit blocks.

4.1 ECG circuit

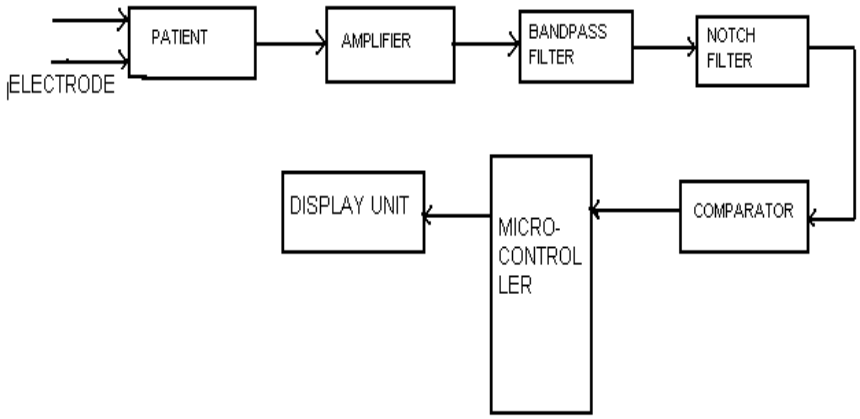

Fig 4.1 Block diagram of an ECG circuit

The first block of the sensing circuit generates the ECG (Electrocardiograph) of the heart. The signals are captured from the three extremities- right arm, left arm and left leg. These reflect the signals from the heart and the leg is taken to be the reference level. Being the maximum distance from the heart, it is assumed the heart signals become sufficiently weak by the time they reach the feet.

4.1.1 Amplifier

The differential signals from the two arms are fed into the input of an instrumentation amplifier. The strongest ECG signal has a magnitude of 0.5-10 mV. So amplification is needed. The most common amplifier used is AD620, and it is the first choice for most biomedical applications. It is used for this purpose because of the following reasons:

- High input impedance.
- Low leakage current.
- Frequency response is flat from 0.05-150 Hz.
- It has high CMRR.

The internal resistor of the amplifier is trimmed at 24.7 KΩ. So the gain of the amplifier is decided simply by the Gain Resistor Rg (in KΩ).

$$Gain = \frac{49.4}{Rg} + 1$$

In this project, Rg is taken to be 249 Ω. Thus the gain approximates to 200.

The schematic of the amplifier designed in Multisim is shown in the subsequent sections.

4.1.2 Band-pass filter

The amplified signal from the AD620 is still contaminated with a lot of noise. Owing to the human body artifacts like motion artifacts are introduced which are inevitable in any medical circuit. So to remove the noise a bandpass filter comes into the picture.

Typically, the range of the filter is from 200 Hz to 2 KHz. It is obtained by cascading two active filters- a low pass filter with a cut off of 2 KHz and then a high pass filter of 200 Hz. The negative feedback in the filters is used to determine the cut off frequency while the positive feedback decides the gain of the circuit.

4.1.2.1 Low pass filter

The values of R1, R2, R and C are chosen such that the cut off frequency equals 2 KHz.

$$Gain = \frac{R1 + R2}{R2}$$

$$.frequency = 1/(2 * pi * R * C)$$

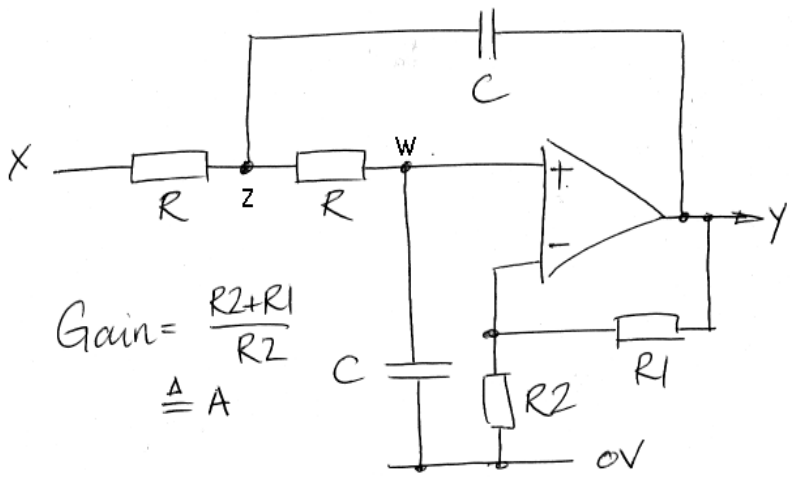

Fig 4.2 Low pass filter.

Here R= 10 KΩ, C= 1 uF, R1= 10 KΩ, R2= 10 KΩ

4.1.2.2 High pass filter

Likewise for the high pass filter, same expressions for the gain and cut off frequency apply. The values of the resistors and capacitors are accordingly changed to give the lower cut off frequency as 200 Hz.

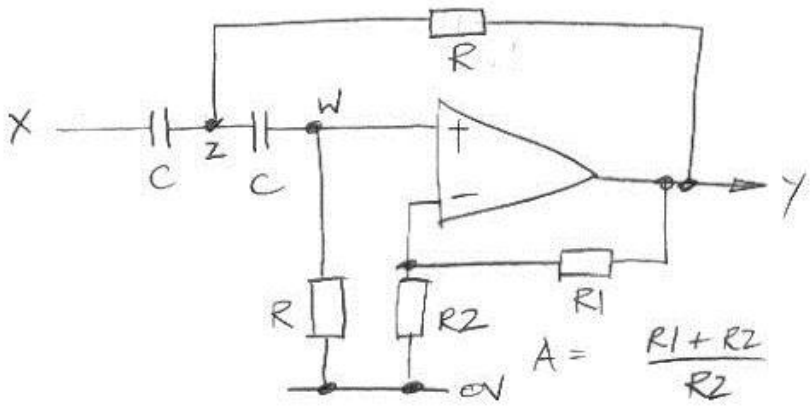

Fig 4.3 High pass filter.

Here R= 31.8 KΩ, C= 10 uF, R1= 10 KΩ, R2= 10 KΩ

The schematics of the filters are designed and simulated in Multisim and circuits follow.

4.1.3 Notch Filter

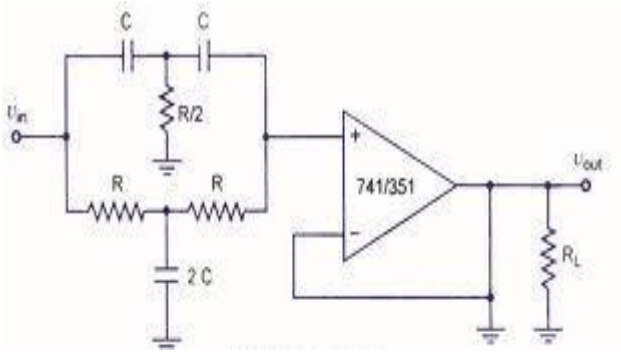

Fig 4.4 Notch Filter

The output of the bandpass filter is passed on to a Notch filter. Biomedical circuits being highly safety critical devices, Electrical isolation is an important aspect of the ECG circuit. To reduce the electrical noise a twin T Notch filter of cut off frequency 50 Hz is used.

$$frequency = 1/(2 * pi * R * C)$$

The values used in the project are R= 318 KΩ, C1= 0.01 uF.

The frequency selector circuit cuts off exactly the signals of 50 Hz frequency. The opamp acts as a voltage follower delivering the input to the output with almost unity gain factor but removing the power-line noise.

The signal obtained next is ideally sent to a comparator and microcontroller to obtain the exact ECG waveform and aid its display on a screen or paper. But our purpose is solved here by simply detecting the R peak of the wave. So additional circuitry is avoided as it adds to the cost and complexity of the device. This output is adequately usable by the R wave detector and input pulse generator to be studied in the next section.

4.2 Input Pulse Generation Circuit

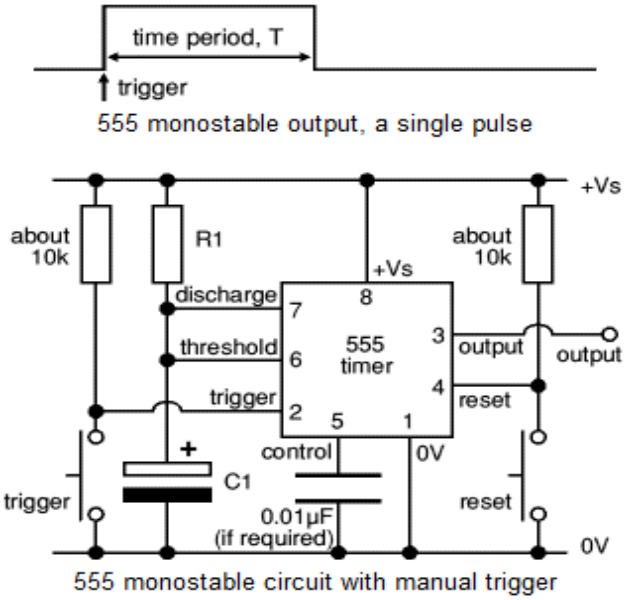

Fig 4.5 Input pulse generation circuit

The output of the ECG circuit is sent as a trigger to the 555 IC configured in the monostable mode. The device works in the following principle:

The timing period is triggered when the trigger value is less than $^1/_3$ Vs, this makes the output high to +Vs and the capacitor C1 starts to charge through resistor R1. After this step, further trigger pulses are ignored.The value of threshold input keeps track of the voltage across C1 and when this attains $^2/_3$ Vs the time period completes and the output is pulled down to low. Simultaneously discharge is connected to ground, discharging the capacitor and ready for the next trigger pulse to be applied. Since the reset function is not required the reset pin should be connected to +Vs. Every time an R wave is detected a pulse is generated to be given as input to the pulse generator of the pacemaker through digital circuitry. Time period of the pulse is given by

$$Time = 1.1 * R1 * C1$$

The values chosen in our circuit are R1= 10 KΩ, C1= 100 uF.

4.3 Circuit Design

4.3.1 Amplifier and Bandpass filter

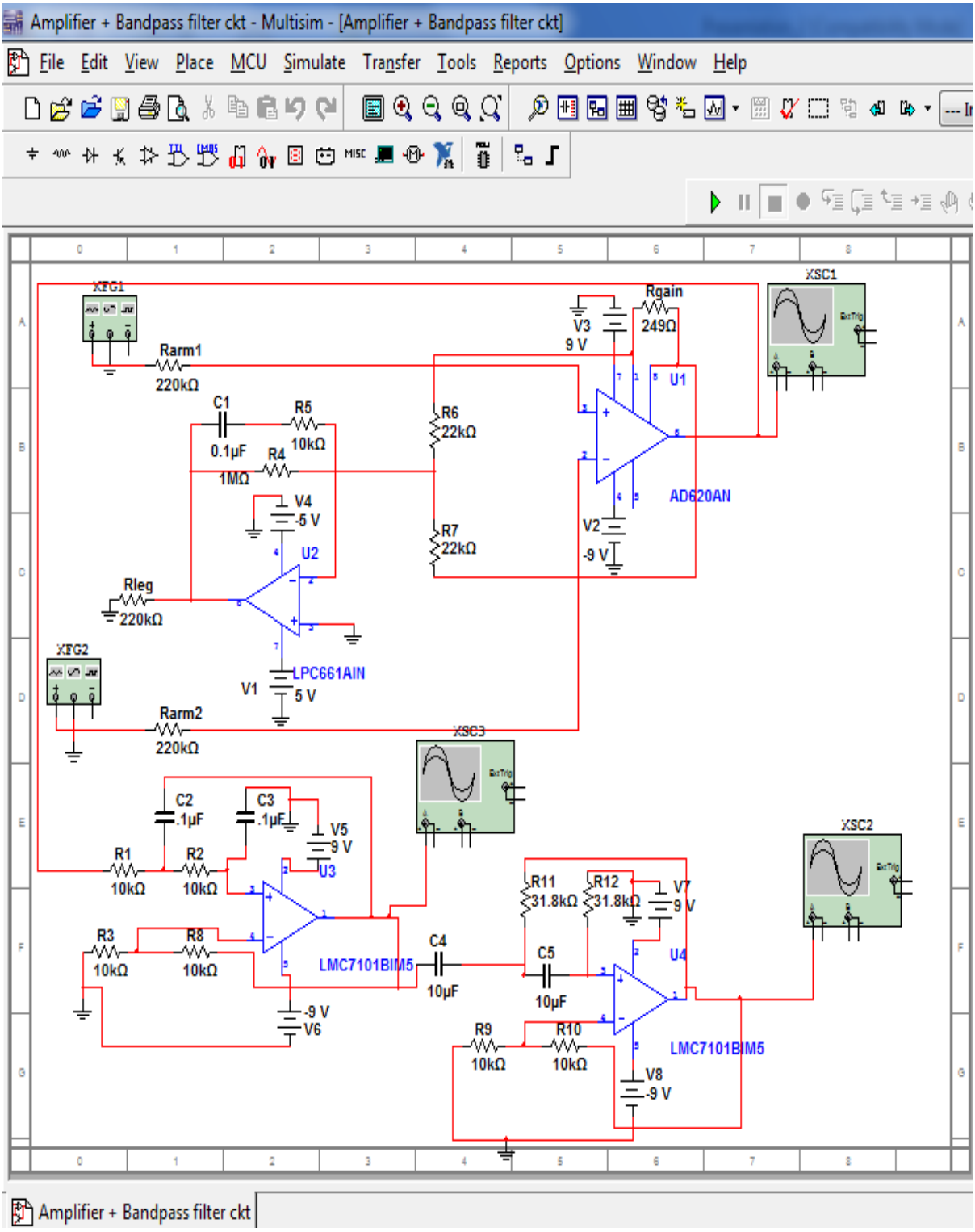

FIG 4.6 Bandpass filter and Amplifier of ECG circuit

4.3.2 Notch Filter

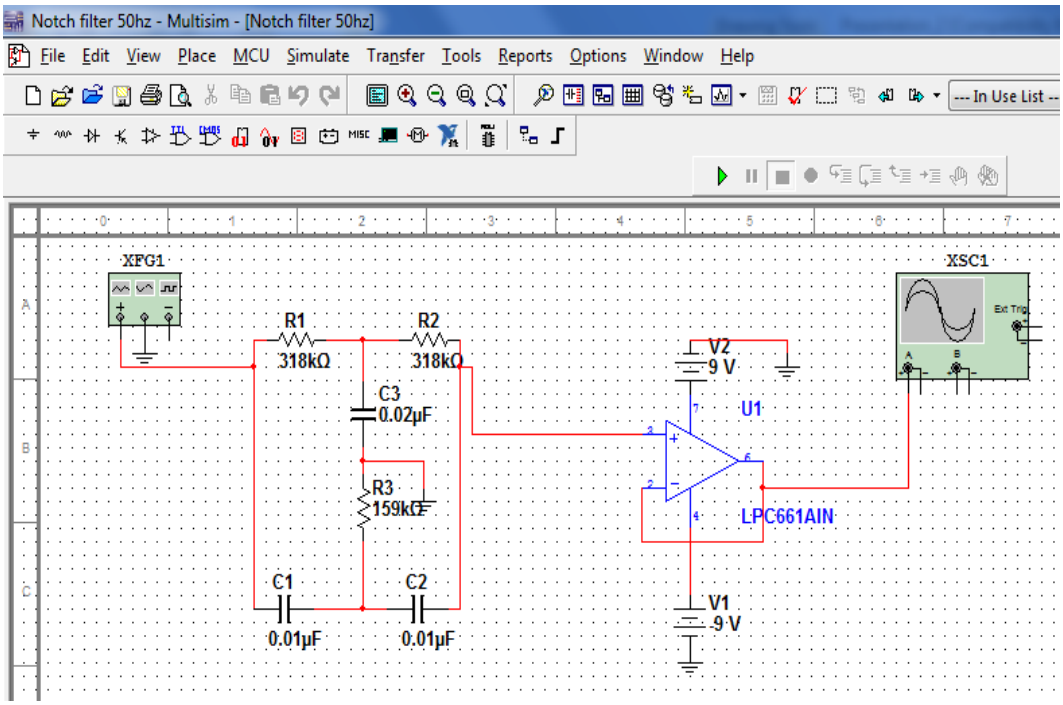

FIG 4.7 Notch filter

4.3.3 Input Pulse Generation Circuit

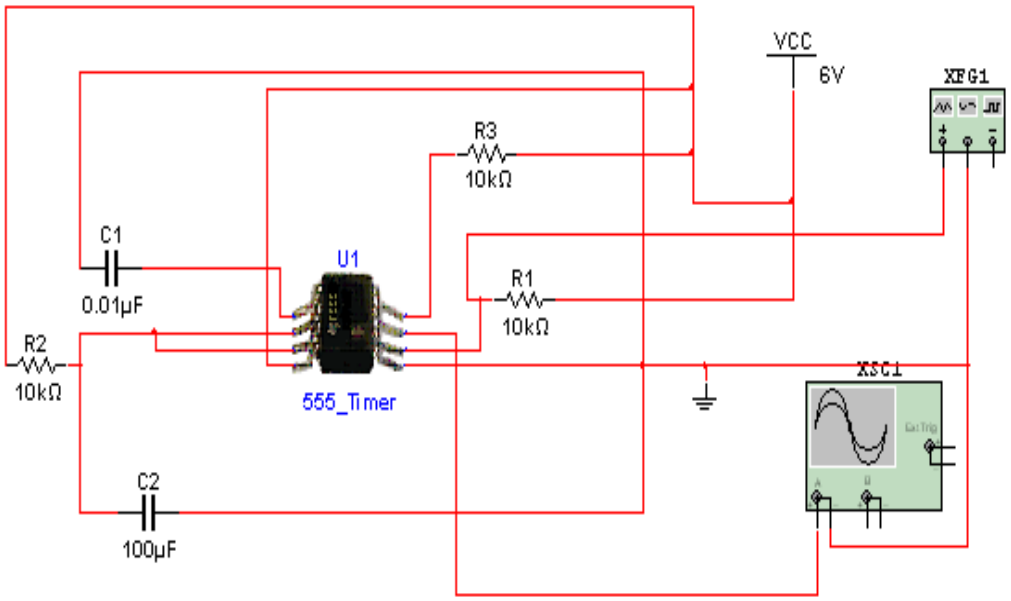

Fig 4.8 Input Pulse Generation

C H A P T E R 5

P E R I P H E R A L S

5. Peripherals

The process of implantation of a pacemaker in the body of a patient is a very intricate and complicated process. Alongside the device is a very effective method to monitor the physical condition of the person owing to its proximity to the heart and hence accuracy of the monitored data. In the process of deciding how to stimulate the heart with impulses, the pacemaker collects data indicating the electrical activity of the heart. By evaluating this information, the pacemaker can change its parameters to every patient's special physiological need and thereby devise an optimal treatment. The leads connecting the heart chambers thus serve both as sensory and stimulatory electrodes. Instead of discarding the collected information, it is continuously analysed and stored by the pacemaker for future use. By means of a technique known as telemetry, it is possible to transfer data between the pacemaker and external equipment, thereby enabling the physician to conclude about the condition of the patient. The information collected by the pacemaker, makes it possible to reprogram the pacemaker and thereby changing the settings for the device. This further allows the device to be customized for the patient's specific requirements.

For this process of storage and telemetry there are a number of peripherals needed by the pacemaker in addition to its routine components. A few of the requirements can be briefly classified to fall under the category of

- storage
- telemetry

As such the additional devices needed in the hardware and software forefront are analysed through case studies. Suggestions for improvement are provided with respect to each of the cases.

5.1 Memory

Pacemakers have been able to store diagnostic data for a long time, but due to limitations in hardware the use has been rather restricted. The storage of data in current commercial pacemaker platforms is characterized by small data sets, low degrees of compression with ad hoc solutions and is often hardware controlled. [16]

5.1.1 CASE STUDY:

Patent number US4873980

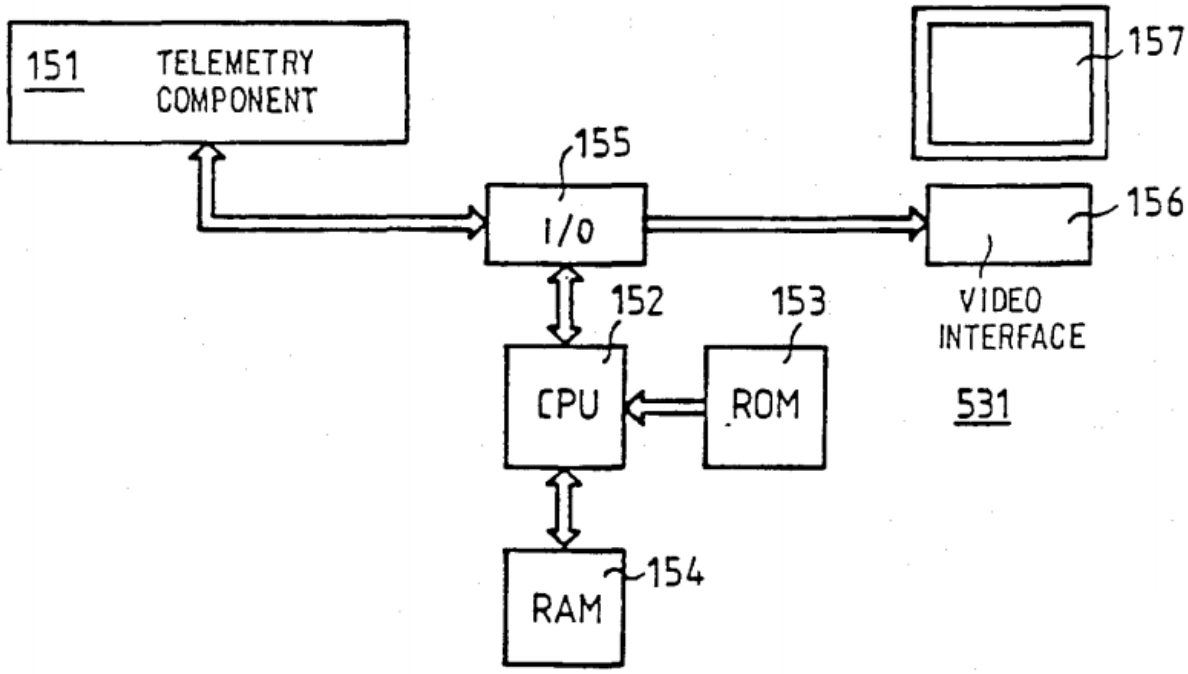

Fig 5.1 General Structure of the memory and peripheral architecture of US4873980

The Memory Structure of US4873980 has RAM ROM buses and CPU just like a general purpose microprocessor. The usage is entirely different though, and it is one of the most commonly used pacemakers commercially. Analysis of its internal circuitry revealed it

to employ a state of the art technology. Additionally, there can be certain improvements possible in this regard.

5.1.2 SUGGESTIONS FOR IMPROVEMENTS:

5.1.2.1 Hardware

- Cache Memory can be incorporated in an effective manner.
- The location of memory with respect to processor can be considered as memories like cache can facilitate for easier and faster access when closer.
- Use of ROM can be made judiciously.

5.1.2.2 Software

- Introduction of OOPs concept rather than assembly level language prevalent in most pacemakers can pave way for better functionality
- Compression techniques can be used for the storage of data.

5.1.3 COMPRESSION:

To store huge volume of data in the available space compression techniques serve as the most effective medium.

5.1.3.1 Data storage methods

Data storage methods in the pacemaker include

- **Histogram:** Using histogram counters, it is possible to get statistical information about events in a compact but still revealing form. The first type can be characterized as a label histogram , where each bin has its own label

describing the contents The other form of histogram used in the current pacemaker platform is the range histogram, in which each bin corresponds to a specific range. [16]

- **Event recorder:** The event record is a more detailed way of storing event data than the histogram. Each event occurring in the device is recorded and placed in a circular buffer with a specified size. The buffer adheres to the first-in-first-out (FIFO) paradigm in that new events overwrite older events stored in the buffer due to storage space limitations. Various triggers can, however, cause a part of the circular buffer to be more permanently stored for future reference. These triggers include several intrinsic heart events as well as extrinsic commands (such as placing a magnet on the patient's chest).[16]

- **IEGM (Intra Cardiac Electrogram):** IEGM recordings are a more detailed view of the intracardiac electrical events than the event records. The two types of information are often used in combination for determining the status of the pacemaker settings and diagnosing the patient. The IEGM samplings contain large amounts of data points as well as other information such as timestamps, sampling rate and measured parameter types. In addition to IEGM samplings, other parameters such as battery status, intrinsic heart rate and pacing thresholds are recorded in the same manner.[16]

Now for these data to be compressed, the compression can either be lossless or lossy. In case of lossless compression no data is lost in the process of compression while lossy compression involves a certain amount of data loss.

5.1.3.2 Compression techniques

5.1.3.2.1 Lossless Compression

- **Difference Encoding:** A particularly attractive alternative for compressing data in the pacemaker environment is run-length encoding, which is applicable to streams of sequential data. The technique can be used to reduce the size of any stream of data but the amount of compression depends on the character of the data. Run-length encoding compresses a run of duplicated items by storing the value of the duplicated once, followed by the length of the run. Difference encoding techniques cannot achieve as high amount of compression as other lossless compression techniques, but is easy to implement and fast to execute.[16]

- **Table Compression:** Some data values occur more frequently than others in a collection. A statistical table is constructed with all data points and their corresponding frequencies. Then, each data value is mapped to a bit sequence where the most frequent data value gets the shortest bit sequence (usually just one bit). All values get mapped to a bit sequence where the longest bit sequence corresponds to the least frequent value. There are many implementations of table compression described, but the most well-known one is the Huffman code. Table compression results in a moderate compression and the implementation is rather straightforward. However, the statistical calculations preceding the coding of compressed data may require some extra processing time thereby reducing the real-time performance.[16]

- **Adaptive Compression:** Algorithms using adaptive compression analyze the data they are compressing and modify their behavior accordingly. These

algorithms often provide very high compress ion ratios and work in several lossless techniques. The great negative aspect of adaptive compression techniques regarding the pacemaker domain is the need for processing time for data calculations.[16]

5.1.3.2.2 Lossy Compression

- **Data Thinning**: Perhaps the most intuitive way of reducing the size of a data point sequence is to simply reduce the number of data points. Reducing the sampling frequency by removing data points, it is possible to accomplish large gains in storage capacity.[16]

- **Precision elimination:** An alternative way of reducing the memory requirements for storing data is to reduce the precision of data. This can be accomplished in several ways. One method is to simply convert large real-type numbers to integers requiring much less storage space (typically 1-2 bytes per number as compared to 4-8 bytes). A potential disadvantage of this approach is that the uncompressed data is in a different format than the compressed information.[16]

- **Curve fitting:** This is an attempt to fit polynomial curves to data points, thereby describing the data in a very compact manner. Many numerical methods exist (including Bezier curves, interpolation and splines) for these purposes. Depending on the underlying data (a continuous data sequence is preferred), they all appear as suitable candidates for compression of data.

- **Transform based methods:** by using mathematical transforms such as the Fourier or wavelet transforms, it is possible to compress data to a very high degree. However, this process usually requires large computing efforts.[16]

5.1.3.3 Algorithms

There are various algorithms which can be followed for optimized compression of data. A few are enlisted below. Reader may go through the references for a detailed idea of the algorithms.

- Data thinning
- AZ Simple
- AZTEC 8
- Adaptive AZTEC
- Fan
- Cortes
- DCT
- Wavelet
- Template
- Adaptive peak

Based on the work in this project, the Fan and the Adaptive peak algorithms seem to be the best candidates for use in the pacemaker. This is mainly due to the facts that they are both able to compress IEGM curves effectively without losing too much diagnostic information. Also, these algorithms are relatively non-complex in terms of the computing power required.

5.2 Remote Monitoring

Remote monitoring system could give a practical solution to the time-taking and expensive office visits. In this section, we will be describing the present technologies and update on this rapidly evolving topic, by incorporating the latest available data and presently monitored trials.[12]

Implanted pacemakers are intrinsically equipped with a small antenna, which communicates with a portable external device, commonly known as transmitter. A receiver called as a "wand," is connected via a wire to the programmer and stationed on the body's surface over the pacemaker site to receive the transmitted signal from the pacemaker. The wand will be communicating with the device as radiofrequency signals (using either the Industrial, Scientific and Medical (ISM) band from 902–928 MHz or a part of the Medical Implant and Communications (MICS) band from 402–405 MHz). The distance for RF signal communication has risen from several centimeters to several meters and some devices can even communicate wand-less. The transmitters are able to analyse and modify programmed parameters and diagnostic data saved in the device memory with the help of a participating patient (via a wand), or automatically (wand-less), at previously set time intervals. The data which is downloaded from the device by the transmitter is uploaded in the form of an encrypted data, to a clinical database, highly secured and protected, either by a standard phone line or through GSM (Global System for Mobile) connection. The programmer is a computer with particular software and specific hardware modifications allowing highly reliable exchange of the encrypted data and precise communication with the implanted device. The transmission of these data may be started by patient (as a pre-scheduled transmission or triggered by an event (symptom or alert by device).[12]

5.2.1 Case Study:

ULP Implantable Transceiver ZL70101

Important features:

12 Channels

– 402-405 MHz (10 MICS)

– 433-434 MHz (2 ISM)

***ƒ* Selectable Data Rate**

– 200/400/800 kbps raw data rate

***ƒ* High Performance Media Access Controller (MAC)**

– Auto error handling and flow control, Reed-Solomon, CRC

– Typically <1.5 x10^10 BER

***ƒ* Min. E xternal Components**

– 3 pieces plus antenna matching

***ƒ* Extremely Low Power**

– 5 mA continuous TX/RX

– <1mA low power TX/RX

***ƒ* Ultra Low-Power Wake-up Circuit**

– <250 nA

***ƒ* Multiple Start-up Methods**

– 2.45 GHz signal

– Pin Control (for Emergenc y messages, 400 MHz sniffing , low freq uen c y inductive link sniffing or other wake-up methods)

Standards Compatible

– MICS, FCC, IE[13]

5.2.2 COMMUNICATION PROCESS

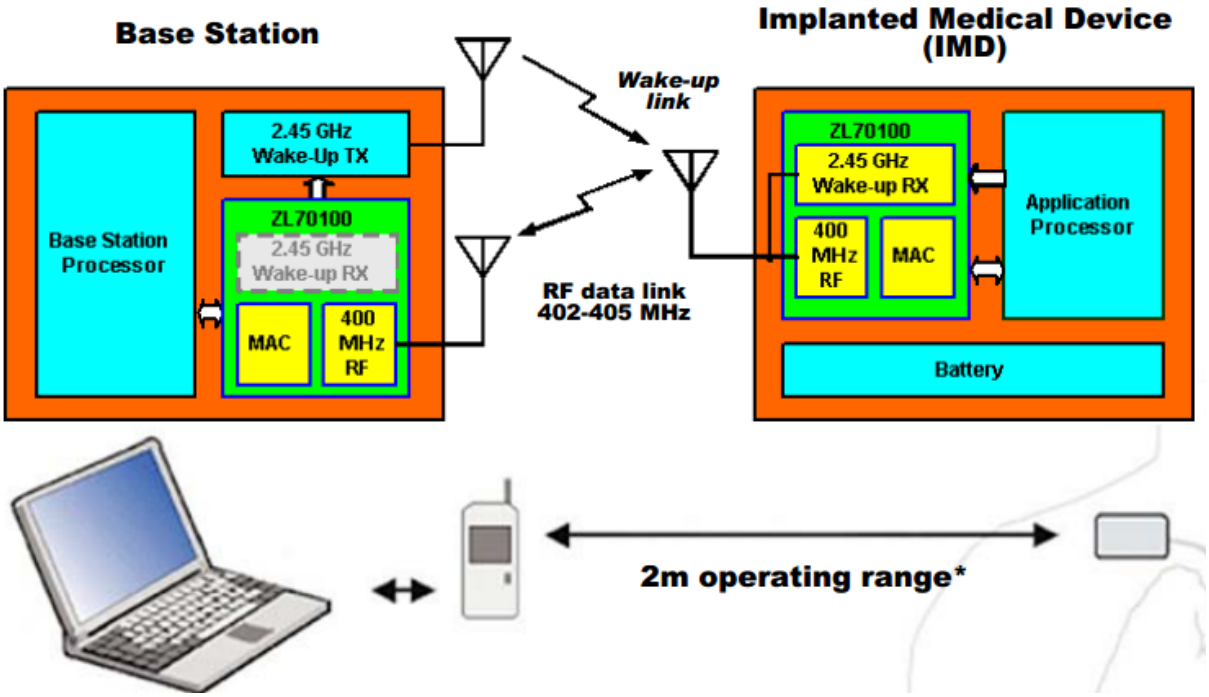

Fig 5.2 Remote Monitoring

The signal is communicated through a wake up link via transceivers. The heart has a transceiver which communicates to the base station via an external transceiver located on the body surface ultimately facilitating communication and remote monitoring

5.2.3 SUGGESTIONS FOR IMPROVEMENT

- The maximum range of communication can be enhanced (at present it is 2 m)
- Number of channels can be used judiciously. Many of them remain unused most of the transmission periods
- Security issues can be addressed to via zero power notification, zero power authentication and sensible key exchange.

CHAPTER6

MODEL BASED CLOSED LOOP TESTING

6 Model based closed loop testing

Traditional software test generation techniques, where the tests are generated independently of the operational environment, are not effective as the device must be tested within the context of the patient's condition and the current state of the heart. Based on these requirements, a closed-loop testing environment between a timed automata-based heart model and pacemaker is described.

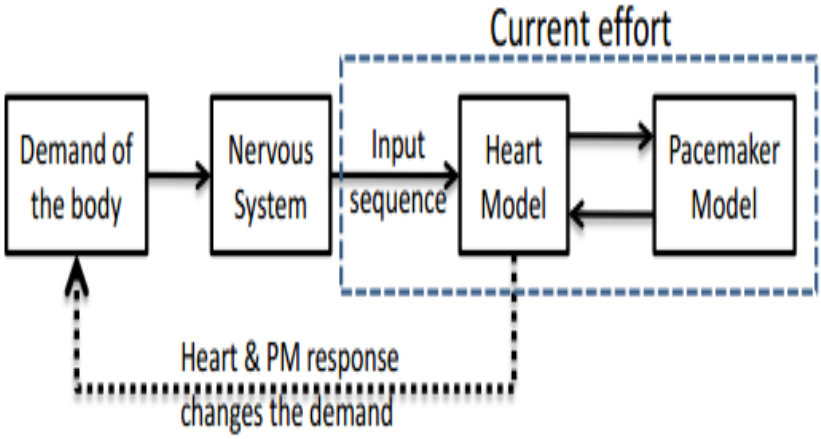

FIG 6.1 closed loop testing

The heart model considered here is the Virtual Heart model (VHM). It has been designed using Simulink and has proved to show effective results. For further clarification on the subject reference section may be looked up.

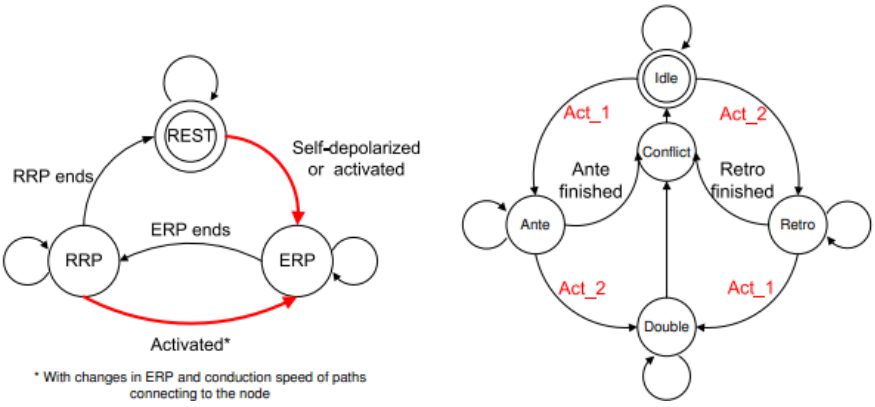

Fig 6.2 VHM to be implemented using Simulink

C H A P T E R 7

H A R D W A R E

I M P L E M E N T A T I O N

7 Hardware Implementation

The pulse generator was implemented in FPGA and checked for compatibility with real time signals. Since procuring a real heart signal was impractical needing the precision in sensory equipment, the R-wave of the ECG wave (which is obtained from the heart) is mimicked by a pulse of 10% duty cycle generated from a 555 timer. It is then sent as the input to the digital circuitry of FPGA via ADC interface to obtain the output pulse waveform from the timing circuit via DAC in the oscilloscope.

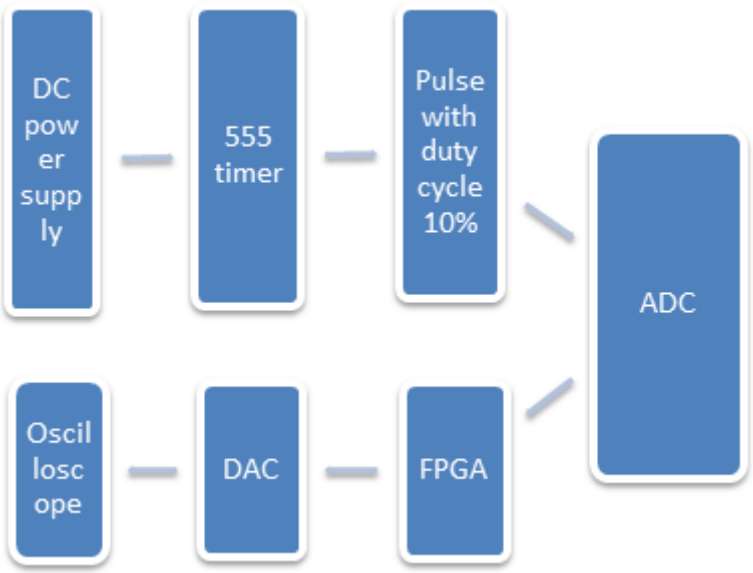

FIG 7.1 Block Diagram for Hardware Implementation of the Pacemaker Pulse Generator

7.1 Input pulse generation

The 555 timer circuit was realized on a separate breadboard. The sensor output (real life R wave of ECG approximated by a pulse of 10% duty cycle) is fed into the ADC which converts the analog signal into digital and sends it to the code in the FPGA. The output of the FPGA i.e. the actual pacing pulses are then converted into analog form by the DAC of FPGA. This is finally sent to the oscilloscope and verified. The 555 Timer works in an astable form

here, and not monostable since we assume the input to the pacer to be periodic in nature. The timing specifications of the input pulse generation circuit are as shown:

$$ton = 0.69 * (R1 + R2) * C$$

$$toff = 0.69 * R2 * C$$

Ton has been assumed to be 1 seconds and Toff to be 10 seconds. Accordingly the values of the components are calculated. The components required are given as below.

- 555 timer
- Resistors: Rb=144.92K (approx 150K),

  Ra= 14.3M (approx 10+(4*1.2)M)
- Capacitors : C=100uF,

  0.01uF
- Breadboard

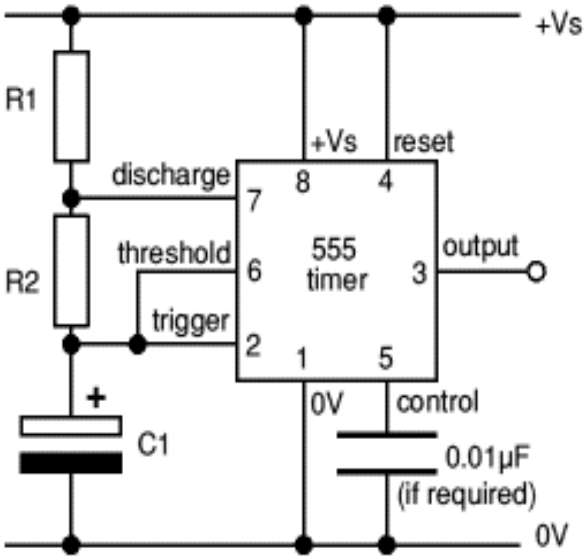

FIG 7.2 555Timer circuit for input pulse generation

7.2 ADC and DAC

The Spartan 3E board provides 2 ADC where both can be sampled simultaneously. The ADC is LTC1407A-1. It gets the input from the external world via an amplifier- LTC6912-1. Gain can be set from the formula

$$D[13:0] = Gain * \frac{Vin - 1.65V}{1.25V} * 8192$$

So the ADC presents a 14 bit, 2's complement digital output. Its value ranges between (-2^13 to 2^13 -1). Input is given via a 6 pin header- J7. Maximum range of gain is 1.25V centred on 1.65V.

DAC is a four channel, serial, 12 bit unsigned resolution, SPI compatible device namely LTC2624. Its input is the output from the FPGA 's pulse generator circuit giving pacing pulses and output is an analog signal corresponding to a particular voltage value in the analog domain. The header used is 6 pin header J5.SPI is used for communication between FPGA and DAC.

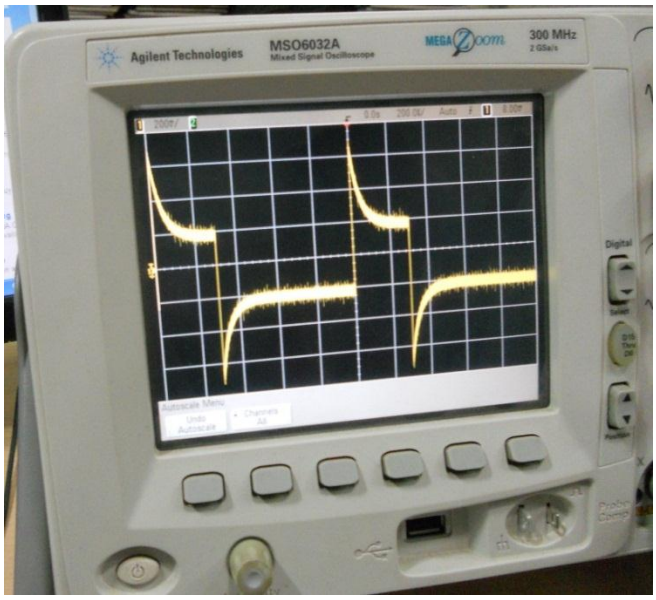

FIG 7.3 Output waveform

CHAPTER 8

CONCLUSION AND FUTURE WORK

8 Conclusion and Future work

The different types of pacemakers were studied. Their application areas were explored. The basic VHDL code was successfully completed and the programs were dumped on FPGA Spartan-3E board. The coding of all the models were sequentially done culminating in the Dual Chamber Rate-Responsive Pacemaker incorporating the Delay and using advanced Algorithm computing the best correlation between heart rate and metabolic needs, Pacing Rate Profile Software (PRPS) and implemented in hardware. The pulse generator was designed for different pacemaker modes too. The final code was optimized and improvised considering the constraints. The device was implemented in VLSI.

The sensor circuit was designed in software. New pacemaker technology focuses on more of software base and as hardware limitations get less restrictive, a new strategy for storing data is required. To enable the storage of more complicated data with substantially larger data sets, a more generic method for storing data has to be thought of. Also remote monitoring using telemetry was observed and analysed. The peripherals were studied with suggestions for selection and improvements on their usage in further research.

The testing methodologies for the device were discussed and the more suitable method was verified. Finally the device was implemented in hardware and conclusions drawn from giving approximate inputs and observation of outputs. Minor errors were observed which were worked upon for reduction.

The **future work** that can be done in this regard includes

- Implementation of peripherals in software and hardware.
- Realising the circuit in CADENCE.
- Optimization and IC design.

R E F E R E N C E

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