DEVELOPMENT OF IMPROVED PERFORMANCE SWITCHMODE CONVERTERS FOR CRITICAL LOAD APPLICATIONS

A Thesis submitted in partial fulfillment of the requirements for the degree of

Doctor of Philosophy
In
Electrical Engineering

By

Swapnajit Pattnaik

Under the supervision of

Prof. Anup Kumar Panda
Prof. Kamalakanta Mahapatra

Department of Electrical Engineering

National Institute of Technology, Rourkela

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Declaration

I hereby declare that the work which is being presented in the thesis entitled "Development of Improved performance Switchmode Converter for Critical load Application" in partial fulfillment of the requirements for the award of the degree of DOCTOR OF PHILOSOPHY submitted to the Department of Electrical Engineering of National Institute of Technology, Rourkela, is an authentic record of my own work under the supervision of Prof. A. K. Panda, Department of Electrical Engineering and Prof. K. K. Mahapatra, Department of Electronics and Communication Engineering. I have not submitted the matter embodied in this thesis for the award of any other degree or diploma of the university or any other institute.

Date 11th January, 2011 Swapnajit Pattnaik

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CERTIFICATE

This is to certify that the thesis entitled "Development of Improved Performance Switchmode Converter for Critical load Applications", being submitted to the National Institute of Technology, Rourkela by Mr. Swapnajit Pattnaik, Roll no. 50602003 for the award of Doctor of Philosophy in Electrical Engineering, is a bona fide record of research work carried out by him under our supervision and guidance.

The candidate has fulfilled all the prescribed requirements

The Thesis which is based on candidate's own work, has not submitted elsewhere for a degree/diploma.

In my opinion, the thesis is of standard required for the award of a Doctor of Philosophy degree in Electrical Engineering.

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RESEARCH PUBLICATIONS

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CONTENTS

ABBREVIATIONS

MOSFET	- Metal-Oxide-Semiconductor Field-Effect-Transistor
PWM	- Pulse Width Modulation
PFM	- Pulse Frequency Modulation
AMD	- Advanced Micro Devices
VR	- Voltage Regulator
HS	- High Side
LS	- Low Side
CMOS	- Complementary Metal–Oxide–Semiconductor
VRM	- Voltage Regulator Module
DC-DC	- Direct Current – Direct Current
SR	- Synchronous Rectifier
ZVT	- Zero Voltage Transition
ZCT	- Zero Current Transition
ZVS	- Zero Voltage Switching
ZCS	- Zero Current Switching
EMI	- Electromagnetic Interference
SRBC	- Synchronous Rectifier Buck Converter
QRC	- Quasi Resonant Converter
DSP	- Digital Signal Processors
CCM	- Continuous Conduction Mode
TI	- Tapped-Inductor
AC	- Alternating Current
ESL	- Equivalent Series Inductance
PSIM	- Power Simulation

PS	- Passive Snubber
SBC	- Synchronous Buck Converter
PI	- Proportional Integrator
PCB	- Printed Circuit Board

NOTATIONS

R_{dson} - On resistance of MOSFET

C_{oss} - MOSFET Output Capacitance

i_{top} - High side MOSFET current

v_{phase} - Instantaneous voltage at output

I_L - Load current

V_D - Drain to source voltage in MOSFET

P_c - Conduction loss

P_{BD} - Body diode power loss

I_{SD} - Body diode current

t_D - Body diode on time

f_{SW} - Switching frequency

Q_g - Gate charge of MOSFET

Q_{oss} - Output charge of MOSFET

Q_{rr} - Reverse recovery charge

P_s - Switching losses

P_g - Gate drive loss

t_{d1}, t_{d2} - Dead time

P_{td1}, P_{td2} - Total body diode loss during t_{d1} and t_{d2}

P_{cdl} - Body diode conduction loss during t_{d1}

P_{rr} - Loss caused by the body diode reverse recovery at the end of t_{d1}

I_{out} - Average output current

ΔI_L - Inductor ripple current

V_f - Forward diode voltage

$\Delta\eta_{cdl}$ - Efficiency degradation due to the body diode conduction during t_{d1}

P_{in} - Input power converter

L_r - Resonant Inductor

C_r - Resonant Capacitor

Q_1 - High side MOSFET

D_1 - Body diode

D_2 - Schottky diode

Q_{GD} - Charge in between gate and drain

$Q_{GS(TH)}$ - Threshold charge in between gate and source

C_1, C_2 and C_b - Clamp capacitor in isolated buck converter

T_x - Transformer used in isolated buck converter

L_m - Magnetizing inductance

L_{lk} - Leakage inductance

T_{on} - On time period

D - Duty cycle

T - Time period of one switching cycle

L_p - Primary equivalent inductance

V_{out} - Output voltage

V_{in} - Input voltage

ΔI, I_{ripple} - Ripple current

n - Turn ratio

D_1, D_2 - Rectifier diode used in secondary side of the transformer

v_{C1}, v_{C2}, v_{Cb} - Voltage across clamp capacitors C_1, C_2 and C_b

V_e - Core volume

A_{min} - Minimum core-cross section

A_{core} - Cross-section of core

B_m - Maximum Flux density

J_m - Current density

A_{window} - Cross section of window of transformer

N_1, N_2 - No. of turns in primary and secondary windings

K_u - Window utilization factor

A_{wire} - Cross section of wire

D_{wire} - Diameter of wire

C_o - Output Capacitor

T_i - Tapped Inductor

I_{Q1}, I_{Q2} - Current through MOSFET Q_1 and Q_2.

L_o - Output Inductor

I_o - Load current

D_S - Schottky diode

C_S - Capacitor across MOSFET S

S, S_1 - MOSFET switches

ω - Resonant frequency

Z - Characteristic Impedance

t_1, t_2, etc. - Instant of Time in different modes

V_{Cr} - Voltage across resonant capacitor

T_D - Delay time

a - Current stress factor

D_{S1}, D_{S2}, D_{S3} - Schottky diodes

I_{Lrmax} - Maximum inductor current

V_{Cbm} - Maximum voltage across capacitor C_b

V_{Crmax} - Maximum voltage across capacitor C_r

t_r - Rise time

t_f - Fall time

I_{omax} - Maximum load current

R - Body diode resistance

ABSTRACT

Emerging portable applications and the rapid advancement of technology have posed rigorous challenges to power engineers for an efficient power delivery at high power density. The foremost objectives are to develop high efficiency, high power density topologies such as: buck, synchronous buck and multiphase buck converters, with the implementation of soft switching technology to reduce switching losses maintaining voltage and current stresses within the permissible range.

Demand of low voltage power supply for telecom system leads to narrow duty cycle which compels to increase operating switching frequency. Design of conventional buck converter under narrow duty cycle is quite objectionable since it leads to poor utilization of components as well as it degrades the system efficiency. A high switching frequency operation reduces the switch conduction time that leads to large increase in switching losses and increases the control complexity. Therefore, duty cycle has to be extended and at the same time switching losses have to be minimized. Transformer based topology can be used to extend the duty cycle. But to reduce switching losses soft switching techniques should be implemented.

An isolated buck converter with simple clamp capacitor scheme is proposed to reduce switching losses and to extend duty cycle by optimizing the turn ratio. Extended duty cycle impose limit on dead time. Dead time has to be controlled with respect to duty cycle to reduce body diode conduction loss and to avoid the shoot through conditions in our proposed topology. The proposed clamp capacitor scheme control the dead time as well as provide better efficiency with reduction in switching losses maintaining ripples within the allowable range.

Current trends in consumer electronics demand progressively lower-voltage supplies. Because of significantly lower conduction losses, synchronous rectifiers i.e. MOSFETs, are

now used essentially in all low-voltage dc power supplies. Passive snubbers or an active auxiliary circuit is generally used to reduce the other important loss i.e. switching loss. Also it reduces the voltage and current stresses of the switches.

In this work two zero-voltage-transition (ZVT) pulse width modulated (PWM) synchronous buck converters are proposed, one with passive auxiliary circuit and the other with active auxiliary circuit. These are designed to operate at low voltage and high efficiency typically required for portable systems. The operation principles and a detailed steady-state analysis of the ZVT-PWM synchronous converters are presented. All the semiconductor devices besides the main switch operate under soft switching conditions. Thus, the auxiliary circuit provides a larger overall efficiency. In addition, the circuits are cheaper and more reliable, and had a higher performance/cost ratio.

Future microprocessor poses many challenges to its dedicated power supplies, such as low voltage, high current, high power density, and high efficiency etc. To decrease the power consumption, supply voltage for the next generations of microprocessors must be as low as possible. The supplied voltage is going to drop to a level of 0.7 V, the total power consumption keeps flying up because of the tremendously increased current. In order to meet the power supply requirements of the new generation microprocessors, a soft-switch multi-phase PWM dc-dc converter with an auxiliary circuit has been proposed. Losses present in multiphase buck converter due to increase components and switches are reduced with the proposed soft switching technique.

The proposed converters presented in this research work are well defined by its mathematical modeling and its mode of operations. The feasibility of all the proposed converters for different applications is confirmed by simulation and experimental results.

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INTRODUCTION

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Chapter 1. Introduction

1.1 Research Background

With the stringent requirements of power supplies for portable electronic equipment under different power ratings pose challenges to power management. The automation in every section of life compel to go for power conversion from ac to fixed dc, ac to variable dc, variable dc to fixed dc and its vice-versa. The growing demand of computers in medical instruments, aircraft, defense, space market, industrial automation and commercial applications impede the general power quality solutions, but sparked the need of precise solutions. With the increasing demand of uninterrupted and high quality power for critical loads, power converter should be properly design to match the nature of the load, the type of power distribution, the quality of local power, and the required reliability. Recent advances in power converter endorses high efficiency, high power density. Lower operating voltages, increased current requirements, and the dynamic characteristics of microprocessor based or microcontroller based system create new demands on power distribution and management. The issues such as achieving high efficiency, high power density, and proper voltage regulation etc. become critical if buck converters are considered for low operating voltage.

Attaining high performance and low power consumption in MP3 players, personal media players, digital cameras, and other portable consumer applications has long been a challenge for designers. Naturally, battery life is of prime importance in handheld battery-powered products, making their success directly related to the efficiency of the power system. A key component of such systems is the step down dc-dc switching regulator, which is also commonly referred to as a step down dc-dc converter or buck converter. In low frequency applications MOSFETs have been used in place of diodes in order to improve the efficiency of switching converters. However, small size requirements encountered in computer systems and portable devices call for increased switching frequencies. As the switching frequency is

increased, the benefit of the low MOSFET on resistance *(R_{dson},)* is diminished by the increase in the switching losses, the gate drive loss, and the body diode loss [1].

Supply voltage scaling is an essential step in the technology scaling process. Two primary reasons for scaling the supply voltage are to maintain the power density of an integrated circuit below a limit dictated by available cost effective cooling techniques and to guarantee the long term reliability of manufactured devices. Microprocessors, with increased power consumption and reduced supply voltages, demand greater amounts of current from external power supplies, creating an increasingly significant power generation and distribution problem (both on chip and off-chip) with each new technology generation [2-5]. Energy efficient, low noise power delivery has become increasingly challenging with the advancement of integrated circuit technologies

In isolated topologies current transitions are typically much slower. The reason is that isolation power transformer introduces additional loop inductance (leakage inductance) [6]. There are two types of the isolated converter of which main switch uses only a single one : one is a forward type which transfers power when a switch is turned on, and the other is a flyback type which transfers power when a switch is turned off. The isolated dc-dc converter is more efficient than non-isolated converter because of most applications require the isolation between the input and the output. Therefore, if possible, it is desirable to make the dc-dc converter in the form of an isolated type. However, the efficiency of isolated dc-dc converters is limited because isolated dc-dc converters can transfer energy of a primary circuit to a secondary circuit only when a switch is turned on or off [7].

Ever increasing demands for processing power has seen companies such as Intel and AMD relentlessly self-obsolete themselves with faster and more powerful processor chips. These advances have, in general, been made through increases in the density of transistors that can be fabricated on a given area of silicon. Current requirements for processors have

increased exponentially over the last 4-5 years and will soon be exceeding 100 A in a number of processor applications [8].

In the past four decades, the Moore's law, which states "transistor density doubles every eighteen months", has successfully predicted the evolution of microprocessors. Currently, the latest processors from Intel consist of hundreds of millions of transistors. It is predicted that in 2015, there will be tens of billions of transistors in a single chip [9].

New power management technologies for the transistors in the microprocessor have been introduced in the past decade. One of the solutions is to decrease the microprocessor supply voltage. Starting with the Intel Pentium processor, microprocessors are using a non-standard power supply of less than 5 V, and the supply voltages have been and will continuously decrease. On the other hand, the increasing number of transistors in the microprocessors results in continuous increase of the microprocessor current demands. Fig. 1.1 shows how quantity of transistors increases with year to year to fulfill the different microprocessors demand. Moreover, due to the high computing speed, the microprocessors' load transition speeds also increase. The low voltage, high current, fast load transition speed, and tight voltage regulation impose challenges on the power supplies of the microprocessors. Fig. 1.2 shows the variation of voltage and current according to the demand from the recent Intel processors.

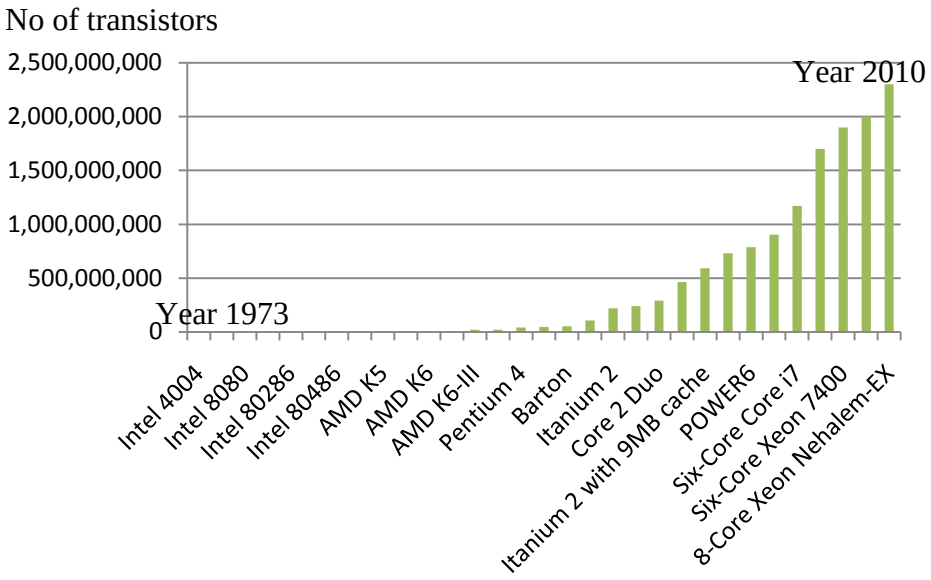


Fig. 1.1 The number of transistors integrated on the CPU die for Intel processors.

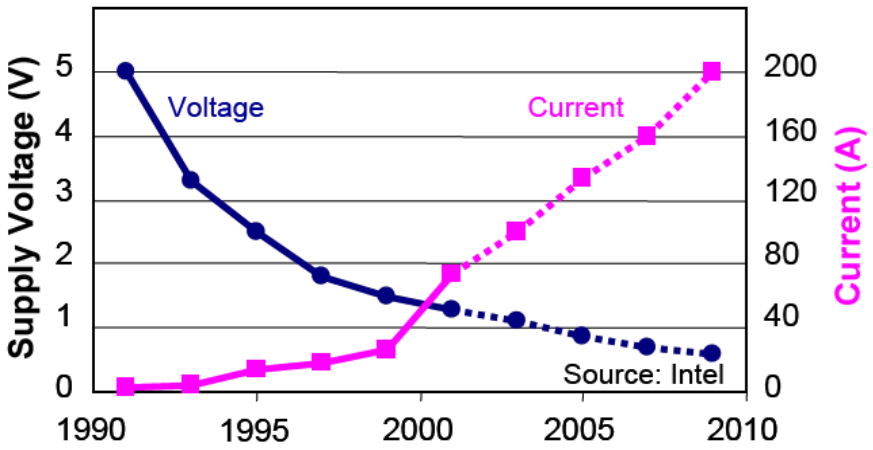


Fig. 1.2 Intel's roadmap for the processor's required voltage and current

1.2 Duty cycle and its effect on performance of converter

To meet fast development of information technology, power conversion equipment employed in computer and telecom power systems must face lot of challenges such as: lower supply voltage, larger current, higher efficiency and faster transient response. Generally, extremely narrow duty cycle is used to convert a higher input voltage to lower output voltage, for example, convert 48 V or 12 V to 1 V or below 1 V. However, extremely narrow duty cycle will seriously influence converter performance, lead to conversion efficiency down and on-time period exceed limitation of the control circuit. To eliminate these drawbacks,

transformer based converter, two stage converter, tapped-inductor converter are proposed to extent duty cycle and provide high step down conversion [10-18], but these proposed topologies bring other new problems such as cost, complex control circuit, large size and leakage-energy reset, etc.

The extreme duty cycle increases switching loss and reverse recovery loss, which are frequency-related and increase greatly when VRs work with high switching frequency; therefore VRs suffer low efficiency. Since the extreme duty cycle is the fundamental limitation of current buck VRs, it is a natural requirement to extend the duty cycle. However, for buck VRs, the duty cycle is equal to voltage gain, it cannot be extended. To extend the duty cycle, the buck converter needs to be modified. The extreme duty cycle is the elemental limitation for increasing efficiency. Using the transformer concept to extend the duty cycle is a good approach to improve the VR efficiency [19].

Concept of extended duty cycle can be expressed from the simple example. A transformer is introduced between top switch and load in a conventional converter shown in Fig. 1.3 (a). An additional design variable - the turn's ratio n, which allows one to modify the duty cycle. Fig. 1.3 (b) and (c) show the waveforms of the top switch current i_{top} and the phase voltage v_{phase} before and after the duty cycle is extended. When the duty cycle is extended, to deliver the same amount of average input current i_{top} waveform is fatter and shorter; therefore the turn-off value is much lower. This reduces the top switch turn-off loss. To get the same V_o, which is the average value of v_{phase}, v_{phase} waveform is also fatter and shorter with an extended duty cycle. This reduces the bottom switch reverse-recovery loss.

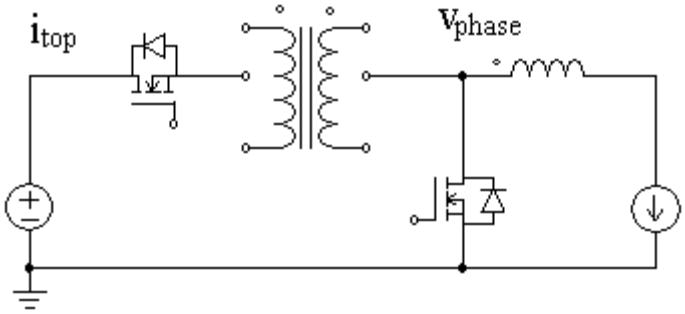


Fig. 1.3 (a) Conventional converter using transformer concept to extend duty cycle

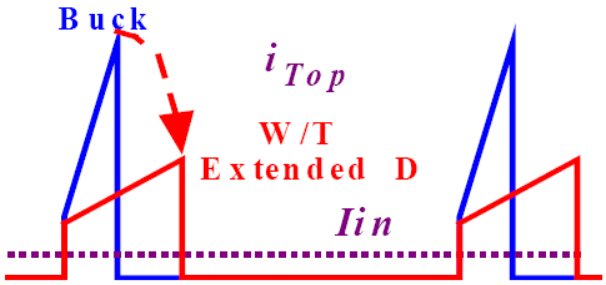


Fig. 1.3 (b) Extending duty cycle reduces top switch turn-off current

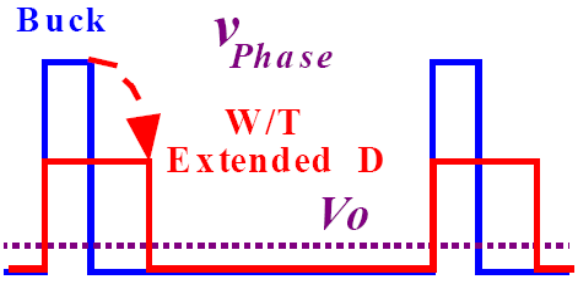


Fig. 1.3 (c) Extending duty cycle reduces the phase voltage.

The tapped-inductor buck converter [20] is the simplest implementation of the transformer concept to extend the duty cycle. Although the tapped-inductor buck converter itself is not a successful solution, it does verify that extending the duty cycle helps to increase efficiency. The efficiency curves in Fig. 1.4 shows a promising trend that converters with extended duty cycle can improve efficiency. The tapped-inductor buck converter is the simplest implementation, but cannot accomplish the job. Its failure unveils one important issue: the transformer leakage inductance. When a transformer is used to extend the duty cycle, the energy stored in the leakage inductor needs to be handled properly; otherwise it may be detrimental.

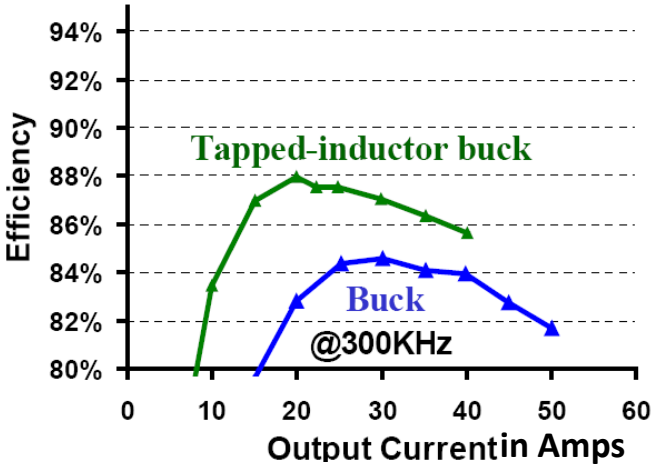


Fig. 1.4 Measured efficiency of the tapped-inductor buck VR

1.2.1. *Dead time* and its effect

Extreme duty cycle also affect the operation of MOSFET switches used in converter. Insufficient dead-time will result in shoot-through current via the high side (HS) and low side (LS) switches, while excessively long *dead time* will result in unwanted body-diode conduction loss and reverse recovery loss in the LS power MOSFET. Therefore *dead time* should be optimized so that overall efficiency can be improved.

The autonomy of battery-operated electronic systems directly depends on the energy conversion efficiency from the battery to the lower voltage levels required by CMOS technologies in recent years. The work presented in reference [21] focuses on optimizing buck converter efficiency (synchronous rectification) by minimizing body-diode conduction losses.

Because of significantly lower conduction losses, synchronous rectifiers are now used in essentially all low-voltage dc power supplies including converters for battery-operated electronics, point-of-load converters, microprocessor power supplies, etc. It is well known that optimum utilization of a synchronous rectifier depends on the ability to adjust the commutation *dead times*. Too long *dead times* result in additional losses due to the body

diode conduction and the body-diode reverse recovery [22]. The *dead times* are adjusted adaptively to minimize the duty-cycle command, which results in maximization of the converter efficiency [23].

The synchronous Buck converter is the most popular topology for low voltage dc-dc conversion [24-27], such as point-of-load and voltage regulator modules (VRMs). To prevent both upper and lower MOSFETs from conducting simultaneously, i.e., shoot-through, a *dead time* interval is inserted between their gate drive signals. During the *dead time* interval, both upper and lower MOSFETs are OFF, and the inductor current flows through MOSFET body diodes. Due to the higher voltage drop across the body diode, the driver *dead time* will reduce the conversion efficiency of the voltage regulator [26-27]. Many schemes, including adaptive *dead time* control, are commonly implemented to keep the *dead time* as short as possible [27-29] to improve efficiency.

Driver *dead time* control is a popular scheme used to prevent the occurrence of the shoot-through issue in a synchronous buck voltage regulator. As the switching frequency is continually increasing in today's converter design, the *dead time* interval is now long enough relative to the switching period to influence the system performance. In addition to its impact on efficiency, driver dead time also affect loop gain and system stability, especially under the critical load condition [29].

Generally speaking, the efficiency of a switch mode converter is mainly restricted by conduction loss, switching loss, and shoot through current loss [30]. The first two terms can be minimized by reducing the sizes of power MOSFETs and their drivers [31]. To eliminate the last term, a long *dead time*, normally 30 ns for a maximum load of 1 A [32], is required to account for process and temperature variations, which deteriorates the efficiency owing to body diode conduction of the power n-MOSFET. Various *dead time* adjusting techniques have been reported [33–35].

A dynamic *dead time* controller based on a novel *dead time* detector for synchronous buck dc-dc converters is proposed in reference [36]. With this controller, the *dead time* of power converters can be dynamically optimized under any load condition. But this method increases complexity of the converter.

Due to the finite turn-on and turn-off delays of power MOSFETs, *dead time* is required to eliminate the conduction loss arise from the simultaneous conduction of the HS and LS switches. The length of the *dead time* affects the power conversion efficiency in a significant way. The reference [37] introduces a novel one-step digital control technique that can dynamically optimize the *dead time* for the turn-on and turn-off of the power MOSFETs in dc-dc converters. This one-step *dead time* correction can improve the converter's efficiency by 2 to 4% as shown in Fig. 1.5 and Fig. 1.6, depending on output current, output voltage and switching frequency.

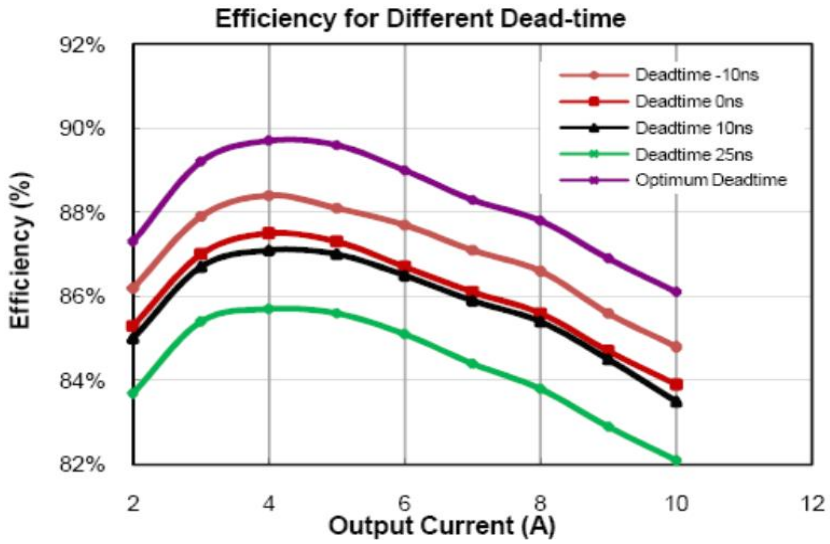


Fig. 1.5 Power conversion efficiency comparisons for various dead-times

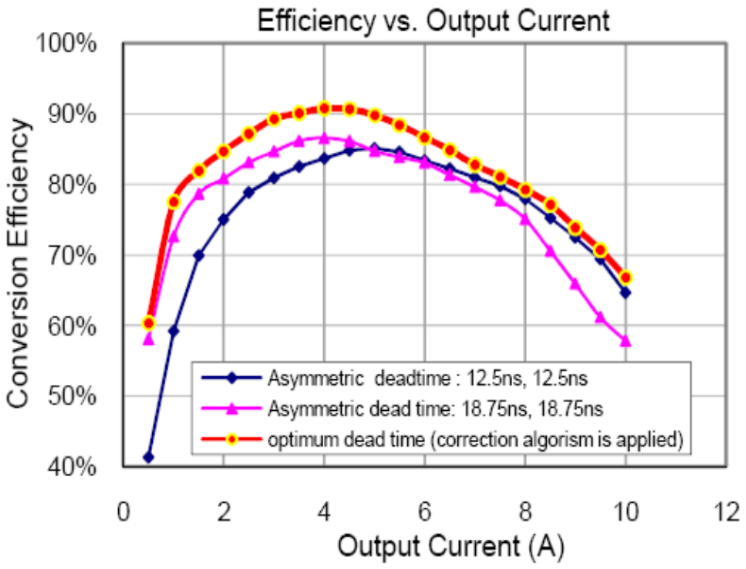


Fig. 1.6 Power conversion efficiency is increased by 2% to 4% compared with non-optimum dead-times case.

1.3 Losses in converter

A good understanding of power loss in a high frequency synchronous buck converter is important for designing optimization of both power MOSFET and circuit itself. MOSFET power losses are divided into conduction loss and switching loss. Conduction loss is due to the current square times any resistance in the loop. On the other hand, switching loss is due to the overlapping between the current and voltage of each MOSFET. This was approximated as the half the drain voltage times the inductor current over the switching time (fall and rise time) [38-40]. Other losses are loss due to the output capacitance C_{oss}, body diode conduction loss, control circuit, and gate drive loss. The output capacitance C_{oss} is composed on the drain-source and drain-gate capacitors and its value can be easily extracted from any vender's datasheet. Loss due to C_{oss} is considered as half C_{oss} times the square of the input voltage times the switching frequency [41-45]. The losses in each component can be calculated, so that those can be eliminated or minimized to improve overall efficiency. With the use of synchronous rectifier, conduction loss is reduced substantially, but it generates extra

switching losses. This effect can be minimized by using resonant tank in the converter. In this way converter will be modified to quasi-resonant, resonant or/and ZVT converter.

A new analysis based on basic energy concept is introduced to calculate the contribution of loss due to the output capacitor C_{oss} [46-48]. The relation between C_{oss} and switching loss is found a combined ratio that cannot be separated into these two basic terms; overlapping VI loss and C_{oss} loss. Results show that the switching loss can remain the same as the total of switching and C_{oss} losses $0.5 \cdot I_L \cdot V_D \cdot (T_{fall} + T_{rise})$, [45]. On the other hand, the effect of C_{oss} is indirect and it affects the rise and fall time period, which in their turn affects the switching loss.

For the design of a high efficient power supply using SR, it is necessary to exactly know where the power losses in the SR MOSFET occur. In the following discussions all important sources of power losses are identified, based on ideal MOSFET switching behavior. Conduction losses are defined by the R_{dson} of the MOSFET. The calculation can be done with the following formula:

$$P_c = I_{rms}^2 R_{dson} \tag{1.1}$$

here I_{rms} is the triangular current through the MOSFET, not the output current of the converter [18].

A certain *dead time* has to be guaranteed for assuring an interlock between the two SR MOSFETs to avoid a current shoot through,. Therefore, the respective MOSFET has to be switched off before the primary side is turned on. This causes the current to commutate from the MOSFET channel to the MOSFET body diode, which can be seen in Fig. 1.7, when a negative voltage drop occurs over the drain source. The time is called body diode on time t_D. The calculation of the diode power loss can be achieved by using following parameters: the forward voltage drops of the body diode, the source to drain body diode current I_{SD}, the body diode on time t_D and the converter switching frequency f_{SW}:

$$P_{BD} = V_D I_{SD} t_D f_{SW} \tag{1.2}$$

Gate drive losses of the SR MOSFET are defined by the gate charge Q_g, the gate driving voltage V_g and the switching frequency f_{SW} as

$$P_g = Q_g V_g f_{SW} \tag{1.3}$$

The output charge Q_{oss} and the reverse recovery charge Q_{rr} also produce losses while turning off the SR MOSFET. The switching off loss can be defined as

$$P_s = V_T \left(\frac{1}{2} Q_{oss} + Q_{rr} \right) f_{SW}, \tag{1.4}$$

where V_T is any instantaneous voltage of the MOSFET.

The loss in the synchronous rectifier can be expressed as [1]:

$$P_{sr} = P_c + P_s + P_g + P_{BD} \tag{1.5}$$

where P_c is the conduction loss, P_s is the switching loss, P_g is the gate drive loss, and P_{BD} is the body diode loss. In (1.5), only P_{BD} is a function of the dead time. Since our goal is to determine the effect of "dead time" delays on the efficiency of a synchronous buck converter, we will concentrate on this loss component. In every switching period, there are two dead time intervals, t_{d1} and t_{d2}. The first interval, t_{d1}, occurs at t_1 when the SR turns off. Since the SR is a bi-directional switch, the inductor current at t_1 can be either positive or negative.

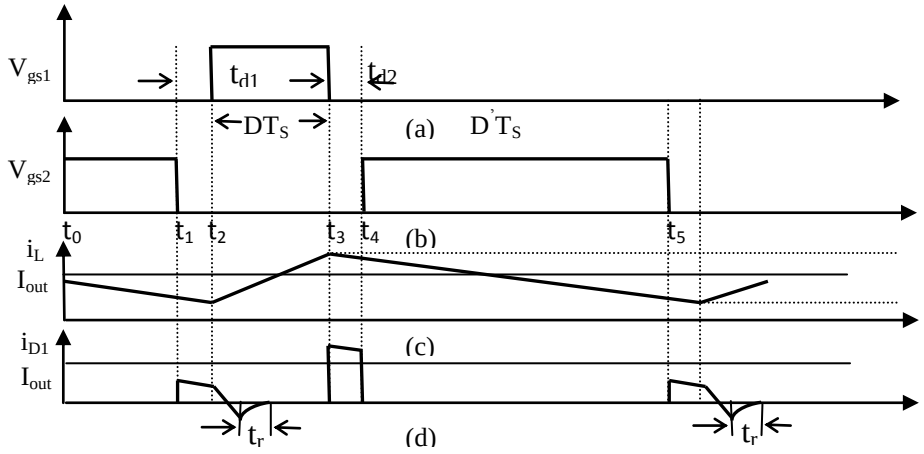


Fig. 1.7 Synchronous buck converter waveforms: a) gate drive signal for Q_1, b) gate drive signal for Q_2, c) inductor current in mode 1, d) SR body diode current in mode l.

If $I_{out} \geq \frac{\Delta I_L}{2}$ the inductor current at t_1 will be positive and the diode will turn on to provide a return path for the inductor current. If, on the other hand, $I_{out} \leq \frac{\Delta I_L}{2}$ the inductor current at t_1 will be negative and the diode will not turn on. Instead, the inductor current will charge and discharge the drain to source capacitance of the SR and the main switch, respectively, until the main switch turns on at t_2. The second dead time interval, t_{d2}, occurs at a time t_3. At t_3, the main switch turns off and allows the diode D_2 (the body diode of the SR or an external Schottky diode) to conduct until the SR turns on at t_4.

The SR body diode will produce losses during the two dead time intervals, t_{d1} and t_{d2}. Therefore, we can express P_{BD} as: $P_{BD} = P_{td1} + P_{td2}$ (1.6)

where P_{tdI} is the total body diode loss during t_{d1}, and P_{td2} is the total body diode loss during t_{d2}. At $t = t_1$, the SR is turned off and the SR body diode D_2 turns on to provide a return path for the inductor current . When Q_1 turns on at t_2, the forward biased body diode sees a reverse voltage equal to the input voltage. Since the SR body diode is a regular p-n diode, it cannot turn off instantaneously due to the stored minority carrier charge. The reverse recovery current spike caused by the removal of the stored charge can be quite large. It can, therefore, be a source of a significant additional loss in both the SR and the main switch. Thus, P_{td1} , is given by:

$$P_{td1} = P_{cdl} + P_{rr} \quad (1.7)$$

Where P_{cdl} is the body diode conduction loss during t_{d1}, and P_{rr} is the loss caused by the body diode reverse recovery at the end of t_{d1}. After the SR turns off at t_1, the body diode will conduct for a time t_{d1} before the main switch turns on at t_2. During this time, the diode conducts the full inductor current equal to $I_{out} - \frac{\Delta I_L}{2}$. Hence, the body diode conduction loss can be expressed as:

$$P_{cdl} = V_f \cdot \left(I_{out} - \frac{\Delta I_L}{2} \right) \cdot t_{d1} \cdot f_{sw} \tag{1.8}$$

where V_f is the diode forward voltage drop, ΔI_L is the inductor current ripple, and f_{SW} is the switching frequency. Clearly, in order to minimize P_{cd1}, we must minimize t_{d1}. The next step is to determine the impact of P_{cdl} on the overall converter efficiency. Therefore, we will define the efficiency degradation due to the body diode conduction during t_{d1} , $\Delta\eta_{cdl}$, in the following way:

$$\Delta\eta_{cdl} = \frac{P_{cdl}}{P_{in}} \tag{1.9}$$

where P_{in} is the input power of the converter.

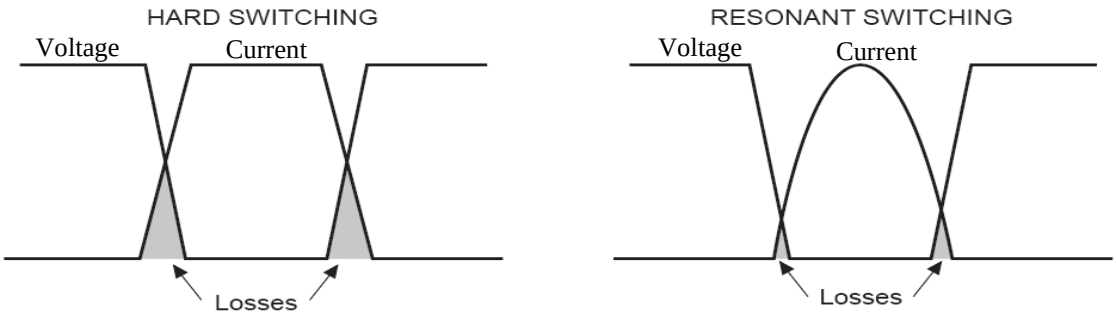


Fig. 1.8 Unavoidable switching losses conventional converter and resonant converter

Overall efficiency can be improved by reducing the unavoidable losses as shown in Fig. 1.8, with application of soft switching techniques in power converter. With high switching frequency operation, the switching loss and gate drive loss are both increased [49]. When switching frequency becomes very high, significant compromise has to be made between conduction loss and frequency related losses, such as switching loss and gate drive loss. Several converter topologies proposed in the past for improving the efficiency [50-54].

1.4 Converter Topologies

Research is still going on to introduce new converter topologies, in recent times converters with quasi-resonant, resonant and ZVT techniques are used [55]. Each technique has its own importance according to their applications. Table 1.1 gives comparison details among quasi-resonant, resonant and ZVT techniques.

Table 1.1 Comparisons among different switching techniques

Switching Techniques	Benefits	Drawbacks	Optimal working conditions
Quasi-resonant	Low switching stress	Provide discontinuous current	Variable frequency and discontinuous resonance
Resonant	Can operate at zero current and zero-voltage to reduce component stresses	Higher peak current, greater complexity	• Suitable for low and medium frequency upto 100 kHz • High voltage converter
Zero-Voltage-Transition (ZVT)	Can operate at high frequency with minimized parasitic effects	Losses due to Cdv/dt across gate	• During turn-on and turn-off it operates as resonant converter and for rest of the time as conventional PWM • Suitable for low power application

In a resonant switch converter, the switch network of a PWM converter is replaced by a switch network containing resonant elements. The resulting hybrid converter combines the properties of the resonant switch network and the parent PWM converter.

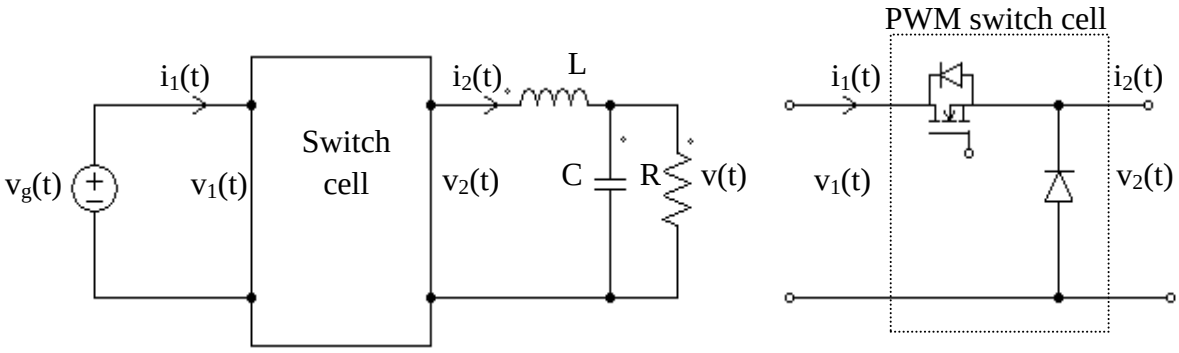


Fig. 1.9 (a) Conventional PWM switch cell

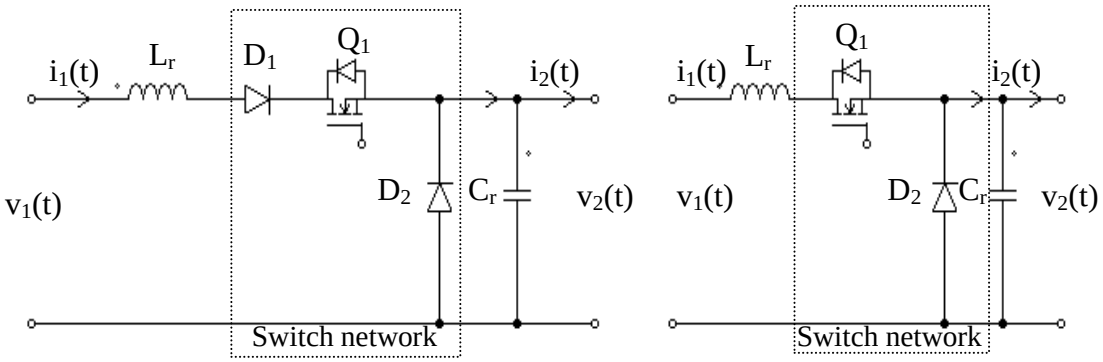


Fig. 1.9 (b) Half-wave ZCS quasi-resonant switch cell and Full-wave ZCS quasi-resonant switch cell

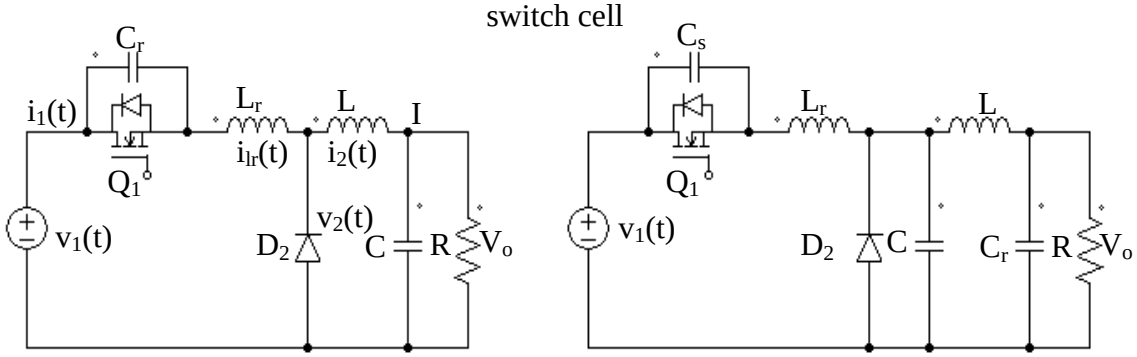


Fig. 1.9 (c) ZVS quasi-resonant switch cell and ZVS multi-resonant switch cell

Combination of L_r and C_r provides resonant condition to PWM converter to achieve zero-voltage-switching (ZVS) and zero-current-switching (ZCS). In the zero-current-switching quasi-resonant switch, diode D_2 operates with zero-voltage switching, while transistor Q_1 and diode D_1 operate with zero-current switching. When diode D_1 is in series with the MOSFET, it gives a half-wave ZCS quasi-resonant and antiparallel diode D_1 across the MOSFET gives a full-wave quasi-resonant switch cell. An inductor in series with the MOSFET gives a ZCS and a capacitor in parallel with switch gives ZVS operations. If a

resonant tank consists of more than one inductor or capacitor then it is called a multi-resonant converter. With the combination of different location of resonant elements, other resonant converter topologies can be designed are shown in Fig. 1.9 (a-c). In specialized applications, resonant networks may be unavoidable, e.g., high voltage converters, where significant transformer leakage inductance and winding capacitance leads to a resonant network. The performance can be increased at one operating point, but not with a wide range of input voltages and load power variations. Significant currents may circulate through the tank elements, even when the load is disconnected, leading to poor efficiency at light load. Quasi-sinusoidal waveforms exhibit higher peak values than equivalent rectangular waveforms. These considerations lead to increase conduction losses, which can offset the reduction in switching losses. Resonant converters are usually controlled by variation of switching frequency. In some schemes, the range of switching frequencies can be very large. However, these converters exhibit reduced efficiency at light load, due to the large circulating currents. In addition, significant switching loss is incurred due to the recovered charge of diode D_1 [56]. The main advantages of resonant converters are: reduced switching losses, voltage stress, and EMI. Turn-on or turn-off transitions of semiconductor devices can occur at zero crossings of tank voltage or current waveforms, thereby reducing or eliminating some of the switching loss. Hence, resonant converters can operate at higher switching frequencies as compared to PWM converters. Resonant converter produces voltage stress over switches which result in conduction loss; this can be overcome by ZVT technique. Produced voltage and current stress is minimized in ZVT converter. For 10% to 100% load range in resonant converter, the peak voltage stress of the power switch can be 11 times the input voltage [57].

The synchronous rectifier buck converter (SRBC) is popular for low-voltage power conversion because of its high efficiency and reduced area consumption [58-59]. This topology uses complementary switches to transfer the energy to the filter inductance from the

power source. High switching frequencies are preferred in order to reduce the size of the off-chip LC filter components. Unfortunately, high switching speeds exacerbate frequency-dependent losses; especially as the load current is reduced, resulting in a substantial reduction in converter efficiency. Many techniques have been developed in an attempt to mitigate this effect. Included among these are; resonant gate drive [60–62], pulse frequency modulation (PFM) [63], and a hybrid control scheme [64], whereby at heavy loads the converter operates in standard PWM condition, but at light loads they switches to PFM mode. The primary drawbacks of these methods are the complexity of their implementation and, in the case of the variable-frequency methods, their potential for generating undesired noise at sub-harmonics of the switching frequency. In many systems, especially those for audio applications, sub-harmonic noise can result in severe degradation of the signal quality. Furthermore, hybrid controllers can provoke relatively large output voltage transients when switching between PWM and PFM control modes [65].

One of the drawbacks of synchronous buck converter is the induced term $C\,dv/dt$ switching losses of MOSFETs used as synchronous rectifiers [66–68]. The induced $C\,dv/dt$ turn on of the synchronous MOSFET can happen after its body diode recovers. The increased voltage across the synchronous MOSFET induces a current to charge the gate through the gate-to-drain capacitor. The induced voltage can possibly invert (turn-on) the synchronous MOSFET channel for a short time period. The overlapping of the V_{ds} voltage and the current generates additional switching losses.

Unfortunately, $C\,dv/dt$ induced voltage in the synchronous buck circuit might cause undesired turn-on of SR MOSFET and deteriorate overall system efficiency. The $C\,dv/dt$ induced turn-on problem is caused by a fast changing voltage on the drain side of SR MOSFET, which results from turning on the control main MOSFET. If this induced gate voltage exceeds the threshold voltage of SR MOSFET; it will be spuriously turned on while

main MOSFET is on. As a result, a shoot-through current will flow from the input voltage bus to the circuit common through the main MOSFET and the SR MOSFET [69].

As non-isolated synchronous buck power converters continue pursuing higher switching frequencies, the key limiting factor has become switching losses in the high-side MOSFET. Fig. 1.10 shows turn-on of the high-side MOSFET (not shown) produces a voltage transient dv/dt across the low-side (synchronous) MOSFET, which leads to the off-state current conduction shown here. However, when the applied dv/dt results in a gate voltage that exceeds the MOSFET gate-to-source threshold voltage, the converter's reliability and overall efficiency suffer [66].

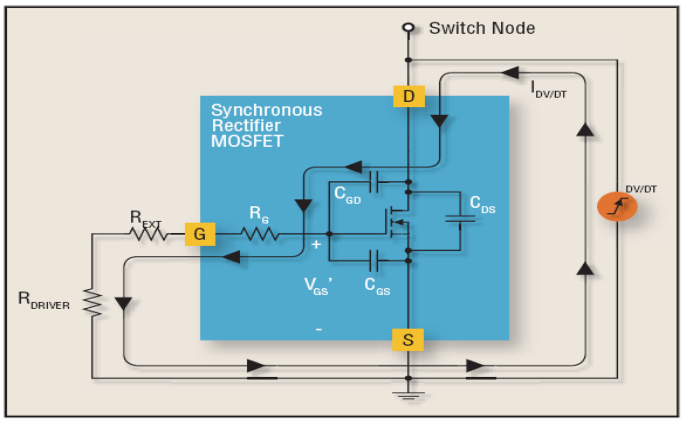


Fig. 1.10 Turn-on of the high-side MOSFET (not shown) produces a voltage transient dv/dt across the low-side (synchronous) MOSFET, which leads to the off-state current conduction shown here.

The dv/dt effects can be minimized by following certain methods such as: a low side MOSFET chosen with a $Q_{GD}/Q_{GS(TH)}$ ratio less than unity, a combination of a MOS/bipolar-MOSFET drive stage with minimum pull-down resistance that can be selected for low-side MOSFET [66].

ZVT is normally a fixed frequency switching PWM, with rise and fall times controlled by LC networks to allow the switches to change state with zero volts across them. ZVS is normally a variable frequency techniques in which one state controls the input energy charging and the other state controls the transfer energy from the resonant element to the

load. In ZVT, only during turn on and turn off, resonance is provided and for the rest of the period it behaves as a PWM converter. In this manner, switching loss and parasitic effects are minimized and component stress is also reduced. The power switches in the ZVT topologies commutate under zero-voltage-switching with the help of resonant snubber cells during a short ZVT time. Circuit operations are identical to common PWM topologies during the rest of the period. For this purpose an auxiliary switch with resonant elements are connected across the main switch to provide resonant conditions during the commutation interval. Before switching on the main switch, the auxiliary switch is to be turned on under soft switch conditions. Many topologies have been designed since last few years to achieve ZVT in power converters [70-74].

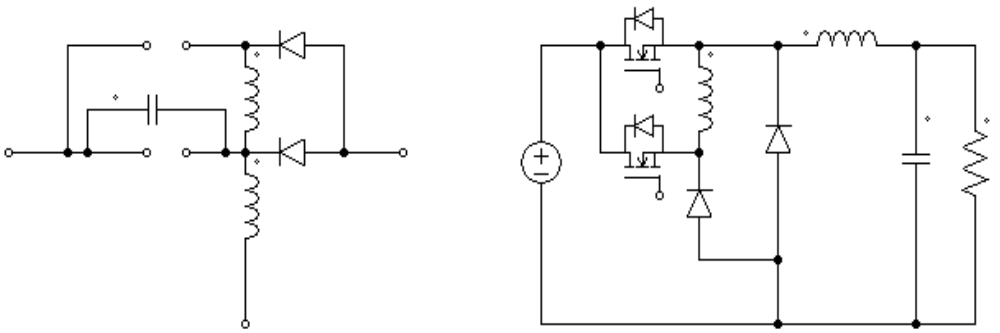


Fig. 1.11 (a) ZVT topologies for reduced switching losses.

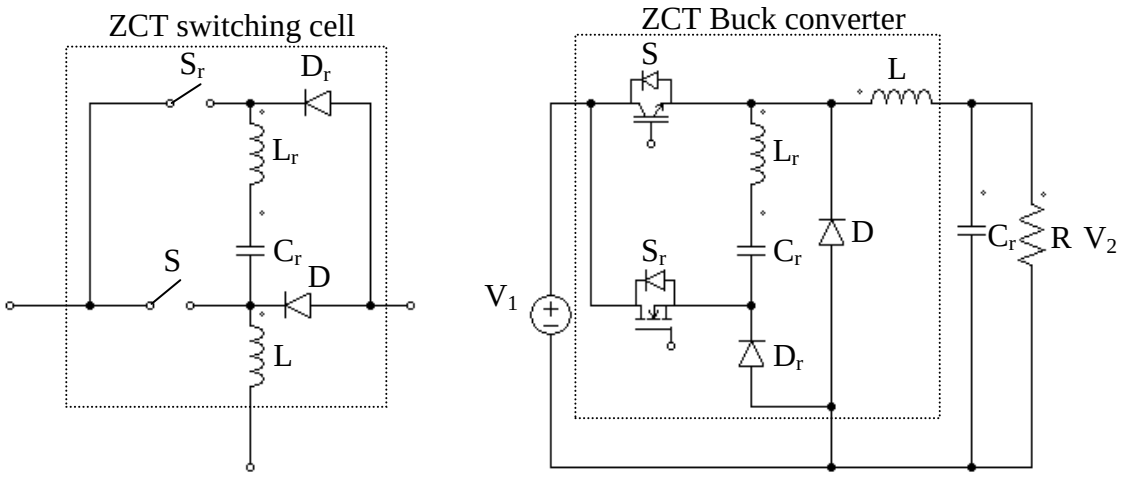


Fig. 1.11 (b) ZCT topologies for reduced switching losses.

Better characteristics are obtained in ZVT topologies, at the expense of increased complexity. Here, to achieve ZVS, switch voltage and current waveforms are changed only during commutation intervals, the behavior of the ZVT converter being otherwise identical to the one hard-switching converter. In converter topologies having only one active switch, the ZVT technique is implemented with an auxiliary circuit, which consists of an additional active switch, an auxiliary inductor, for the resonant process that discharges the drain-source capacitance of the switch and for limiting the rate of change of the diode current at turn-off, as well as a few other passive components. Some topologies with ZVT and ZCT techniques used to reduced switching as well as conduction loss is shown in Fig. 1.8 [75].

Zero Current Transition (ZCT) topologies, working on similar principles as the ZVT topologies, have been proposed as well [75]. The auxiliary switch is turned on prior to turning off the main switch, and it initiates a resonant process that shapes current to ensure zero current through S during switching. In this way, the main switch can be turned off with zero current.

To facilitate ZVS while preserving the advantages of the PWM technique, hybrid topologies incorporate PWM technique and resonant converters in order to minimize circulating energy and corresponding conduction loss and switching loss. Adding an auxiliary switch across the resonant converter in a ZVS–QRC derives ZVS-PWM converter, which can be considered as hybrid circuits of ZVS–QRCs and PWM converters [76], wherein ZVS is achieved for the power switch and the converter operates at a constant switching frequency. However, the power switch suffers from a high voltage stress that is proportional to the load range. Compared with ZVS–PWM converter, ZVT–PWM converters [77-78] are more desirable since soft switching is achieved without increasing switch voltage and current stress. By adding an auxiliary shunt network to discharge switch junction capacitance and

shift the rectifier diode current, ZVS is achieved for the switch and reverse recovery of rectifier diode is attenuated.

1.5 Motivation

The tremendous requirements of power converters for portable electronic equipment under different power ratings poses stiff challenges to power supply designers. Lower operating voltages, increased current requirements, and the dynamics of microprocessor-based or microcontroller-based systems create new demands on power distribution and management. The issues such as high efficiency, high power density, and proper voltage regulation etc. become critical if buck converters are considered for low operating voltage. The conversion of electrical energy from one form to another with low cost and increased efficiency has been made possible due to advances in power electronic converter design and control methods. But a compromise is to be formed in some extends with size, weight, cost and power density, etc. in today's power electronic apparatus. The cost, size and performance advantages have promoted power electronic applications extensively in industrial, commercial, residential, transportation, utility, aerospace, and military environments in recent years. According to Moore's law, the number of transistors on an IC has doubled every year. To achieve high power density with the high rate of increase in the number of transistors, demand increased switching frequency. But high switching frequency introduces switching losses.

Extreme step down voltage in telecom power systems lead to a low duty cycle. But low duty cycle compels to go for high switching frequency, which will amplify the switching losses as well as affect the dead time between switches. Another basic requirement from telecom power systems is to provide a galvanic isolation to satisfy the safety standards and to achieve a flexible system reconfiguration. These requirements can be fulfilled by high step-down isolated buck converters. Research is still required to achieve better efficiency, high

power density in previous proposed power supply, which motivates to improve performance of high step down isolated buck converter. A simple clamp capacitor scheme is employed with the proposed converter to reduce the switching loss and body diode loss. At the same time, the duty cycle is extended by varying the turn ratio of the transformer to improve the performance of the converter.

Increased popularity of low power portable equipment claims for high power density and efficiency converter. Power density will be improved by reduction of losses and size of components. Size reduction can be done up to certain extend depending upon the operating switching frequency of the converter. So minimization of losses will improve the power density and efficiency of the converter. Several topologies have been proposed in the past few years such as: quasi-resonant converter, resonant converter and ZVT-PWM converter; to reduce losses. But resonant converters suffer from the disadvantage of high voltage and current peaks. This in-turn causes the device ratings to be much higher than the hard-switched counterparts. ZVT buck converters become popular as they provide reduced voltage and current stresses. Increased efficiency can be achieved by utilizing proper converters that can reduce conduction and switching losses. Recent demands of high efficiency, high power density, low cost power supply for portable equipment motivates to design ZVT synchronous buck converters with active and passive auxiliary circuits at different conditions. These converters can achieve high efficiency by reducing losses. They reduce voltage and current stresses, which lead to low cost and low power ratings components.

Microprocessors and DSPs are widely used in many commercial and industrial applications. Power supplies for these processors have been improved from clock frequency, integration and applicability point of views. However to meet these improvements, the operation voltage must to be reduced without reducing the power consumption, while maintaining a high operating switching frequency. These requirements can be accomplished

with the use of multiphase buck converter. An increased number of components and switches lead to a low efficiency. Reducing of switching losses in multiphase buck converter to achieve high efficiency is now a big challenge. These requirements motivate to implement soft switching techniques in multiphase synchronous buck converter to achieve a high power density with an improved efficiency.

1.6 Objectives:

From the preceding discussion, the dissertation objectives may streamline as follows:

- To develop an isolated buck converter topology for telecom application that can extend duty cycle by optimizing *dead time* and the turns ratio of transformer. This would facilitate the reduction of current ripples and to decrease the size of the filter components. A simple soft switching technique, using clamped capacitors, is employed to this topology for further improvement in power density and efficiency. With this simple scheme, *dead time* is controlled to further increase the efficiency by reducing the body diode loss and at the same time it avoids the shoot through conditions in our proposed topology.
- To implement soft switching techniques in synchronous buck converter topology employing an active auxiliary circuit and a passive snubber circuit. This proposed topology will improve power density and efficiency for low power portable applications. Another main objective is to reduce the voltage and current stresses employing these auxiliary circuits. The proposed converters can achieve better efficiency at a wide load range, whereas the simple passive snubber circuit provides high efficiency, high power density at high switching frequency.

- To develop multiphase SBC for new generation microprocessors and DSPs power supply at low output voltage; 1 to 1.5 V and high load current; 1 to 140 A with reduced switching losses, reduced voltage and current stresses.

1.7 The work of this Dissertation:

Chapter I introduces the background of this work. It first discusses the requirement of buck converters in recent years. Then developing trends in converters are presented according to the demand. Finally motivation factors and objectives are discussed.

To fulfill the power requirements for telecom system, an isolated topology with *dead time* and duty cycle control is presented in Chapter II. A simple clamp capacitor scheme is employed in the isolated topology to reduce switching losses as well as to reduce voltage stresses across switches. The clamp capacitor minimizes *dead time* between switches to reduce the body diode conduction losses. By varying the turn ratio of transformer, the duty cycle is extended to reduce switching losses. The complete analysis of extend duty cycle and *dead time* control are presented. The hardware prototype of the proposed converter is developed in laboratory with the designed parameter. Detail design considerations are presented in this chapter. The discussed features to improve performance of the proposed isolated buck converter are verified with simulation and experimental results.

Chapter III introduces the implementation of ZVT technique in synchronous buck converter to achieve high efficiency at low voltages typically required for portable application. An active auxiliary circuit that allows the main switch to operate with zero-voltage switching has been incorporated in the conventional PWM synchronous buck converter. The operation principles and a detailed steady-state analysis of the ZVT-PWM synchronous are presented. Design considerations of the proposed converter are discussed and it has been built in a laboratory with the calculated parameters. The performance of the proposed converter is verified with simulation and experimental results.

To overcome the drawbacks of active auxiliary circuit such as the excess switching losses, the low operating frequency range, and its complex nature, active auxiliary circuit is replaced by a passive snubber circuit. In chapter IV, a simple passive snubber ZVT synchronous buck converter is discussed. The proposed converter with a detailed steady state analysis is presented. The proposed converter has been designed and fabricated in an laboratory. Its capabilities to improve the performance of converter are verified by simulation and experimental results.

In the present scenario with a increased demand of microprocessor based products, dc-dc buck converters are designed for low voltage and high current applications. The multiphase buck converter is the best substitute over all possible topologies. The increase number of switches in multiphase converter intensifies switching losses. Therefore a soft switching technique is implemented for multiphase buck converter with an auxiliary circuit to reduced switching losses. A detail steady-state analysis of the proposed multiphase converter is proposed in chapter V. Design procedures for successful hardware implementations are presented. The fabricated prototype is evaluated by simulation and experimental results.

The last chapter VI, is dedicated to a summary and present future works of buck converters.

CHAPTER 2

INNOVATIVE TOPOLOGICAL APPROACH TO IMPROVE PERFORMANCE OF HIGH STEP-DOWN BUCK CONVERTER

Proposed Isolated Buck Converter Topology

Duty cycle and its control

Dead time control

Operating principles and analysis

Design procedure

Simulation and Experimental Results

Summary

Chapter 2. Innovative topological approach to improve performance of high step-down buck converter

The discussion in Chapter 1 has shown that the dc-dc buck converter has gone through significant improvement to fulfill the requirement from all sectors such as industry, domestic etc. The increasing demands on portable equipment impose the researchers to design converter with stringent dynamic performance, efficiency, reliability, durability and size requirements.

Dc–dc converters with extreme step-down voltage conversion ratios are required in newly emerging power electronic applications, such as automotive power systems, telecommunication power systems, data communication systems, industrial controls, and distributed power systems. For example, the emergence of 42 V automotive power systems calls for a larger step-down converter to supply the recently developed integrated circuits (3.3 V or 1.5 V) [79-80].

The conventional buck converter has difficulty in dealing with very low voltage conversion ratios, because it would require designing the converter to operate with a very low duty-cycle (e.g. less than 10%). Such operations become objectionable since it leads to poor utilization of components as well as it degrades the system efficiency and impairs transient response [56]. A high switching frequency operation reduces the switch conduction time even shorter and gives rise to an objectionable increase in switching losses and it increases the control complexity. Thus, it does not only degrade the efficiency of the converter, but it also puts an upper-bound limit on the switching frequency. Consider, for example, that buck converter stepping a 340 V into a 3.3 V output voltage operating at 100 kHz would require a switch-on-time of 97 ns, which is below the physical limitation of some of the low cost PWM controller's minimum on-time [81].

Thus, in an effort to further decrease the voltage conversion ratio and to extend the duty-cycle range, a number of converter topologies have been proposed [81-84]. However, this scheme requires more switching devices; hence, the overall conversion efficiency of the system is reduced due to the losses in the switching devices. Alternatively, using a large step-down ratio transformer would not solve the problem. The use of a transformer increases the system cost, weight, and complexity which are not tolerable especially for applications where galvanic isolation is not required [56]. As a matter of fact, topologies based on a coupled inductor or tapped-inductor (TI) provides better performance than transformer based topologies. Moreover, it has been shown that by controlling the tapped winding ratio, the switch duty-cycle can be extended to a favorable range [20, 55, 85-89]. However, the TI topologies suffer from a voltage spike across the active switch caused by the leakage inductance between the coupled windings and the switch parasitic capacitance. Furthermore, the magnetic structure in these topologies is relatively complex and the conducted electromagnetic interference (EMI) in these topologies is also a concern. Therefore, tapped-inductor and transformer topologies are almost infeasible without utilizing soft-switching techniques which increase the circuit complexity [11-12, 16, 55, 85, 90-94].

Isolated high step-down buck converters are widely employed in telecom power systems, because the galvanic isolation is necessary to satisfy the safety standards and to achieve a flexible system reconfiguration. By varying the turn ratio of the transformer, duty cycle can be extended. An extended duty cycle reduces ripples and allows to decrease the filter component size. A clamp capacitor scheme is used in high step down isolated buck to control the dead time and switching losses. The concept of a clamp capacitor is extended to a tapped-inductor buck converter for low power and very high frequency operation.

This chapter illustrates the improvement of the overall performance of a high step-down converter. A simple and attractive solution is presented to control the duty cycle and

dead time and to improve the efficiency of the converter with soft switching in both isolated and non-isolated buck converters. Auxiliary switches are not required for this scheme. Therefore, switching losses due to auxiliary switch are not present which improves the efficiency further as compared to other converter with soft switching techniques.

An isolated dc-dc buck converter with an inherent clamp scheme is proposed. The concept of clamp capacitor scheme is extended for tapped-inductor converter. The leakage energy is absorbed and the voltage spikes on the switches are limited by the inherent clamp scheme. A prototype with 360 W rated powers has been built to verify circuit performance.

This proposed isolated converter is designed to achieve high efficiency and high power density for telecom power systems. Section 2.1 presents the topology description of the isolated converter. The relationship between turn ratio and duty cycle is established and their effects on the performance of converter are discussed in section 2.2. *Dead time* control technique using clamp capacitor scheme is presented in section 2.3. The detail analyses of different modes of operations are elaborated in section 2.4. The designed process for determining the different parameters used in the converter are expressed in section 2.5. In section 2.6, the simulated and experimental results are shown to prove all of the theoretical analysis. Finally, in section 2.7, the main features of proposed isolated converter are summarized. Concept of simple soft switching technique is extended for a tapped-inductor. The TI converter topology is described in section 2.8. The modes of operations are analyzed in section 2.9. In section 2.10, simulation results are presented to extend the verification of the concept. In section 2.11, its features are summarized.

2.1 Proposed Isolated Buck Converter Topology

The proposed converter scheme is shown in Fig. 2.1. The circuit scheme includes two MOSFET switches Q_1 and Q_2, and three clamp capacitors C_1, C_2 and C_b. The transformer T_x

denotes the combination of the magnetizing inductance L_m, the leakage inductance L_{lk} and the ideal transformer with transformer winding-ratio *n:1:1*. The proposed dc-dc converter is designed through AC link as energy transfer devices. The capacitor used in series with the transformer provides a better *dead time* control. The resonance between two capacitors in same arm of the bridge and the leakage inductance of the transformer make the switches turned on/off under ZVS. This simple configuration is easy to be controlled. With a less number of components, this converter becomes more economical and attractive as compared to other converter. In [4, 16, 95-99], different soft switching techniques are used to reduce switching losses and their operations are analyzed. However, the duration of current flowing through the body diode of MOSFET switches has not been controlled in the past work.

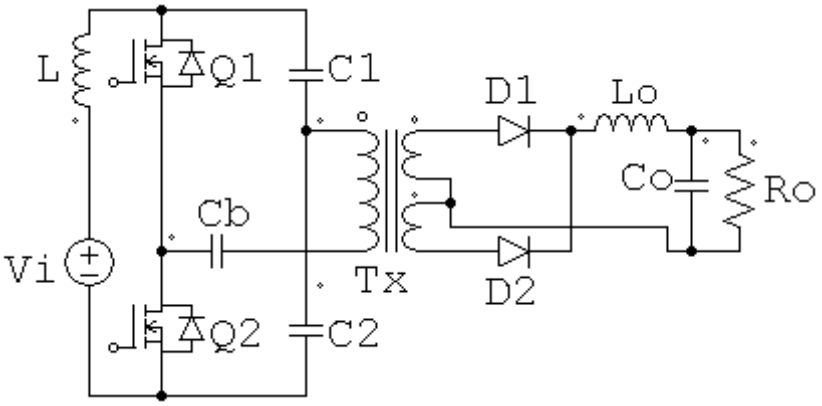


Fig. 2.1 Proposed Isolated Converter Topology.

2.2 Duty cycle and its control

A low duty cycle has an adverse effect in the performance of a converter. An extended duty cycle has several advantages such as: high efficiency, high power density, and reliability. The duty cycle can be increased with increase in turn ratio of transformer. A low duty cycle improves the durability of the system. The duty cycle cannot be reduced beyond certain limit to avoid the condition of inability to turn on the switch. So *dead time* and turn ratio controls duty cycle.

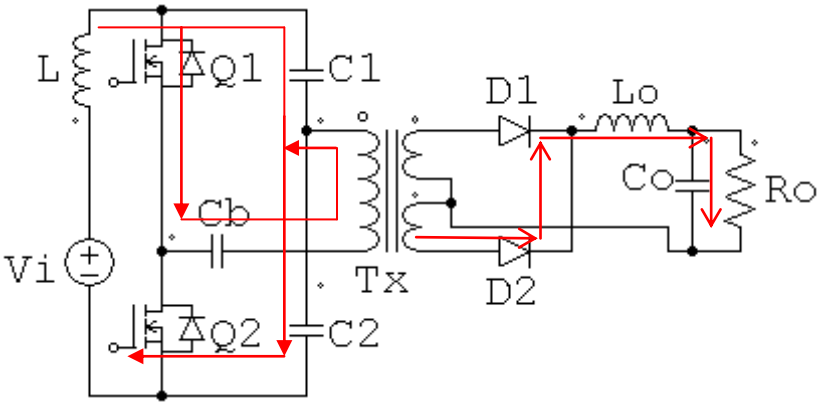


Fig. 2.2 Operation Mode 1 (t_0- t_1)

The current flow direction during T_{on} is shown in Fig. 2.2. The current flowing through a conductor can be expressed as: $I_L = \frac{\Delta V}{L}\Delta T$. This can be written as

$$\Delta I_L = \frac{V_i - (-nV_o)}{L_p} DT \text{ , for } T_{on} \text{ period} \tag{2.1}$$

The input voltage of transformer is nV_o. For having a continuous current through the transformer, the maximum current at the end of the DT period will be the initial condition of the next mode. So, the current expression for the (1-DT) period can be expressed with initial condition as

$$\Delta I = \frac{V_i + (V_i + nV_{out})DT - nV_{out}}{L_p} \text{ , for } (T\text{-}T_{on}) \text{ period} \tag{2.2}$$

If we assume that the converter operates in steady state, the energy stored in each component at the end of a commutation cycle T is equal to that at the beginning of the cycle. By equating the two equations, the relationship between the turn ratio and the duty cycle for isolated topology is

$$\frac{V_{out}}{V_{in}} = \frac{D + (D-1)(1+DT)}{n(DT-1)(1-D) - nD} \tag{2.3}$$

where, D = Duty cycle ratio, n = turn ratio of transformer, T = time period of one cycle.

For input voltage as 50 V, output voltage as 6 V and switching frequency as 100 kHz, the voltage gain or duty cycle becomes 0.12.

The duty cycle control is limited. For a duty cycle below a certain range, the switches used in the converter cannot be turned on, as turn on and turn off of switch depends on reverse recovery of switches used in converter.

For example: for V_{out} = 1.5 V, the duty cycle is 1.5/12 = 0.125 for a 12 V-input buck VR, as opposed to 0.3 for a 5 V-input buck VR. It can be seen that after the VR input voltage switches from 5 V to 12 V, the buck VR needs to work with a smaller duty cycle due to the large step-down ratio. This extreme duty cycle makes it difficult to design an efficient buck converter. For a low duty cycle, the load current will be in a discontinuous mode. So unnecessarily ripples will be produced and this will affect the performance of the converter. Thus the converter parameter has to be optimized with respect to duty cycle.

The output filter of the conventional buck converter used to get constant output current and voltage in respective of the types of load. For specific application such as in microprocessor, variations in voltage hamper processor performance. But these requirements are not fulfilled due to the limitations of the capacitor and inductor. So some ripples are associated with the output parameters. The ripple current in a buck converter switching at 100 kHz is shown in Fig. 2.3. The first parameter to be considered will be the maximum output loop inductance and the capacitor ESL as it has been traditionally ignored in the past, but it becomes critical as the physical size of converters shrink. This is not just the inductance of the capacitor (ESL) but must include inductances in the output filter of converter.

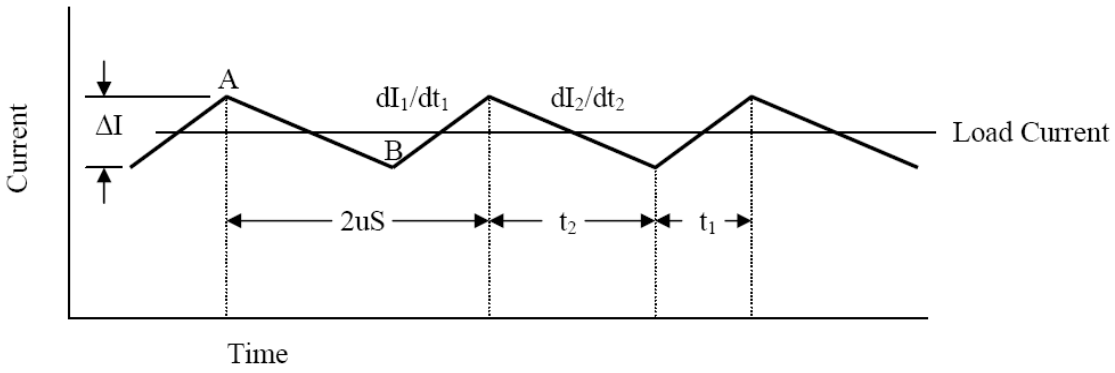


Fig. 2.3 Buck Converter Ripple Current

The largest di/dt is at current inflection points where current is sourced from different portions of the circuit. The voltage across an inductor is V = L di/dt

For an Inductor, we have $V = L \cdot \Delta I / \Delta T$

(2.4)

Rearranging and substituting gives:

$$L = (V_{in} - V_{out}) \cdot (D / f_{sw}) / I_{ripple} \quad (2.5)$$

where V_{in} is the input voltage, V_{out} is the output voltage, D is the duty cycle, f_{SW} is the Switching frequency, I_{ripple} is the Ripple current.

For an input voltage of 50 V and an output voltage of 6 V, the duty cycle will be:

$$D = V_{out} / V_{in} = 6/50 = 0.12 \quad (2.6)$$

The voltage across the inductance is:

$V_1 = V_{in} - V_{out} = 50 - 6 = 44$ V, when the switch is on (2.7)

$V_1 = -V_{out}$, when the switch is off (2.8)

In require inductance for ripple current of 0.22 A and switching frequency of 100 kHz can be calculated as

$$L = V_1 \cdot dt / di = (44 \times 0.12 / 100 \times 10^3) / 0.22 \quad (2.9)$$

$L = 240$ μH

From (2.3), it can be seen that increasing the ripple current leads to an increased duty cycle for keeping the filter size constant.

For n = 1, the duty cycle increase from D = 0.12 to 0.3775 for 1:1:1 transformer. In a conventional buck converter, the voltage gain is equal to the duty cycle. By increasing the turn ratio, the duty cycle increases keeping the voltage constant. From the Fig. 2.4, it can be seen that for a turn ratio n = 4, the duty cycle becomes 0.998 where the voltage gain is constant at 0.12. It is clear now that a transformer-linked converter has advantage over other conventional buck converter.

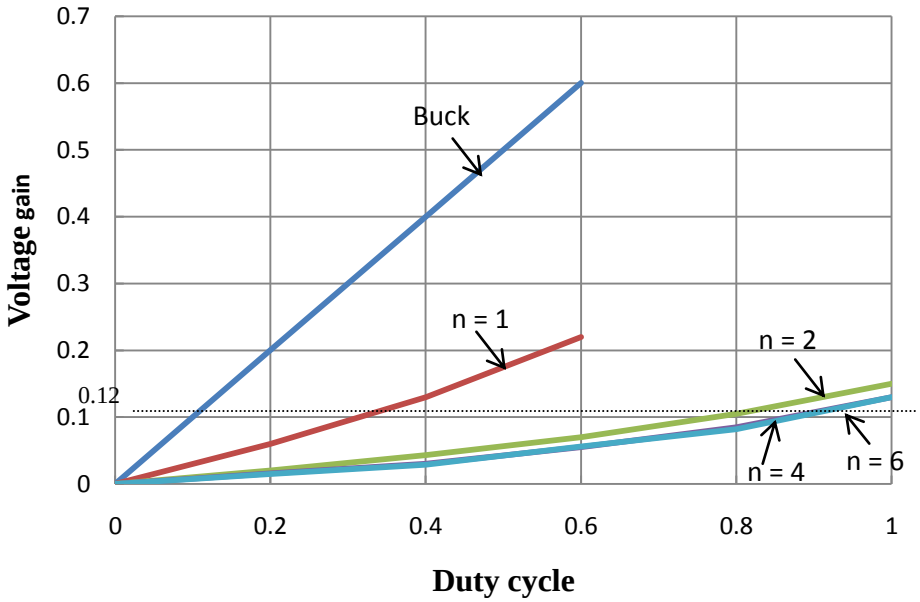


Fig. 2.4 Variation in duty cycle with turn ratio

2.3 *Dead time* Control

Another factor affecting the longevity of battery-operated electronic systems is the *dead time*. Converter losses decrease by 19% to 32% with the regulation of the *dead time* to a minimum value [100]. Insufficient *dead time* will result in shoot-through current via the HS and LS switches, while excessively long *dead time* will result in an unwanted body-diode

conduction loss and reverse recovery loss in the LS power MOSFET. Therefore, the *dead time* should be reduced so that the overall efficiency can be improved.

Because of significantly lower conduction losses, synchronous rectifiers are now used in essentially all low-voltage dc power supplies including converters for battery-operated electronics, point-of-load converters, microprocessor power supplies, etc. It is well known that optimum utilization of a synchronous rectifier depends on the ability to adjust the commutation *dead times*. Too long *dead times* result in additional losses due to the body diode conduction and the body-diode reverse recovery [22]. The *dead times* are adjusted adaptively to minimize the duty-cycle command, which results in maximization of the converter efficiency [100].

In the proposed transformer-link converter, a clamp capacitor C_b is used to control the *dead time* between the switches. As previously discussed, the *dead time* control is required to improve the efficiency of the converter. Charging and discharging of clamp capacitor control the *dead time*. The *Dead time* should not be very high otherwise the efficiency will decrease because of the increase of the body diode loss.

2.4 Operating principles and analysis

The following assumptions are made to simplify the circuit analysis:

- the secondary side leakage inductance is neglected;
- the capacitance of the blocking capacitor C_b is taken more as compared to other two capacitors used in this circuit;
- the capacitances of other two capacitors C_1 and C_2 are taken as same value;
- the turn ratio of transformer is taken asymmetrical;
- to make magnetizing current ripple free, the magnetizing inductance L_m is chosen as high value;

- and the current flowing through transformer is continuous.

At steady-state, the proposed converter has four operation states during one switching cycle. The key theoretical waveforms and the equivalent circuits of each operation state are shown by Fig. 2.5 and Fig. 2.6 (a-d).

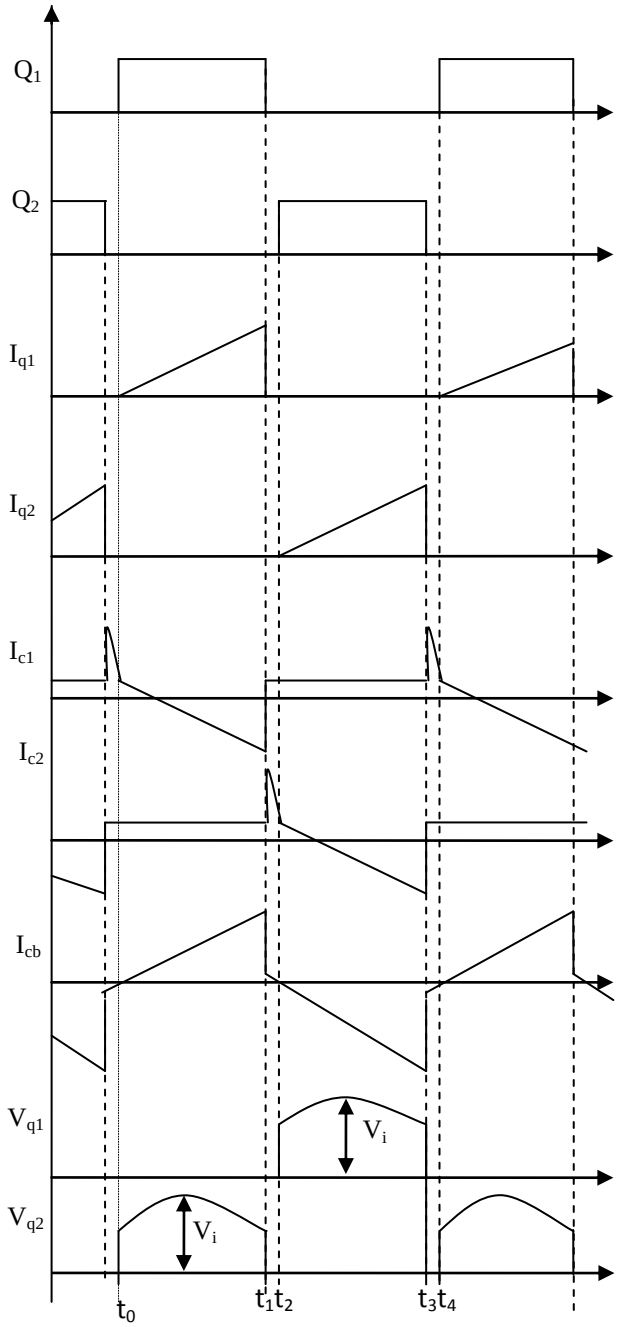


Fig. 2.5 Key theoretical waveforms of the proposed isolated converter

Mode 1 (t_0-t_1) : At t = t_0, MOSFET Q_1 is turned on by providing proper gate pulse. Now current starts to flow through the transformer. With the induction property, diode D_2 is compelled to conduct. Resonant conditions occur with the magnetizing inductance L_m and equivalent capacitance of C_b and C_1. However, the resonant period is less, so a high peak current and voltage stresses cannot appear across the switch Q_1.

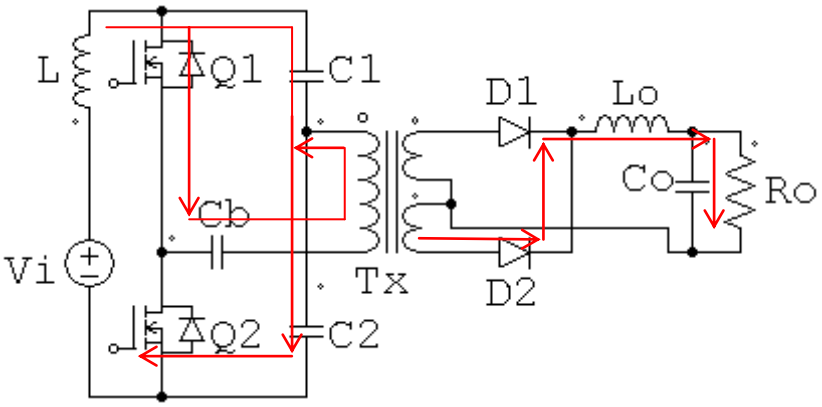


Fig. 2.6 (a) Operation Mode 1($t_0 - t_1$)

The voltage across capacitors C_1 and C_2, and the current through the input filter for this mode are derived as:

$$i_L(t-t_0)=\frac{V_i}{L}\left[P\sin\sqrt{k_1}(t-t_0)+Q\sin\sqrt{k_2}(t-t_0)\right] \tag{2.10}$$

$$v_{C1}(t-t_0)=\frac{V_i}{LC_1}\cdot\frac{P}{\sqrt{k_1}}\cos\sqrt{k_1}(t-t_0)-\frac{V_i}{LC_1}\cdot\frac{Q}{\sqrt{k_2}}\cos\sqrt{k_2}(t-t_0) \tag{2.11}$$

$$v_{C2}(t-t_0)=V_i-v_L(t-t_0)-v_{C1}(t-t_0) \tag{2.12}$$

where,

$$k_1,k_2=\frac{-\left(\frac{1}{L_mC_e}+\frac{1}{LC_e^{'}}\right)\pm\sqrt{\left(\frac{1}{L_mC_e}+\frac{1}{LC_e^{'}}\right)^2-\frac{4}{LL_mC_1C_2}}}{2},$$

$$C_e=\frac{C_1C_b}{C_1+C_b},\quad C_e^{'}=\frac{C_1C_2}{C_1+C_2},$$

$$Q = \frac{k_2 - \frac{1}{L_m C_e}}{k_1 - k_2},\ P = 1 - Q,$$

L is the input filter inductance, L_m is the magnetizing inductance of transformer

C_1 , C_2 and C_b are the clamp capacitors connected in the circuit,

k_1, k_2 are the resonant frequencies generated by the inductive and capacitive elements.

The switch is turned on under ZCS due to transformer leakage inductance L_m. This mode ends when capacitor C_1 completely discharges its energy to capacitor C_b and L_p. At this moment, the input current completely flow through capacitor C_1, providing a current through the switch equal to zero. At this moment switch Q_1 can be turned off under ZCS. At the end of this mode, C_b is charged up to V_{Cb1}, opposite to that of its initial value.

At t = t_1, we have $i_L(t_1) = I_{L1}$, $v_{C1} = 0$, $v_{Cb} = v_{Cb1}$, $v_{C2} = v_{C2}$',

Mode 2 (t_1-t_2) : At t = t_1, the stored energy of the inductor is forced the body diode of switch to conduct and inductor discharged its stored energy through C_2-Dq_2-C_b. Resonance condition occur between the primary inductance L_P and capacitors C_2 and C_b. However, the resonant period is not more than the *dead time*. The *Dead time* is controlled by capacitor C_b. This mode ends at t_2, when current through C_b becomes zero i.e., when this blocking capacitor is charged up to its maximum value.

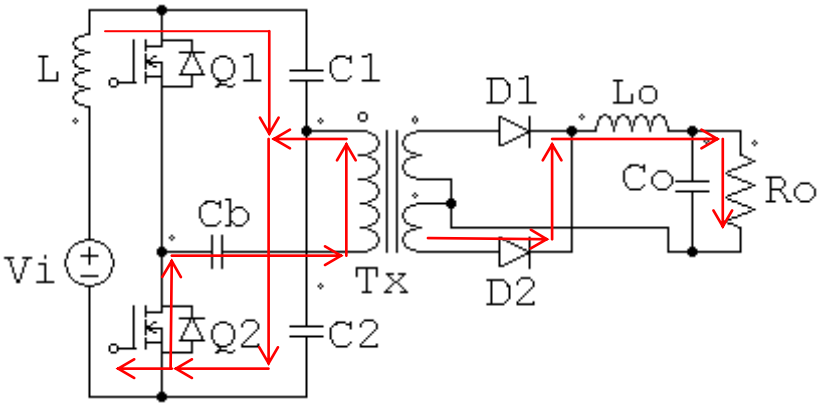


Fig. 2.6 (b) Operation Mode 2 ($t_1 - t_2$)

The voltage and current expressions for this mode are derived as:

$$i_L(t-t_1)=\frac{V_i-v_{C2}^{'}}{L}\left[R\sin\sqrt{k_3}(t-t_1)+S\sin\sqrt{k_4}(t-t_1)\right]+ I_{L1}\left[T\cos\sqrt{k_3}(t-t_1)+U\cos\sqrt{k_4}(t-t_1)\right] \tag{2.13}$$

$$i_{Lp}(t-t_1)=I_{L1}\cos\frac{1}{\sqrt{L_pC_e^{''}}}(t-t_1)-\frac{v_{Cb1}+v_{C2}^{'}}{Z_1}\sin\frac{1}{\sqrt{L_pC_e^{''}}}(t-t_1) \tag{2.14}$$

$$v_{Cb}(t-t_1)=\frac{I_{L1}\sqrt{L_pC_e^{''}}}{C_b}\sin\frac{1}{\sqrt{L_pC_e^{''}}}(t-t_1)+\left(v_{Cb1}+v_{C2}^{'}\right)C_e^{''}\cos\frac{1}{\sqrt{L_pC_e^{''}}}(t-t_1) \tag{2.15}$$

$$v_{C2}(t-t_1)=\frac{V_i-v_{C2}^{'}}{LC_2}\left[-\frac{R\cos\sqrt{k_3}(t-t_1)}{\sqrt{k_3}}-\frac{S\cos\sqrt{k_4}(t-t_1)}{\sqrt{k_4}}\right]+ \frac{I_{L1}}{C_2}\left[\frac{R\sin\sqrt{k_3}(t-t_1)}{\sqrt{k_3}}+\frac{S\sin\sqrt{k_4}(t-t_1)}{\sqrt{k_4}}\right] \tag{2.16}$$

Now the voltage across capacitor C_2 can be expressed as:

$$v_{C2}(t-t_1)=V_i-v_L(t-t_1)-v_{C1}(t-t_1) \tag{2.17}$$

where $T=\dfrac{L_PC_e^{'}C_2\left(V_i-v_{C2}^{'}\right)\cdot k_3-\left(LC_2+L_PC_e^{'}\right)I_{L1}}{2\left(\dfrac{1}{L_PC_e^{'}}+\dfrac{1}{LC_e}\right)}$, R = 1 - T,

$S=\dfrac{L_PC_e^{'}C_2\left(V_i-v_{C2}^{'}\right)\cdot k_3-\left(V_i-v_{C2}^{'}\right)C_2-\left(v_{cb1}+v_{C2}^{'}\right)C_e^{'}}{2\left(\dfrac{1}{L_PC_e^{'}}+\dfrac{1}{LC_e}\right)}$, U = 1 – S,

$$k_3=\frac{-\left(\dfrac{1}{L_PC_e^{'}}+\dfrac{1}{LC_e}\right)+\sqrt{\left(\dfrac{1}{L_PC_e^{'}}+\dfrac{1}{LC_e}\right)^2-4\left(\dfrac{1}{L_PC_e^{'}}+\dfrac{1}{LL_PC_2^2}\right)}}{2}$$

$$k_4=\frac{-\left(\dfrac{1}{L_PC_e^{'}}+\dfrac{1}{LC_e}\right)-\sqrt{\left(\dfrac{1}{L_PC_e^{'}}+\dfrac{1}{LC_e}\right)^2-4\left(\dfrac{1}{L_PC_e^{'}}+\dfrac{1}{LL_PC_2^2}\right)}}{2}$$

and $Z_1 = \sqrt{\frac{L_p}{C_e^{''}}}$, $C_e^{''} = \frac{C_b C_2}{C_b + C_2}$

Mode 3 (t_2-t_3) : This mode starts with switch Q_2 turned-on under ZVS, diode D_1 on with D_2 off. This mode will come to end with capacitor C_b charged upto its peak value, but with opposite polarity as compared to the previous mode. This mode ends when capacitor C_2 completely discharges its energy to capacitor C_b and L_p. At this moment, the input current completely flows through capacitor C_2, providing a current through the switch Q_2 equal to zero. Thus, switch Q_2 can be turned off under ZCS. At end of this mode, C_b is charged up to V_{Cb2} opposite to that of its initial value.

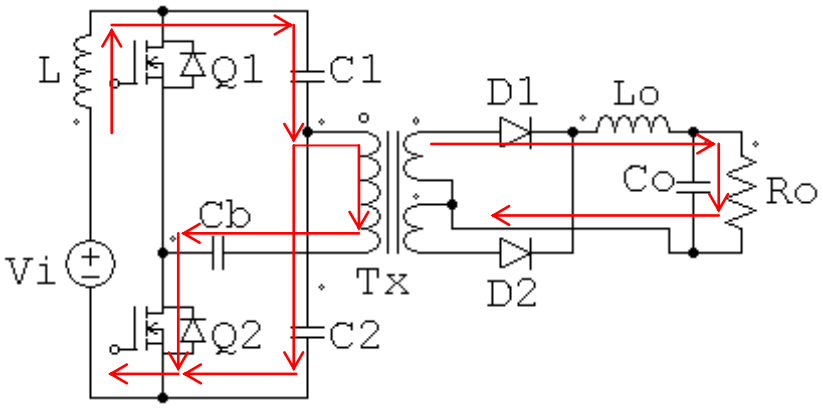


Fig. 2.6 (c) Operation Mode 3 ($t_2 - t_3$)

The current and voltage expressions for this mode are given as follows,

$$i_L(t-t_2) = I_{L2}\left[A\cos\sqrt{k_5}(t-t_2) + B\cos\sqrt{k_6}(t-t_2)\right] + \left(\frac{V - v_{C1}^{'}}{L} + \frac{v_{C2}^{''}}{L}\right)\left[C\sin\sqrt{k_5}(t-t_2) + D\sin\sqrt{k_6}(t-t_2)\right] \quad (2.18)$$

At the end of this mode, the current through the transformer is zero.

$$v_{C2}(t-t_2) = I_{L2}\left[\frac{A\sin\sqrt{k_5}(t-t_2)}{\sqrt{k_5}} + \frac{B\sin\sqrt{k_6}(t-t_2)}{\sqrt{k_6}}\right] - \left(\frac{V - v_{C1}^{'}}{L} + \frac{v_{C2}^{''}}{L_p}\right)\cdot\left[\frac{C\cos\sqrt{k_5}(t-t_2)}{\sqrt{k_5}} + \frac{D\cos\sqrt{k_6}(t-t_2)}{\sqrt{k_6}}\right] \quad (2.19)$$

$$v_{C1}(t-t_2) = V - v_L(t-t_2) - v_{C2}(t-t_2) \quad (2.20)$$

where $A = \dfrac{LL_PC_1C_2C_bI_{L1}\cdot k_5 - \left(LL_PC_bC_1C_2 + LC_1C_2\right)I_{L2} - L_PC_1C_bI_{cb2}}{2\left(\dfrac{1}{LC_1C_2} + \dfrac{1}{L_PC_2C_b} + \dfrac{1}{L_PC_2} + \dfrac{1}{LC_2}\right)}$, C = 1 – A,

$B = \dfrac{\left(L_PC_bC_1C_2\cdot k_5 - \left(C_1C_b + C_1C_2\right)\right)\left(V_i - v_{C1}^{'} - v_{C2}^{''}\right)}{2\left(\dfrac{1}{LC_1C_2} + \dfrac{1}{L_PC_2C_b} + \dfrac{1}{L_PC_2} + \dfrac{1}{LC_2}\right)}$, D = 1 – B,

$$k_5 = \frac{-\left(\frac{1}{LC_1C_2} + \frac{1}{L_PC_2C_b} + \frac{1}{L_PC_2} + \frac{1}{LC_2}\right) + \sqrt{\left(\frac{1}{LC_1C_2} + \frac{1}{L_PC_2C_b} + \frac{1}{L_PC_2} + \frac{1}{LC_2}\right)^2 - 4\cdot\frac{1+C_1+C_b}{LL_PC_1C_2C_b}}}{2},$$

$$k_6 = \frac{-\left(\frac{1}{LC_1C_2} + \frac{1}{L_PC_2C_b} + \frac{1}{L_PC_2} + \frac{1}{LC_2}\right) - \sqrt{\left(\frac{1}{LC_1C_2} + \frac{1}{L_PC_2C_b} + \frac{1}{L_PC_2} + \frac{1}{LC_2}\right)^2 - 4\cdot\frac{1+C_1+C_b}{LL_PC_1C_2C_b}}}{2},$$

$I_{L2} = i_L(t_2)$,

$v_{C2}^{''} = v_{C2}(t_2)$

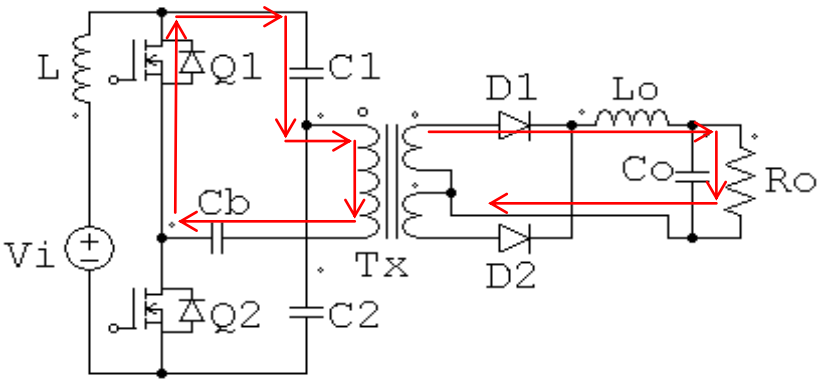


Fig. 2.6 (d) Operation Mode 4 ($t_3 - t_4$)

Mode 4 (t_3-t_4) : The transformer starts to transfer the stored energy to secondary side as well as to capacitor C_1. This ensure the continuous flow of the current at the output. Then, the rectified diode D_2 will start to conduct, while diode D_1 will be turned off under ZVS. The body diode of the switch Q_1 is turned on due to the energy transferring property of the inductor in the same direction in which it get charged. The mode ends at t_4, when current through C_b becomes zero i.e., when the blocking capacitor is charged up to its maximum value. The next mode starts when Q_1 is turned on under ZVS.

The current and voltage expressions for this mode are given as follow:

$$i_{Lp}(t-t_3) = I_{Lp1}\cos\frac{1}{\sqrt{L_pC_e}}(t-t_3) + \frac{v_{Cb2}}{Z_2}\sin\frac{1}{\sqrt{L_pC_e}}(t-t_3) \tag{2.21}$$

$$\begin{aligned} i_L(t-t_3) = \frac{V_i}{Z_3}\sin\frac{1}{\sqrt{LC_e}}(t-t_3) - \frac{I_{Lp1}}{LC_1}\left[E\sin\sqrt{k_8}(t-t_3) + F\sin\sqrt{k_9}(t-t_3)\right] \\ + \frac{v_{Cb2}}{Z_2}\left[G\cos\sqrt{k_8}(t-t_3) + H\cos\sqrt{k_9}(t-t_3)\right] \end{aligned} \tag{2.22}$$

$$v_{Cb}(t-t_3) = \frac{I_{Lp1}\sqrt{L_pC_e}}{C_b}\sin\frac{1}{\sqrt{L_pC_e}}(t-t_3) - \frac{v_{Cb2}\sqrt{L_pC_e}}{Z_2}\sin\frac{1}{\sqrt{L_pC_e}}(t-t_3) \tag{2.23}$$

where $Z_2 = \sqrt{\frac{L_p}{C_e^{'}}}$, $C_e^{'} = \frac{C_1C_2}{C_1+C_2}$, $C_e = \frac{C_bC_1}{C_b+C_1}$ and $Z_3 = \sqrt{\frac{L}{C_e}}$

where $G = \frac{L_PC_eC_1\left(V_i - v_{C2}^{'}\right)\cdot k_7 - \left(LC_1 + L_PC_e\right)I_{L3}}{2\left(\frac{1}{L_PC_e} + \frac{1}{LC_e^{'}}\right)}$, E = 1 - G,

$F = \frac{L_PC_eC_1\left(V_i - v_{C1}^{''}\right)\cdot k_7 - \left(V_i - v_{C1}^{''}\right)C_1 - \left(v_{cb1} + v_{C1}^{''}\right)C_e}{2\left(\frac{1}{L_PC_e} + \frac{1}{LC_e^{'}}\right)}$, H = 1 – F,

$$k_7 = \frac{-\left(\frac{1}{L_PC_e} + \frac{1}{LC_e^{'}}\right) + \sqrt{\left(\frac{1}{L_PC_e} + \frac{1}{LC_e^{'}}\right)^2 - 4\left(\frac{1}{L_PC_e} + \frac{1}{LL_PC_1^2}\right)}}{2}$$

$$k_8 = \frac{-\left(\frac{1}{L_PC_e} + \frac{1}{LC_e^{'}}\right) + \sqrt{\left(\frac{1}{L_PC_e} + \frac{1}{LC_e^{'}}\right)^2 - 4\left(\frac{1}{L_PC_e} + \frac{1}{LL_PC_1^2}\right)}}{2},$$

$v_{C1}^{"} = v_{C1}(t_3)$,

At the end of this mode $v_{Cb} = - v_{Cbmax}$.

2.5 Design procedure

The advent of the switching regulator has greatly reduced the size, weight and volume of power conversion circuitry, while improving both the response speed and efficiency. It is easy to minimize the resistance because we have very low ESR capacitors, low on-resistance MOSFETs and low series-resistance inductors.

The design should take into account the following considerations:

1. $C_b \geq C_1$ and C_2: This condition gives a minimized *dead time* with reduced of turn-on and turn-off losses. Charging process of C_b should be more as compared to that of C_1 and C_2, which is responsible to provide minimum *dead time*. It controls the duration of body diode conduction. This is possible with higher value of C_b. The clamp capacitor C_b can be determined form the inequality as:

$$t_{12} = (t_2 - t_1) \geq \frac{C_b (v_{Cb\max} - v_{Cb1})}{I_{Cb1}} \tag{2.24}$$

2. The transformer primary inductance L_p should be such a value that it can discharge its energy completely to C_b, C_1, C_2:

$$\frac{1}{2} L_p I_{Lp\max}^2 = \frac{1}{2} C_b v_{Cb}^2 + \frac{1}{2} C_1 v_{C1}^2 + \frac{1}{2} C_2 v_{C2}^2 \tag{2.25}$$

2.5.1 Transformer Design:

The high-frequency transformer is designed with the help of the effective core volume V_e and the minimum core-cross-section A_{min}. For a required power output $P_{out} = V_{out} \cdot I_{out}$ and for the operating frequency f, a suitable core volume V_e must be determined. Then, an optimal ΔB is selected depending on the chosen switching frequency

and also regarding the temperature rise of the transformer. The physical size is dependent on the power to be transferred as well as on the operating frequency. The trend in power supplies is towards miniaturization. In general, an increase of the switching frequency results in a smaller size of magnetic components. However, since core loss and copper loss increase with the frequency, the size of the magnetic components has to be optimized at the operating frequency.

The first step to design a high frequency transformer is usually to choose an appropriate core. Core-weight or core-volume is determined depending on the transfer power and switching frequency. In the second step, the primary number of turns is calculated because this determines the magnetic flux-density within the core. Then, the wire-diameter is calculated, which is dependent on the current in the primary and secondary coils.

According to Faraday's law, for the tertiary winding transformer, the cross section area of the core can be expressed as

$$A_{core} = \frac{\sqrt{2}V_i}{2\pi N_1 f B_m} \tag{2.26}$$

where B_m is the maximum flux density, f is the operating frequency, V_i is the input voltage on the transformer primary side.

On the other hand, the cross sectional areas A_{cop1} and A_{cop2} of the copper wire can be determined by choosing a current density J_m. The window area is

$$A_{window} = \frac{N_1 A_{cop1} + N_2 A_{cop2}}{K_u} = \frac{N_1 I_1 + N_2 I_2}{K_u J_W} \tag{2.27}$$

where, K_u is the window utilization factor, which depends on the wire type, wire size, insulation requirement, and winding technique. But K_u can be chosen as 0.4 for solid wire and 0.3 for Litz wire [101-103].

Now the required area,

$$A_p = A_{core} A_{window} = \frac{V_1 I_1 + V_2 I_2}{\sqrt{2}\pi K_u B_m J_w} \tag{2.28}$$

core volume V_e can be determined from the A_p data.

The transformer should be designed to minimize the leakage inductance, ac winding losses, and core losses. When the transformer is designed to operate in discontinuous mode the total inductance is lower than in continuous mode, and the size of the transformer may be smaller. But the peak currents will be at least twice the average current, therefore ac winding losses and core losses are the predominant factors rather than the dc losses and core saturation.

2.5.1.1 Core selection:

To reduce the core losses, ferrite-P material is usually the preferred material for discontinuous transformers with operating switching frequencies higher than 100 KHz. The window shape of the core should be as wide as possible to minimize the number of layers and therefore minimize the ac winding losses and the leakage inductance. E-type cores with an internal air-gap are the best choice for low cost and lower leakage inductance.

To minimize the ac losses, leakage inductance and the EMI noise, particular attention has to be paid to the design of the primary and secondary windings of the transformer. The primary winding should be designed for less than three layers, to minimize the winding capacitance and the leakage inductance of the transformer. In high switching frequency applications an additional insulating layer is usually used between windings.

2.5.1.2 Calculation of the wire-diameter:

The wire diameter depends on the respective r.m.s. value of the coil current. This can be calculated from the coil power.

The current density S is chosen between 2 and 5 A/mm^2, depending on the thermal resistance. The wire cross-section A_{wire} and the wire diameter d_{wire} can be calculated as follows [33]:

$$A_{wire} = \frac{I}{S} \text{ and } d_{wire} = \sqrt{I \cdot \frac{4}{S \cdot \pi}} \tag{2.29}$$

Usual cores are designed such that the above calculated coil fits into the available winding area. Both primary and secondary windings need an equal amount of the winding area.

2.6 Simulation and Experimental results

The validity and performance of the proposed converter are evaluated with simulated and experimental tests. The converter is designed for 360 W, 50 V/6 V and with a switching frequency of 100 kHz. The other chosen parameters are, R_o = 0.1 Ω, L_m = 5 μH, n_1:n_2 = 4 : 1,. Simulated waveforms results are shown in Figs. 2.7 (a-c), Figs. 2.8 (a-c), Figs. 2.9 (a-c) and Figs. 2.10 (a-c). Experimental results are shown in Figs. 2.11 (a-b).

2.6.1 Simulation results

The converter is simulated using PSIM 7.1 version. Simulation results presented in Figs. 2.7 (a-c) show the effects of the duty cycle on the ripple current of the converter. For a turn ratio = 1:1:1, the ripple current in the output inductor as well as in the input inductor is shown in Fig. 2.7 (a). Similarly, the change in ripple current for n = 2 and n = 4, is shown in Fig. 2.7 (b-c). It can be observed from Figs. 2.7 (a-c) that, an increased turn ratio extends the duty cycle and that an extended duty cycle reduces the amount of ripple current.

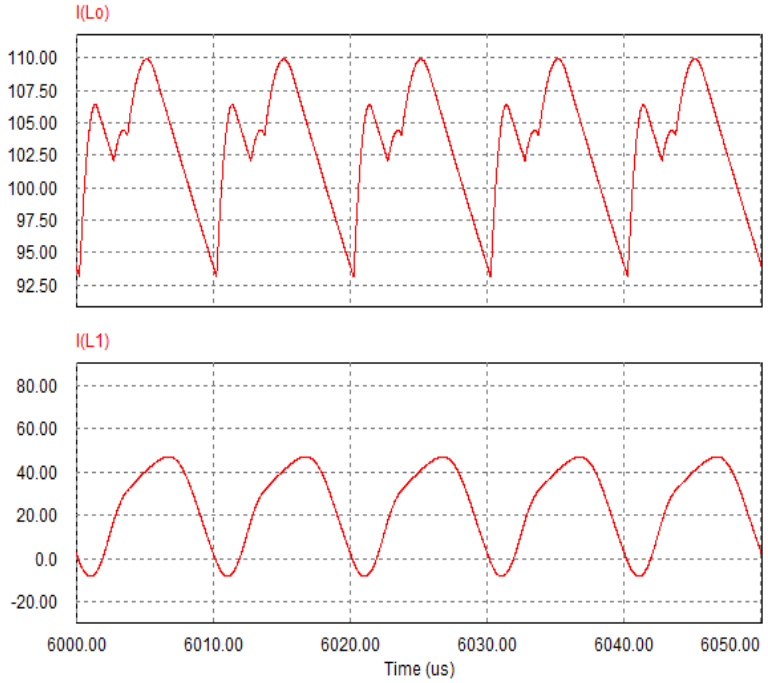


Fig. 2.7 (a) Simulated current waveforms of output and input inductor current at n = 1: I_{L0} and I_{L1} in Amps

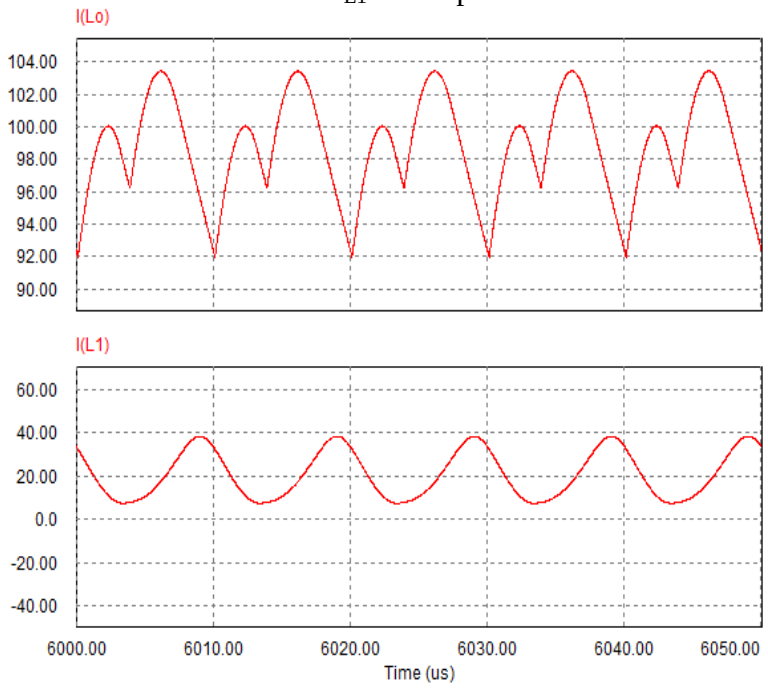


Fig. 2.7 (b) Simulated current waveforms output and input inductor current at n = 2: I_{L0} and I_{L1} in Amps

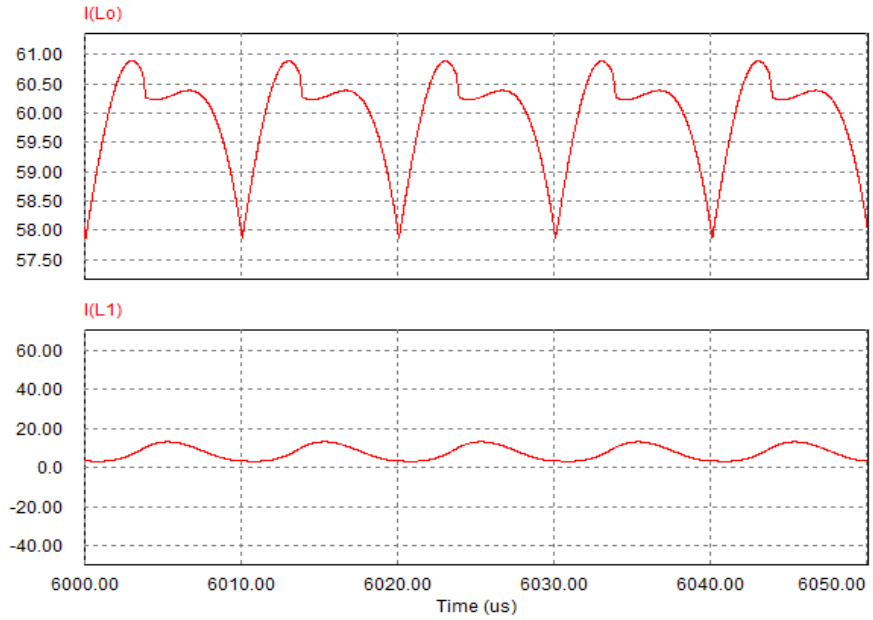


Fig. 2.7 (c) Simulated current waveforms output and input inductor current at n = 4: I_{L0} and I_{L1} in Amps

The effect of duty cycle on the voltage stress across the switches can be seen. Fig. 2.8 (a) shows the current stress and voltage stress of the main switch at turn ratio n = 1. The same is represented in Fig. 2.8 (b) with n = 2 and in Fig. 2.8 (c) with n = 4. It is observed that with n = 1 the voltage & current stresses are very high, which is not tolerable. A high turn ratio (n = 4) controls the stresses within a tolerable limit. Similarly, the effect of turn ratio on voltage and current stresses for switch Q_2, are shown in Fig. 2.9 (a-c).

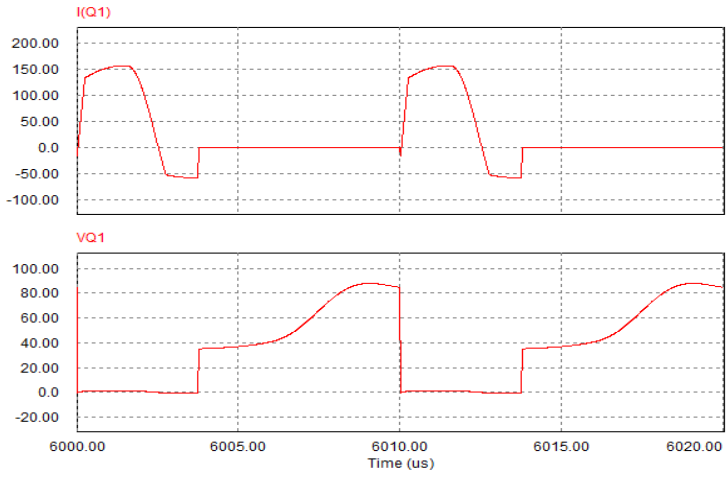


Fig. 2.8 (a) Simulated voltage and current waveforms for switch Q_1 for n =1: V_{Q1} in Volts and I_{Q1} in Amps

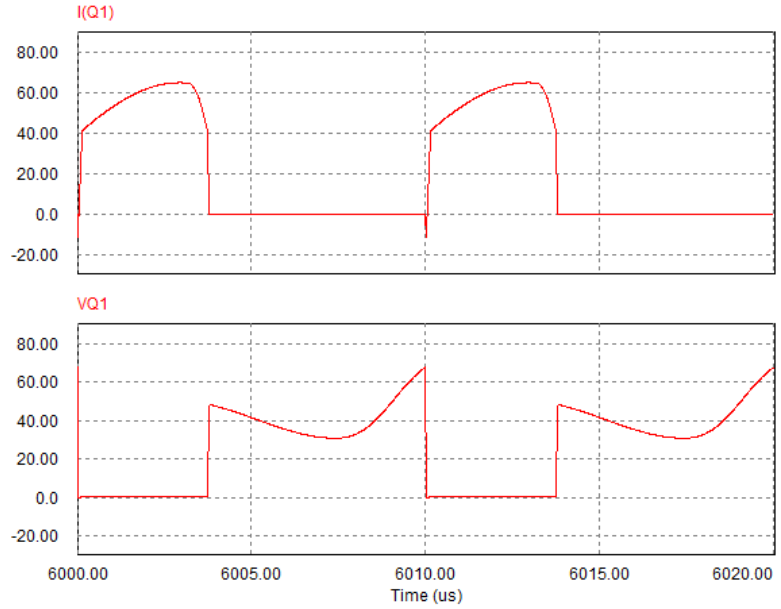


Fig. 2.8 (b) Simulated voltages and current waveforms for switch Q_1 for n = 2: V_{Q1} in Volts and I_{Q1} in Amps

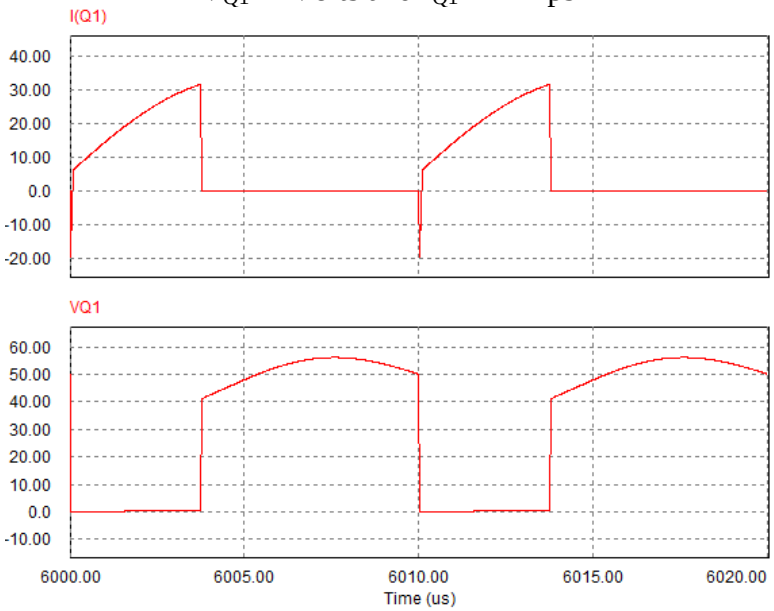


Fig. 2.8 (c) Simulated voltage and current waveforms for switch Q_1 for n = 4: V_{Q1} in Volts and I_{Q1} in Amps

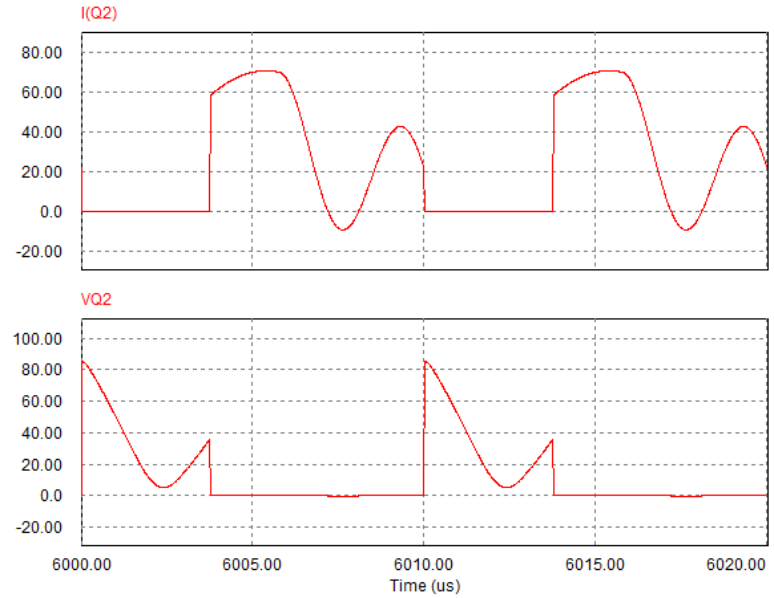


Fig. 2.9 (a) Simulated voltage and current waveforms for switch Q_2 for n = 1: V_{Q2} in Volts and I_{Q2} in Amps

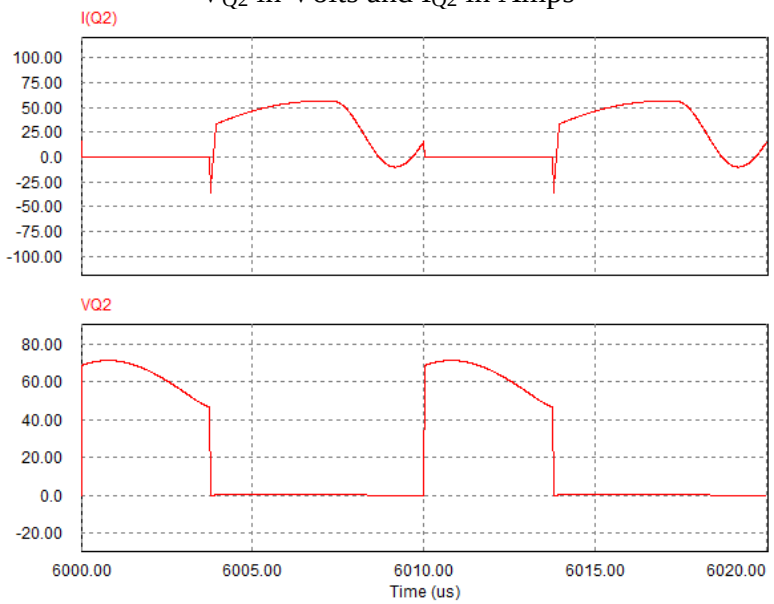


Fig. 2.9 (b) Simulated voltage and current waveforms for switch Q_2 for n = 2: V_{Q2} in Volts and I_{Q2} in Amps

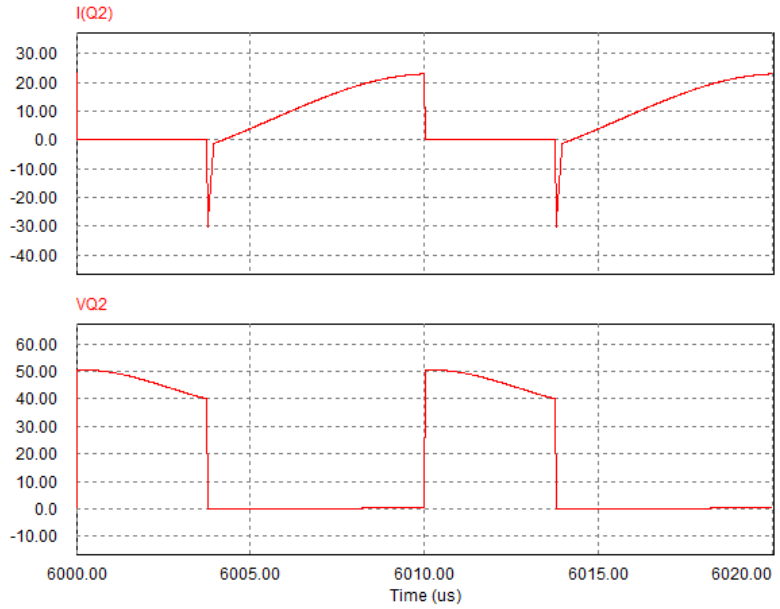
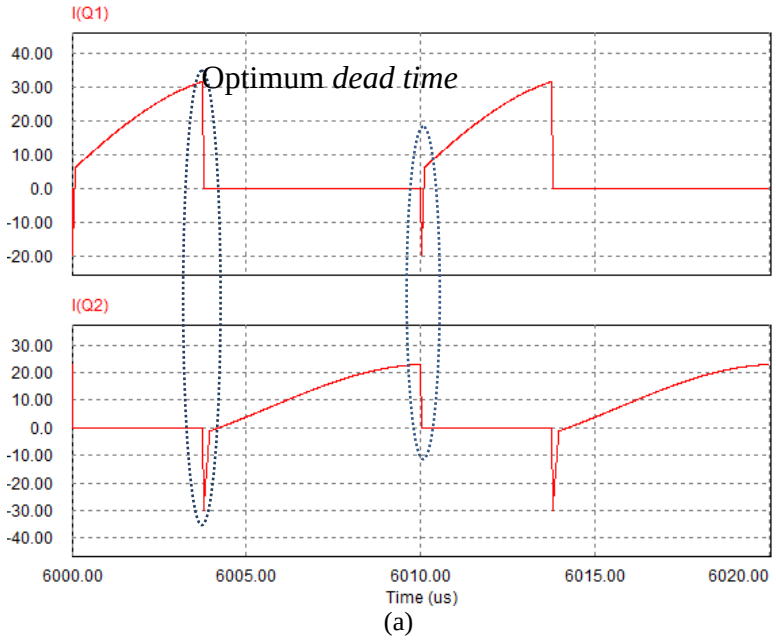


Fig. 2.9 (c) Simulated voltage and current waveforms for switch Q_2 for n = 4. : V_{Q2} in Volts and I_{Q2} in Amps

The optimum dead time required for the proposed converter is controlled by the clamp capacitor C_b, which is shown in Fig 2.10 (a). From the simulated waveforms presented in Figs. 2.10 (b-c), it can be seen that both switches are turned on under ZVS and turned off under ZCS.



(a)

Fig. 2.10 (a) Optimum *dead time* for both switches

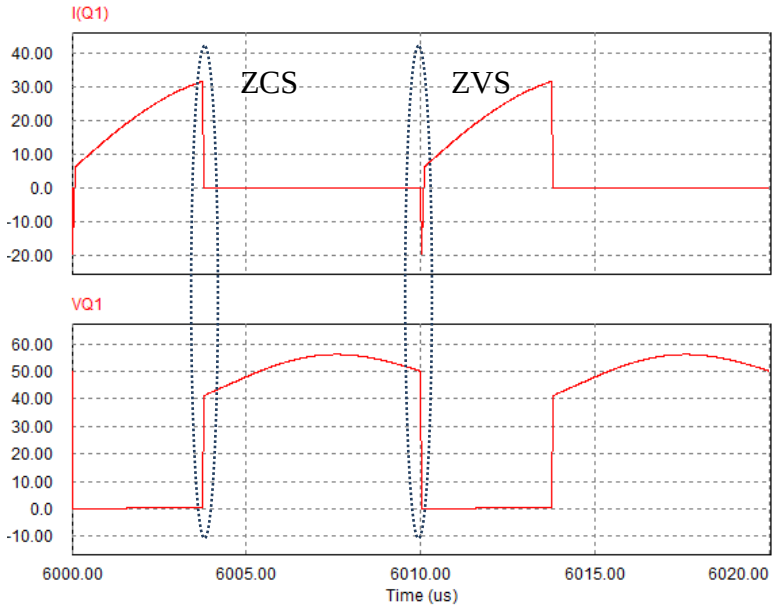


Fig. 2.10 (b) Simulated current and voltage waveforms of switch Q1: V_{Q1} in Volts and I_{Q1} in Amps

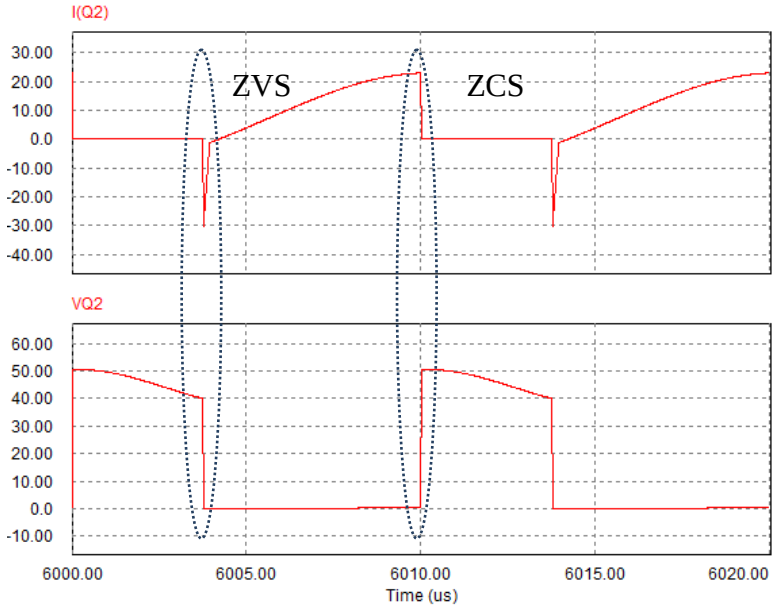


Fig. 2.10 (c) Simulated current and voltage waveforms of switch Q2: V_{Q2} in Volts and I_{Q2} in Amps

2.6.2 Experimental Results

A prototype model is developed and tested in the laboratory to demonstrate the validity of the simulated results. The experimental results show that the proposed converter is properly designed with soft switching realization for the switches. The photograph of

proposed isolated converter is shown in Fig. 2.12. The experimental waveforms of the proposed converter are shown in Fig. 2.11 (a) and 2.11 (b). All parameters details are given in Tables 2.1 and 2.2.

TABLE 2.1
Transformer designed parameter for experimental converter

Parameter		Name	Value	Unit
	Core	RM10×1	8	mm
Transformer	Inductance	L_M	5	μH
	Trans Ratio	N_p:N_s:N_t	4:1:1	
	Leakage Inductance	L_{lk}	0.1	μH

TABLE 2.2
Components used in the proposed converter

Component	Value/Model	
	Simulation	Experiment
MOSFET Switch, Q_1	Ideal	IRFP250N
MOSFET Switch, Q_2	Ideal	IRFP250N
Schottky Diode, D_1	Ideal	MBR60L45CTG
Schottky Diode, D_2	Ideal	MBR60L45CTG
Input Inductor, L_1	2 μH	2 μH
Capacitor, C_1	4 μF	4 μF
Capacitor, C_2	4 μF	4 μF
Blocking Capacitor, C_b	6 μF	6 μF
Output Inductor, L_o	3 μH	3 μH
Output Capacitor, C_o	20 μF	20 μF

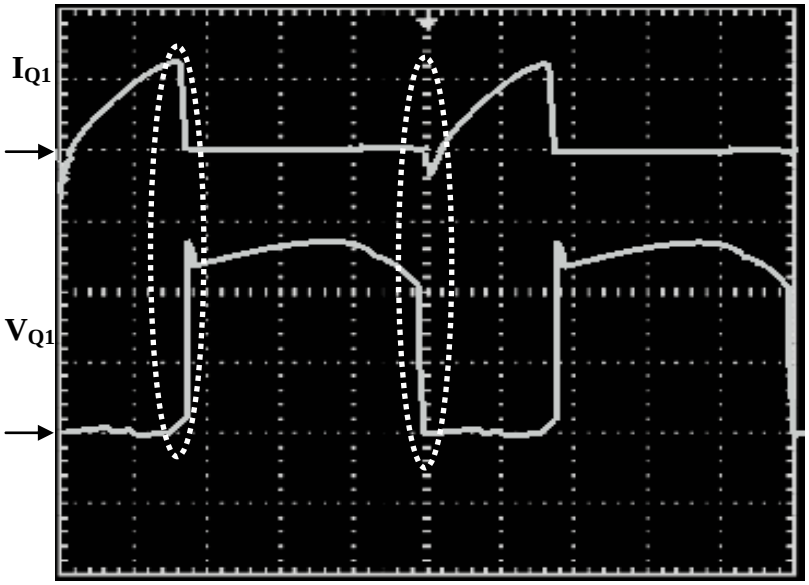


Fig. 2.11 (a) Experimental voltage and current waveforms of switch Q_1: (V_{Q1}: 20 V/div, $I_{Q1:}$ 20 A/div)

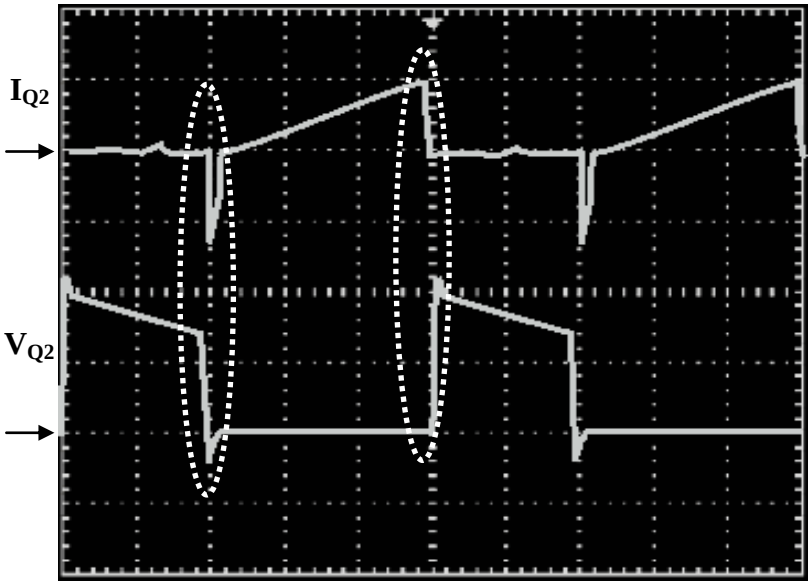


Fig. 2.11 (b) Experimental voltage and current waveforms of switch Q_2: (V_{Q2}: 20 V/div, I_{Q2} : 20 A/div),time (2 μs/div)

Fig. 2.12 Photograph of proposed isolated buck converter

The experimental results at 100 kHz switching frequency confirm the validity of the simulation results. In Fig. 2.13, the efficiency as a function of the load current is shown and indicates that efficiency can be improved by 12% with the ZVS. The efficiency obtained in our topology is compared with the converter which is proposed in [96] and [97]. Fig. 2.14 shows the improved efficiency computed from experimentation of proposed converter as compared to other topologies.

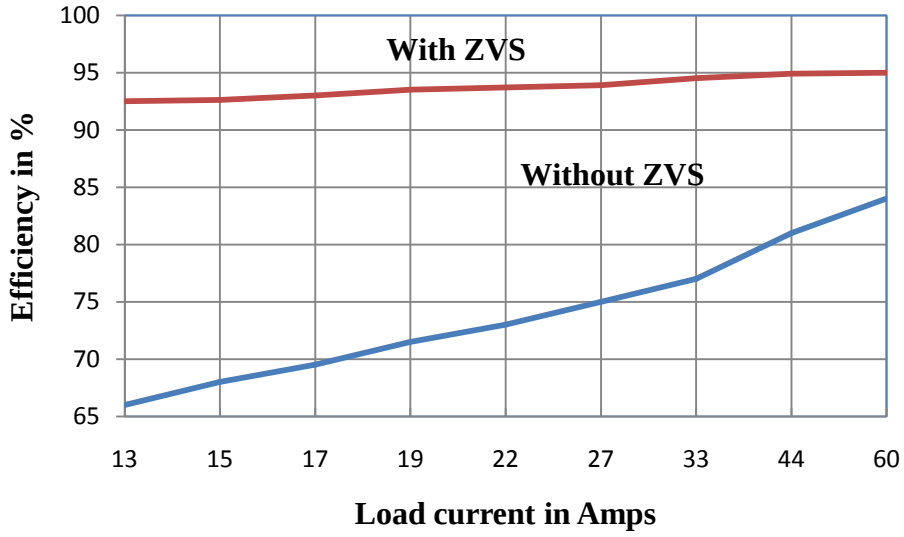


Fig. 2.13 Graph between efficiency and load current

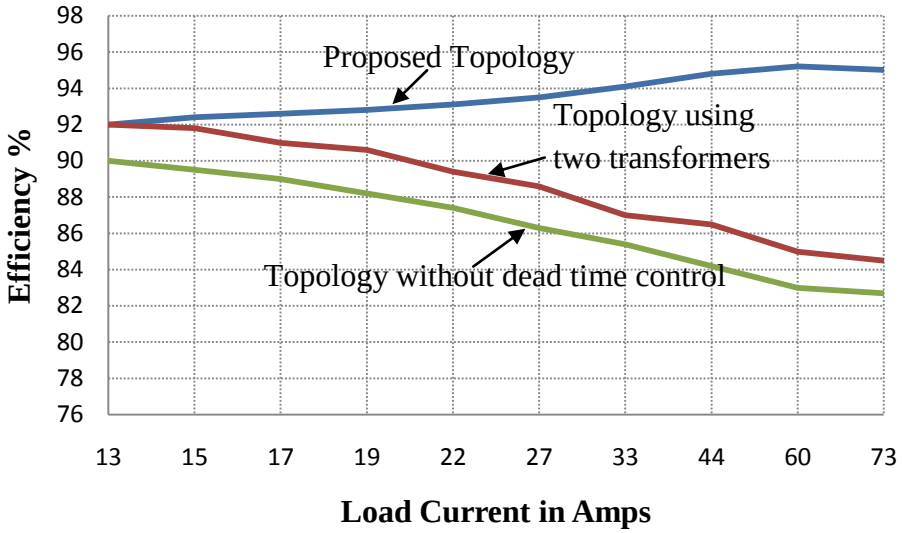


Fig 2.14 Comparison of Efficiency of proposed topology with other referred papers

Fig. 2.14 shows that efficiency of the proposed converter remains constant at 95% for the load range 55 Amps to 60 Amps. Then, after it starts decreasing.

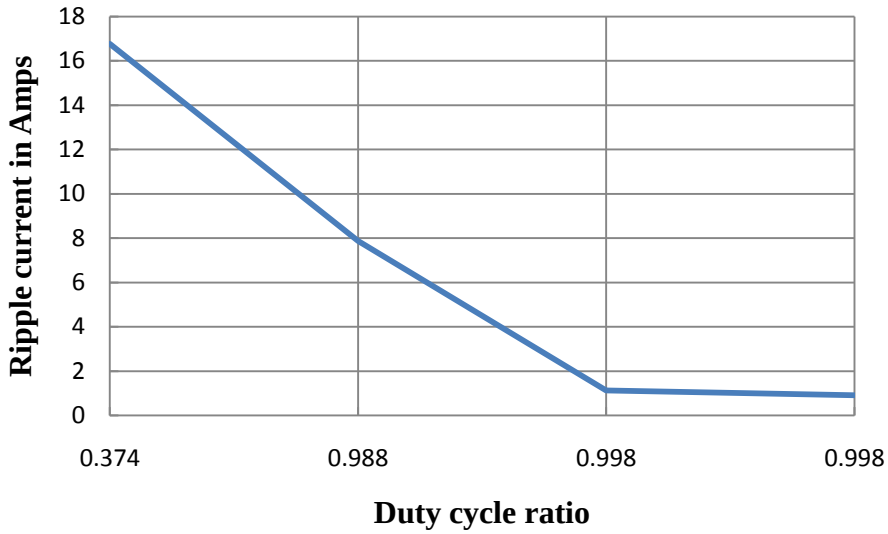


Fig. 2.15 Ripple current variation with respect to duty cycle

Comparing both Fig. 2.15 and Fig. 2.16, allows to conclude that a turn ratio n = 4 provide the optimum duty cycle i.e. 0.998 and that the ripple current is also minimum. By taking the ripple current value, the filter inductor can be designed according to (2.3).

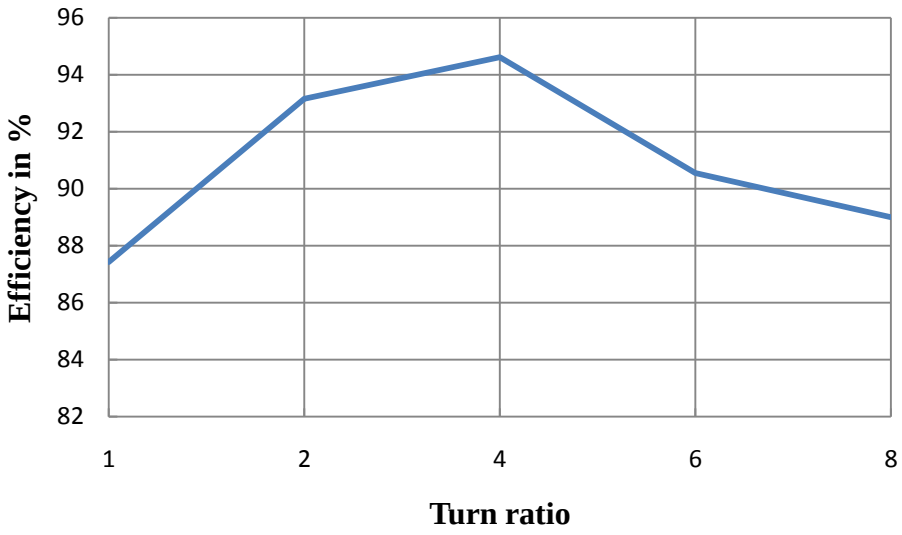


Fig. 2.16 Efficiency vs. Turn ratio

Fig. 2.16 shows the variation of the efficiency with respect to the turn ratio. With turn ratio n = 4, the proposed converter gives highest efficiency. The effect of dead time on efficiency can be explored from Fig. 2.17.

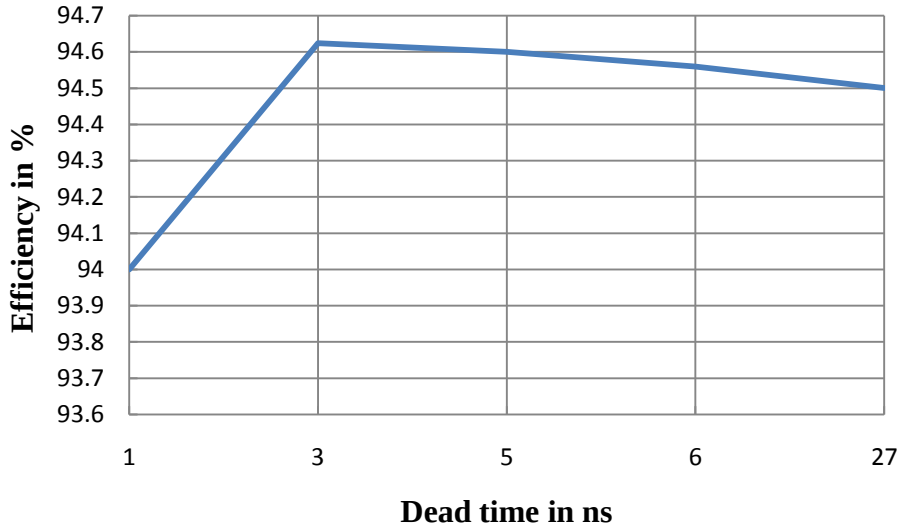


Fig. 2.17 Efficiency vs. Dead time

2.7 Summary of Isolated Buck Converter

An isolated buck converter with a clamp capacitor scheme has been presented. The duty cycle is extended by increasing the turn ratio and the dead time is controlled with the clamp capacitor scheme to improve efficiency. It is configured in a simple way. It has a low cost and is easy of control. The converter acts as a conventional PWM converter during most of the switching cycle. All the switches used in this circuit are turned on and off under ZVS and ZCS respectively. Filter components are designed using the duty cycle to get tolerable ripple current. Voltage and current stresses in switches are also reduced with an extended duty cycle. A prototype of 360 W, 50 V/6 V at switching frequency of 100 kHz with an optimized turn ratio was implemented to experimentally verify the improved performance.

2.8 Concept extension with tapped inductor

The previous sections analyze the isolated converter employing a transformer. With the replacement of the transformer by a tapped inductor, its efficiency may be maximized for low power applications and power quality is improved as low order harmonics are predominantly reduced. A tapped inductor provides a better power density as compared to an isolation buck converter. This converter is cost effective and attractive for high performance. The peak current of the main switch is reduced by tapped inductor operations, thus the conduction loss and switching loss levels of the main switch are lowered. Consequently, this tapped inductor scheme alleviates the severe power stress and enhances the device utilization. A novel ZVS step-down converter with a tapped inductor is proposed in this section. This soft-switching buck converter is suitable for extremely low step-down ratio applications. The principle of the proposed scheme, analysis of the operation, and design guidelines are included. Finally, the simulation result of the 10 W dc-dc converter is verified with the theoretical concept.

The isolation type converters keep a low efficiency level due to the transformer loss itself and the bulky size with an increasing number of extra components to reset the transformer. To obtain the extreme voltage conversion and the high efficiency, the application of a tapped inductor (TI) has been considered as one of the effective alternatives in previous researches [15, 94, 104], where the tapped inductor operates as an autotransformer without the need of a reset circuit. Furthermore, an autotransformer employment utilizes less copper than an isolation-type transformer. However, there are still some difficulties in applying the TI to converters because the ringing between the leakage inductance of the inductor and the parasitic capacitances in switches leads to higher voltage stress across switching devices and more EMI. These problems prevent the tapped inductor employment from being the optimal solution for extreme conversion ratio applications. In order to remove these problems, it is necessary to apply the soft-switching technique to TI applications [12, 105-106].

2.9 Tapped Inductor Circuit Topology

The proposed converter scheme is shown in Fig. 2.19. The circuit scheme includes two MOSFET switches Q_1 and Q_2 and two clamp capacitors C_1 and C_2. The tapped inductor T_i denotes the combination of the fixed and variable inductance. The proposed dc-dc converter designed through AC link as energy transfer devices. In steady-state, the proposed converter has five operation states during one switching cycle.

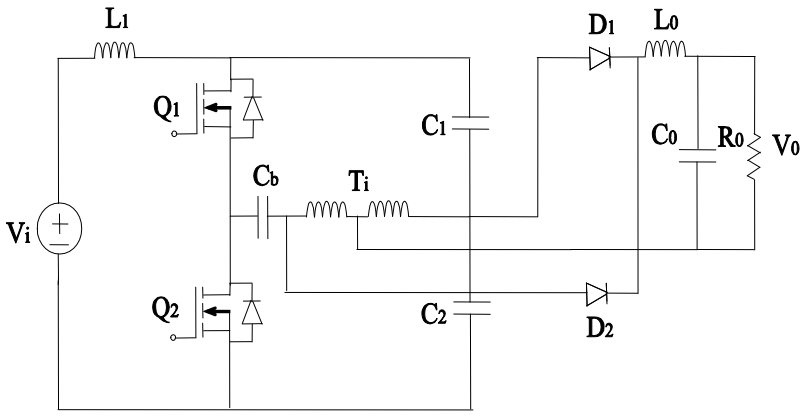


Fig. 2.18. The proposed TI converter

In this topology, the ZVS technique implemented in the transformer converter topology is applied. The proposed converter improves the performance. The clamp capacitor and the tapped inductor perform soft switching operation, so the stresses across the switches are reduced to increase the efficiency at the low power output. The improvement includes another soft switching technique by two capacitors C_1 and C_2 which gives alternate design freedom for the selection of the turn-ratios and enables the optimal design of the TI so that both the switching loss and the conduction loss may be minimized. This soft-switching converter is suitable for applications with wide input ranges leading to extremely low step-down ratios. The principle of operation and the design process will provide elaborately in the following sections of the paper.

On the secondary side, a rectifier circuit is used to maintain the unidirectional output current. Two diodes simultaneously cannot conduct. The performance of the propose converter is compared with the conventional converter and with previously proposed converters.

2.10 Operating principles

The following assumptions are made to simplify the circuit operations

- the capacitance of the blocking capacitor is taken more as compared to other two capacitors used in this circuit;
- the capacitances of other two capacitors are taken at the same value;
- the inductance of tapped inductor L_{Ti} is designed properly to make input current ripple free;
- the current flowing through transformer is continuous;

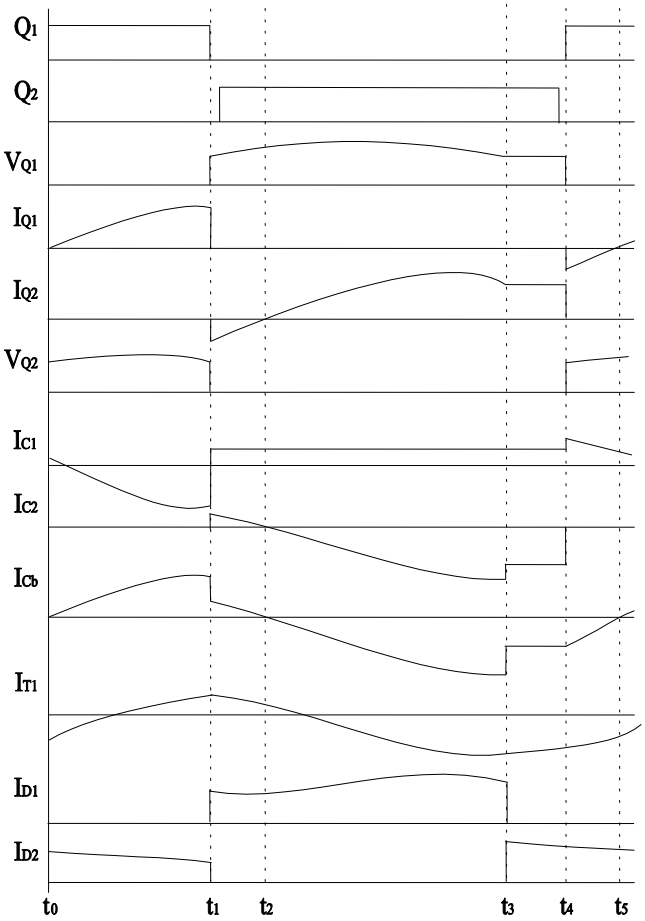


Fig. 2.19. Key Waveforms of proposed TI converter

The key theoretical waveforms and the equivalent circuits of each operation state are shown in Fig. 2.19 and Fig. 2.20 (a - e), respectively.

Mode 1 (t_0-t_1) : At t = t_0, the MOSFET Q_1 is turned on by providing a proper gate pulse. Then the current starts to flow through the trapped inductor. The diode D_2 is forward biased while voltage drop across tapped inductor will turn off diode D_1. Resonant conditions occur

by the inductance L_{Ti} and by equivalent capacitance of C_b and C_1. But the resonant period is less, so high peak current and voltage stresses cannot appear across the switch Q_2.

The switch is turned on under ZCS due to tapped inductor inductance L_{Ti}. This mode ends when capacitor C_1 completely charges to its peak value. At this moment, the input current completely flow through capacitor C_1, providing current through the switch equal to zero. At this moment switch Q_2 can be turned off under ZCS. At end of this mode, C_b is charged up to C_{b1} opposite to that of its initial value.

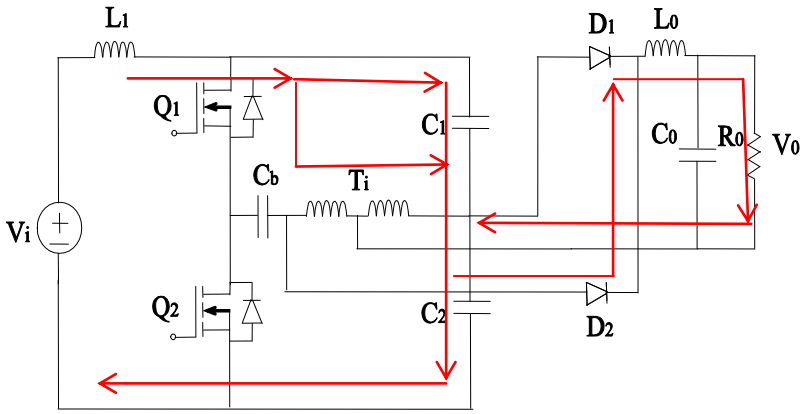


Fig. 2.20 (a) Modes of Operation: Mode I ($t_0 - t_1$)

Mode 2 (t_1-t_2) : At $t = t_1$, the stored energy of inductor is forced the body diode of switch Q_2 and rectifier diode D_1 starts to conduct. The tapped inductor discharged its stored energy through C_2-D_{q2}-C_b and some part of the energy is transferred to the load. The resonance occurs between inductance L_{Ti} and capacitors C_2 and C_b. However, the resonant period is not more than the dead time. Dead time is controlled by capacitor C_b. The mode ends at t_2, when the current through C_b becomes zero, i.e., this blocking capacitor is charged upto its maximum value.

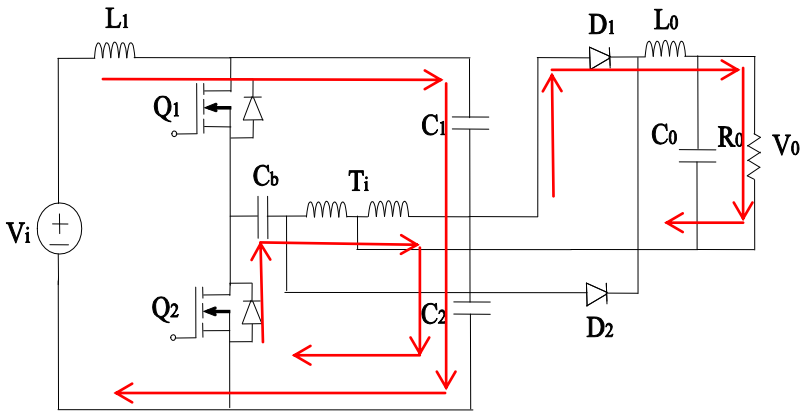


Fig. 2.20 (b) Modes of Operation: Mode II ($t_1 - t_2$)

Mode 3 (t_2-t_3) : This mode starts with switch Q_2 turned-on under ZVS. This mode will come to end when the part of tapped inductor connected to load, has completely discharged its energy to the load. At the end of this mode, C_b charged up to C_{b2} opposite to that of its initial value.

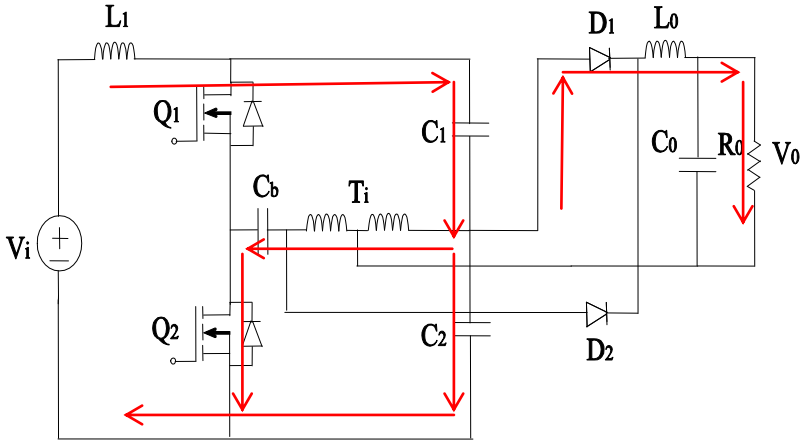


Fig. 2.20 (c) Modes of Operation: Mode III ($t_2 - t_3$)

Mode 4 (t_3-t_4) : At $t = t_3$, the rectifier diode D_1 will be off and from the other part of the tapped inductor energy will transfer to load through D_2. The tapped inductor forced the diode D_2 conduct under ZVS and the diode D_1 stops conducting any more. This ensures the continuous flow of current at the output. At the end of the mode, the body diode of the switch

Q_1 is turned on due to the energy transferring property of the inductor in the same direction in which it get charged.

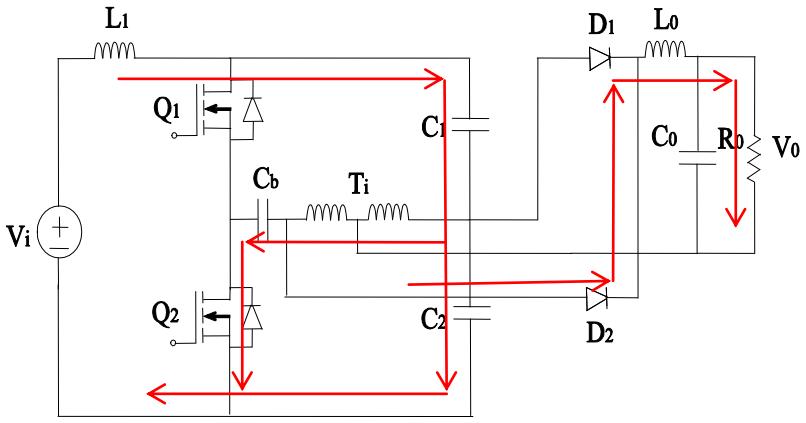


Fig. 2.20 (d) Modes of Operation: Mode IV ($t_3 - t_4$)

Mode 5 (t_4-t_5) : The rectified diode D_2 will start to conduct. The body diode of the switch Q_1 is turned on due to the energy transferring property of the inductor in the same direction in which it get charged. In the next mode, the gate pulse Q_1 is turned on under ZVS.

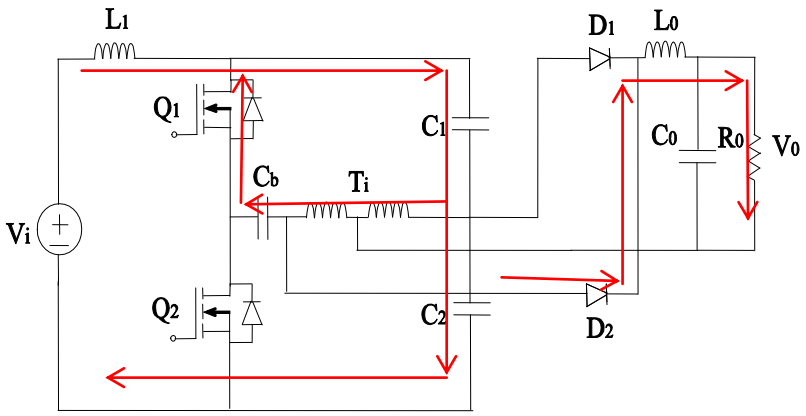


Fig. 2.20 (e) Modes of Operation: Mode V ($t_4 - t_5$)

2.11 Simulation results

Considering the limited practical utility of TI and many disadvantages of TI such as ringing between the leakage inductance of the inductor and the parasitic capacitances causes

higher voltage stresses across switching devices and developed EMI problems, we have only verified performance with simulation results.

The validity and performance of the proposed converter is simulated with the theoretical concept. The 10 W 12 V/3.3 V converter is chosen for the investigations. The proposed converter parameters are: Ro=0.8 Ω, L_1=10 µH, C_1 = C_2 = C_b = 3 µF, L_{TI} = 3 µH, switching frequency = 1 MHz.

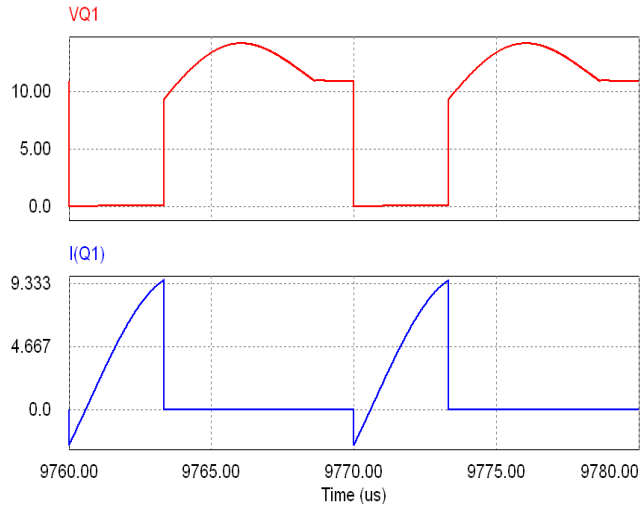


Fig. 2.21 (a) Simulated voltage and current waveforms of switch Q_1: V_{Q1} in Volts and I_{Q1} in Amps

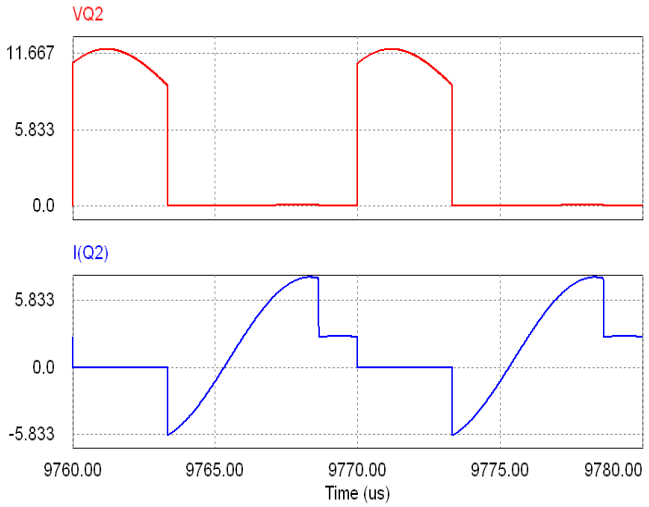


Fig. 2.21 (b) Simulated voltage and current waveforms of switch Q_2: V_{Q2} in Volts and I_{Q2} in Amps

The simulated converter delivers a load of 10 W with efficiency of 95.2 %. The simulated waveforms shown by Figs. 2.21 (a) and 2.21 (b), are obtained by using PSIM 7.1. From the simulated waveform, it can be seen that both switches are turned on and turned off ZVS and ZCS.

2.12 Summary

The proposed TI converter is presented to verify the improved efficiency employing clamp capacitor scheme. From simulation results it is concluded that TI converter have more advantages as compared to isolated buck converters. They have a ripple free input current and output currents yielding better power quality. Peak current is controlled by tapped inductor, so switching and conduction losses are minimized. The frequency dependent losses is less in TI converter as it is suitable for wide frequency range. Switches are turned on under ZVS due to clamping capacitors and turned off under ZCS due to tapped inductor, which results maximum power utilizations.

CHAPTER 3

APPLICATION OF ZVT TO SYNCHRONOUS BUCK CONVERTER WITH ACTIVE AUXILIARY CIRCUIT

Topology description

Modes of Operation

Design Procedure

Simulation and Experimental Results

Efficiency curve

Summary

Chapter 3. Application of ZVT to synchronous buck converter with active auxiliary circuit

This chapter proposes a ZVT-PWM synchronous buck converter, which is designed to operate at a low output voltage and at the high efficiency which typically required for portable systems. A synchronous converter is an obvious choice to make the dc-dc converter efficient at lower voltage because of the lower conduction loss in the diode. The high-side MOSFET is dominated by the switching losses and it is eliminated by the soft switching technique. Additionally, the designed resonant auxiliary circuit is also devoid of the switching losses. The suggested procedure ensures an efficient converter. Theoretical analysis, computer simulation, and experimental results are presented to explain the proposed schemes.

The next generation of portable products such as: personal communicators and digital assistants have demanded improvements in dc-dc converter topology in order to increase the battery life time and to enable smaller, cheaper systems. Since many portable devices operate in low-power standby modes for a majority of the time they are on, increasing light load converter efficiency can significantly increase battery lifetime. For low output voltage operations synchronous rectifier is the most appropriate candidate for future microprocessors and memory chips. The synchronous rectifier buck converter is popular for low-voltage power conversion because of its high efficiency and reduced area consumption [1, 64, 108, 112, 125]. A synchronous rectifier is an electronic switch that improves the power-conversion efficiency by placing a low-resistance conduction path across the diode rectifier in a switch-mode regulator. MOSFETs usually serve this purpose.

However, higher input voltages and lower output voltages have brought about very low duty cycles, increasing switching losses and decreasing conversion efficiency. So in this chapter, we have optimized the efficiency of the synchronous buck converter by reducing

switching losses using soft switching techniques. The voltage-mode soft-switching method that has attracted most interest in recent years is the zero voltage transition [23, 72, 74, 76, 107, 109-111, 113-122, 123-124, 126-127, and 129-130].

This is because of its low additional conduction losses and its operation is closest to the PWM converters. The auxiliary circuit of the ZVT converters is activated just before the main switch is turned on and ceases after it is accomplished. The auxiliary circuit components in this circuit have lower ratings than those in the main power circuit because the auxiliary circuit is active for only a fraction of the switching cycle; this allows a device that can turn on with least switching losses than the main switch to be used as the auxiliary switch. The improvement in efficiency caused by the auxiliary circuit is mainly due to the difference in switching losses between the auxiliary switch and the main power switch if it were to operate without the help of the auxiliary circuit.

Previously proposed ZVT-PWM converters have at least one of the following key drawbacks.

1) The auxiliary switch is turned off while it is conducting current. This causes switching losses and EMI to appear that offsets the benefits of the using the auxiliary circuit. In converters such as the ones proposed in [76, 113, 116-117], the turn off is very hard.

2) The auxiliary circuit causes the main converter switch to operate with a higher peak current stress and with more circulating current. This results in the need for a higher current-rated device for the main switch, and in an increase of conduction losses. The converters proposed in [1, 72, 74, 108, 114, 118] would have current stresses those are very high on the main switch.

3) The auxiliary circuit components for converters proposed in [76, 107, 115, 118] have high voltage and/or current stresses. The converter proposed in [124, 128] reduces the current

stress on the main switch, but its circuit is very complex. Reducing switching losses for low power circuits such as a synchronous buck is not known to be present in the literature [1, 23, 64, 74, 76, 107-124, 126-128].

This chapter is organized as follows: Section 3. 1 gives a short description of the proposed topology. In section 3.2, its principle of operations is described. Section 3.3 presents some design considerations. Section 3.4 includes simulation and experimental results to illustrate the features of the proposed converter scheme. In Section 3.5, the efficiency curve, which proves the application of the converter over a wide load range is shown. Finally important features are summarized in Section 3.6.

3.1 Topology description

The circuit scheme of the proposed ZVT synchronous buck converter is shown in Fig. 3.1. The auxiliary circuit consists of switch S_1, resonant capacitor C_r, resonant inductor L_r. The auxiliary circuit operates only during a short switching transition time to create ZVS conditions for the main switch. The body diode of the main switch is also utilized in the converter. A high frequency schottky diode D_S is used for discharging the capacitor voltage to the output, which happens before the turn on of the synchronous switch. By using a resonant auxiliary network in parallel with the main switch, the proposed converters achieve zero-voltage switching for the main switch and for the synchronous switch; and zero-current switching for the auxiliary switch without increasing their voltage and current stresses.

During one switching cycle, the following assumptions are made in order to simplify the steady-state analysis of the circuit shown in Fig. 3.1.

1. the input voltage V_i is constant.

2. the output voltage V_o is constant or output capacitor C_o is large enough.

3. the output current I_o is constant or output inductor L_o is large enough.

4. the output Inductor L_o is much larger than resonant circuit inductor L_r.

5. the resonant circuits are ideal.

6. the semiconductor devices are ideal.

7. the reverse recovery time of all diodes is ignored.

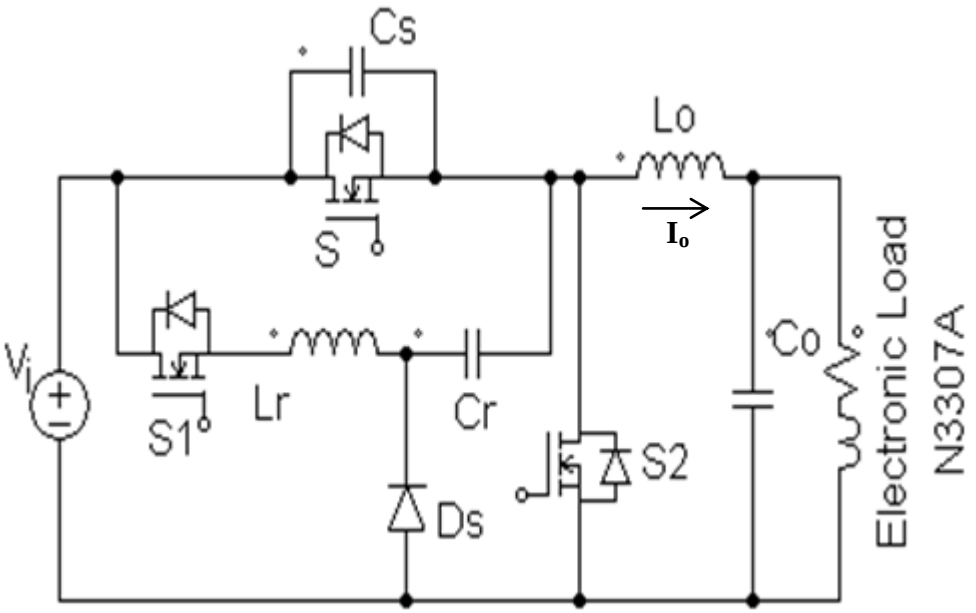


Fig. 3.1 Proposed ZVT SBC

3.2 Modes of Operation

Eight stages take place in the steady-state operation during one switching cycle in the proposed converter. The key waveforms of these stages are given in Fig. 3.2 and the equivalent circuit schemes of the operation stages are given in Fig. 3.3. The detailed analysis of every stage is presented below:

Mode 1 (t_0, t_1): Prior to $t = t_0$, the body diode of S_2 was conducting; the main switch S and the auxiliary switch S_1 are turned off. At t_0, the auxiliary switch S_1 is turned on which realizes

zero-current turn-on as it is in series with the resonant inductor L_r. The current through the resonant inductor L_r and the resonant capacitor C_r rise at the same rate as fall of current i_{S2} through body diode of S_2. The resonance occurs between L_r and C_r during this mode. The mode ends at $t = t_1$, when i_{Lr} reaches I_o and i_{S2} falls to zero and as a result, the body diode of S_2 stops conducting. The voltage and current expressions which govern this circuit mode are given by:

$$i_{S2} = I_o - i_{Lr} \tag{3.1}$$

$$i_{Lr}(t - t_0) = \frac{V_i}{Z} Sin\omega(t - t_0) \tag{3.2}$$

where

$\omega = \frac{1}{\sqrt{L_r C_r}}$ is the resonant frequency

$Z = \sqrt{L_r / C_r}$ is the characteristic impedance

V_i is the input voltage of converter

$$t_{01} = t_1 - t_0 = \frac{1}{\omega} Sin^{-1}\left(\frac{I_o Z}{V_i}\right) \tag{3.3}$$

At $t = t_1$

$$V_{Cr}(t_1 - t_0) = V_{Cr1} \tag{3.4}$$

$$i_{Lr}(t_1 - t_0) = I_o \tag{3.5}$$

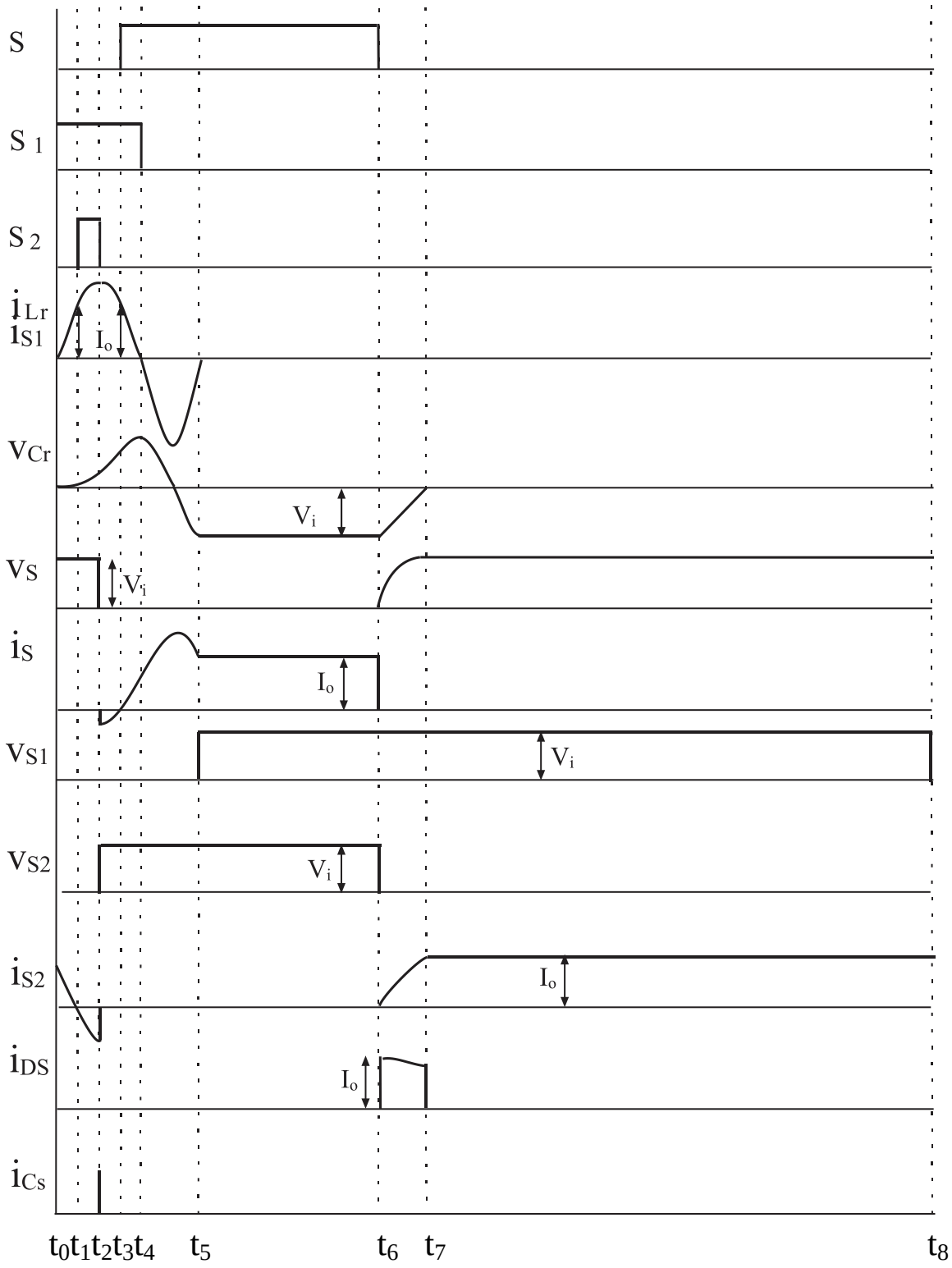


Fig. 3.2 Key theoretical waveforms concerning the operation stages in the ZVT SBC

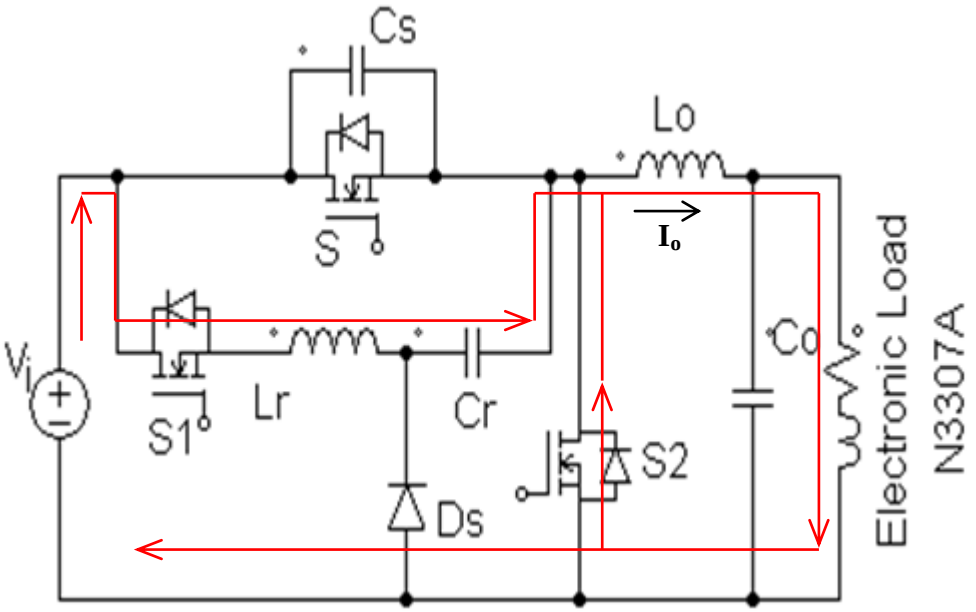


Fig. 3.3 (a) Modes of Operation: Mode 1 (t_0-t_1)

Mode 2 (t_1, t_2): L_r and C_r continue to resonate. At t_1, the synchronous switch S_2 is turned on under ZVS. This mode is made to end by turning off the switch S_2 under ZVS, when i_{Lr} current reaches to it maximum value i.e. i_{Lrmax}.

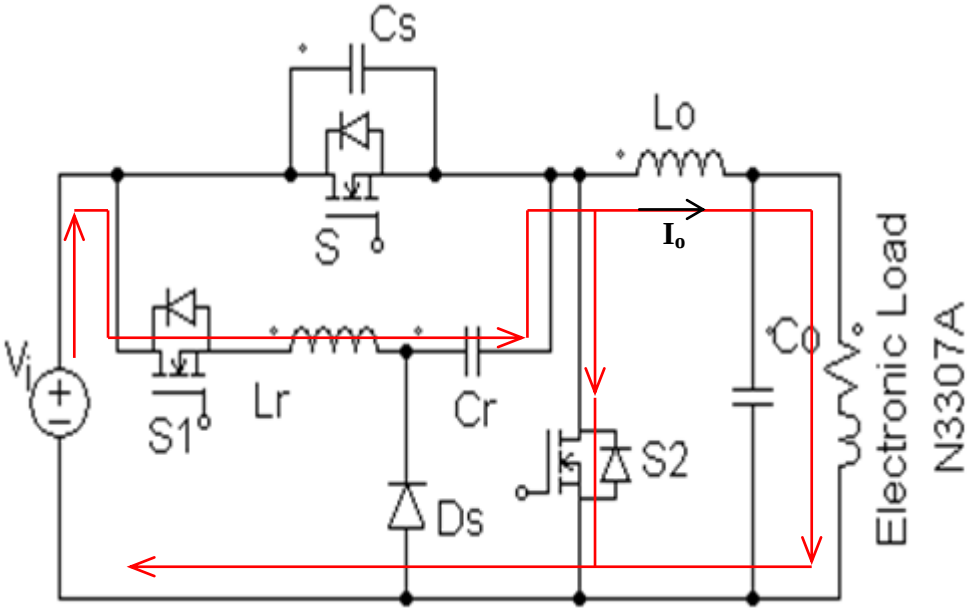


Fig. 3.3 (b) Modes of Operation: Mode 2 (t_1-t_2)

$$i_{S2} = i_{Lr} - I_o \tag{3.6}$$

$$i_{Lr}(t-t_1)=\frac{V_i-V_{Cr1}}{Z}Sin\omega(t-t_1)+I_oCos\omega(t-t_1) \tag{3.7}$$

where V_{Cr1} is the voltage across capacitor C_r at $t = t_1$

At $t = t_2$

$$i_{Lr}(t_2-t_1)=I_{Lr\max} \tag{3.8}$$

$$t_{12}=\frac{1}{\omega}\tan^{-1}\left(\frac{V_i-V_{Cr1}}{I_0Z}\right) \tag{3.9}$$

$$V_{Cr}(t_2-t_1)=V_{Cr2} \tag{3.10}$$

Mode 3 (t_2, t_3): At t_2, i_{Lr} reaches its peak value i_{Lrmax}. Since i_{Lr} is more than the load current I_o, the capacitor C_S will be charged and discharge through the body diode of the main switch S, which leads to the conduction of the body diode. This mode ends when the resonant current i_{Lr} falls to the load current I_o. So the current through the body diode of the main switch S becomes zero which results to the turned off of the body diode. At the same time, the main switch S is turned on under ZVS. The voltage and current expressions for this mode are:

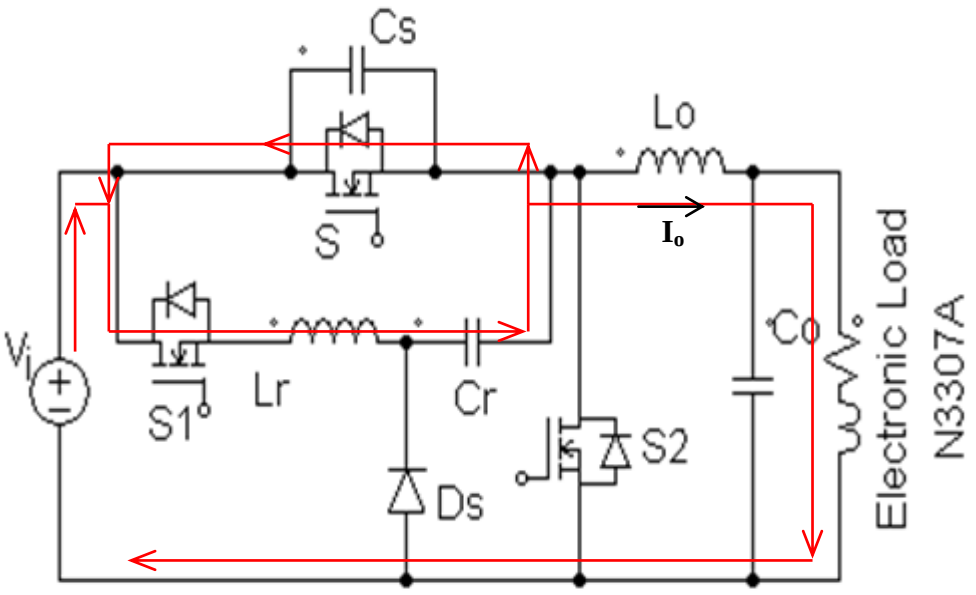


Fig. 3.3 (c) Modes of Operation: Mode 3 (t_2-t_3)

$$i_{Lr}(t-t_2) = -\frac{V_{Cr2}}{Z} Sin\omega(t-t_2) + I_{Lr\max} Cos\omega(t-t_2) \quad (3.11)$$

$$t_{23} = \frac{1}{\omega}\left[\tan^{-1}\left(\frac{I_{Lr\max} Z}{V_{Cr2}}\right) - Sin^{-1}(I_o)\right] \quad (3.12)$$

At $t = t_3$

$$i_{Lr}(t_{23}) = I_o \quad (3.13)$$

$$V_{Cr}(t_{23}) = V_{Cr3} \quad (3.14)$$

Mode 4 (t_3 t_4): At t_3, the main switch is turned-on with ZVS. During this stage the growth rate of i_S, is determined by the resonance between L_r and C_r. The resonant process continues in this mode and the current i_{Lr} continue to decrease. This mode ends when i_{Lr} falls to zero and S_1 can be turned-off with ZCS. The voltage and current expressions for this mode are:

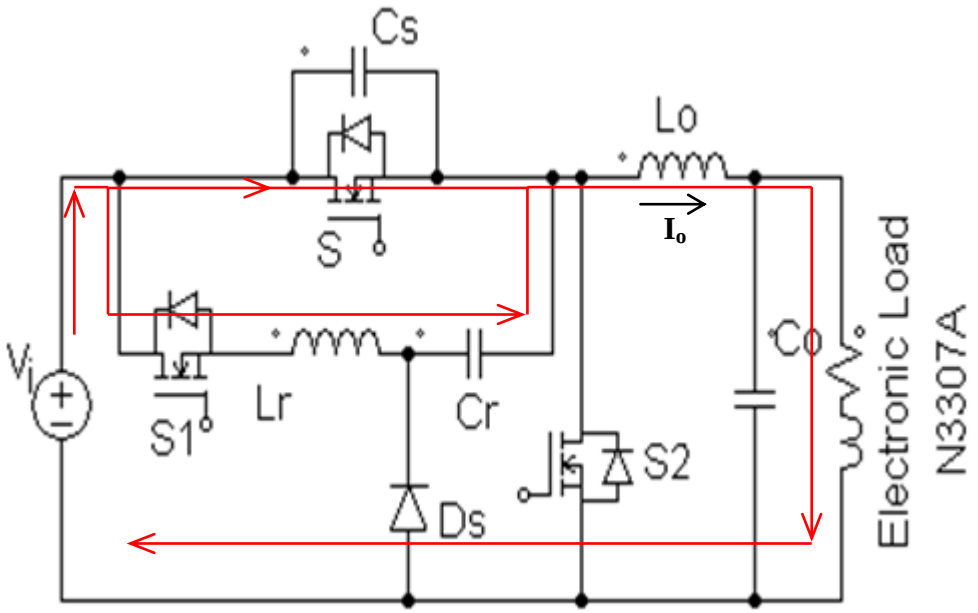


Fig. 3.3 (d) Modes of Operation: Mode 4 (t_3-t_4)

$$i_{Lr}(t-t_3) = -\frac{V_{Cr3}}{Z} Sin\omega(t-t_3) + I_o Cos\omega(t-t_3) \quad (3.15)$$

At $t = t_4$

$$i_{Lr} = 0 \quad (3.16)$$

$$t_{34} = \tan^{-1}\left(\frac{I_o Z}{V_{Cr3}}\right) \tag{3.17}$$

$$V_{Cr}(t_4) = V_{Cr\max} \tag{3.18}$$

Mode 5 (t_4 t_5): At t_4, the auxiliary switch S_1 is turned-off with ZCS. The body diode of S_1 begins to conduct due to resonant capacitor C_r which starts to discharge. The resonant current i_{Lr} rises in the reverse direction, reaches a maximum negative and increases to zero. At this moment the body diode of S_1 is turned off and the mode ends. The voltage and current equations for this mode are given by:

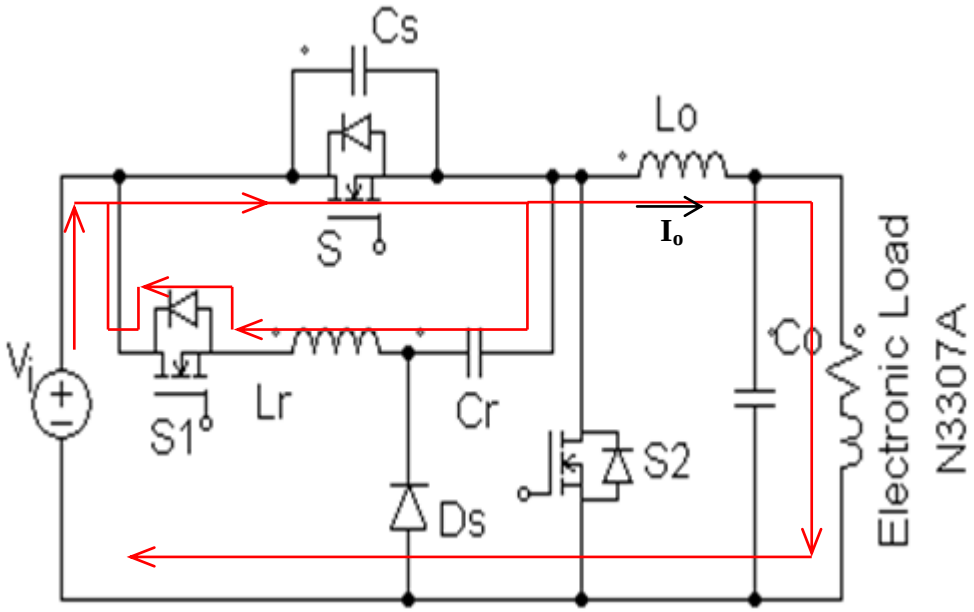


Fig. 3.3 (e) Modes of Operation: Mode 5 (t_4-t_5)

$$i_{Lr}(t - t_4) = \frac{V_{Cr\max}}{Z} Sin\omega(t - t_4) \tag{3.19}$$

At $t = t_5$

$$i_{Lr}(t_5) = 0 \tag{3.20}$$

$$t_{45} = \frac{\pi}{\omega} \tag{3.21}$$

$$V_{Cr}(t_5) = -V_{Cr4} \tag{3.22}$$

Mode 6 (t_5, t_6): Since the body diode of S_1 has turned off at t_5, now only the main switch S carries the load current. There is no resonance in this mode and the circuit operation is identical to a conventional PWM buck converter. The voltage and current equations for this mode are given by:

$$i_S = I_o \tag{3.23}$$

$$i_{Lr}(t_6) = 0 \tag{3.24}$$

$$V_{Cr}(t_6) = -V_{Cr4} \tag{3.25}$$

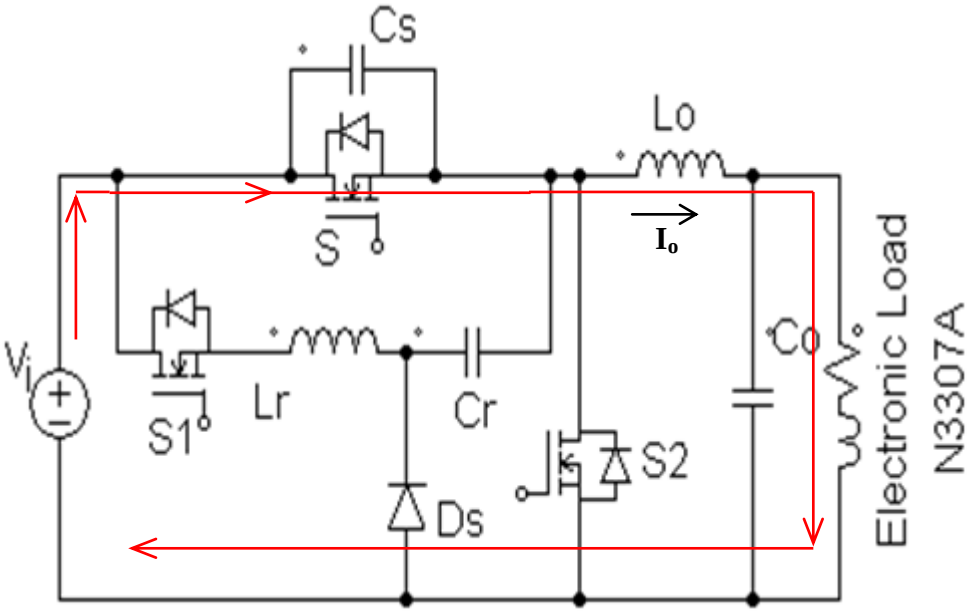


Fig. 3.3 (f) Modes of Operation: Mode 6 (t_5-t_6)

Mode 7 (t_6, t_7): At t_6, the main switch S is turned off with ZVS. The schottky diode D_S starts to conduct. The resonant energy stored in the capacitor C_r starts discharging to the load through the high frequency schottky diode D_S for a very short period of time, hence body – diode conduction losses and drop in output voltage is too low. This mode finishes when C_r is fully discharged. The equations that define this mode are given by:

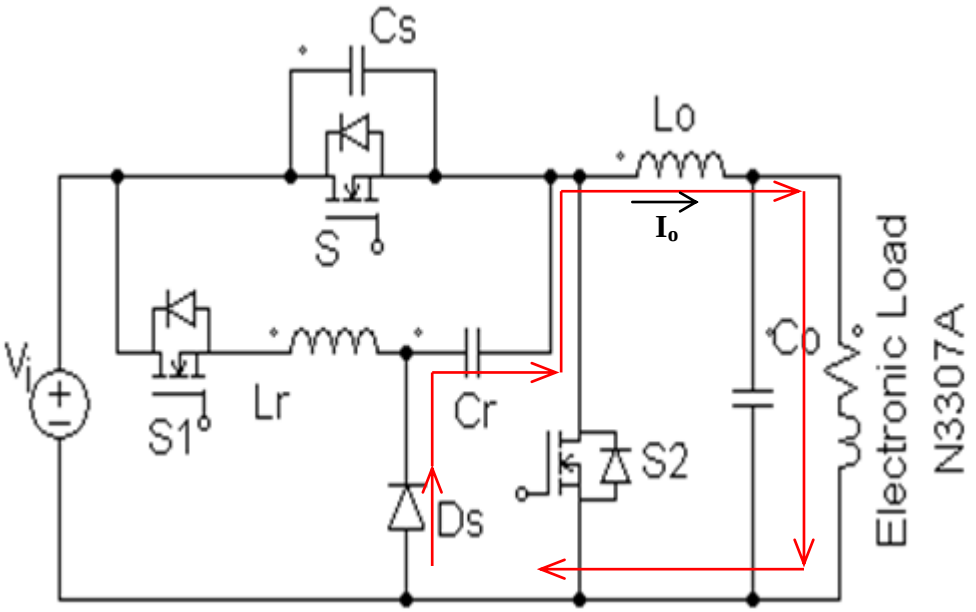


Fig. 3.3 (g) Modes of Operation: Mode 7 (t_6-t_7)

$$V_{Cr}(t-t_6) = -V_{Cr4} + \frac{I_o}{C_r}(t-t_6) \tag{3.26}$$

At t = t_7

$$V_{Cr}(t_7) = 0 \tag{3.27}$$

$$t_{67} = \frac{C_r V_{Cr4}}{I_0} \tag{3.28}$$

Mode 8 (t_7, t_8): At t_7, the body diode of switch S_2 is on as soon as C_r is fully discharged and schottky diode is turned off under ZVS. Dead time loss is negligibly small compared to the conventional synchronous buck converter. During this mode, the converter operates like a conventional PWM buck converter until the switch S_1 is turned on in the next switching cycle. The equation that defines this mode is given by:

$$i_{S2} = I_o \tag{3.29}$$

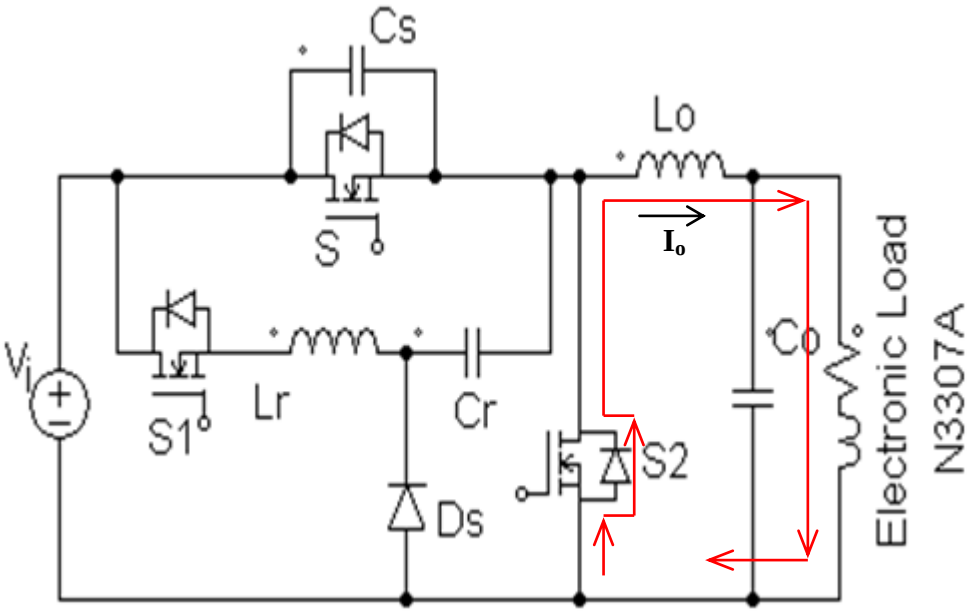


Fig. 3.3 (h) Modes of Operation: Mode 8 (t_7-t_8)

3.3 Design Procedure

The design of conventional PWM converters has been well presented in literature [110]. Thus it is more significant to focus on the design procedures of the auxiliary circuit. The resonant inductor, the resonant capacitor, and the delay time of the auxiliary switch are the most important components while designing the auxiliary circuit. The proposed auxiliary resonant circuit provides soft switching conditions for the main transistor. The following design procedure is developed considering procedures such as those presented previously [110].

3.3.1 Delay time

The on time of auxiliary switch (S_1) must be shorter than one tenth of the switching period.

$$T_D = \frac{1}{10} T_S \tag{3.30}$$

Where

T_D = Delay time introduced due to turn-on time of auxiliary switch

T_S = Switching time period = $1/f_{SW}$

f_{SW} = Switching frequency

3.3.2 Current Stress Factor (a)

The current stress factor of the auxiliary switch is defined as

$$a = \frac{I_{Lrm}}{I_{in(\max)}} \tag{3.31}$$

It is greater than 1 $(1 \le a \le 1.5)$ and is desired to be as small as possible. This factor can be used for the selection of the auxiliary switch.

3.3.3 Resonant Capacitor (C_r)

The resonant capacitor can be expressed as

$$C_r = \frac{(a-1)^2 I_{in(\max)} T_D}{V_{out}\left[1+\frac{\pi}{2}(a-1)\right]} \tag{3.32}$$

where 'a' = current stress factor

T_D = Delay time derived in equation (3.30)

I_{inmax} = Maximum input current

3.3.4 Resonant Inductor (L_r)

The resonant inductor is given by

$$L_r = \frac{V_{out} T_D}{I_{in(\max)}\left[1+\frac{\pi}{2}(a-1)\right]} \tag{3.33}$$

3.3.5 MOSFET Selection

A method to choose the MOSFETs for the converter is to compare the power dissipation values for a number of different MOSFET types. Usually, a low on-state drain resistance MOSFET is chosen for the synchronous rectifier, and a MOSFET with a low gate charge is chosen for the switches.

3.4 Simulation and Experimental Results

A prototype of the proposed converter, as shown in Fig. 3.1 has been built in the laboratory. The proposed converter operates with an input voltage V_i = 12 V, an output voltage V_o = 3.3 V, a load current of 10 A and a switching frequency of 200 kHz. The converter is simulated using PSIM 7.1. The major parameters and components are given in Table 3.1. Figs. 3.4 (a-d) show the simulation results of the proposed converter and Figs. 3.5 (a-d) present the experimental results. Fig. 3.6 shows the photograph of the fabricated proposed converter.

Table 3.1: Components used in the
Proposed SBC with active auxiliary circuit

Component	Value/Model	
	Simulation	Experiment
Main Switch, S	Ideal	IRF1312
Auxiliary Switch, S_1	Ideal	IRF1010E
Synchronous Switch, S_2	Ideal	IRF1010E
Schottky Diode, D	Ideal	MBR60L45CTG
Capacitance, C_S	0.05 nH	0.05 nH
Resonant Inductor, L_r	200 nH	200 nH
Resonant Capacitor, C_r	0.2 μF	0.2 μF
Output Capacitor, C_o	100 μF	100 μF
Output Inductor, L_o	2 μH	2 μH

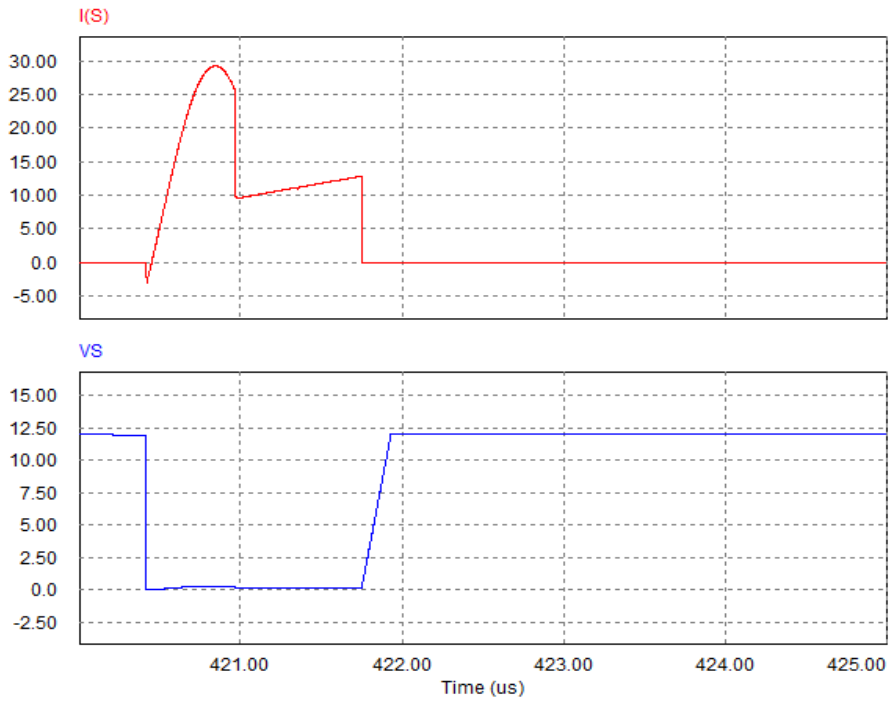


Fig. 3.4 (a) Simulated voltage and current waveforms of main switch S: V_S in Volts; I_S in Amps

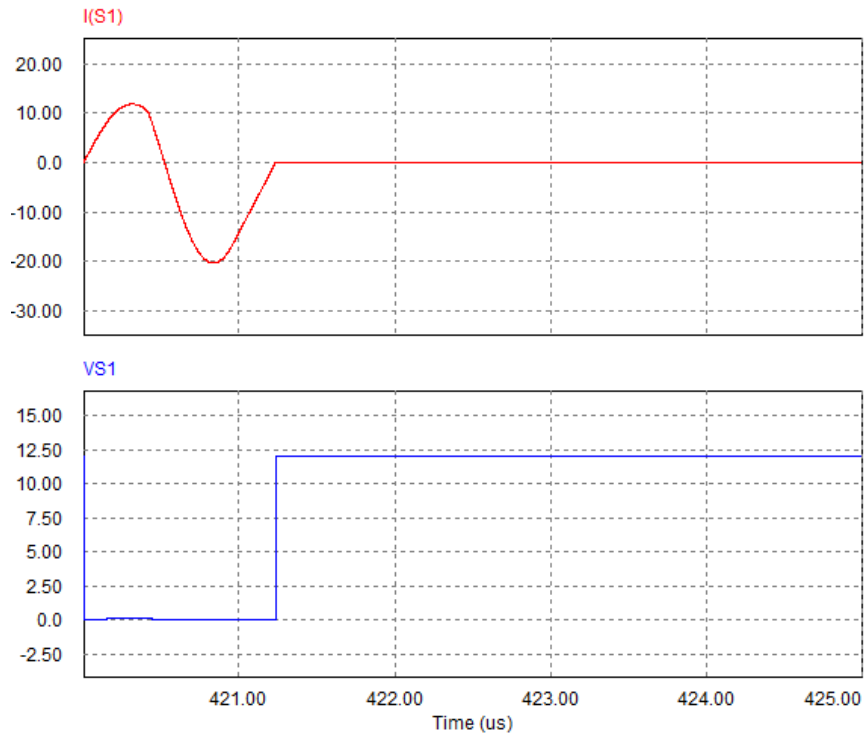


Fig. 3.4 (b) Simulated voltage and current waveforms of auxiliary switch S1: V_{S1} in Volts; I_{S1} in Amps

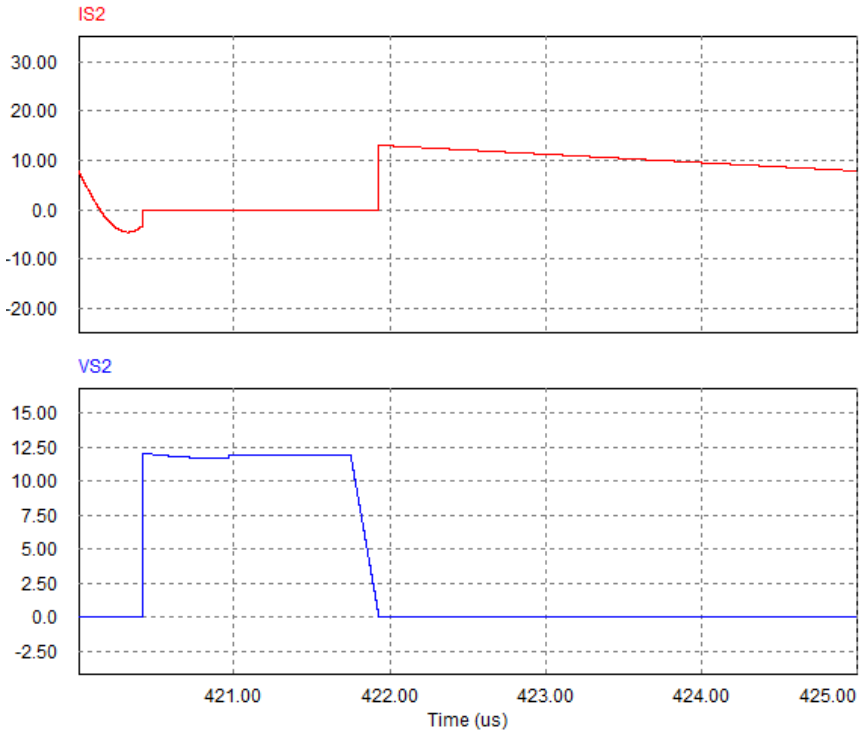


Fig. 3.4 (c) Simulated voltage and current waveforms of synchronous switch S2: V_{S2} in Volts; I_{S2} in Amps

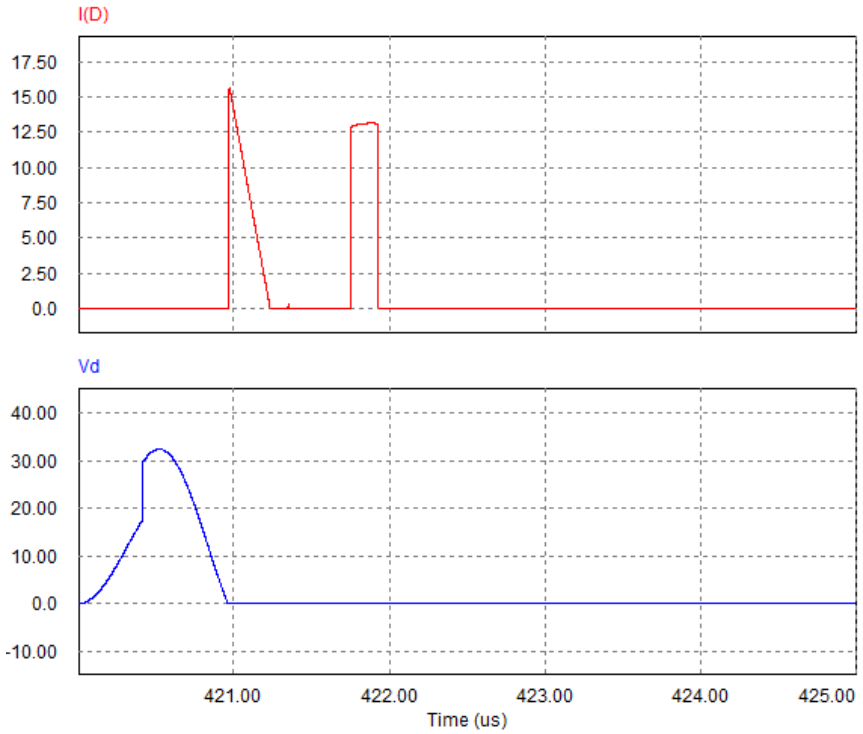


Fig. 3.4 (d) Simulated voltage and current waveforms of schottky diode DS: V_{DS} in Volts; I_{DS} in Amps

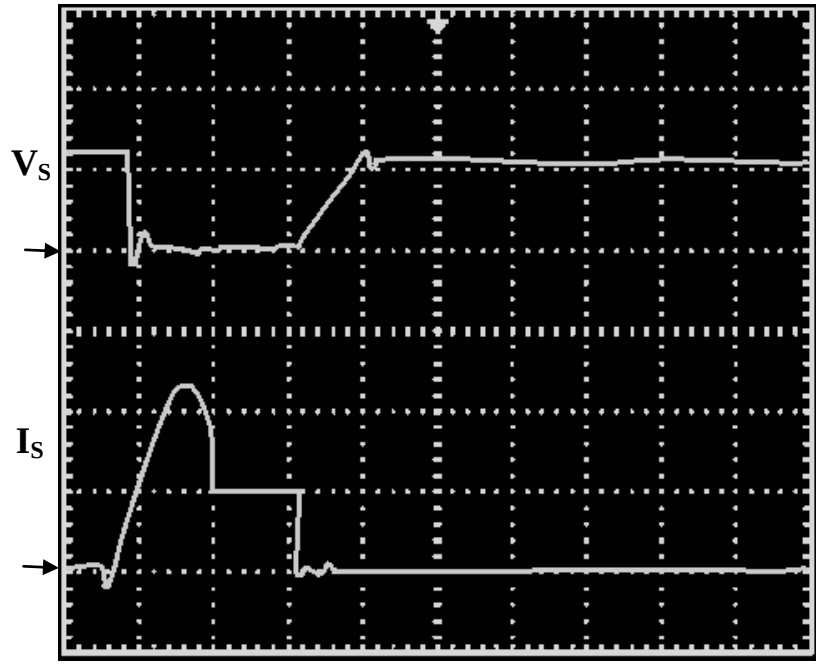


Fig. 3.5 (a) Experimental voltage and current waveforms of main switch S: V_S; I_S: (V: 10 V/div, I: 10 A/div, time: 0. 5 μs/div)

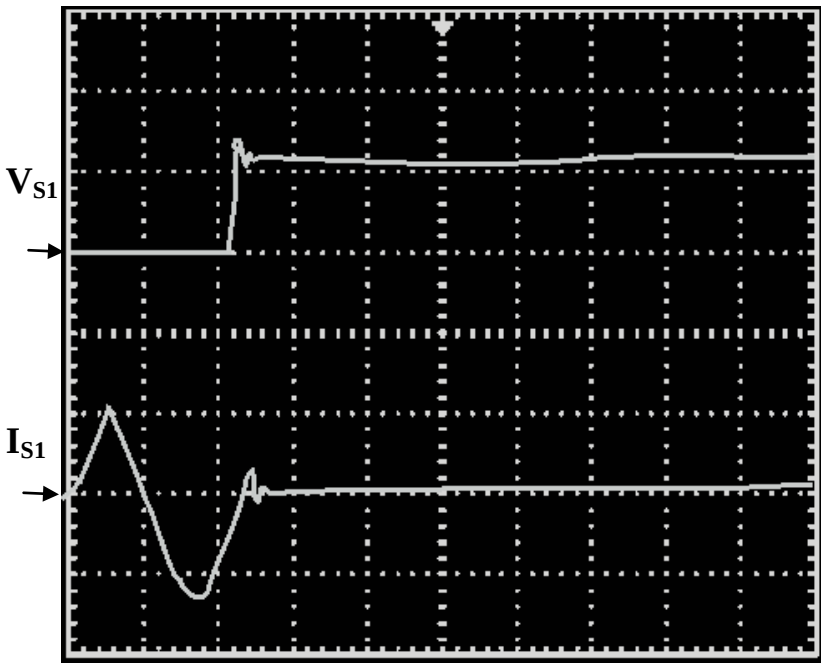


Fig. 3.5 (b) Experimental voltage and current waveforms of auxiliary switch S_1: V_{S1}; I_{S1}: (V: 10 V/div, I: 10 A/div, time: 0. 5 μs/div)

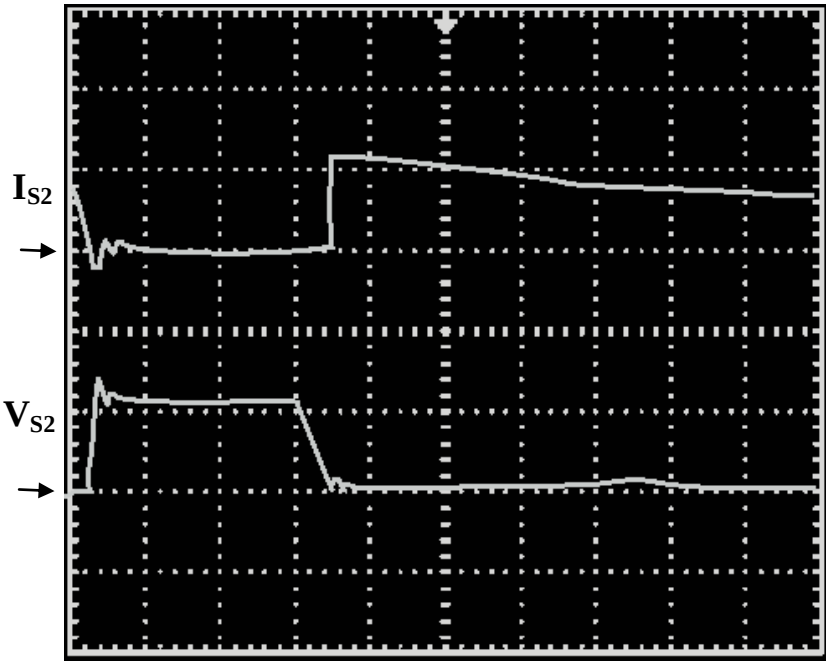


Fig. 3.5 (c) Experimental voltage and current waveforms of synchronous switch S_2: V_{S2}; I_{S2}: (V: 10 V/div, I: 10 A/div, time: 0. 5 μs/div)

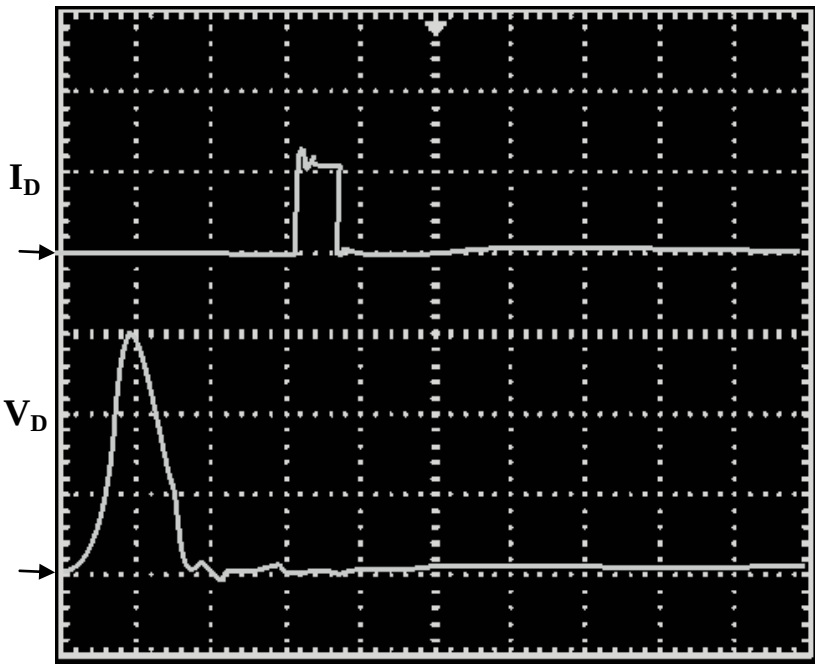


Fig. 3.5 (d) Experimental voltage and current waveforms of schottky diode D: V_D; I_D: (V: 10 V/div, I: 10 A/div, time: 0. 5 μs/div)

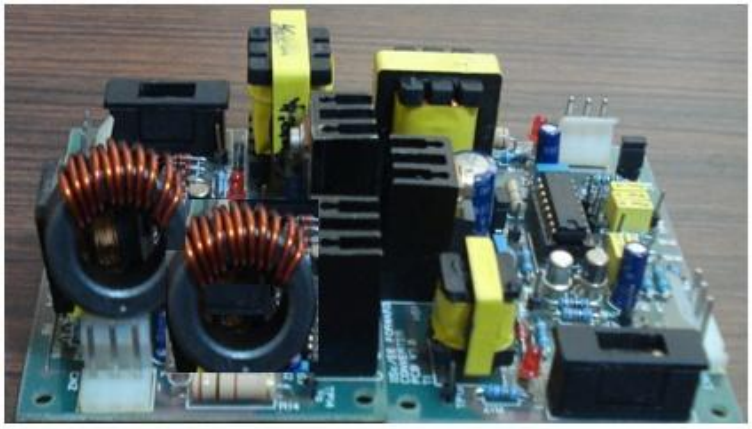


Fig. 3.6 Photograph of proposed ZVT synchronous buck converter

3.4.1 Main Switch S

It is noted from Figs. (3.4 a & 3.5 a) that the main switch S is turned on under ZVS, when voltage across C_S is zero. The converter has not exceeded the voltage limits; however the current stress is slightly higher for a very short period of time. The main switch also switches off under ZVS. The current and voltage waveforms obtained through simulation and experimental investigations are in close agreement with the theoretical analysis.

3.4.2 Auxiliary Switch S_1

It is noted from Figs. (3.4 b & 3.5 b) that auxiliary switch S_1 also operates with soft switching. The switch S_1 is turned on under ZCS because of the inductor L_r and turns off under ZCS when resonant current through L_r and C_r falls to zero. Its body diode also turns on as soon as S_1 is off at zero current and turns off when the resonant current is zero. The auxiliary switch is active only for a short period of time, which is verified by its conduction period and it is too small. Also, the current and voltage stresses are well within the operating limits.

3.4.3 Synchronous switch S_2

The synchronous switch is turned on under ZVS when C_r has completely discharged and also turns off under ZVS, which can be observed from Figs. (3.4 c & 3.5 c). The synchronous switch also has characteristics similar to the switches S and S_1. They operate within the safe limits and it can be noted here that the conduction period of S_2 is more confining to the design values and it operates at a low power when compared to the other switches.

3.4.4 Schottky Diode D_S

The schottky diode works for a very short period to discharge the resonant capacitor C_r as can be observed from Figs. (3.4 d & 3.5 d). The schottky diode also turns on and turns off under ZVS. A high-frequency schottky diode which is available at high-current, low voltages can be used. The conduction of the schottky diodes may cause a considerable drop in output voltage for low power circuits but due to the advancement in semiconductor techniques, schottky diodes are also now available with a low forward voltage drop for high frequency circuits.

3.5 Efficiency curve

From Fig. 3.7, it can be observed that the efficiency values of the soft switching converter are relatively high with respect to those of the hard switching converter. The efficiency values towards the minimum output power decrease naturally because the converter is designed for the maximum output current. At 70% output power, the overall efficiency of the proposed converter increases to about 97% from the value of 92% in its counterpart hard switching converter. The high efficiency concludes the correctness of the design values.

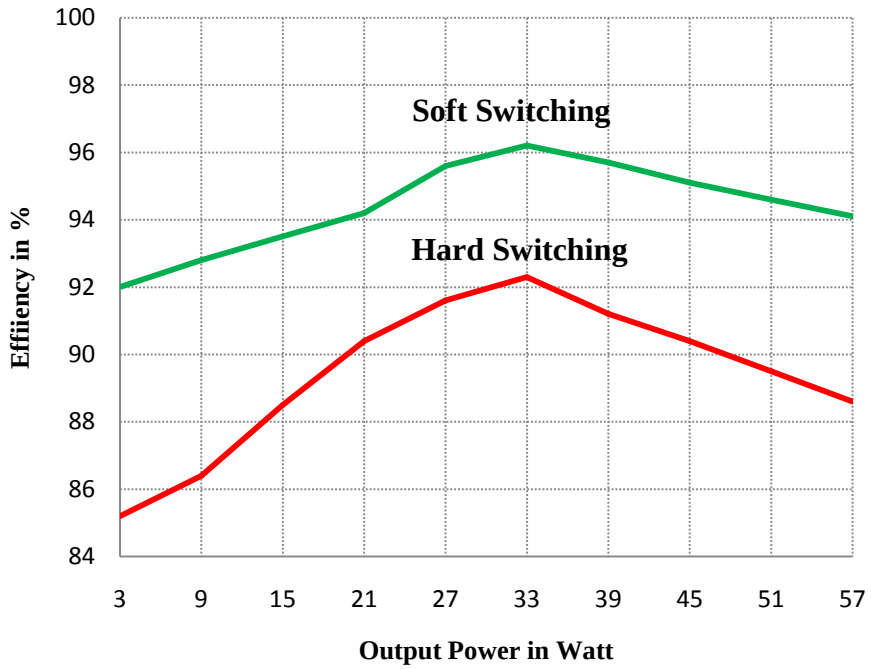


Fig. 3.7 Converter efficiency versus output power

3.6 Summary

The concepts of ZVT used in high power were implemented in a synchronous buck converter and it was shown that the switching losses in this converter were reduced. The main switch and the synchronous switch are turned-on and turned-off with ZVS. Thus, the auxiliary switch undergoes ZCS switching. Thus all of the active and passive semiconductor devices are turned on and off under exact ZVS and/or ZCS. Hence switching losses are reduced and the newly proposed ZVT synchronous buck is more efficient than the conventional converter. Efficiency is computed by experiment results. An efficiency graph shows the wide load range applicability of the converter. The additional voltage and current stresses on the main devices do not take place, and the auxiliary devices are subjected to allowable voltage and current values. Moreover, the converter has a simple structure, and is easy to control. A prototype of a 3.3 V, 10 A, 200 kHz system was implemented to experimentally verify the improved performance.

CHAPTER 4

APPLICATION OF ZVT TO SYNCHRONOUS BUCK CONVERTER WITH PASSIVE AUXILIARY CIRCUIT

Topology description

Operating Principles and analysis

Design procedure

Simulation and experimental results

Efficiency curve

Summary

Chapter 4. Application of ZVT to synchronous buck converter with passive auxiliary circuit

The previous chapter discussed the soft switching implementation in a synchronous buck converter (SBC) with an active auxiliary circuit for reduction of switching losses. Although, this soft switching technique improves the performance, but it requires an additional active switch and makes control relatively complex. Further it increases the cost and reduces the reliability of an extent. A relatively simple snubber circuit consisting of a diode, an inductor and a capacitor can overcome the drawbacks of the active auxiliary circuit.

Passive snubbers are generally used to reduce switching losses. It provides allowable voltage and current stresses across semiconductor switches used in the converter. In the past, research works have been done on passive snubbers to increase the efficiency of the converter [1, 76, 121, 131-134]. In addition, it has been reported that the passive circuits are cheaper and more reliable, and had a higher performance/cost ratio than the active ones [74, 114, 118, 123-124, 135-137].

In this chapter, a simple passive snubber (PS) circuit is employed to achieve ZVT. The proposed circuit not only serves as an energy recovery turn-on snubber, which greatly reduces the reverse-recovery peak current of the diode and the turn-on loss of the switch, but also provides a zero-voltage or reduced voltage turn-off condition to the switch with extended operating range. Since it uses fewer circuit components, the circuit layout is simple.

This chapter is organized as follows: Section 4.1 presents the description of the circuit topology. The steady state analysis and modes of operations are discussed in Section 4.2. Design considerations for practicability of the proposed topology are illustrated in section 4.3. In Section 4.4, the simulation and experimental results are shown to prove the theoretical analysis. In Section 4.5, the efficiency curve is illustrated and proves the application of the

converter for a constant load current. Finally, important features are summarized in Section 4.6.

4.1 Topology description

The proposed converter is shown in Fig. 4.1. It utilizes a passive snubber to reduce the switching losses in ZVT SBC. Two buffer capacitors C_r and C_b with the three set of schottky diodes D_{S1}, D_{S2} and D_{S3} provide soft switching to main switch as well as to the synchronous switch. The diodes are also turned on and turned off under ZVS or/and ZCS. The PS further uses a resonant inductor L_r based energy regenerative circuit to recover the energy captured in the snubber capacitors. The resonant inductor L_r and the set of capacitors forms resonant conditions during the transition period of the switches and provide ZVT conditions to the main switch.

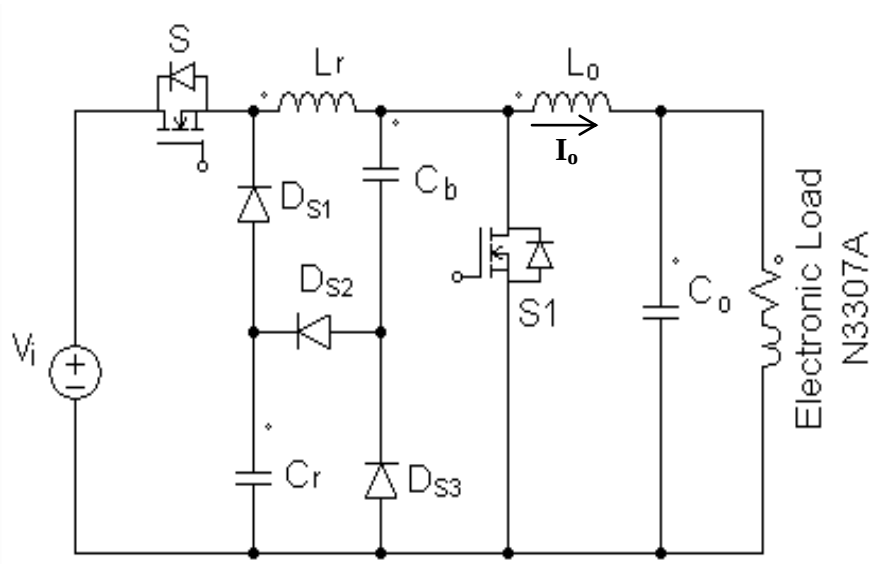


Fig. 4.1 The proposed PS SBC

4.2 Operating Principles and analysis

To analyze the steady-state operations of the proposed circuit, the following assumptions are made during one switching cycle.

1. the input voltage V_i is constant.

2. the output voltage V_o is constant or the output capacitor C_o is large enough.

3. the output current I_o is constant or the output inductor L_o is large enough.

4. the output Inductor L_o is much larger than the resonant circuit inductor L_r.

5. the resonant circuits are ideal.

6. the semiconductor devices are ideal.

7. the reverse recovery time of all diodes is ignored.

Based on these assumptions, circuit operations in one switching cycle can be divided into eight stages. The key waveforms of these stages are shown by Fig. 4.2 and the equivalent circuit schemes of the operation stages are illustrated by Fig. 4.3. The detailed analysis of every stage is presented below:

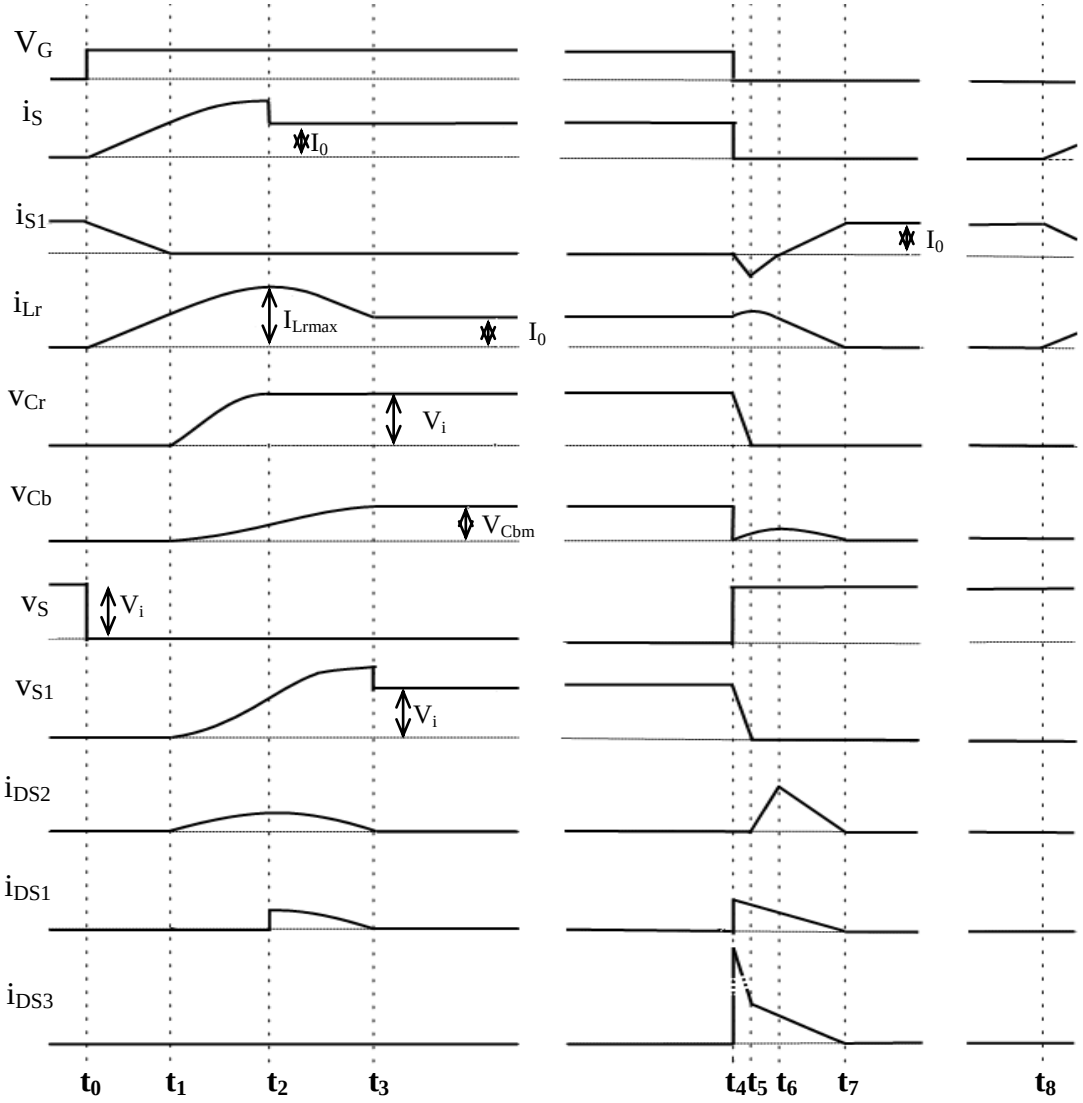


Fig. 4.2 Key theoretical waveforms of the proposed PS SBC

Mode 1 (t_0-t_1): Prior to t_0, the body diode of switch S_1 was conducting while the main switch S is off. The equations $i_S = 0$, $i_{D1} = I_o$, $i_{Lr} = 0$, $v_{Cr} = 0$, $v_{Cb} = 0$ are valid at the beginning of this stage. At $t = t_0$, the main switch is turned on, which realizes zero-current turn-on as it is in series with the resonant inductor L_r. During this stage, i_{Lr} rises and the current i_{D1} through the body diode of switch S_1 falls simultaneously at the same rate linearly. The mode ends at $t = t_1$ when i_{Lr} reaches I_0 and i_{D1} becomes zero. The body diode D_1 is turned off with ZVT because of capacitor C_r and C_b existent. In this state,

$$i_S = i_{Lr} = \frac{V_i}{L_r}(t - t_0)$$

(4.1) $$i_{D1} = I_o - i_{Lr} = -\frac{V_i}{L_r}(t - t_0) + I_o$$

(4.2)

In this state

$$t_{01} = \frac{L_r}{V_i} I_o \qquad (4.3)$$

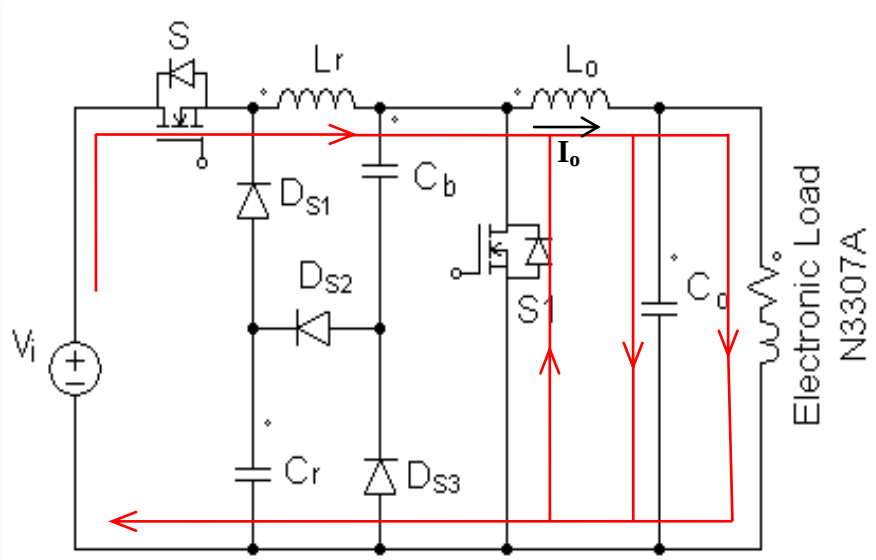


Fig. 4.3 (a) Converter Operation in Mode 1 ($t_0 - t_1$)

Mode 2 (t_1-t_2): The diode D_{S2} starts conducting at the instant when the body diode D_1 is turned off. At $t = t_1$, $i_S = i_{Lr} = I_o$, $i_{D1} = 0$, $v_{Cr} = 0$, and $v_{Cb} = 0$. In this interval, resonance occurs with the inductor L_r and capacitors C_r and C_b. This mode ends with C_r charged up to the input voltage V_i.

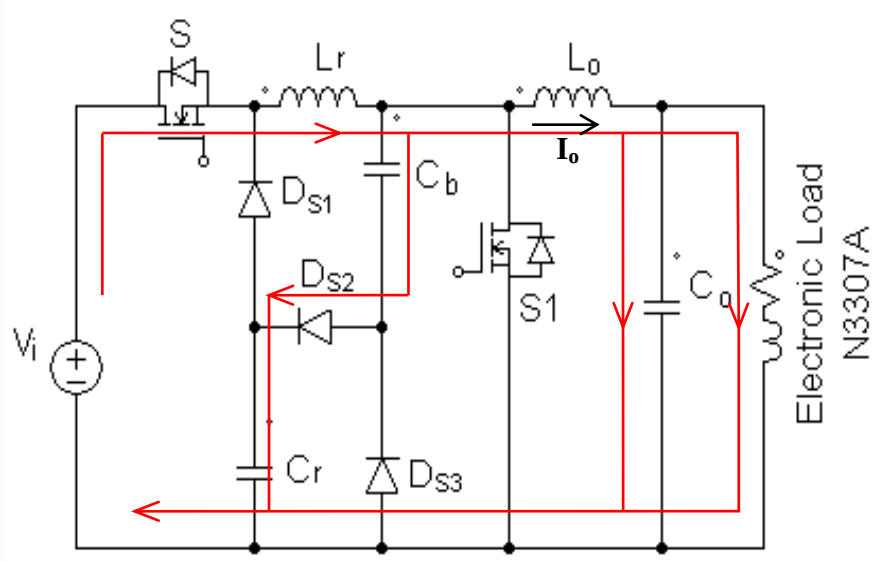


Fig. 4.3 (b) Converter Operation in Mode 2 ($t_1 - t_2$)

$$i_{Lr}(t-t_1) = \frac{V_i}{Z_1} Sin\omega_1 (t-t_1) + I_o \tag{4.4}$$

$$v_{Cr}(t-t_1) = \frac{C_e}{C_r}\left[-V_i \cos\omega_1 (t-t_1) + V_i\right] \tag{4.5}$$

$$v_{Cb}(t-t_1) = \frac{C_e}{C_b}\left[-V_i \cos\omega_1 (t-t_1) + V_i\right] \tag{4.6}$$

Where

$C_e = C_r C_b / (C_r + C_b)$

$\omega_1 = 1/\sqrt{L_r C_e}$

$Z_1 = \sqrt{L_r / C_e}$

The diode D_{S1} is turned on with ZVT at the moment when v_{Cr} becomes V_i.

Mode 3 (t_2-t_3): At t = t_2, $i_S = I_o$, $i_{Lr} = I_{Lrmax}$, $v_{Cr} = V_{Crmax} = V_i$, $v_{Cb} = V_{Cb1}$. When diode D_{S1} turns on, a new resonance starts with L_r and C_b. This mode ends when i_{Lr} becomes equal to load current I_0 and C_b is charged upto its maximum voltage V_{Cbm}. Both diodes D_{S1} and D_{S2} are turned off under ZCT due to the existence of L_r. The voltage and current expressions that govern this circuit mode are given by

$$i_{Lr}(t-t_2)=(I_{Lr\max}-I_o)\cos\omega_2(t-t_2)-\frac{V_{Cb1}}{Z_2}\sin\omega_2(t-t_2)+I_o \tag{4.7}$$

$$v_{Cb}(t-t_2)=(I_{Lr\max}-I_o)Z_2\sin\omega_2(t-t_2)+V_{Cb1}\cos\omega_2(t-t_2) \tag{4.8}$$

The time interval of this stage can be found as follows:

$$t_{23}=\frac{1}{\omega_2}\tan^{-1}\left(\frac{I_{Lr\max}-I_o}{V_{Cb1}}\right) \tag{4.9}$$

Where

$\omega_2=1/\sqrt{L_rC_b}$

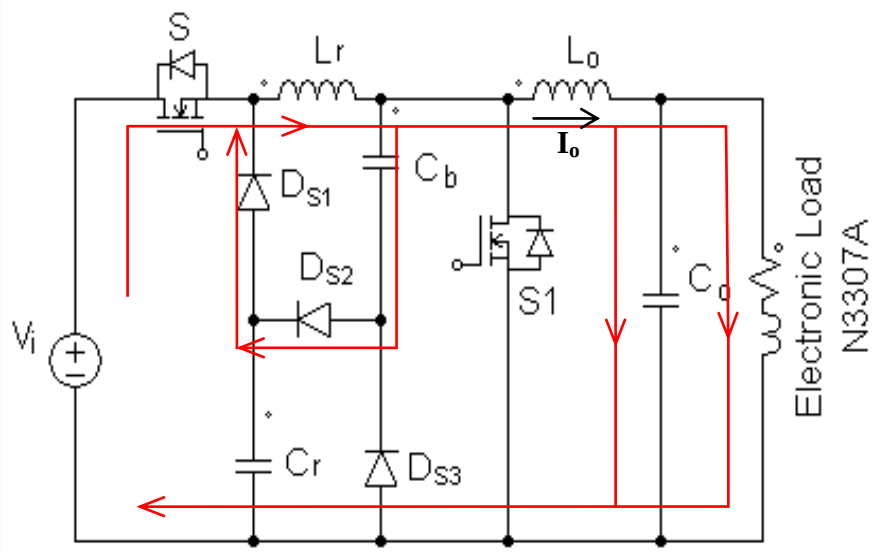


Fig. 4.3 (c) Converter Operation in Mode 3 ($t_2 - t_3$)

Mode 4 (t_3-t_4): Since both diodes D_{S1} and D_{S2} have turned off at t_3, now only the main switch S and inductor L_r carries the load current. There is no resonance in this mode and the circuit operation is identical to that of a conventional PWM buck converter. The voltage and current equations for this mode are

$$i_S=i_{Lr}=I_o \tag{4.10}$$

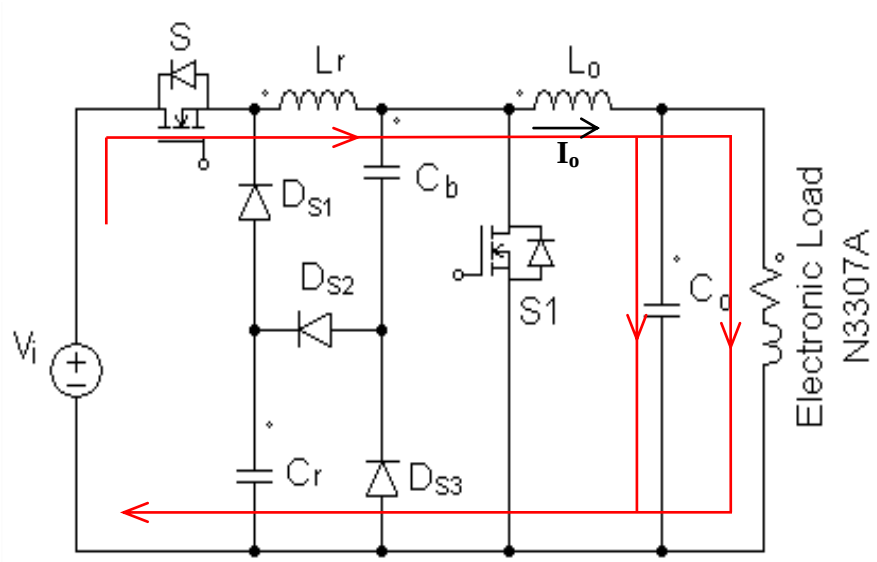


Fig. 4.3 (d) Converter Operation in Mode 4 ($t_3 - t_4$)

Mode 5 (t_4-t_5): This mode starts with the initial conditions $i_S = I_o$, $i_{Lr} = I_o$, $v_{Cr} = V_{Crmax} = V_i$, $v_{Cb} = V_{Cbm}$. The main switch is turned off under ZVT and at the same instant the synchronous switch is turned on under ZCT. Since the synchronous switch S_1 is conducting the voltage across capacitor C_b is clamped to zero. Resonance occurs with L_r and C_r. The voltage and current equations for this mode are,

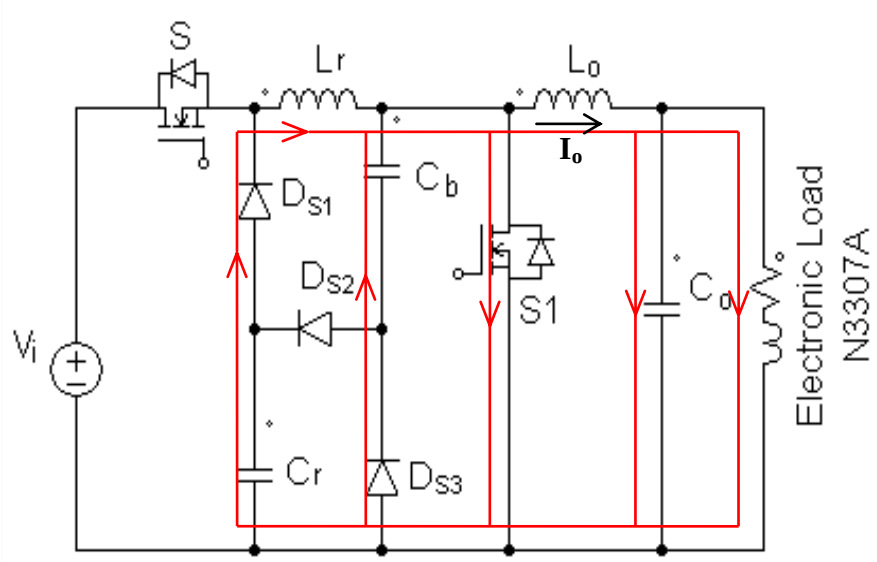


Fig. 4.3 (e) Converter Operation in Mode 5 ($t_4 - t_5$)

$$v_{Cb}(t-t_4)=0 \tag{4.11}$$

$$i_{Lr}(t-t_4)=I_o\cos\omega_3(t-t_4)-\frac{V_i}{Z_3}\sin\omega_3(t-t_4) \tag{4.12}$$

$$v_{Cr}(t-t_4)=I_oZ_3\sin\omega_3(t-t_4)+V_i\cos\omega_3(t-t_4) \tag{4.13}$$

The time duration of this mode can be found as follows:

$$t_{45}=\frac{1}{\omega_3}\tan^{-1}\frac{V_i}{I_oZ_3} \tag{4.14}$$

Where

$$\omega_3=1/\sqrt{L_rC_r}$$

$$Z_3=\sqrt{L_r/C_r}$$

This mode ends when voltage across C_r becomes zero. Therefore, the diode D_{S2} turns on under ZVT.

Mode 6 (t_5-t_6): In this stage, a new resonance takes place through L_r-C_b-D_{S2}-D_{S1}. At t = t_5, i_S = 0, i_{Lr} = I_{Lr2}, v_{Cr} = 0, v_{Cb} = 0 are initial conditions for this mode. For this state, the equations are

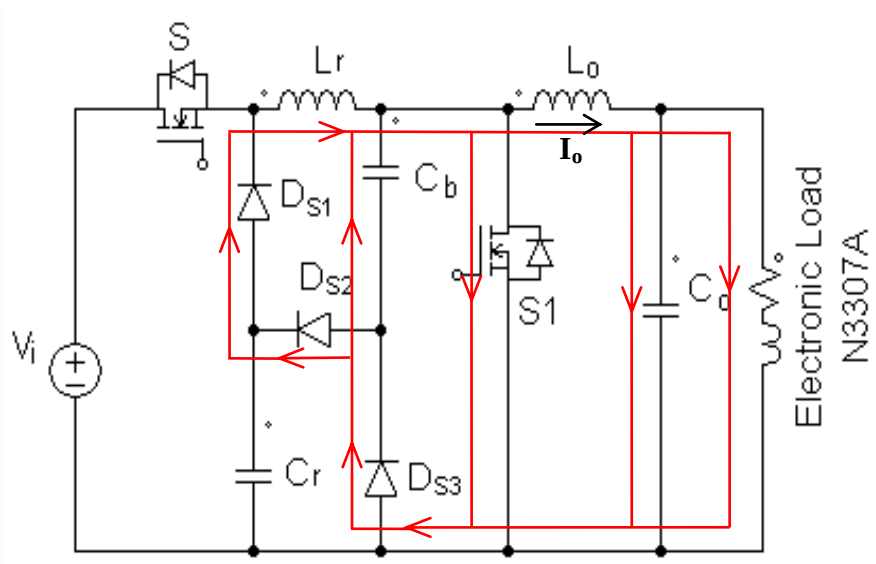


Fig. 4.3 (f) Converter Operation in Mode 6 (t_5 – t_6)

$$v_{Cb}\left(t-t_5\right)=I_{Lr2}Z_2\sin\omega_2\left(t-t_5\right) \tag{4.15}$$

$$i_{Lr}\left(t-t_5\right)=I_{Lr2}\cos\omega_2\left(t-t_5\right) \tag{4.16}$$

When i_{Lr} becomes I_0, this mode comes to an end. The time interval for this mode is given as

$$t_{56}=\frac{1}{\omega_2}\tan^{-1}\left(\frac{I_o}{I_{Lr2}}\right) \tag{4.17}$$

Where

$$\omega_2=1/\sqrt{L_rC_b}$$

$$Z_2=\sqrt{L_r/C_b}$$

Mode 7 (t_6-t_7): At $t = t_6$, $i_S = 0$, $i_{Lr} = I_o$, $v_{Cr} = 0$, $v_{Cb} = V_{Cb2}$ are initial conditions for this mode. As i_{Lr} becomes I_o, the synchronous switch is turned off under ZCT. The stored energy of inductor L_r and capacitor C_b is now transferred to the load. ON-state resistances of diodes and switches are neglected. The voltage and current equations for this mode are given as

$$v_{Cb}\left(t-t_6\right)=-\frac{I_o}{C_b}\left(t-t_6\right)+V_{Cb2} \tag{4.18}$$

$$i_{Lr}\left(t-t_6\right)=-\frac{V_o}{L_r}\left(t-t_6\right)+I_o \tag{4.19}$$

This mode ends when i_{Lr} becomes zero. The interval of this mode is given by

$$t_{67}=\frac{I_oL_r}{V_o} \tag{4.20}$$

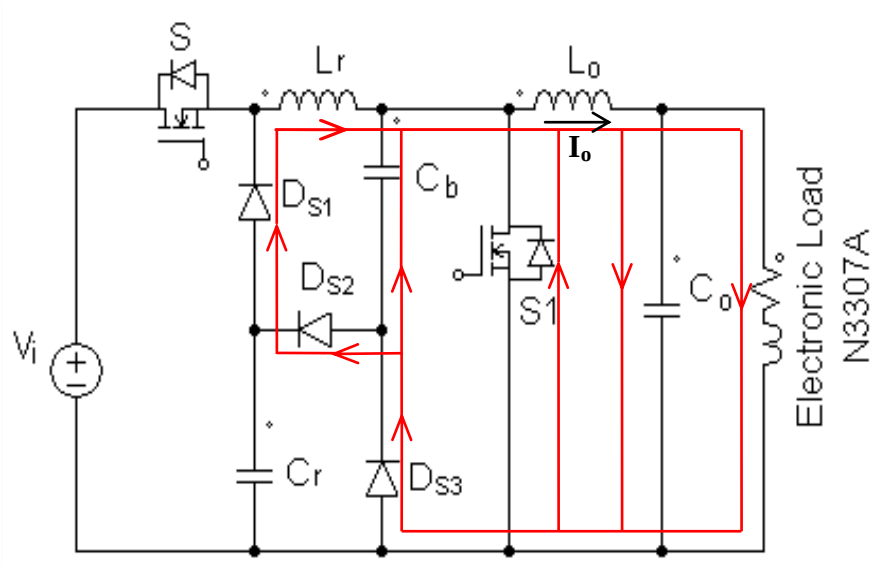


Fig. 4.3 (g) Converter Operation in Mode 7 ($t_6 - t_7$)

Mode 8 (t_7-t_8): Now the load current will flow through the body diode of the synchronous switch S_1. During this mode, the converter operates like a conventional PWM buck converter until the switch S is turned on in the next switching cycle. In this mode

$$i_{D1} = I_o \tag{4.21}$$

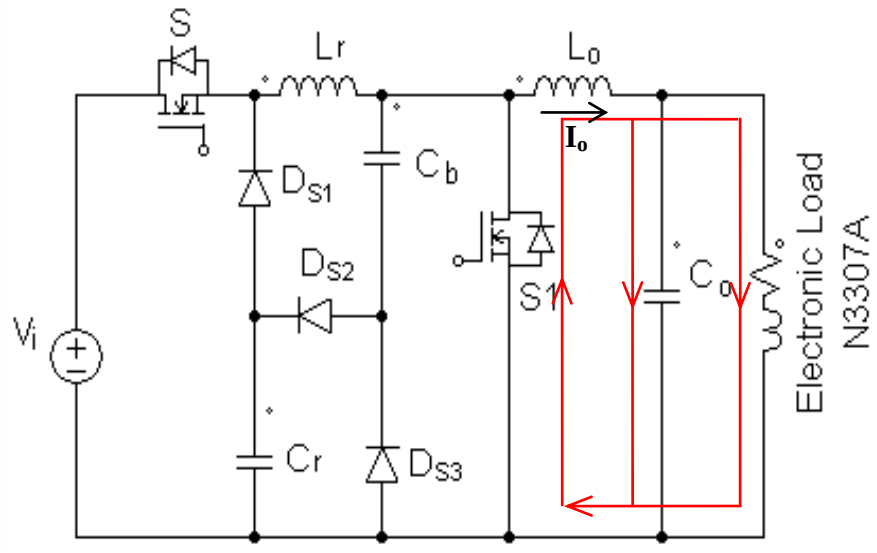


Fig. 4.3 (h) Converter Operation in Mode 8 ($t_7 - t_8$)

4.3 Design procedure:

Since the auxiliary circuit is providing soft switching for the switches, more focus is given on the designing of the auxiliary circuit, where the resonant inductor and the resonant capacitor are the most important components [136].

1. The snubber inductor L_r is selected to permit its current to rise up to at most the maximum output current within t_r time periods, during the turn on of the main transistor or the turn off of the synchronous switch. In this case, from equation (4.1)

$$\frac{V_i}{L_r} t_r \le I_{o\max} \tag{4.24}$$

Here t_r is the rise time of the main transistor. These equations provide ZCS turn on for the main transistor and ZVS turn off for the body diode of synchronous switch.

2. The snubber capacitor C_r is selected to discharge from V_i to zero with the maximum output current over at least the time period t_f during the turn off of the main transistor. For this state, according to equations (4.13) and (4.14)

$$\frac{1}{I_{o\max} Z_3} V_i \ge t_f \tag{4.25}$$

Here, t_f is the fall time of the main transistor and

$$Z_3 = \sqrt{L_r / C_r}$$

3. The buffer capacitor C_b is selected to be charged from zero up to at most a value decided before, such as half the input voltage [136]. This capacitor takes on the energies that are stored in the snubber inductor during the turn off of the synchronous switch and charge of the snubber capacitor. This energy balance can be defined as follows:

$$\frac{1}{2} C_r V_i^2 + \frac{1}{2} C_b V_{Cb\mathrm{m}}^2 = \frac{1}{2} L_r I_{o\max}^2 \tag{4.26}$$

The charging rate of capacitor C_r should be more than the fall time of main switch S, which is equal to the rate of increase of current through inductor L_r.

$$\frac{C_r V_i}{I_{Lr\max} - I_o} \geq t_{12} \tag{4.27}$$

From equation (4.5), t_{12} can be determined as

$$t_{12} = \frac{1}{\omega_1} \sin^{-1}\left(\frac{C_r}{C_e} - 1\right) \tag{4.28}$$

By solving equation (4.27) and (4.28) two equations, C_b is derived as

$$\sin\left(\frac{\omega_1 C_r V_i}{I_{Lr\max} - I_o}\right) \geq \frac{C_r}{C_b} \tag{4.29}$$

Now C_b can be determined and proved that C_b should be greater than C_r.

The value of C_b is normally larger than the value of C_r to provide the condition for energy transfer from inductor L_r to C_b. Consequently the bigger the value of C_b selected, the lower the value of $V_{Cbmax,}$ because of more time required to charge up to peak value. Moreover, if the value of C_b increases, the voltage across the synchronous switch falls, but the time periods t_{23}, t_{45}, t_{56}, and t_{67} on which the inductor energies are transferred to C_b or the load rises.

4.4 Simulation and Experimental results:

A prototype of the proposed converter has been fabricated in the laboratory. The proposed converter operates with an input voltage V_i = 12 V, an output voltage V_o = 3.3 V, a load current of 11 A and a switching frequency of 500 kHz. The converter is simulated using PSIM 7.1. The major parameters and components are given in Table 4.1. Figs. 4.4 (a-e) show the simulation results of the proposed converter and Figs. 4.5 (a-e) present the experimental results. The photograph of the prototype converter is shown in the Fig. 4.6.

Table 4.1: Components used in the Proposed PS SBC

Component	Value/Model	
	Simulation	Experiment
Main Switch, S	Ideal	IRF1312
Synchronous Switch, S_1	Ideal	IRF1010E
Schottky Diode, D_{S1}	Ideal	MBR60L45CTG
Schottky Diode, D_{S2}	Ideal	MBR60L45CTG
Schottky Diode, D_{S3}	Ideal	MBR60L45CTG
Resonant Inductor, L_r	15 nH	15 nH
Resonant Capacitor, C_r	1 nF	1 nF
Buffer Capacitor, C_b	3.3 nF	3.3 nF
Output Capacitor, C_o	15 µF	15 µF
Output Inductor, L_o	5 µH	5 µH

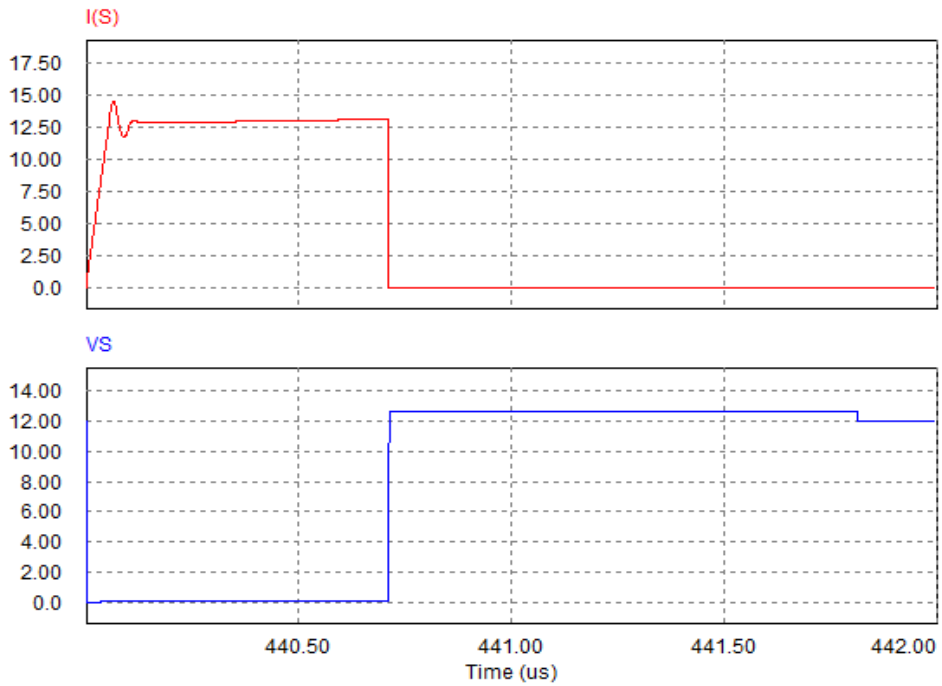


Fig. 4.4 (a) Simulated voltage and current waveforms of the main switch S: V_S in Volts; I_S in Amps

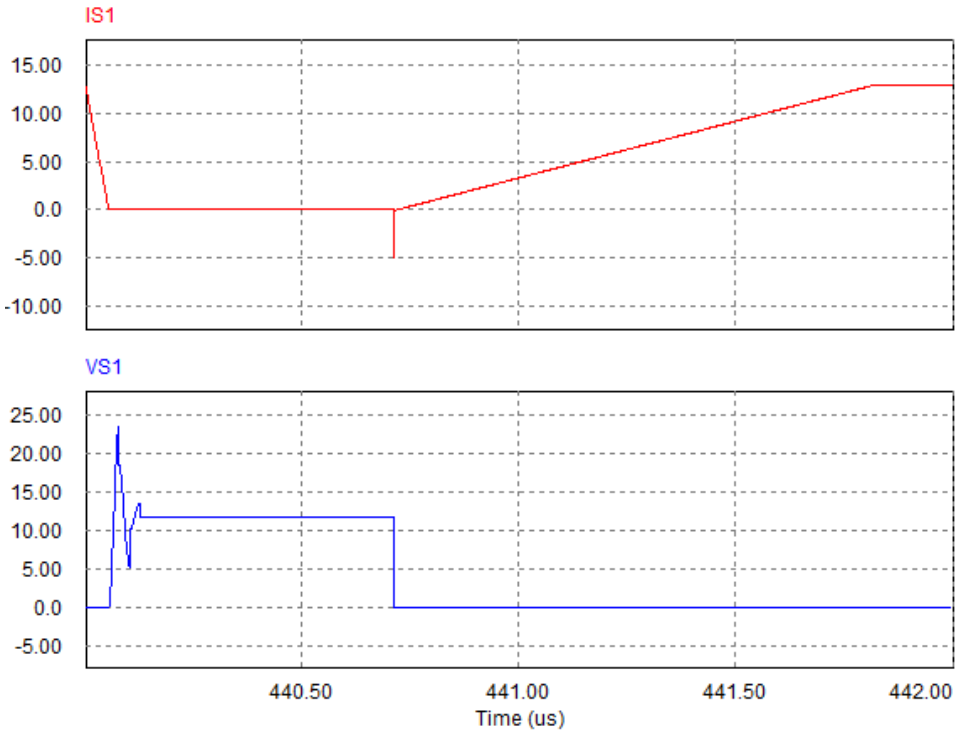


Fig. 4.4 (b) Simulated voltage and current waveforms of the synchronous switch S_1: V_{S1} in Volts; I_{S1} in Amps

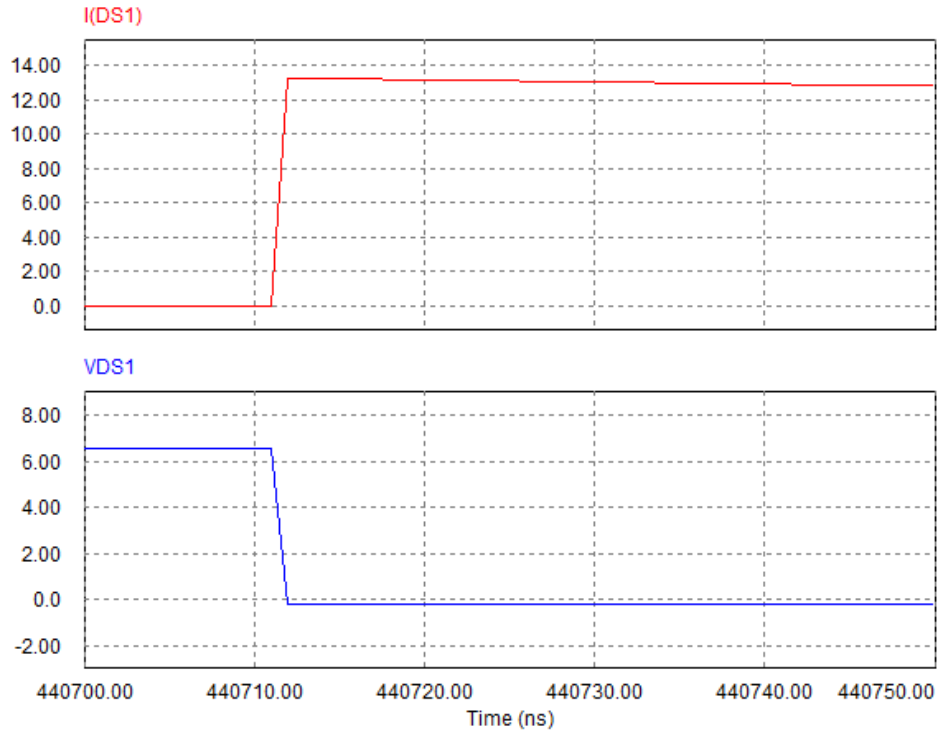


Fig. 4.4 (c) Simulated voltage and current waveforms of the Diode D_{S1}: V_{DS1} in Volts; I_{DS1} in Amps

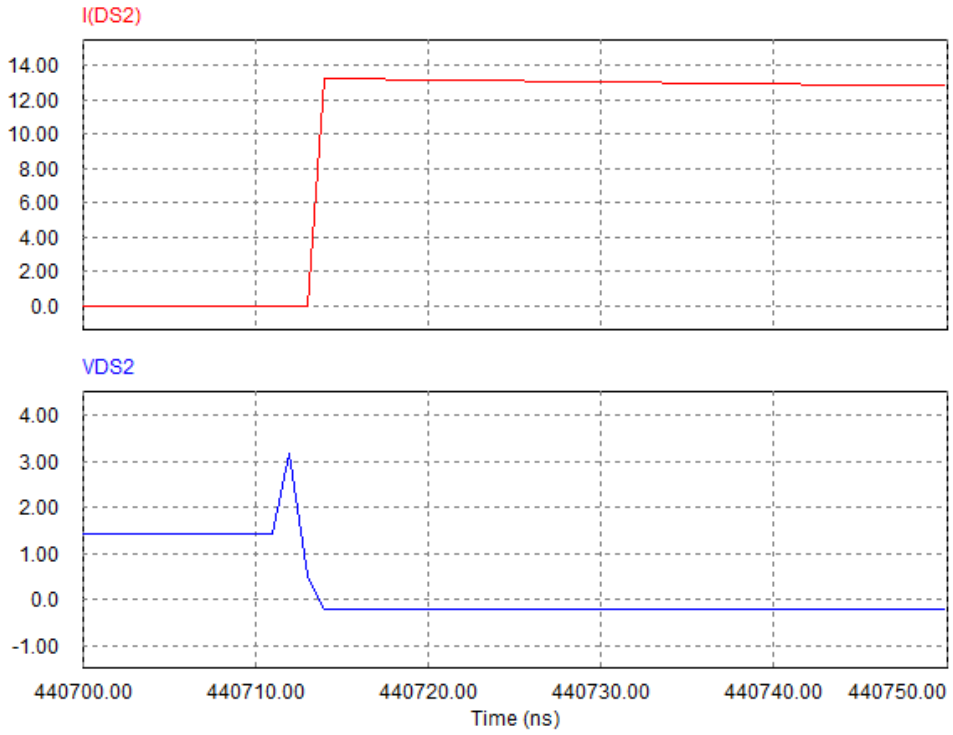


Fig. 4.4 (d) Simulated voltage and current waveforms of the Diode D_{S2}: I_{DS2} in Amps; V_{DS2} in Volts

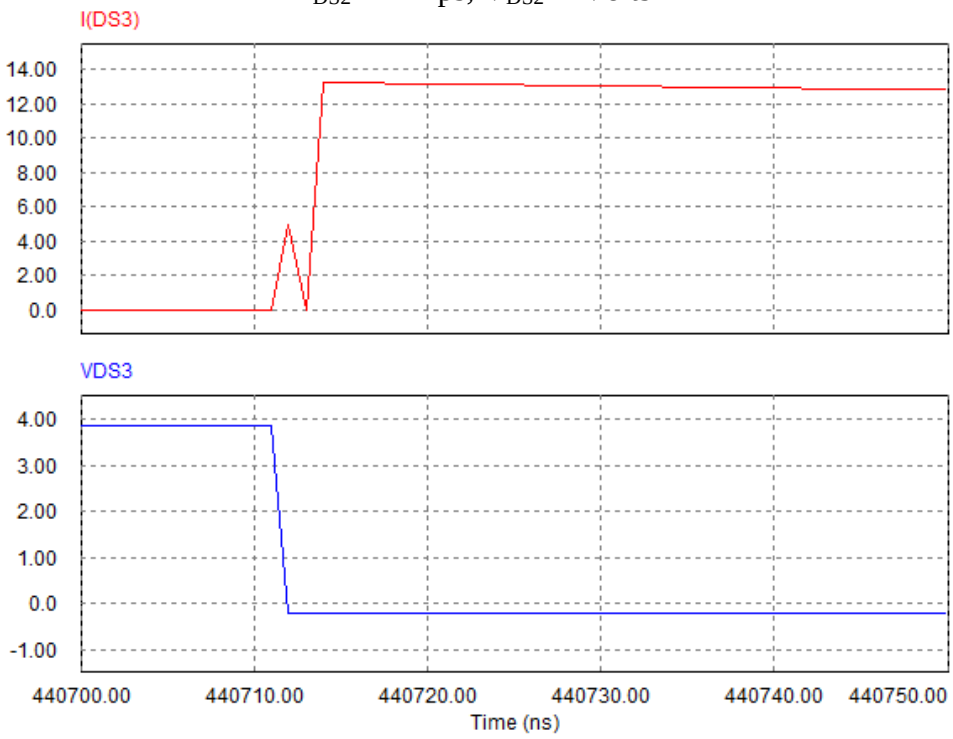


Fig. 4.4 (e) Simulated voltage and current waveforms of the Diode D_{S3}: I_{DS3} in Amps; V_{DS3} in Volts

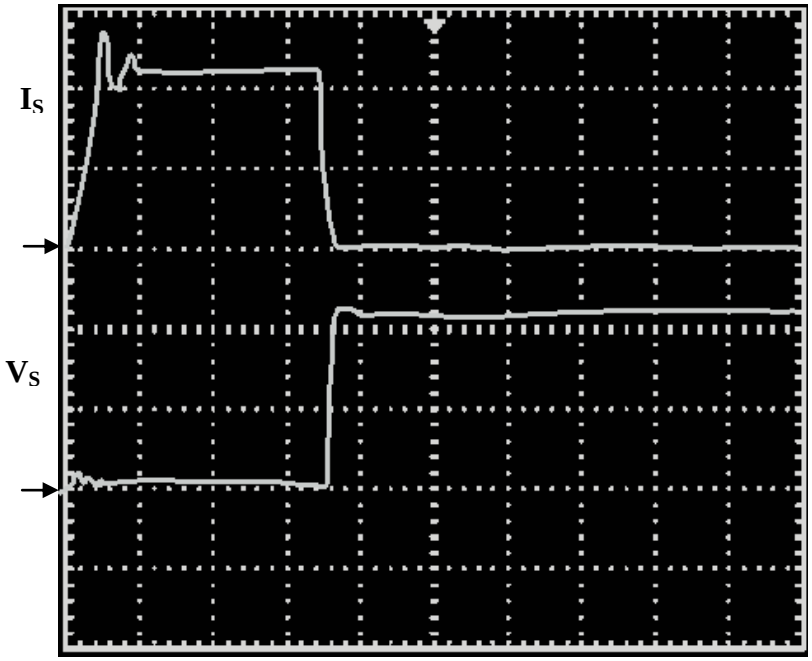


Fig. 4.5 (a) Experimental voltage and current waveforms Main switch S:
V_S; I_S: (V: 5 V/div, I: 5 A/div, time: 0.2 μs/div)

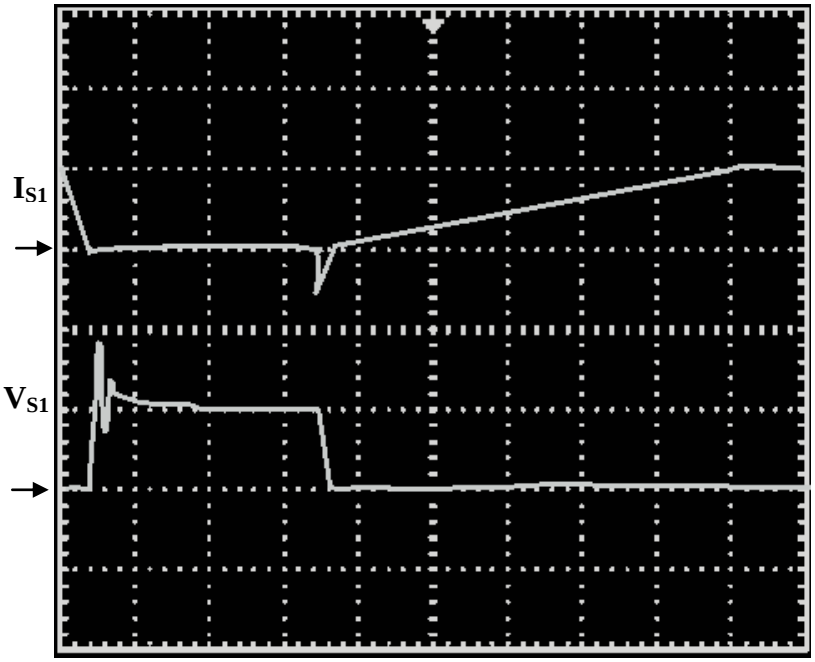


Fig. 4.5 (b) Experimental voltage and current waveforms Synchronous switch S_1:
V_{S1}; I_{S1}: (V: 10 V/div, I: 10 A/div, time: 0. 2 μs/div)

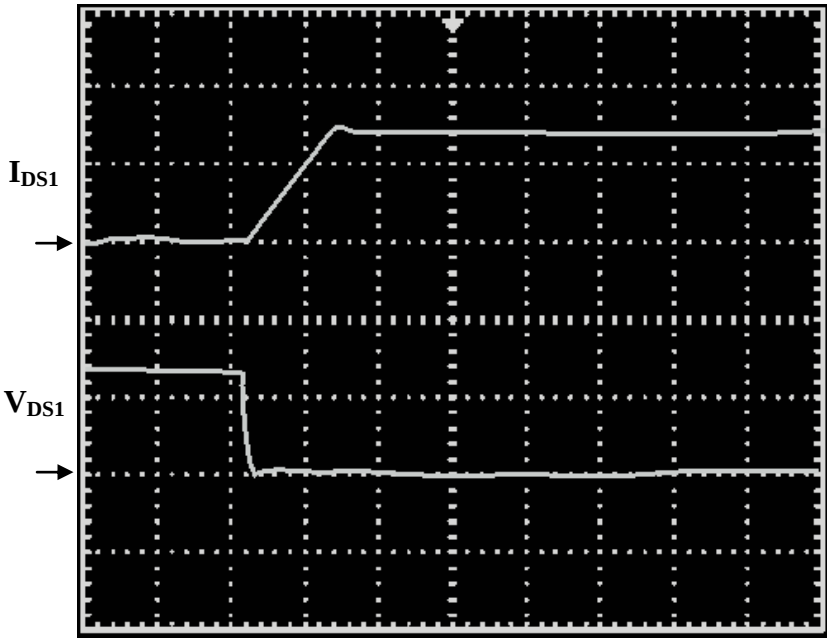


Fig. 4.5 (c) Experimental voltage and current waveforms Diode D_{S1}: I_{DS1}; (10 A/div), V_{DS1} (5 V/div), time: 0. 5 ns/div)

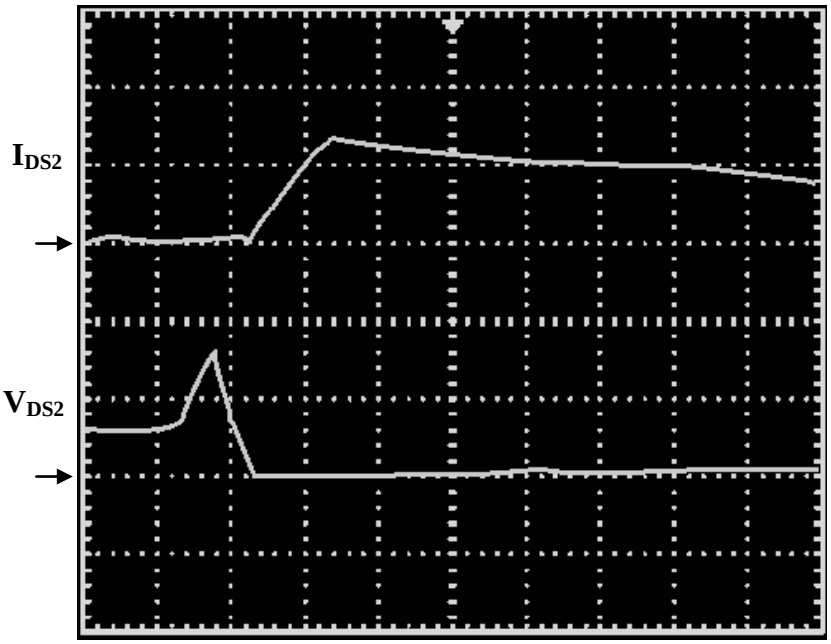


Fig. 4.5 (d) Experimental voltage and current waveforms Diode D_{S2}: I_{DS2}; (10 A/div), V_{DS2} (2 V/div), time: 0. 5 ns/div)

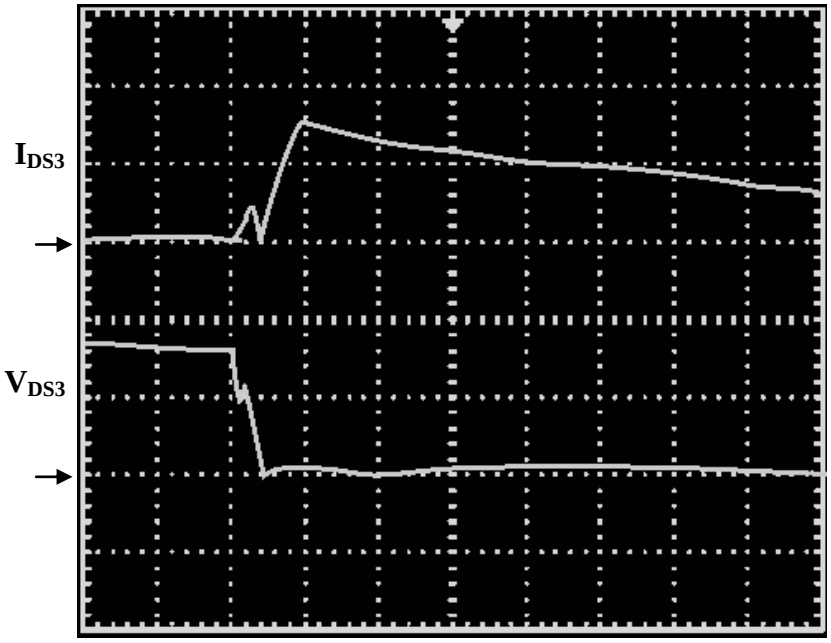


Fig. 4.5 (e) Experimental voltage and current waveforms Diode D_{S3}: I_{DS3}; (10 A/div), V_{DS2} (2 V/div), time: 0. 5 ns/div)

Fig. 4.6 Photograph of proposed ZVT PS synchronous buck converter

4.5 Efficiency curve

The relationship between the output power and the efficiency is presented in Fig.4.6. It can be observed that the efficiency values of the soft switching converter are relatively high with respect to those of the hard switching converter. The efficiency values towards the minimum output power decrease naturally because the converter is designed for the maximum output current. At 70% of the output power, the overall efficiency of the proposed

converter increases to about 96% from the value of 87% in its counterpart hard switching converter. The high efficiency concludes the correctness of the design values.

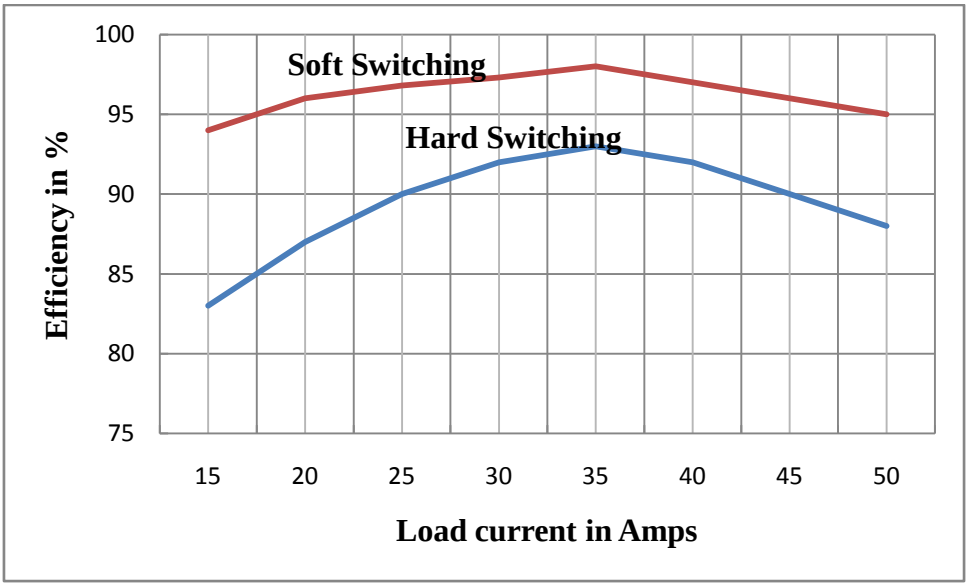


Fig. 4.7 Efficiency vs Load current

4.6 Summary

A passive snubber is incorporated in the conventional SBC to improve the performance. The switching losses are reduced with this soft switching technique and it is highly efficient than the synchronous buck converter employing active auxiliary switch. The snubbers' energy is recuperated to the load without using the main switch path, thus, the conduction loss is reduced. But this additional conduction loss is present in SBC utilizing an active auxiliary switch, because the transfer of the stored energy to the load takes place through main switch. The excess voltage and current stresses on the main devices do not take place, and the auxiliary devices are subjected to allowable voltage and current values. The main switch S and The synchronous switch S_1 are turned on and turned off under ZCS and ZVS respectively due to inductor L_r and capacitors C_r and C_b. All the diodes are turned on and turned off under ZVS and ZCS respectively. Moreover, the converter has a simple structure, low cost and can be control easily. A prototype of a 3.3V, 11A, 500 kHz converter is tested in the laboratory to verify the simulation results.

CHAPTER 5

EXTENSION OF ZVT TO MULTIPHASE BUCK CONVERTER

Topology description

Operating principles and analysis

Current control scheme

Design consideration

Simulation and experimental results

Summary

Chapter 5. Extension of ZVT to multiphase buck converter

In chapter 3 and chapter 4, ZVT techniques to SBC are presented they facilitate the reduction of switching losses, while maintaining voltage and current stresses within a tolerable limit. This ZVT concept is further extended to a multiphase buck converter which has recently emerged as the leading candidate for meeting the power requirement of the portable electronics systems.

High current multiphase buck converters (MBC) are used in computing, graphics, and telecom applications. With a duty cycle of less than 10 %, raising the switching frequency to multi-MHz level will reduce the efficiency to less than 80 %. Because the switching frequency is equal to the inductor current ripple frequency, the switching frequency is limited between 300 kHz to 500 kHz [24, 138-142]. When the inductor current slew rate is increased with a smaller inductance value to improve the transient response, then the inductor current ripple also increases. It is not only a harmful action for the high-side switch due to larger turn-off loss, but also for the low-side switch due to a larger conduction loss. It also increases the inductor winding losses. This conflict limits the average inductor current in each channel [143-148]. Moreover, there is a tradeoff between efficiency and transient response. As a result, these technical conflicts do not only increase the costs and sacrifice the power density, but also difficultly meet the power requirements of future microprocessors before the technical conflicts are resolved [149-151]. Therefore there is a need to increase the efficiency of the multiphase buck converter at a high operating frequency by reducing switching losses.

In this chapter, the ZVT multiphase synchronous buck converter is presented with the directive to improve its performance. The proposed converter achieves ZVS with reduction in voltage and current stresses across switches to improve the efficiency by minimizing the switching and conduction losses with a simple active auxiliary circuit. Here the proposed

multiphase is associated with active auxiliary circuit rather than passive auxiliary circuit because at high load current passive auxiliary circuit will give high conduction losses. Section 5.1 presents a description of the proposed topology. Principles of operations and its analysis are discussed in section 5.2. Section 5.3 provides the design process of the multiphase converter. The predicted operation principles and the theoretical analysis of the converter are verified in section 5.4 with some simulation and experimental results. In the last section, all the concluding remarks are discussed.

5.1 Topology description

The proposed multiphase converter is shown by Fig. 5.1 (a). It is a combination of the proposed converter along with active auxiliary circuit that facilitates reduction of switching losses. The auxiliary circuit consists of inductor L_r, diode D_1, and MOSFET switches S_7, S_8, and S_9. The number of auxiliary MOSFET switches depends on the number of phases. Body diodes of main switches S_1, S_2, and S_3 are utilized to provide zero voltage switching. Additionally, a simple current mode control scheme is proposed for current sharing respectively in each phases. The phase current unbalance effect is overcome by a simple current control scheme. The schematic view of the control technique is shown in Fig. 5.1 (b). It consists of a proportional integral compensator, a limiter, a comparator, and a mono-stable multi-vibrator. A PI controller properly designed reduces the steady-state error. This control scheme uses a current control method because of its advantages over voltage mode methods such as: faster response and stability over a wide range of loads. A PWM signal is generated using a multi-vibrator with a predefined dead time control between the main switches and the synchronous switches.

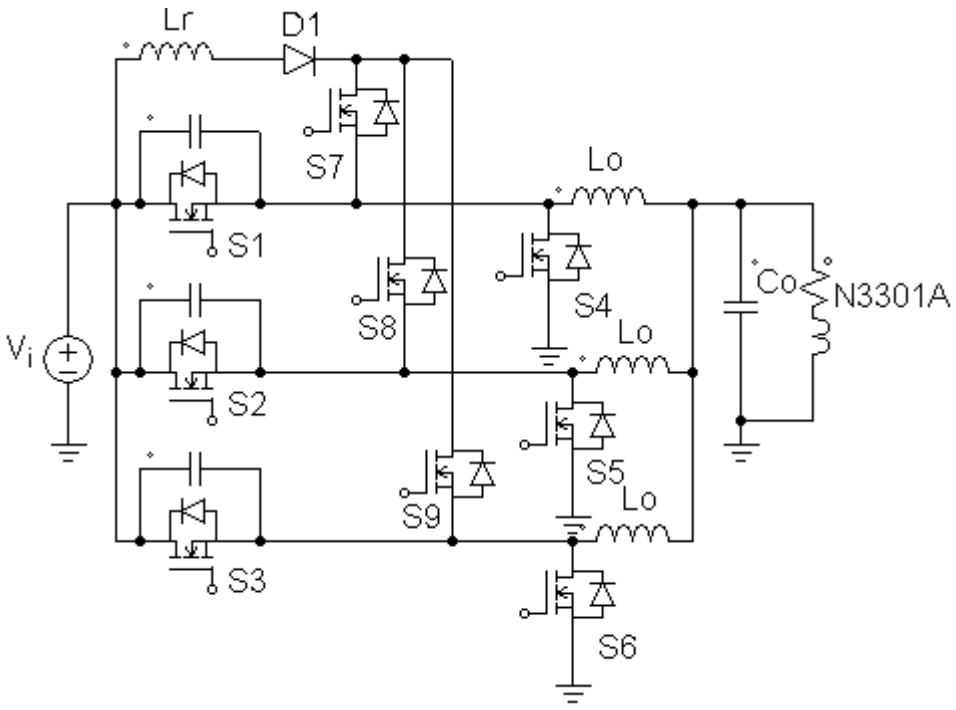


Fig. 5.1 (a) Proposed MBC

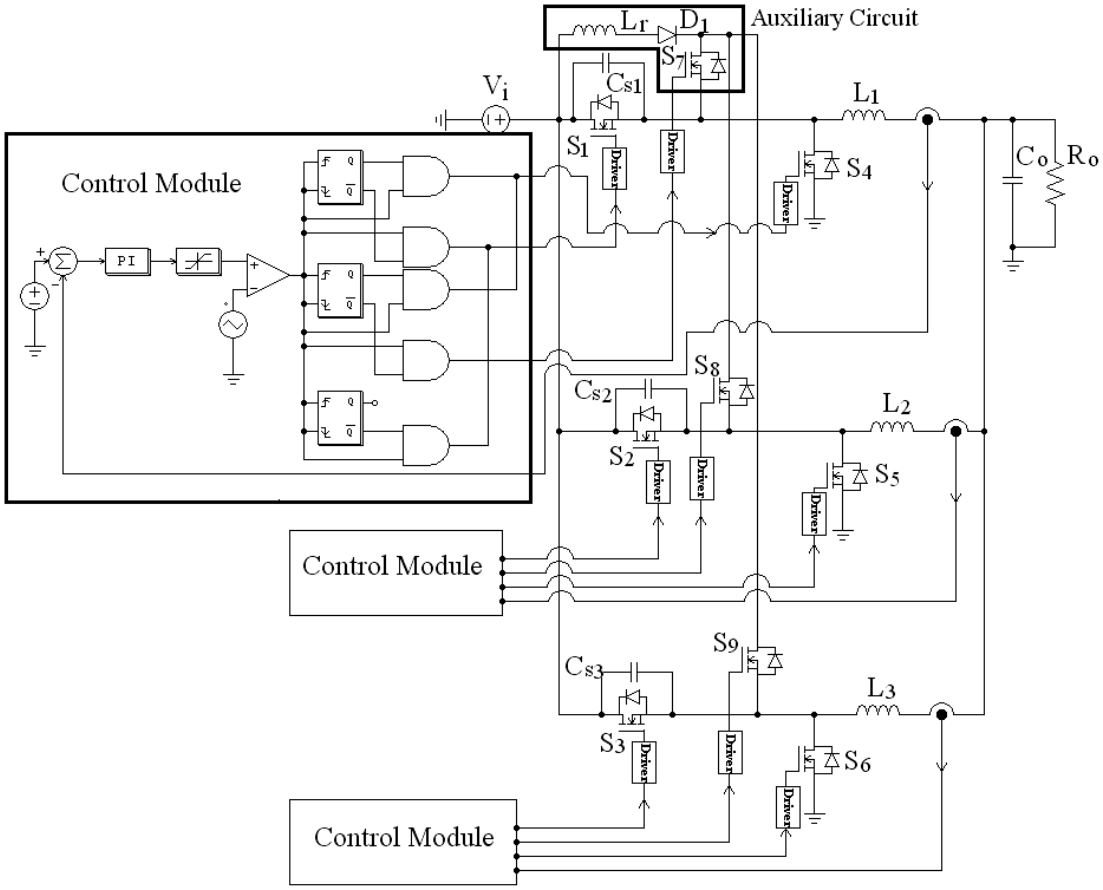


Fig. 5.1 (b) Proposed MBC with current control topology

5.2 Operating principles and analysis

In order to analyze the steady-state operations of the proposed circuit, the following assumptions are made during one switching cycle.

1. the input voltage V_i is constant.
2. the output voltage V_o is constant or the output capacitor C_o is large enough.
3. the output current I_o is constant or the output inductor L_o is large enough.
4. the output Inductor L_o is much larger than the resonant circuit inductor L_r.
5. the resonant circuits are ideal.
6. the semiconductor devices are ideal.
7. the reverse recovery time of diode is ignored.

Based on these assumptions, circuit operations in one switching cycle can be divided into fifteen stages. The key waveforms of these stages are illustrated in Fig. 5.2 and the equivalent circuit schemes of the operation stages are given in Fig. 5.3. The detailed analysis of every stage is presented below:

Mode 1(t_0-t_1): Prior to $t = t_0$, the body diode of switch S_4 was conducting while the main switch S_1 is off. The equations $i_S = 0$, $i_{D4} = I_0/3$, $i_{Lr} = 0$, are valid at the beginning of this stage. At $t = t_0$, the auxiliary switch S_7 is turned on, which realizes zero-current turn-on as it is in series with the resonant inductor L_r. During this stage, i_{Lr} rises and current i_{Ds4} through body diode of switch S_1 falls simultaneously at the same rate. The resonance occurs between L_r and C_{s1}.

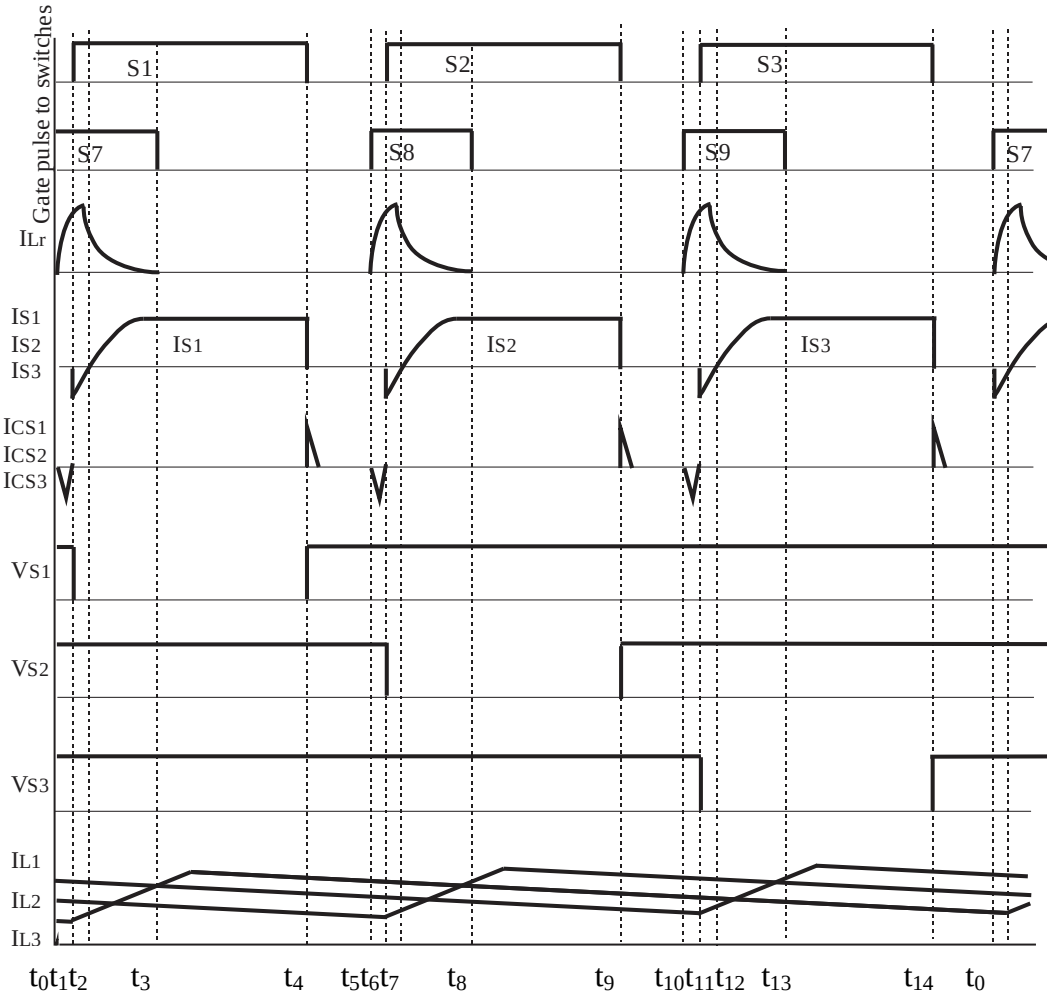


Fig. 5.2 Key waveforms of proposed MBC

This mode ends at t = t_1, when i_{Lr} reaches $I_0/3$, and i_{D4} becomes zero. The body diode D_4 is turned off with ZCS. The resonant current through inductor L_r is given by

$$i_{resonant}(t) = C_{S1} V_{CS1} \omega sin\omega t \tag{5.1}$$

$$i_{Lr}(t) = \frac{V_i}{L_r} \times t \tag{5.2}$$

Where $\omega = 1/\sqrt{L_r C_{S1}}$

At t = t_1, $i_{Lr}(t) = I_o/3$, therefore $t_{01} = t_1 - t_0 = \frac{I_o L_r}{V_i}$

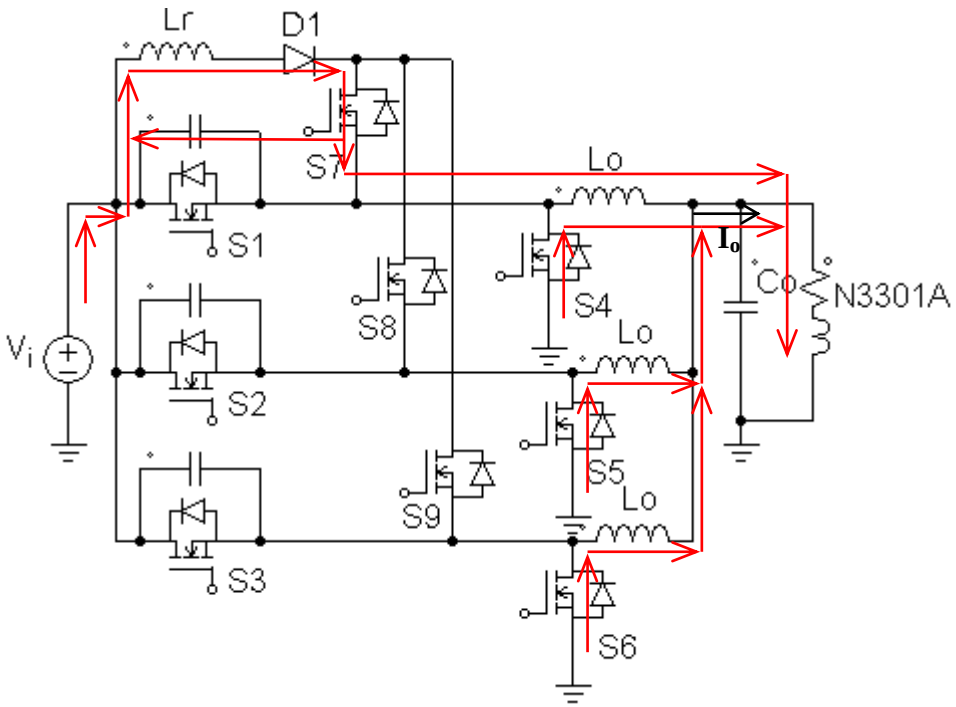


Fig. 5.3 (a) MBC operation in Mode 1($t_0 - t_1$)

Mode 2(t_1-t_2): Since the inductor current i_{Lr} is increasing continuously beyond one third of load current, the exceeding current makes the diode D_{S1} to conduct. At $t = t_1$, $i_{S7} = i_{Lr} = I_0/3$. After reaching the peak current I_{Lrmax}, the inductor current starts decreasing. This mode comes to an end when i_{Lr} becomes again equal to $I_0/3$. At this moment, the main switch is triggered to turn on under zero voltage switching (ZVS). The discharge current of capacitor C_{S1} through the body diode having a resistance R is given as:

$$i_{C_{s1}} = \frac{V_{Cs1}}{R} e^{-t/RC_{S1}} \tag{5.3}$$

Mode 3(t_2-t_3): At $t = t_2$, the main switch is turned on while the auxiliary switch is still in on state. Now the stored energy in inductor L_r will be transfered to the load at the same rate as the current increase through the main switch S_1. At $t = t_2$, $i_{Lr} = I_0/3$.

This mode comes to end when the total energy of the resonant inductor will be transfered to the load. The auxiliary switch S_7 will turn off under ZCS.

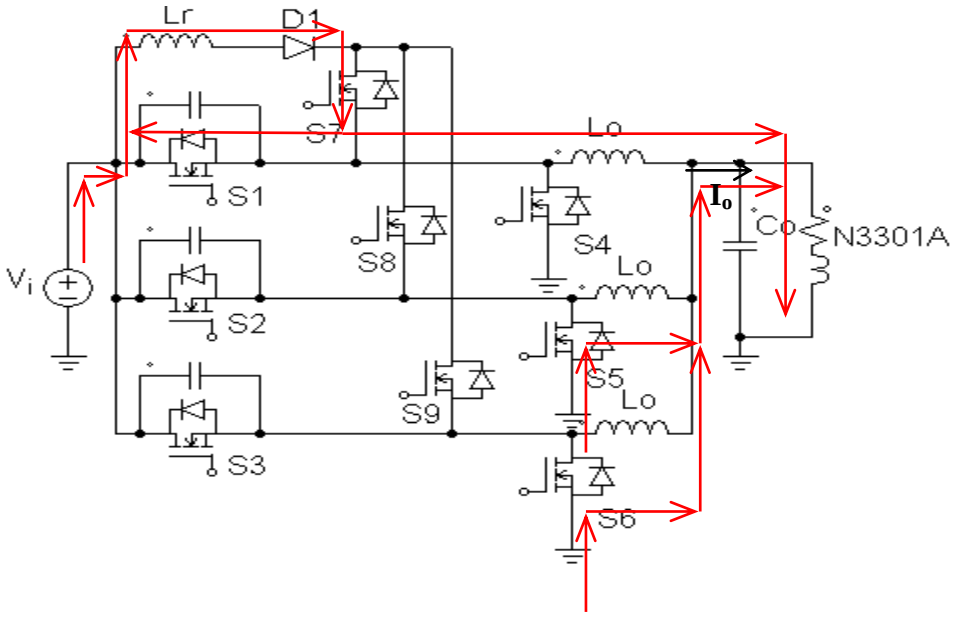


Fig. 5.3 (b) MBC operation in Mode 2($t_1 - t_2$)

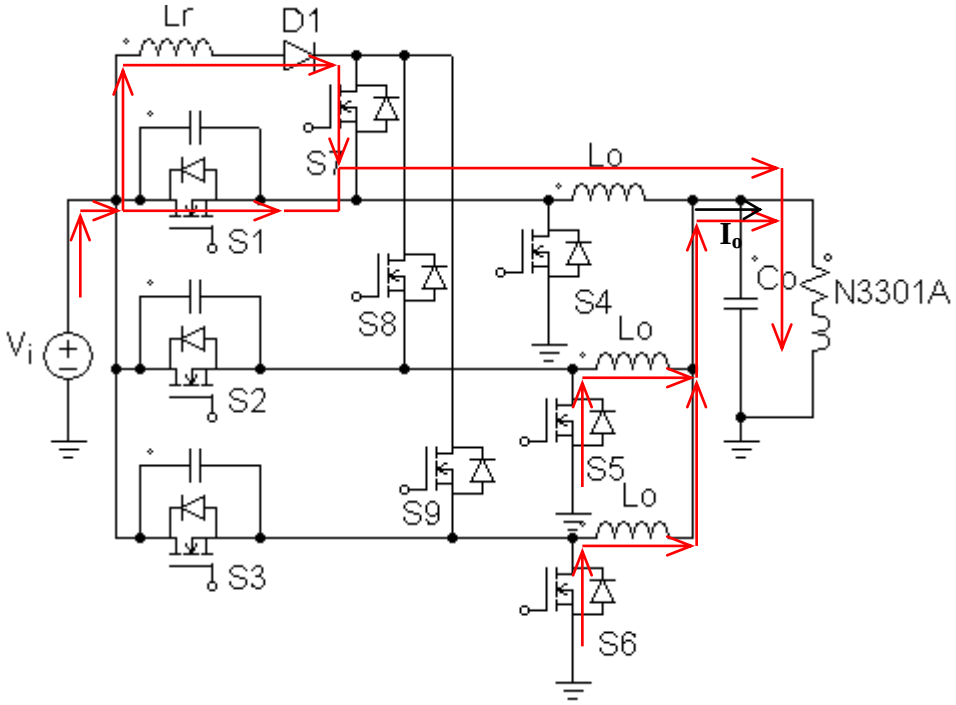


Fig. 5.3 (c) MBC operation in Mode 3($t_2 - t_3$)

The inductor current i_{Lr} during this mode can be expressed as

$$i_{Lr}(t) = I_{Lr\max} e^{-tLr/R_{on}} \tag{5.4}$$

and

$$i_{S1} + i_{Lr} = I_0/3 \tag{5.5}$$

At the end, at t = t_3.

$$i_{S1} = I_o / 3 \tag{5.6}$$

$$i_{Lr} = 0 \tag{5.7}$$

Mode 4(t_3-t_4): In this mode, the converter behaves as a conventional PWM converter. For the required output voltage, the turn on period of the main switch is decided. At the end of this mode, the main switch S_1 is turned off under ZVS due to the existent of capacitor C_{S1} across it. The current expression for this mode can be expressed as:

$$i_{S3} = I_0 \diagup 3 \tag{5.8}$$

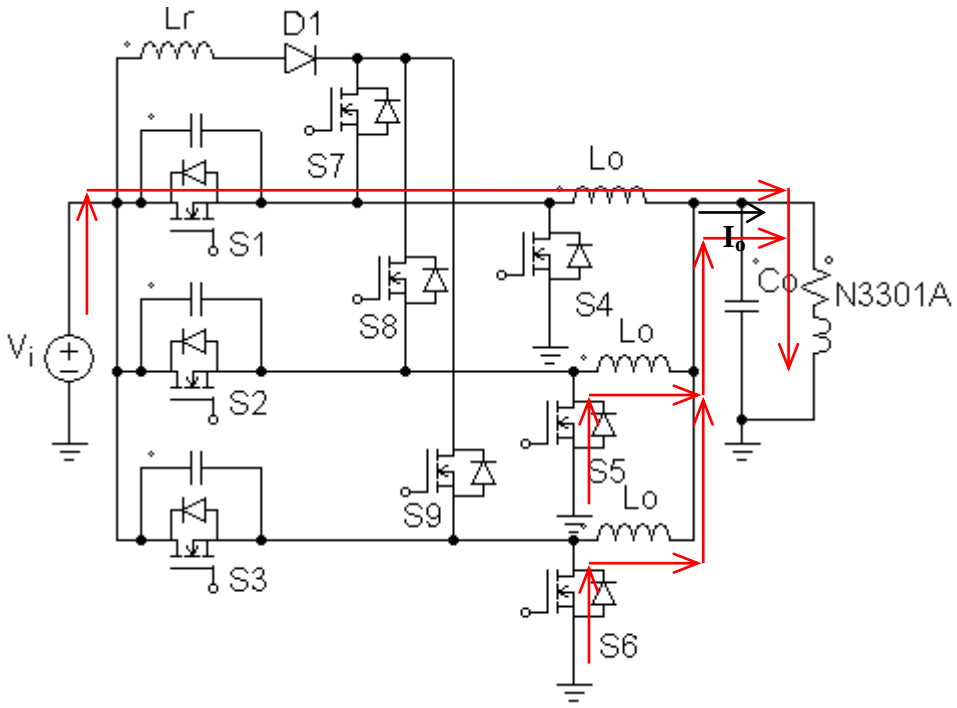


Fig. 5.3 (d) MBC operation in Mode 4(t_3 – t_4)

Mode 5(t_4-t_5): At t = t_4, the synchronous switch is turned on to provide a constant load current. At the end of this mode, the complete operation for one phase converter is completed and the second auxiliary switch S_8 is turned on with a phase difference of 360/n, where n is

the number of phases, here n = 3. The same five modes will be repeated for each phase. So there are fifteen modes for this proposed multiphase converter. The current expression for this mode can be expressed as:

$$i_{S4} = I_o / 3 \tag{5.9}$$

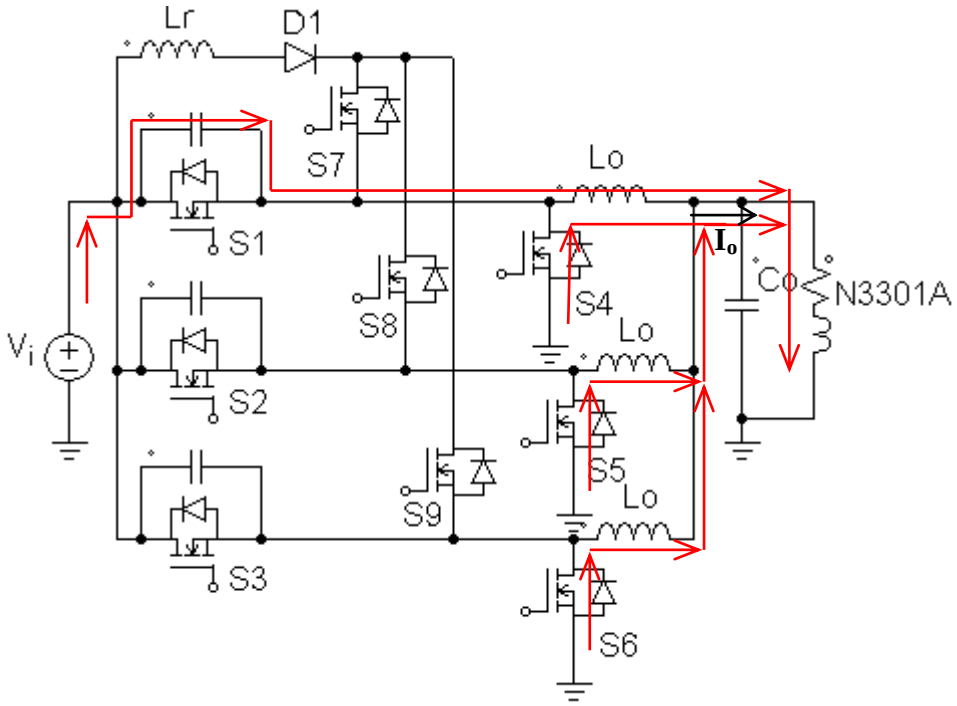


Fig. 5.3 (e) MBC operation in Mode 5($t_4 - t_5$)

5.3 Current control scheme

In this control architecture, a mono-stable multi-vibrator provides the required PWM pulses to the corresponding driver circuits, so that all SBC should operate with proper phase differences. The inductor current is compared with the reference current which is the average current flowing through each phase. The error is compensated by a PI controller (used to provide a zero steady state error), which is then compared with the desired high frequency ramp signal to produce high frequency switching pulses. In this chapter, the current sharing

problem is not discussed. The main focus is the loss minimization in the multiphase synchronous buck converter by assuming an equal current sharing in each phase.

5.4 Design consideration

In order to generate an optimized solution for a application as VRM, the designer must consider a number of criteria like; the number of phases, the current per phase, the auxiliary circuit parameters etc.

5.4.1 Number of Phases

The first thing to be considered is the optimum number of phases. Increasing the number of phases reduces the ripple current in the input and output filters and potentially improves the transient response, however it also increases complexity, PCB layout difficulty, and at some point, cost. Usually, the choice is based on how many power MOSFETs are required to efficiently handle the per phase output current. This requires an additional output inductor but the increased cost and PCB area of these components tends to offset by reductions in the cost and size of the input filter and output capacitors.

5.4.2 Current Per Phase

The performance of the MOSFETs tends to determine the optimal current per phase, which today ranges from 10 to 30 A. Designs operating at lower switching frequencies, using state-of-the-art MOSFETs, and having low thermal impedance (heat sinks) tend to be in the upper end of this range. Designs targeting compact size, maximum efficiency, fast transient response, higher switching frequencies, or use of mature lower cost MOSFETs tend to be in the lower end of the range. As future generations of MOSFETs become available, it will be possible to increase the current per phase without compromising the efficiency or the thermal performance.

5.4.3 Auxiliary circuit components

The auxiliary circuit parameter design procedures are the same as ones followed in the Chapter 3.

1. The resonant capacitor C_{S1} is selected to discharge from V_i to zero with the maximum output current over at least the time period t_{on} during the turn on of the body diode. For this state and according to (5.3), we have

$$RC_{S1} \ln \frac{RI_0}{V_{CS1}} \geq t_{on} \tag{5.10}$$

Here, t_{on} is the turn on time of the body diode.

2. The resonant inductor L_r is selected such that the current through the inductor can be reduced to zero from $I_o/3$ in the same duration of the rise in current form zero to $I_o/3$ in the main switch. In this case, from equation (5.4), we have

$$t_{23} = \frac{R_{on}}{L_r} \tag{5.11}$$

5.5 Simulation and Experimental results

A prototype of the proposed converter, as shown in Fig. 5.1 has been built in the laboratory. The converter is simulated using PSIM 7.1. The major parameters and components are given in Table 5.1. The proposed converter is experimentally validated with the theoretical and simulation results with the help of the appropriate components mentioned in the Table 5.1. Figs. 5.4 (a-j) show the simulation results of the proposed converter and Figs. 5.5 (a-i) present the experimental results. The photograph of the prototype converter is shown in the Fig. 5.6.

TABLE 5.1
Components used in the proposed MBC

Component	Value/Model
	Simulation/Experimental
Main Switches, S_1, S_2, S_3	Ideal/HRF3205
Synchronous Switches, S_4, S_5, S_6	Ideal/ HRF3205
Auxiliary Switches, S_7, S_8, S_9	Ideal/ HRF3205
Resonant Inductor, L_r	1 nH
Capacitors C_{s1}, C_{s2}, C_{s3}	1 nF
Output Capacitor, C_o	20 µF
Output Inductor, L_1, L_2, L_3	1 µH
Dual Synchronous Driver	Ideal/ADP3419
Monostable Multivibrator	Ideal/SN74121
AND Gate	Ideal/74ACT08

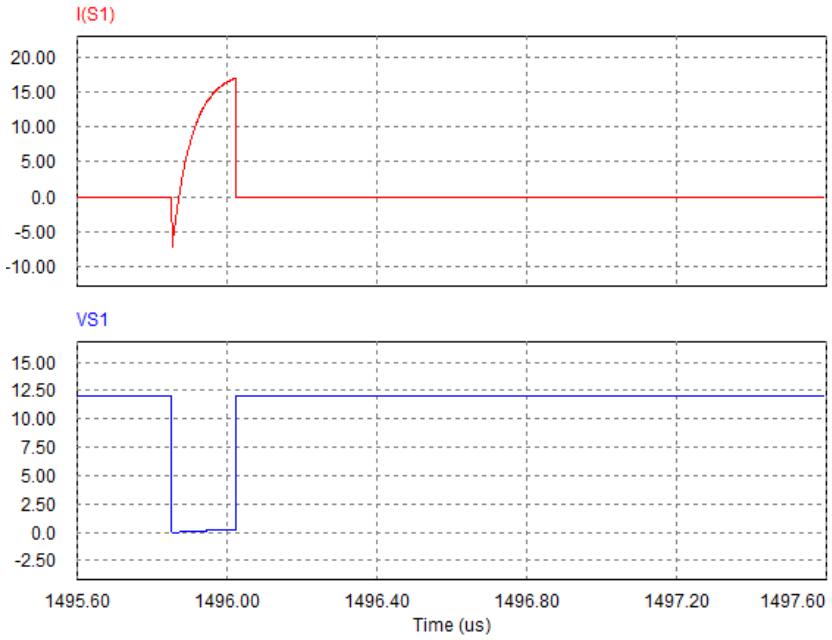


Fig. 5.4 (a) Simulated voltage and current waveforms of main switch S_1: V_{S1} in Volts; I_{S1} in Amps

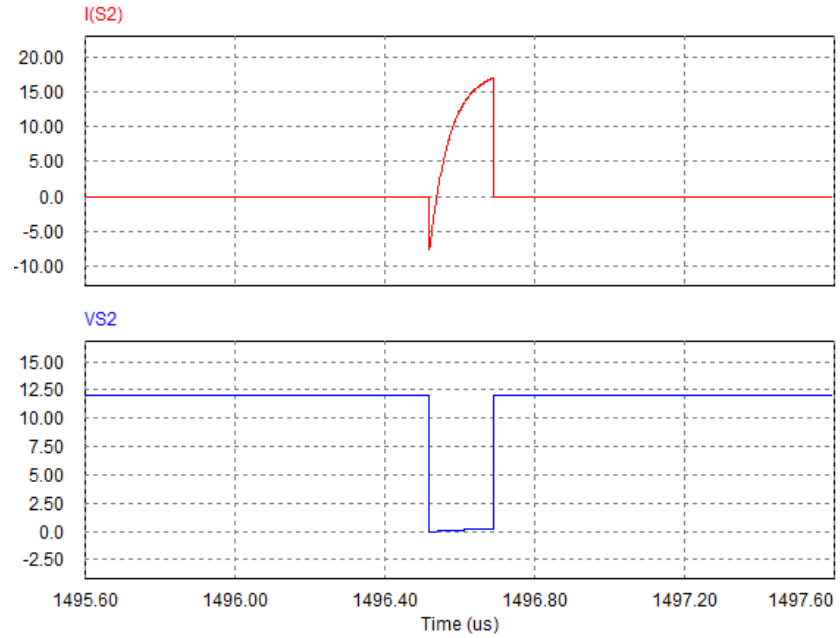


Fig. 5.4 (b) Simulated voltage and current waveforms of main switch S_2: V_{S2} in Volts; I_{S2} in Amps

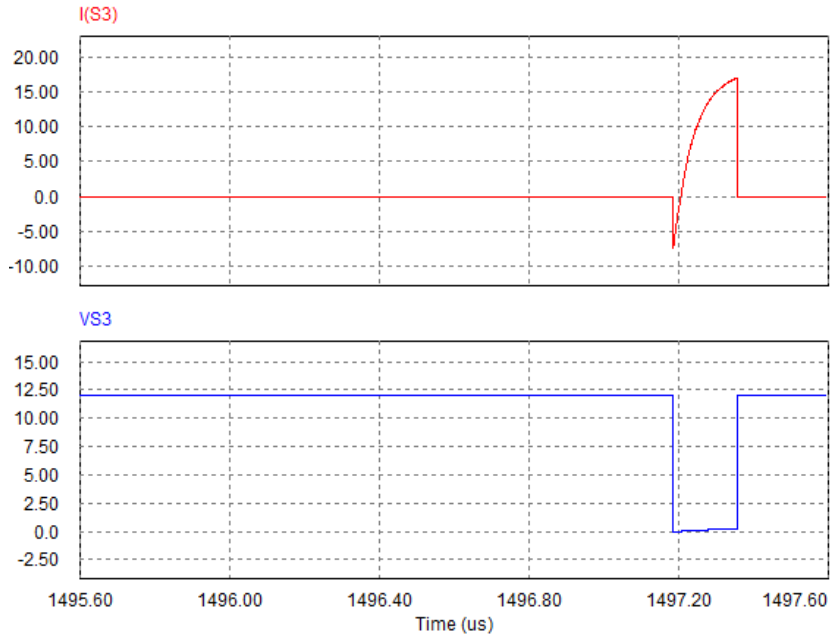


Fig. 5.4 (c) Simulated voltage and current waveforms of main switch S_3: V_{S3} in Volts; I_{S3} in Amps

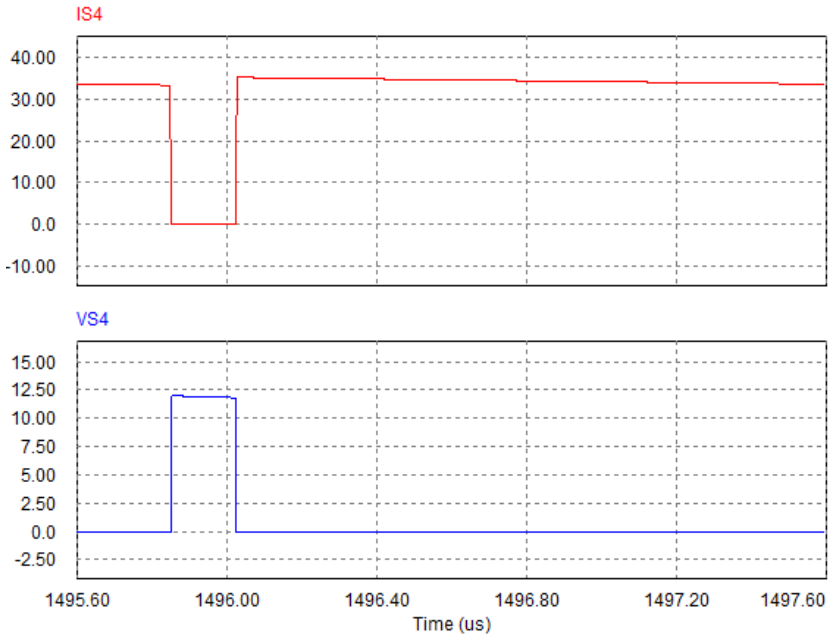


Fig. 5.4 (d) Simulated voltage and current waveforms of synchronous switch S_4: V_{S4} in Volts; I_{S4} in Amps

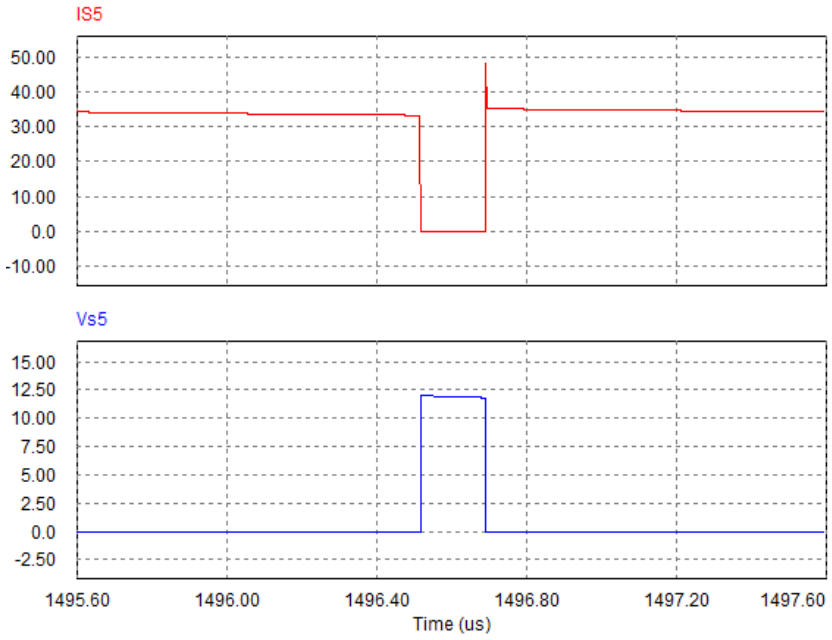


Fig. 5.4 (e) Simulated voltage and current waveforms of synchronous switch S_5: V_{S5} in Volts; I_{S5} in Amps

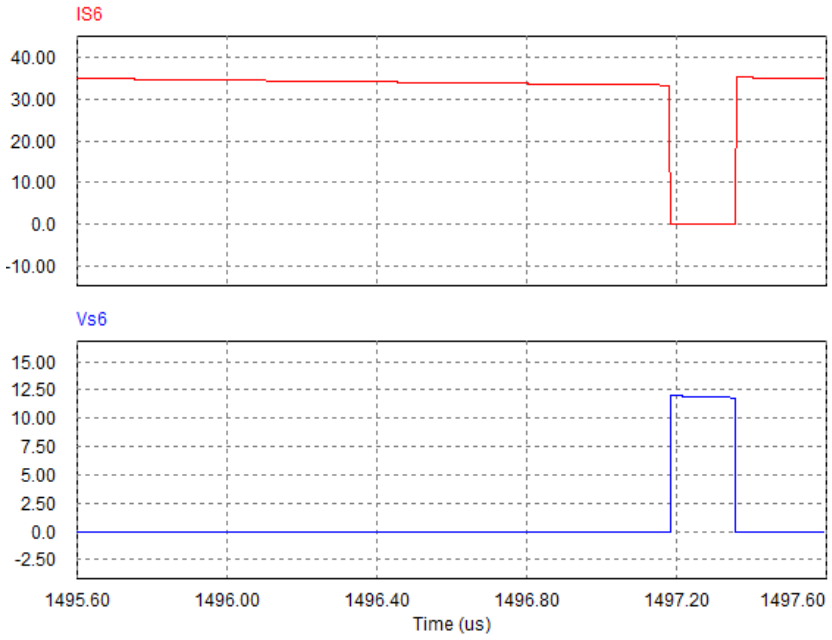


Fig. 5.4 (f) Simulated voltage and current waveforms of synchronous switch S_6: V_{S6} in Volts; I_{S6} in Amps

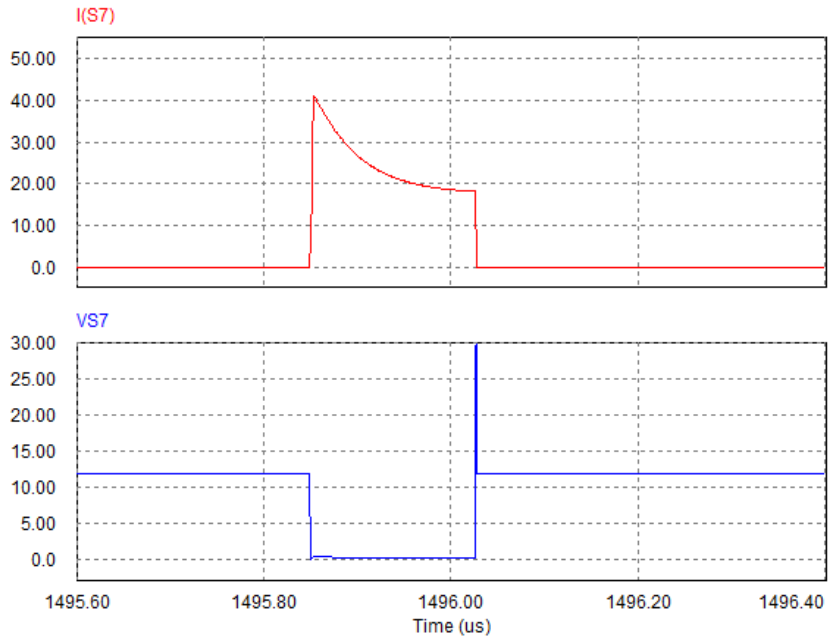


Fig. 5.4 (g) Simulated voltage and current waveforms of auxiliary switch S_7: V_{S7} in Volts; I_{S7} in Amps

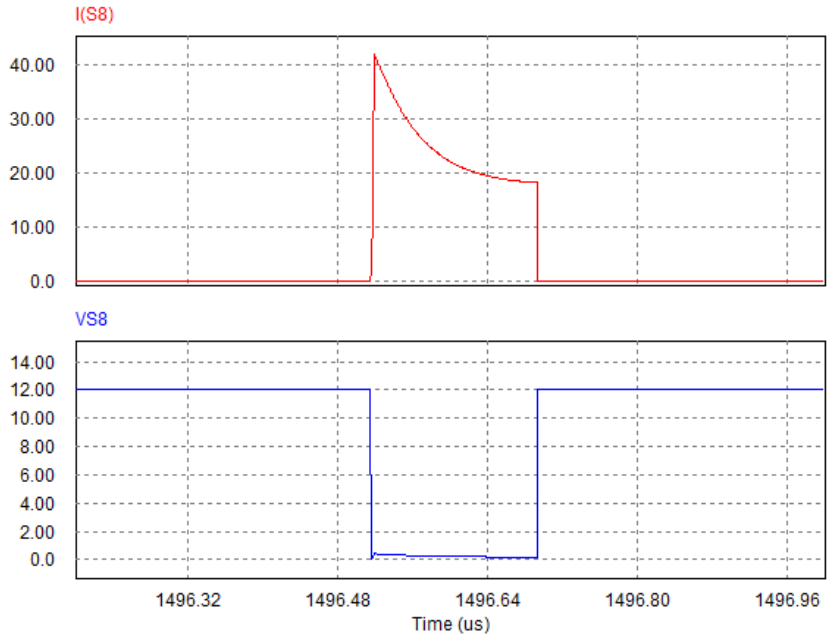


Fig. 5.4 (h) Simulated voltage and current waveforms of auxiliary switch S_8: V_{S8} in Volts; I_{S3} in Amps

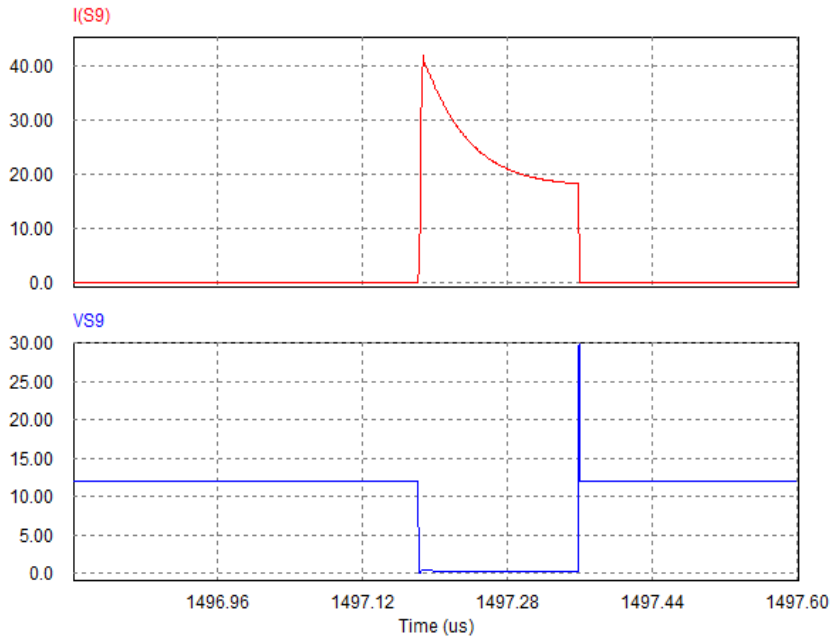


Fig. 5.4 (i) Simulated voltage and current waveforms of auxiliary switch S_9: V_{S9} in Volts; I_{S9} in Amps

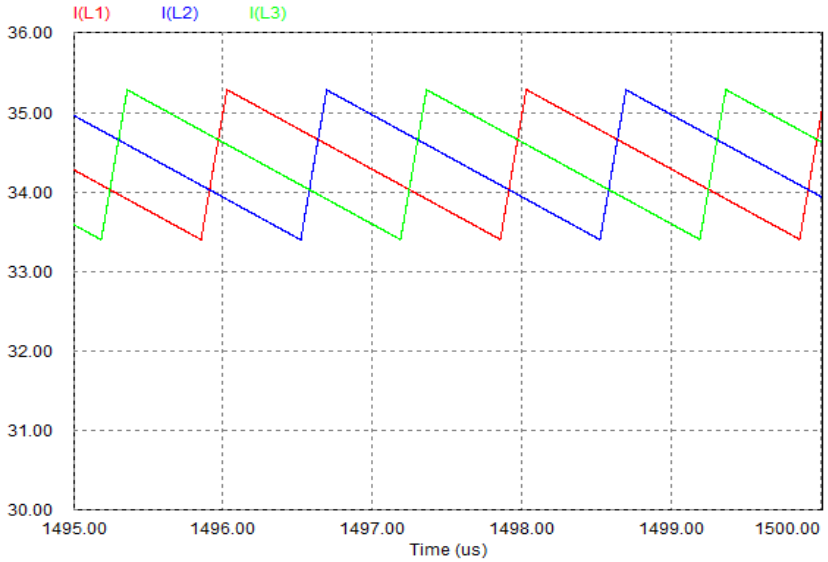


Fig. 5.4 (j) Current sharing in three phases

From the experimental results, it is concluded that the main switch, the auxiliary switch and the synchronous switch are turned on and turned off with soft switching this improves the overall efficiency of the proposed converter. The proposed topology is justified with a 500 kHz switching frequency. The experimental photograph of the proposed converter is shown in the Fig. 5.6. The efficiency graph shown in Fig. 5.7 is compared experimentally for hard switching and soft switching converter.

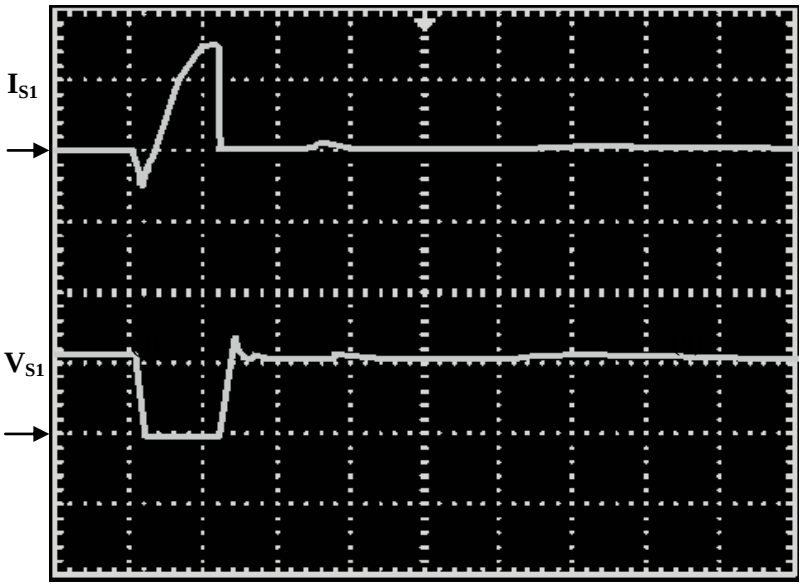


Fig. 5.5 (a) Experimental current and voltage waveforms of main switch S_1: I_{S1}(20 A/div), V_{S1}(10 V/div), 0.2 µs/div

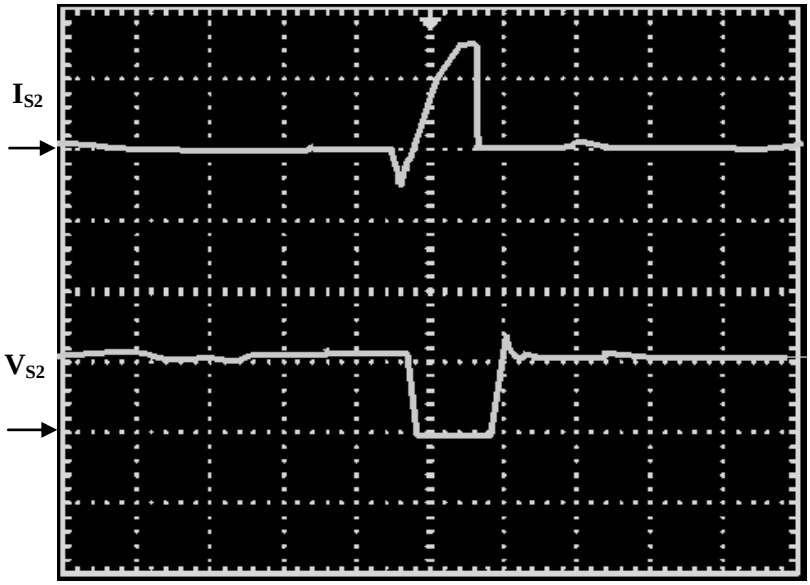


Fig. 5.5 (b) Experimental current and voltage waveforms of main switch S_2: I_{S2}(20 A/div), V_{S2}(10 V/div), 0.2 µs/div

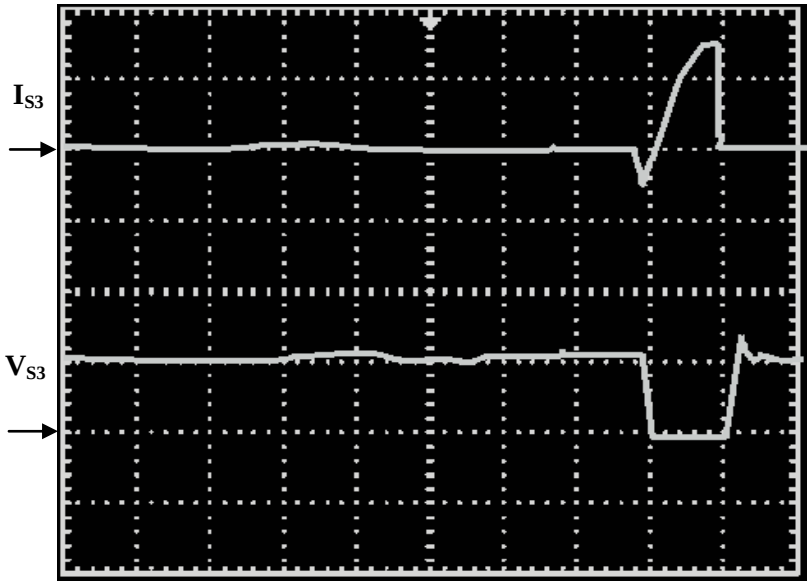


Fig. 5.5 (c) Experimental current and voltage waveforms of main switch S_3: I_{S3}(20 A/div), V_{S3}(10 V/div), 0.2 µs/div

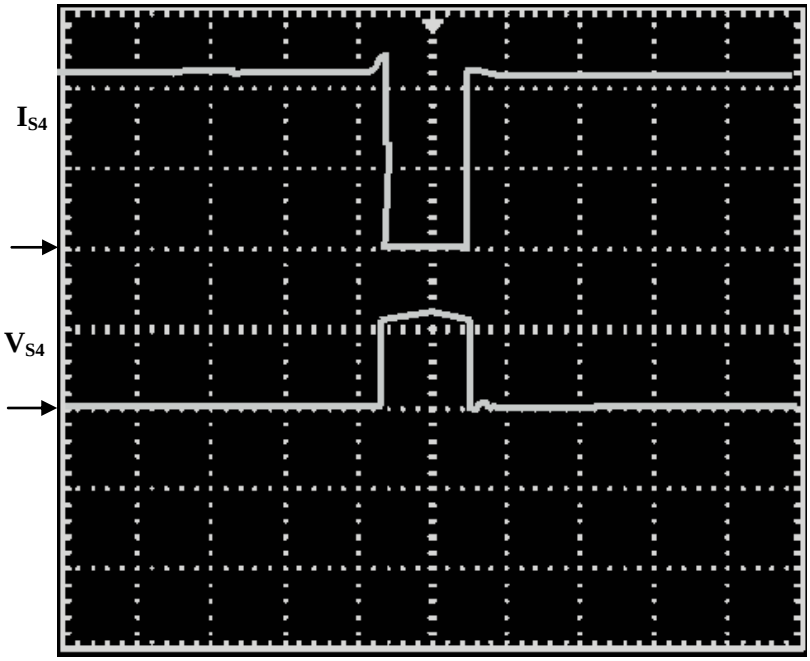


Fig. 5.5 (d) Experimental current and voltage waveforms of synchronous switch S_4: I_{S4}(15 A/div), V_{S4}(10 V/div), 0.2 µs/div

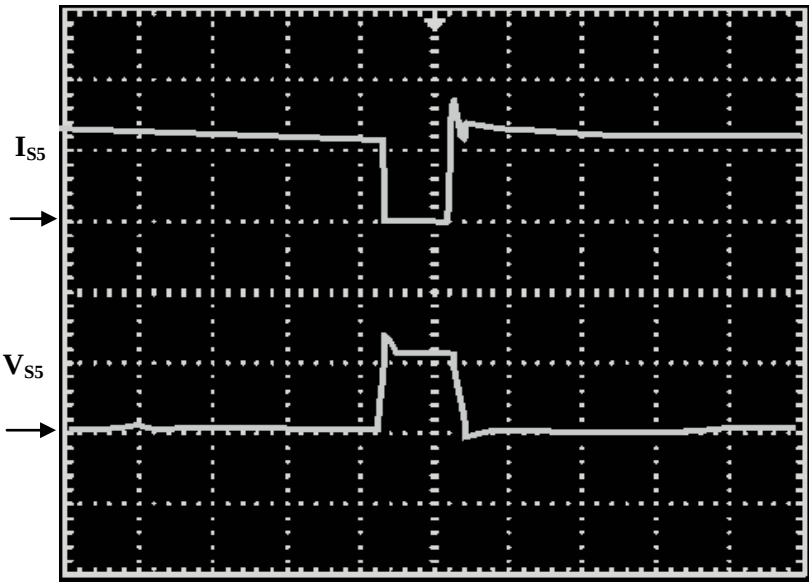


Fig. 5.5 (e) Experimental current and voltage waveforms of synchronous switch S_5: I_{S5}(20 A/div), V_{S5}(10 V/div), 0.2 µs/div

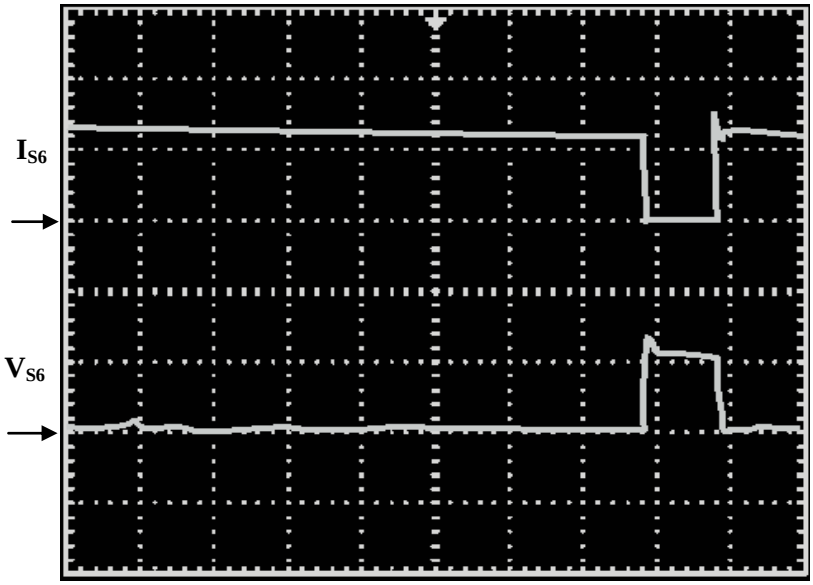


Fig. 5.5 (f) Experimental current and voltage waveforms of synchronous switch S_6: I_{S6}(20 A/div), V_{S6}(10 V/div), 0.2 µs/div

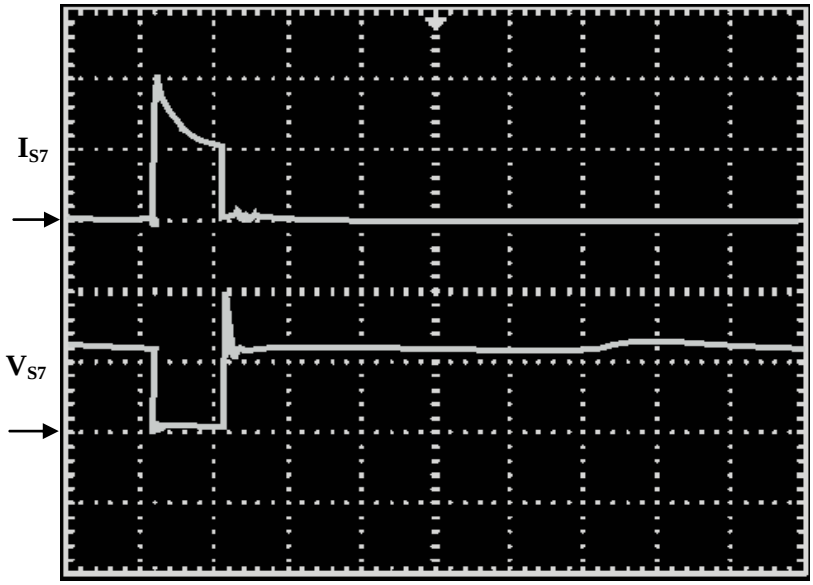


Fig. 5.5 (g) Experimental current and voltage waveforms of auxiliary switch S_7: I_{S7}(20 A/div), V_{S7}(10 V/div), 0.2 µs/div

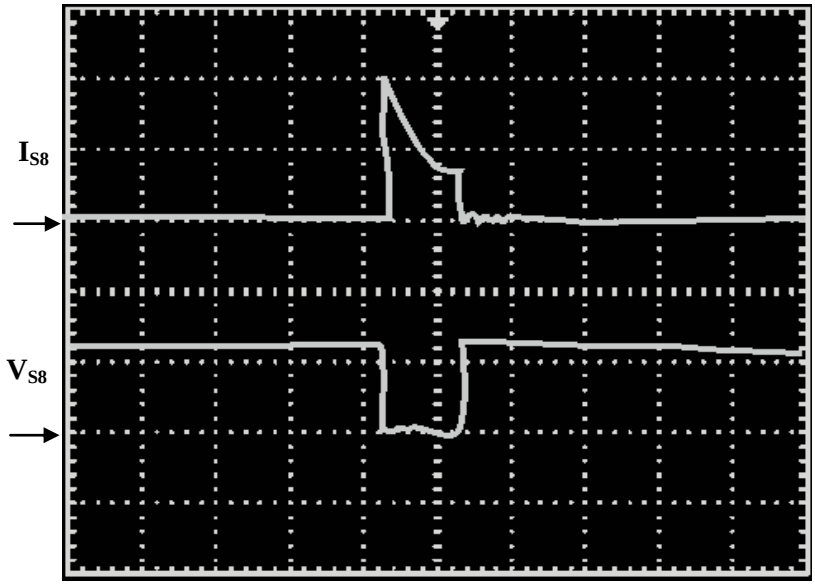


Fig. 5.5 (h) Experimental current and voltage waveforms of auxiliary switch S_8: I_{S8}(20 A/div), V_{S8}(10 V/div), 0.2 µs/div

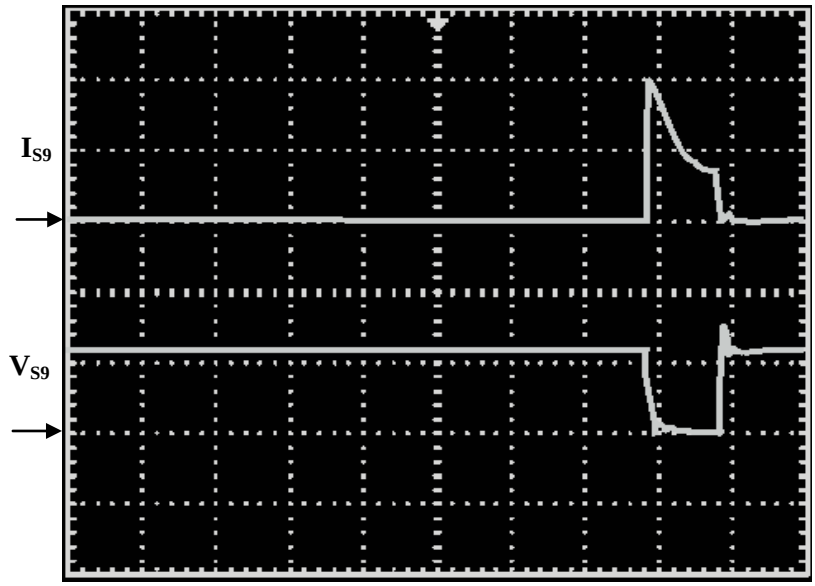


Fig. 5.5 (i) Experimental current and voltage waveforms of auxiliary switch S_9: I_{S9}(20 A/div), V_{S9}(10 V/div), 0.2 µs/div

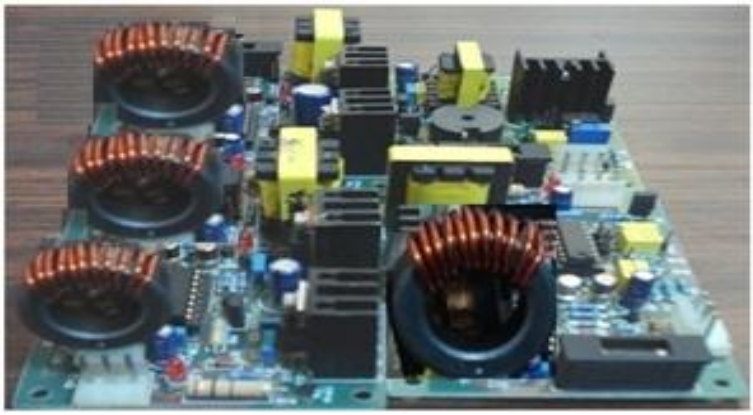


Fig. 5.6 Photograph of the proposed multiphase buck converter

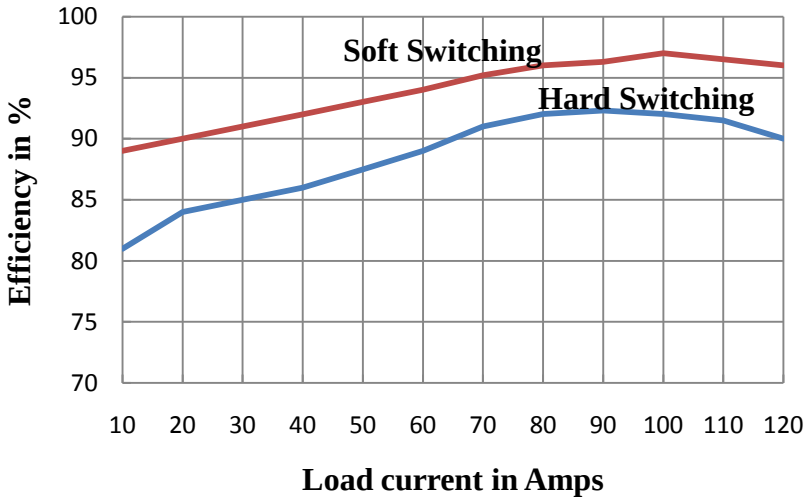


Fig. 5.7 Efficiency curve

5.6 Summary

The concept of ZVS is implemented in a multiphase synchronous buck converter and it is shown that the switching losses in the synchronous buck are reduced. A significant efficiency improvement with soft switching as compared to a hard switching converter is achieved as shown in Fig. 5.7. Both main switch and synchronous switches are turned-on and turned-off under ZCS and ZVS respectively. But auxiliary switches are turned-on and turned-off under ZCS with tolerable voltage stresses across the switch. Hence switching losses are reduced and the proposed multiphase synchronous buck is more efficient than the conventional converter. This proposed converter of high switching frequency is designed for new generation microprocessor applications.

CHAPTER 6

SUMMARY AND FUTURE WORK

Summary

Future work

Chapter 6. Summary and Future Work

The emergence of portable electronic equipments poses many challenges to the power supply designer such as: high efficiency, high power density, low cost and reliability. The improved performance switchmode converter must meet these requirements. A high efficiency dc-dc buck converter is to be designed keeping in pace with the recent developments of technologies. Dc–dc converters with extreme step-down voltage conversion ratios are required in newly promising power electronic applications, such as automotive power systems, telecommunication power systems, data communication systems, industrial controls, and distributed power systems. An extreme step-down voltage conversion ratio leads to a low duty cycle which compels to go for high switching frequency operations. Operating the converter at high frequency reduces cost and size of converter; while it increases frequency dependent losses. In this dissertation, emphases are given to two major problems: low duty cycle and switching losses.

6.1 Summary

This dissertation is engaged in exploring solutions for high step down converters and low power converters operating at a high frequency. The conventional buck converter has difficulty in dealing with very low voltage conversion ratios, because it leads to poor utilization of components as well as it degrades the system efficiency and impairs transient response. This dissertation introduces topologies to solve these problems by applying either transformer or tapped inductor structure to extend the duty cycle. In spite of having few drawbacks, transformer based topology is used in telecom power system to provide galvanic isolation.

But extended duty cycle techniques decrease power density of converter. To achieve high power density, the switching frequency has to be increased. The increase of the

switching frequency increases switching losses. Thus, the loss minimization in the low power converter is a prime issue which is accomplished by soft switching techniques.

This research presents different topologies with improved performance dc-dc converter for different applications. The specific goals of this study, based on chapters 2 to 5 can be summarized as follows:

1. For applications in telecom power system, an isolated topology is designed to extend the duty cycle, to reduce switching losses, and to reduce voltage and current stresses in the devises. The duty cycle is extended by varying the turns ratio of the transformer. Reduced ripples are produced with the effect of extended duty cycle which provides a better power density. The leakage energy is absorbed and the voltage spikes on the switches are limited by the proposed clamp capacitor scheme. The dead time is controlled with the clamp capacitor to reduce the body diode conduction loss. With the optimized turn ratio of n = 4, the filter components are designed with a tolerable ripple current and is fabricated in the laboratory. The voltage and current stresses in switches are reduced with an extended duty cycle. Furthermore, it provides a higher power density with lower number of components. All the switches are turned on and off under ZVS and ZCS. The converter has a higher overall efficiency and a wide load range control. The discussed features of the topology are authenticated with experimental results. The soft switching concept is extended to a tapped-inductor based topology at a very high frequency.
2. For low power portable applications, a ZVT synchronous buck converter is proposed. This topology is designed with active auxiliary switch and its feasibility is verified in our laboratory. The auxiliary circuit components have lower ratings than those in the main power circuit; this contributes in lower loss, because of its

very short use in a switching cycle. The concepts of ZVT used in high power conditions were implemented in a synchronous buck converter and it is shown that the switching losses in the synchronous buck were reduced. Experimental results show that the main switch and the synchronous switch are turned-on and turned-off with ZVS, and the auxiliary switch undergoes ZCS switching. In this manner, the ZVT technique reduces switching losses in the converter. The proposed ZVT SBC is highly efficient as compared to conventional SBC, which is authenticated from an efficiency graph. The efficiency graph also shows the wide load range applicability of the converter. The results show that all switches used in this topology are turned on/ turned off maintaining voltage and current stresses within the tolerable range. Moreover, the converter has a simple structure, a low cost and its control is easy. A prototype of a 3.3 V, 10 A, 200 kHz system was built to experimentally verify the improved performance.

3. For low power applications at a higher switching frequency, a passive snubber circuit is employed to achieve the soft switching in the synchronous buck converter. The proposed circuit serves as an energy recovery turn-on snubber, which greatly reduces the reverse-recovery peak current of the diode and the turn-on losses of the switches. Additionally it also provides a ZVS and/or ZCS condition for the switches to turn on or turn off. The snubber energy is recuperated to the load without using the main switch path, so conduction loss is reduced. But this additional conduction loss is present in SBC utilizing active auxiliary switch, because the transfer of the stored energy to the load takes place through the main switch. Therefore, the synchronous buck converter that employs active auxiliary switch is highly efficient. Since it uses fewer circuit components, the circuit layout is simple. The converter also operates over an extended

operating range with good efficiency. It is fabricated in the laboratory and experimental results are close to the simulation results. The excess voltage and current stresses on the main devices do not take place, and the auxiliary devices are subjected to allowable voltage and current values.

4. For low voltage and high current applications such as in new generation microprocessors, the ZVT soft switching technique is extended to a multiphase buck converter. The very narrow duty cycle in the multiphase converter compels to go for a high switching frequency which increases switching losses. Thus, a soft switching technique is implemented to improve the efficiency. The prototype model is built in the laboratory and verified in terms of efficiency improvement at a high switching frequency. From experimental and simulation results, it is shown that all switches are turned on under ZCS and are turned off under ZVS, maintaining the stresses within the tolerable range.

As a conclusion, a low duty cycle and switching losses are two major problems for power supplies for portable equipments. Solutions for these problems are discussed in the thesis with the proposed soft switching topologies.

6.2 Future work

This dissertation has tried to break through some technology barriers for future power management. Some good ideas and solutions have been explored, but further research work is necessary and which are suggested thereafter.

6.2.1 Control issues for the proposed topology

All the proposed topologies have been evaluated under open loop conditions. Different control techniques like current mode control, voltage mode control, sliding mode control,

hybrid control, hysteresis control etc., are used to improve the performance such as line regulation, transient response, output ripple voltage of buck converters.

6.2.2 Parasitic effects

In electrical circuits, the parasitic capacitance is an unavoidable and usually unwanted phenomenon that exists between the parts of an electronic component or circuit simply because of their proximity to each other. All actual circuit elements such as inductors, diodes, and transistors have an internal capacitance which can cause their behavior to depart from that of 'ideal' circuit elements. In addition, a parasitic capacitance can exist between closely spaced conductors such as wires or printed circuit board traces.

For example, an inductor often acts as though it includes a parallel capacitor, because of its closely spaced windings. When a potential difference exists across the coil, wires lying adjacent to each other at different potentials are affected by each other's electric field. They act like the plates of a capacitor, and store charge. Any change in the voltage across the coil requires an extra current to charge and discharge these small 'capacitors'. When the voltage doesn't change very quickly, as in low frequency circuits, the extra current is usually negligible, but when the voltage is changing quickly the extra current is large and can dominate the operation of the circuit.

Therefore at low frequencies parasitic capacitance can usually be ignored, but in high frequency circuits it is a major problem. Parasitic capacitance across gate and source of MOSFET can create an unwanted conduction of the switch with no gate pulse applied to it. Therefore, proper designing of converter at high frequency can minimize the effects of the parasitic capacitance.

6.2.3 Design of converter at very high switching frequency

In this thesis, several topologies are designed for switching frequency up-to 500 kHz. A high output power density in very high frequency converters has become important in recent years. This output power density of the converter is experiencing an adverse effect resulted from the applied switching frequency. Thus, further improvement on circuit analysis and PCB layout design could contribute to improve the higher operating frequency. In spite of issues resulted from the very high frequency converter design, the power device selection and PCB layout circuit design are among of the critical factors to be considered in order to maximize the capability of frequency-output power product in the very high frequency converter applications.

As frequency increases, driving high speed switches become impractical. Cell modulation on/off burst mode control technique can overcome the problem [152]. Resonant class E converter can be suitable for this operation [153].

6.2.4 System integration

The final goal of converter designers is the ability to integrate the converter together with portable electronic systems so that the parasitic in the power delivery path are minimized. This will significantly change the power delivery architecture. The advanced material and packaging technologies are key issues for reducing the passive component size so that the system integration becomes possible. Research works on a high-frequency magnetic thin-film inductor for MHz switching frequencies has been reported in some papers. The ultimate challenge is the system-level integration, in which the integration of electrical properties must be accompanied by thermal management and integration of a mechanical structure for the system integrity. Furthermore, integrated converter must be compatible with the packaging practice of the future processors. To realize this vision, we must address a

number of important technology fronts, including advanced power semiconductor devices, advanced circuit and control concepts, and advanced material and packaging technologies. The advanced material and packaging technologies are keys to reducing the passive component size so that system integration becomes possible. Research on a high-frequency magnetic thin-film inductor for the MHz switching frequency has been reported [154, 155].

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