FPGA Based Active Power Filter for Harmonics Mitigation

A Thesis Submitted in Partial Fulfilment
of the Requirements for the Award of the Degree of

Master of Technology

in
Electrical Engineering
(Power Control & Drives)

by

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Department of Electrical Engineering
National Institute of Technology Rourkela
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June 2011

Dedicated to my

Grandfather

and

Parents

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CERTIFICATE

This is to certify that the Thesis Report entitled "**FPGA BASED ACTIVE POWER FILTER FOR HARMONICS MITIGATION**", submitted by **Mr. SMRUTI RANJAN PRUSTY bearing roll no. 209-EE-2172** in partial fulfillment of the requirements for the award of **Master of Technology in Electrical Engineering** with specialization in "**Power Control and Drives**" during session 2009-2011 at National Institute of Technology, Rourkela is an authentic work carried out by him under our supervision and guidance.

To the best of our knowledge, the matter embodied in the thesis has not been submitted to any other university/institute for the award of any Degree or Diploma.

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ABSTRACT

The application of power electronics devices such as arc furnaces, adjustable speed drives, computer power supplies etc. are some typical non-linear characteristic loads used in most of the industrial applications and are increasing rapidly due to technical improvements of semiconductor devices, digital controller and flexibility in controlling the power usage. The use of the above power electronic devices in power distribution system gives rise to harmonics and reactive power disturbances. The harmonics and reactive power cause a number of undesirable effects like heating, equipment damage and Electromagnetic Interference effects in the power system. The conventional method to mitigate the harmonics and reactive power compensation is by using passive LC filters but this method has drawbacks like large size, resonance problem and fixed compensation behaviour etc., so this solution becomes ineffective [7]. Subsequently, the active power filter (APF) comes in to the picture, which gives promising solution to compensate for the above adverse effects of harmonics and reactive power simultaneously by using suitable control algorithms. Different APF topology has proposed by many authors, such as series, shunt and hybrid type and these may be based on current source or voltage source. Series APF is used to compensate the voltage harmonics and shunt type for current harmonics. As non-linear loads are injecting current harmonics to the power system, the suitable choice to eliminate current harmonics and reactive power is voltage source shunt APF. To extract the fundamental component of source current synchronous reference frame (SRF) theory [12] is suitable because of its easy mathematical calculation compared to p-q (Instantaneous theory) control algorithm. Further, switching signals to drive the VSI of the APF two popular control strategies namely hysteresis current controller (HCC) and adaptive hysteresis current controller (Adaptive-HCC) are used. Also fuzzy logic controller is used generate the reference current and maintain the DC side capacitor voltage almost constant. A comparative study of the performances of two current control strategies HCC and Adaptive-HCC is carried out in this thesis and it has been observed from simulation results that AHCC exhibits superior performance compared to the HCC. These current controllers have some disadvantages such as high cost, slow response, and large size etc., during real-time implementation. But by using digital controller one can avail the advantages like reconfigurable hardware designs, low cost developments, selection of bit width according to applications etc. In this thesis, a PI current control algorithm together with a hysteresis current controller is written in VHDL code and then is implemented using FPGA platform.

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ABBREVIATIONS

SCR: Silicon controlled rectifier

IGBT: Insulated gate bipolar transistor

MOSFET: Metal oxide semiconductor field effect transistor

APF: Active power filter

DSP: Digital signal processing

FPGA: Field programmable gate array

PCC: Point of common coupling

PLL: Phase locked loop

CSI: Current source inverter

VSI: Voltage source inverter

SPWM: Sinusoidal pulse width modulation

PI: Proportional integral

SRF: synchronous reference frame

VHDL: Very High-level Design Language

THD: Total harmonic distortion

SMPS: Switched mode power supplies

APLC: Active power line conditioners

FACTS: Flexible ac transmission

PCC: Point of common coupling

ADC: Analog to digital converter

LPF: low pass filter

FSM: Finite state machine

DFG: Data flow graph

ALU: Arithmetic and logic unit

RAM: Random access memory

CRO: Cathode ray oscilloscope

HCC: Hysteresis current controller

AHCC: Adaptive hysteresis current controller

CHAPTER 1 INTRODUCTION

1.1 BACKGROUND

In recent years both power engineers and consumers have been giving focus on the "electrical power quality" i.e. degradation of voltage and current due to harmonics, low power factor etc. Nearly two decades ago majority loads used by the consumers are passive and linear in nature, with a few non-linear loads thus having less impact on the power system. However, due to technical advancement in semiconductor devices and easy controllability of electrical power, non-linear loads such as SMPS, rectifier, chopper etc. are more used. The power handling capacity of modern power electronics devices such as power diode, silicon controlled rectifier (SCR), Insulated gate bipolar transistor (IGBT), Metal oxide semiconductor field effect transistor (MOSFET) are very large, so the application of such semiconductor devices is very popular in industry as well as in domestic purpose. Whilst these advantages are certainly good but there lies of such excessive use of power electronic devices a great problem, i.e. generation of current harmonics and reactive power in the power system network. As a result, the voltage at different buses of power system network is getting distorted and the utilities connected to these buses are not operated as designed. The harmonic current pollute the power system causing problems such as transformer overheating, voltage quality degradation, rotary machine vibration, destruction of electric power components and malfunctioning of medical facilities etc. To provide clean power at the consumer-end active power filter (APF) is used. Digital domain like micro-controller, digital signal processing (DSP) and Field programmable gate array (FPGA) implemented to the APF giving a number of advantages compared to analog controllers. Fig.1.1 shows a shunt active power filter connected to the power system at the point of common coupling (PCC). Due to use of non-linear loads, the load current is highly nonlinear in nature. The compensating current which is output of the APF is injected at PCC, so the harmonic cancellation takes place and the current between sources to PCC is sinusoidal in nature.

The active power filter (APF) is a popular approach for cancelling the harmonics in power system. The main component in the APF is the control unit. The control unit is mainly divided into two parts as follows.

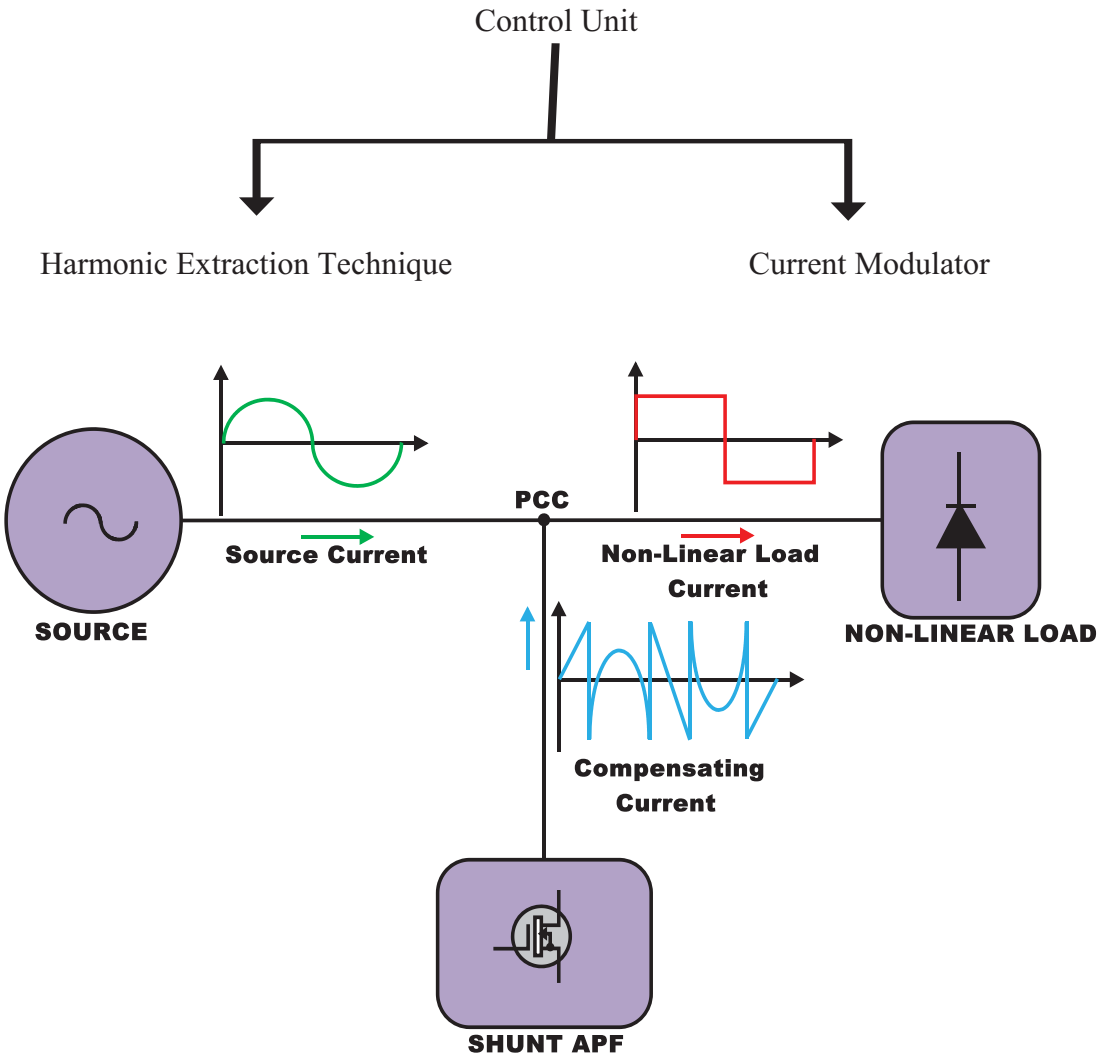

Fig.1.1 Shunt Active Power Filter

1.1.1 Harmonic Extraction:

Harmonic extraction is the process in which, reference current is generated by using the distorted waveform. Many theories have been developed such as p-q theory (instantaneous reactive power theory), d-q theory, frieze controller, PLL with fuzzy logic controller [31], neural network etc.. Out of these theories, more than 60% research works consider using p-q theory and d-q theory due to their accuracy, robustness and easy calculation.

1.1.2 Current Modulator (Gate control signal):

Current modulator is mainly used to provide the gate pulse to the active power filter (Inverter). There are many techniques used for giving the gating signals to PWM VSI such as

sinusoidal PWM, triangular PWM, hysteresis current controller, adaptive hysteresis current controller, space vector modulation and space vector with hysteresis current controller etc.

The above described two control techniques (harmonics extraction technique and current modulator technique) are main research foci of many researchers in the recent years. It may be noted that either harmonics extraction technique or the current modulator can be used individually or both at a time. Apart from these two techniques, most of the research works are directed also in dealing with multi-level inverter control problems.

1.2 LITERATURE REVIEW OF ACTIVE POWER FILTER:

1.2.1 Harmonics in Power System Due to Non-Linear Loads:

The literature study for the thesis work begins with the detection of the harmonics arising due to the use of non-linear loads. The main sources of voltage and current harmonics are due to control and energy conversion techniques involved in the power electronic devices such as chopper, rectifier, cyclo-converter etc. The harmonic sources are energy conversion devices such as power factor improvement and voltage controller devices of motor, high-voltage direct-current power converters, traction and power converters, battery-charging systems, static-var compensators, wind and solar-powered dc/ac converters, direct energy devices-fuel cells, storage batteries which require dc/ac power converters, control of heating elements[1]. The current and voltage harmonics were measured using a dynamic signal analyzer by M. Etezadi-Amoli, and plotted at for different substations [2]. Due to use of non-linear loads like rectifier, chopper etc. the load current gets distorted, which is explained nicely by Robert considering harmonic study [3].

1.2.2 Brief Introduction to Active Power Filter:

To reduce the harmonics conventionally passive L–C filters were used and also capacitors were employed to improve the power factor of the ac loads. But the passive filters have several drawbacks like fixed compensation, large size and resonance problem. To mitigate the harmonics problem, many research work development are developed on the active power (APF) filters or active power line conditioners [4-5].

1.2.3 Various Topology of Active Power Filter:

APLC's are basically categorized into two types, namely, single phase (two-wire connection), three-phase (three wire and four-wire connection) configurations to meet the

requirements of the nonlinear loads in the distribution systems. Single-phase loads, such as domestic lights, TVs, air conditioners, and laser printers behave as nonlinear loads and cause harmonics in the power system [6]. Many configurations, such as the active series filter [7], active shunt filter [8-9], and combination of shunt and series filter has been developed [10]. The above mentioned APLC's either based on a current source inverter (CSI) with inductive energy storage or voltage source inverter (VSI) with capacitive energy storage devices.

1.2.4 Control techniques used for Active Power Filter:

Designing a suitable controller for an APF is very important. A number control strategies such as instantaneous reactive power theory initially developed by Akagi et al. [11], synchronous frame d–q theory [12], synchronous detection method [13], notch filter and fuzzy logic controller [32] method are used in the development of three-phase AFs and the gate pulses are generated by current control technique like sinusoidal pulse width modulation (SPWM), triangular PWM, hysteresis current control technique [14].

1.2.5 Digital Controller for Active Power Filter:

Advancement in Microelectronics has motivated new directions for APF design starting from the use of analog and digital components to microprocessors, microcontrollers, digital signal processors (DSP's) [15-16] and FPGA implementation [17-18]. Further, these developments have made it possible to use different control algorithm such as proportional integral (P-I), fuzzy logic etc. for improving the steady state and dynamic performance of APFs. By implementing this performance, response as well as the cost is efficient compare to the analog one.

1.3 MOTIVATION OF PROJECT WORK:

As discussed before, power distribution system is polluted by harmonic and reactive power disturbances due to the large usages of non-linear loads (Computers, Laser printers, SMPS, Rectifier etc.), which is undesirable. It is a gigantic challenge to eliminate the undesirable current harmonics and condensate the reactive power from the power system. The performances of Conventional method (LC filter) is not satisfactory due to the drawbacks as discussed. The shunt APF takes the challenge and gives promising results compare to conventional one based up on suitable control algorithms. The control algorithms play a vital role for the development of the APF. Mainly two controllers are needed for APF

one is for extracting the reference current and another to giving the gating signal to the PWM VSI. But as discussed these analog controller having drawbacks during real-time implementations and the difficulties can be overcome by adopting digital controller (DSP or FPGA). As per as the digital processor is concerned, the FPGA is given the highest priority as compared to DSP because of its low cost development, faster response, application oriented selection of the bit width for the data resister.

1.4 OBJECTIVES OF THE THESIS:

The objectives of thesis are as follows.

- To analyze the effect of non-linear loads on power system.
- To study different methods already proposed for mitigation of harmonics due to non-linear loads.
- Design of synchronous reference frame (SRF) controller.
- Design of Hysteresis current controller.
- Design of Adaptive Hysteresis current controller.
- Design of Digital Hysteresis current controller for pulse generation by writing suitable VHDL code.
- To propose a hard-ware for APF along with digital controller to mitigate current harmonics and reactive power compensation.

1.5 THESIS ORGANISATION:

Chapter 1 deals with an introduction about active power filter. It also includes a comprehensive literature review of different topology of active power filter and its control schemes. Also focus towards the motivation and objectives of the project works.

Chapter 2 deals with harmonics, brief idea about linear and non-linear load. The quality which describes the voltage and current distortion are also explained. The source which causes the current harmonics and the effect of the current harmonics is described.

In **chapter 3**, different topology of the active power filter is explained based on the converter type, active power filter connection and phases of the system. The APF model which is used for the project work is also explained.

Chapter 4 deals with the control strategy for APF. Both analog and digital controller is explained. In analog controller SRF and Fuzzy logic controller along with hysteresis and

adaptive hysteresis is described. In digital part VHDL code is written for the digital hysteresis current controller and algorithm is explained.

Chapter 5 deals with the simulation results and discussion. A comparative analysis is made between two current control methods i.e. hysteresis current controller and adaptive hysteresis current controller. The output of fuzzy logic along with hysteresis current controller is described. The results of the digital hysteresis current controller are also described.

Chapter6 deals with the conclusion and suggestion for future work.

CHAPTER 2

HARMONICS RELATED TO POWER SYSTEM

2.1 INTRODUCTION:

"Harmonics" means a component with a frequency that is an integer multiple (where n is the order of harmonic) of the fundamental frequency; the first harmonic is the fundamental frequency (50 or 60 Hz). The second harmonic is the component with frequency two times the fundamental (100 0r 120 Hz) and so on. As shown in Fig.2.1 harmonic distortion can be considered as a sort of pollution of the electric system which causes problems if the sum of the harmonic currents exceeds certain limits. The utilization of electrical power mainly depends up on supply of power with controllable frequencies and voltages, where as its generation and transmission takes place at nominally constant levels. So to convert nominal frequency to variable frequency power electronics circuitry (non-linear loads) is needed, which distorts the voltage and current waveforms. Therefore, the main source of harmonics in the power systems is the non linear loads [24].

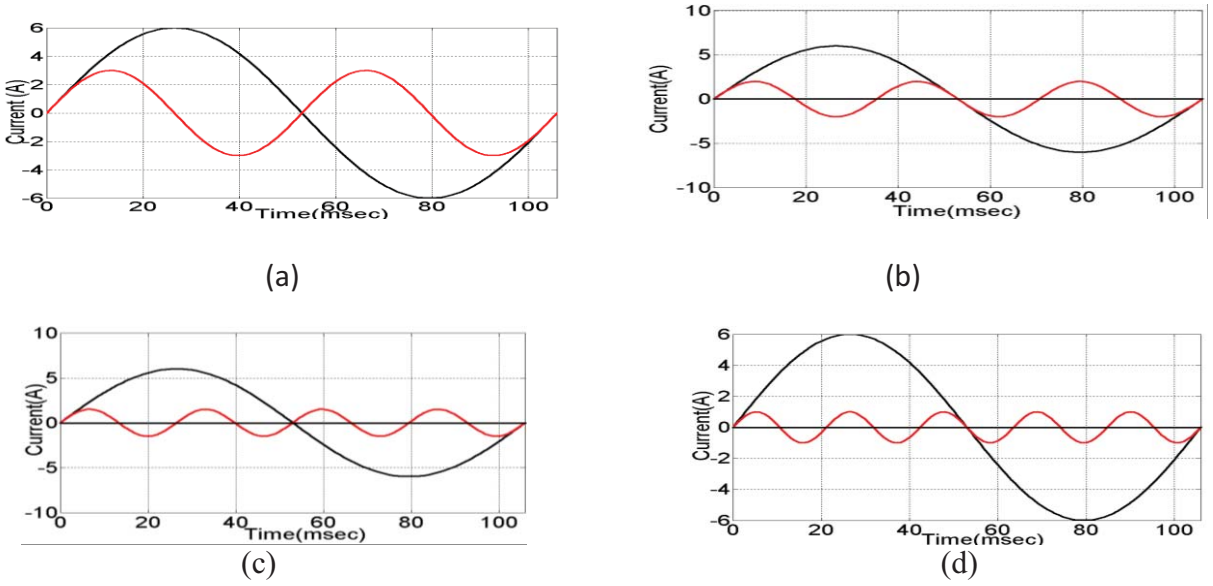

Fig. 2.1 A sinusoidal waveform with fundamental frequency 50 Hz and its harmonics: (a) second (100 Hz); (b) third (150 Hz); (c) fourth (200 Hz); (d) fifth (250 Hz)

The French mathematician Jean Baptiste Joseph Fourier (1768–1830), demonstrated that any periodic waveform can be deconstructed into a sinusoid at the fundamental frequency with a number of sinusoids at harmonic frequencies. A DC component may complete these purely sinusoidal terms. This concept can be explained by the following equation:

$$f(x) = \frac{a_0}{2} + a_1 \cos x + b_1 \sin x + a_2 \cos 2x + b_2 \sin 2x + \ldots\ldots + a_n \cos nx + b_n \sin nx$$

$$= \frac{a_0}{2} + \sum_{n=1}^{\infty} an \cos nx + \sum_{n=1}^{\infty} bn \sin nx \quad (2.1)$$

$$= \frac{a_0}{2} \sum_{n=1}^{\infty} c_n \sin(nx + \phi_n) \quad (2.2)$$

where f(x) = General periodic waveform

a_0 = D.C component

a_n, b_n = Coefficients of the series

n = Integer number

T = 2π is the period

$$a_0 = \frac{1}{\pi} \int_0^{2\pi} f(x)dx \quad , \quad b_n = \frac{1}{\pi} \int_0^{2\pi} f(x)\cos(nx)dx \quad , \quad x = \sqrt{a_n{}^2 + b_n{}^2} \quad , \quad \emptyset_n = tan^- \frac{a_n}{b_n}$$

2.2 LINEAR AND NON LINEAR LOADS:

2.2.1 Linear Loads:

AC electrical loads where the voltage and current waveforms are sinusoidal and the current at any time proportional to voltage are treated as linear loads. If pure sinusoidal voltage is passed through the resistive element, then the shape of the current wave form will be purely sinusoidal without distortion. Voltage and current waveform in a circuit involving inductor make voltage lead current. On the other hand for a circuit involving capacitor, current leads voltage

2.2.2 Non-Linear Loads:

AC loads where the current is not proportional to the voltage are considered as nonlinear loads. Non-linear loads generate harmonics in the current waveform that leads to distortion of the voltage waveform; under these conditions the voltage is no longer proportional to the current. Table 2.1 shows the examples of linear and non-linear loads and comparison between them.

TABLE 2.1 Comparisons Between Linear And Non-Linear Loads:

Sl. No.	Linear Loads	Nonlinear Loads
1	Examples; Power Factor Improvement Capacitor, Heaters, Incandescent Lamps. Etc	Examples; Computer, Laser Printer, SMPs, Rectifier, Refrigerator etc
2	Ohms law is valid	Ohms law is not valid
3	Load current does not contain harmonics.	Load current contains all odd harmonics.
4	Could be inductive or capacitive.	Can't be categorized as leading or lagging loads.
5	Zero neutral current, if 1-Phase loads are equally balanced on 3-Phase Mains (Vector sum of line current)	Even if single phase loads are equally balanced on 3-phase neutral current could be 2.7 times the line current.
6	May not demand high inrush currents while starting.	Essentially very high inrush current (20 time of Normal) is drawn while starting for approximant One cycle.

2.3 QUANTITIES DESCRIBING VOLTAGE AND CURRENT DISTORTION:

Voltage or current distortion can be characterized in either the time or the frequency domain. Description in the time domain consists of finding the differences between the actual, distorted waveform values and the reference sinusoidal waveform values. Due to difficulty in determining these differences by means of measurement, this method has limited use. The distortion description in the frequency domain is commonly accepted. The most complete information is provided by the set of numbers determining the orders, amplitudes (R.M.S values) and phases of individual harmonics. The quantities defined below are the bases of power quality standardization.

2.3.1 Peak factor:

The ratio of the peak and R.M.S value of a periodic waveform is called as peak factor, for a sinusoidal wave peak factor is 1.41. This factor is restricted for certain design tasks, e.g. selecting semiconductor devices according to the voltage/current peak value. Mathematically, the peak factor is defined as below.

$$\text{Peak factor} = \frac{U_{peak}}{U} \tag{2.3}$$

where U_{peak}= peak value of periodic wave form.

U = R.M.S value of periodic wave form.

2.3.2 Total Harmonic Distortion (THD):

The total harmonic distortion (THD), of a signal is a measurement of the harmonic distortion present and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency. Harmonic distortion is caused by the introduction of waveforms at frequencies in multiplies of the fundamental i.e. 3rd harmonic is three multiplied by the fundamental frequency (150Hz). THD is a measurement of the sum value of the waveform that is distorted.

$$THD = \frac{\sqrt{\left(V_2^2 + V_3^2 + ... + V_N^2\right)}}{V_1} \tag{2.4}$$

The THD is a very useful quantity for many applications. It is the most commonly used harmonic index. However, it has the limitation that, it is not a good indicator of voltage stress within a capacitor because that is related to the peak value of voltage waveform.

2.4 SOURCES OF CURRENT HARMONICS:

Among the sources of harmonic voltages and currents in power systems three groups of equipment can be distinguished:

- Magnetic core equipment, like transformers, electric motors, generators, etc.
- Arc furnaces, arc welders, high-pressure discharge lamps, etc.
- Electronic and power electronic equipment.

2.4.1 Transformers:

The first source of harmonics of power systems is transformer. The relationship between the primary voltage and current is shown in Fig.2.2 as a magnetization curve is strongly non-linear and hence its location within the saturation region causes distortion of the magnetizing current. Transformers are designed so that the magnetizing current will not exceed 1–2% of the nominal current. The nominal operating point is located below the knee of the magnetizing curve, within its linear region. As a result, even if a large number of transformers are operated in the power system, they are not a significant source of harmonics under normal operating conditions. This condition may change because of a slight voltage increase for a short interval of time. Within the saturation region even a small voltage increase above the nominal value results in a large increase in the magnetizing current. Also the harmonic content rises significantly.

For instance, at the voltage above the nominal point (U_N), the magnetizing current third-harmonic value may increase up to 50 %. This may occur under low-load conditions in the cable networks or as a consequence of switching (on or off) large reactive power loads, e.g. switching off shunt reactors or switching on a capacitor bank. The effects of switching are transients which propagate in the system and can cause transformer saturation and sometimes over a large area.

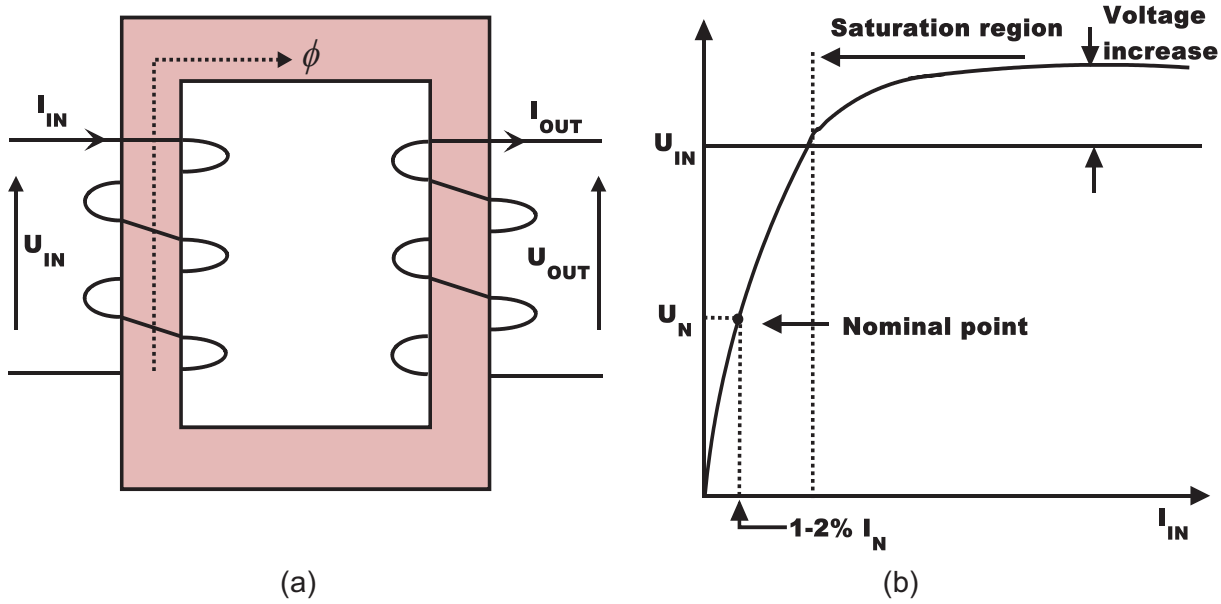

Fig.2.2 (a) Schematics diagram, (b) transformer magnetization curve

2.4.2 Motors and Generators:

Motors can also generate harmonic currents in order to produce a magnetic field but less compare to transformer due to very small magnetizing characteristics. The magnetizing characteristic of motors is much more linear compared to the transformer due to the presence of air gap. The pitch of motor winding can also be a root of harmonic currents. Typical motor windings have 5–7 slots per pole, which results in the generation of the fifth or seventh harmonic. In spite of the fact they are incomparably smaller than high harmonics in converter equipment; their presence is noticeable in the case of very large motors. Harmonics (of very small magnitude) also occur in generator voltage, since for both practical and economic reasons a spatial distribution of the stator windings which could guarantee a purely sinusoidal voltage waveform is neither advisable nor possible. The induced voltages are therefore slightly distorted, and usually the third harmonic is the dominant one. It causes the third-harmonic current flow under generator load conditions.

2.4.3 Arc Furnaces:

Distortion of arc furnace is an important issue because of their common use and large in comparison to the short-circuit capacity at the point of connection with individual powers. Moreover, for technological reasons, arc furnaces are presently operated at a lower power factor than in the past. The form of the furnace voltage and current waveforms implies that representation of their distortion employing a discrete spectrum. These waveforms, having the nature of stochastic variables, are non-periodic functions of time as Fig.2.3. A continuous spectrum between the dominant harmonics has the nature of white noise of significant value.

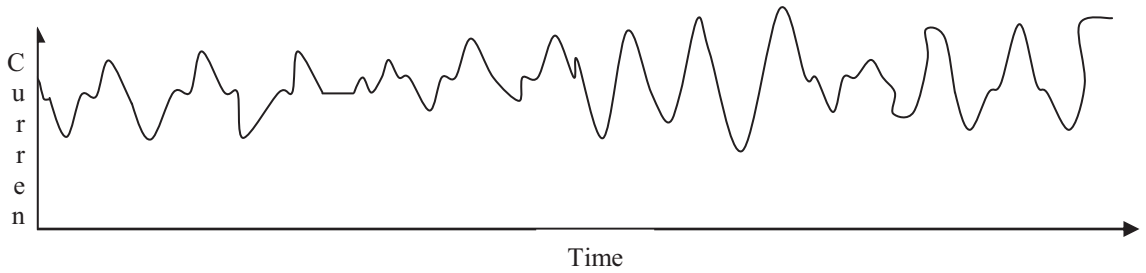

Fig.2.3 Example time graph of a furnace current during the starting phase of melting

2.4.4 Switched Mode Power Supplies (SMPS):

The major part of modern electronic devices is fed by switched mode power supplies (SMPS) with single-phase rectifiers. The main difference from older units is in the lack of the traditional step-down transformer and rectifier: they are replaced by direct controlled rectification of the supply to charge a reservoir capacitor from which the direct current for the load is derived in order to obtain the output voltage and current required. With this approach, the main advantage is that size, cost and weight have been reduced and the power unit can be made with practically any form factor. The disadvantage introduced is that now, instead of drawing continuous current from the supply, the unit draws pulses of current which contain large amounts of third- and higher-order harmonic components.

2.5 EFFECTS OF HARMONICS:

The voltage or current distortion limit is determined by the sensitivity of loads (also of power sources), which are influenced by the distorted quantities. The least sensitive is heating equipment of any kind. The most sensitive kind of equipments are those electronic devices which have been designed assuming an ideal (almost) sinusoidal fundamental frequency voltage or current waveforms. Electric motors are the most popular loads which are situated between these

two categories. An example classification of the effects of the presence of high harmonics is given in Table 2.2.

TABLE 2.2 Effects of current and Voltage Harmonics:

Classification of Criterion	Type of Effect	Comments
Period	Very short-term effects	These effects are associated with a failure, malfunction or inoperative state of equipment exposed to high harmonics, such as control and instrumentation equipment, electronic equipment, IT equipment, etc.
	Long-term effects	Mainly of thermal nature. The thermal effect (causing accelerated ageing of insulation) is a function of many variables, of which the most important are the values and orders of harmonics.
Physical Nature Of The Distorted Quantity	Current effects	Related to the instantaneous or time-averaged current value (overheating of electric machines, capacitor fuses blowing, increased losses in transmission lines, unwanted operation of relays, etc.). Harmonics in power supply systems are the main cause of temperature rise in the equipment and shortening of in-service time.
	Voltage effects	Related with the peak, average or RMS value of distorted voltage.

2.6 CHAPTER SUMMARY:

This chapter describes the basic definition of the harmonics and expression of harmonics by using Fourier analysis. The main source corresponding to the harmonics is the non-linear load and a comparison between two types of load namely linear and no-linear loads are made. The quantity which describes the current or voltage harmonics and the source of harmonics in power systems are described. The effects of harmonics in power system are also explained in this chapter.

CHAPTER 3

ACTIVE POWER FILTERS

3.1 INTRODUCTION:

To cancel the harmonics and compensate the reactive power APF is the suitable solution. The APF concept is to use an inverter to inject currents or voltages harmonic components to cancel the load harmonic components. The more usual configuration is a shunt APF to inject current harmonics into the point of common coupling (PCC). The APF can be installed in a low voltage power system to compensate one or more loads; thus, it avoids the propagation of current harmonics in the system. The developments of different control strategies give APF to a new location. As APF compensate the reactive power and cancel the harmonics, it is also called as active power line conditioners (APLC). The concept of shunt APLC was first introduced by Gyugyi and strycula in 1976 [26].

The three main aspects of an active power conditioner are:

- The configuration of power converter (the scheme and the topology of converter and the electronics device used)
- The control strategy (the calculation of APLC control reference signals)
- The control method used (how the power inverter follows the control reference)

3.2 CONFIGURATION OF ACTIVE POWER FILTERS:

APF's can be classified based on converter type, topology, and the number of phases.

- The converter type is mainly two types.
  - Voltage source inverter (VSI)
  - Current source inverter (CSI)
- The topology of active power filter is classified in to three types.
  - Series active power filters
  - Shunt active power filters
  - Hybrid active power filters
- Finally based on the phases the APF mainly two types.
  - Two-wire (single phase) system.
  - Three or four-wire three-phase system.

3.2.1 Voltage Source Inverter (VSI):

In voltage source inverter (VSI) the dc voltage always has one polarity, and the power reversal takes place through reversal of dc current polarity. For reasons of economics and performance, VSI's are often preferred over current source inverter (CSI) for flexible ac transmission (FACTS). Since the direct current in a VSI flows in either direction, the converter valves have to be bidirectional, and also, since the dc voltage doesn't reverse, the turn off device need not to have reverse voltage capability. IGBTs, MOSFETs etc may have parallel reverse diode built in as a part of complete integrated device suitable for voltage source inverter. Figure 3.1 topology of the VSI. On the dc side, voltage is unipolar and is supported by capacitor. This capacitor is large enough to at least handle a sustained charge or discharge current that accompanies the switching sequence of the converter valves and shifts in phase angle of the switching valves without significant change in the dc voltage.

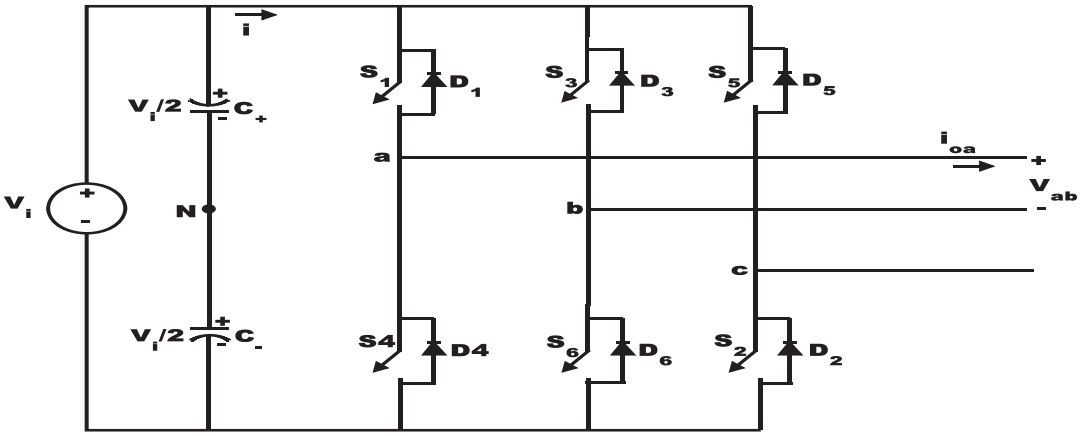

Fig.3.1 Basic topology of a voltage source inverter

3.2.2 Current Source Inverter (CSI):

A current-sourced inverter (CSI) is characterized by the fact that the dc current flow is always in one direction and the power flow reverses with the reversal of dc voltage. Basically there are three types of CSI i.e. Diode inverter, Line-commutated inverter, Self commutated inverter. For flexible AC transmission (FACTS) application self commutated inverter is preferred and basically it is based on turn off devices (MOSFET, IGBT etc.), in which commutation of current from valve to valve takes place with the device turn-off action and provision of ac capacitors, to facilitate transfer of current from valve to valve. Whereas, in a voltage sourced converter the

commutation of current is supported by a stiff dc bus with a dc capacitor. The figure 3.2 shows the topology of CSI [25].

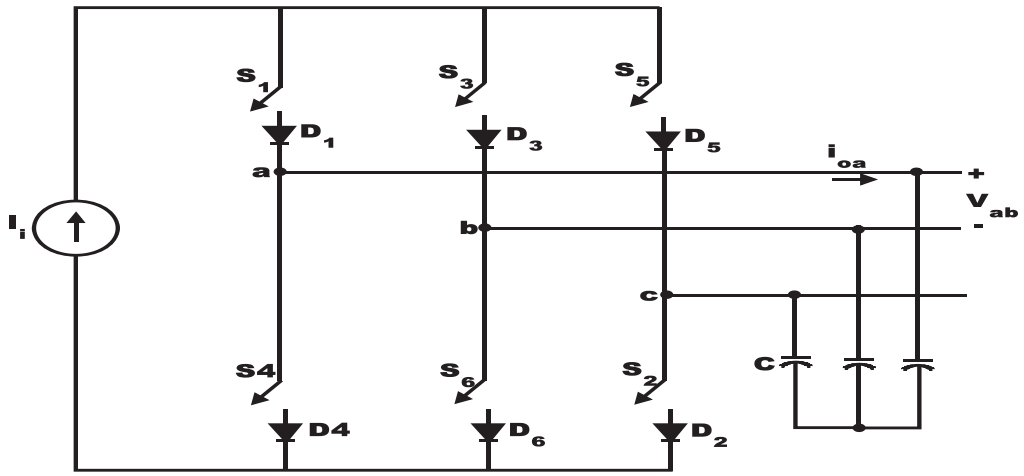

Fig.3.2 Basic topology of a current source inverter

3.2.3 Series Active Power Filter:

Fig.3.3 shows the connection scheme of a series APLC. It is connected to the power system through coupling transformer. The compensation voltage is used to cancel the voltage harmonics of load.

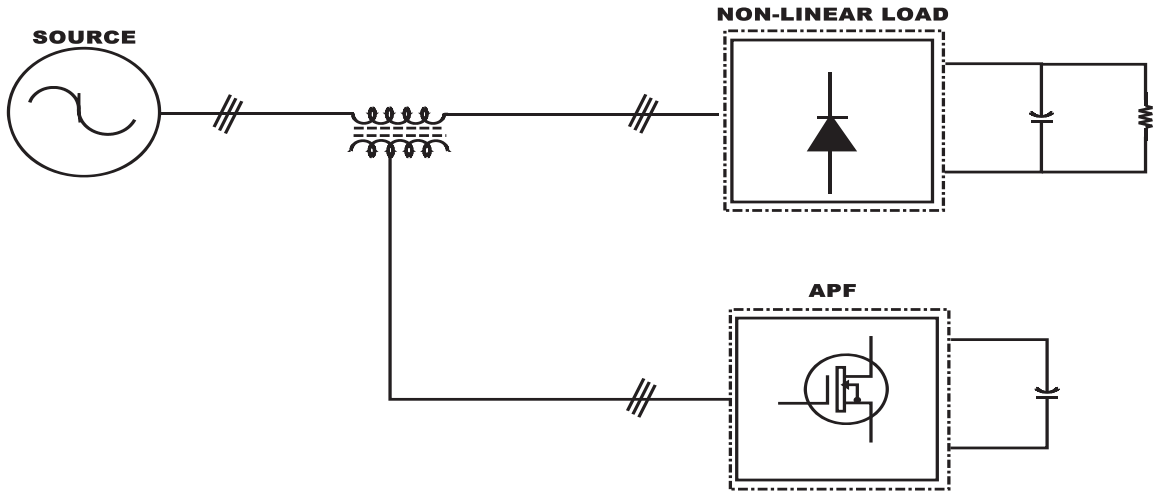

Fig.3.3 A series APLC scheme

The performance scheme of series APLC is shown in figure 3.4. The APLC supplies a compensating voltage as in Fig.3.4b. These harmonic components cancel the voltage harmonics of the load. After the compensation, the source voltage will be sinusoidal bas shown in Figure3.3c [26-27].

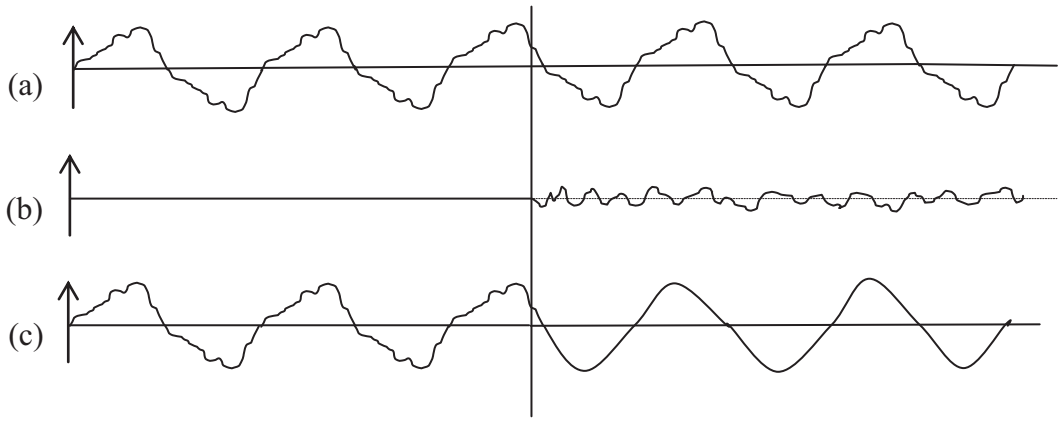

Fig.3.4 Performance schemes of series active power filter.

3.2.4 Shunt Active Power Filter:

The more usual APLC configuration is the shunt or parallel connection. Fig.3.5 shows the basic scheme of the connection, where the MOSFET switching device represents the APLC power block. The loads with current harmonics can be can be compensated by this APLC configuration [28].

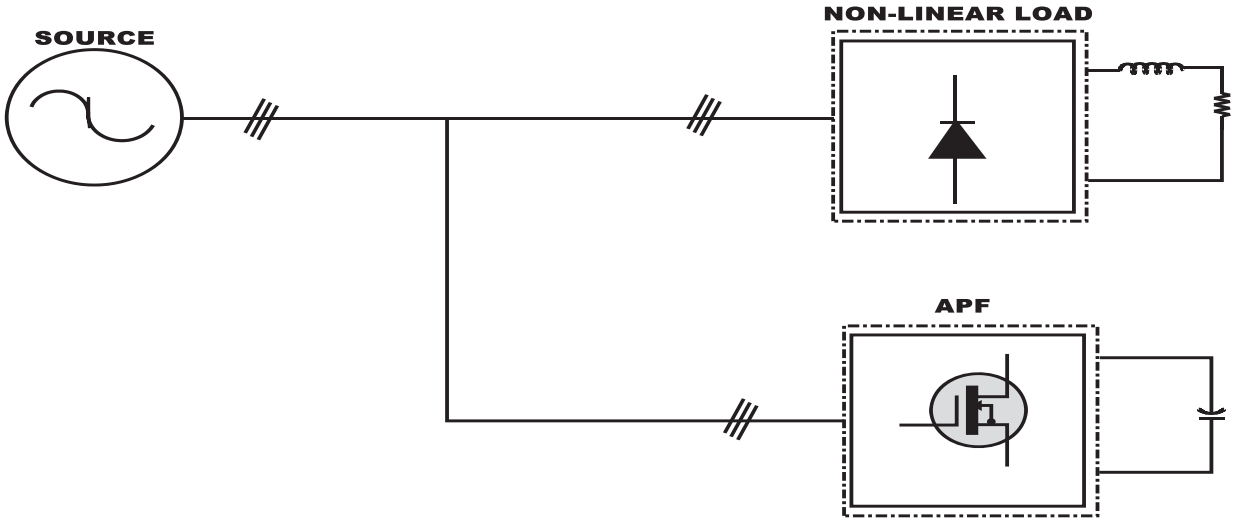

Fig.3.5 A shunt APLC scheme.

3.2.5 Hybrid Active Power Filter:

To reduce the cost of the static compensation, combination of static and passive filters is called as hybrid active power filter. The passive filters are used to cancel the most relevant harmonics of the load, and the active filter is dedicated to improving the performance of passive filters or to cancel other harmonics components. As a result, the total cost decreases without reduction of efficiency. Fig.3.6, 3.7 and 3.8 shows the more usual hybrid topologies [29].

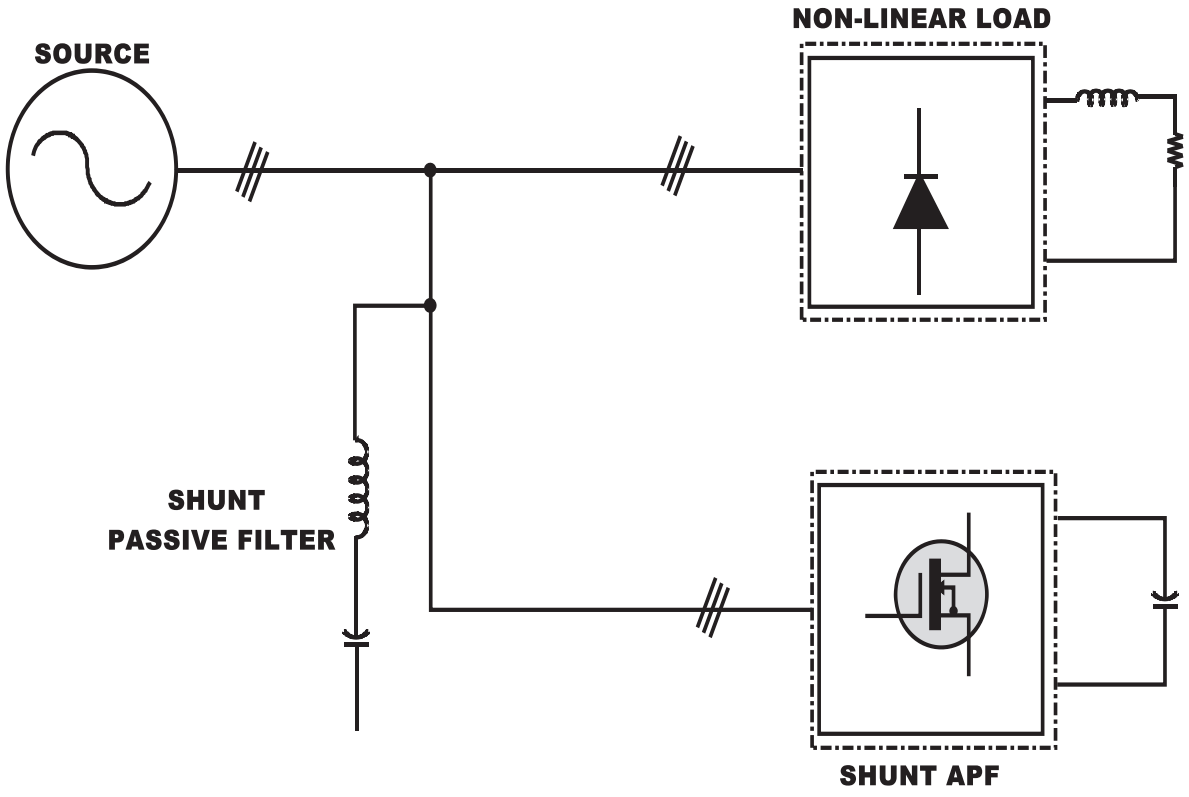

Fig.3.6 Hybrid filter with a shunt passive filter and a shunt active filter

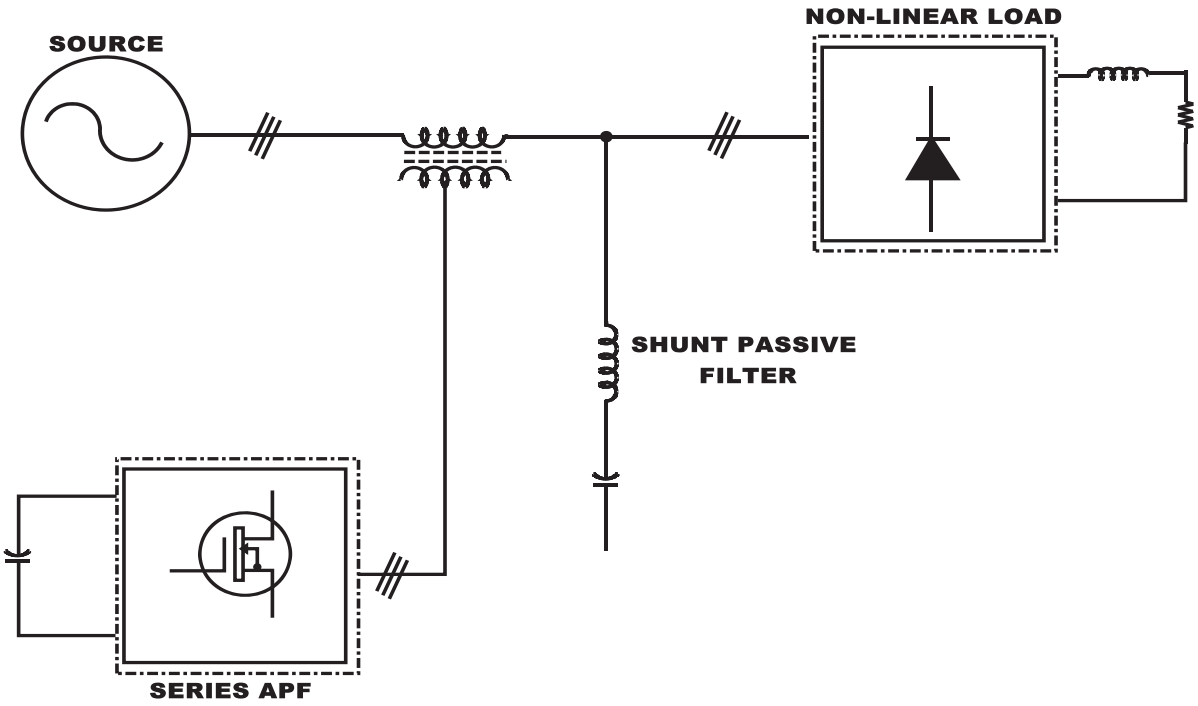

Fig.3.7 Hybrid filter with a shunt passive filter and a series active filter

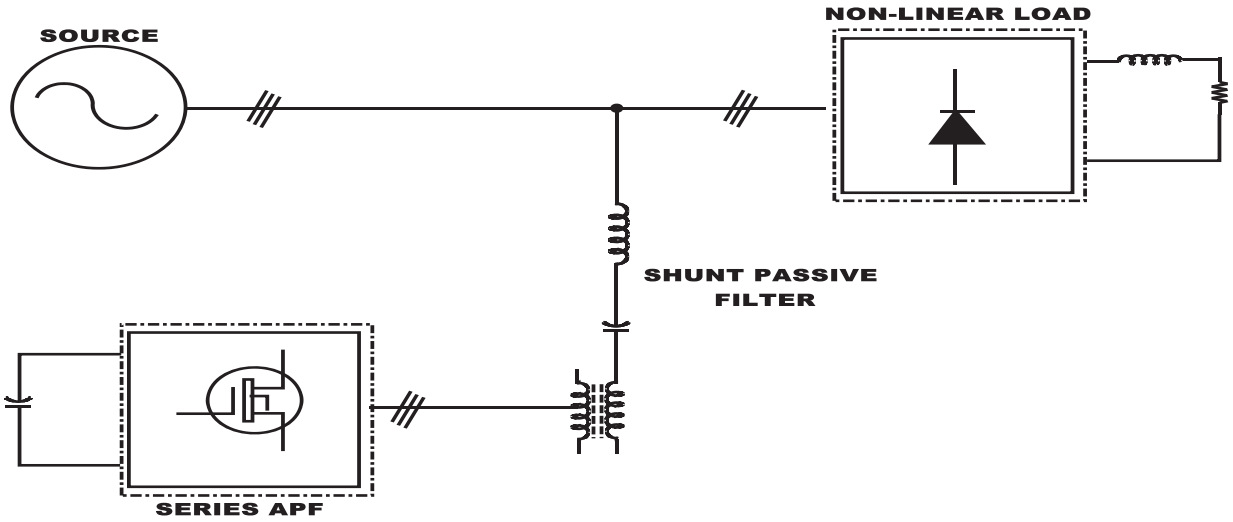

Fig.3.8 A shunts passive filter and a shunt active filter and an active filter in series with it

3.2.6 Two-Wire (Single Phase) System:

Two-wire (single phase) system is available in three mode of configuration (active series, active shunt and combination of both). Also available according to converter configuration i.e. current source PWM with inductive energy storage elements and voltage source PWM with capacitive dc-bus energy storage elements.

3.2.7 Three or Four-Wire Three-Phase System:

There are several nonlinear loads with three phase configuration. In three phase four wire systems with unbalanced loads, it is possible to use three single phase inverters as an APLC power circuit. The main objective is to compensate the phase by phase. In general, in four wire power systems, it is usual to use APLCs with three phase configurations. I n this case, a split capacitor will be necessary in the DC side [30].

3.3 APF SYSTEM STUDIED:

3.3.1 APF with Analog Current Controller (HCC and AHHC):

Figure 3.9 shows the basic structure of shunt active power filter. It consists of the following parts.

1. A three phase source
2. A non-linear load (three phase bridge rectifier with R-L load)
3. A voltage source PWM inverter
4. Controller (both to generate reference current and gating signal for PWM VSI)

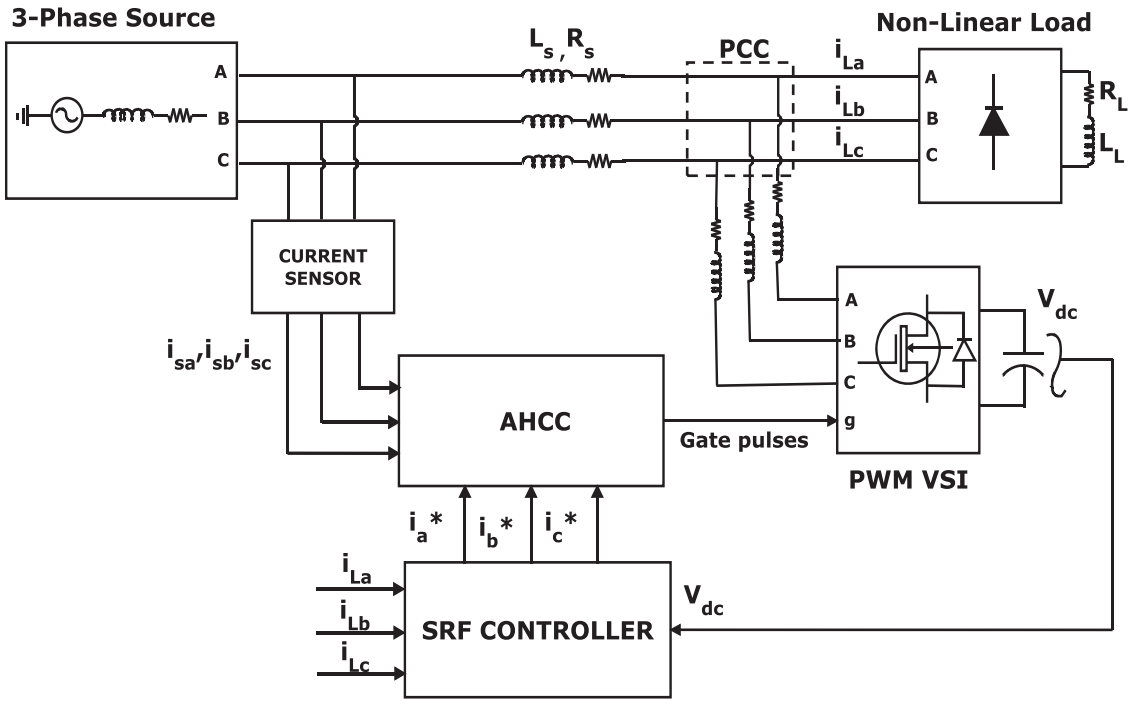

Fig.3.9 SRF with AHCC based APF implemented with PWM VSI configuration

In Fig.3.9, the 3-phase source is connected to the three phase non-linear load (3-phase diode bridge rectifier) with load resistance (R_L) and load inductance (L_L). The L_s and R_s represent the line inductance and resistance respectively. Due to the non-linear load, the load current (i_{La}, i_{Lb}, i_{Lc}) is non-linear in nature. The control part is used for generation of reference current (SRF controller) and providing gate signal (Hysteresis Current Controller and Adaptive Hysteresis Current Controller) to the PWM voltage source inverter. The non-linear current is sensed by the current sensor and voltage across the capacitor is sensed by the voltage sensor. Finally the current controller is provided the gate pulses to the PWM voltage source inverter. The output of the inverter 'i_c' is called as compensating current, which is injected to the power system at the point of common coupling (PCC) with opposite phase to the load current.

3.3.1.1 Modeling of Non-Linear Load:

The non-linear load is considered as a 3-phase bridge diode rectifier with R-L load. Figure 5.2 shows the circuit diagram of the non-linear load. The diodes are arranged in three legs. Each leg has two series connected diodes. Upper diode D1, D3, D5 constitutes the positive group of diodes. The lower diodes D2, D4, D6 form the negative group of diodes. Positive group of diodes conduct when these have the most positive anode. Similarly, negative group of diodes

would conduct if these have the most negative anode. Due to the presence of source inductance, six overlapping and six lion-overlapping conduction intervals occur in a cycle. The dynamic equations during non-overlap and overlap intervals are given in (8) and (9), respectively:

$$pi_d = \frac{\left(V_0 - \left(2R_S + R_L\right) i_d - 2v_d\right)}{2L_S + L} \tag{3.1}$$

$$pi_d = \frac{\left(V_0 - \left(1.5R_S + R_L\right) i_d - 2v_d\right)}{1.5L_S + L} \tag{3.2}$$

Where, Rs and Ls are the elements of the source impedance, v_d is the drop across each device, RL, and L are the elements of load impedance, id is the load current flowing through the diode pairs and 'p' is the differential operator (d/dt). Vo is the AC side line voltage segment v_{ac}, vbc, vba, vcb, vab ,v_{cc} during non-overlap intervals, and $(v_{bc}+v_{ac})$ /2, $(v_{ba}+v_{bc})/2$, $(v_{ca}+v_{ba})/2$, $(v_{cb}+v_{ca})/2$, $(v_{ab}+v_{cb})/2$ and $(v_{ac}+v_{ab})/2$ during overlap intervals, based on diode pair conduction. The phase currents i_{sa}, i_{sb}, i_{sc} are obtained by considering the respective diode pair combination.

3.3.2 APF with Digital Current Controller:

Fig.3.10 shows the digital hysteresis current controller with APF. Three phase source is connected to the three phase bridge rectifier load (Non-linear load). Here SRF controller is used for extracting the fundamental component of current. To implement digital controller to APF

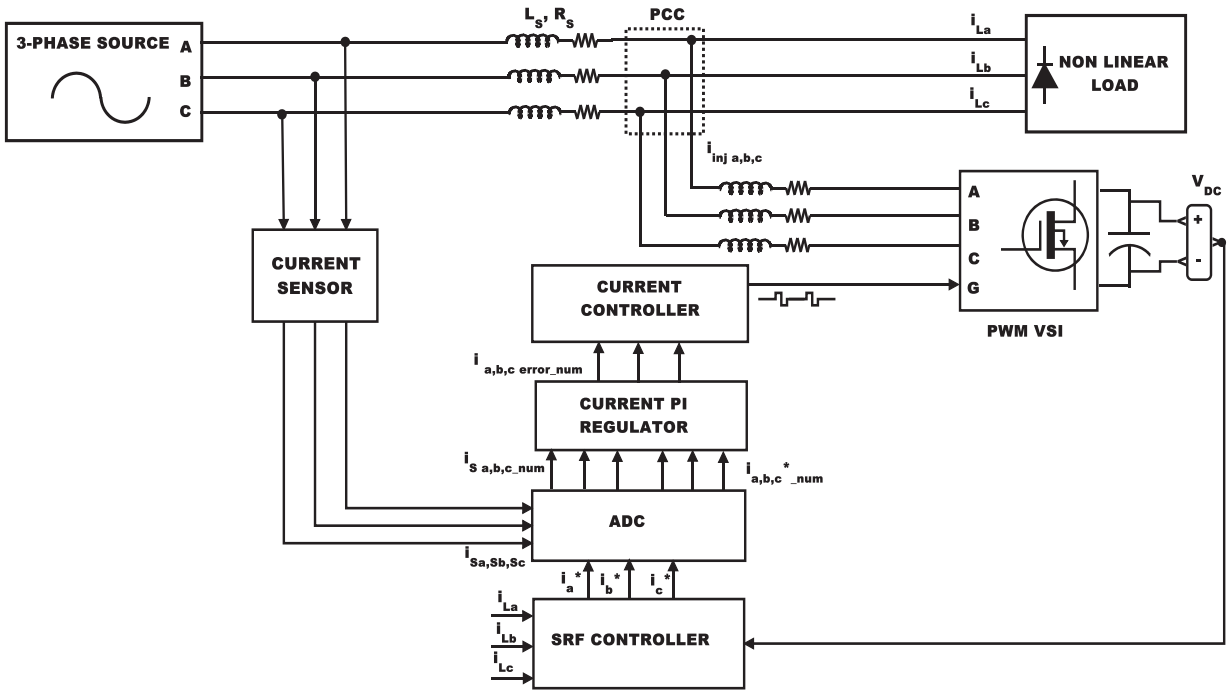

Fig.3.10 SRF with digital HCC based APF implemented with PWM VSI configuration

analog to digital (ADC) converter is needed. The ADC will convert analog value in to digital domain. The analog value of source current and reference current are given to the ADC and the output of ADC gives the digital value of reference and source current. These two currents are given to the PI current controller, which gives the error signal and that error signal is given to the digital hysteresis block and the output of the digital hysteresis block gives gating signal to PWM VSI for drive the MOSFET. The output of PWM VSI is generating compensating signal, which is fed to PCC for cancellation of harmonics between the source to the load.

3.4 CHAPTER SUMMARY:

This chapter has described different topologies of APF and the merits and demerits of the each topology are explained. It is shown that shut active power filter is suitable for eliminating the current harmonics. The APF model used for the project work is described (both analog and digital current controller); the modeling of the non-linear loads is explained.

CHAPTER 4

ANALOG AND DIGITAL CONTROLLER OF APLC

4.1 INTRODUCTION:

The heart of the APLC is the controller part. For providing harmonic suppression and reactive power compensation, the shunt active power filter is a suitable choice. The controller of active power filter mainly divided into two parts i.e. reference current generation and PWM current controller. In reference current generation scheme, reference current is generated by using the distorted wave form. Many control schemes are there for reference current generation, such as p-q theory, PLL controller and neural network etc. The PWM current controller is principally used for providing gating pulse to the active power filter.

4.2 FUNDAMENTAL COMPENSATION PRINCIPLE:

Figure 4.1 shows the fundamental idea of shunt current compensation. As shown in the Fig.4.1 the source is connected to non-linear load. The non linear load injecting current harmonics to the power system, so the shape of the load current is highly non-linear,

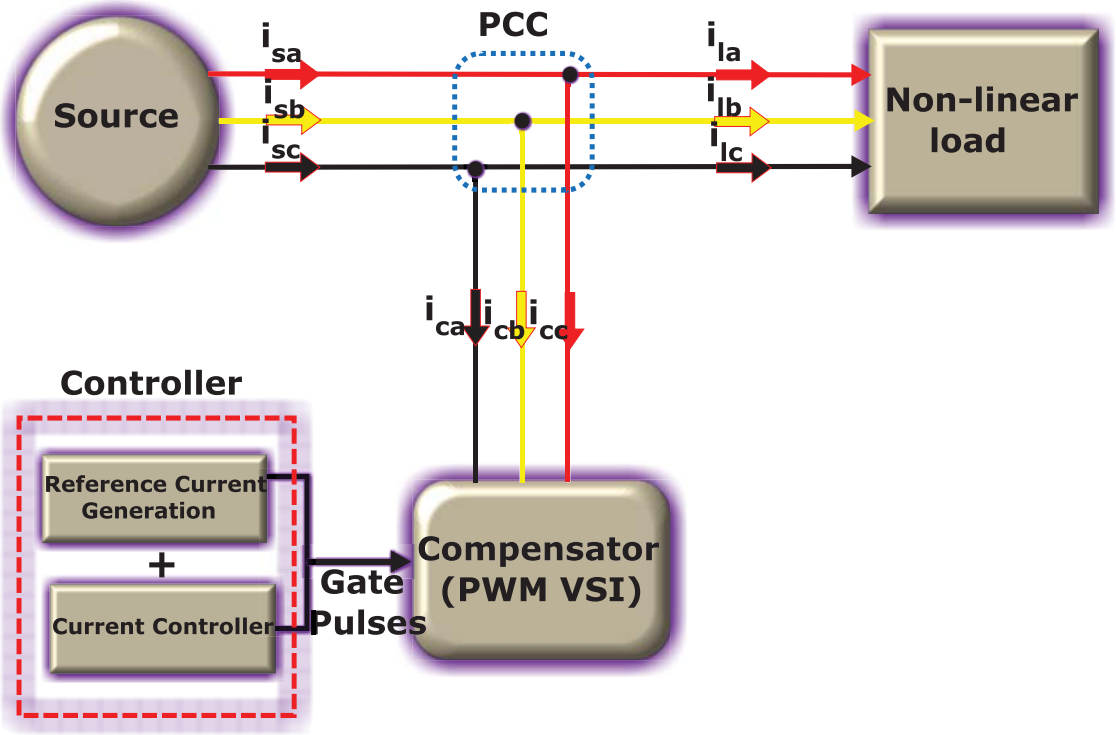

Fig.4.1 Basic principle of shunt current compensation

here the role of the APF is to inject the current harmonics exactly in the opposite phase at the point of common coupling (PCC). As a result the harmonic gets cancelled by the compensating current, so the shape of the source current remains sinusoidal from source to PCC. To produce the compensating current, control algorithm plays a big job. The control algorithm used for APF is basically divided in to two parts one is to generate the reference current signal and the other is for generating gate pulses for PWM VSI.

4.3 SRF CONTROLLER:

The synchronous reference frame theory or d-q theory is based on time-domain reference signal estimation techniques. It performs the operation in steady-state or transient state as well as for generic voltage and current waveforms. It allows controlling the active power filters in real-time system. Another important characteristic of this theory is the simplicity of the calculations, which involves only algebraic calculation. The basic structure of SRF controller consists of direct (d-q) and inverse $(d\text{-}q)^{-1}$ park transformations as shown in Fig.4.2. These can useful for the evaluation of a specific harmonic component of the input signals [19].

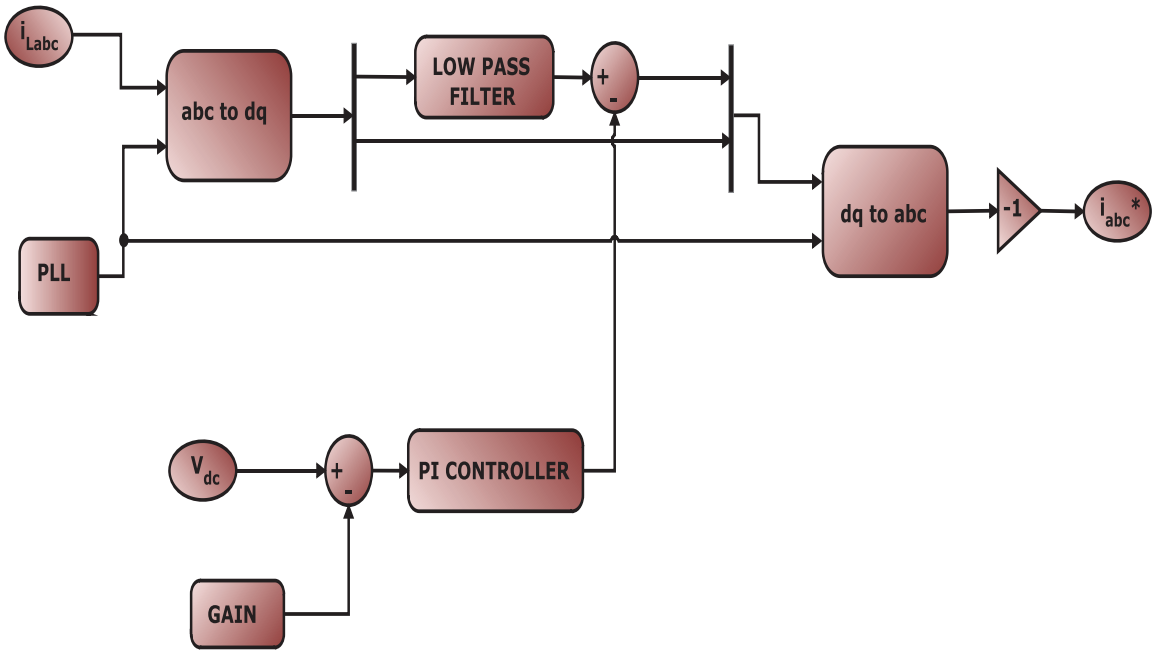

Fig.4.2 Synchronous d-q-0 reference frame based compensation algorithm

The reference frame transformation is formulated from a three-phase a–b–c stationary system to the direct axis (d) and quadratic axis (q) rotating coordinate system. In a-b-c, stationary axes are separated from each other by 120^0 as shown in Fig.4.3 The instantaneous space vectors, v_a and i_a are set on the a-axis, v_b and i_b are on the b-axis, similarly v_c and i_c are on the c-axis.

These three phase space vectors stationary coordinates are easily transformed into two axis d-q rotating reference frame transformation. This algorithm facilitates deriving i_d-i_q (rotating current coordinate) from three-phase stationary coordinate load current i_{La}, i_{Lb}, i_{Lc}, as shown in equation 4.1.

$$\begin{pmatrix} i_{Ld} \\ i_{Lq} \\ i_{L0} \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} \cos(\theta) & \cos(\theta - 2\pi/3) & \cos(\theta + 2\pi/3) \\ \sin(\theta) & \sin(\theta - 2\pi/3) & \sin(\theta + 2\pi/3) \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{pmatrix} \begin{pmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{pmatrix} \tag{4.1}$$

The d-q transformation output signals depend on the load current (fundamental and harmonic components) and the performance of the Phase Locked Loop (PLL). The PLL circuit provides the rotation speed (rad/sec) of the rotating reference frame, where ωt is set as fundamental frequency component. The PLL circuit provides the vectorized 50 Hz frequency and 30^0 phase angle followed by sinθ and cosθ for synchronization. The id-iq current are sent through low pass filter (LPF) for filtering the harmonic components of the load current, which allows only the fundamental frequency components. The LPF is a second order Butterworth filter, whose cut off frequency is selected to be 50 Hz for eliminating the higher order harmonics. The PI controller is used to eliminate the steady state error of the DC component of the d-axis reference signals. Furthermore, it maintains the capacitor voltage nearly constant. The DC-side capacitor voltage of PWM-voltage source inverter is sensed and compared with desired reference voltage for calculating the error voltage. This error voltage is passed through a PI controller whose propagation gain (KP) and integral gain (KI) is 0.1 and 1 respectively.

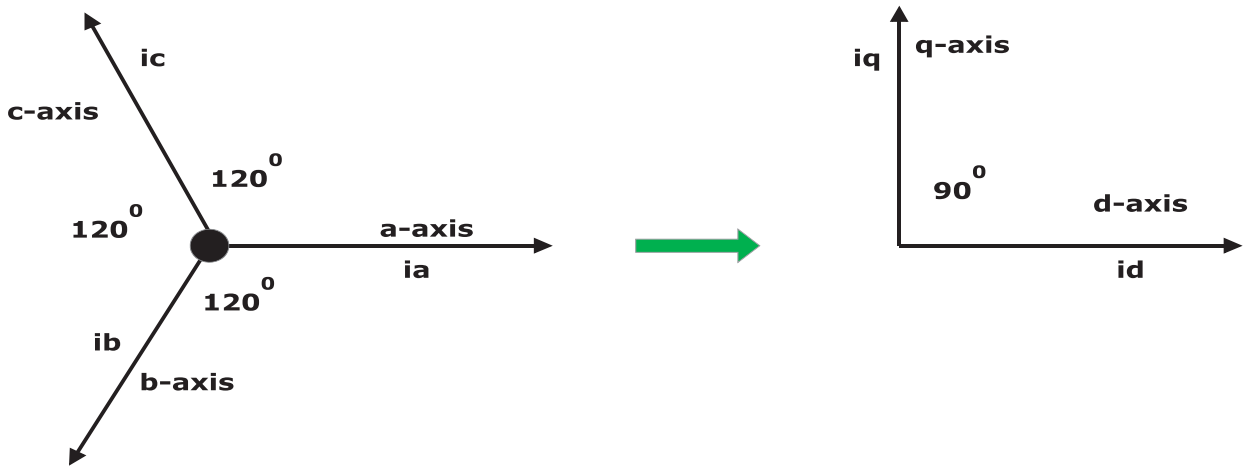

Fig.4.3 a-b-c to d-q-0 transformation

4.4 FUZZY LOGIC CONTROL SCHEME:

Fuzzy sets originated in the year 1965 by Lofti A. Zadeh. Fuzzy logic provides an inference morphology that enables approximate human reasoning capabilities to be applied to knowledge base system. Fuzzy logic controllers are based on the combination of fuzzy set theory and fuzzy logic. Systems are controlled by fuzzy logic controllers based on rules instead of equations. Once all the rules have been defined based on the application, the control process starts with the computation of the rule consequences. Fig. 4.4 shows the active power filter compensation system with fuzzy control scheme. For maintain DC side capacitor value nearly constant, capacitor voltage (V_{dc}) is sensed and then compared with the reference value ($V_{dc,ref}$) [32, 33].

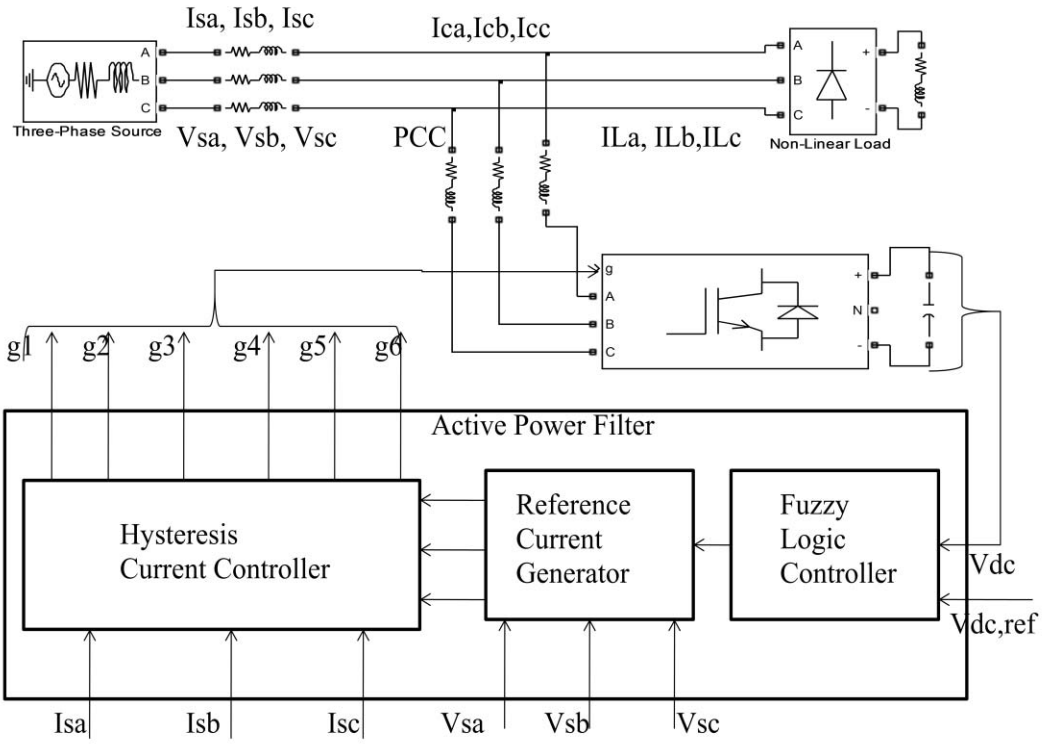

Fig 4.4 Shunt Active power line conditioners using fuzzy logic controller

In case of a fuzzy logic control scheme, the error ($e=V_{dc\_ref}$ - Vdc) and integration of error signal ($\int e$) are used as inputs for fuzzy processing as shown in Fig. 4.5. The fuzzy controller output after the limiting value is considered as peak reference current I_{max} . The switching signals for the PWM converter are obtained by comparing the actual source currents (i_{sa}, i_{sb}, i_{sc}) with the

reference current templates (i_{sa}*, i_{sb}*, i_{sc}*) in the hysteresis current controller. The output pulses are then given to the switching devices of the PWM converter.

4.4.1 Fuzzification:

Just like an algebraic variable takes numbers as a value, a linguistic variable takes words or sentences as values. The set of values that it can take is called its term set. Each value in the term set is a fuzzy variable defined over a base variable. Lofti Zadeh proposed the concept of linguistic or fuzzy variables. In a control system, error between reference and output can be labeled as zero (ZE), positive small (PS), negative small (NS), positive medium (PM), negative medium (NM), positive big (PB), negative big (NB). The process of converting a numerical variable (real number) to a linguistic variable (fuzzy number) is called fuzzification.

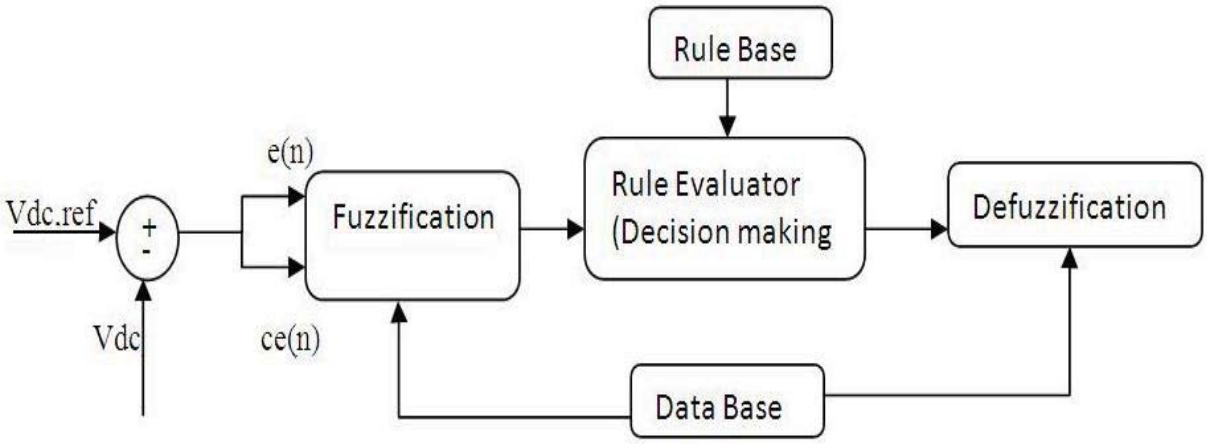

Fig. 4.5 Fuzzy logic controller

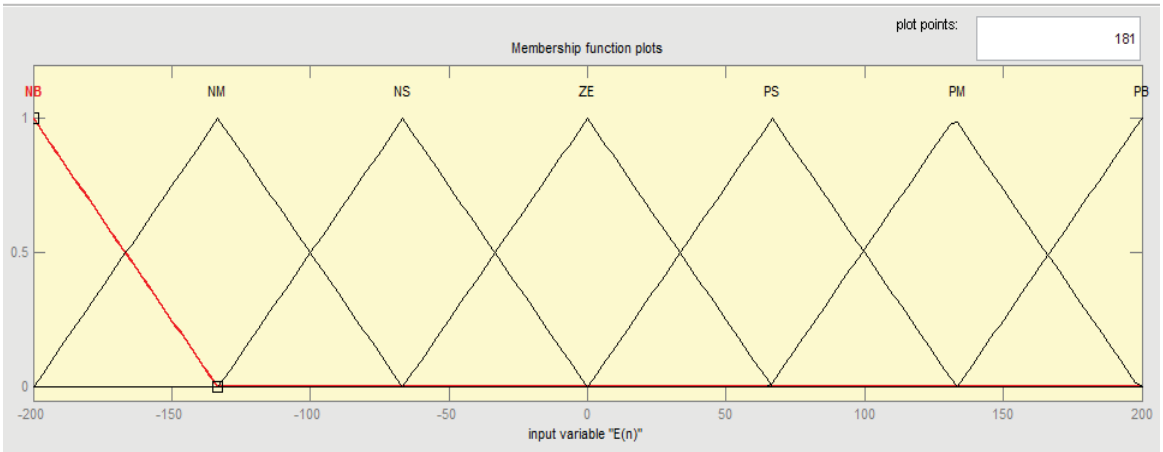

Fig. 4.6 Error input e(n)

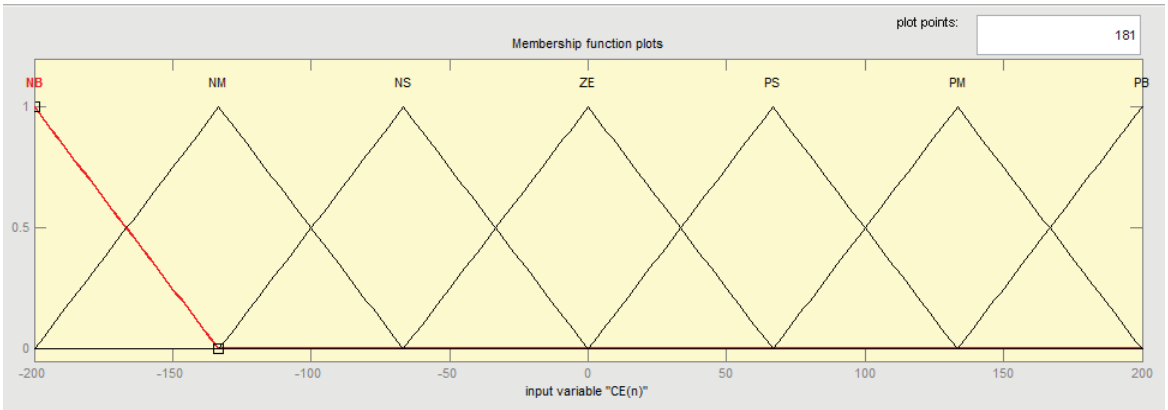

Fig. 4.7 Change in error input ce(n)

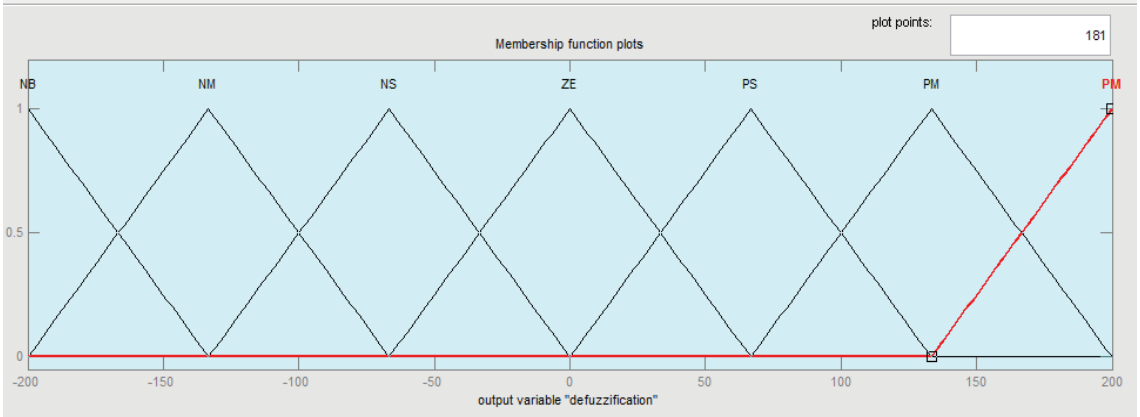

Fig. 4.8 Change of reference output

4.4.2 Rule Base:

In conventional controllers, we have control gains or control laws which are combination of numerical values. In FLC, the equivalent term is rules and they are linguistic in nature. A typical rule can be written as follows;

Rk: If e is A_i and ce is B_i then output is C_i

Where A_i, B_i, C_i are the labels of linguistic variables of error (e), change of error (ce) and output respectively. e, ce and output represents degree of membership.

Let X be a collection of objects denoted by {x}, which could be discrete or continuous, X is called the universe of discourse. If an element in the universe, say x, is a member of fuzzy set 'A' then mapping is given as

$\mu(x) \varepsilon [0, 1]$

$A=[x, \mu(x) | x \varepsilon X]$

The basic fuzzy set operations needed for evaluation of fuzzy rules are AND (∩) OR (U) NOT (-)

AND-Intersection: $\mu A (\cap) B = \min [\mu A(x), \mu B(x)]$

OR-Union: $\mu AUB = \max [\mu A(x), \mu B(x)]$

NOT-Complement: $\mu A = 1- \mu A(x)$

4.4.3 Defuzzification:

The rules of FLC generate required output in a linguistic variable (Fuzzy Number) according to real world requirements. The choices available for defuzzification are numerous. The conversion of a fuzzy set to a single crisp value is called defuzzification. Finally, crisp output is obtained by using

$$\text{Output} = \sum Ai^* xi / \sum Ai$$

4.4.4 Database:

The Database stores the definition of the membership function required by fuzzifier and defuzzifier. Storage format is a compromise between available memory and MIPS of the digital controller chip.

4.4.5 Rule Base:

The Rule base stores the linguistic control rules required by rule evaluator (decision making logic). The rules used in this paper are shown in Table 4.1.

Table 4.1 Rule base table

Ce(n) / e(n)	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	ZE
NM	NB	NB	NB	NM	NS	ZE	PS
NS	NB	NB	MN	NS	ZE	PS	PM
ZE	NB	NM	MS	ZE	PS	PM	PB
PS	NM	MS	ZE	PS	PM	PB	PB
PM	NS	ZE	PS	PM	PB	PB	PB
PB	ZE	PS	PM	PB	PB	PB	PB

4.5 HYSTERESIS CURRENT CONTROLLER:

The hysteresis band current controller for active power filter can be carried out to generate the switching pattern of the inverter. There are various current control methods proposed for such active power filter configurations, but in terms of quick current controllability and easy implementation hysteresis current control method has the highest rate among other current control methods. Hysteresis band current controller has properties like robustness, excellent dynamics and fastest control with minimum hardware. The two-level PWM-voltage source inverter systems of the hysteresis current controller are utilized independently for each phase. Each current controller directly generates the switching signal of the three phases. In the case of positive input current, if the error current e(t) between the desired reference current $i_{ref}(t)$ and the actual source current $i_{actual}(t)$ exceeds the upper hysteresis band limit (+h), the upper switch of the inverter arm is become OFF and the lower switch is become ON as shown in the Fig.4.9 [20].

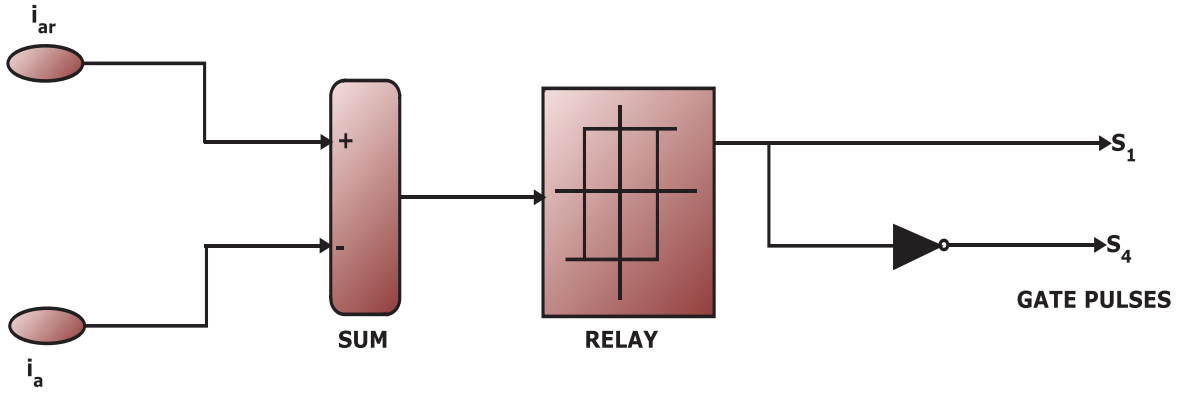

Fig.4.9 Hysteresis band current controllers

4.5.1 Advantages of Hysteresis PWM:

- Excellent dynamic response.
- Low cost and easy implementation.

4.5.2 Disadvantages of Hysteresis PWM:

- Large current ripple in steady-state.
- Variation of switching frequency.
- The modulation process generates sub-harmonic components.

4.6 ADAPTIVE HYSTERESIS CURRENT CONTROLLER:

Inspite of several advantages, the basic hysteresis technique exhibits several undesirable features, such as uneven switching frequency that causes acoustic noise and difficulty in designing input

filters. The hysteresis band current controller is composed of a hysteresis around the reference line current. In equation (4.2), the reference line current of APF is referred to as i_{ref}, and measured line current of the APF is referred to as 'i'. The difference between i and i_{ref} is referred to as δ [21-22].

$$\delta = i - i_{ref} \tag{4.2}$$

The switching logic is formulated as follows:

If δ >HB upper switch is OFF (S1=0) and lower switch is ON (S4=1).

If δ <-HB upper switch is ON (S1=1) and lower switch is OFF (S4=0).

The switching logic for phase b and phase c is similar as phase a, using corresponding reference and measured currents and hysteresis bandwidth (HB).

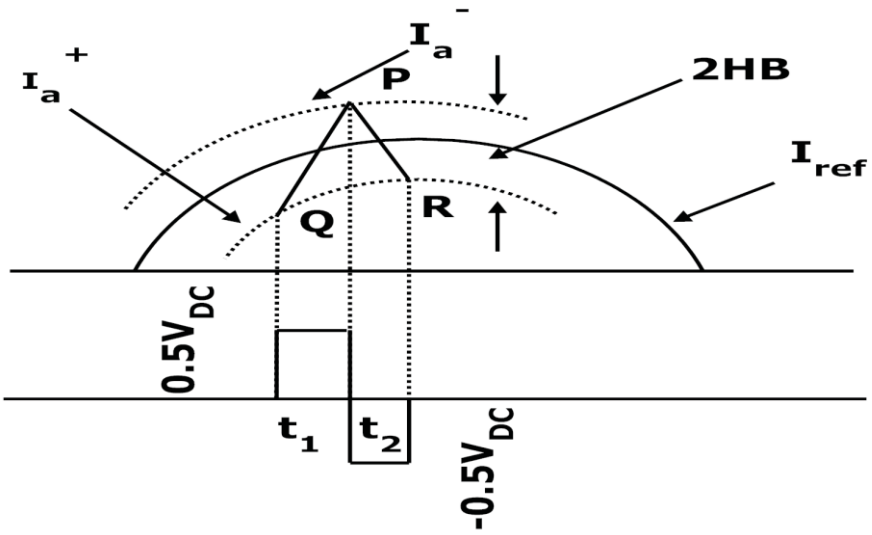

Fig.4.10 Current and voltage waveform with hysteresis band current controller

In case of Adaptive HCC, the rate of change of the line current vary the switching frequency, therefore the switching frequency does not remain constant throughout the switching operation, but varies along with the current waveform. Furthermore, the line inductance (that interfaces inverter and PCC) value of the APF and the capacitor voltage are the main parameters for determining the rate of change of line currents. Fig.4.10 shows the PWM current and voltage waveforms for phase-a. The currents 'i_a' tends to cross the lower hysteresis band at point Q, where S_1 is switched on. The linearly rising current (i_a^+) then touches the upper band at point P, where is S_4 switched on. The following equations can be written in the respective switching intervals t_1 and t_2 from Fig.4.10. The MATLAB/SIMULINK model for adaptive hysteresis band is shown in Fig.4.11.

$$di_a^{+} = \frac{1}{L}\left(0.5V_{DC} - V_a\right) \tag{4.3}$$

$$di_a^{-} = -\frac{1}{L}\left(0.5V_{DC} + V_a\right) \tag{4.4}$$

From Fig.4.10

$$\frac{di_a^{+}}{dt}t_1 - \frac{di_{aref}}{dt}t_1 = 2HB \tag{4.5}$$

$$\frac{di_a^{-}}{dt}t_2 - \frac{di_{aref}}{dt}t_2 = -2HB \tag{4.6}$$

$$t_1 + t_2 = T_c = \frac{1}{f_c} \tag{4.7}$$

where t_1 and t_2 are the respective switching intervals and f_c is the switching frequency. Adding equation (4.5) and (4.6) and substituting in equation (4.7), it can be written as

$$\frac{di_a^{+}}{dt}t_1 + \frac{di_a^{-}}{dt}t_2 - \frac{1}{f_c}\frac{di_{aref}}{dt} = 0 \tag{4.8}$$

Subtracting equation (4.6) from (4.5)

$$\frac{di_a^{+}}{dt}t_1 - \frac{di_a^{-}}{dt}t_2 - \left(t_1 - t_2\right)\frac{di_{aref}}{dt} = 4HB \tag{4.9}$$

Substituting equation (4.4) in (4.9)

$$\left(t_1 + t_2\right)\frac{di_a^{+}}{dt} - \left(t_1 - t_2\right)\frac{di_{aref}}{dt} = 4HB \tag{4.10}$$

Substituting equation (4.4) in equation (4.8) and solving

$$\left(t_1 - t_2\right) = \frac{di_{aref}/dt}{f_c\left(di_a^{+}/dt\right)} \tag{4.11}$$

Substituting equation (4.11) in (4.10)

$$HB = \frac{0.125V_{DC}}{f_c L}\left[1 - \frac{4L^2}{{V_{DC}}^2}\left(\frac{V_a}{L} + m\right)^2\right] \tag{4.12}$$

where f_c is modulation frequency, $m = di_{aref}/dt$ is the slope of command current waveform.

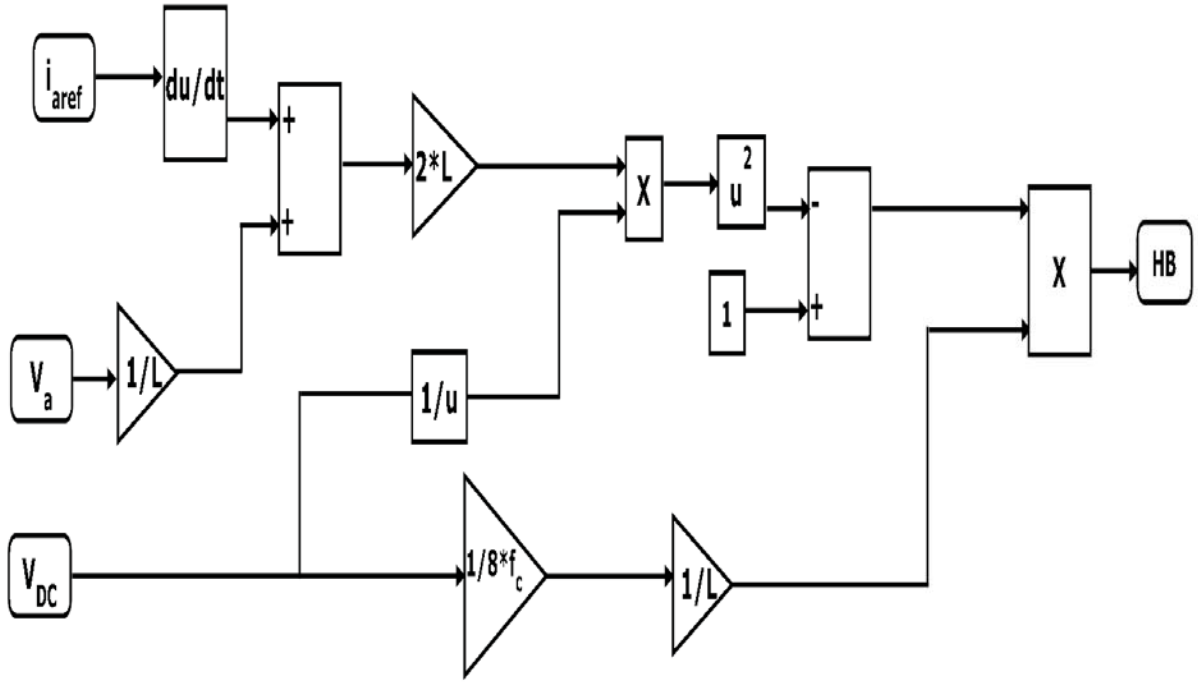

Fig. 4.11 Adaptive hysteresis bandwidth calculation block diagram

4.7 DIGITAL CONTROLLER:

In this project work digital PI hysteresis current controller is developed. It consists of one regulatory block which uses PI controller algorithm, FSMD (finite state machine +data path) architecture, hysteresis block. For implementation of digital, individual VHDL code is written and assembled together [17].

4.7.1 Regulator Description:

The regulator block is implemented using a PI-controller that is based on a recurrent equation (4.13) and shown in Fig.4.7, Here 16-bit signed bits integer coding is used with thousand order precision [17]. The output of the PI control is given by.

$$u(t) = K\left[e(t) + \frac{1}{T_i}\int_0^t e(t)] \right] \tag{4.13}$$

By discrete equation (4.13)

$$u(t) = K\left[e(t) + \frac{1}{T_i} s(n) \right] \tag{4.14}$$

$$s(n) = \int_{n-1}^{n} e(t)dt \tag{4.15}$$

By using forward rectangular rule of integration

$$s(n) = s(n-1) + he(n-1) \tag{4.16}$$

By putting equation (4.16) in equation (4.14)

$$u(n) = K\left[e(n) + \frac{1}{T_i}\left(s(n-1) + he(n-1)\right)\right] \tag{4.17}$$

Similarly

$$u(n-1) = K\left[e(n-1) + \frac{1}{T_i}s(n-1)\right] \tag{4.18}$$

Substituting (4.18) from (4.17)

$$u(n) - u(n-1) = Ke(n) + \frac{K}{T_i}s(n-1) + \frac{Kh}{T_i}e(n-1) - Ke(n-1) - \frac{K}{T_i}s(n-1) \tag{4.19}$$

$$u(n) = u(n-1) + Ke(n) + K\left(\frac{h}{T_i} - 1\right)e(n-1) \tag{4.20}$$

where h= sampling period of the controller

K= proportional gain

T_i= Integral gain

e(n)= Error

n= Number of iteration

4.7.2 Behavioral Description:

The behavioral description of the PI-controller is implemented by using control device algorithm. It is implemented by a data flow graph (DFG).The DFG is implemented with the help of FSMD architecture for FPGA implementation. The mathematical calculation of the data flow graph is as fallows.

$e(n)=(I_{ref} - I_{source})$ (4.21)

$I_{source}=\{(I_{mag}*I_{source\_num})/2^{15}\}$ (4.22)

$I_{ref}=\{(I_{mag}*I_{ref\_num})/2^{15}\}$ (4.23)

$e(n)\_num = 1024*error$ (4.24)

$= 1024*(I_{ref} - I_{source})$ (4.25)

$$= 1024*[\{(I_{mag}*I_{ref\_num})/2^{15}\}-\{(I_{mag}*I_{source\_num})/2^{15}\} \quad (4.26)$$

$$= 2^{-5}*I_{mag}*(I_{ref\_num}- I_{source\_num}\,)$$

$$= [I_{max}*I_{ref\_num}(>>5)]+[- I_{mag}*I_{source\_num}(>>5)] \quad (4.27)$$

where e(n)= Error signal

e(n)_num= Numeric value of the error signal

I_{ref} =Reference current

I_{ref_num}= Numeric value of reference current

I_{source} = source current

I_{source_num}= Numeric value of source current

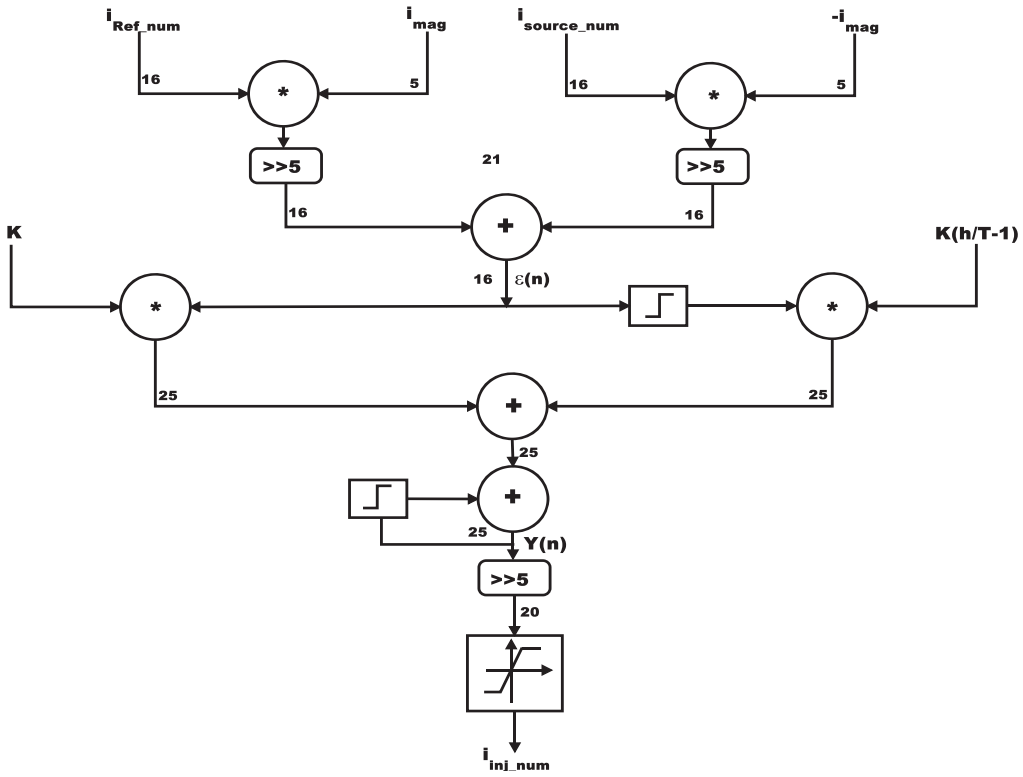

Fig.4.12 Data flow graph of PI regulator

4.7.3 FSMD Architecture:

The FSMD includes finite state machine (FSM) along with data path to implement a controller. Here space optimized FSMD architecture is used. The FSMD consist of a control unit and a data path, where the data path operates under the control of control unit (FSM). The FSM provides

control signals to the data path and data path provides status signals to the FSM. Input data are given to the data path. The data path consists of RAM, ALU, MUX and REGISTER. The control unit consists of finite state machine that includes 29 states for calculating the error signal. The mathematical calculation using the data path is achieved using the following stages.

Stage-1.Acquisition:

The I_{ref_num} and I_{source_num} are loaded to the memory from input via MUX by choosing appropriate select line of MUX.

Stage-2 Calculation:

For the arithmetic operations, we used one state to read operands and select operators for ALU operation and next state is used to save the computed result in memory location (RAM). At the end of S28 the command value is loaded to register by making i_{inj_en} to become high and i_{inj_num} is available. This is the steady state error updated by PI-controller at the end of S28 as shown in Fig.4.13.

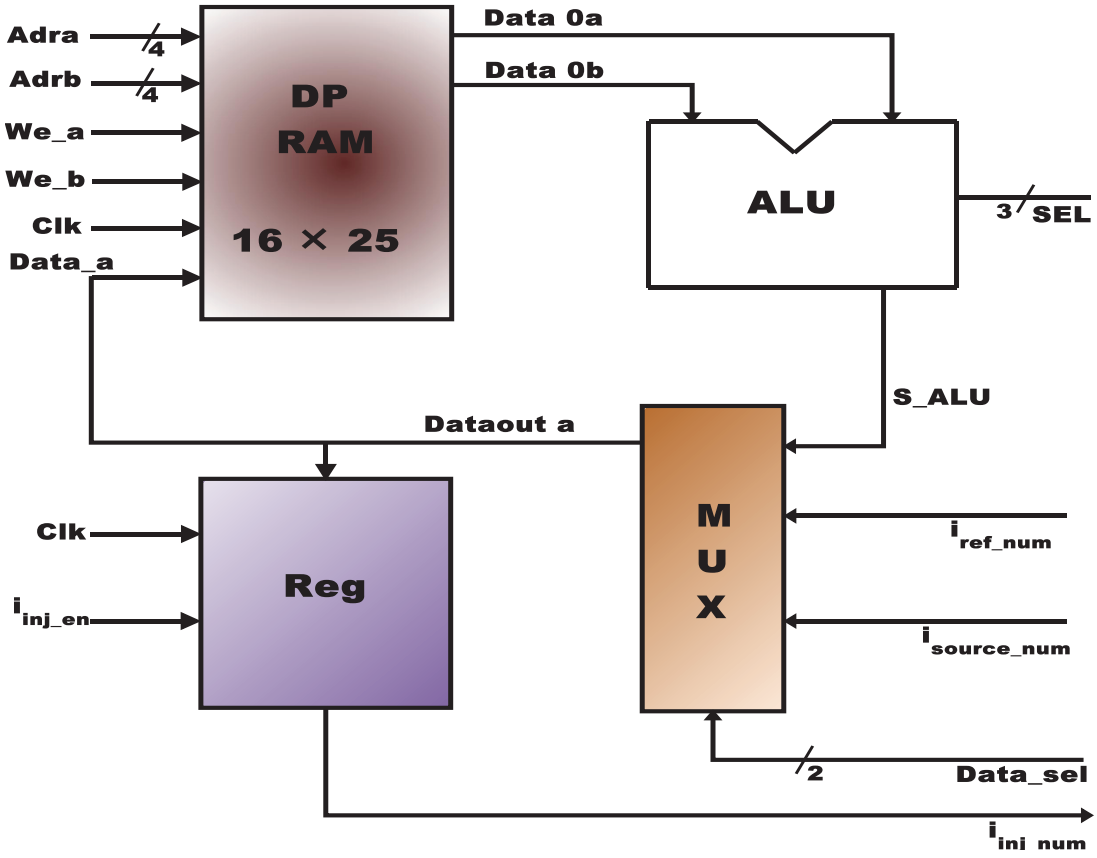

Fig. 4.13 Data path Structure

TABLE4.2 State Table

STATE	Adra	Adrb	We_a	We_b	Data_sel MUX	Sel (ALU)	I_{inj_en}	COMMENTS
S0	0	0	1	0	01	-	0	Adra(0) ← I_{ref_num}
S1	1	-	1	0	10	-	0	Adra(1) ← I_{source_num}
S2	0	2	0	0	00	001	0	D0a← I_{ref_num}, D0b← I_{mag}
S3	8	-	1	-	-	-	0	Adra(8) ← I_{ref_num} * I_{mag}
S4	1	3	0	0	00	001	0	Da← I_{source_num},Db← I_{mag}
S5	9	-	1	-	-	-	0	Adra(9)← I_{source_num} * -I_{mag}
S6	8	-	0	-	00	011	0	D 0a← Adra(8 bit * I_{mag})
S7	10	-	1	-	-	-	0	>>5
S8	9	-	0	-	00	011	0	Data 0a← I_{source}*(- I_{mag})
S9	-	8	-	1	-	-	0	>>5
S10	10	8	0	0	00	000	0	Da← Adr_10, Db← Adr_8
S11	11	-	1	-	-	-	0	ξ(n)
S12	11	5	0	0	00	010	0	Da← ξ(n), Db←K(h/T)
S13	12	-	1	-	-	-	0	ξ(n)*K(h/T) ← Adra12
S14	11	-	0	-	00	100	0	Data 0a ← ξ(n)
S15	4	-	1	-	-	-	0	(4) ξ(n-1) ← ξ(n)
S16	4	6	0	0	00	010	0	Da← ξ(n-1) Db ← -K(h/T)
S17	-	9	-	1	-	-	0	9 ← ξ(n-1)* -I_{max}
S18	12	9	0	0	00	000	0	Da ← 12Adra,Db← Adrb 9
S19	13	-	1	-	-	-		ξ(n)* K(h/T) + ξ(n-1)*K(h/T)→ 13
S20	13	-	0	-	00	100	0	Da ← y(n)
S21	-	10	-	1	-	-	0	Y(n-1)← y(n)
S22	13	10	0	0	00	000	0	Da← y(n),Db← y(n-1)
S23	14	-	1	-	-	-	0	y(n)+y(n+1)← y(n)
S24	14	-	0	-	00	011	0	Y(n)→a
S25	15	-	1	-	-	-	0	Y(n)>>5
S26	15	-	0	-	00	101	1	I_{inj_num}←S_ALU
S27	-	-	0	0	-	-	0	REG←Result
S28	-	-	-	-	-	-	1	I_{inj_num}←REG

Stage-3 (update):

The transition from one state to another state in FSM is occurred on positive edge of the clock input. There are 29 states used and initial state is TOP, When START = '0' or RESET= '1' then state is TOP else under normal case RESET='0' and START='1' the control unit undergoes through S0 to S28 for calculating the error as shown in the Fig.4.8. The function of all the states is described at the table 4.2.

At state 'S0', address write enable (we_a) and data selection line of MUX status is high as a result the digital value of the reference current 'I_{ref_num}' is loaded at the address location 'Adra(0)'. The digital value of the source current 'I_{source_num}' is loaded at the address location 'Adra(1)' at 'S1'. At 'S2' I_{ref_num} and maximum value of reference current 'I_{mag}' are loaded at data line D0a and D0b respectively. Then at the next state 'S3' both I_{ref_num} and I_{mag} are multiplied at ALU and stored at address 'Adra(8)'. At state 'S4' source current 'I_{source_num}' and 'I_{mag}' are loaded at data line D01and D02 respectively. At state S5, I_{source_num} and $-I_{mag}$ are multiplied at ALU and stored at address 'Adra(9)'. All the states are described at Table 4.1 and finally at state S28 PI controller output i.e I_{inj_num} is get at the output of register.

Fig.4.14 shows the controller unit diagram, here the controller inputs are CLKF, RESET, and Start. Address (a & b), data selection line and enables lines are the output as shown in the figure. All the states (s0 to s28) will control by FSM controller.

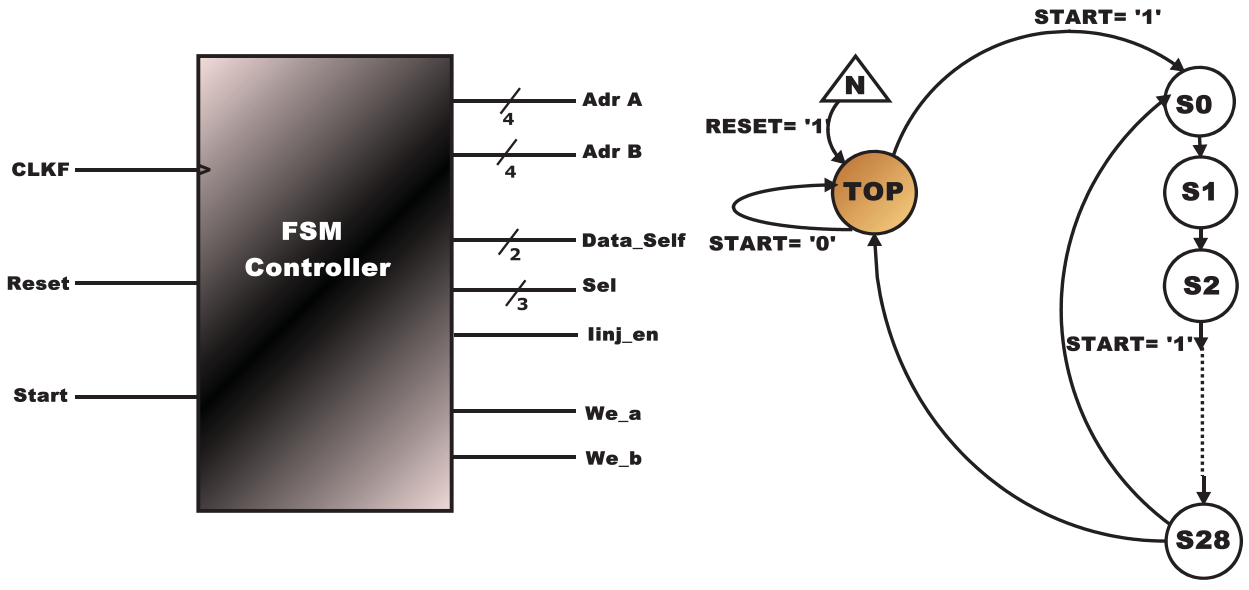

Fig.4.14 Controller unit diagram

4.7.4 HCC Blocks Description:

The HCC block consists of three identical HCC block. Each one is developed in RTL level VHDL code. This module consists of the following signals.

- CLK : Basic clock signal.
- RESET: Asynchronous reset activates at high state.
- LOAD: Lode the counter.
- DOWN: Enable for up/down counter.
- ena : Enable for the comparator.
- C, C' : Complementary control signal.

The HCC block consists of an up/down counter and a comparator along with a clock divider to control the frequency of switching pulses. The output of the PI-controller blocks i.e. FSMD output I_{inj_num} is compared with the band created by up/down counter. When the error exceeds the lower limit switch is ON and when it exceeds the upper limit switch is OFF. The C' is complementary of C pulse and delayed to take account of switching time 'S' in the power converters with the help of a dead band. Hysteresis current controller is shown in fig.4.15.

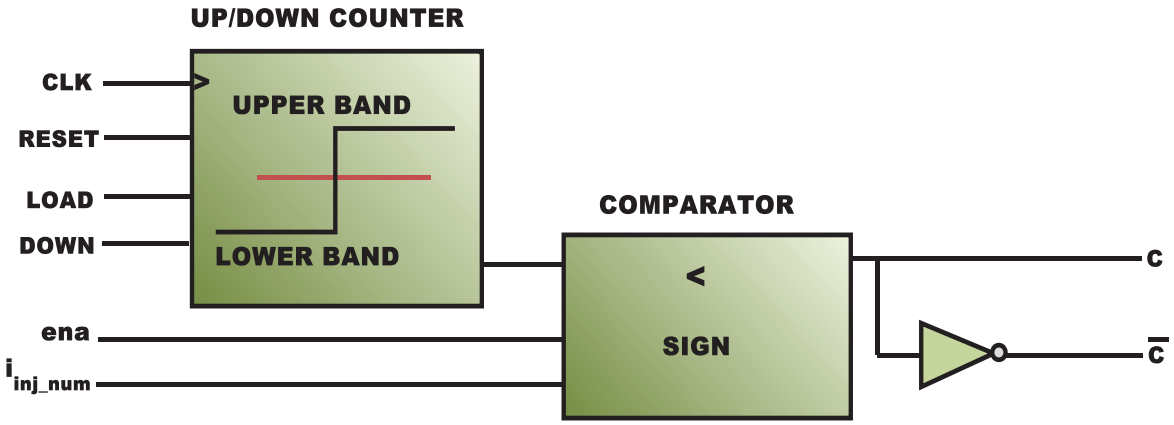

Fig.4.15 Hysteresis current controller

Fig.4.16 shows the internal modules of the digital controller. It represents connection between different components. It consists of finite state machine (FSM), dual port RAM, register, MUX, ALU, clock divider, up/down counter and comparator. The FSM will decide the different operation as described in Table 4.2. RAM, ALU, MUX and register together form FSMD architecture as discussed before. Here the work of the FSMD part is to generate error signal by taking the two digital input namely digital value of reference current (i_{ref_num}) and digital value of

source current (i_{source_num}). These two digital inputs are given to the MUX and depending up on the selection input MUX will allows the data to RAM.RAM will provide the digital data to ALU and depending up on the selection it will do the arithmetic and logic operation. The output of the RAM is S_ALU2, which is given to the MUX and depending up on the selection line the MUX allows this to RAM or register. Finally the resister will give the digital value of the reference current i_{inj_num}. The i_{inj_num} and output of up/down counter is given to the comparator i.e. the i_{inj_num} value is compare with a fixed band created by the up/down counter. The output of the comparator gives gating pulse. The frequency of the pulse also control by the clock divider. Fig.4.17 shows the hardware implementation of digital controller through the FPGA board. The VHDL code for digital controller is dump in to the FPGA and the output pulses are observed at CRO.

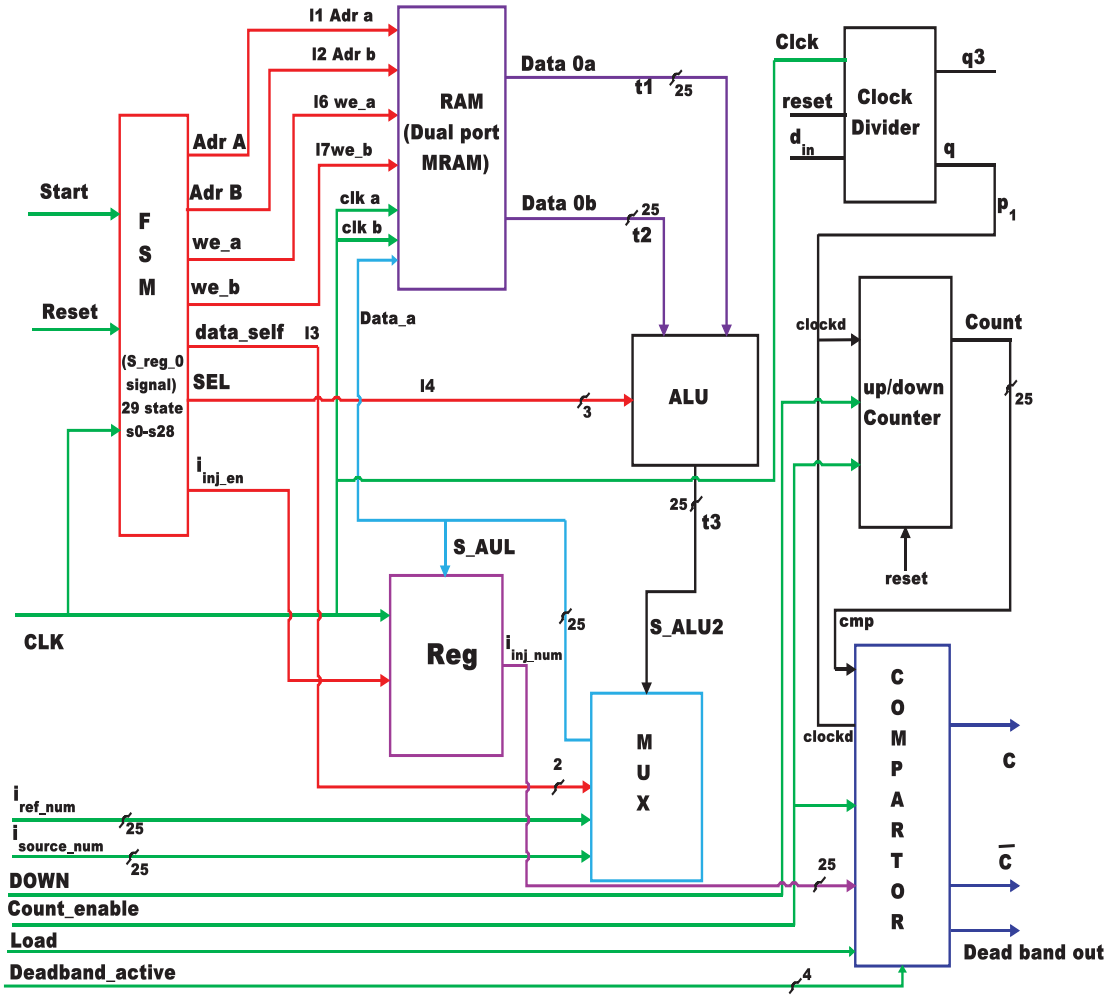

Fig.4.16 Internal modules of digital controller

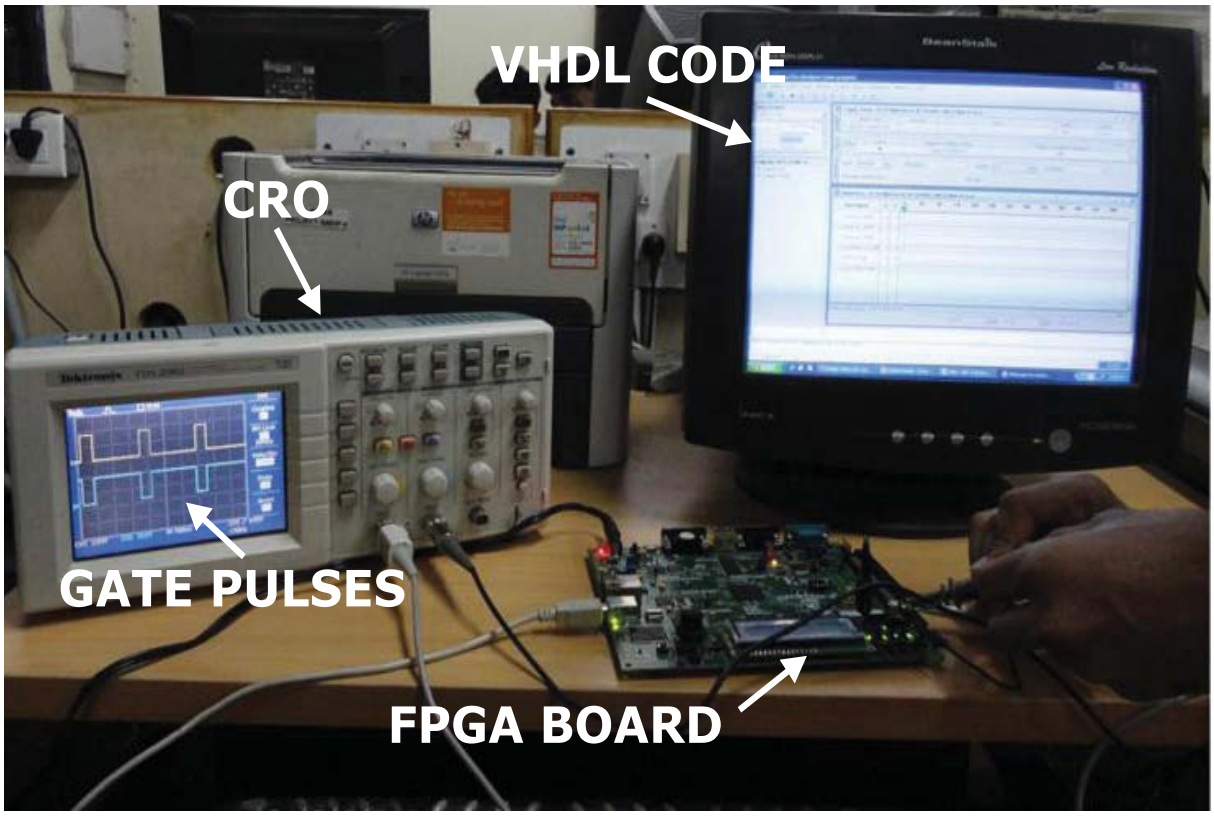

Fig.4.17 Observation of desired gate pulses by using digital controller

4.8 CHAPTER SUMMARY:

In this chapter the basic compensation principle is described. That purely deepens up on the control algorithms. For extraction of reference current the superior features of SRF controller are described. The Hysteresis and adaptive hysteresis current controller algorithm are explained. The digital hysteresis current controller algorithm is also described.

CHAPTER 5

RESULTS AND DISCUSSIONS

(Comparison of Performances of Controllers and Gating pulses from Digital controllers

5.1 SIMULATION RESULTS:

5.1.1 System Parameters:

The system parameters considered for the study of APF for both SRF controller with hysteresis current controller and adaptive hysteresis current controller are given in Table 5.1. The PI controller used inside the SRF controller for maintaining the capacitor voltage constant having proportional gain (K_P) and integral gain (K_I) are 0.1 and 1 respectively. The gain of the PI control is chosen by iterative manner until good performance is achieved. The system parameters for the fuzzy controller applied to the APF is given in the table 5.2.

TABLE 5.1 APF System Parameters using SRF theory

SYSTEM PARAMETERS	VALUE
Line Voltage	440 V
Supply Frequency	50 Hz
Source Impedance:(Resistance Rs, Inductance Ls)	1 Ω, 0.1 mH
Non-Linear load under steady state:(Resistance Rs, inductance Ls)	10 Ω, 100 mH
Filter Impedance:(Resistance Rs, inductance Ls)	1 Ω, 2.5 mH
Dc side capacitance	1400 μF
Reference Dc Voltage	800 V
Power converter	6 MOSFET/DIODE

Table 5.2 steady state system parameters using fuzzy logic controller

System Parameters	Values
Source voltage	120 (peak)
Supply Frequency	50 Hz
Source Impedance:(Resistance Rs, Inductance Ls)	0.1 Ω, 0.5 mH
Non-Linear load under steady state:(Resistance Rs, inductance Ls)	7 Ω, 200 mH
Filter Impedance:(Resistance Rs, inductance Ls)	1 Ω, 1.66 mH
Dc side capacitance	2100 V
Reference Dc Voltage	220 V

5.2 SIMULATION RESULTS USING HCC AND AHCC:

5.2.1 Steady State Performance of APF with SRF and Hysteresis Current Controllers:

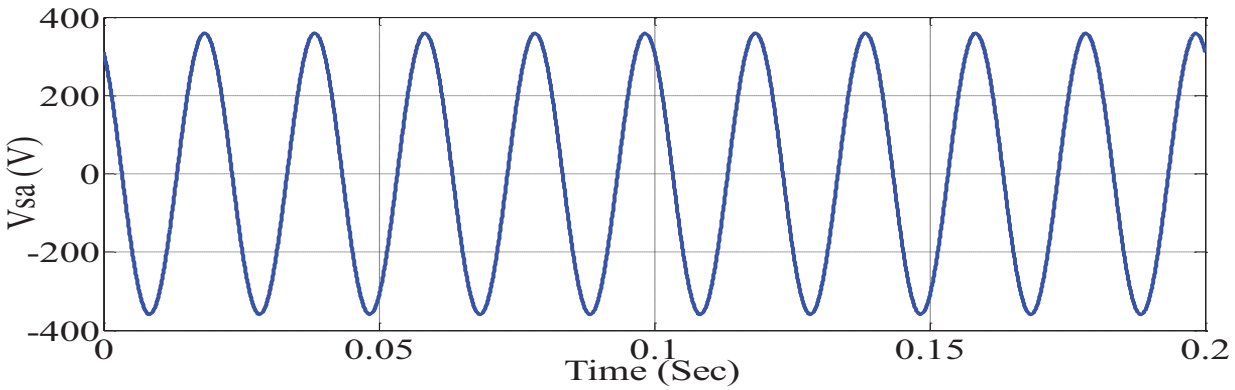

Fig. 5.1 (a) Source Voltage

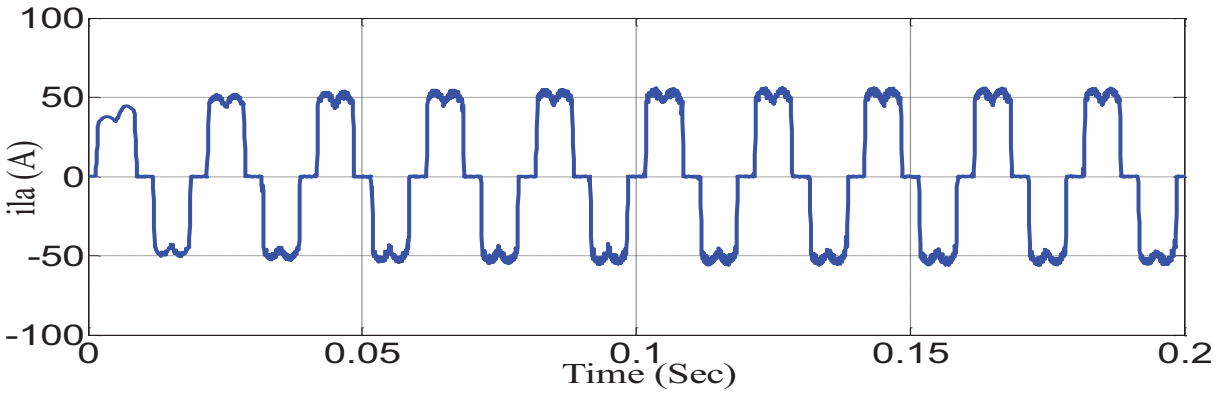

Fig. 5.1 (b) Load Current

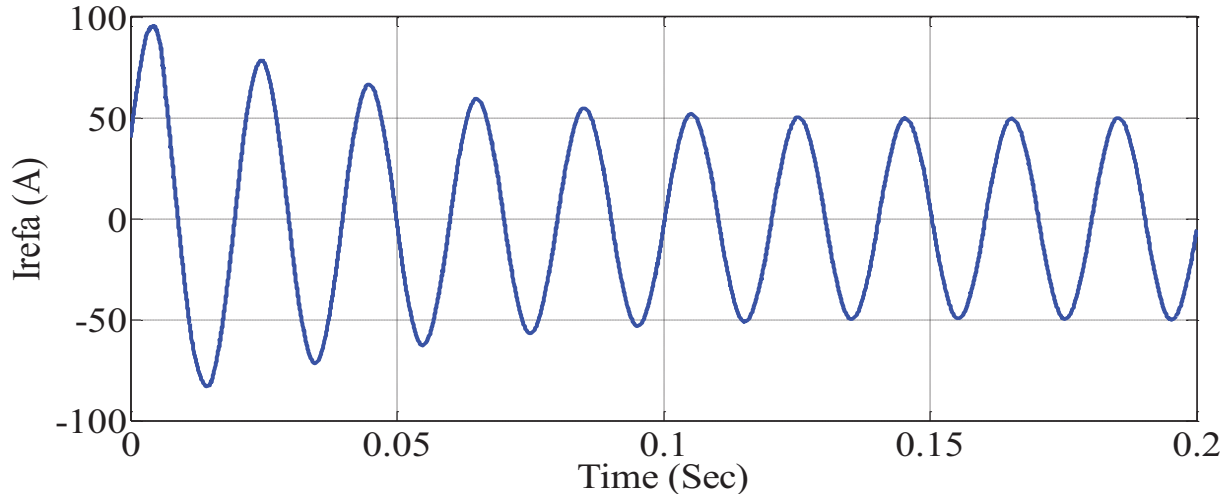

Fig. 5.1 (c) Reference current

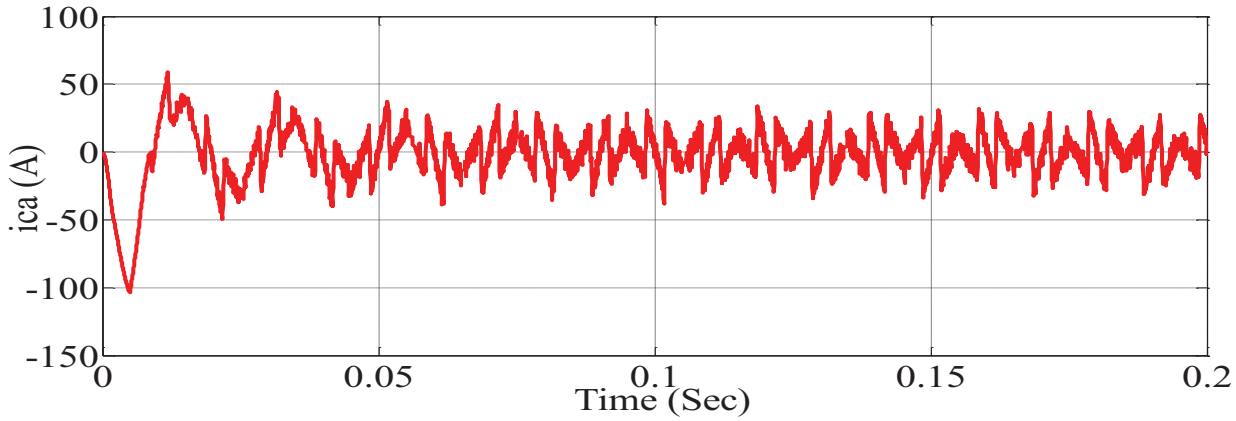

Fig. 5.1 (d) Compensating Current

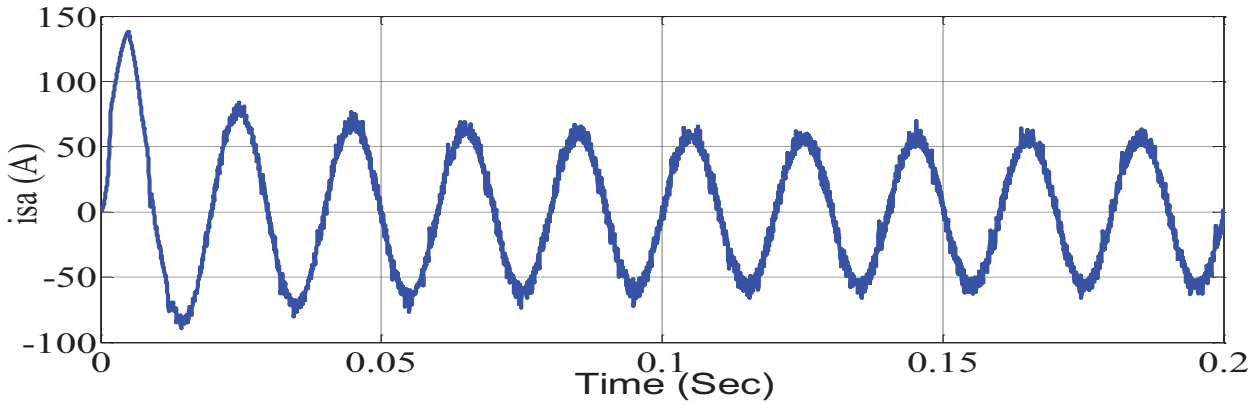

Fig. 5.1 (e) Source Current after Compensation

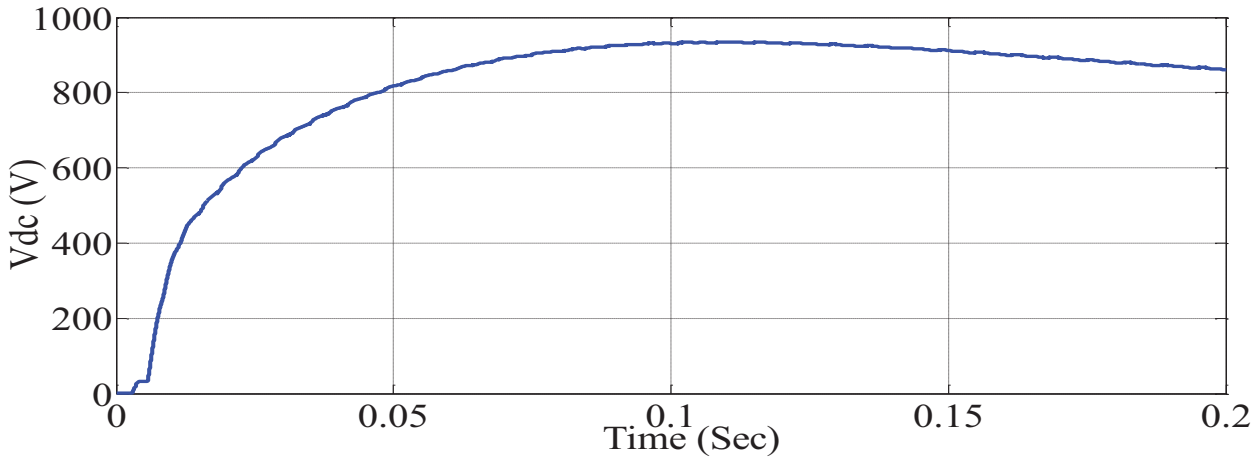

Fig. 5.1 (f) Voltage across Capacitor

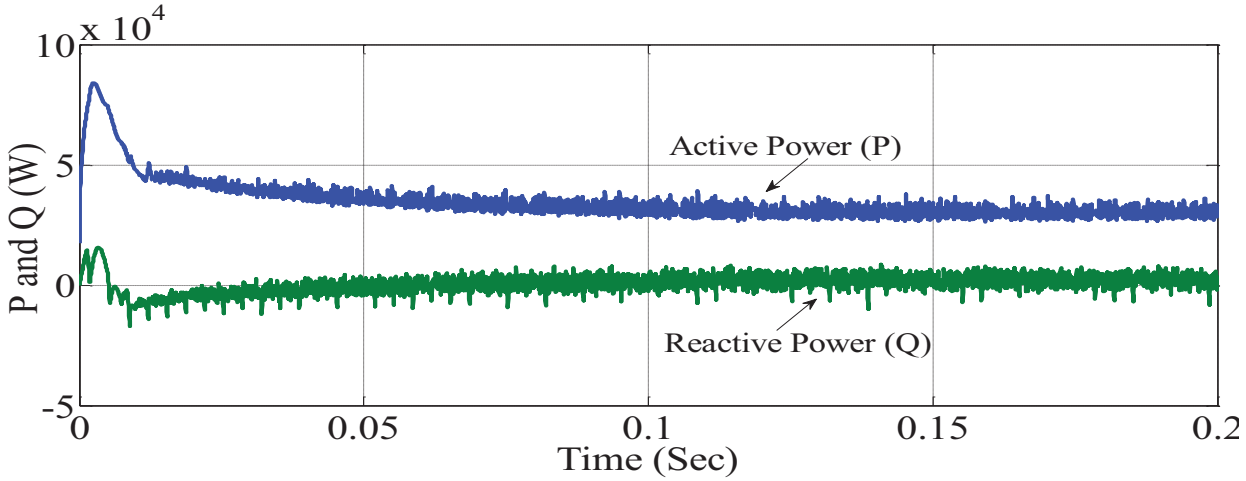

Fig. 5.1 (g) Active and Reactive Power

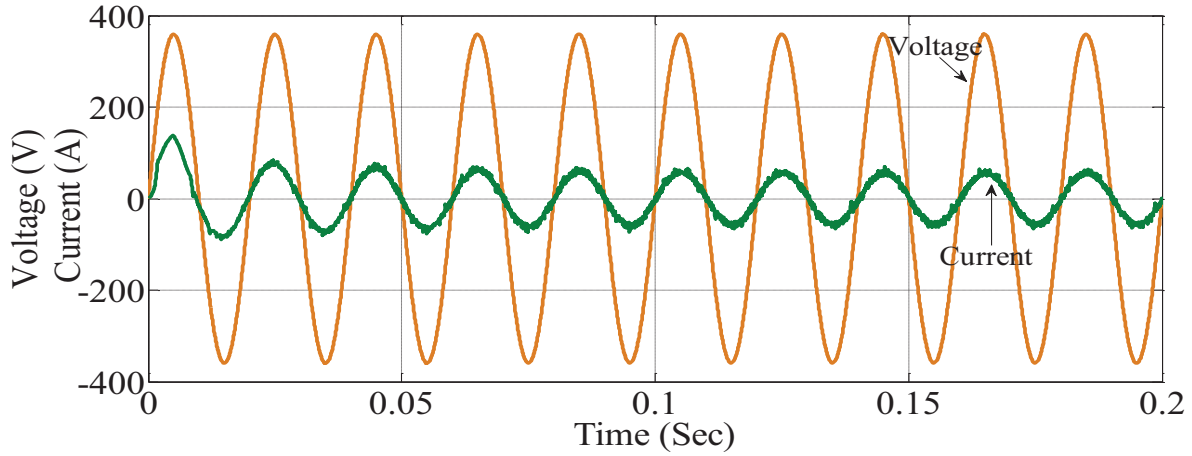

Fig. 5.1 (h) Source Voltage and Current,

Fig. 5.1 Steady state response of APF with SRF and HCC

In steady state condition the simulation time is taken as t=0 to t=0.2 sec with constant load. The source voltage is shown in Fig. 5.1 (a).The load current is shown in Fig. 5.1 (b), which is highly non-linear in nature. The actual reference current for phase-a is shown in Fig. 5.1(c). This waveform is obtained from SRF controller. The APF inject the compensating current to PCC, which is shown in Fig. 5.1 (d). The compensating current containing only the harmonic current, which is introduced to the power system due to non-linear load but in opposite phase. The current after compensation is as shown in 5.1(e). It is clear from the Fig. that, the waveform is sinusoidal with some high frequency ripples. The time domain response of the SRF controller is shown in 5.1 (f) which clearly indicates that, the controller output settles after a few cycles. The magnitude of the active and reactive power is shown in Fig. 5.1 (g) and the source current and voltage, from which we will get the knowledge of unity power factor, is shown in Fig. 5.1 (h).

5.2.2 Transient State Performance Of APF with SRF and Hysteresis Current Controller:

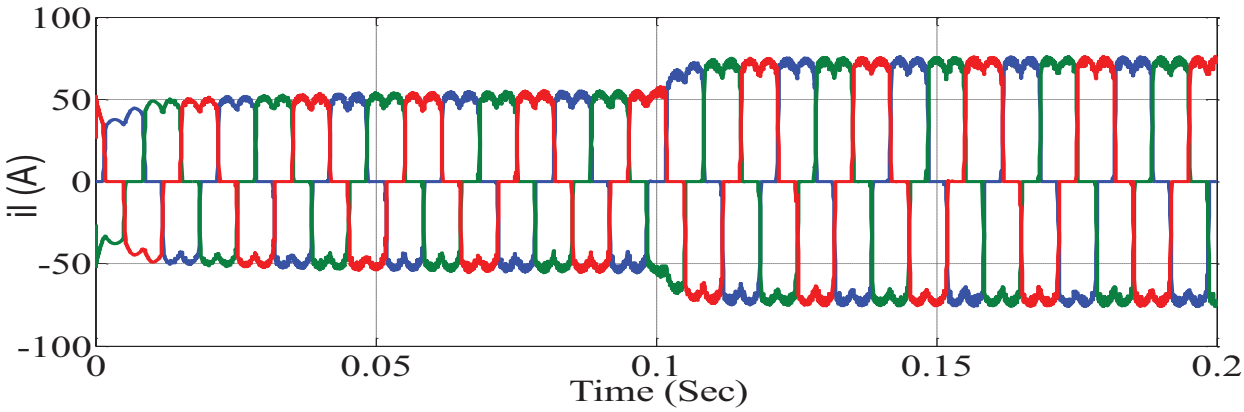

Fig. 5.2 (a) Load Current

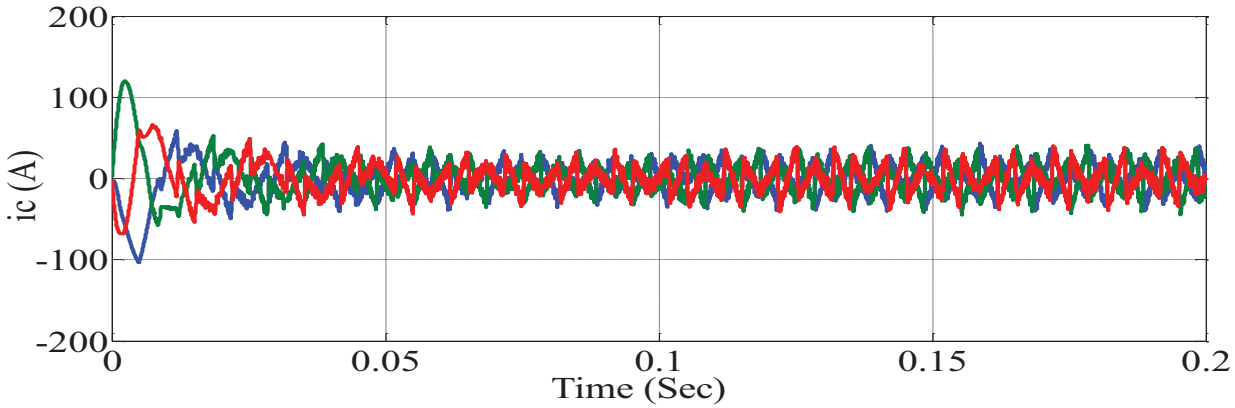

Fig. 5.2 (b) Compensating Current

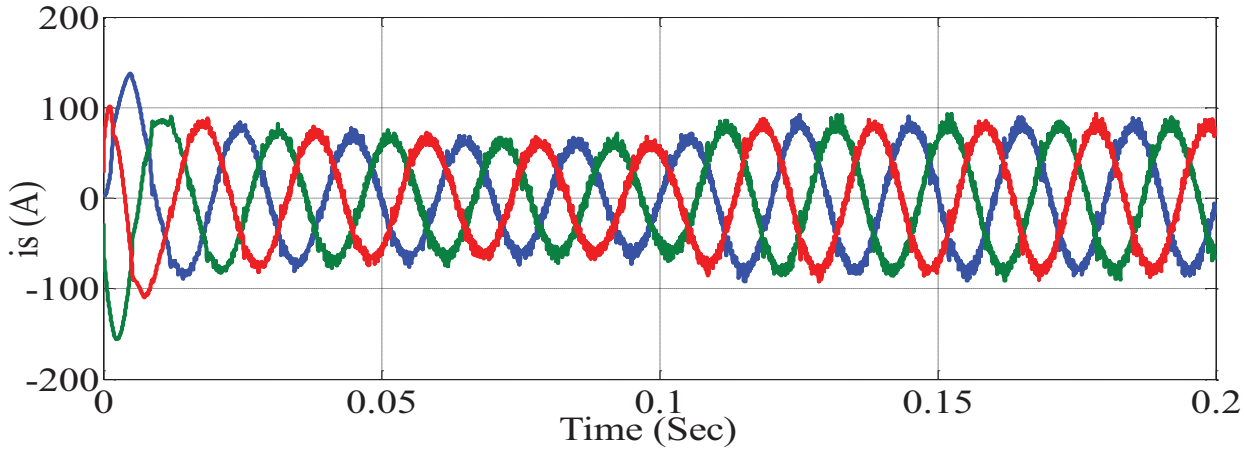

Fig. 5.2 (c) Source Current after compensation

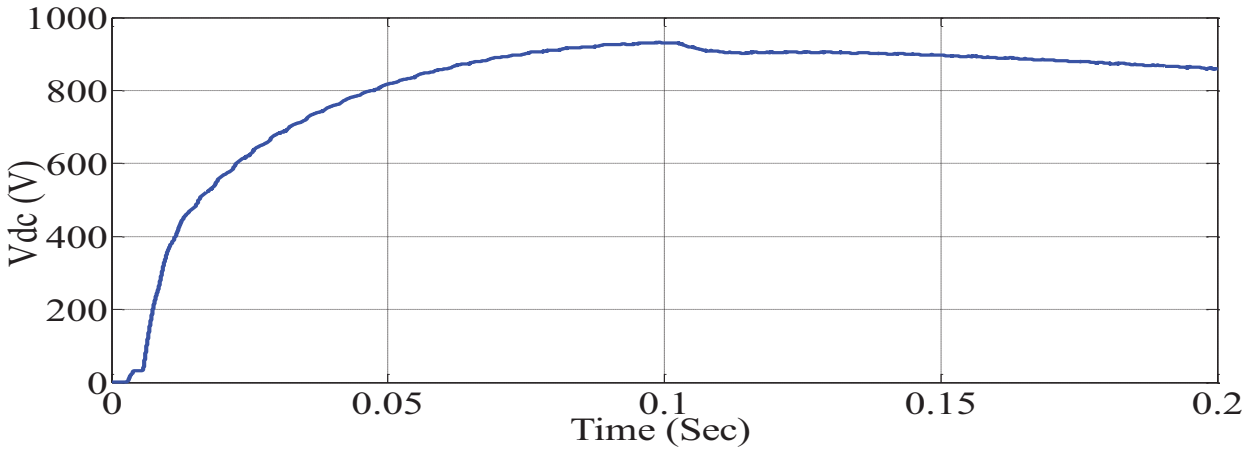

Fig. 5.2 (d) Capacitor Voltage

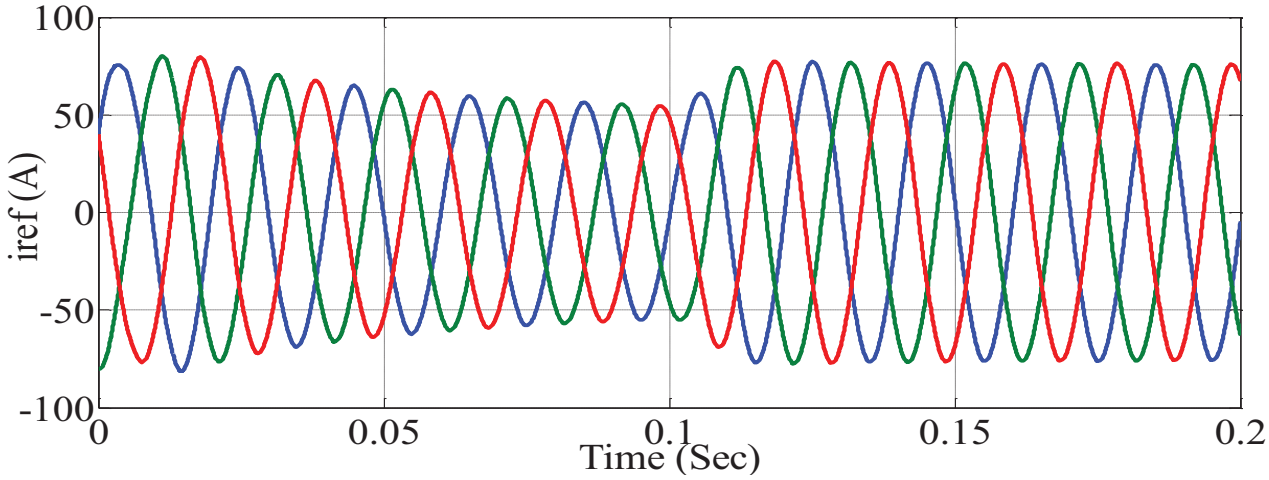

Fig. 5.2 (e) Reference Current

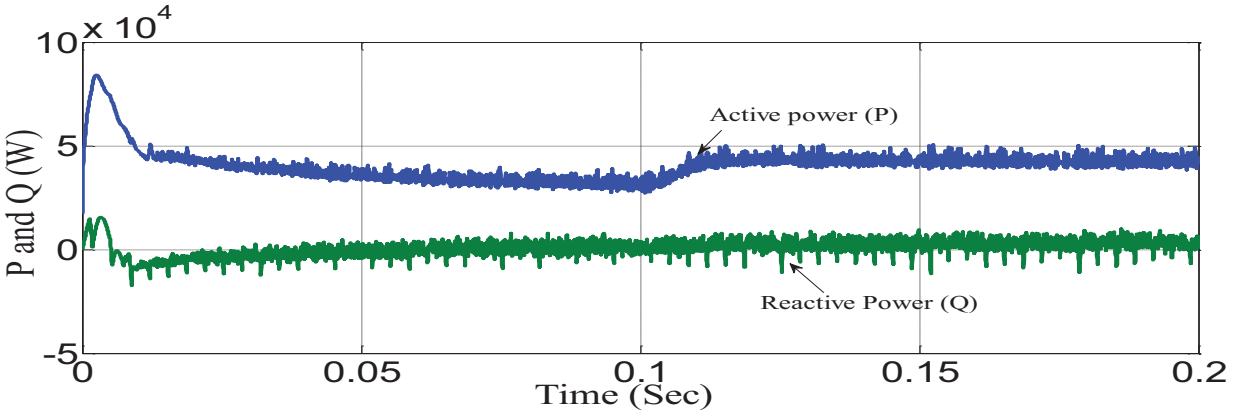

Fig. 5.2 (f) Active and Reactive Power

Fig.5.2 Transient state response of APF with SRF and HCC

During the period t=0 to t=0.1 sec R, L parameters of the nonlinear load are set as 20 Ω and 200 mH respectively. From t=0.1 to 0.2 sec the load parameters are changed to 10 Ω and 100 mH respectively. The corresponding waveforms obtained are shown in the Fig. 5.2. The load current waveform is shown in Fig. 5.2 (a). And Fig. 5.2 (a) indicates that after 0.1 sec the load current magnitude is changing as the load is changing and settling very quickly. The APF supplies the compensating current that is shown in Fig. 5.2 (b). The source current after compensation is presented in Fig. 5.2 (c) that indicates the current becomes sinusoidal. The capacitor voltage during transient period is nearly same as the steady period is shown in Fig. 5.2 (d). The reference current and active and reactive power is shown as Fig. 5.2 (e), 5.2 (f) respectively.

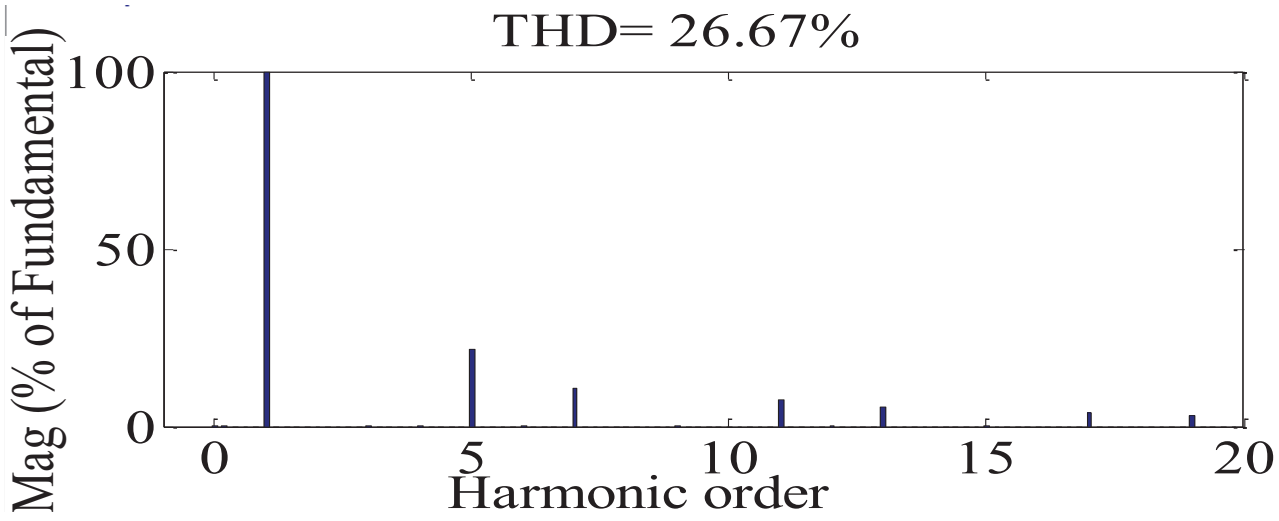

Fig. 5.3 (a) THD without HCC

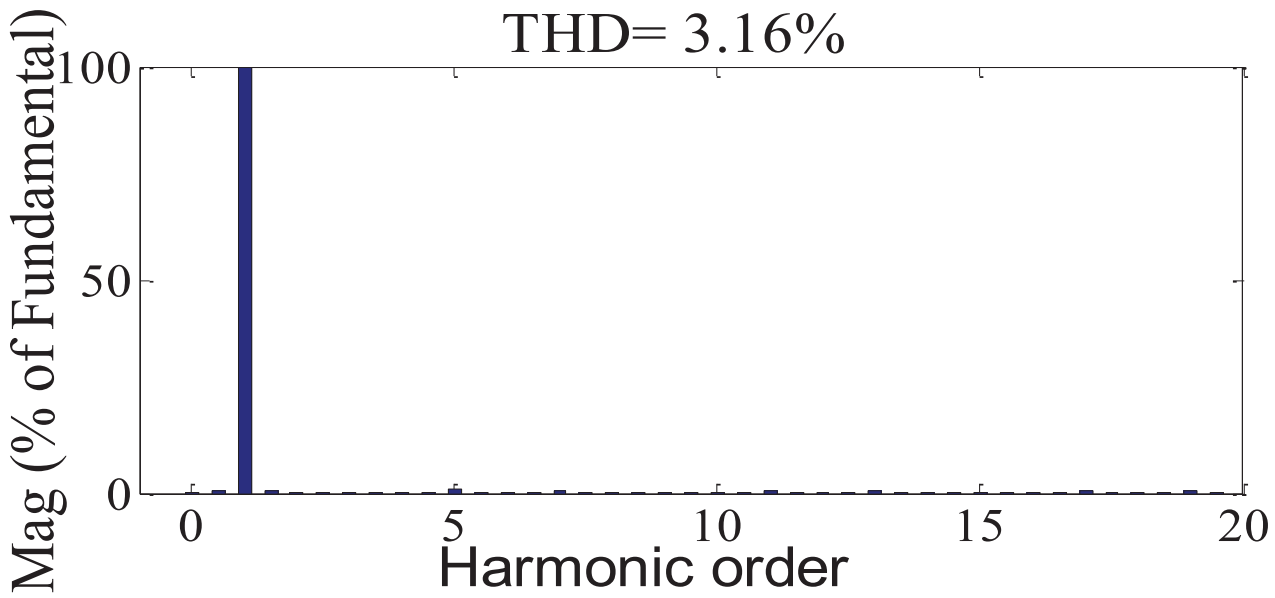

Fig. 5.3 (b) THD with HCC

Fig. 5.3 THD without and with HCC

Fig. 5.3 (a) and 5.3(b) are source current THD, without APF and with APF under HCC. The results presented both in the steady state and transient state conditions.

5.2.3 Steady State Performance of APF with SRF and Adaptive Hysteresis Current Controllers:

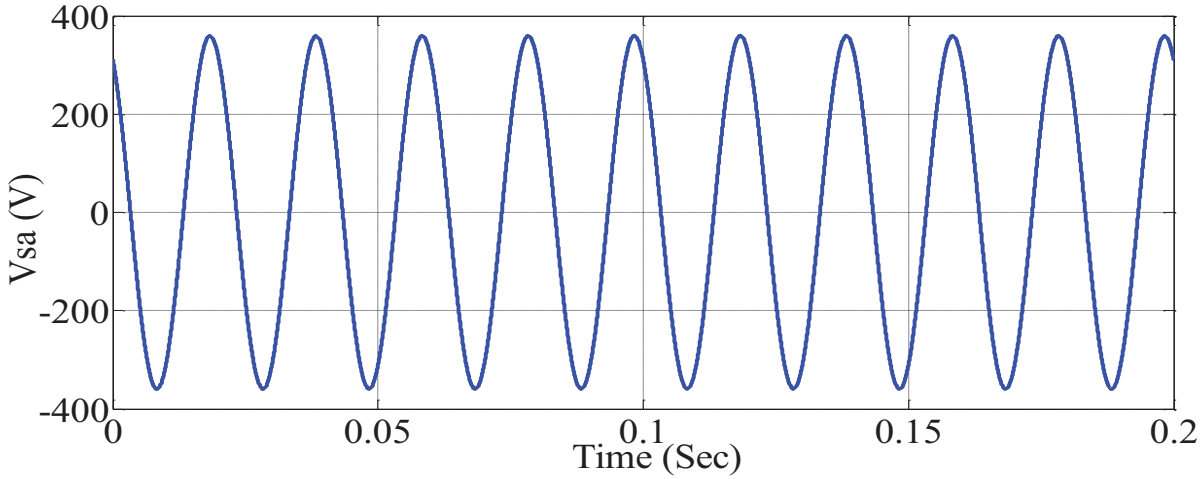

Fig. 5.4 (a) Source Voltage

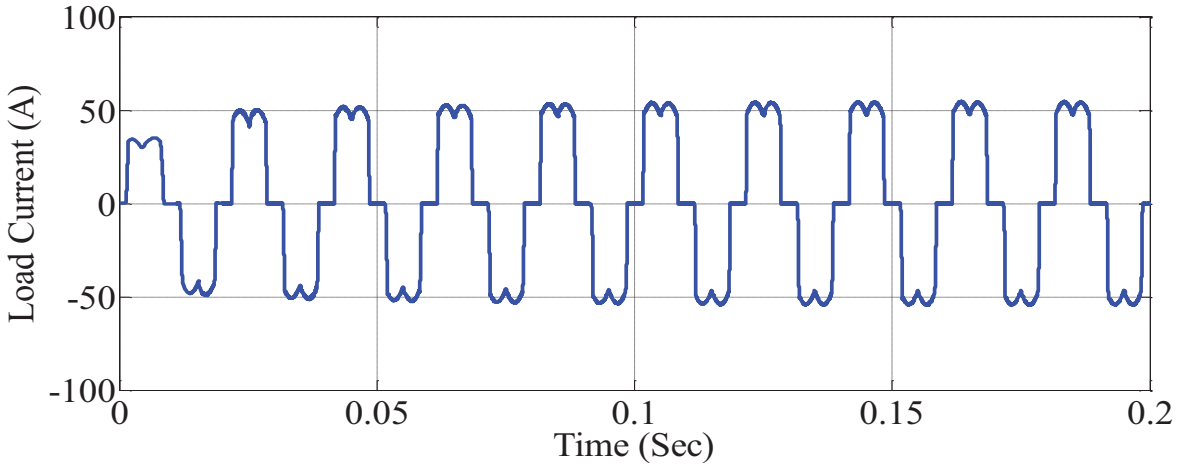

Fig. 5.4 (b) Load Current

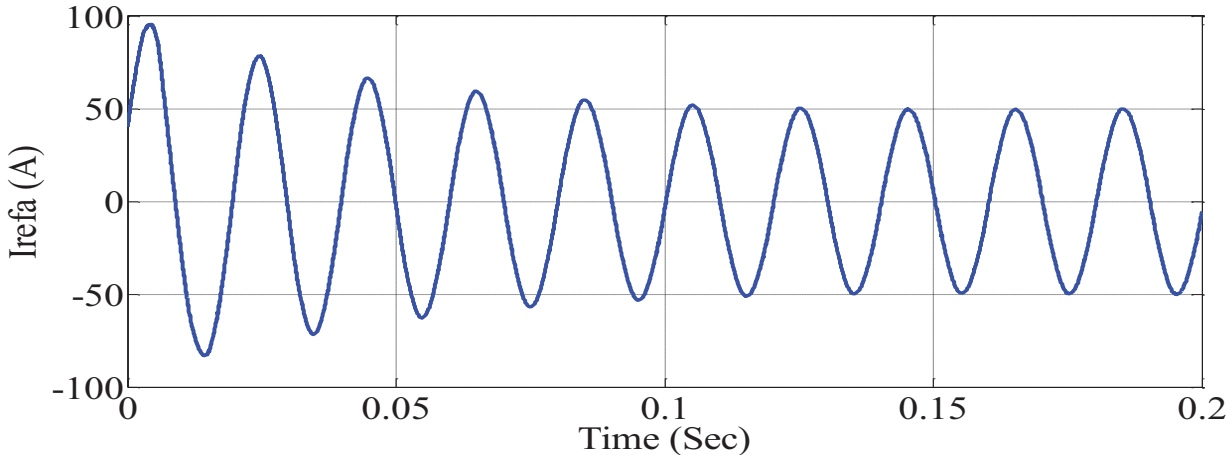

Fig. 5.4 (c) Reference Current

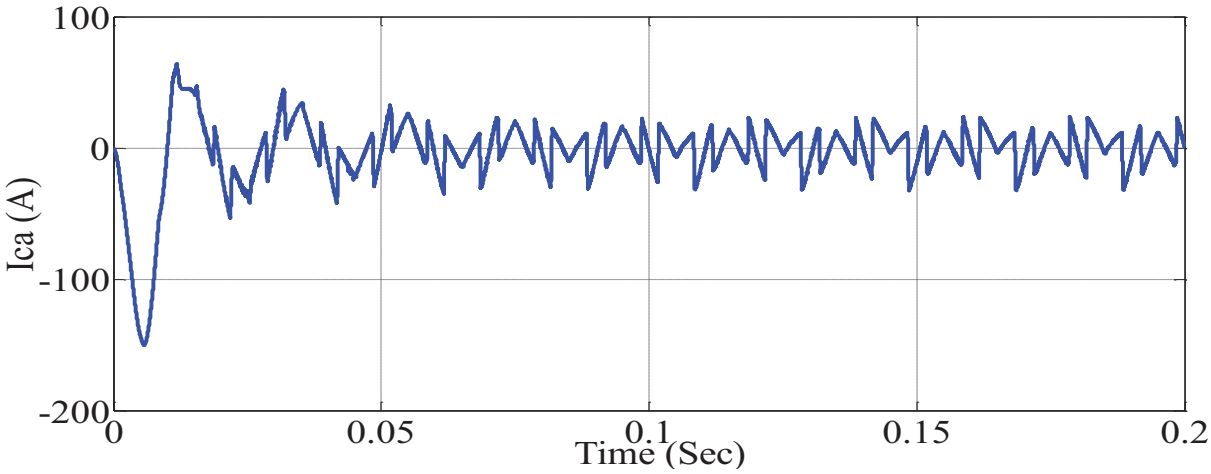

Fig. 5.4 (d) Compensating Current

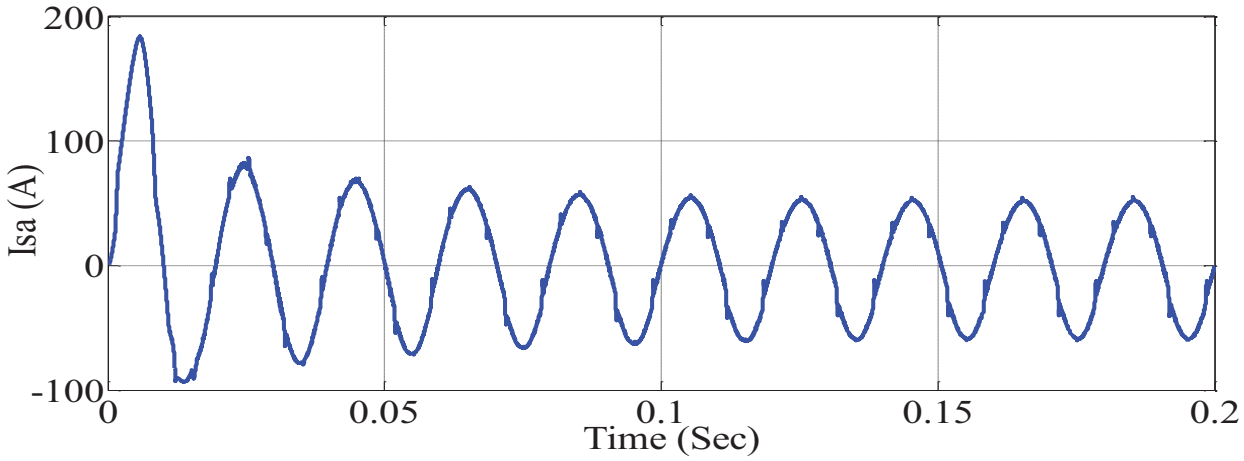

Fig. 5.4 (e) Source Current after Compensation

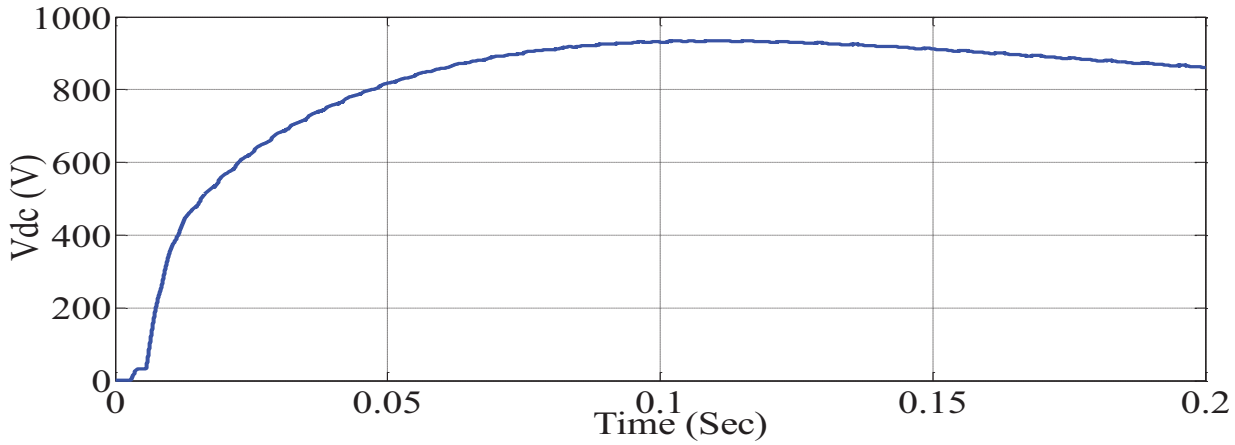

Fig. 5.4 (f) Voltage across Capacitor

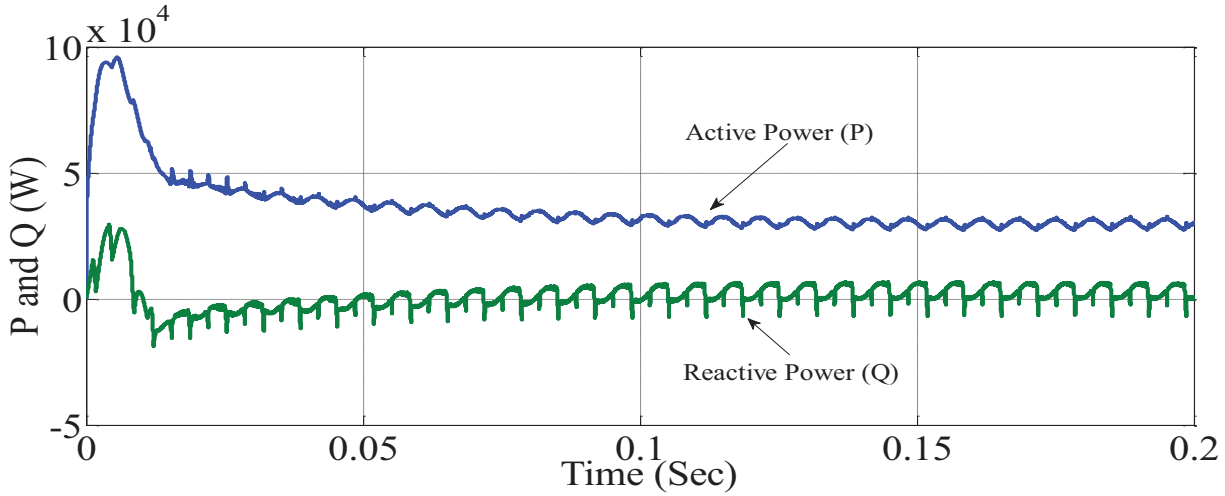

Fig. 5.4 (g) Active and Reactive Power

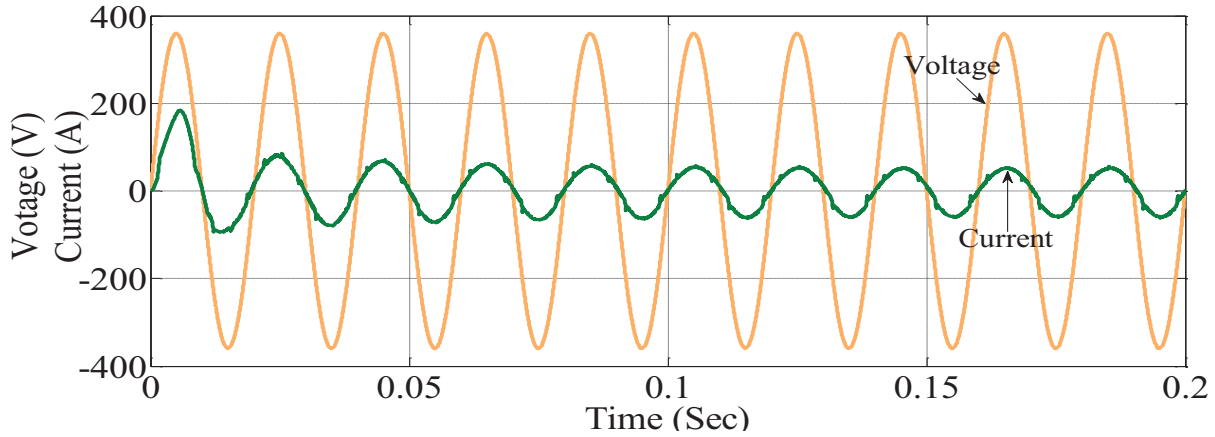

Fig. 5.4 (h) Source Voltage and Current

Fig. 5.4 Steady state response of APF with SRF and AHCC

For SRF with adaptive hysteresis controller, simulation time is taken as t=0 to t=0.2 sec with constant load in steady state. The source voltage is shown in the Fig. 5.4 (a).The load current is shown in Fig. 5.4(b), which is highly non-linear in nature. Here the analysis is done by taking only one phase out of three individual phases. The actual reference current for phase-a is shown in Fig. 5.4(c). The APF inject the compensating current to PCC, which is shown in Fig. 5.4 (d). The current after compensation is as shown in 5.4 (e). It is clear from the Figure that, the waveform is sinusoidal with less ripple compared to the hysteresis current controller technique. The voltage across the capacitor is settling down quickly after few cycle as shown in Fig. 5.4 (f). The magnitude of the active and reactive power is shown in Fig. 5.4 (g) and the source current and voltage which in Fig. 5.4 (h).

5.2.4 Transient State Performance of APF with SRF and Adaptive Hysteresis Current Controllers:

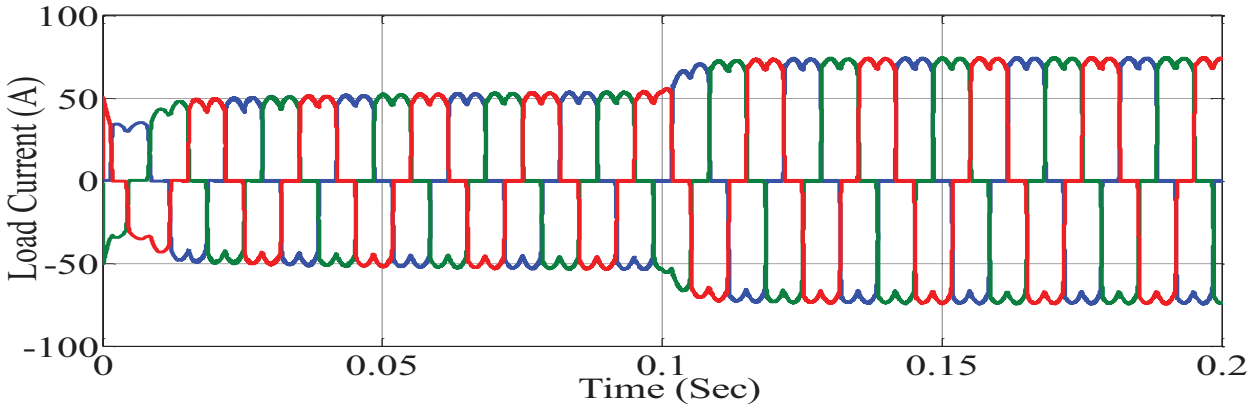

Fig. 5.5(a) Non-linear Load Current

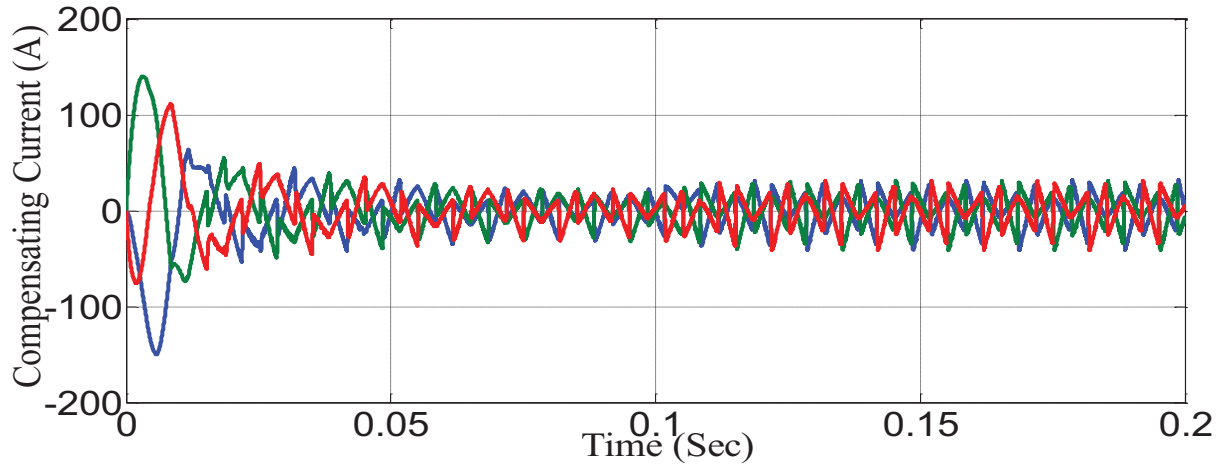

Fig. 5.5(b) Compensating Current

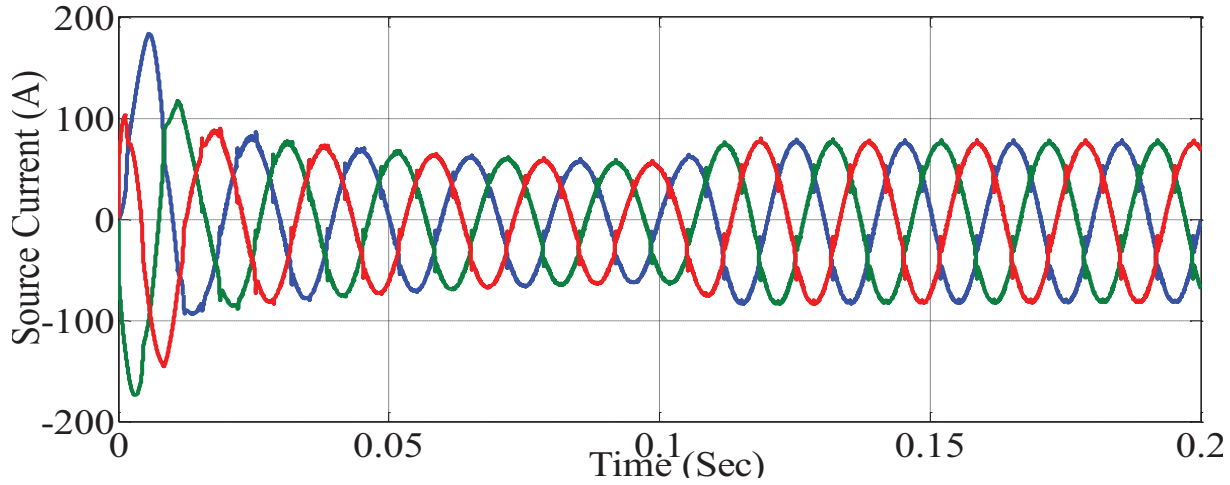

Fig. 5.5(c) Source Current after Compensation

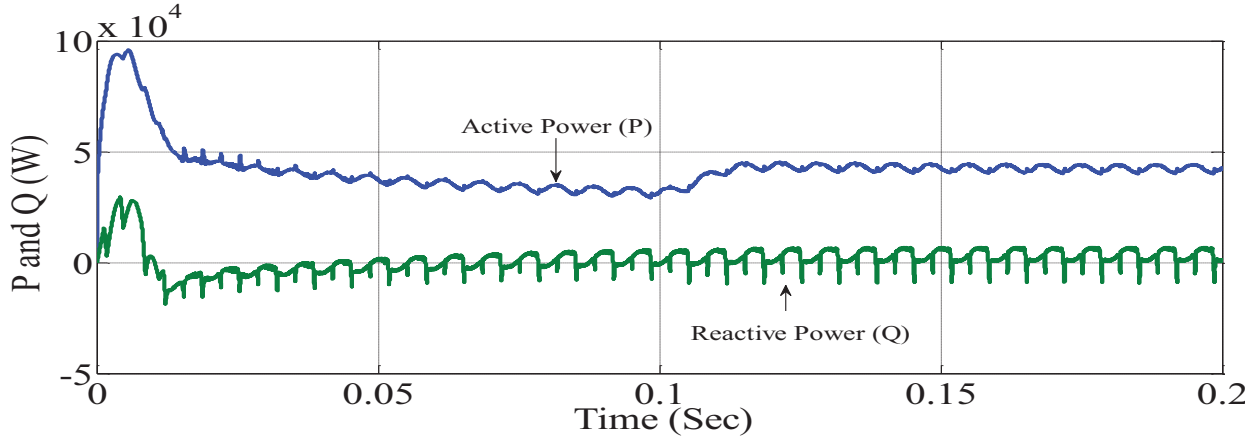

Fig. 5.5(d) Active and Reactive Power

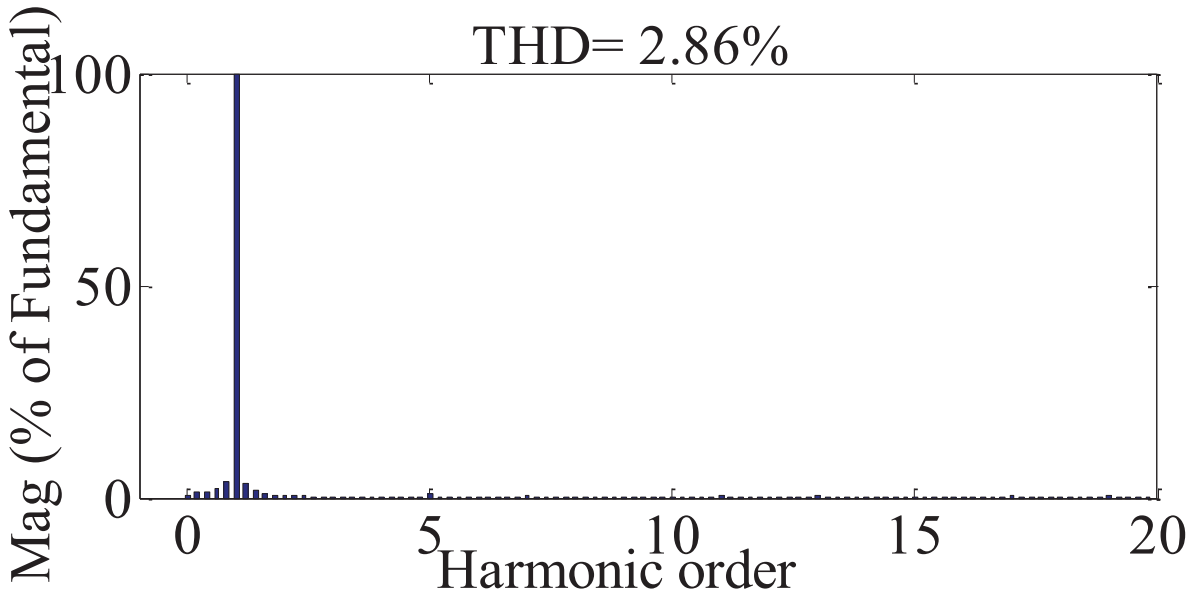

Fig. 5.5(e) Total Harmonic Distortion

Fig.5.5 Transient state response of APF with SRF and AHCC

Fig. 5.5(e) shows the total harmonic distortion (THD) of source current by using adaptive hysteresis current controller. The results in Fig. 5.5(e) presented both in the steady state and transient state conditions. Clearly source current THD indicating that, the harmonic content is reduced by using AHCC compared to the HCC. A comparison is made between HCC and AHCC in the following table at various load conditions.

TABLE 5.3 THD Analyses

Conditions	Without APF (%THD)	With APF (%THD)	
		HCC	AFCC
Steady State	26.67	3.50	2.86
Transient State	26.7	3.54	2.93

Simulations of integrated control circuit of APF are conducted with steady state and transient conditions. The results obtained show that the source current and load current THD has small variation in steady state and transient conditions. FFT analysis of the active power filter brings the THD of the source current into compliance with IEEE-519 & IEC-6000-3 standards.

5.2.5 Steady State Performance of APF with fuzzy logic controller and HCC:

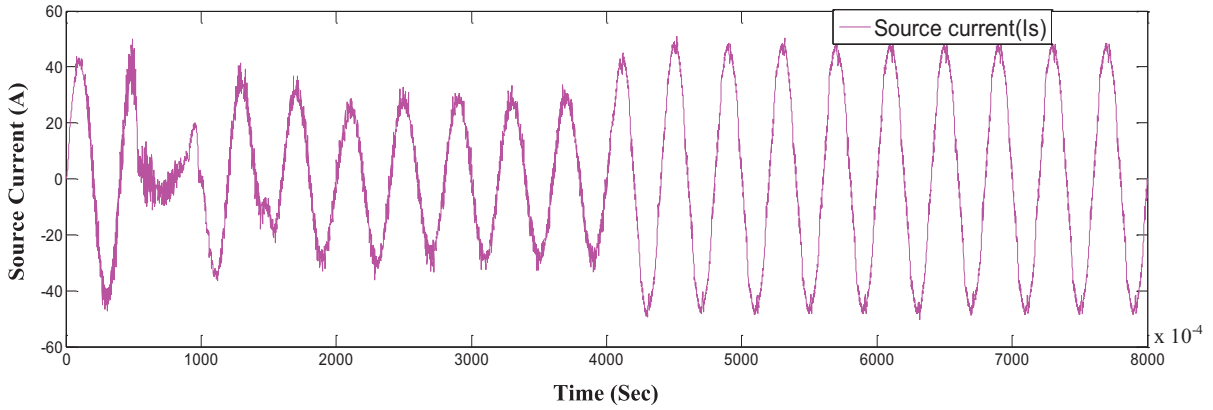

Fig.5.6 (a) source current with APF

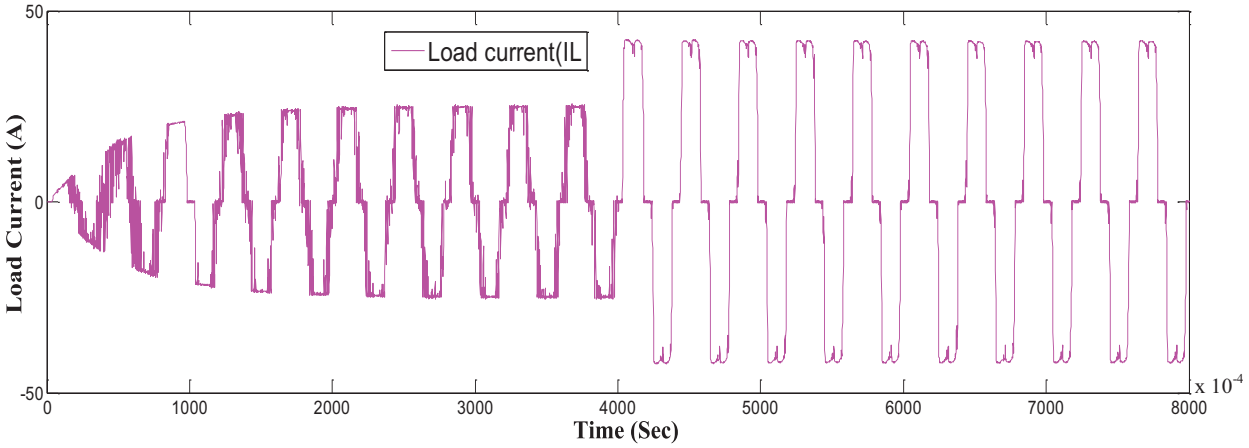

Fig.5.6 (b) Load current

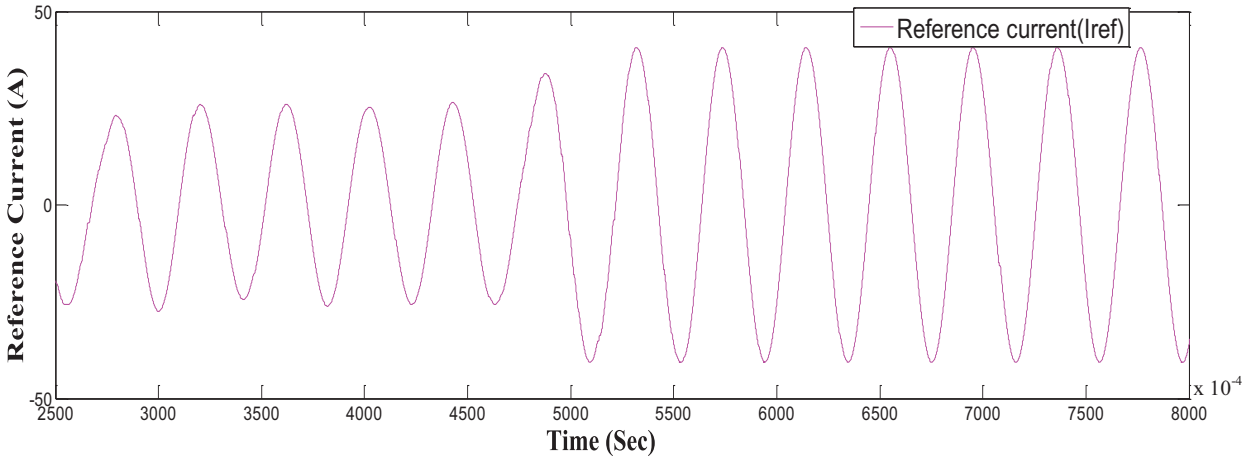

Fig.5.6 (c) Reference current

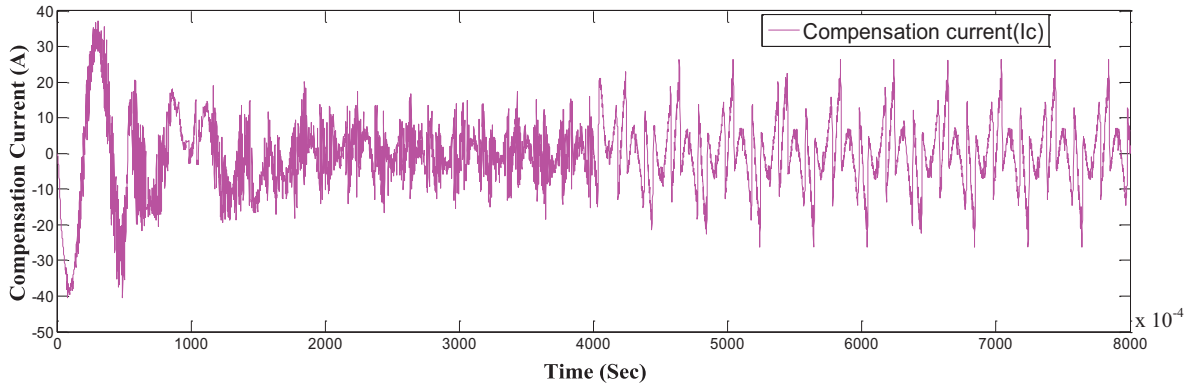

Fig. 5.6 (d) Compensation current generated by APF

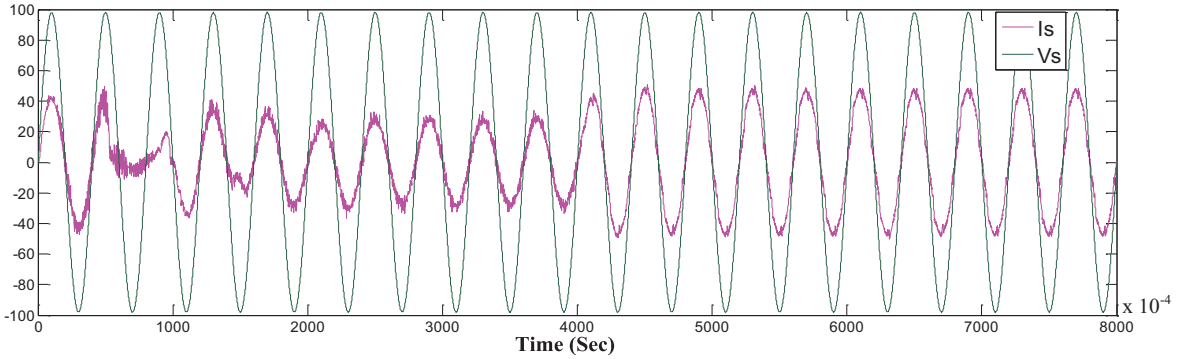

Fig. 5.6 (e) Current and Voltage

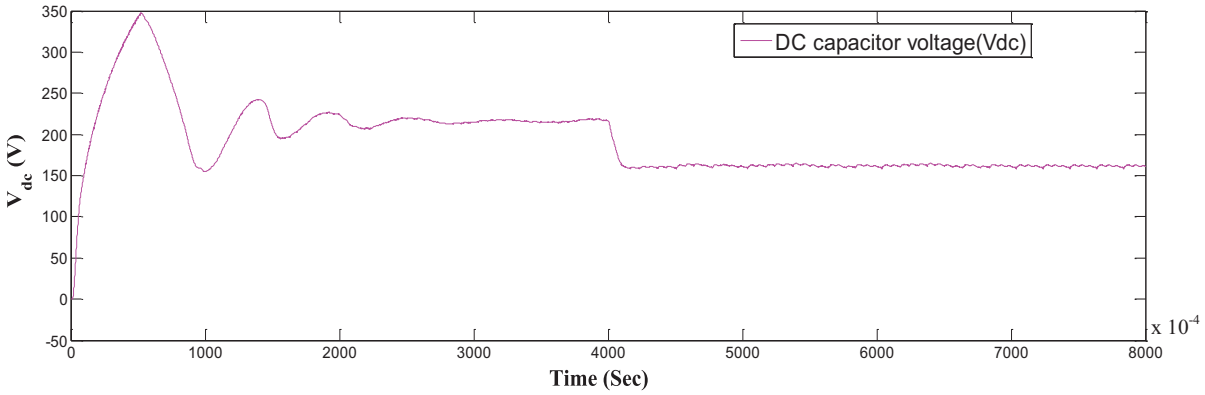

Fig. 5.6 (f) DC capacitor voltage

Fig 5.6 Steady state response of APF with fuzzy logic controller and HCC

Fig. 5.6 shows response of APF in steady state condition with fuzzy logic and hysteresis current controller in. Fig. 5.6 (a) shows the source current after compensation, even if the source current appears sinusoidal but it having small current ripples. Fig. 5.6 (f) shows the voltage

across the capacitor. It is clearly shown that the voltage across the capacitor is maintaining nearly steady value after few cycles.

5.2.6 Transient State Performance of APF with fuzzy logic controller and HCC:

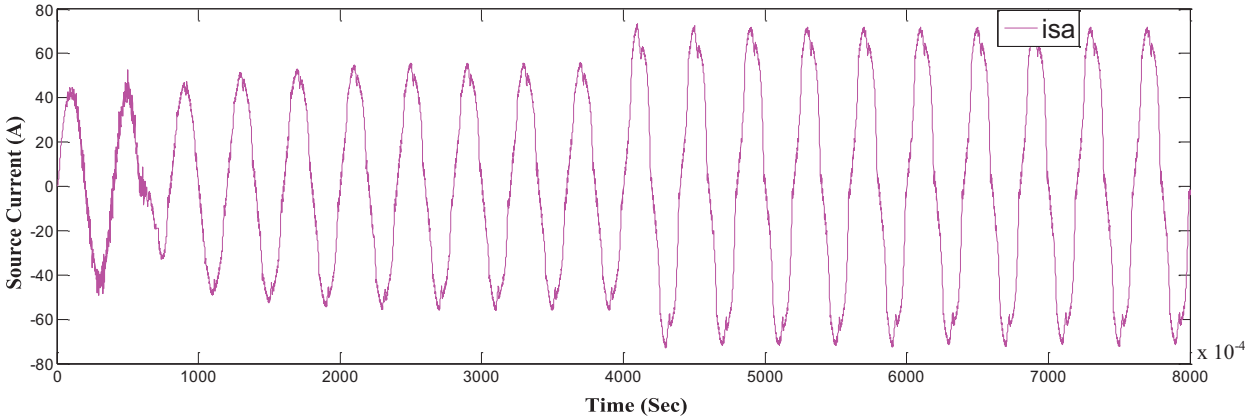

Fig. 5.7 (a) source current with APF

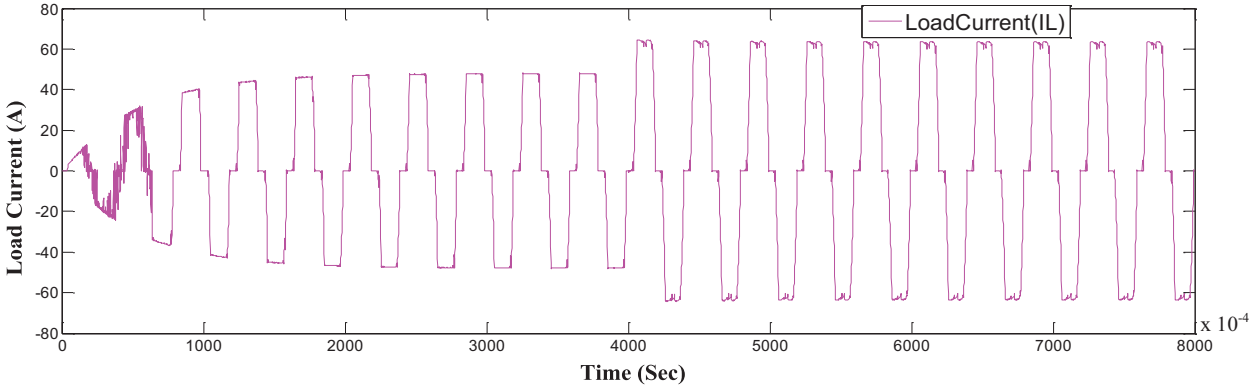

Fig. 5.7 (b) load current

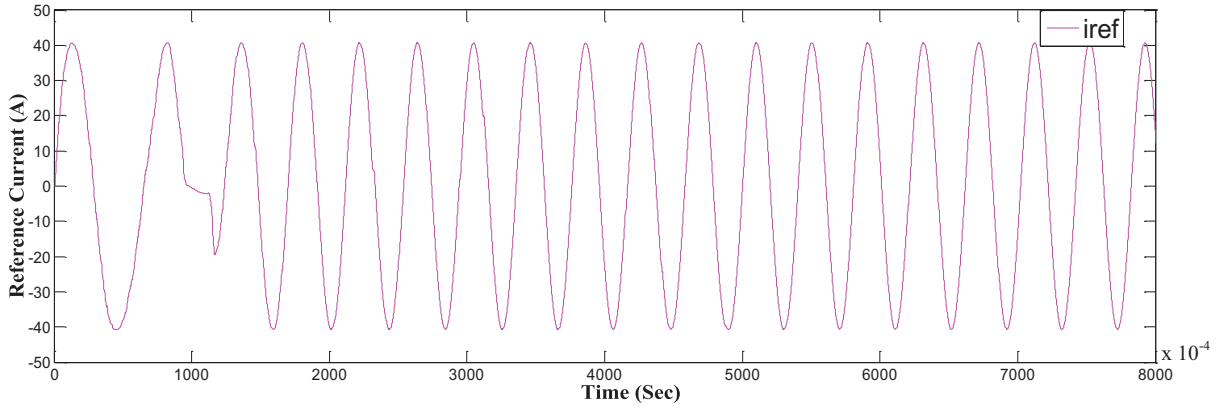

Fig. 5.7 (c) Reference current

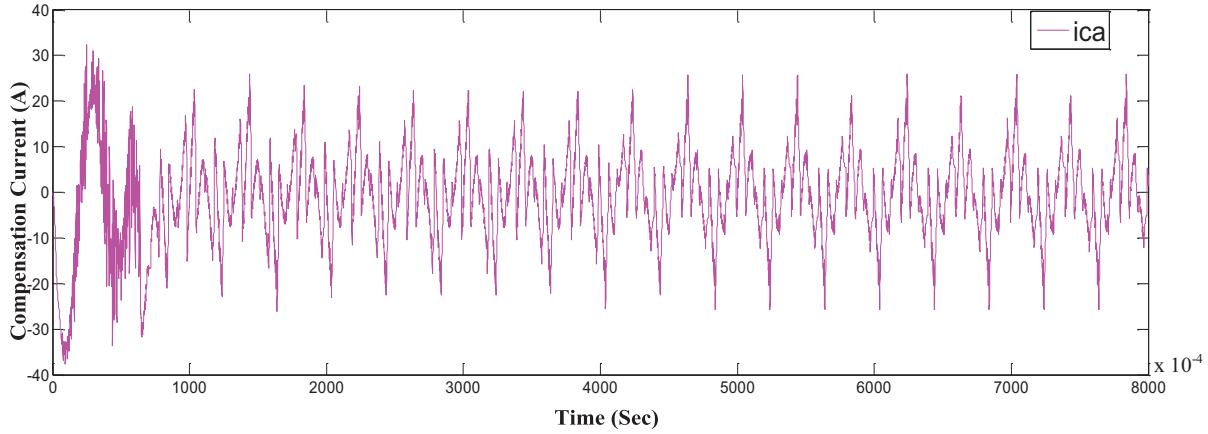

Fig. 5.7 (d) Compensation current genetated bu APF

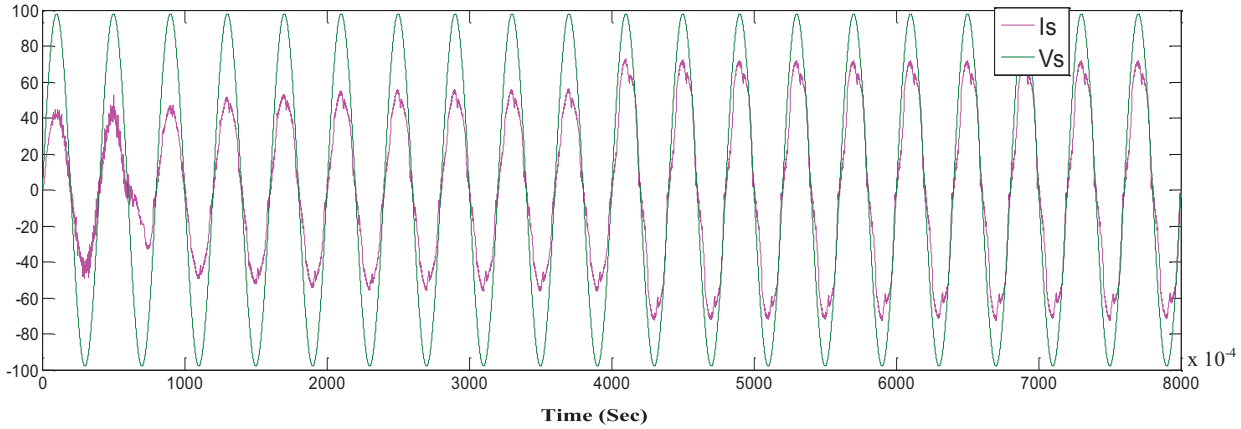

Fig. 5.7 (e) Voltage and Current

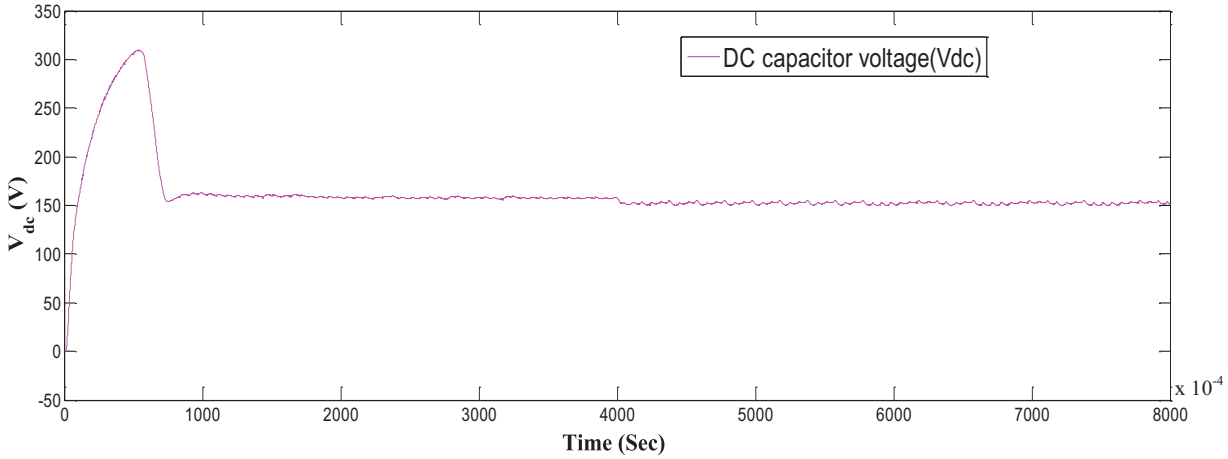

Fig. 5.7 (f) DC capacitor voltage

Fig. 5.7 Transient state response of APF with fuzzy logic controller and HCC

5.3 FPGA IMPLEMENTATION:

5.3.1 RTL Schematics of Digital Controller:

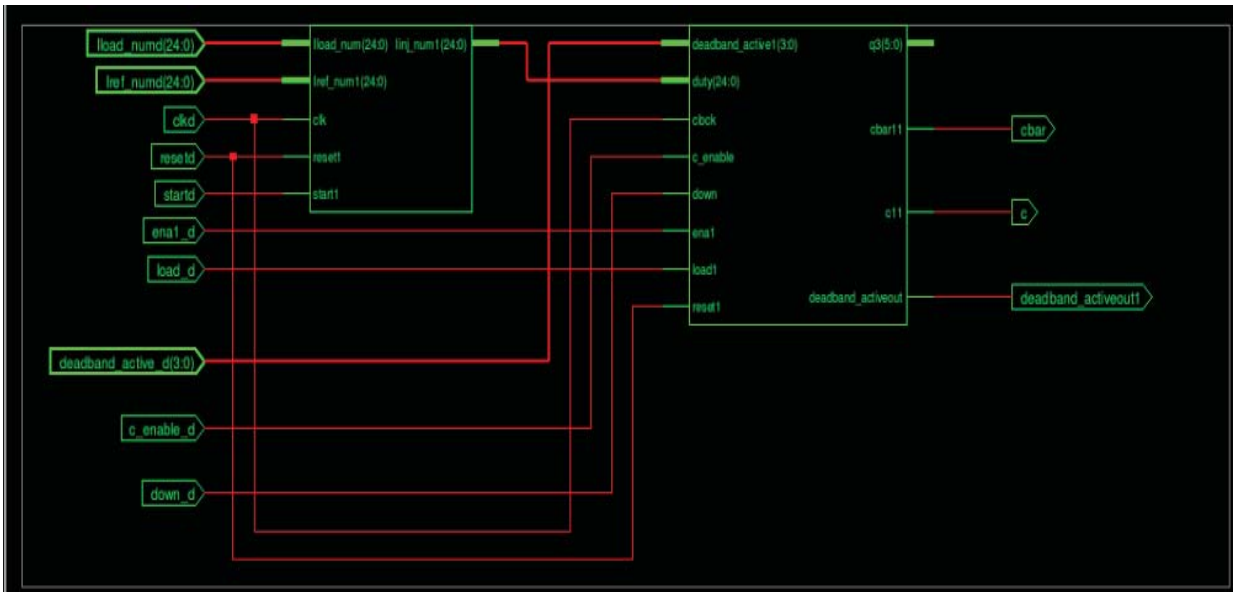

Fig. 5.8 (a) RTL schematics of hysteresis PI current controller

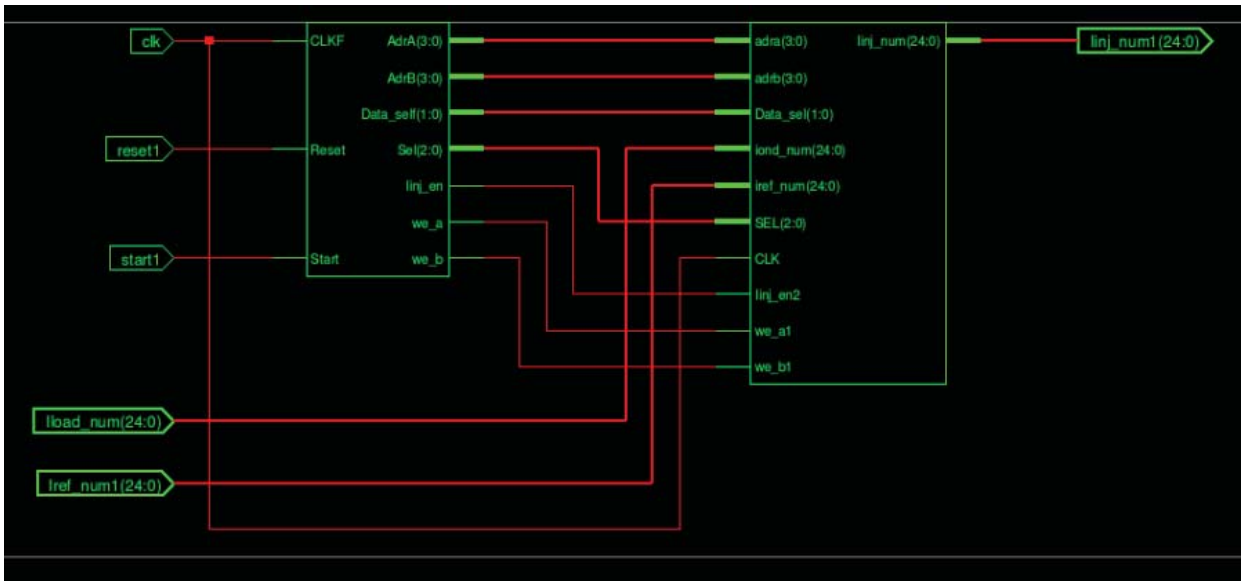

Fig. 5.8 (b) RTL schematics of FMSD (finite machine and data path)

Fig.5.8 RTL schematics of digital controller

After writing the VHDL code, Fig. 5.7 (a) shows the RTL (Register transfer level) schematics of total digital PI hysteresis current controller. It indicates that the number of inputs and outputs corresponding to the controller. The RTL schematics of the FSMD (finite machine and data path) architecture is shown in Fig. 5.7 (b).

5.3.2 Switching Pulse Generation by Using Digital Controller:

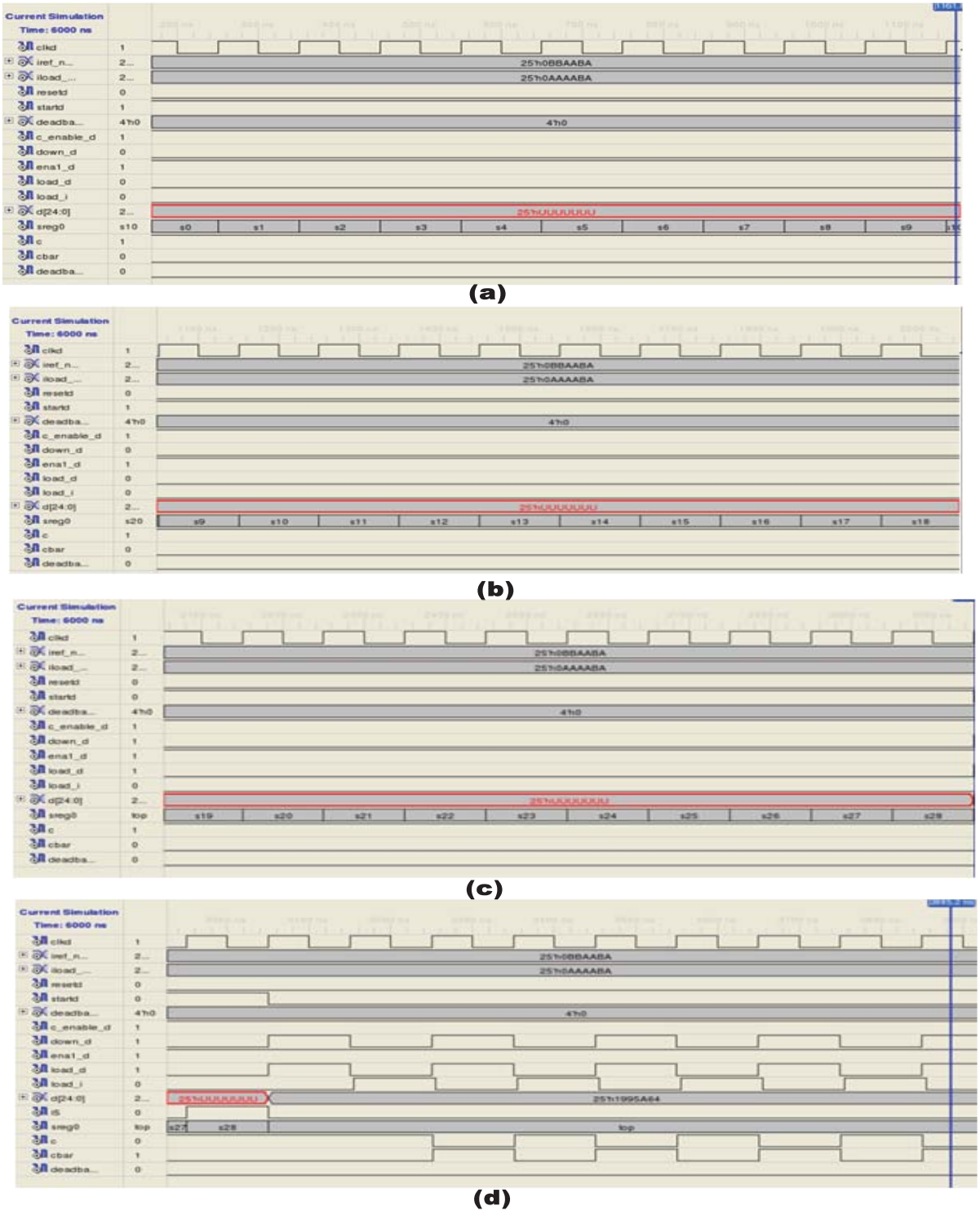

Fig. 5.9 Simulation results for switching pulse generation (a) state 0 to 8, (b) state 9 to 18, (c) state 19 to 28, (d) c and c' switching pulses obtained after state 28.

The calculation of error Iinj_num will take 29 states from S0 to S28 as shown in Fig. 5.8 (a) (c).The comparator along with the help of a up/down counter(decides the hysteresis band) gives the switching pulses C and C' by comparing the error signal (Iinj_num) and the band as shown in Fig. 8 (d). The following table shows the device utilization summary.

TABLE 5.7 DEVICE UTILIZATION SUMMARIES

Logic utilization	Used	Available	Utilization
Number of slices	273	4676	5 %
Number of slice flip flops	206	9312	2 %
Number of 4 input LUTs	504	9312	5 %
Number of bonded IOBs	63	190	33 %

CHAPTER 6

CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

6.1 CONCLUSIONS:

- During this part of the project work the performance of the shunt active power filter is analyzed using HCC & AHCC technique for minimizing harmonics, compensating reactive power and improving the pf in the power system.
- The SRF theory is used to generate reference current from the distorted load current and maintain the PWM VSI DC side capacitor nearly constant.
- Also Fuzzy logic controller is used to extract the reference current and maintain the PWM VSI DC side voltage nearly constant. The beauty of this controller is, it can applicable to any system where mathematical models are difficult to get.
- The performance of the AHCC and fixed HCC shunt active power filter are verified with the simulation results. Form the results; it clearly indicates that, the current ripple is less by using HCC compared to AHCC. The transient response and steady state performance of these two current controllers have been compared. The THD of the source current after compensation is 2.86 % which is less than 5 %, the harmonic limit imposed by the IEEE-519 & IEC-6000-3 standard. A digital HCC has been implemented for three phase shunt active power filter
- The digital controller (FSMD+HCC) is implemented in FPGA platform by using chip-scope pro analyzer and is imported to FPGA for hardware implementation.
- The gate pulses for PWM VSI observed through CRO by dump the VHDL code in to the FPGA kit.

6.2 SUGGESTIONS FOR FUTURE WORK:

- Experimental investigations can be done on shunt APF by developing a prototype model in the laboratory to verify the simulation results for both conventional and digital controllers.
- By taking the algorithm of digital HCC development of control algorithm for AHCC.

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