DESIGN OF A NOVEL HIGH SPEED DYNAMIC COMPARATOR WITH LOW POWER DISSIPATION FOR HIGH SPEED ADCs

A THESIS SUBMITTED

By

PRASUN BHATTACHARYYA

Roll No: 209EC2123

to

The Department of Electronics and Communication Engineering

in partial fulfillment of the requirements

for the degree of

Master of Technology

In

VLSI Design & Embedded Systems

NATIONAL INSTITUTE OF TECHNOLOGY ROURKELA

ROURKELA, ORISSA

MAY, 2011

DESIGN OF A NOVEL HIGH SPEED DYNAMIC COMPARATOR WITH LOW POWER DISSIPATION FOR HIGH SPEED ADCs

A THESIS SUBMITTED

By

PRASUN BHATTACHARYYA

Roll No: 209EC2123

to

The Department of Electronics and Communication Engineering

in partial fulfillment of the requirements

for the degree of

Master of Technology

In

VLSI Design & Embedded Systems

Under the guidance of

Prof. Kamala Kanta Mahapatra

NATIONAL INSTITUTE OF TECHNOLOGY ROURKELA

ROURKELA, ORISSA

National Institute Of Technology
Rourkela

CERTIFICATE

This is to certify that the thesis entitled, "**DESIGN OF A NOVEL HIGH SPEED DYNAMIC COMPARATOR WITH LOW POWER DISSIPATION FOR HIGH SPEED ADCs"** submitted by **PRASUN BHATTACHARYYA (209EC2123)** in partial fulfillment of the requirements for the award of Master of Technology degree in Electronics and Communication Engineering with specialization in "VLSI design & Embedded systems" during session 2010-2011 at National Institute Of Technology, Rourkela (Deemed University) and is an authentic work by him under my supervision and guidance .

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other university/institute for the award of any Degree or Diploma.

Date:

Prof. K. K. Mahapatra
Dept. of Electronics and Communication Engineering
National Institute of Technology
Rourkela

ACKNOWLEDGMENTS

First of all, I would like to express my deep sense of respect and gratitude towards my advisor and guide **Prof. K. K. Mahapatra,** who has been the guiding force behind this work. I want to thank him for introducing me to the field of Analog Design and giving me the opportunity to work under him. I consider it my good fortune to have got an opportunity to work with such a great person.

I express my sincere respect and gratitude to our Head of the Department **Prof. S.K. Patra**, He has given full of resources and lots of support towards completion of my project and from bottom of my heart, I would like to thank him.

I also would like to thank our Research Scholar **Ayaskanta Swain, Jaganath Prasad Mohanty, Srinivas V.S. Sarma D., Prakash Rout** of the **Department of Electronics and Communication Engineering, NIT Rourkela** for their generous help in various ways for the completion of this thesis.

I would like to thank my friends, especially, **Preetisudha Meher, Dipanjan Bhadra, Bibhu Prasad Panda** for their help during the course of this work. I am also thankful to my classmates for all the thoughtful and mind stimulating discussions we had, which prompted us to think beyond the obvious.

I am especially indebted to my parents (**Mr. Sankar Bhattacharyya and Mrs. Ruma Bhattacharyya**) and my grandmother **Mrs. Lalita Banerjee** for their love, sacrifice, and support. They are my first teachers after I came to this world and have set great examples for me about how to live, study, and work.

ABSTRACT

A new CMOS dynamic comparator using dual input single output differential amplifier as latch stage suitable for high speed analog-to-digital converters with High Speed, low power dissipation and immune to noise than the previous reported work is proposed. Back-to-back inverter in the latch stage is replaced with dual-input single output differential amplifier. This topology completely removes the noise that is present in the input. The structure shows lower power dissipation and higher speed than the conventional comparators. The circuit is simulated with 1V DC supply voltage and 250 MHz clock frequency. The proposed topology is based on two cross coupled differential pairs positive feedback and switchable current sources, has a lower power dissipation, higher speed, less area, and it is shown to be very robust against transistor mismatch, noise immunity. Previous reported comparators are designed and simulated their DC response and Transient response in Cadence® Virtuoso Analog Design Environment using GPDK 90nm technology. Layouts of the proposed comparator have been done in Cadence® Virtuoso Layout XL Design Environment. DRC and LVS has been checked and compared with the corresponding circuits and RC extracted diagram has been generated. After that post layout simulation with 1V supply voltage has been done and compared the speed, power dissipation, Area, delay with the results before layout and the superior features of the proposed comparator are established.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

THESIS OVERVIEW

1.1. BASICS OF CMOS COMPARATOR:

Comparators are most probably second most widely used electronic components after operational amplifiers in this world. Comparators are known as 1-bit analog-to-digital converter and for that reason they are mostly used in large abundance in A/D converter. . In the analog-to-digital conversion process, it is necessary to first sample the input. This sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal. The conversion speed of comparator is limited by the decision making response time of the comparator. Apart from that, comparators are also can be found in many other applications like zero-crossing detectors, peak detectors, switching power regulators, BLDC operating motors, data transmission, and others. The basic functionality of a CMOS comparator is used to find out whether a signal is greater or smaller than zero or to compare an input signal with a reference signal and outputs a binary signal based on comparison. The schematic symbol and basic operation of a voltage comparator are shown in fig1.1, this comparator can be thought of as a decision making circuit.

1.1.1 Definition:

The comparator is a circuit that compares an analog signal (voltage) with another analog voltage or reference voltage and outputs a binary signal based on the comparison.

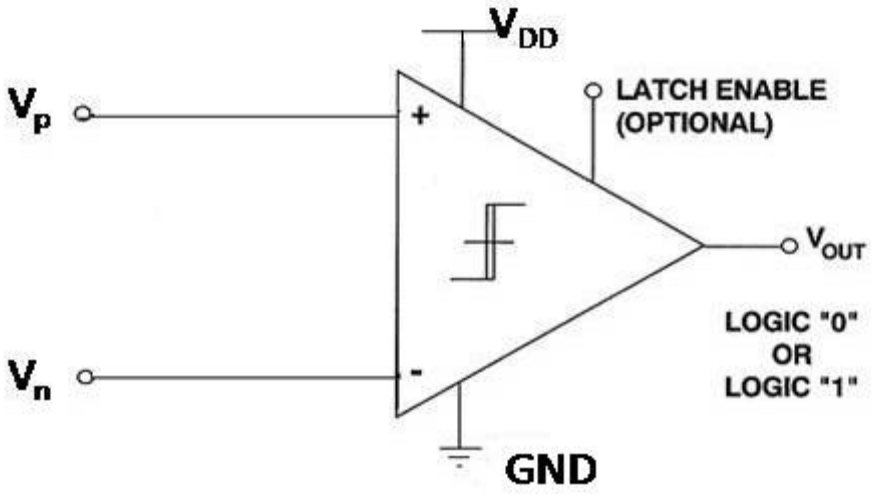


Figure 1.1 (a): Schematic of Comparator

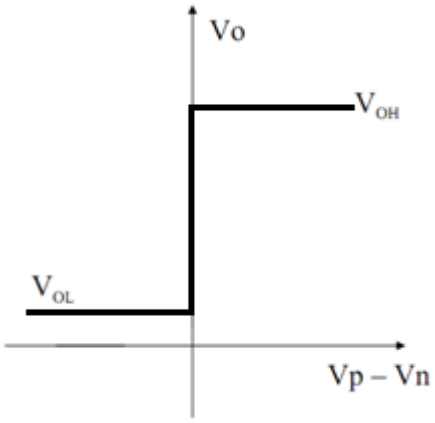


Figure 1.1 (b): Ideal voltage transfer characteristic of comparator.

Figure 1.1(a) shows the schematic symbol of the comparator and 1.1 (b) shows its ideal transfer characteristics. V_P is the input voltage (Pulse voltage) applied to the positive input terminal of comparator and V_n is the reference voltage (constant DC voltage) applied to the negative terminal of comparator. Now if V_p , the input of the comparator is at a greater potential than the V_n, the reference voltage, then the output of the comparator is a logic 1, where as if the V_p is at a potential less than the V_n , the output of the comparator is at logic 0.

If $V_p > V_n$, then V_o= logic 1.

If $V_p < V_n$, then V_o= logic 0.

What is meant here by an analog signal is one that can have any of a continuum of amplitude values at a given point in time .In the strictest sense a binary signal can have only one of two given values at any point in time, but this concept of a binary signal is too ideal for real-world situations, where there is a transition region between the two binary states. It is important for the comparator to pass quickly through the transition region of the analog signal. The presentation on comparators will first examine the requirements and characterization of comparators. It will be seen that comparators can be divided into open-loop and regenerative comparators. The open-loop comparators are basically op amps without compensation. Regenerative comparators use positive feedback, similar to sense amplifiers or flip-flops, to accomplish the comparison of the magnitude between two signals. A third type of comparator emerges that is a

combination of the open-loop and regenerative comparators. This combination results in comparators that are extremely fast.

1.2 Motivation:

Nowadays high speed devices like High speed ADCs, operational amplifiers became of great importance. And for these high speed applications, a major thrust is given towards low power methodologies. Minimization in power consumption in these devices can be achieved by moving towards smaller feature size processes. However, as we move towards smaller feature size processes, the process variations and other non-idealities will greatly affect the overall performance of the device. Now analog-to-digital converter requires lesser power dissipation, low noise, better slew rate, high speed, less hysteresis, less Offset. The performance limiting blocks in such ADCs are typically inter-stage gain amplifiers and comparators. The power consumption, speed takes major roll on performance measurement of ADCs. Dynamic comparators are being used in today's A/D converters extensively because these comparators are high speed, consume lesser power dissipation, having zero static power consumption and provide full-swing digital level output voltage in shorter time duration. Back-to-back inverters in these dynamic comparators provide positive feedback mechanism which converts a smaller voltage difference in full scale digital level output. However, an input-referred latch offset, resulting from the device mismatches such as threshold voltage, current factor β(=μCoxW/L) and parasitic node capacitance and output load capacitance mismatches, limits the accuracy of such comparators [7], [8]. This offset voltage can be minimized by introducing preamplifier based comparators as shown in Figure 1.2.

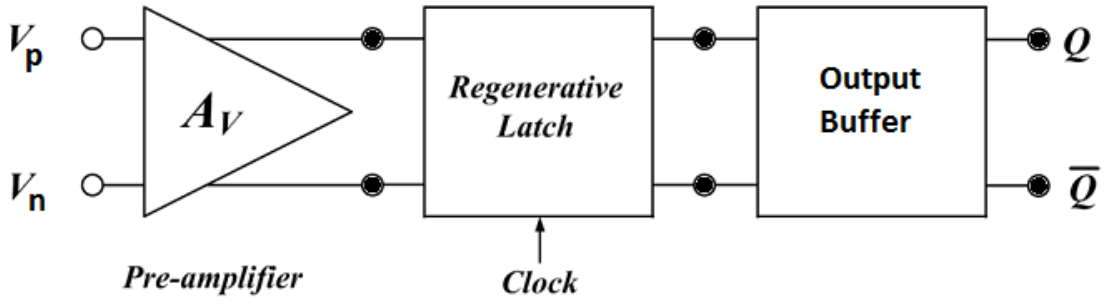


Figure 1.2: Preamplifier based comparator.

It can amplify a small input voltage difference to a large enough voltage to overcome the latch offset voltage and also can reduce the kickback noise [11]. However, the pre-amplifier based comparators suffer large static power consumption as well as from the reduced intrinsic gain with a reduction of the drain-to-source resistance r_{ds} due to the continuous technology scaling [10].

1.3 Thesis Organization:

This thesis provides a new dynamic comparator which shows lower power dissipation, better speed and least effected by noise than the conventional and existing comparators. The Thesis can be organized as follows. **Chapter 2** provides the literature survey and advantages and disadvantages of the existing comparators. **Chapter 3** describes the comparator characteristics. **Chapter 4** provides analysis of the present comparators and compares their results. **Chapter 5** introduces the proposed comparator and provides its analysis. **Chapter 6** provides the results of the simulation and discussion about it. **Chapter 7** discusses about conclusion and future scope of work with the proposed comparator.

CHAPTER 2

LITERATURE REVIEW

By literature review, we find that there are various types of comparator architectures available in our today's electronic world. Among these comparators, we analyzed the static and dynamic characteristics & advantages and disadvantages of *Preamplifier Based Comparator* i.e. comparators having a preamplifier followed by a regenerative latch stage which is again followed by an output buffer (which is basically a self-biased differential amplifier) and *Fully Dynamic Latched Comparators* i.e. comparators having positive feedback based back-to-back latch stage that determines output of the circuit.

2.1. Preamplifier based comparator [11, 12, 14]:

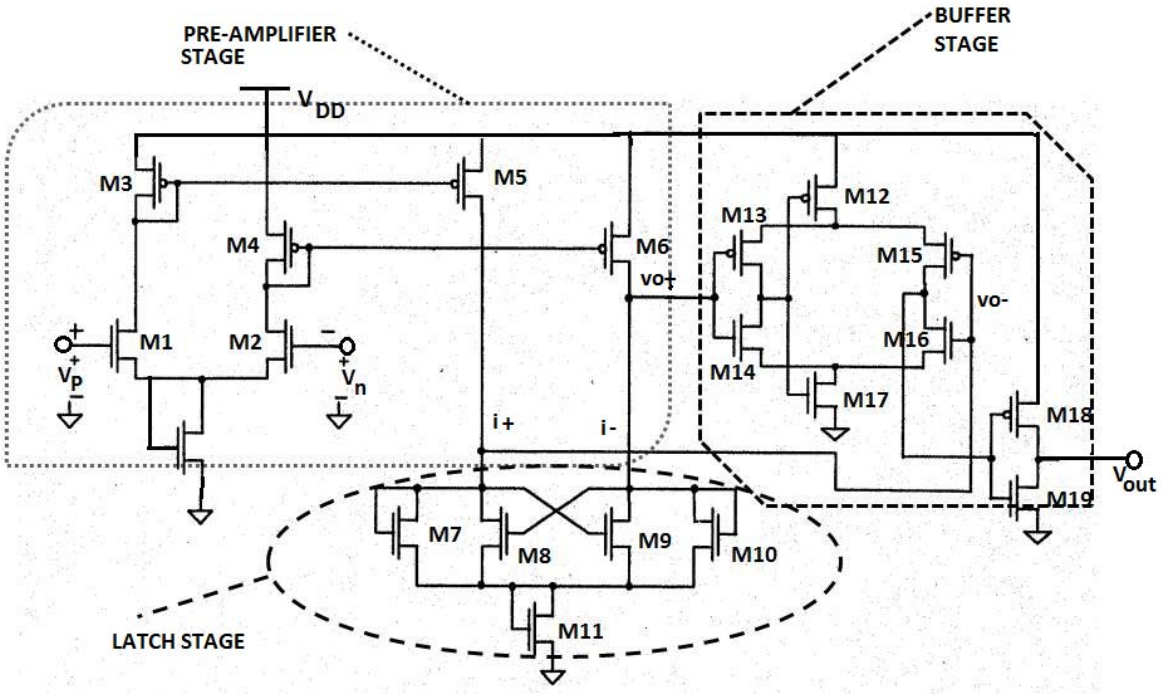


Figure 2.1: Preamplifier based comparator.

Figure 2.1 shows the preamplifier based comparator. The comparator consists of three stages: the input preamplifier stage, a latch stage, and an output buffer stage (it is basically a self-biased differential amplifier followed by an inverter which gives the digital output. The preamplifier stage is basically a differential amplifier with active loads [11]. The preamp stage (or stages) amplifies the input signal to improve the comparator sensitivity (i.e., increases the minimum input signal with which the comparator can make a decision) and isolates the input of the comparator from switching noise (often called kickback noise) coming from the positive feedback stage [11]. It also can reduce input referred latch offset

voltage. The sizes of Ml and M2 are set by considering the diff-amp transconductance and the input capacitance. The transconductance sets the gain of the stage, while the size of Ml and M2 determines the input capacitance of the comparator [11]. Here $g_{m1}= g_{m2}$.

The positive feedback latch stage is used to determine which of the input signals is larger and extremely amplifies their difference [12]. It takes positive feedback from the cross gate connection of M8 and M9. Consider i+ >> i- so that M7 and M9 are ON and M8 and M10 are OFF. Here also $\beta_7= \beta_{10}=\beta_a$ and $\beta_8= \beta_9=\beta_b$ for which vo- is ~ 0V and v0+ is

$$\mathbf{vo+}= \sqrt{\frac{\mathbf{i+}}{\beta_a}} + V_{th}$$

If we start to increase i- and decrease i+, when drain to source voltage of M9 is equal to the threshold voltage, V_{th} of M8, switching takes place. At this point M8 takes current away from M7 which decreases drain to source voltage of M7 and M9 turns off. If we assume that maximum value of v+ or v- is equal to $2V_{th,}$ then under these circumstances M8 and M9 operate under cut-off or triode region under steady state conditions [11]. Then voltage across M9 becomes V_{th} and M9 enters into saturation and current of M9 is

$$i- = \frac{\beta_b}{\beta_a}\ i+$$

This is the point at which switching takes place; i.e. M9 shuts off and M8 turns on. If $\beta_a= \beta_b$, then switching takes place when the currents, i+ and i-, are equal. A similar analysis of increasing i+ and decreasing i- results in

$$i+= \frac{\beta_b}{\beta_a}\ i-$$

The output buffer, the final component of our comparator, converts the output of the latch stage into a full scale digital level output (logic 0 or logic 1). The output buffer should accept a differential input signal and not have slew-rate limitations. The circuit of the output buffer is basically a self-biased differential amplifier followed by an inverter. The inverter is added as a separate additional gain stage and isolates any load capacitance from differential amplifier [11].

In summary, the preamplifier based comparator offers high speed and less offset voltage but has huge static power consumption.

2.2 Fully dynamic latch based comparators:

2.2.1. Latch-Type voltage SA (Sense Amplifier) [1, 2]:

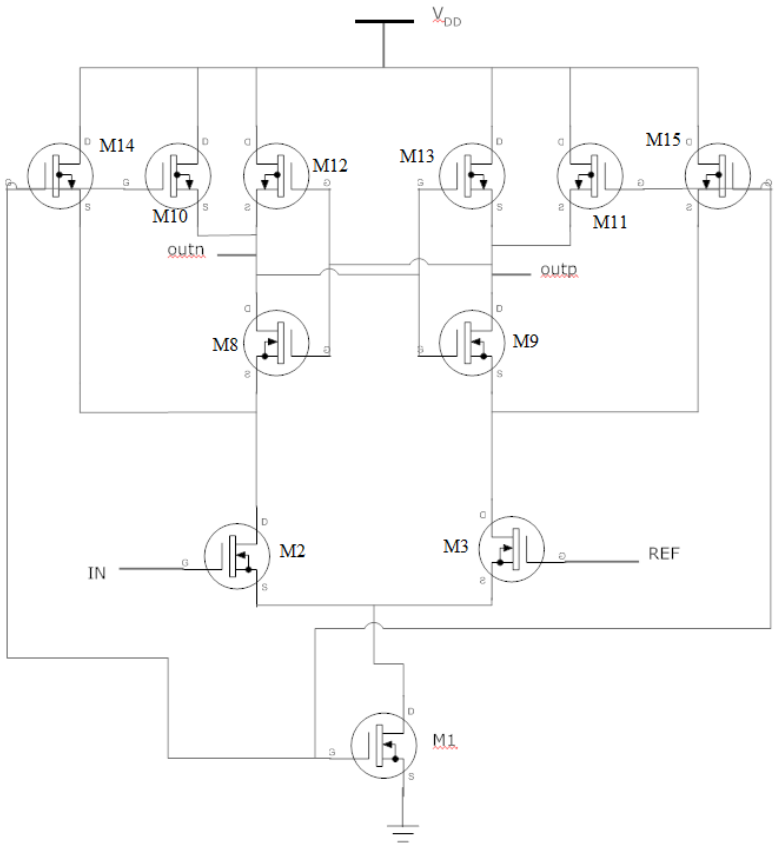


Figure 2.2: A Latch Type Voltage Sense Amplifier [1, 2].

Latch type sense amplifiers are used to read the contents of the different kinds of memory, A/D converters, data receivers and on-chip transistors since they yield fast decision due to positive feedback. These are very effective comparators [3]. Figure 2.2 shows the circuit diagram of the latch type voltage sense amplifier that uses back to back latch stage to generate positive feedback. This circuit was introduced by Kobayashi *et al.* in 1993 [1]. The current flow of the differential input transistors M8 and M9 controls the latch circuit. A small difference between currents through M8 and M9 converts to a large output voltage. Extra switching transistors M10 and M11 are added to increase its characteristics. These circuits are used in sense amplifier based flip-flop, current-sensed SRAM [2].

2.2.1.1. Operation:

During *reset phase* when *clk=0V*, the output nodes of the comparator are reset to V_{DD} through the reset transistors M10 and M11. During *evaluation phase* when *clk=*V_{DD}, M1 turns ON and the input transistors M2 and M3 starts to discharge Ni node voltages to GND. When any of Ni node voltages falls from V_{DD} to V_{DD}-V_{tn}, NMOS transistors of the cross coupled inverters turn ON initiating positive feedback. Further when any of *out* node voltage drops to V_{DD}-V_{tp}, PMOS transistors of the inverters turns ON and further enhances the positive feedback and converts a small input voltage difference to large full scale output.

2.2.1.2. Drawbacks [5]:

To increase the drive current of the cross-coupled latch stage, M1 has to be size up. If size of M1 is increased, then the drain currents of both M2 and M3 will be increased during the evaluation phase (clk = V_{DD}). Because of that the Ni nodes of M2, M3 will be discharged from V_{DD} to ground in a very short period because of which the the time duration of M2 and M3 being operated in the saturation region decreases. Hence the lower amplification of the input voltage difference will be made. Moreover this structure shows very strong dependency on speed with different common mode input voltages, it is now become less attractive for ADCs [5].

Using this SA in low-voltage deep-sub-micron CMOS technologies is difficult because stack of the four transistors requires large voltage headroom. And also speed and offset of this SA is very much dependent on the common mode voltage of the input because of which it is problematic to use this SA in A/D converters where wide common mode ranges are used [3].

2.2.2. Double-Tail Latch Type Voltage SA [3]:

Figure 2.3 shows the schematic of the Double-Tail Latch type Voltage SA. Double-Tail derived from the fact that the comparator uses one tail for input stage and another for latching stage. It has less stacking and can therefore operate at lower supply voltages [3]. Large size of the Transistor M14 enables large current at latching stage which is independent of common mode voltages at inputs and small size of M1 offers lower supply voltages resulting lower offset.

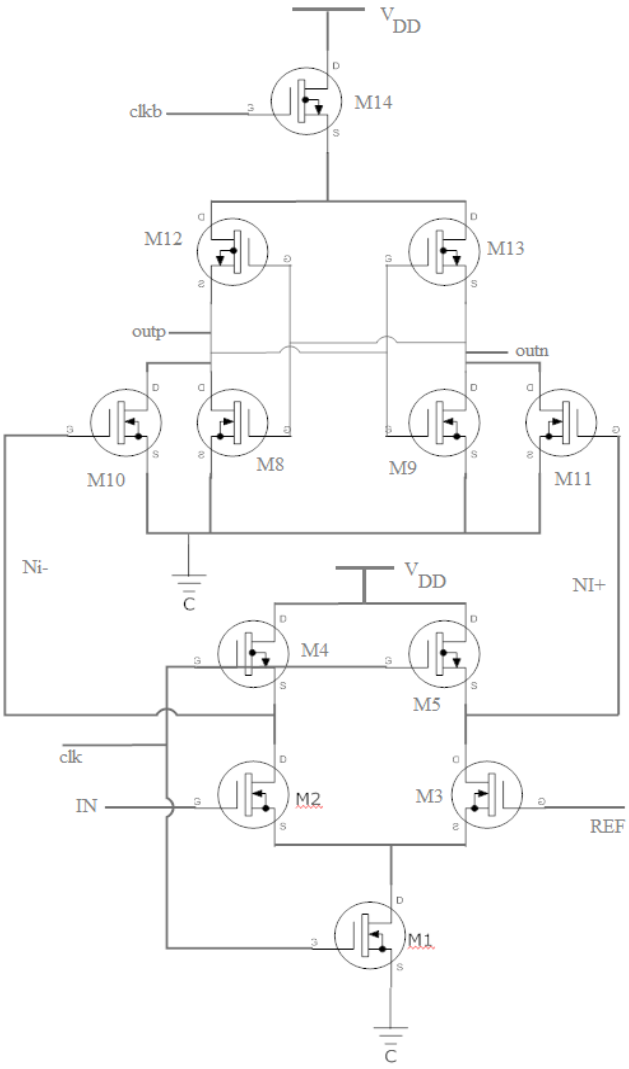


Figure 2.3: Double-Tail Latch Type Voltage Sense Amplifier [3].

2.2.2.1. Operation:

During rest phase (clk=0V), M4 and M5 charges to V_{DD} which in turn charges Ni nodes to V_{DD}. Hence M10 and M11 turns on and discharges output nodes to GND. During evaluation phase (clk=V_{DD}), the tail current transistors M1 and M14 turns ON. On Ni nodes common mode voltage decreases and one input dependent differential mode voltage generates. M10 and M11 pass this differential mode voltage to latch stage. The inverters start to regenerate the voltage difference as soon as the common-mode voltage at the Di nodes is no longer high enough for M10 and M11 to clamp the outputs to ground [3]. M10 and M11 also provide additional shielding between the input and output which in turn reduces kickback noise.

2.2.2.2 Disadvantages:

clk and clkb requires high accuracy timing because the latch stage has to regenerate the differential input voltage coming from input stage at very limited time. Now if we replace the clkb with the inverter whose input is clk signal then clk has to drive heavier load in order to drive largest transistor M14 in a smallest possible delay. Now if clkb leads clk, then comparator will undergo increased power dissipation and if clkb lags clk, it results in increased delay means less speed of operation due to short circuit current path from M14 to M10/M11 through M12/M13 [5].

2.2.3. Energy Efficient Two Stage Comparator [13]:

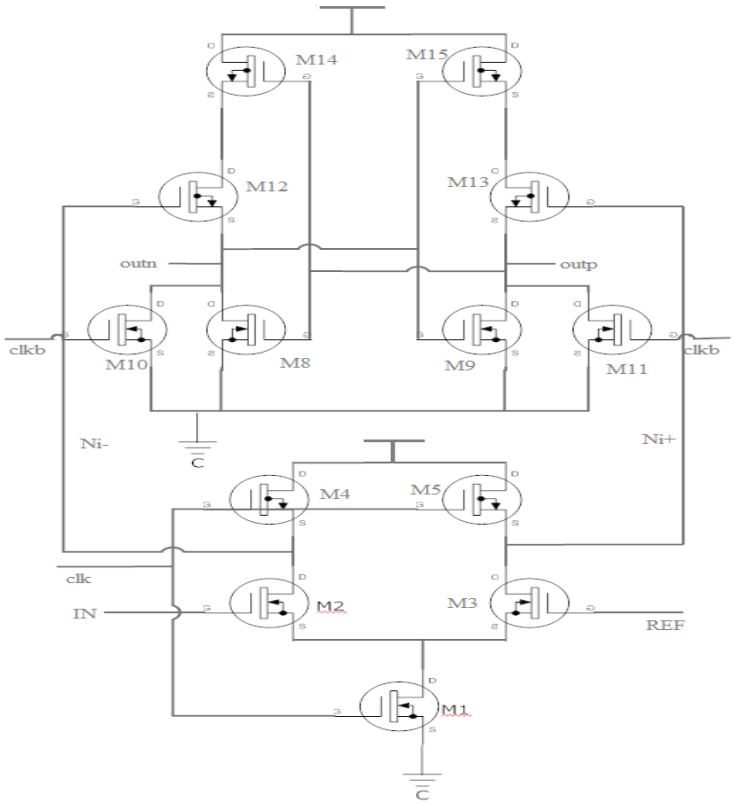


Figure 2.4: Energy Efficient Two-Stage Comparator [13]

Figure 2.4 shows the energy efficient two-stage comparator. The circuit is almost same as Figure.2.3 except the output latch stage. By modifying the output latch stage during reset phase (clk=0V and clkb=VDD), the drain diffusion capacitances of PMOS transistors M14 and M15 & NMOS transistors M2 and M3 is much lesser than the Ni node capacitances. And hence it can be operated in lesser power dissipation and higher speed

than the previous comparator. But still the clocking problem was not solved since clk and clkb is operating in same clock signal as that was in previous comparator.

2.2.4 Dynamic Comparator without Calibration [4]:

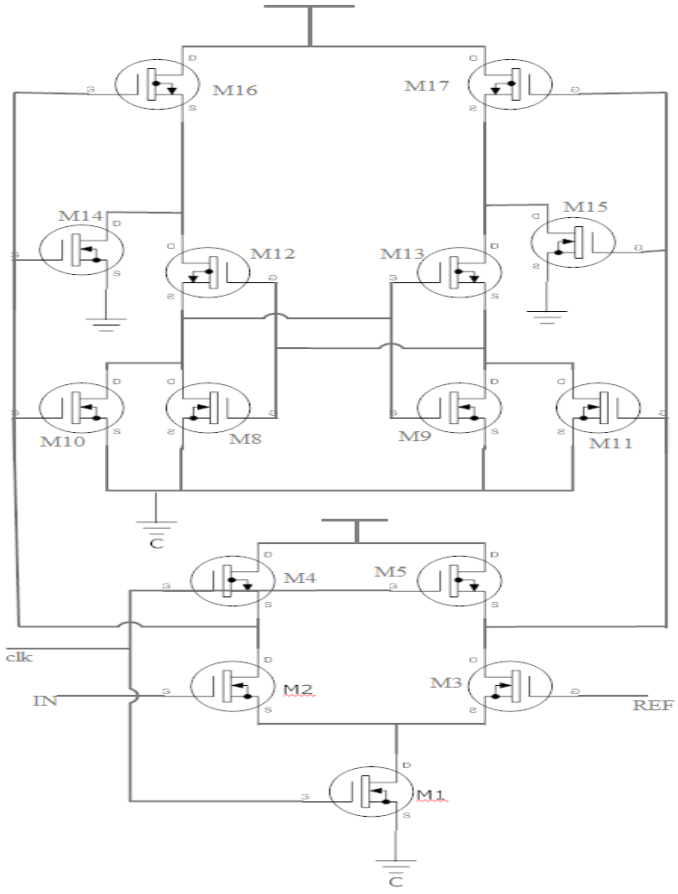


Figure 2.5 Self-Calibrating Dynamic Comparator [4]

Figure 2.5 shows the Self-Calibrating Dynamic Comparator. This comparator resolved the above said problem by replacing clkb signal with Ni nodes. But it results in increased delay since transistor M16/M17 use Ni node voltages as their input signal which shows a slow exponential decay shape and hence the current drivability of the output node decreases. The input referred latch offset is also reduced in this circuit due to the fact that output latch stage takes load from the M10/M11 and M16/M17. Maximum drive current of the output node also decreased to half since the supply voltage VDD has been divided into two transistors.

2.2.5 Double-Tail Dual-Rail Dynamic Latched Comparator [5, 15]:

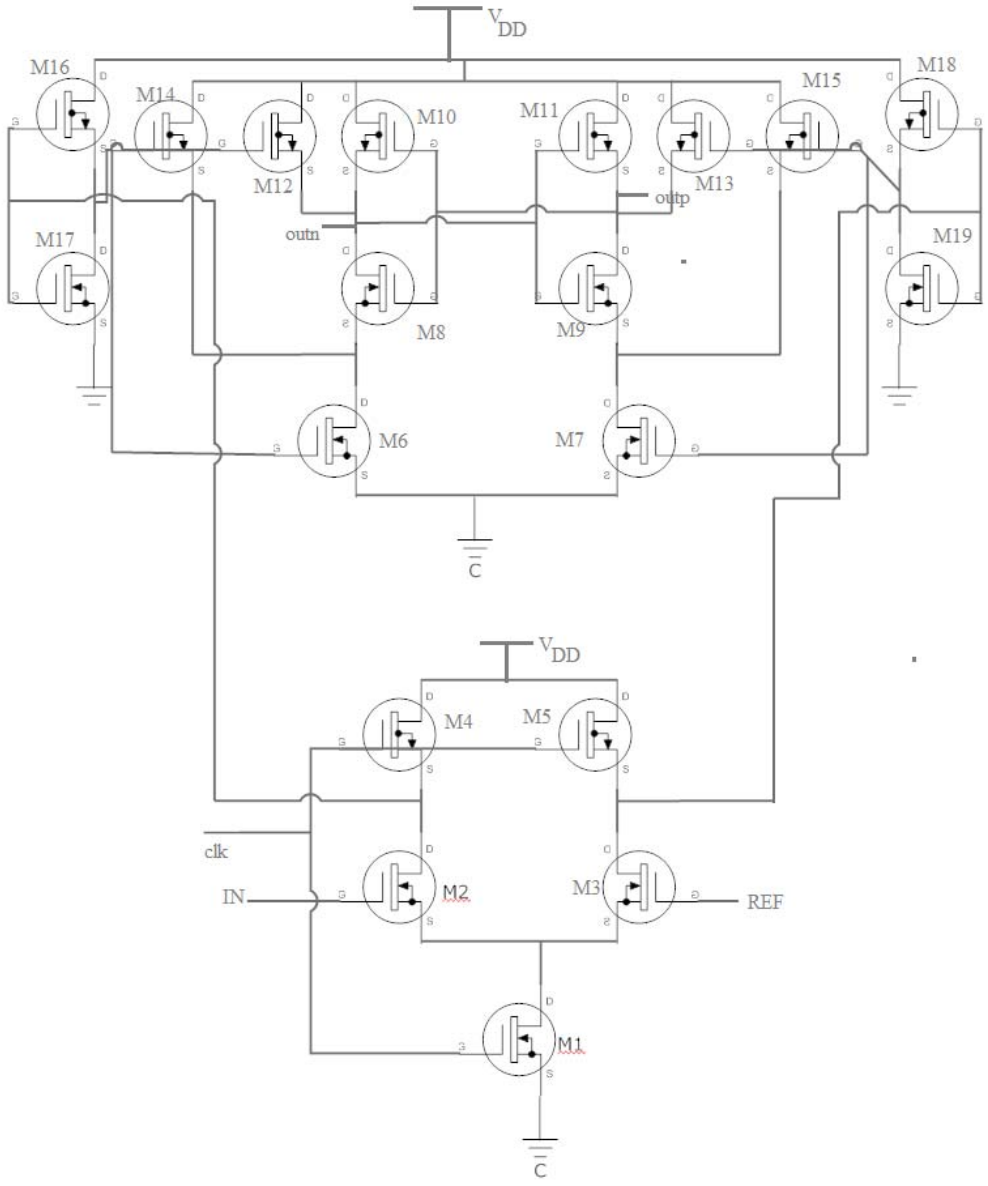


Figure 2.6: Double-Tail Dual-Rail Dynamic Comparator

Figure 2.6 shows the schematic of the Double-Tail Dual-Rail Dynamic Comparator. This comparator eliminated the weakened Ni nodes by inserting an inverter between input and output stages. Due to inverter, weak signal of Ni node is regenerated and fed to the output stage. This comparator shows faster operation and lesser power dissipation than the previous comparators.

CHAPTER 3

COMPARATOR CHARACTERISTICS

In this section we will describe both static and dynamic characteristics of comparator. Figure 3.1 shows the ideal characteristics of the comparator.

3.1 Static Characteristics:

Static characteristics comprises of gain, output high (V_{OH}) and low states (V_{OL}), Input Resolution, Offset and Noise.

3.1.1 Gain:

Gain of comparator can be written as:

$$\text{Gain} = A_v = \lim_{\Delta V \to 0} \frac{V_{OH}\text{-}V_{OL}}{\Delta V} \text{ where } \Delta V \text{ is the input voltage change}$$

a. First-Order Model for a Comparator:

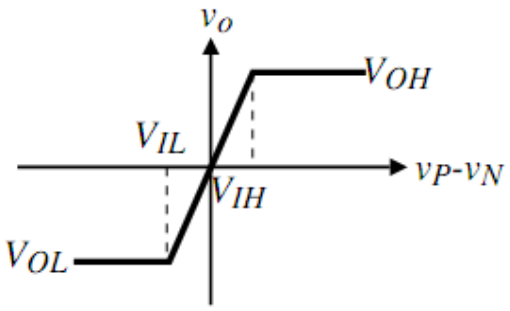


Figure 3.1 First-Order Model of Comparator [8].

VIH= Smallest input voltage for which the output voltage is VOH

VIL= Largest input voltage for which the output voltage is VOL

$$\text{The voltage gain is } A_v = \frac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}}$$

b. First Order Model With Input Offset Voltage and Noise:

Figure 3.2 shows the first order model with input offset voltage and noise.

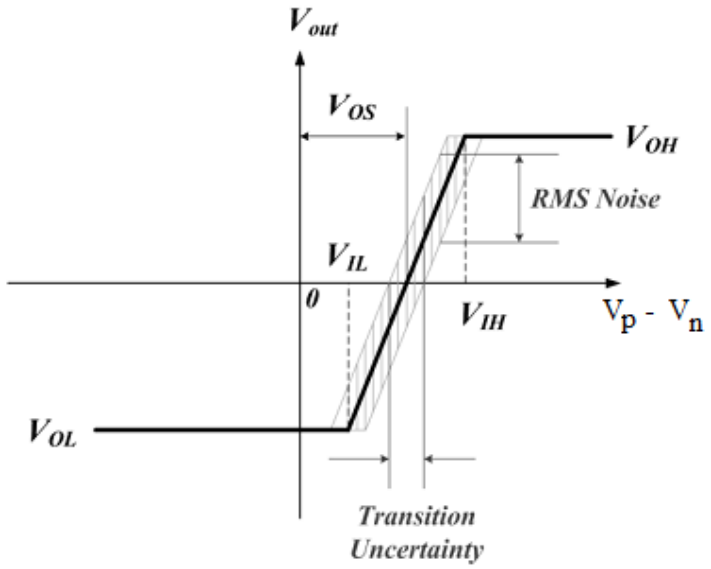


Figure 3.2: First order model with input offset voltage and noise.

3.1.2 Resolution: It is the input voltage change which is necessary to make output swing to valid binary states.

3.1.3 Offset: Offset voltages can be classified as two types viz. (i) systematic offset and (ii) random offset. Offset in the Operational amplifier as well in the comparators generates due to input transistor mismatches (i.e. mismatches in threshold voltages and mismatches in transconductance parameter $\beta=\mu C_{ox}$ W/L).

3.1.3.1 Input Offset Current: The input offset current is the difference between the separate currents entering the input terminals of a balanced amplifier.

3.1.3.2 **Input Offset Voltage*:*** The input offset voltage is that voltage which must be applied between the input terminals to balance the amplifier**.**

3.1.3.3 Output Offset Voltage: The output offset voltage is the dc voltage present at the output terminal when the two input terminals are grounded.

3.1.4 Noise: Noise of a comparator is modeled as if the comparator were biased in the transition region. Noise leads to an uncertainty in the transition region which causes jitter.

3.1.5 Input Common Mode Range (ICMR): This can be defined as the range of input voltage where comparator functions normally & meets all required specifications.

3.2 Dynamic Characteristics:

Dynamic characteristics of the comparator comprises of Propagation delay and Gain.

3.2.1 Propagation delay:

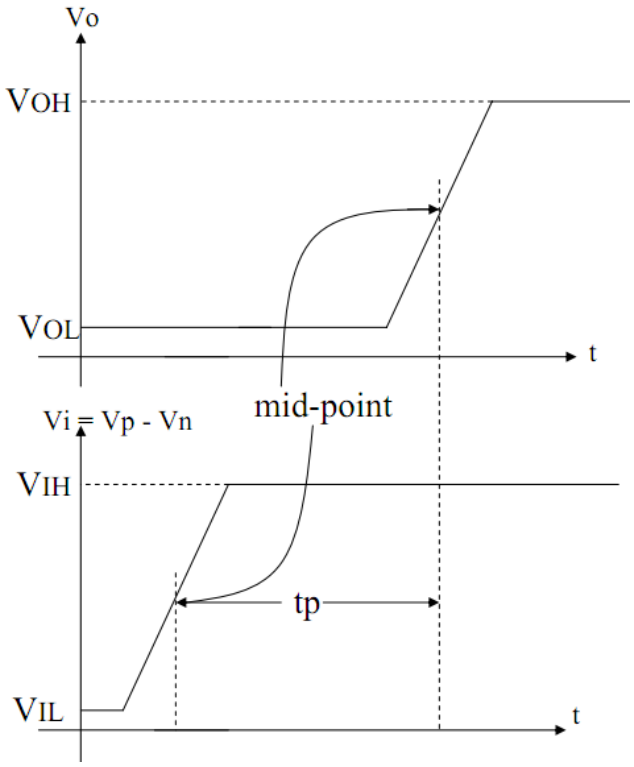


Figure 3.3: Propagation Delay Time of Comparator.

Propagation delay can be defined as at how much speed the amplifier responds with applied input. Simply speaking propagation delay is the delay between output and input. Figure 3.3 shows the propagation time delay characteristics of comparator. It can be calculated as:

Propagation time delay= (Rising Propagation Delay time +
Falling Propagation Delay Time) /2

3.2.2 Slew Rate:

Slew rate can be defined as the rate of change of output voltage with respect to time.

$$SR= dV_{out}/dt$$

If the rate of rise or fall of a comparator becomes large, the dynamics may be limited by

the slew rate.Slew rate comes from the relationship,

$$I=C\ dV/dt$$

where I is the current through a capacitor and V is the voltage across it.

If the current becomes limited, then the voltage rate becomes limited. Therefore for a comparator that is slew rate limited we have,

$$tp = \Delta T= \Delta V/SR = (VOH- VOL)/ 2\cdot SR$$

where SR= slew rate of the comparator.

CHAPTER 4

ANALYSIS OF THE COMPARATORS

Table 1: Input Specifications

Supply voltage (VDD)	1V
TECHNOLOGY	CADENCE GPDK 90 nm
INPUT VOLTAGE RANGE	0V-0.9V
CLOCK FREQUENCY	250 KHz
CLOCK RISE TIME	100 ps
CLOCK FALL TIME	100 ps
CLOCK DELAY	1 ns
CLOCK PULSE WIDTH	2 ns
TEMPARATURE	27 ◦C
REFERENCE VOLTAGE	0.2V-0.7V

Table 2: Transistor Dimensions (µm)

	[1]		[3]		[4]		[5]		PROPOSED COMP.	
TRANSISTOR	W	L	W	L	W	L	W	L	W	L
M1	8	0.1	8	0.1	8	0.1	8	0.1	4	0.1
M2	4	0.1	4	0.1	4	0.1	4	0.1	4	0.1
M3	4	0.1	4	0.1	4	0.1	4	0.1	4	0.1
M4	X	X	2	0.1	2	0.1	2	0.1	2	0.1
M5	X	X	2	0.1	2	0.1	2	0.1	2	0.1
M6	X	X	X	X	2	0.1	2	0.1	2	0.1
M7	X	X	X	X	2	0.1	2	0.1	2	0.1
M8	2	0.1	2	0.1	2	0.1	2	0.1	1	0.1
M9	2	0.1	2	0.1	2	0.1	2	0.1	1	0.1
M10	2	0.1	4	0.1	4	0.1	2	0.1	0.5	0.1
M11	2	0.1	4	0.1	4	0.1	2	0.1	0.5	0.1
M12	2	0.1	2	0.1	2	0.1	4	0.1	0.5	0.1
M13	2	0.1	2	0.1	2	0.1	4	0.1	0.5	0.1
M14	4	0.1	4	0.1	4	0.1	4	0.1	4	0.1
M15	4	0.1	X	X	4	0.1	4	0.1	4	0.1
M16	X	X	0.18	0.1	4	0.1	0.18	0.1	0.18	0.1
M17	X	X	0.18	0.1	4	0.1	0.18	0.1	0.18	0.1
M18	X	X	X	X	X	X	0.18	0.1	0.18	0.1
M19	X	X	X	X	X	X	0.18	0.1	0.18	0.1
M20	X	X	X	X	X	X	X	X	1	0.1
M21	X	X	X	X	X	X	X	X	1	0.1

In this section we will analyze the existing comparators that were discussed in literature review. We will compare their advantages and disadvantages in respect of their speed, delay, power dissipation, slew rate and offset voltage. We are using Cadence Virtuoso® Analog Design Environment, Virtuoso® XL Layout Editing Software for analyzing the circuits.

4.1 Preamplifier Based Comparator:

4.1.1 Circuit Diagram:

Figure 4.1 shows the schematic (designed in Cadence) of the Preamplifier based comparator circuit. The supply voltage of this comparator is 1 V. Input voltage is .9 V and Reference voltage is .5 V. The temperature is 27˚C. The input specifications are specified in detail in Table 1.

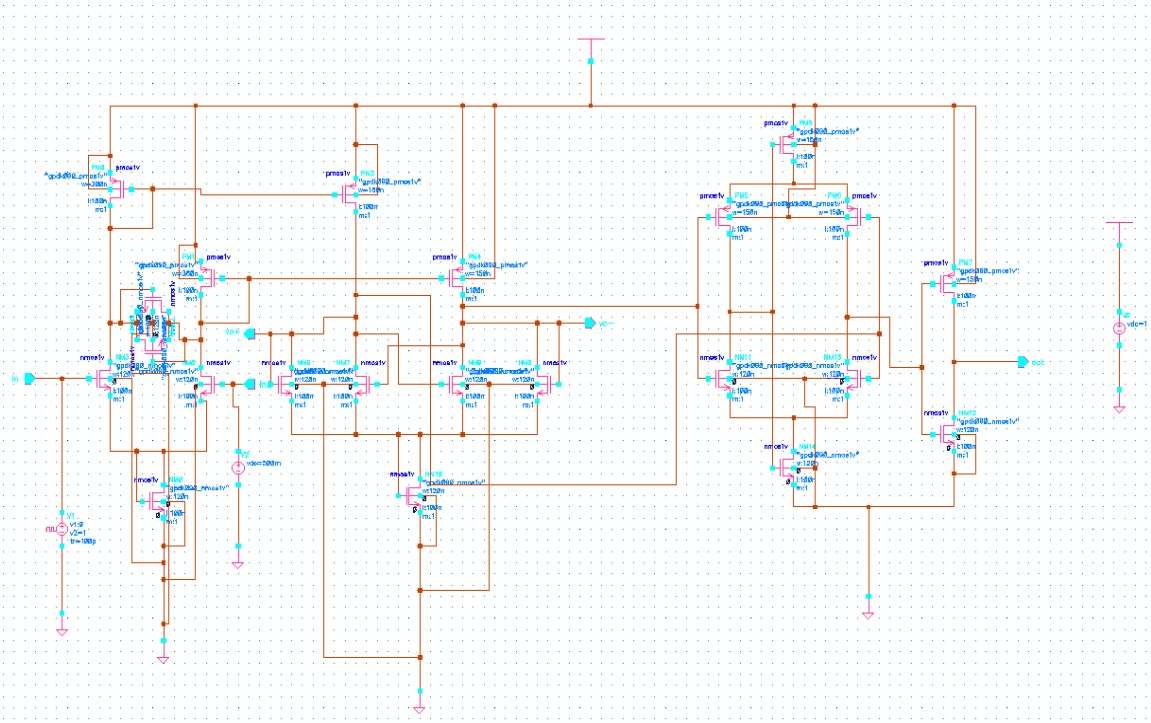


Figure 4.1: Preamplifier Based Comparator.

4.1.2 DC Analysis:

Figure 4.2 shows the DC analysis of the preamplifier based comparator. For calculating DC analysis, both input and reference voltage is taken as the DC voltage source. DC analysis states that the above comparator works perfectly. Back-to-back NMOS transistors in preamplifier stage keep the PMOS transistors in the preamplifier from turning off.

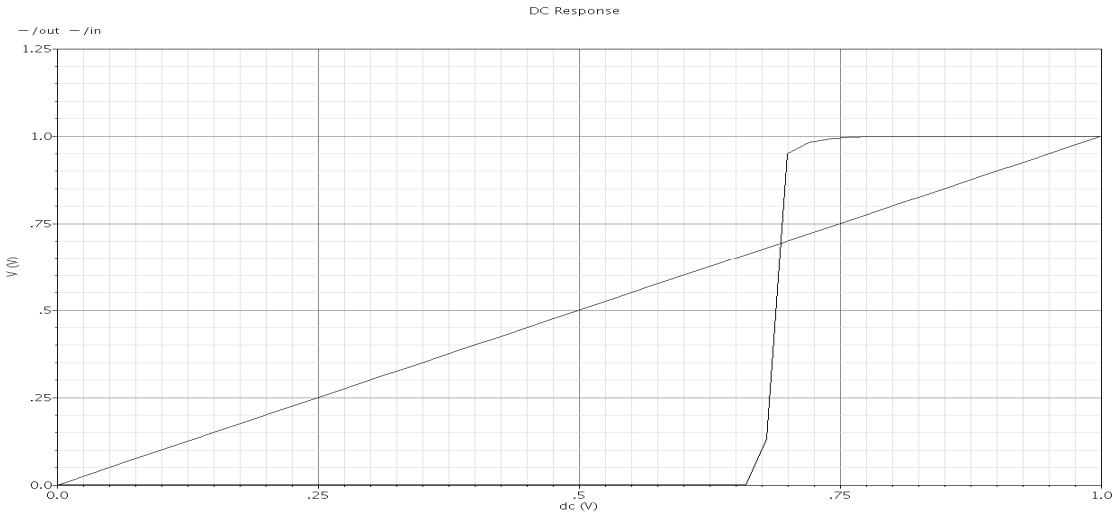


Figure 4.2 DC Response of the preamplifier based comparator.

4.1.3 Transient Analysis:

Figure 4.3 shows the Transient response of the above circuit. For calculating transient response a PULSE voltage source is used as input voltage source and reference voltage source is a DC voltage source.

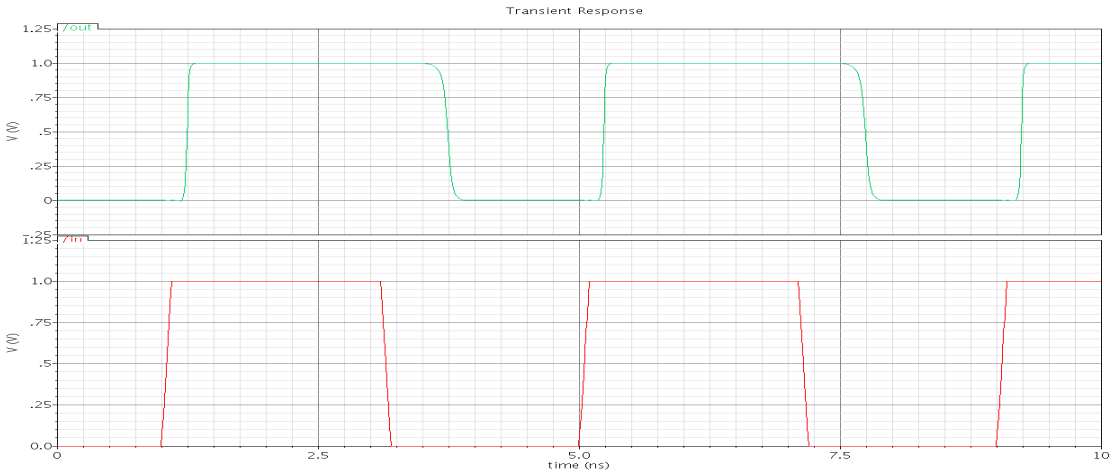


Figure 4.3 Transient response of the circuit.

4.1.4 Results:

Offset Voltage: 64.35 mV

Static Power Dissipation: 10.89 µW

Dynamic Power Dissipation: 72.56 µW

Delay: .3935 nS

Speed: 2.54 GHz

Slew Rate: 21.23 V/nS

4.2 Latch Type Voltage Sense Amplifier:

4.2.1 Circuit Diagram:

Figure 4.4 shows the Circuit Diagram (designed in Cadence) of Latch type voltage sense amplifier. Specifications are given in Table 1. Transistor sizes are specified in Table 2. The circuit comprises of a latch stage followed by buffer stage (which is nothing but a self-biased differential amplifier followed by an inverter).

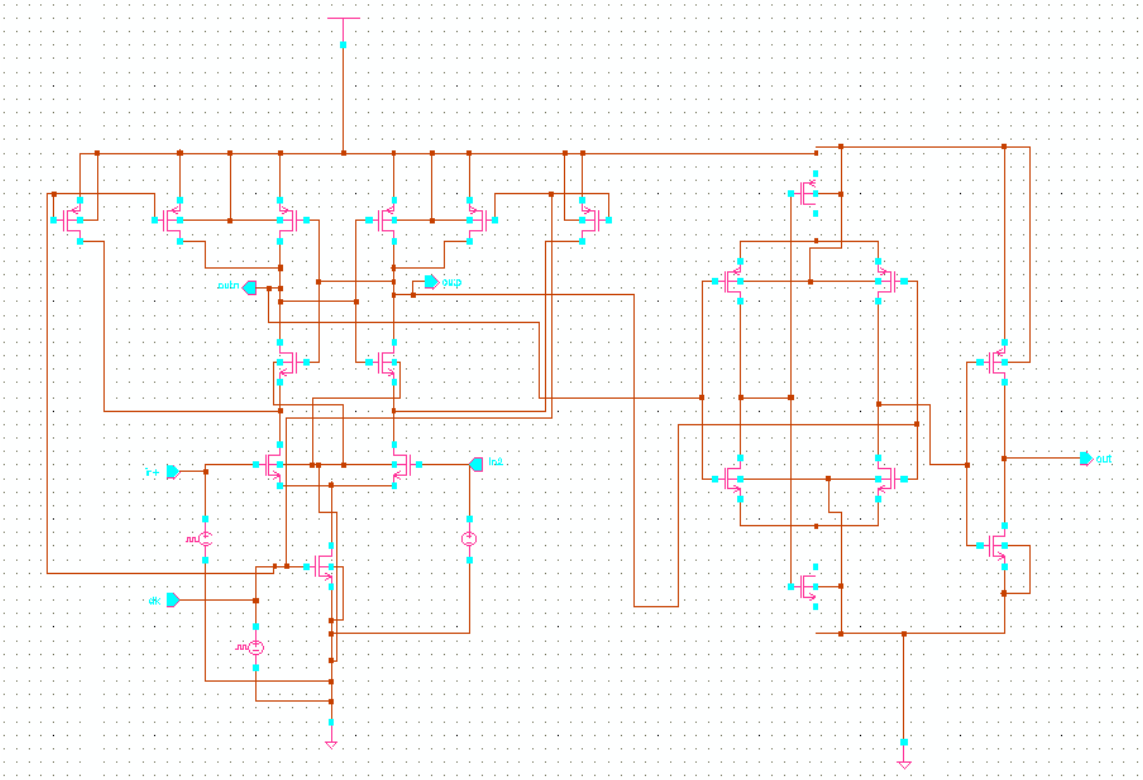


Figure 4.4 Circuit Diagram of Latch Type Voltage Sense Amplifier.

4.2.2 DC analysis:

Figure 4.5 shows the DC analysis of the circuit. From Figure 4.5, we can say that the comparator is working fine. Input voltage is swept from -1V to +1V and reference voltage is taken as .2 V.

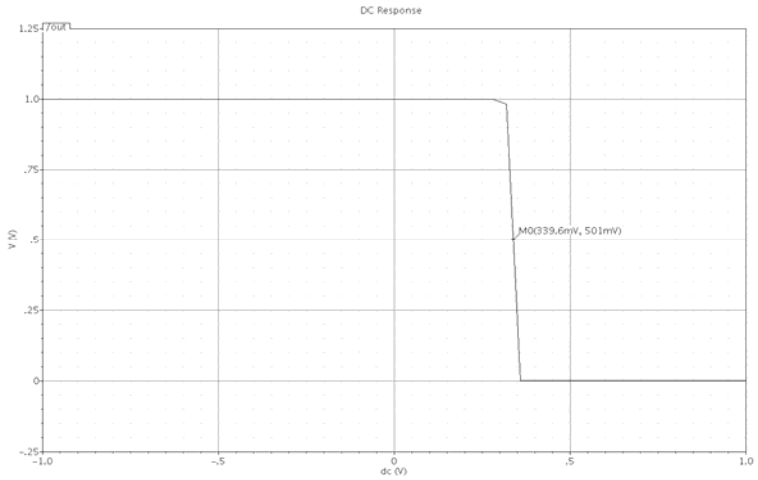


Figure 4.5 DC analysis of the circuit.

4.2.3 Transient Analysis:

Figure 4.6 shows the transient response of the circuit. From transient response we can conclude that output of *outp(as well as outn node)* node which acts as an one of the input of the output buffer stage (which is mainly comprises of a self-biased differential amplifier followed by an inverter) is distorted by the noise present in the comparator.

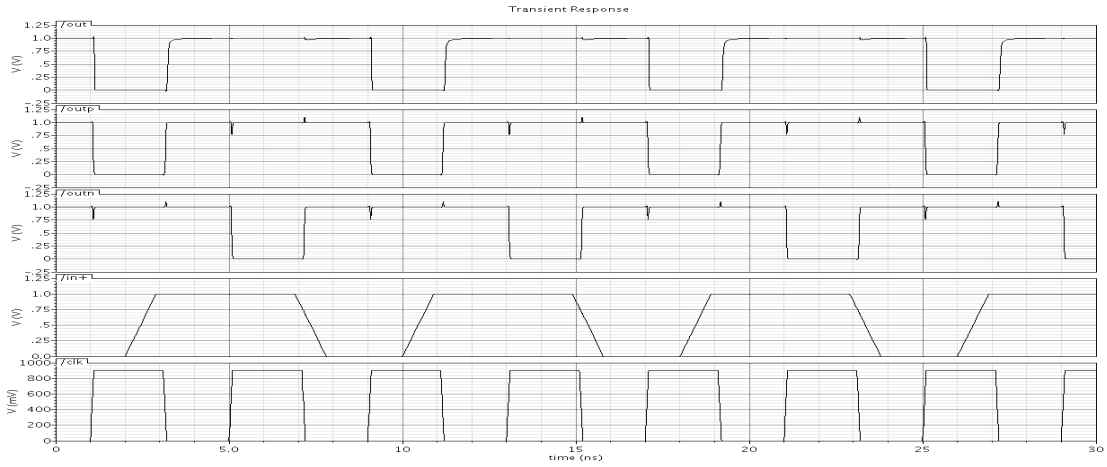


Figure 4.6 Transient response of the circuit.

4.2.4 Results:

Before Layout Simulation:

Offset Voltage: 339.6 mV

Dynamic Power Dissipation: 14.84 µW

Delay: 1.247 nS

Speed: .802 GHz

Slew Rate: 11.08 V/nS

After Post Layout Simulation:

Dynamic Power Dissipation: 16 µW

Delay: 1.35 nS

Speed: .735 GHz

Slew Rate: 18.27 V/nS

4.3 Double Tail Latch Type Voltage Sense Amplifier:

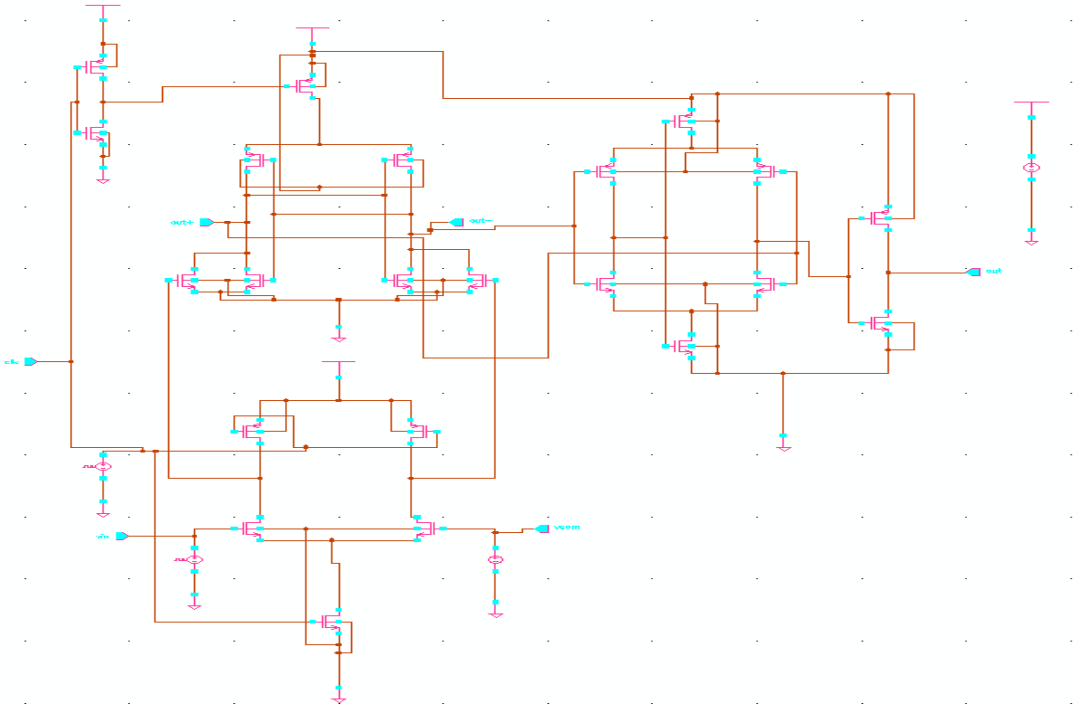


Figure 4.7 Circuit Diagram of Double Tail Latch Type Voltage Sense Amplifier.

4.3.1 Circuit Diagram:

Figure 4.7 shows the Circuit Diagram (designed in Cadence) of Double tail latch type voltage sense amplifier. Specifications are given in Table 1. Transistor sizes are specified in Table 2.This circuit also comprises of latch stage followed by buffer stage.

4.3.2 DC Analysis:

Figure 4.8 shows the DC Analysis graph of the circuit. Input voltage is taken as 1 V and swept from -1V to +1V. Reference Voltage is taken as .2V. From the graph we can

conclude that the comparator is working fine.

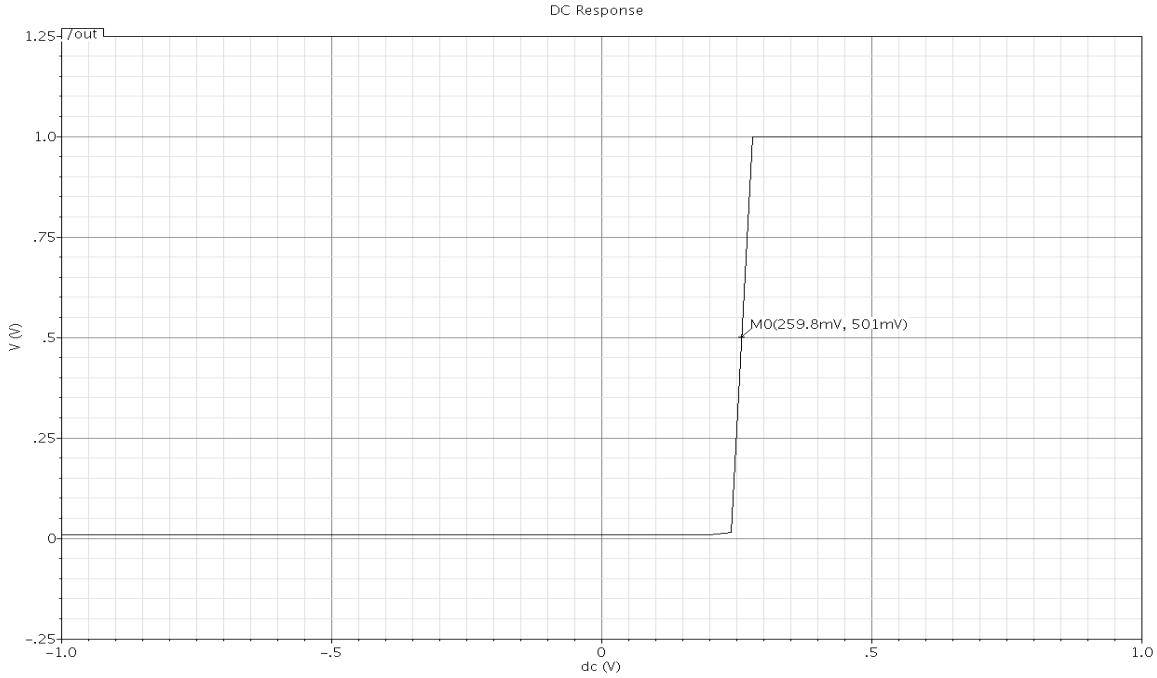


Figure 4.8 DC analysis of comparator.

4.3.3 Transient Analysis:

Figure 4.9 shows the transient analysis of the circuit. From this analysis we can say that the output of *out+* node in latch stage is affected by noise and fluctuating with the clock transition as that was in the previous comparator. For the transient analysis we have taken pulse voltage source as Input stage and a dc voltage source as reference node.

Figure 4.9 Transient Analysis of the comparator.

4.3.4 Results:

Before Layout Simulation:

Offset Voltage: 259.8 mV

Dynamic Power Dissipation: 127.9 µW

Delay: 1.745 nS

Speed: .573 GHz

Slew Rate: 39.85 V/nS

After Post Layout Simulation:

Dynamic Power Dissipation: 145.07 µW

Delay: 2.52 nS

Speed: .390 GHz

Slew Rate: 2.16 V/nS

4.4 Dynamic Comparator without Calibration:

4.4.1 Circuit Diagram:

Figure 4.10 shows the Dynamic Comparator without Calibration (Designed in Cadence). This figure also consists of a latch followed by a output buffer stage. Specifications are given in Table 1. Transistor sizes are specified in Table 2.

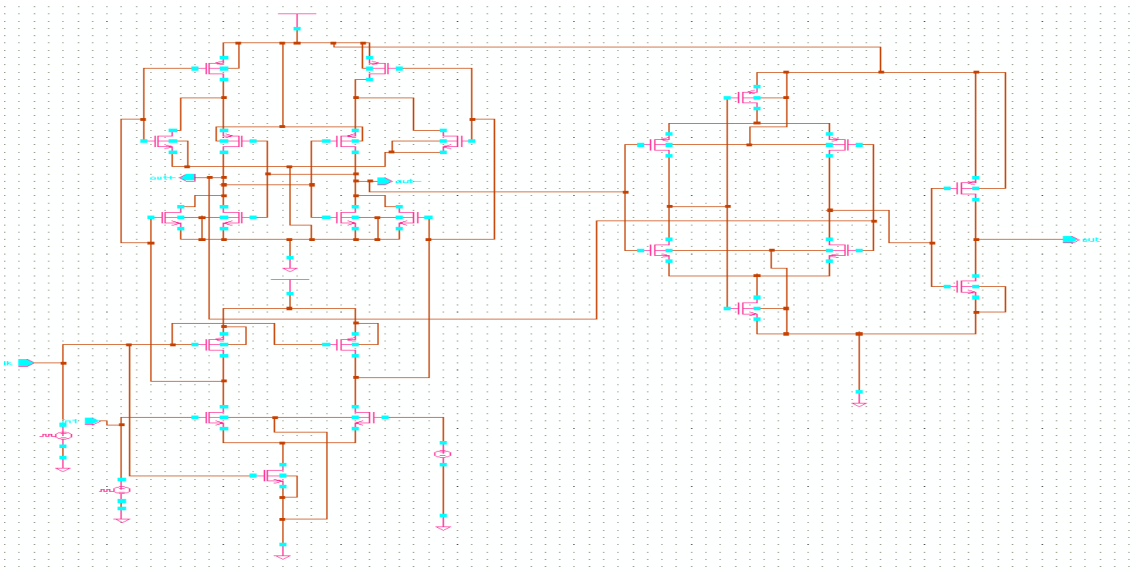


Figure 4.10 Figure of Dynamic Comparator without Calibration.

4.4.2 DC Analysis:

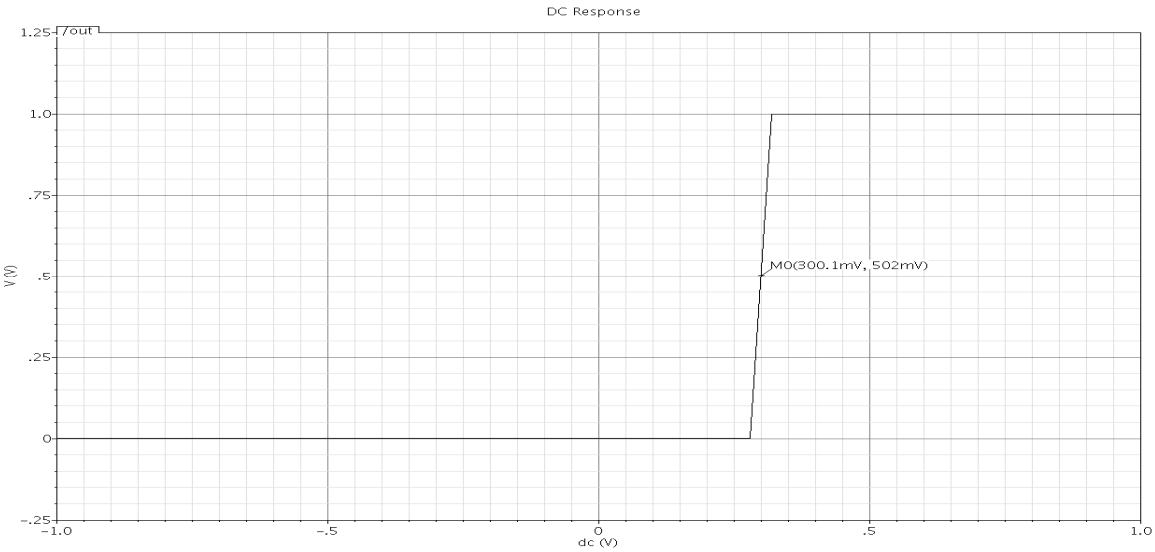


Figure 4.11 DC Analysis of Comparator.

Figure 4.11 shows the DC response of the circuit. Input voltage is taken as 1 V and swept from -1V to +1V. Reference Voltage is taken as .4V. From the graph we can conclude that

the comparator is working fine.

4.4.3 Transient Analysis:

Figure 4.12 shows the transient analysis of the circuit. From this analysis we can say that the output of *out+* node in latch stage is affected by noise and fluctuating with the clock transition as that was in the previous comparator. For the transient analysis we have taken pulse voltage source as Input stage and a dc voltage source as reference node.

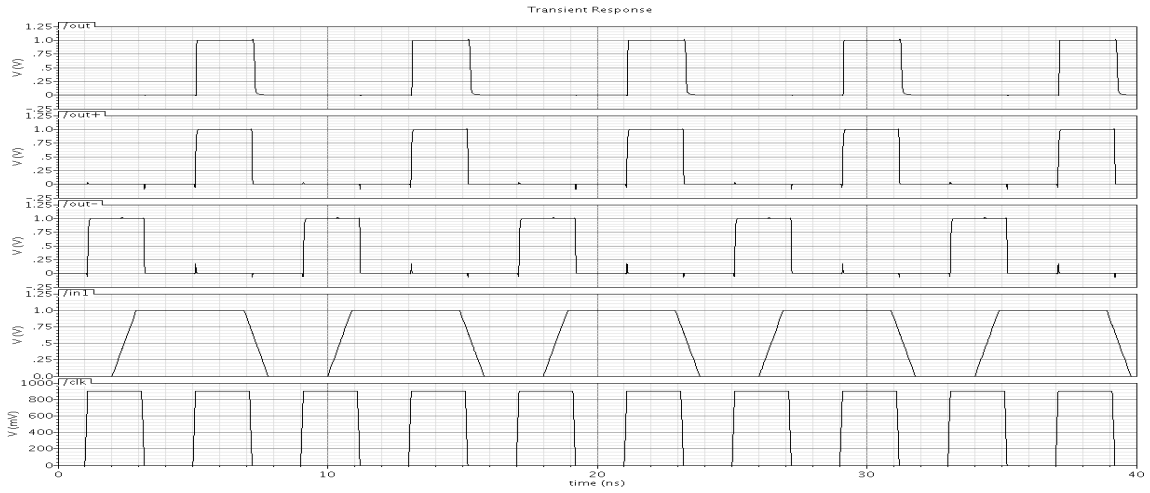


Figure 4.12 Transient Response of Comparator.

4.4.4 Results:

Before Layout Simulation:

Offset Voltage: 300.1 mV

Dynamic Power Dissipation: 105.33 µW

Delay: .61 nS

Speed: 1.639 GHz

Slew Rate: 3.09 V/nS

After Post Layout Simulation:

Dynamic Power Dissipation: 110 µW

Delay: 1.95 nS

Speed: .570 GHz

Slew Rate: 16.37 V/nS

4.5 Double-Tail Dual-Rail Dynamic Latched Comparator:

4.5.1 Circuit Diagram:

Figure 4.13 shows the schematic diagram of the Dynamic Comparator without Calibration (designed in Cadence). This circuit also comprises of latch stage followed by buffer stage. Specifications are given in Table 1. Transistor sizes are specified in Table 2.

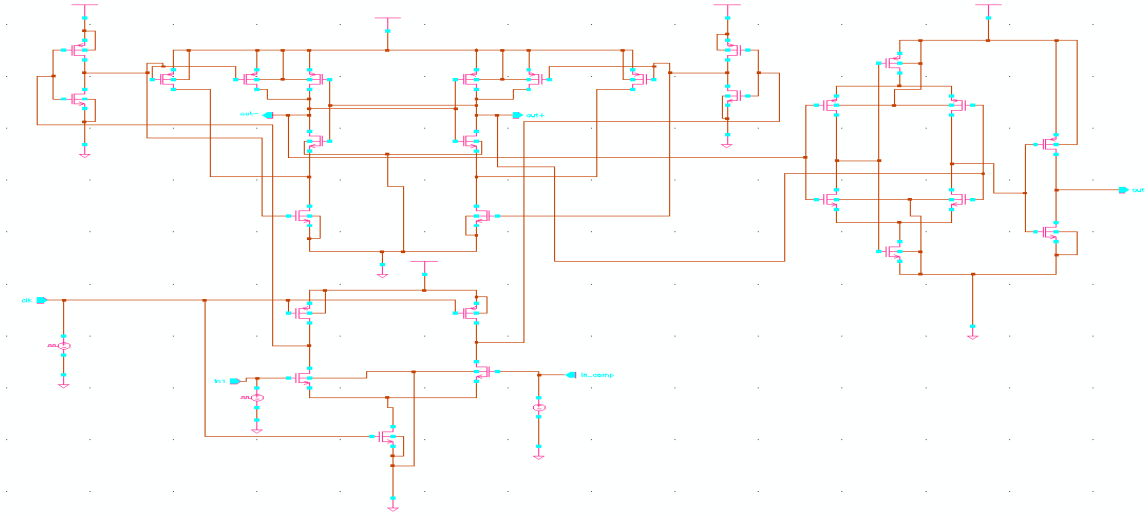


Figure 4.13 Schematic Diagram of Double-Tail Dual-Rail Dynamic Latched Comparator.

4.5.2 DC Characteristics:

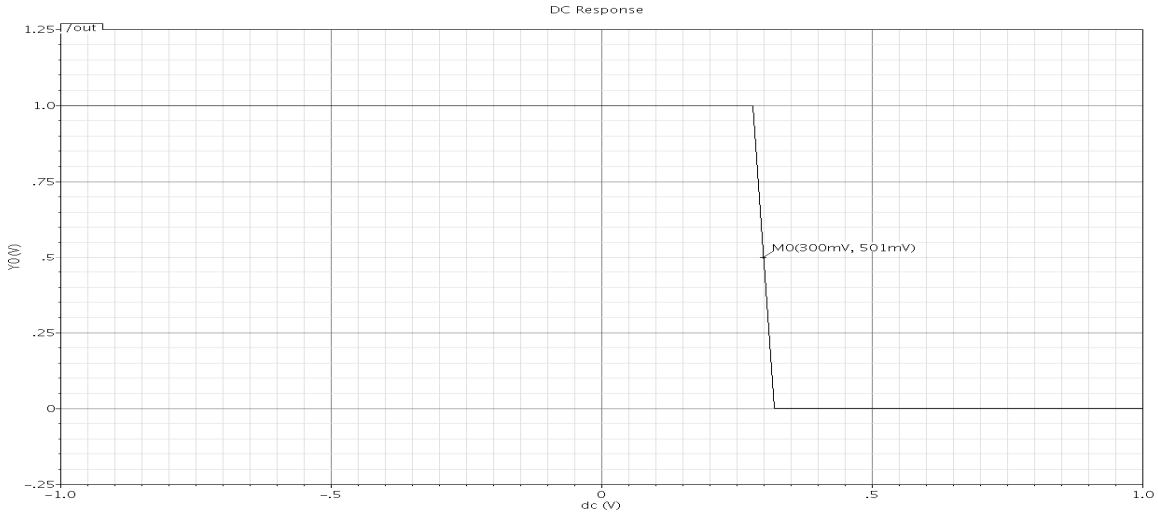


Figure 4.14 DC Characteristics of the Comparator.

Figure 4.14 shows the DC response of the circuit. Input voltage is taken as 1 V and swept from -1V to +1V. Reference Voltage is taken as .4V. From the graph we can

conclude that the comparator is working fine.

4.5.3 Transient Analysis:

Figure 4.15 shows the transient analysis of the circuit. From this analysis we can say that the output of *out+* node in latch stage is affected by noise and fluctuating with the clock transition as that was in the previous comparator. For the transient analysis we have taken pulse voltage source as Input stage and a dc voltage source as reference node.

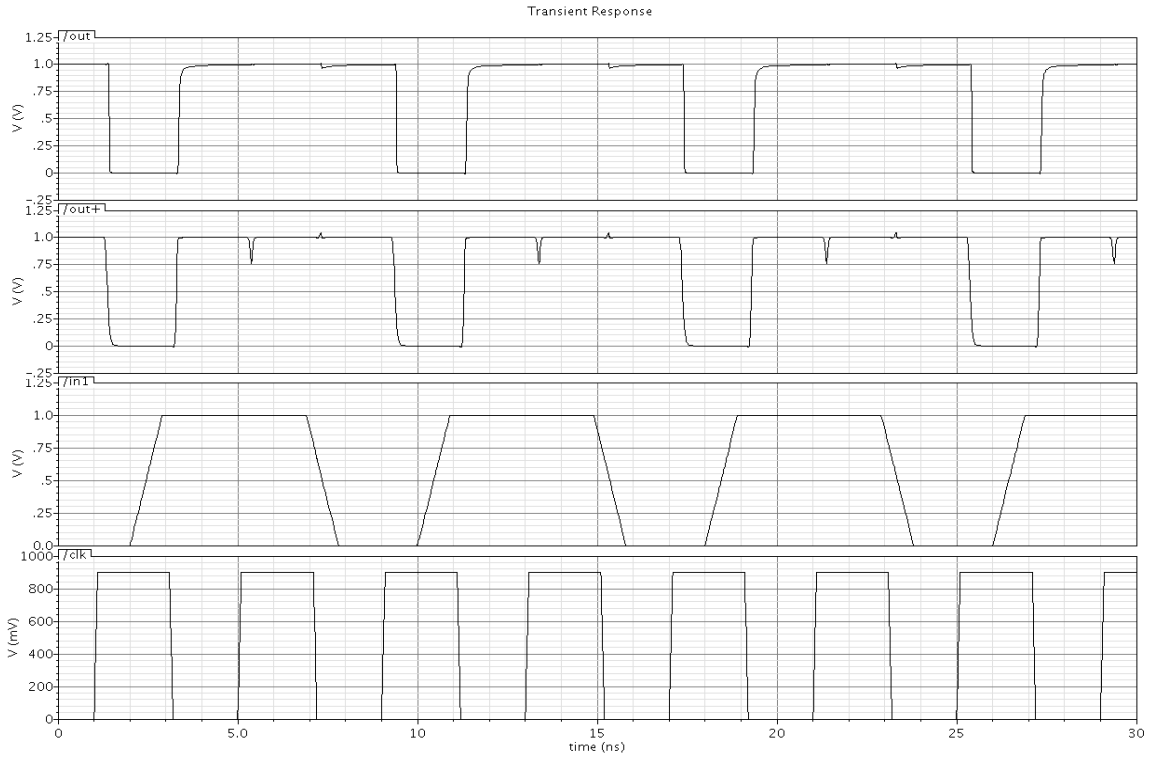


Figure 4.15 Transient Response of the Comparator.

4.5.4 Results:

Before Layout Simulation:

Offset Voltage: mV

Dynamic Power Dissipation: 57.37 µW

Delay: 1.49 nS

Speed: .671 GHz

Slew Rate: 10.77 V/nS

After Post Layout Simulation:

Dynamic Power Dissipation: 65 µW

Delay: 2.15 nS

Speed: .460 GHz

Slew Rate: 11.07 V/nS

4.6 Result Summary:

Table 3: Result Summary before layout:

COMPARATORS	*Transistor Count*	*Offset Voltage (mV)*	*Power Dissipation (µW)*	*Delay (nS)*	*Speed (GHz)*	*Slew Rate (V/nS)*
Preamplifier Based Comparator	*22*	*64.35*	*83.45*	*0.393*	*2.54*	*21.23*
Latch Type Voltage Sense Amplifier	*19*	*339.6*	*14.84*	*1.247*	*0.802*	*11.08*
Double Tail Latch Type Voltage SA	*22*	*259.8*	*127.9*	*1.745*	*0.573*	*39.85*
Dynamic Comparator without Calibration	*23*	*300.1*	*105.33*	*0.61*	*1.639*	*3.09*
Double Tail Dual Rail Dynamic Latched Comp.	*27*	*300*	*57.37*	*1.49*	*0.671*	*10.77*

Table 4: Result Summary after Post Layout Simulation:

COMPARATORS	*Power Dissipation (μW)*	*Delay (nS)*	*Speed (GHz)*	*Slew Rate (V/nS)*	*Area (μm^2)*
Latch Type Voltage Sense Amplifier	*16*	*1.35*	*0.735*	*18.27*	*349.08*
Double Tail Latch Type Voltage SA	*145.07*	*2.52*	*0.390*	*2.16*	*86.24*
Dynamic Comparator without Calibration	*110*	*1.95*	*0.510*	*16.37*	*124.23*
Double Tail Dual Rail Dynamic Latched Comp.	*65*	*2.15*	*0.460*	*11.07*	*110.24*

4.7 Conclusion:

Preamplifier based comparators; Dynamic comparators are simulated in Cadence® Analog Design Environment using gpdk 90nm technology. The results are compared and given in Table 3 and 4. The main problem with all these comparators is the output signal of the latch stage is fluctuating during clock transition. This is happening due to the presence of noise in input terminals. Now here we have to design a circuit which removes the noise from the output and dissipates less power and provides high speed. Keeping these things in mind we have designed a new differential amplifier based comparator which is described in the next chapter.

CHAPTER 5

PROPOSED COMPARATOR: ANALYSIS AND SIMULATION

5.1 Circuit Diagram:

Circuit Diagram of Proposed Comparator is shown in Figure 5.1. This circuit mainly is a derived version of the [5]. The back-to-back latch stage is replaced with back-to-back dual-input single output differential amplifier. Differential amplifier has so many advantages over the conventional latch which nothing but an inverter. It has higher immunity to environmental noise.and it rejects common mode noise or in other words it has better CMRR. Another property of differential signaling is the increase in maximum achievable voltage swings. It also provides simpler biasing and higher linearity. Here our main purpose is to eliminating the noise that is present in the latch stage and for which output is getting fluctuated with clock transition.

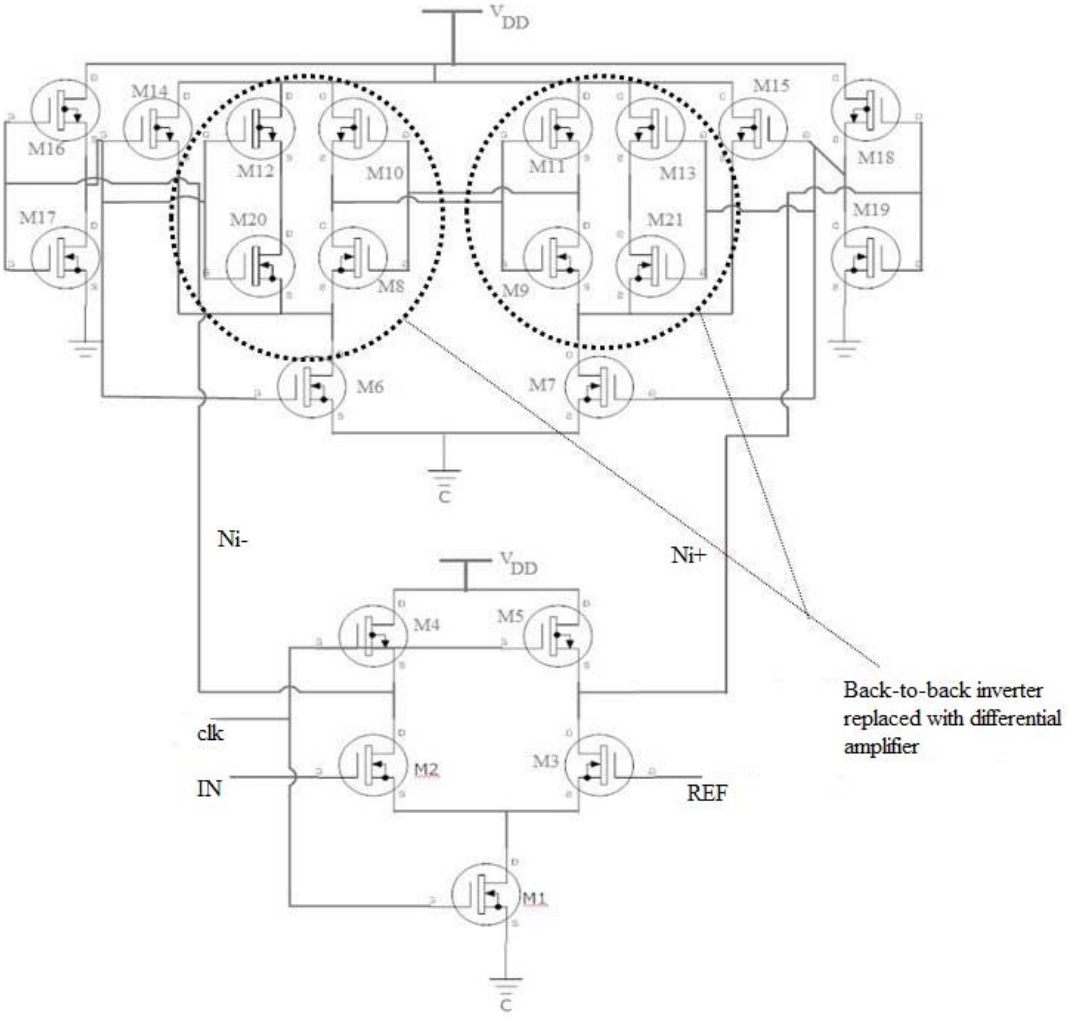


Figure 5.1: Schematic of the Proposed Comparator

5.2 Operation:

During reset phase (clk= 0V), PMOS transistor M4 and M5 turn on and they charge Ni node voltages to V_{DD}. And Hence NMOS transistors M17 and M19 turns on and discharges Ni' nodes voltages to GND. Then M14, M15 and PMOS transistors of differential amplifier blocks M12 and M13 turns on, NMOS transistors of differential amplifier block M8, M9 and M6, M7 turns off. The out nodes are charges to V_{DD}.

During evaluation phase (clk= V_{DD}), the Ni node capacitances are discharged from V_{DD} to GND in a rate which is proportional to the input voltages. At a certain voltage of Ni nodes, the inverter pairs M16/M17 and M18/M19 invert the Ni node signal into a regenerated signal. These regenerated signals turn PMOS transistors M14, M12, M13, and M15 off. And eventually M6, M7, M20, M21 turns on. Hence the back-to-back differential pair again regenerates the Ni' node signals and because of M6 and M7 being on, the output latch stage converts the small voltage difference transmitted from Ni' node into a full scale digital level output.

5.3 Analysis of Proposed Comparator:

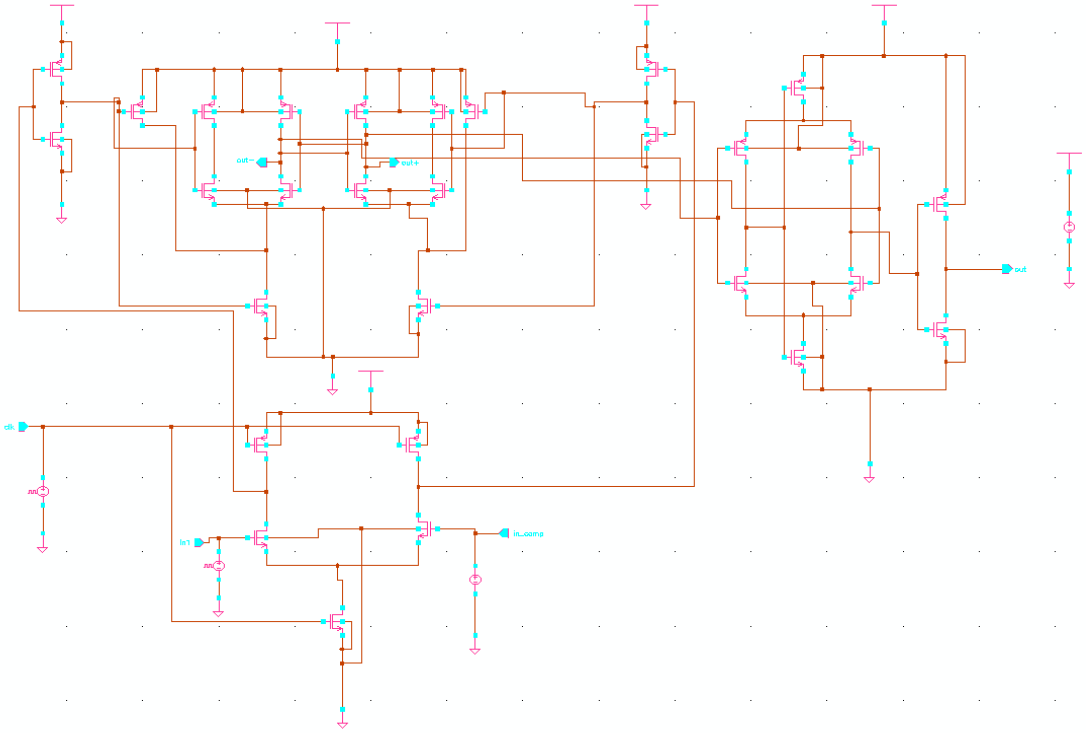


Figure 5.2 Schematic of the proposed comparator.

The circuit diagram drawn in Cadence® Virtuoso Analog Design Environment is shown in Figure 5.2. Figure 5.3 shows the DC response of the circuit. Figure 5.3 shows the transient response of the circuit. From transient response curve, it is confirmed that out+ node voltage does not get distorted during clock transition and it works fully fine. The supply voltage for DC analysis is taken as 1V and input is varied from -1V to +1 V. Reference voltage is taken as .5 V.

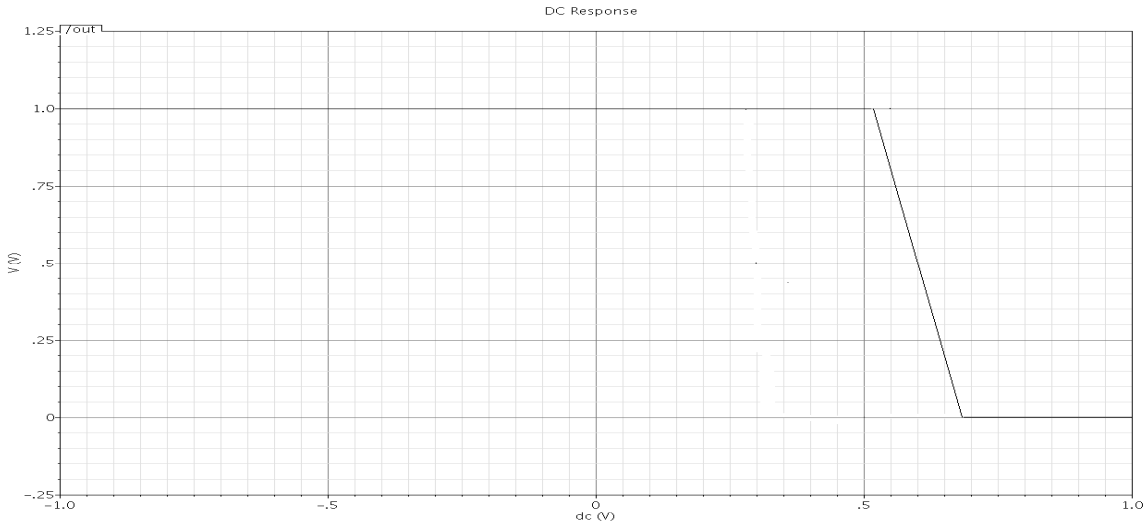


Figure 5.3 DC response of the Proposed Comparator.

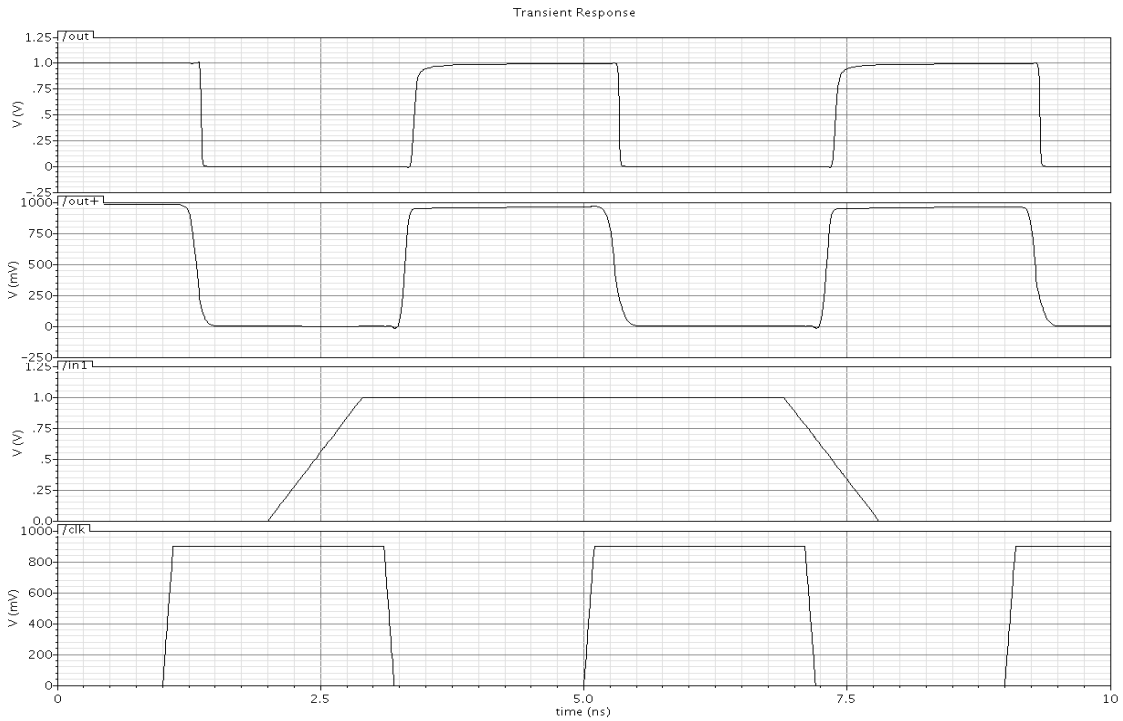


Figure 5.4: Transient Response.

Figure 5.4 shows the transient response of the circuit. Input specifications are mentioned in Table 1. Table 2 shows the sizes of the transistors. From transient response it is evident that the output of the buffer stage and the output of the out+ node are almost equal which was not seen in the previous comparators either.

CHAPTER 6

RESULTS AND DISCUSSION

6.1 Results and Discussions:

To compare the performance of the proposed comparators with previous works, each circuit was simulated in Cadence® virtuoso analog design environment. Technology used is gpdk 90nm technology with V_{DD}=1V as supply voltage. The layout diagrams and RC extracted diagrams has given in Appendix B. Table 5 shows the result summary before post layout simulation. Table 6 shows the result summary after post layout simulation. From table 5 we can say that though proposed comparator have highest transistor count but it still consumes less power than [2], [3], [4], [5]. We can also say that from Table 5, the speed is improved with respect to [5]. from Table 6, we can say that the power dissipation of proposed comparator, after post layout simulation is increased by 31% but it is still less than [5]. After post layout simulation the speed of proposed comparator is decreased from 0.910 GHz to .485 GHz but is still better than that of [5].

Table 5: Result summary before layout

COMPARATORS	***Transistor Count***	***Offset Voltage (mV)***	***Power Dissipation (µW)***	***Delay (nS)***	***Speed (GHz)***	***Slew Rate (V/nS)***
Preamplifier Based Comparator [11]	*22*	*64.35*	*83.45*	*0.393*	*2.54*	*21.23*
Latch Type Voltage Sense Amplifier [2]	*19*	*339.6*	*14.84*	*1.247*	*0.802*	*11.08*
Double Tail Latch Type Voltage SA[3]	*22*	*259.8*	*127.9*	*1.745*	*0.573*	*39.85*
Dynamic Comparator without Calibration [4]	*23*	*300.1*	*105.33*	*0.61*	*1.639*	*3.09*
Double Tail Dual Rail Dynamic Latched Comp.[5]	*27*	*300*	*57.37*	*1.49*	*0.671*	*10.77*
Proposed Comparator	***29***	***300***	***44***	***1.1***	***0.910***	***10.26***

Table 6: Result Summary after Post Layout Simulation

COMPARATORS	*Power Dissipation (µW)*	*Delay (nS)*	*Speed (GHz)*	*Slew Rate (V/nS)*	*Area (μm^2)*
Latch Type Voltage Sense Amplifier[2]	*16*	*1.35*	*0.735*	*18.27*	*84.28*
Double Tail Latch Type Voltage SA[3]	*145.07*	*2.52*	*0.390*	*2.16*	*86.24*
Dynamic Comparator without Calibration[4]	*110*	*1.95*	*0.510*	*16.37*	*124.23*
Double Tail Dual Rail Dynamic Latched Comp.[5]	*65*	*2.15*	*0.460*	*11.07*	*110.24*
Proposed Comparator	***58.25***	***2.06***	***0.485***	***8.95***	***130.42***

Table 7: Comparison of Results before Layout and After Post Layout Simulation

Performance Metrices	***Latch Type Voltage SA***		***Double Tail Latch Type Voltage SA***		***Dynamic Comparator without Calibration***		***Double-Tail Dual-Rail Dynamic Latched Comparator***		***Proposed Comparator***	
	Before Layout	***After Post Layout Simulation***	***Before Layout***	***After Post Layout Simulation***	***Before Layout***	***After Post Layout Simulation***	***Before Layout***	***After Post Layout Simulation***	***Before Layout***	***After Post Layout Simulation***
Power Dissipation (µW)	*14.84*	*16*	*127.9*	*145.07*	*105.33*	*110*	*57.37*	*65*	*44*	*58*
Delay (nS)	*1.247*	*1.35*	*1.745*	*2.52*	*0.61*	*1.95*	*1.49*	*2.15*	*1.1*	*2.06*
Speed (GHz)	*0.802*	*0.735*	*0.573*	*0.39*	*1.639*	*0.51*	*0.671*	*0.46*	*0.91*	*0.485*
Slew Rate (V/nS)	*11.08*	*18.27*	*39.85*	*2.16*	*3.09*	*16.37*	*10.77*	*11.07*	*10.26*	*8.95*

CHAPTER 7

CONCLUSION AND FUTURE SCOPE

7.1 Conclusion:

A new dynamic comparator using positive feedback which shows better noise response, higher speed, lower power dissipation than the conventional dynamic latched comparators has been proposed & targeted for ADC application. The results are simulated in Cadence® Virtuoso Analog Design Environment with GPDK 90nm technology. In the proposed design, the back-to-back inverter is replaced with dual input single output differential amplifier in the latched stage. Output of the latch stage in the proposed design is not affected by noise. The noise present in the input and the clock is completely suppressed by the differential amplifiers present in the output latch stage. The proposed structure shows significantly lower power dissipation, higher speed compared to the dynamic comparators present in the literature. The transistor count in the proposed comparator is higher to an extent among all the comparators analyzed. After Post layout simulation the power dissipation of the comparator is increased by 31% and speed is decreased by 46% as compared to the simulation results that was achieved before layout. But still the comparator gives lesser power dissipation and higher speed than that of from which it was derived. The layouts and RC extracted files are given in Appendix A.

7.2 Scope for future work:

From simulation results, we can see that power dissipation is increased by 31% and speed is decreased to 46% than that of before post layout simulation, then the optimization in the circuit as well as the layout of the proposed comparator can be one topic. Furthermore searching of the suitable application can be another topic. Offset voltage after post layout simulation has not been analyzed. Offset voltage optimization can be another topic of interest.

REFRERENCES

[1] T. Kobayashi, K. Nogami, T. Shirotori and Y. Fujimoto, "A current-controlled latch sense amplifier and a static power-saving input buffer for low-power architecture," IEEE J. Solid-State Circuits, vol. 28, pp. 523-52, April 1993.

[2] B. Wicht, T. Nirschl, and D. Schmitt-Landsiedel, "Yield and speed optimization of a latch-type voltage sense amplifier", IEEE J. Solid-State Circuits, vol. 39, pp. 1148-1158, July 2004.

[3] D. Schinkel, E. Mensink, E. Kiumperink, E. van Tuijl and B. Nauta, "A Double-Tail Latch-Type Voltage Sense Amplifier with 18ps Setup+Hold Time," ISSCC Dig. Tech. Papers, pp. 314-315 and 605, Feb. 2007.

[4] M. Miyahara, Y. Asada, P. Daehwa and A. Matsuzawa, "A Low-Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs," in Proc. A-SSCC, pp. 269-272, Nov. 2008.

[5] H.J. Jeon, Y.B. Kim, "A Low-offset High-speed Double-tail Dual-rail Dynamic Latched Comparator," ACM GLSVLSI'10(Great Lakes Symposium on VLSI), May 16-18, 2010

[6] Philip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design, 2nd ed., Oxford Indian Edition, 2006.

[7] Jun He, Sanyi Zhan, Degang Chen, and R.L. Geiger, "Analyses of Static and Dynamic Random Offset Voltages in Dynamic Comparators," IEEE Trans. Circuits Syst. I: Reg. Papers, vol. 56, pp. 911-919, May 2009.

[8] Nikoozadeh and B. Murmann, "An Analysis of Latch Comparator Offset Due to Load Capacitor Mismatch," IEEE Trans. Circuits Syst. II: Exp. Briefs, vol. 53, no. 12, pp. 1398-1402, Dec. 2006

[9] Pedro M.Figueiredo, Joao C.Vital, "Kickback Noise Reduction Techniques for CMOS Latched Comparator", IEEE Transactions on Circuits and Systems, vol.53, no.7, pp.541-545, July 2006.

[10] B. Murmann et al., "Impact of scaling on analog performance and associated modeling needs," IEEE Trans. Electron Devices, vol. 53, no. 9, pp. 2160-2167, Sep. 2006.

[11] R. Jacob Baker, Harry W. Li, David E. Boyce, "CMOS- Circuit Design, Layout, And Simulation", IEEE Press Series on Microelectronic Systems, IEEE Press, Prentice Hall of India Private Limited, Eastern Economy Edition,2002

[12] Meena Panchore, R.S. Gamad, "Low Power High Speed CMOS Comparator Design Using .18µm Technology", International Journal of Electronic Engineering Research, Vol.2, No.1, pp.71-77, 2010.

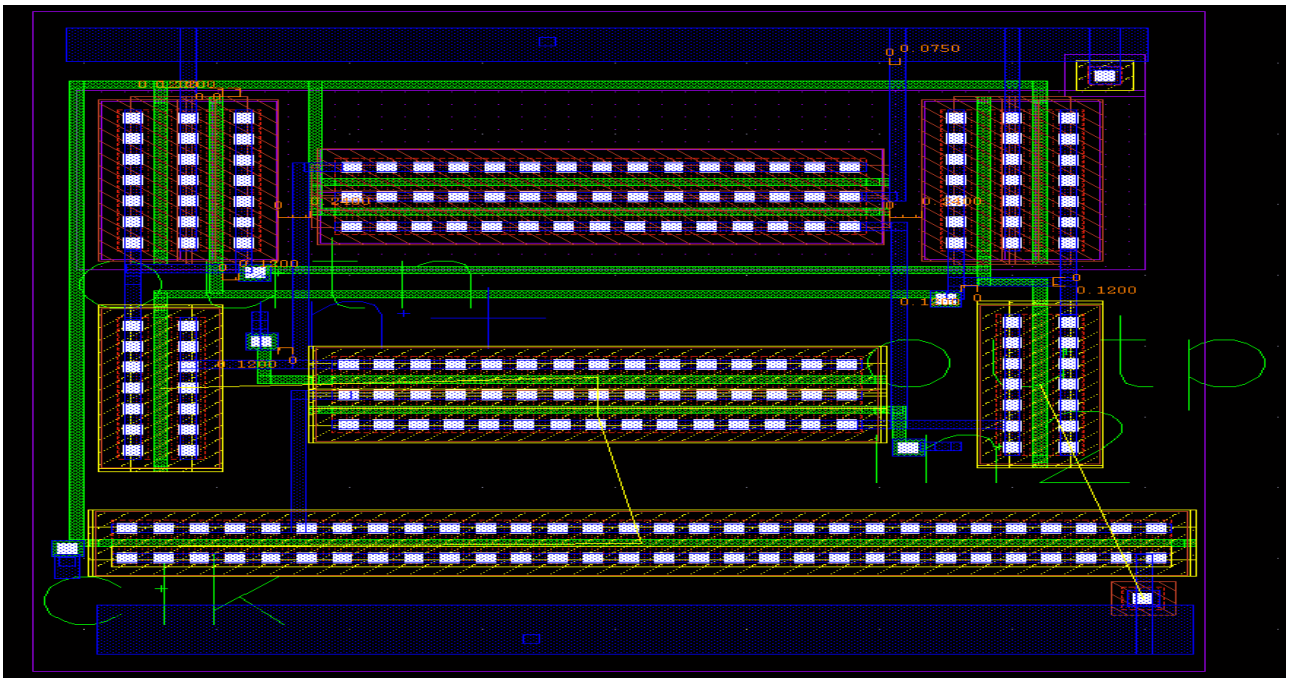
[13] M. van Elzakker, A.J.M. van Tuijl, P.F.J. Geraedts, D. Schinkel, E.A.M. Klumperink and B. Nauta, "A 1.9W 4.4fJ/Conversion-step 10b 1MS/s Charge-Redistribution ADC," ISSCC Dig. Tech. Papers, pp. 244–245, February 2008.
[14] S. Kale and R. S. Gamad, "Design of a CMOS Comparator for Low Power and High Speed" , Internationl Journal of Electronic Engineering Research, vol. 2, no. 1, pp. 29-34, 2010.
[15] Heungjun Jeon and Yong-Bin Kim, "A Novel Low-Power, Low-Offset and High-Speed CMOS Dynamic Latched Comparator", IEEE, 2010.
[16] Razavi Behzad, "Design of Analog CMOS Integrated Circuits", New York, NY: McGraw-Hill, Inc., 2000
[17] Sansen Willy M.C., Analog Design Essentials", Neatherlands, Springer International Edition, 2006.
[18] Dutta Ramen, "CMOS Voltage Comparator", Advanced VLSI Design Lab, IIT Kharagpur.[Online].Available:conf05.iitkgp.ac.in/avlsi/logf/summercourse/2008/comparator.pdf [Accessed: 14 March, 2011].
[19] Allen Phillip E., Short Course Notes on CMOS Analog IC Design. [Online]. Available: http://www.aicdesign.org/scnotes10.html [Accessed: February 12, 2011].
[20] Allen Phillip E., "Lecture-360- Characterization of Comparator". [Online]. Available:users.ece.gatech.edu/pallen/.../L360-Char_Comparators-2UP.pdf [Accessed 20 February, 2011].
[21] Johns D., Martin K., Analog Integrated Circuit Design, Wiley India Pvt. Ltd., 2008
[22] Cadence Online Documentation. Avilable: http://www.cadence.com

APPENDIX A:

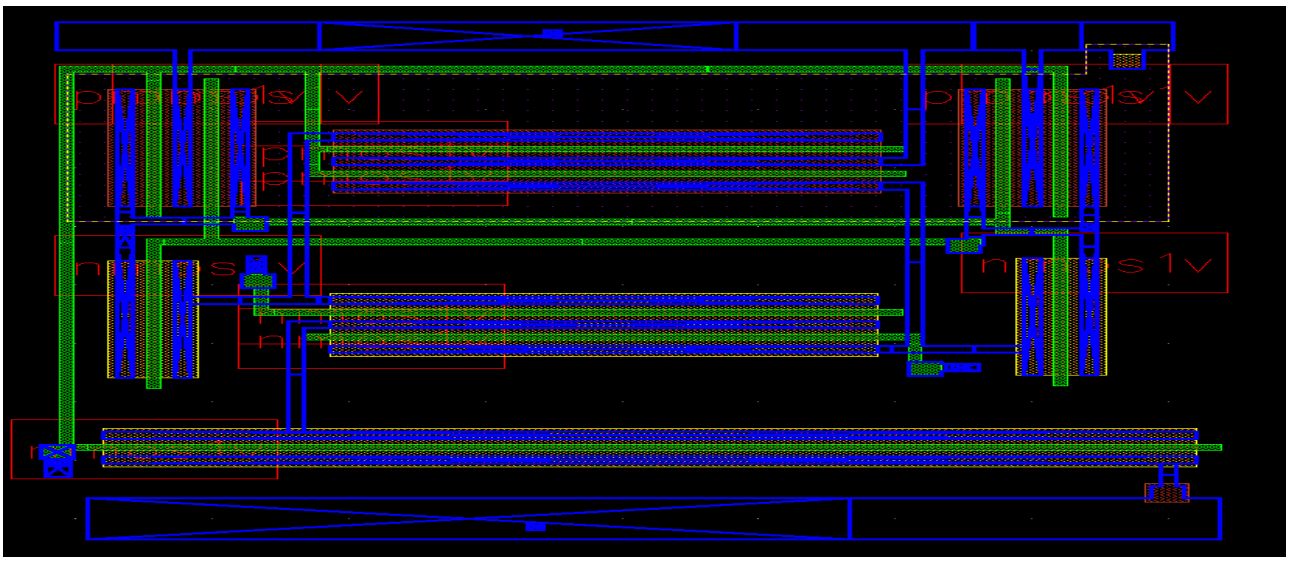
CIRCUIT LAYOUTS AND RC EXTRACTED DIAGRAMS

Latch Type Voltage Sense Amplifier

Layout:

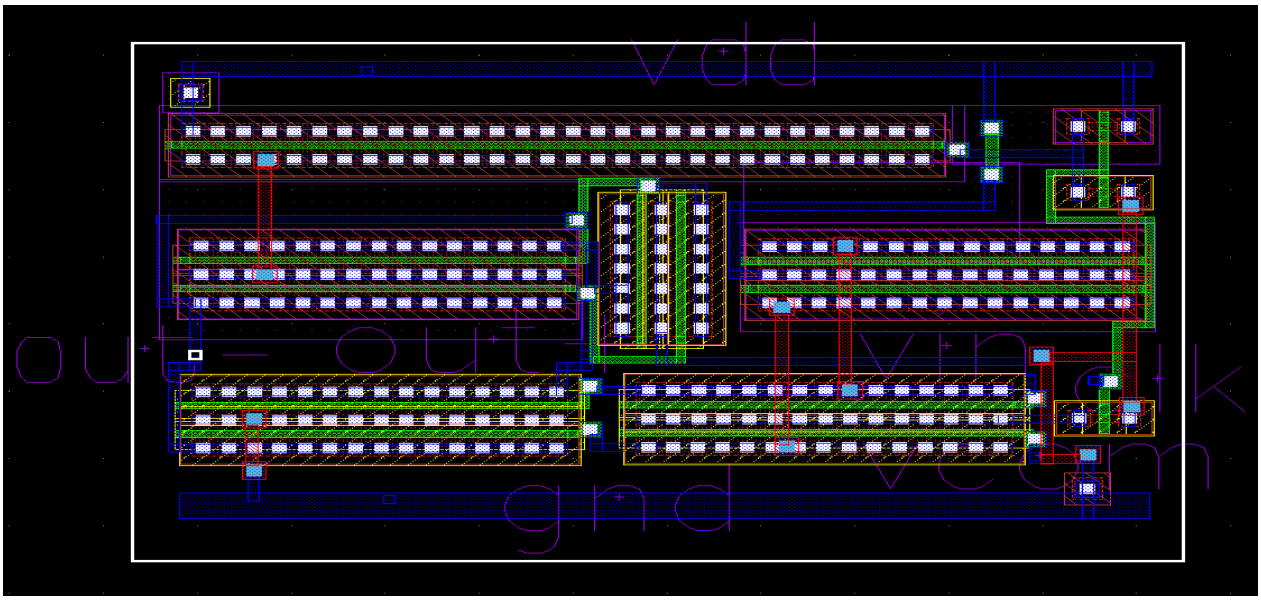


RC EXTRACTED:

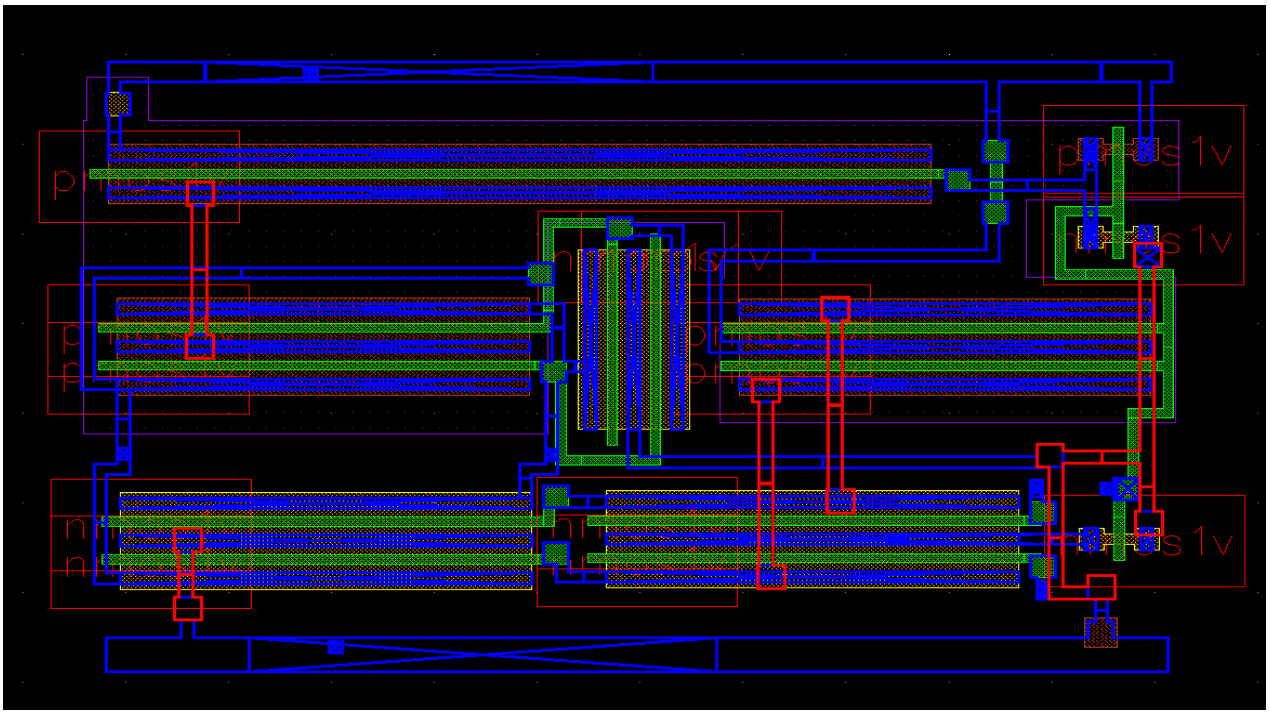


Double Tail Latch Type Voltage SA:

Layout:

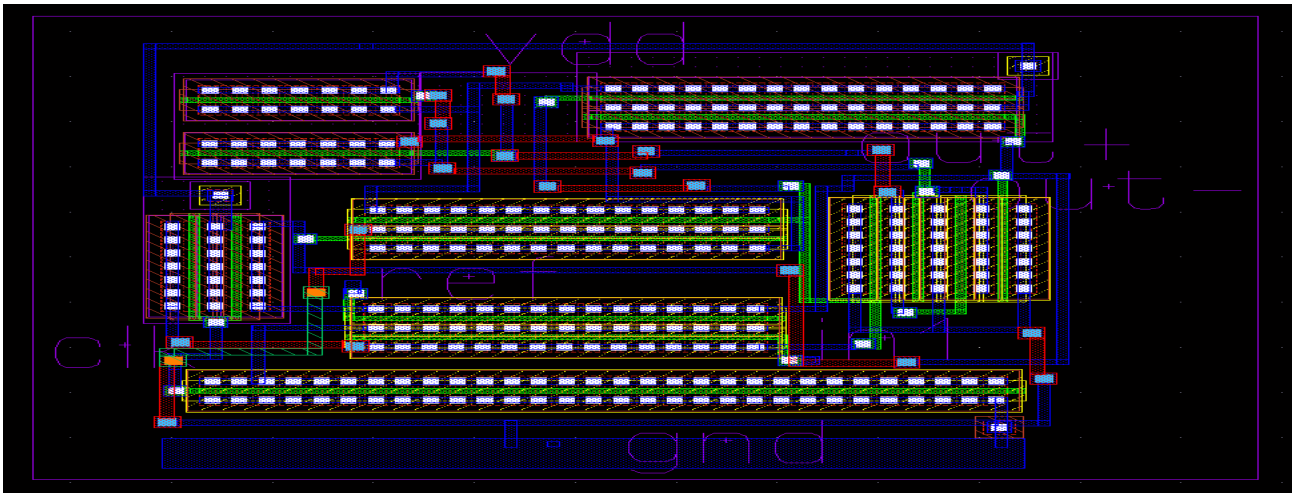


RC Extraction:

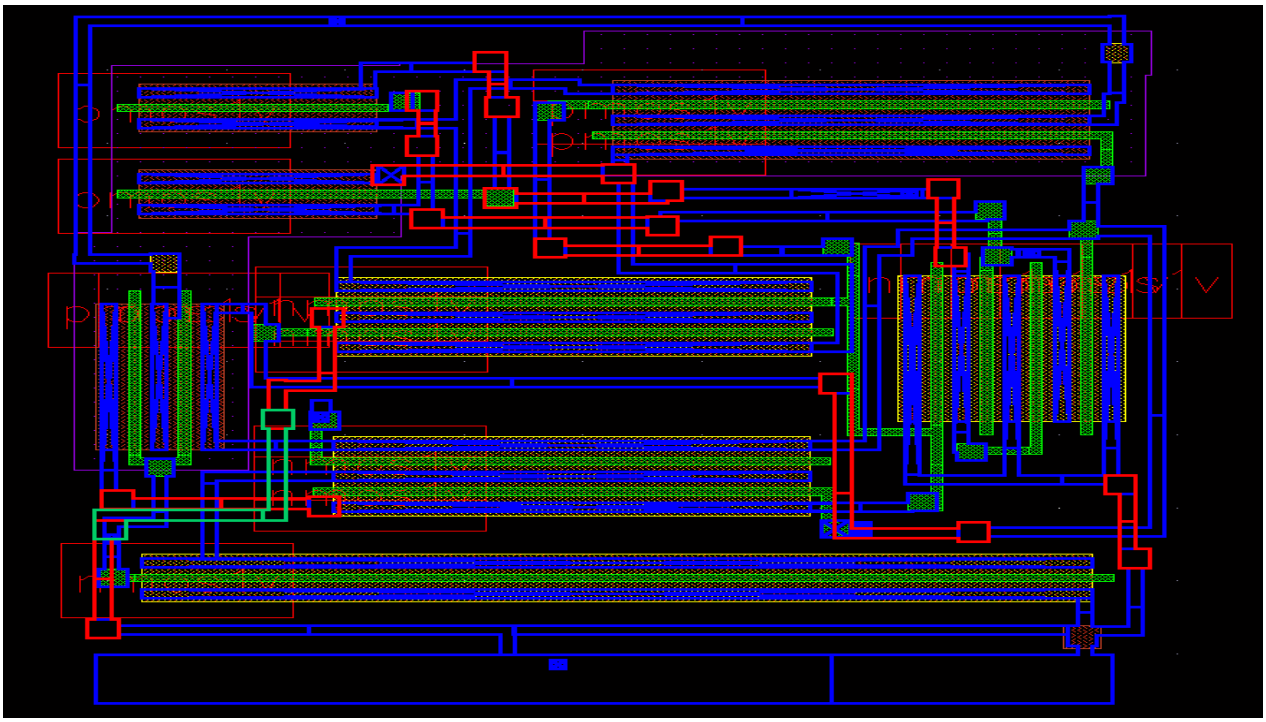


Dynamic Comparator without Calibration:

Layout:

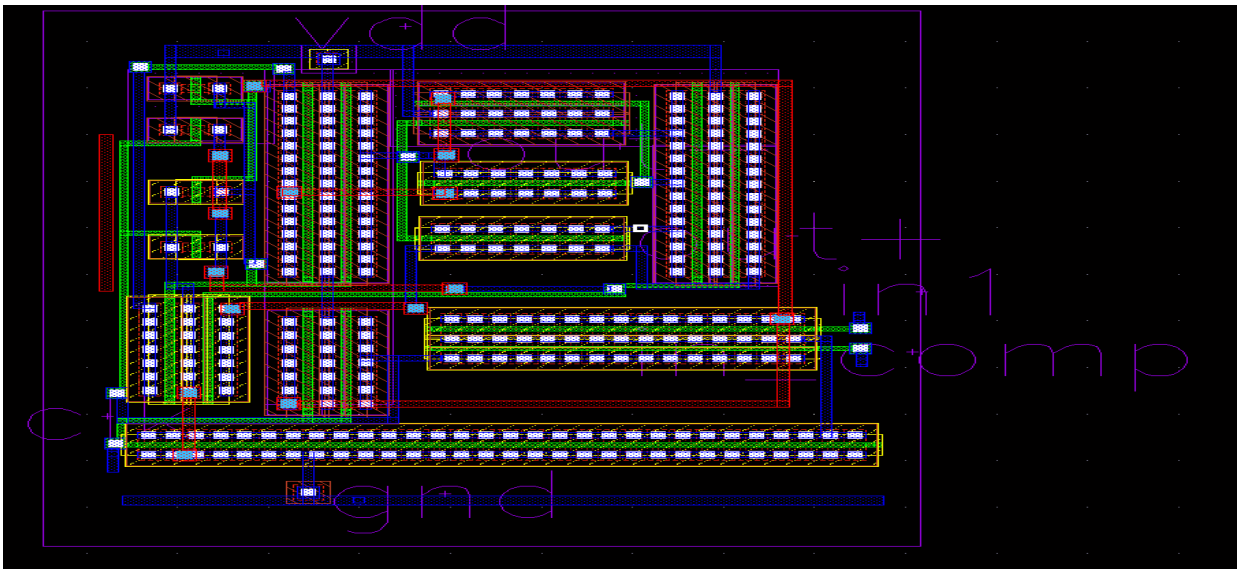


RC Extracted:

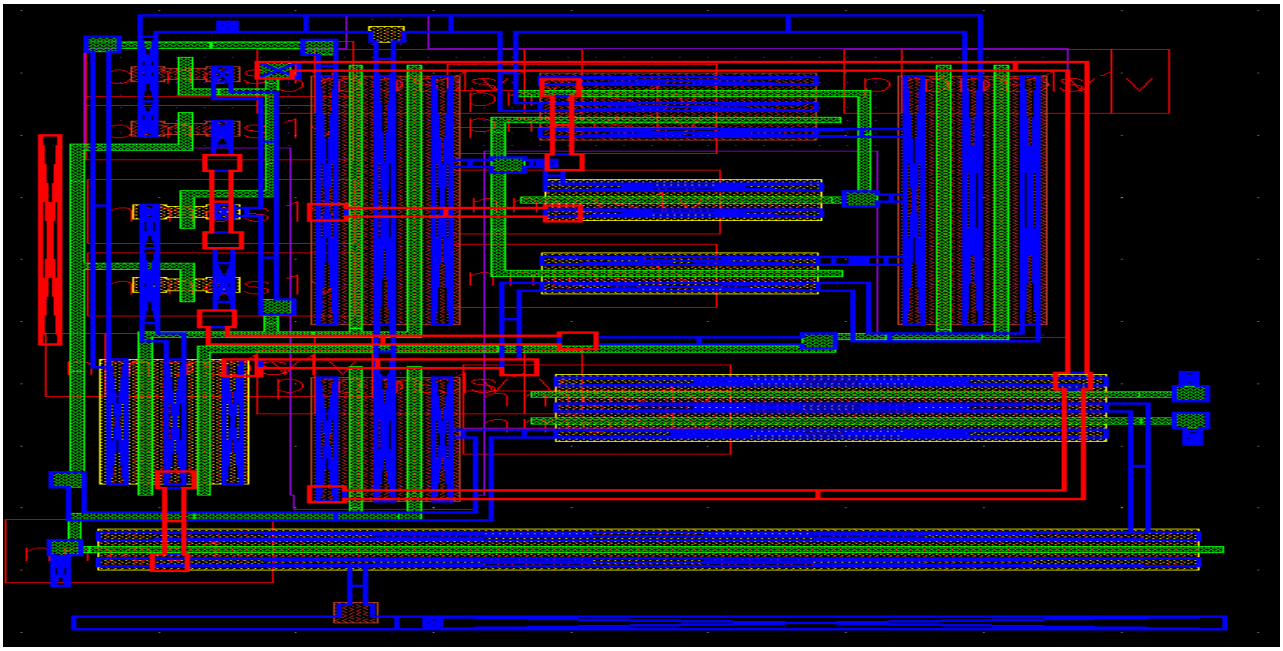


Double Tail Dual Rail Dynamic Latched Comparator:

Layout:

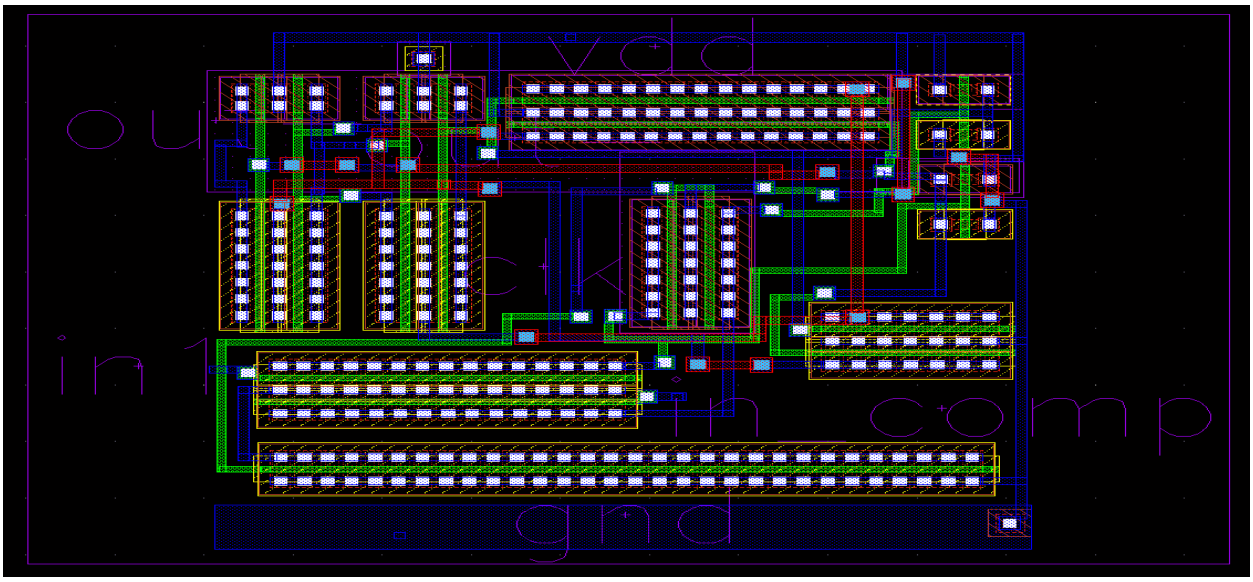


RC EXTRACTED:



PROPOSED COMPARATOR:

Layout:



RC Extracted: