INVESTIGATION OF POWER FACTOR CORRECTION IN SINGLE PHASE AC-DC CONVERTERS

A THESIS

SUBMITTED IN PARTIAL FULFILLMENT OF THE

REQUIREMENTS FOR

THE DEGREE OF

MASTER OF TECHNOLOGY (RESEARCH)

IN
POWER ELECTRONICS

By

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National institute of Technology
Rourkela-769008
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CERTIFICATE

This is to certify that the thesis entitled "**Investigation Of Power factor correction in single phase ac-dc converters**" submitted by **Ms. Nirjharini Sahoo**, in partial fulfillment of the requirements for the award of Master of Technology (Research) in the Department of Electrical Engineering, with specialization in '**Power Electronics'** at National Institute of Technology, Rourkela (Deemed University) is an authentic work carried out by her under my supervision and guidance.

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other University/Institute for the award of any Degree or Diploma.

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Ms.Nirjharini Sahoo
M.Tech (Research)
(Power Electronics)

CONTENTS

ABBREVIATIONS

AC	-Alternating Current
CICM	- Continuous Inductor Current Mode
DC	-Direct Current
DICM	- Discontinuous Inductor Current Mode
EMI	- Electromagnetic Interference
HPF	-High Power Factor
IEEE	-Institute of Electrical and Electronics Engineers
IEC	- International Electro-technical Committee
IGBT	-Insulated Gate Bipolar Transistor
MOSFET	-Metal Oxide Semiconductor Field Effect Transistor
PFC	-Power Factor Correction
PWM	- Pulse Width Modulation
RMS	-Root Mean Square
THDi	-Total Harmonic Distortion of input line current
ZVT	- Zero Voltage Transition
ZVS	- Zero Voltage Switching
ZCS	- Zero Current Switching

LIST OF SYMBOLS

C	-Capacitance
L	- Inductance Of The Ideal Inductor
P	-Active Power In A Sinusoidal System
R	-Resistance Of The Ideal Resistor R
S	-Active Switch
S	- Apparent Power
T_{off}	-Off-Time Of An Active Switch
T_{on}	-On-Time Of An Active Switch
T_s	-Switching Period
T_D	- Delay Time
Thd_i	-Total Harmonic Distortion Of The Line Current
V	-Phasor Representation Of A Sinusoidal Voltage
V_{rms}	-RMS Value Of The Purely Sinusoidal Line Voltage
PF	-Power Factor
Ø	-Displacement Angle
K_p	- Purity Factor
I_{vref}	-Inductor Valley Current Reference
I_{pref}	-Inductor Peak Current Reference
C_f	- Filter Capacitance
L_r	- Resonant Inductor
C_r	- Resonant Capacitor
I_{lr}	-Resonant Inductor Current
V_{cr}	-Resonant Capacitor Voltage
V_0	-Output Voltage
L_{in}	- Primary Input Inductor Current

ABSTRACT

An ac to dc converter is an integral part of any power supply unit used in the all electronic equipments. These electronic equipments form a major part of load on the utility. Generally, to convert line frequency ac to dc, a line frequency diode bridge rectifier is used. To reduce the ripple in the dc output voltage, a large capacitor is used at the rectifier output. But due to this large capacitor, the current drawn by this converter is peaky in nature. This input current is rich in low order harmonics. Also, as power electronics equipments are increasingly being used in power conversion, they inject low order harmonics into the utility. Due to the presence of these harmonics, the total harmonic distortion is high and the input power factor is poor. Because of the problems associated with low power factor and harmonics, utilities will enforce harmonic standards and guidelines, which will limit the amount of current distortion allowed into the utility, and thus the simple diode rectifier may not be in use. So, there is a need to achieve rectification at close to unity power factor and low input current distortion. Initially, **power factor correction schemes** have been implemented mainly for heavy industrial loads like induction motors, induction heating furnaces etc., which forms a major part of lagging power factor load. Hence, PFC is becoming an important aspect even for low power application electronic equipments.

There are two types of PFC's. 1) Passive PFC, 2) Active PFC. The active PFC is further classified into low-frequency and high-frequency active PFC depending on the switching frequency. Different techniques in passive PFC and active PFC are presented here. Among these PFC's, we will get better power factor by using high-frequency active PFC circuit. Any DC-DC converters can be used for this purpose, if a suitable control method is used to shape its input current or if it has inherent PFC properties. The DC-DC converters can operate in Continuous Inductor Current Mode – CICM, where the inductor current never reaches zero during one switching cycle or Discontinuous Inductor Current Mode - DICM, where the inductor current is zero during intervals of the switching cycle.

In DICM, the input inductor is no longer a state variable since its state in a given switching cycle is independent on the value in the previous switching cycle. The peak of the inductor current is sampling the line voltage automatically. This property of DICM input circuit can be called "self power factor correction" because no control loop is required from its input side. In

CICM, different control techniques are used to control the inductor current. Some of them are (1) peak current control (2) average current control (3) Hysteresis control (4) borderline control. These control techniques specifically developed for PFC boost converters are analyzed. For each control strategy advantages and drawbacks are highlighted.

This high frequency switching PFC stage also has drawbacks, such as: it introduces additional losses, thus reducing the overall efficiency; it increases the EMI, due to the high frequency content of the input current. The efficiency will be improved by reducing the losses using soft switching techniques such as 'Zero Voltage Switching'- (ZVS), 'Zero Voltage Transition' (ZVT), and 'Zero Current Switching'- (ZCS).

We study circuit techniques to improve the efficiency of the PFC stage by lowering the conduction losses and/or the switching losses. Operation of a ZVT converter has been discussed, in which the switching losses are minimized by using an additional auxiliary circuit incorporated in the conventional PWM boost converter. The proposed converter achieves zero voltage or zero current turn-on and turn-off for the main switch and soft switching for the auxiliary switch. Thus, the switching losses are reduced and the higher efficiency of the system is achieved.

Finally, ZVT technique has been implemented in a single-phase active power factor correction circuit based on an ac-dc boost converter topology and operating in a continuous inductor current mode with peak current control method. A 500 W, 40 kHz ZVT PWM boost PFC converter has been simulated and simulation results are validated with experimental results.

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CHAPTER 1

INTRODUCTION

Nonlinear loads and their effects

Standards regulating line current harmonics

Power factor correction

Applications of PFC

Research Background

Objective of this thesis work

INTRODUCTION:

Most applications requiring *ac-dc* power converters need the output *dc* voltage to be well regulated with good steady-state and transient performance. The circuit typically favored until recently (diode rectifier-capacitor filter) for the utility interface is cost effective, but it severely deteriorates the quality of the utility supply thereby affecting the performance of other loads connected to it besides causing other well-known problems. In order to maintain the quality of the utility supply, several national and international agencies have started imposing standards and recommendations for electronic instrument connected to the utility. Since the mid-1980's power electronics engineers have been developing new approaches for better utility interface, to meet these standards. These new circuits have been collectively called *Power factor correction (PFC)* circuits.

With the increase of consumer electronics the power quality becomes poor. The reactive power drawn from the supply is increasing [3]. This is because of the use of rectification of the AC input and the use of a bulk capacitor directly after the diode bridge rectifier. Reducing the input current harmonics to meet the agency standards implies improvement of power factor as well. For this reason the publications reported in this area have used "Power factor correction methods" and "Harmonic elimination/reduction methods" almost inter changeably. Several techniques for PFC and harmonic reduction have been reported and a few of them have gained greater acceptance over the others.

This chapter discusses the i) Nonlinear loads and their effect on the electricity distribution network, ii) Standard IEC and IEEE regulation for harmonics, iii) Power factor correction and its benefits, iv) application of PFC both for linear and non-linear loads, v) research background, vi) problem formulation , and vii) aim of the dissertation

1.1 NONLINEAR LOADS AND THEIR EFFECT ON THE ELECTRICITY DISTRIBUTION NETWORK:

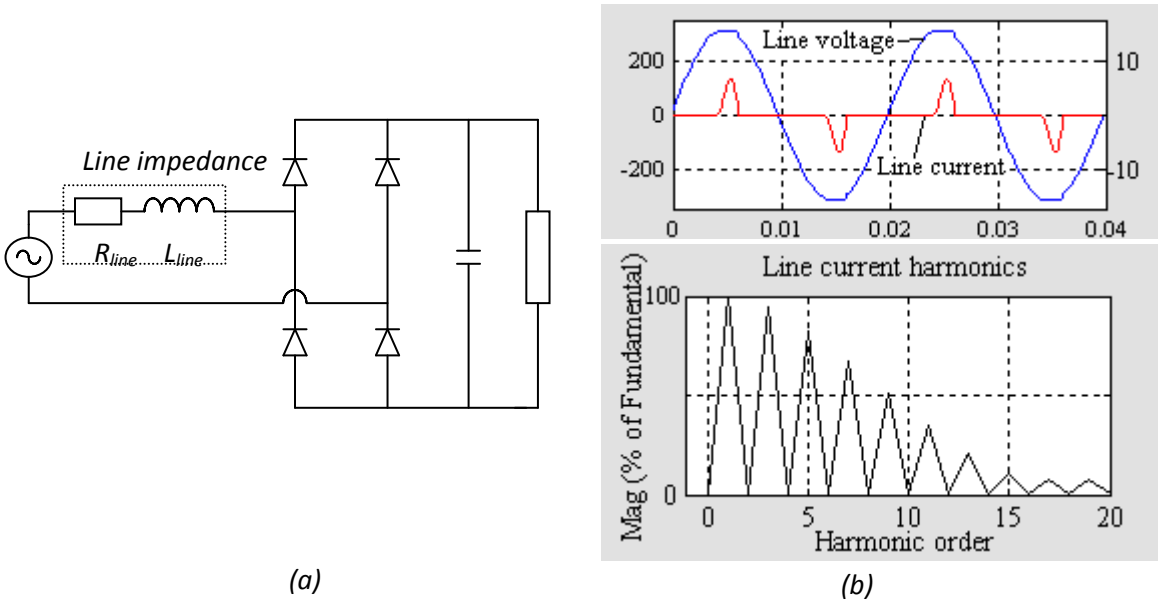
The instrument connected to an electricity distribution network usually needs some kind of power conditioning, typically rectification, which produces a non-sinusoidal line current due to the non-linear input characteristic.

Line-frequency diode rectifiers convert AC input voltage into DC output voltage in an uncontrolled manner. Single-phase diode rectifiers are needed in relatively low power instrument that needs some kind of power conditioning, such as electronic instrument and household appliances. For higher power, three-phase diode rectifiers are used. In both single and three-phase rectifiers, a large filtering capacitor is connected across the rectifier output to obtain DC output voltage with low ripple. As a consequence, the line current is non sinusoidal.

In most of these cases, the amplitude of odd harmonics of the line current is considerable with respect to the fundamental. While the effect of a single low power nonlinear load on the network can be considered negligible, the cumulative effect of several nonlinear loads is important. Line current harmonics have a number of undesirable effects on both the distribution network and consumers.

These effects include:

1. Losses and overheating in transformers, shunt capacitors, power cables, AC machines and Switchgear, leading to premature aging and failure.
2. Excessive current in the neutral conductor of three-phase four-wire systems, caused by odd Triple current harmonics (triple-n: 3rd, 9th, 15th, etc.).
3. Reduced power factor, hence less active power available from a wall outlet having a certain apparent power rating.
4. Electrical resonances in the power system, leading to excessive peak voltages and RMS currents, and causing premature aging and failure of capacitors and insulation.
5. The distorted line voltage may affect other consumers connected to the electricity distribution network.
6. Telephone interference.
7. Errors in metering instrument.
8. Increased audio noise.
9. Cogging or crawling in induction motors, mechanical oscillation in a turbine-generator combination or in a motor-load system.
10. Distortion of the line voltage via the line impedance shown in Fig.1.1 where the typical worst case values: R-Line=0.5 ohm, and L-Line=1mH have been considered. The effect is stronger in weaker grids. For example, some electronic instrument is dependent on accurate determination of aspects of the voltage wave shape, such as amplitude, RMS and zero-crossings



(a) *(b)*

Fig. 1.1: Single-phase diode bridge rectifier: (a) Schematic; (b) Typical line voltage and line current waveforms (upper plot) and odd line current harmonics (lower plot). And the line current has THD_i=1.5079 and power factor of 0.5475.

1.2. Standards regulating line current harmonics:

1.2.1 Standard IEC 1000-3-2:

1. It applies to instrument with a rated current up to and including 16Arms per phase which is to be connected to 50Hzor 60 Hz, 220-240Vrms single-phase or 380-415Vrms three-phase mains [1],[2].
2. Items of electrical instrument are categorized into four classes (A, B, C, and D), for which specific limits are set for the harmonic content of the line current.
3. These limits do not apply for the instrument with rated power less than 75w, other than lighting instrument.

CLASS-A:

Instrument not specified in one of the other three classes should be considered as class-A instrument. The classification can also be represented using the flowchart:

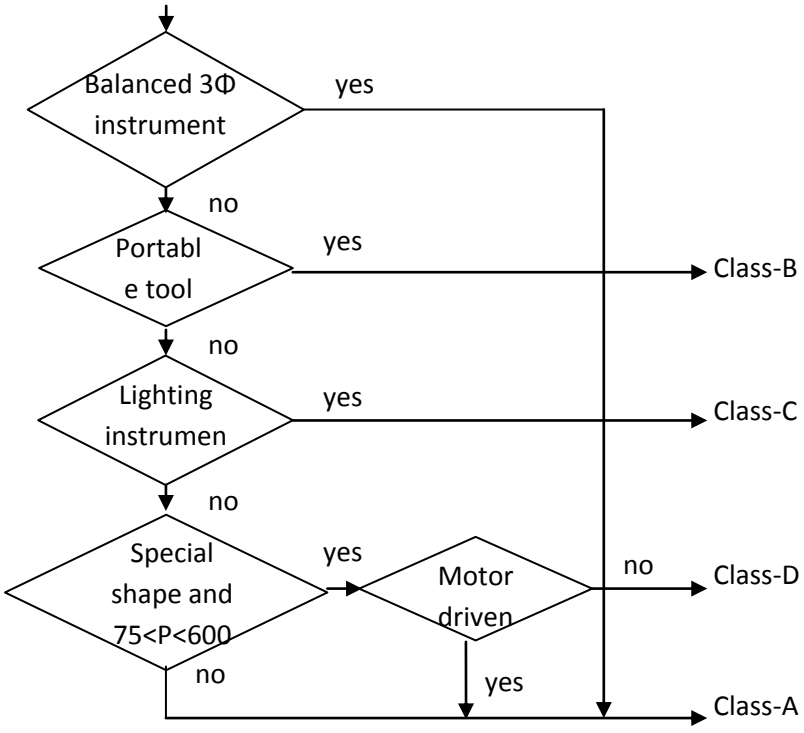


Fig: 1.2. Classification of instrument under Standard IEC 1000-3-2

CLASS-B:

It includes portable tools, and nonprofessional arc welding instrument.

CLASS-C:

It includes lighting instrument (except for dimmers for incandescent lamps, which belong to class-A).

CLASS-D:

Instrument with special line current shape i.e. includes instrument having an active input power less than or equal to 600w, of the following types:

i. Personal computers.
ii. Personal computer monitors.
iii. Television receivers.

Limits in standard IEC 1000-3-2:

Table 1.1(a): Limits for Class-A and Class-D

	Harmonic order	Class-A	Class-D	
		A_{rms}	A_{rms}	mA/W
odd harmonics	3	2.30	2.30	3.40
	5	1.14	1.14	1.90
	7	0.77	0.77	1.00
	9	0.40	0.40	0.50
	11	0.33	0.33	0.35
	13	0.21	0.21	0.29
	15 to 39	2.25/n	2.25 /n	3.85/n
Even harmonics	2	1.08		
	4	0.43		
	6	0.30		
	8 to 40	1.84/n		

Table 1.1(b): Limits for Class-B and C

	Harmonic order	Class-B	Class-C
		A_{rms}	%
odd harmonics	3	3.45	30*PF
	5	1.71	10
	7	1.15	7
	9	0.60	5
	11	0.49	3
	13	0.31	3
	15 to 39	3.375/n	3
Even harmonics	2	1.62	2
	4	0.64	
	6	0.45	
	8 to 40	2.76/n	

1.2.2 STANDARD IEEE 519-1992:

Gives recommended practices and requirements for harmonic control in electrical power systems for both individual consumers and utilities. The limits for line current harmonics are given as a percentage of the maximum demand load current I_L at the point of common coupling-PCC at the utility. They decrease as the ratio I_{SC}/I_L decreases where I_{SC} is the maximum short circuit current at PCC, meaning that the limits are lower in weaker grids. This standard covers also high voltage loads of much higher power.

Limits in standard IEEE 519-1992:

Table 1.2: Odd harmonic limits:

I_{SC}/I_L(%)	h<11	11≤h<17	17≤h<23	23≤h<35	35≤h	TDD*
<20	4.0	2.0	1.5	0.6	0.3	5
20 to 50	7.0	3.5	2.5	1.0	0.5	8
50 to 100	10.0	4.5	4.0	1.5	0.7	12
100 to 1000	12.0	5.5	5.0	2.0	1.0	15
>1000	15.0	7.0	6.0	2.5	1.4	20

*TDD=Total Demand Distortion.

1.3 POWER FACTOR CORRECTION:

Reduction of line current harmonics is needed in order to comply with the standard. This is commonly referred to as the Power Factor Correction – PFC, which may be misleading. When an electric load has a PF lower than 1, the apparent power delivered to the load is greater than the real power that the load consumes. Only the real power is capable of doing work, but the apparent power determines the amount of current that flows into the load, for a given load voltage.

Power factor correction (PFC) is a technique of counteracting the undesirable effects of electric loads that create a power factor PF that is less than 1.

The power factor is defined as the ratio of the active power P to the apparent power S:

PF = P/S (1.1)

For purely sinusoidal voltage and current, the classical definition is obtained:

PF= cos ∅ (1.2)

Where cosΦ is the displacement factor of the voltage and current. In classical sense, PFC means compensation of the "displacement factor".

The line current is non-sinusoidal when the load is nonlinear. For sinusoidal voltage and non-sinusoidal current the PF can be expressed as.

$$\mathrm{PF} = \frac{V_{rms}\mathrm{I1}rms}{V_{rms}I_{rms}}\cos\emptyset = \frac{\mathrm{I_{1rms}}}{\mathrm{I_{rms}}}\cos\emptyset = K_p\cos\emptyset \quad (1.3)$$

$$K_p = \frac{\mathrm{I_{1rms}}}{\mathrm{I_{rms}}}, K_p \in [0,1] \quad (1.4)$$

K_p describes the harmonic content of the current with respect to the fundamental. Hence, the power factor depends on both harmonic content and displacement factor. K_p is referred to as purity factor or distortion factor.

The total harmonic distortion factor THD_i is defined as

$$\mathrm{THDi} = \frac{\sqrt{\sum_{n=2}^{\infty} I_{n,rms}^2}}{\mathrm{I_{1rms}}} \quad (1.5)$$

Hence the relation between Kp and THDi is

$$K_p = \frac{1}{\sqrt{1+THD^2}} \quad (1.6)$$

Standard IEC 1000-3-2 sets limits on the harmonic content of the current but does not specifically regulate the purity factor Kp or the total harmonic distortion of the line current THD_i. The values of Kp and THD_i for which compliance with IEC 1000-3-2 is achieved depend on the power level. For low power level, even a relatively distorted line current may comply with the standard. In addition to this, it can be seen from (1.6) that the distortion factor Kp of a waveform with a moderate THD_i is close to unity (e.g. Kp=0.989 for THDi=15%). Considering (1.3) as well, the following statements can be made:

1. Power factor PF is not significantly degraded by harmonics, unless their amplitude is quite large (low K_p, very large THD_i).
2. Low harmonic content does not guarantee high power factor (K_p close to unity, but low $\cos\Phi$).

1.3.1 Benefits Of Power Factor:

1. Voltage distortion is reduced.
2. All the power is active.
3. Smaller RMS current.
4. Higher number of loads can be fed.

Most of the research on PFC for nonlinear loads is actually related to the reduction of the harmonic content of the line current. There are several solutions to achieve PFC [3], [4]. The shape of the input current can be further improved by using a combination of low pass input and output filters [5],[6][7],[8].Depending on whether active switches (controllable by an external control input) are used or not, PFC solutions can be categorized as "Passive" or "Active".

In *passive* PFC, only passive elements are used in addition to the diode bridge rectifier, to improve the shape of the line current. Obviously, the output voltage is not controllable. For *active* PFC, active switches are used in conjunction with reactive elements in order to increase the effectiveness of the line current shaping and to obtain controllable output voltage. The switching frequency further differentiates the active PFC solutions into two classes. In *low-frequency* active PFC, switching takes place at low-order harmonics of the line-frequency and it is synchronized with the line voltage. In *high-frequency* active PFC, the switching frequency is much higher than the line frequency.

1.4 APPLICATIONS OF PFC:

1.4.1 Electricity industry: Power factor correction of linear loads.

Power factor correction is achieved by complementing an inductive or a capacitive circuit with a (locally connected) reactance of opposite phase. For a typical phase lagging PF load, such as a large induction motor, this would consist of a capacitor bank in the form of several parallel capacitors at the power input to the device. Instead of using a capacitor, it is possible to use an unloaded synchronous motor. This is referred to as a synchronous condenser. It is started and connected to the electrical network. It operates at full leading power factor and puts VARs onto

the network as required to support a system's voltage or to maintain the system power factor at a specified level. The condenser's installation and operation are identical to large electric motors.

The reactive power drawn by the synchronous motor is a function of its field excitation. Its principal advantage is the ease with which the amount of correction can be adjusted; it behaves like an electrically variable capacitor.

1.4.2 Switched mode power supply: Power factor correction of non-linear loads.

A typical switched-mode power supply first makes a DC bus, using a bridge rectifier or similar circuit. The output voltage is then derived from this DC bus. The problem with this is that the rectifier is a non-linear device, so the input current is highly non-linear. That means that the input current has energy at harmonics of the frequency of the voltage. This presents a particular problem for the power companies, because they cannot compensate for the harmonic current by adding capacitors or inductors, as they could for the reactive power drawn by a linear load. Many jurisdictions are beginning to legally require PFC for all power supplies above a certain power level.

The simplest way to control the harmonic current is to use a filter: it is possible to design a filter that passes current only at line frequency (e.g. 50 or 60 Hz). This filter kills the harmonic current, which means that the non-linear device now looks like a linear load. At this point the power factor can be brought to near unity, using capacitors or inductors as required. This filter requires large-value high-current inductors, however, which are bulky and expensive.

It is also possible to perform active PFC. In this case, a boost converter is inserted between the bridge rectifier and the main input capacitors. The boost converter attempts to maintain a constant DC bus voltage on its output while drawing a current that is always in phase with and at the same frequency as the line voltage. Another switch-mode converter inside the power supply produces the desired output voltage from the DC bus. This approach requires additional semiconductor switches and control electronics, but permits cheaper and smaller passive components. It is frequently used in practice. Due to their very wide input voltage range, many power supplies with active PFC can automatically adjust to operate on AC power from about 100 V (Japan) to 240 V (UK). That feature is particularly welcome in power supplies for laptops and cell phones.

1.5 Research Background:

There is a significant interest on the part of society to reduce the amount of nonlinear loading on AC power systems. This loading reduces the distribution capacity of the public power system, and it can degrade the quality of the power by distorting the AC power waveform delivered to nearby customers. The negative effects of line current distortion have prompted a need for setting limits for the line current harmonics of instrument connected to the electricity distribution network. Standardization activities in this area have been carried out for many years. As early as 1982, the International Electro-technical Committee-IEC published its standard IEC 555-2, which was also adopted in 1987 as European standard EN 60555-2, by the European Committee for Electro-technical Standardization - CENELEC. Standard IEC 555-2 has been replaced in 1995 by standard IEC 1000-3-2 [1], [2], also adopted by CENELEC as European standard EN 61000-3-2. Most of the research on PFC for nonlinear loads is actually related to the reduction of the harmonic content of the line current. There are several solutions to achieve PFC, which were discussed in [3], [4]. Depending on whether active switches (controllable by an external control input) are used or not, PFC solutions can be categorized as "Passive" or "Active".

1.5.1 Passive PFC

In Passive PFC circuit only passive elements are used in addition to the diode bridge rectifier, to improve the shape of the line current. In order to improve the shape of the line current Passive Power Factor correction circuit simply uses an inductor in the input circuits. The shape of the input current can be further improved by using a combination of low pass input and output filters was given in [5-8]. To maintain the flow of input current, voltage doublers is inserted to feed the valley fill circuit [9], [10]. Even though line current harmonics are reduced, the fundamental component may show an excessive phase shift that reduces the power factor. Better characteristics can be obtained by using "Active PFC".

1.5.2 Active PFC

Active power factor correction can be accomplished by many ways. The Boost converter operated on the rectified output uses a constant switching frequency PWM and DCM operation reduces the total harmonic distortion of the input current [11], [12], [14], [15]. In a Boost circuit the switching device can handles only a portion of output power which increases the efficiency. The efficiency can be increased by keeping the ratio of output voltage to input voltage closer to unity. The effect of second harmonic in PWM in reducing third harmonic component in the input current is established. In this converter the output is varied by varying the duty cycle keeping the

frequency constant. In this control method, the duty cycle D is varied by injecting second harmonic to the reference signal. The variation of D is given by $D = K[1 + m.\sin(2\omega t + \Omega)]$,where k proportional coefficient which controls the input power, m modulation index, w input frequency, Ω initial phase angle that controls the THD value in the input current[16].

The other converter topologies for a PFC based Sepic topology are reported in [17-19], which allow comparison of converter performance with different control techniques. The advantages of clamped current control include overall simplicity, relatively low inductive energy storage and component stresses, and fixed operating frequency discussed in[20],[22]. Another control method, which allows a better input current waveform, is the average current control represented in Fig.5.3 [21, 23-25].

Hysteresis control technique has been reported in [26-27]. In this control technique, the switch is turned on when the inductor current goes below the lower reference I_{vref}, and is turned off when the inductor current goes above the upper reference, giving rise to a variable frequency control. But in Borderline Control approach [28] the switch on-time is held constant during the line cycle and the switch is turned on when the inductor current falls to zero, so that the converter operates at the boundary between Continuous and Discontinuous Inductor Current Mode (CICM-DICM). The paper [48] presents a new approach for generating reference currents for an active filter and a static compensator. The purpose of the compensating scheme is to balance the load, as well as make the supply side power factor a desired value. Here a suitable compensator structure is proposed which tracks the reference currents in a hysteresis band control scheme.

1.5.3 EMI Problem

The converters operating in CICM reduces the line current harmonics, but it has some drawbacks, such as: 1) It increases the EMI, due to the high-frequency content of the input current. 2) It introduces additional losses, thus reducing the overall efficiency. However the high frequency EMI can be eliminated by introducing an EMI filter between AC supply and diode bridge rectifier were found in various studies [29],[30],[31]. The second requirement for the EMI filter: the displacement angle Φ must be kept low. The third requirement is related to the overall stability of the system. It is known that unstable operation may occur due to the interaction between the EMI filter and the power stage. This phenomenon is given in [32], [33] and [34] .

However the losses are reduced by inserting an inductor in the series path of the boost rectifier to reduce the di/dt rate during its turn-off [35]. Better characteristics are obtained in Zero Voltage

Transition – ZVT topologies, at the expense of increased complexity. Several ZVT topologies was found in [36-41]. The converter proposed in [42] reduces the current stress on the main switch, and it will still keep the advantages of a PWM converter because after the switching transition is over, the circuit reverts back to PWM operation mode. Most attention is paid to the damping of voltage harmonics. However, this control strategy allows mitigating voltage dips in [43].

The focus of the topology [44] is to reduce the DC bus voltage at light load without compromising with input power factor and voltage regulation. The boost inductor operation is maintained in the discontinuous current mode (DCM) [45], So that natural power factor correction is obtained. The research got a tremendous boost with the strides made in the miniaturization of the electrical industry [47]. According to this the harmonics and noise can be reduced by using EMI Filter connected at the input side of Boost PFC Converter. The purpose of the compensating scheme [48] is to balance the load, as well as make the supply side power factor a desired value. However Over the years, lot of research has been carried out for the supply of quality power to the consumers, by minimizing Electro Magnetic Interference is presented in [49].

1.5.4 Switching Loss:

In active PFC circuit, switching of semiconductor devices normally occurs at high current levels. Therefore, when switching at high frequencies these converters are associated with high power dissipation. Also, the higher input and lower output voltages bring about very low duty cycles. Hence, the high side MOSFET switch should turn on and off in a very short period of time, which also brings switching losses into picture [50], [51], [52]. The losses due to switching produce three considerable effects [53] on the converters in general,

1. Achievable f_S and efficiency limited
2. EMI at high frequencies due to high di/dt, dv/dt and induces noise
3. Switching losses may sometimes exceed safe operating area

Switching loss of a MOSFET can be represented mathematically as,

$$P_{SW} = \frac{V_{DS}.I_D.f_S}{2}(t_{on} + t_{off})$$

From above equation some important result can be deduced that switching losses can be reduced by two methods:

(i) By reducing the turn-on and turn-off delay times. This is done by using faster and more efficient switches in the converter.

(ii) By making the current or voltage across the switch zero before turning it on or off. Soft switching resonant converters are based on this concept.

Also it is inferred from the equation that the switching loss in any semiconductor switch varies linearly with f_S and the delay times [53], [54].

Hard switching is the predominant loss mechanism in the high side MOSFET followed by the conduction losses of the low side MOSFET [55], [56]. Some 60% to 70% of the total losses are in the MOSFET for a 60W power converter (Step – Down). Thus, more efficient power MOSFETs is needed that offer both reduced conduction and switching losses at higher frequencies [57]. The switching losses at higher frequencies can be eliminated by the soft switching techniques available.

1.5.4.1 Solution

There are mainly two techniques to eliminate the switching losses namely ZVS and ZCS. QRCs were introduced to overcome the disadvantages of conventional PWM converters operating at high switching frequency by achieving ZVS for the active switch and ZCS for the rectifier diode [58]-[61]. ZVS MRCs technique utilizes all major parasitic of the power stages and all semiconductor devices in MRC operate with ZVS, which substantially reduces the switching losses and noise [62].

In both techniques, the switching losses in the semiconductor devices are eliminated due to the fact that current through or voltage across the switching device at switching point is equal to or near zero. This reduction in the switching loss allows the designer to attain a higher operating frequency without sacrificing converter efficiency. By doing so, the resonant converters show promise of achieving what could not be achieved by the PWM converter that is the design of small size and weight converters. Currently, resonant power converters operating in the range of a few megahertz are available. Another advantage of resonant converters over PWM converters is the decrease of harmonic content in the converter voltage and current waveforms. Therefore, when the resonant and PWM converters are operated at the same power level and frequency, it is expected that the resonant converter will have lower harmonic emission [63].

The Resonant converters operate with sinusoidal current through the power switches which results in high peak and RMS currents for the power transistors and high voltage stresses on the

rectifier diodes. Furthermore, when the line voltage or load current varies over a wide range, QRCs are modulated with a wide switching frequency range, making the circuit design difficult to optimize [64]. As a compromise between the PWM and resonant techniques, various soft switching PWM converter techniques has been proposed to aim at combining desirable features of both the conventional PWM and Quasi Resonant techniques without a significant increase in circulating energy.

1.5.4.2 ZVT and ZCT

Such a solution has been achieved by ZVT and ZCT. The choice between the two depends on the semiconductor device technology that will be used. In the case of majority carrier semiconductors, the best choice would be ZVS, where the capacitive turn-on losses can be eliminated. On the other hand, in the case of minority carrier semiconductors, the ZCS technique can avoid the turn off losses caused by the current tail [65].

The voltage-mode soft-switching method that has attracted most interest in recent years is the ZVT. This is because of its low additional conduction losses and because its operation is closest to the PWM converters. Instead of using a series resonant network across the power switch, an alternative way is to use a shunt resonant network across the power switch. The auxiliary circuit of the ZVT converters is activated just before the main switch is turned on and ceases after it is accomplished. The auxiliary circuit components in this circuit have lower ratings than those in the main power circuit because the auxiliary circuit is active for only a fraction of the switching cycle. A partial resonance is created by the shunt resonant network to achieve ZCS or ZVS during the switching transition. And it will still keep the advantages of a PWM converter because after the switching transition is over, the circuit reverts back to PWM operation mode [66 -70].

Previously proposed ZVT-PWM converters have at least one of the following key drawbacks.

1. The auxiliary switch is turned off while it is conducting current. This causes switching losses and EMI to appear that offsets the benefits of the using the auxiliary circuit. In converters such as the ones proposed in [71], [72] the turn off is very hard.
2. The auxiliary circuit components have high voltage and/or current stresses. Such as converters proposed in [73], [74]. The converter proposed in [70] reduces the current stress on the main switch, but circuit is very complex.

3. The active clamp technique have been reported in [46], where zero-voltage switching has been achieved for main and auxiliary switch.

Reducing switching loss for high side switch is of more importance. Hence this work presents the implementation of ZVT techniques in PFC circuit, where soft switching is achieved for both main and auxiliary switches.

1.6 Problem Formulation:

The investigation of PFC faces the following problems:

1. High PF with low efficiency.
2. High efficiency with low PF.

1.7 Aim of This Dissertation:

To better define the scope of the research reported in this dissertation, the PFC is performed by a high frequency switching DC/DC converter that shapes the input current as close as possible to a Sinusoidal waveform which is in phase with the line voltage. Thus, from the electrical point of view, the instrument connected to the line behaves like a resistive load.

While the high-frequency switching PFC stage reduces the line current harmonics, it also has drawbacks, such as: it introduces additional losses, thus reducing the overall efficiency; it increases the EMI, due to the high-frequency content of the input current; and it increases the complexity of the circuit, with negative effects on the reliability of the instrument, as well as on its size, weight and cost. The general aim of this dissertation is to investigate high-frequency switching circuit topologies and methods to be applied in the PFC stage, which would alleviate some of the aforementioned drawbacks. The research addresses several aspects which can be divided into seven topics.

1.8 Thesis Organization:

Chapter 2: Provides the fundamental concepts and overview of passive PFC

Chapter 3: Deals with in-depth study of low frequency and high frequency active PFC.

Chapter 4: Discusses operations of converters In Discontinuous Inductor Current Mode (DICM).

Chapter 5: Presents detail control techniques during operation of converter in Continuous Inductor Current Mode (CICM).

Chapter 6: Presents the analysis, simulation, and experimental results of the proposed converters.

Chapter 7: Provides the concluding remarks and points to possible directions for future work to be carried out in this field.

CHAPTER 2

PASSIVE PFC

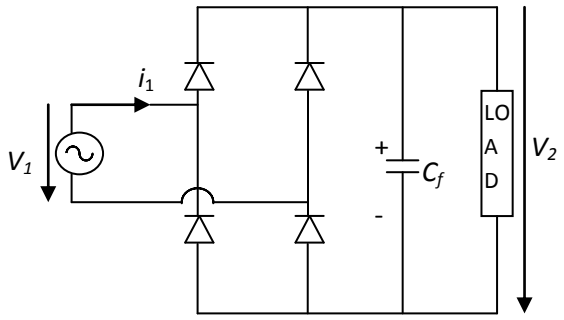
Diode bridge rectifier

Advantages of passive PFC

Disadvantages of Passive PFC

PASSIVE PFC:

Passive PFC methods use only passive elements in addition to the diode bridge rectifier, to improve the shape of the line current. As mentioned in the previous chapter, the diode bridge rectifier, shown again in Fig.2.1 (a), has non-sinusoidal line current. This is because most loads require a supply voltage with low ripple, which is obtained by using a correspondingly large capacitance the output capacitor C_f. Consequently, the conduction intervals of the rectifier diodes are short and the line current consists of narrow pulses with an important harmonic content.



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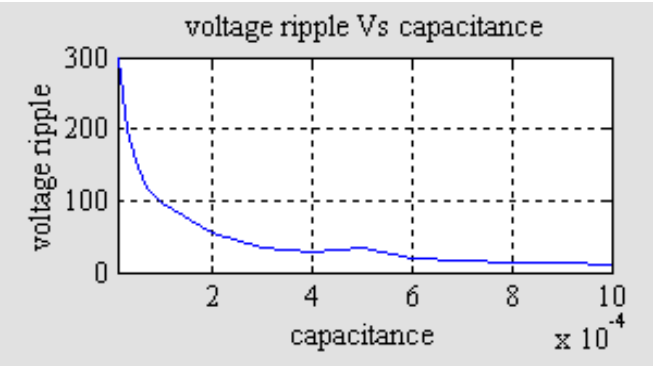

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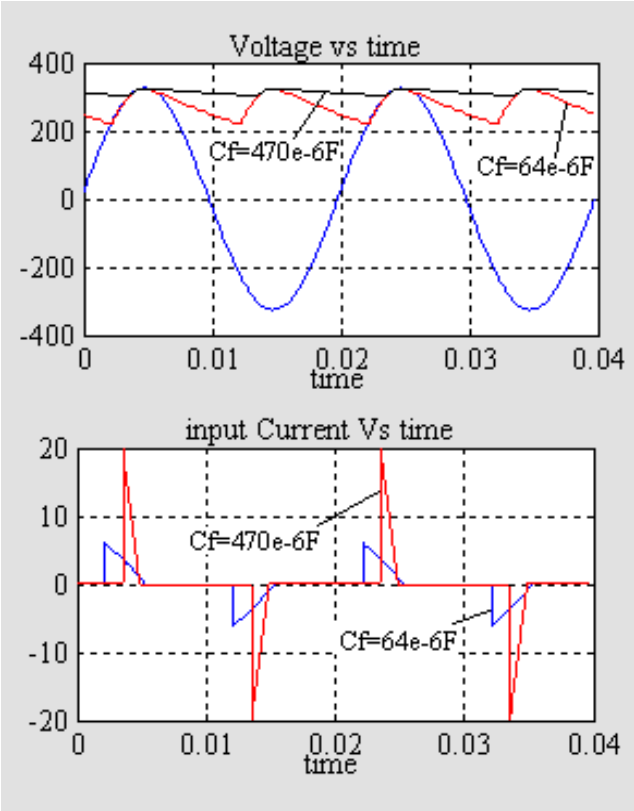

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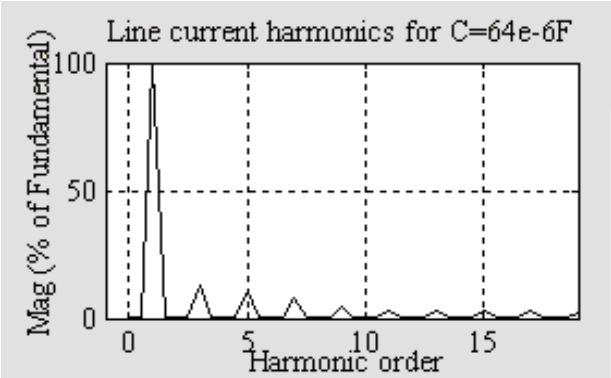

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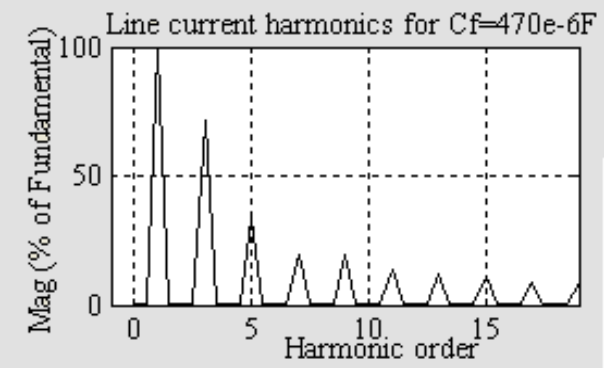


(e)

Fig. 2.1 Diode bridge rectifier: (a) Schematic; (b) Voltage ripple as a function of the output filter capacitance; (c) Line voltage and output voltage (upper plot), and input current (lower plot), with V_1=230Vrms 50Hz and constant power load P = 200W . With C_f = 470µF, the line current has K_p = 0.4349, cosΦ = 0.9695 and PF =0.4216, and the output voltage ripple is V_2 =25V. With Cf = 64µF, the line current has K_p = 0.6842, cosΦ = 0.8805 and PF =0.6024, and the output voltage ripple is V_2 =105V; (d) and (e) Line current harmonics with C_f=64µF and C_f =470µF respectively.

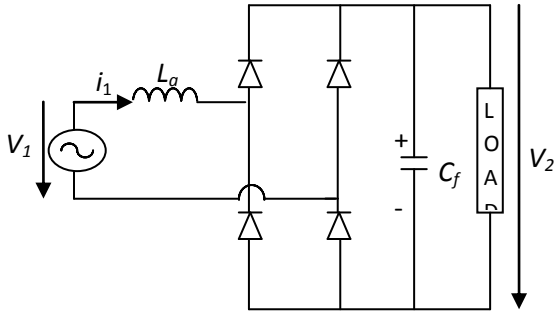
The simplest way to improve the shape of the line current, by adding additional components, is to use a lower capacitance of the output capacitor C_f . When this is done, the ripple of the output voltage increases and the conduction intervals of the rectifier diodes widen. The shape of the input current depends on the type of load that the rectifier is supplying. The shape of the input current is improved to a certain extent with the lower capacitance, at the expense of increased output voltage ripple, which can be seen from the results listed in the caption of Fig. 2.1. The concept is highlighted by the simulated waveforms shown in Fig. 2.1c), for two values of the output capacitor and assuming constant power load.

2.1 Diode Bridge Rectifiers:

Before going to passive PFC, let us discuss the simplest way to improve the shape of the line current by adding an output capacitor C_f When this is done, the ripple of the output voltage increases (shown in fig. 2.1(b)) and the conduction intervals of the rectifier diodes increases. The shape of the input current becomes also dependent on the type of load that the rectifier is supplying. The concept is highlighted by the simulated waveforms shown in Fig. 2.1, for two values of the output capacitor and assuming constant power load. The shape of the input current is improved to certain extent with the lower capacitance, at the expense of increased output voltage ripple, as can be seen also from the Fig. 2.1(b).The method presented above has severe limitations: it does not reduce substantially the harmonic currents and the output voltage ripple is large, which is not acceptable in most of the cases. Several other methods to reduce the harmonic content of the line current in single-phase systems exist, and an overview of the Passive PFC is presented next.

2.1.1 Rectifier with AC side inductor:

One of the simplest methods is to add an inductor at the AC-side of the diode bridge, in series with the line voltage as shown in Fig.2.2 (a), and to create circuit conditions such that the line current is zero during the zero crossings of the line voltage. The maximum power factor that can be obtained is PF= 0.78. Simulated results for the rectifier with AC-side inductor are presented in Fig.2.2. From the simulation results we can observe that increase in inductance L_a results in improved line current waveform with a lower THD_i, a better distortion factor and a better power factor.



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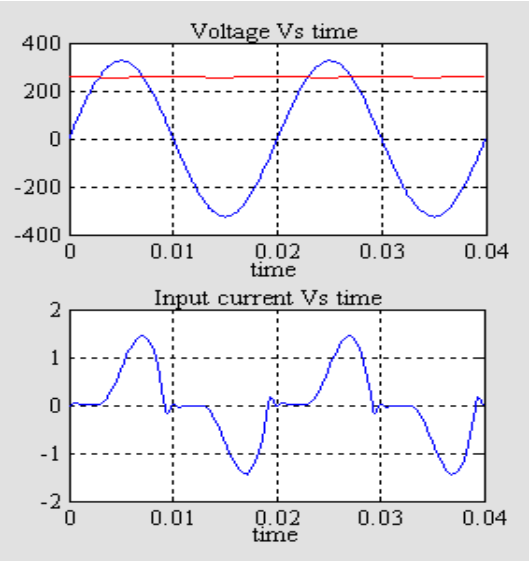

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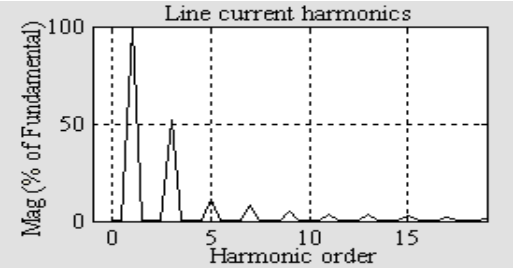

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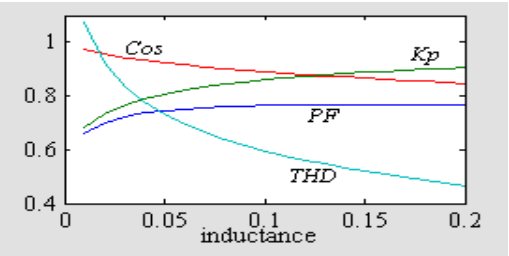
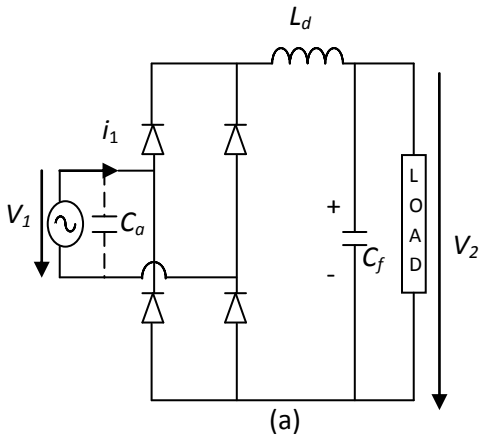


(d)

Fig.2.2 Rectifier with AC side inductor.(a) Schematic; Rectifier with AC-side inductor. (b)Line voltage, output voltage (upper plot) and line current (lower plot) with V_1=230Vrms 50Hz, resistive load R=500Ω: C_f =470μF, and L_a=130mH. The line current has K_p=0.8778, cosφ =0.8758 and PF =0.7688.The output voltage is V_2 =257V; (c) Line current harmonics; (d) Variation of different parameters as a function of inductance.

2.1.2 Rectifier with DC-side inductor:

The inductor can be also placed at the DC-side [5], as shown in Fig. 2.3(a) .The inductor current is continuous for a large value of inductance L_d. In the theoretical case of near infinite inductance, the inductor current is constant, so the input current of the rectifier has a square shape and the power factor is PF = 0.9, shown in Fig. 2.3(b). However, operation close to this condition would require a very large and impractical inductor, as illustrated by the simulated line current waveform for L_d =3H (without Ca), shown in Fig. 2.3(b). For lower inductance L_d, the inductor current becomes discontinuous. The maximum power factor that can be obtained in such a case is PF = 0.78, the operating mode being identical to the case of the AC-side inductor previously discussed. An improvement of the power factor can be obtained by adding the capacitor Ca between the bridge rectifier and AC power supply as shown in Fig. 2.3(a), which compensates for the displacement factor cosΦ. A design for maximum purity factor Kp and unity displacement factor cosΦ is possible, leading to a maximum obtainable power factor PF = 0.9118. The simulation results for L_d = 275mH with and without C_a=4.8µF is shown in Fig. 2.3(c).



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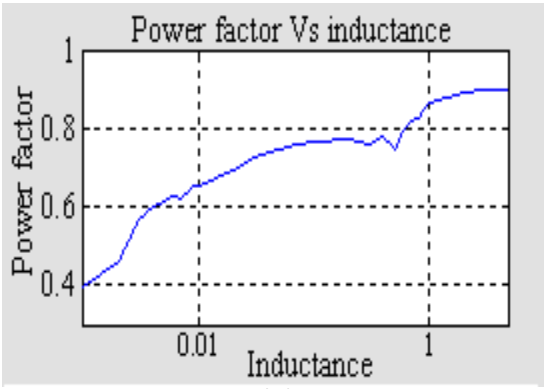

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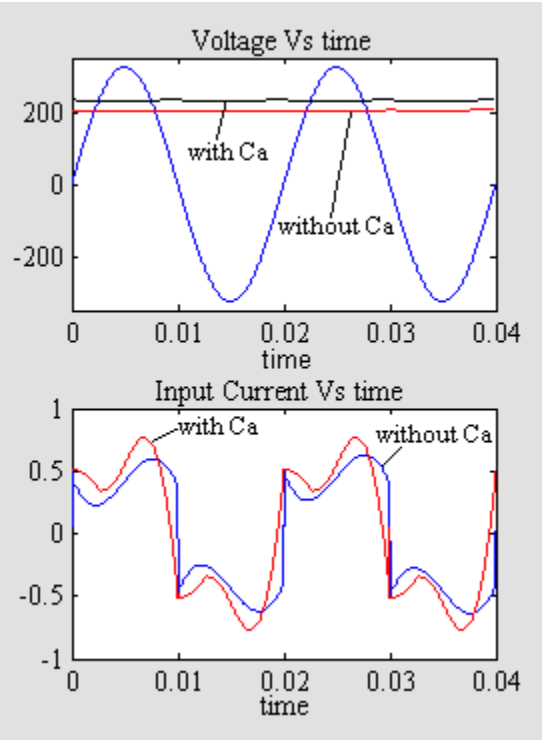

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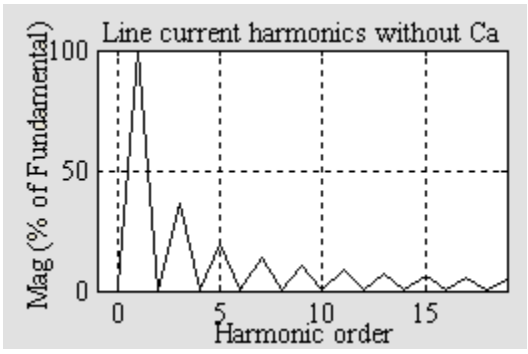

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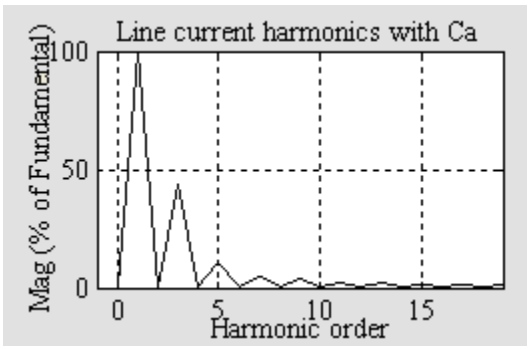
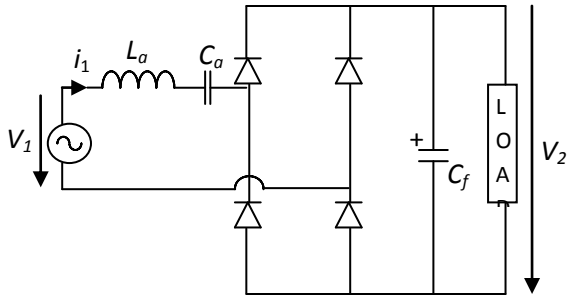


(e)

Fig.2.3 Rectifier with DC-side inductor. (a) Schematic; (b) Power factor Vs inductance without Ca; (c)Line voltage, output voltage (upper plot) and line current (lower plot) with V_1 = 230Vrms 50Hz, resistive load R=500Ω: and C_f =470μF. With La=275mH and without Ca, the line current has Kp = 0.8846, cosΦ = 0.9580 and PF = 0.8474, and the output voltage is V_2= 210V. With La=275mH and with Ca=4.8μF,the line current has Kp=0.9128, cosΦ=0.9989 and PF=0.9118, and the output voltage is V_2=231V. (d) Line current harmonics without C_a and (e) with Ca respectively.

2.1.3 Rectifier with series-resonant band-pass filter:

A band-pass filter of the series-resonant type, tuned at the line-frequency, is introduced in-between the AC source and the bridge rectifier as shown in Fig. 2.4 together with simulated waveforms [4, pp. 488-489]. By this method we can obtain almost unity power factor. For 50Hz networks, large values of the reactive elements are needed. Therefore, this solution is more practical for higher frequencies, such as for 400Hz and especially 20 kHz networks.



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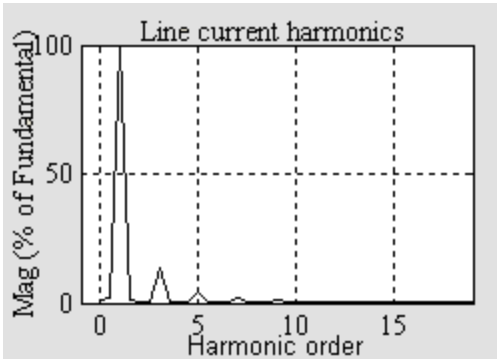

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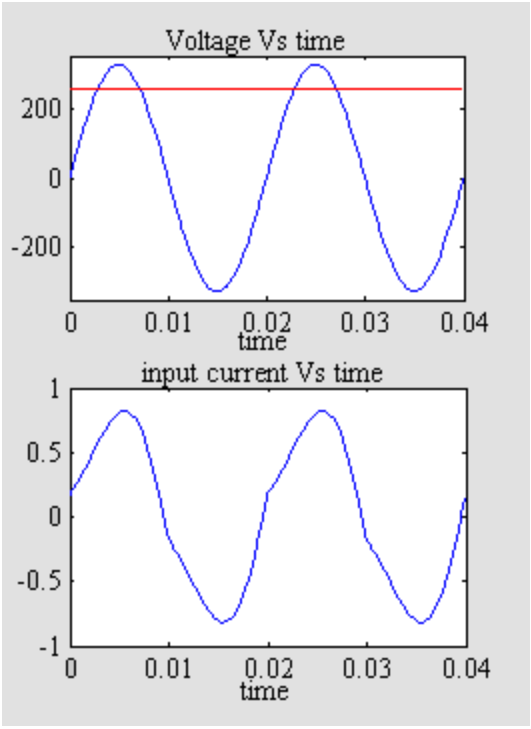


(c)

Fig.2.4 Rectifier with series-resonant band-pass filter. (a) Schematic; (b) Line current harmonics; (c) Line voltage, output voltage (upper plot) and line current (lower plot) with output voltage (red line) for V_1=230Vrms 50Hz, resistive load R=500Ω: C_f =470μF, La=1.5H and Ca=6.75μF. The line current has K_p=0.9937, cosΦ=0.9997 and PF=0.9934. The output voltage is V_2=254V.

2.1.4 Rectifier with parallel-resonant band-stop filter:

The band-stop filter of the parallel-resonant type [6] is presented in Fig. 2.5 together with simulated waveforms. The filter is tuned at the third harmonic, hence it allows for lower values of the reactive elements when compared to the series-resonant band-pass filter.

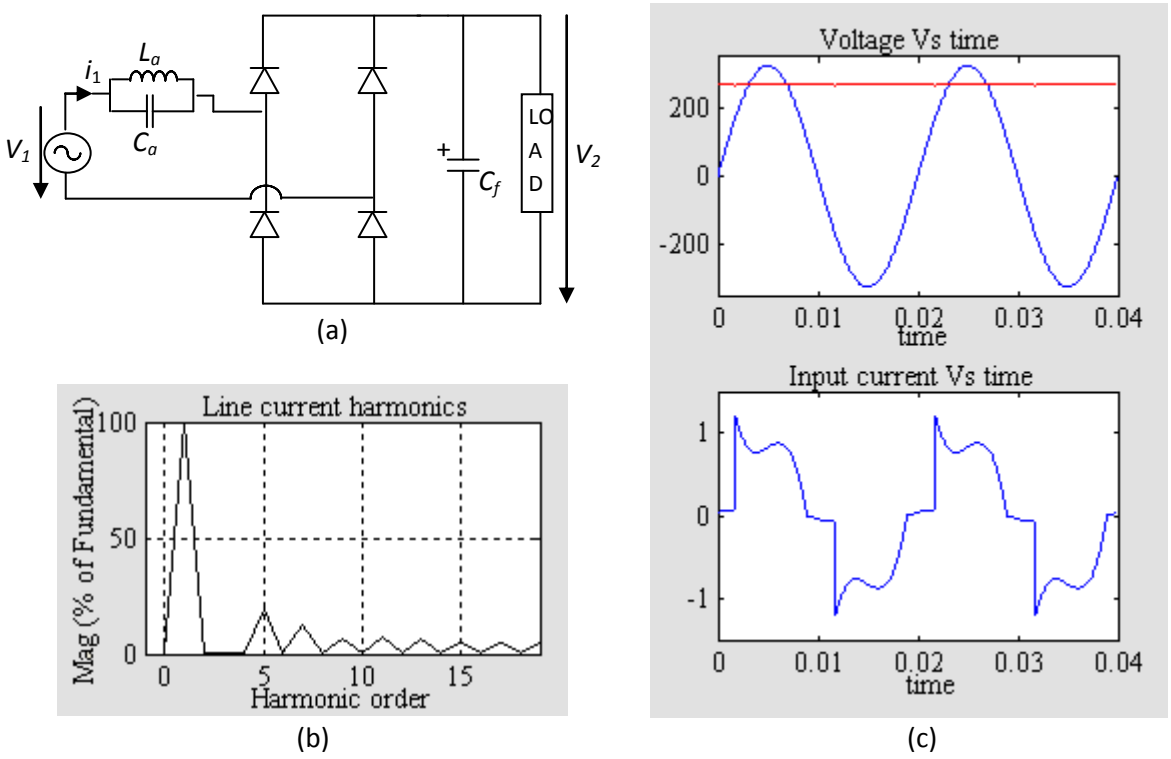


Fig.2.5 Rectifier with parallel-resonant band-stop filter. (a) Schematic; (b) Line current harmonics; (c) Line voltage (upper plot) and line current (lower plot) with output voltage is the straight line for V_1=230Vrms 50Hz, resistive load R=500Ω: filter capacitance C_f=470μF, band-stop filter components Lp=240mH, Cp=470μF tuned at third harmonic. Line current has Kp=0.9586,cosΦ=0.9987, and PF=0.9574. The output voltage is V_2=266V.

2.1.5 Capacitor-fed rectifier:

The capacitor-fed rectifier [7], shown in Fig. 2.6 together with simulated waveforms, is a very simple circuit that ensures compliance with standard IEC 1000-3-2 for up to approximately 250W input power at a 230V_{rms} line voltage. The conversion ratio is a function of X_a/R, where $X_a=1/(\omega_L C_a)$. Therefore, it is possible to obtain a specific output voltage, which is nevertheless lower than the amplitude of the line voltage and strongly dependent on the load. Despite the harmonic current reduction, the power factor is extremely low. This is not due to current harmonics, but due to the series-connected capacitor that introduces a leading displacement factor $cos\Phi$. An advantage could be that the leading displacement factor $cos\Phi$ can assist in compensating for lagging displacement factors elsewhere in the power system.

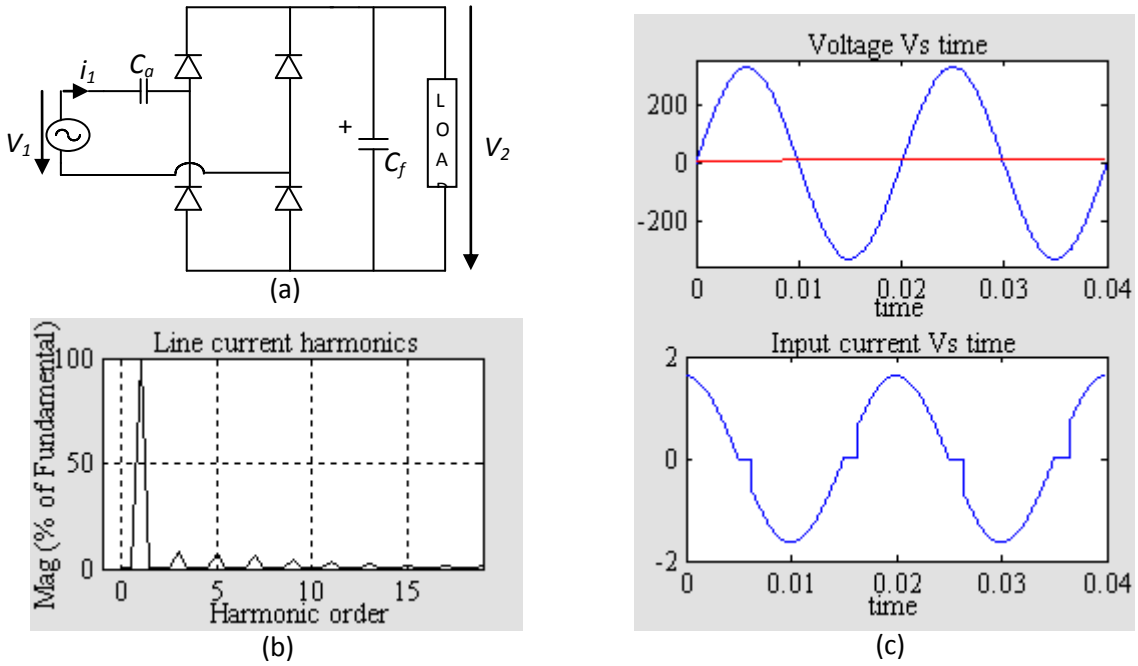


Fig.2.6 Capacitor-fed rectifier (a) Schematic; (b) Line current harmonics; (c) Line voltage, output voltage and line current (lower plot) with V_1=230Vrms 50Hz, resistive load R=500Ω: C_f =470μF, and Ca=16μF. The line current has Kp=0.9824, cosΦ=0.076 and PF=0.0747. The output voltage is V_2 =12V, efficiency=3.5387.

2.1.6 Rectifier with an additional inductor, capacitor and diode (LCD):

The rectifier with an additional inductor, capacitor, and diode – LCD rectifier [8] – is shown in ig.2.7, together with simulated waveforms. The circuit can be used to about 300W. The added reactive elements have relatively low values. The idea behind the circuit is linked to the previous definition of Class-D of the Standard IEC 1000-3-2. The circuit changes the shape of the input current .Here the power-related to limits of Class-D were avoided and the absolute limits of Class-A could be met for low power, in spite of the line current being relatively-distorted.

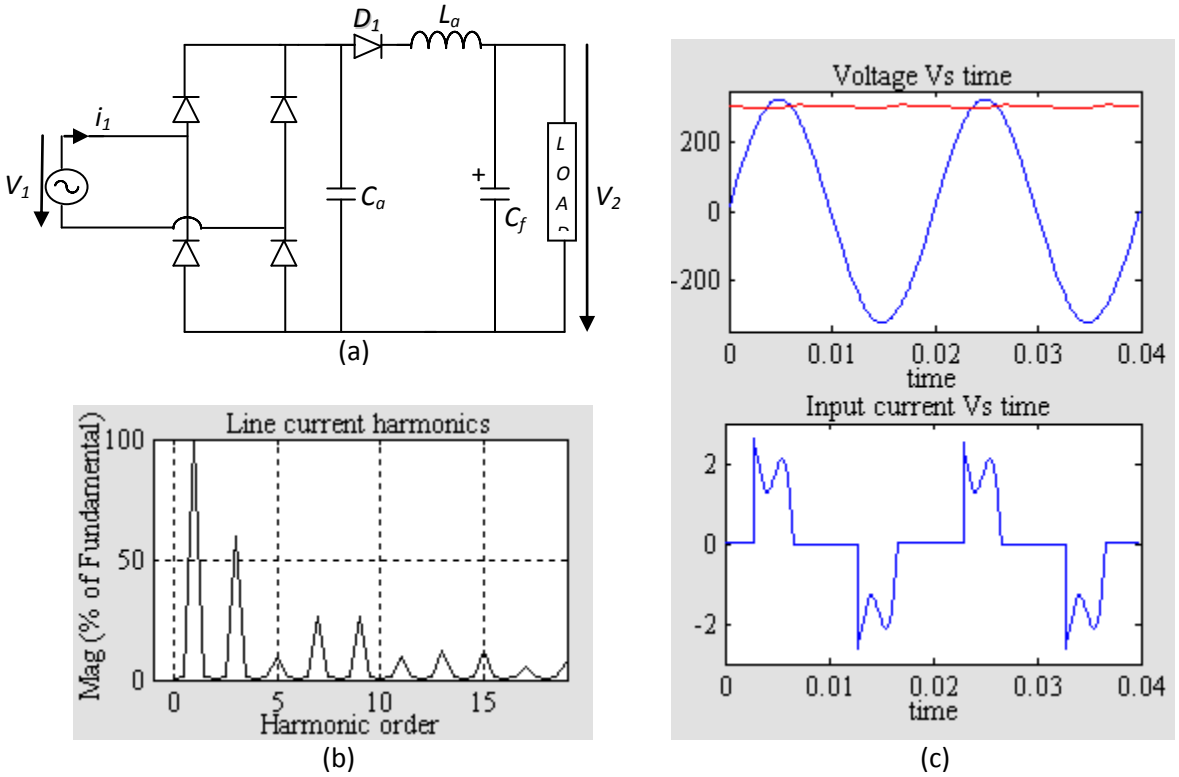


Fig.2.7 Rectifier with an additional inductor, capacitor and diode (LCD). (a) Schematic; (b) Line current harmonics; (c) Line voltage, output voltage (upper plot) and line current (lower plot) with V_1=230Vrms 50Hz, resistive load R=500Ω,C_f =470μF, Ca=40μF, and La=10mH.The line current has Kp= 0.7261, cosΦ=0.9947 and PF=0.7223. The output voltage is V_2 =304V.

2.1.7 Valley-fill rectifier:

Most of the input current distortion is caused by the discontinuous operation which crosses from positive to negative, and then from negative to positive, during each cycle. Due to these discontinuities substantial amount of harmonics were introduced into the input current waveform. If this cross-over distortion can be lessened or eliminated, then the likelihood of using this circuit to meet the IEC specifications would be very high. To maintain the flow of input current, a voltage doublers is inserted to feed the valley-fill circuit [10]. The current response can further be improved by the insertion of another resistor R_1. Insertion of this resistor will remove the charging spike at the cross-over points, and further enhance the quality of the input current.

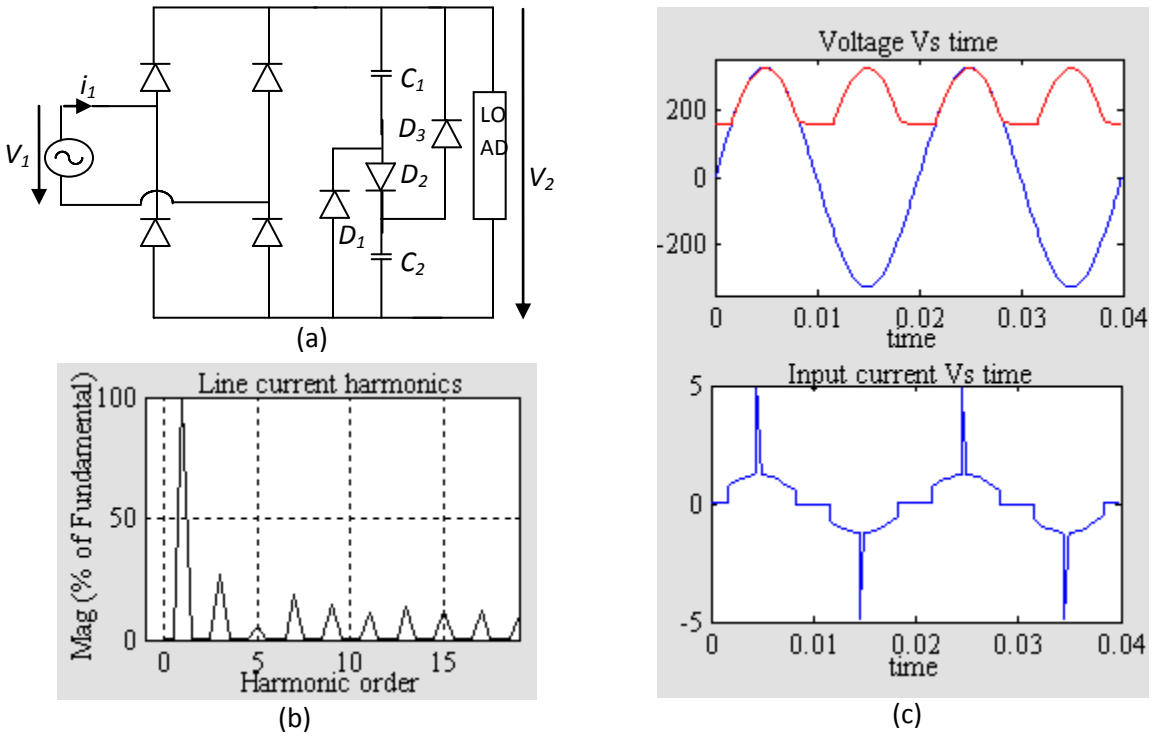


Fig.2.8 Valley-fill rectifier: (a) Schematic; (b) Line current harmonics; (c) Line voltage, output voltage, and line current with V_1=230Vrms 50Hz, resistive load R=500Ω:and C_1=C_2=470μF. The line current has Kp=0.8724, cosΦ=0.998 and PF=0.8707. The output voltage ripple is ΔV_2=168V, efficiency=0.3791.

2.2 Advantages Of Passive PFC:

Passive power factor correctors have certain advantages, such as:

1. Simplicity.
2. Reliability.
3. Ruggedness.
4. Insensitive to noises and surges.
5. No generation of high-frequency EMI.
6. No high-frequency switching losses.

2.3 Disadvantages Of Passive PFC:

On the other hand, they also have several drawbacks:

1. They have poor dynamic response.

2. Solutions based on filters are heavy and bulky, because line-frequency reactive components are used.

3. Lack voltage regulation and the shape of their input current depend on the load. Even though line current harmonics are reduced, the fundamental component may show an excessive phase shift that reduces the power factor.

Better characteristics are obtained with active PFC circuits, which are reviewed in the next chapter.

Summary:

Some of the techniques to implement "Passive PFC" have been presented in this chapter. The passive PFC circuit uses low-frequency filter components to reduce harmonics. This approach typically meets EN standards for Class-A equipment up to 250W, at a much lower cost than a comparable switch mode power supply (SMPS) employing active PFC techniques. They typically yield less PFC's compared to active topologies; they require a voltage doubler circuit for universal operation on most topologies above 150W.Better characteristics can be obtained by using "Active PFC", which will be discussed in the next chapters.

CHAPTER 3

ACTIVE PFC

Low-frequency active PFC

High-frequency active PFC

Summary

ACTIVE PFC:

An active PFC in a power electronic system controls the amount of power drawn by a load in order to obtain a power factor as close as possible to unity. In most applications, the active PFC controls the input current of the load so that the current waveform is proportional to the mains voltage waveform (a sine wave). Active switches are used in conjunction with reactive elements in order to increase the effectiveness of the line current shaping and to obtain controllable output voltage. The switching frequency further differentiates the active PFC solutions into two classes.

1. Low frequency active PFC:

Switching takes place at low-order harmonics of the line-frequency and it is synchronized with the line voltage.

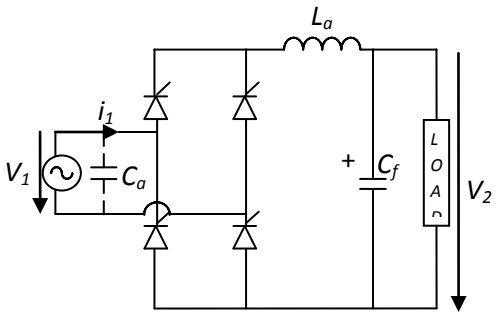
2. High frequency active PFC:

The switching frequency is much higher than the line frequency.

3.1 Low-Frequency Active PFC:

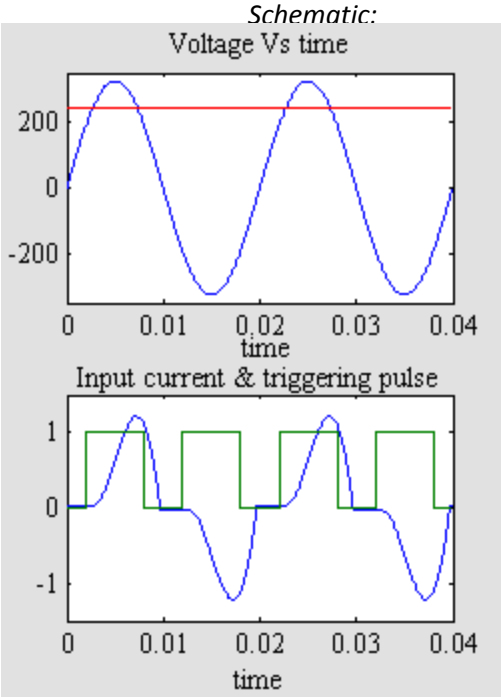
3.1.1. Phase controlled rectifier with dc-side inductor:

The phase-controlled rectifier is shown in Fig. 3.1(a), and its simulation results are shown in Figs.3.1 (b) to 3.1 (e) represents the simulation results. It is derived from the rectifier with a DC-side inductor from Fig. 2.3, where diodes are replaced with thyristors. In this solution, depending on the inductance La and the firing-angle α, near-unity purity factor K_p or displacement factor $\cos\varphi$ can be obtained [11]. The variation of power factor with respect to firing angle, for different values of inductance and vice versa are shown in Fig.3.1(c).However, the overall power factor PF is always less than 0.8. This implies a lagging displacement factor $\cos\varphi$ is compensated for by an additional input capacitance Ca, even though it increases line current harmonics. This approach is similar to that used for the diode bridge rectifier with a DC-side inductor, which is discussed in the previous chapter.

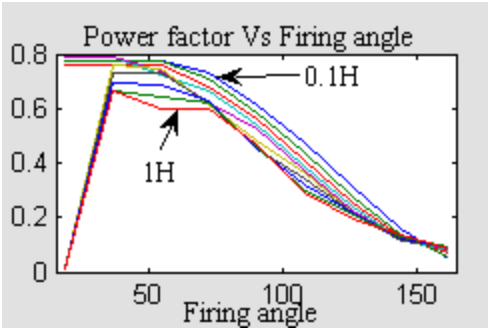


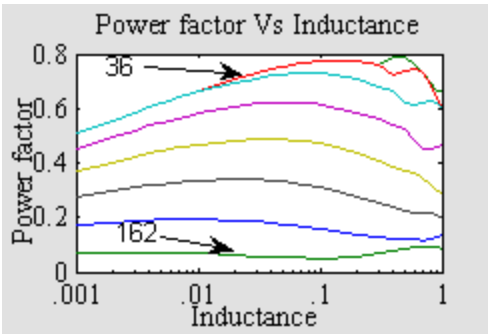
(a)

Fig. 3.1 Phase controlled rectifier. (a) Schematic:

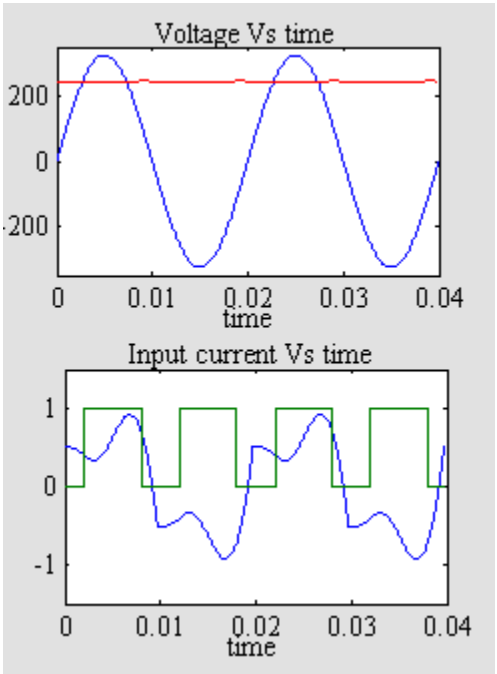


(b)

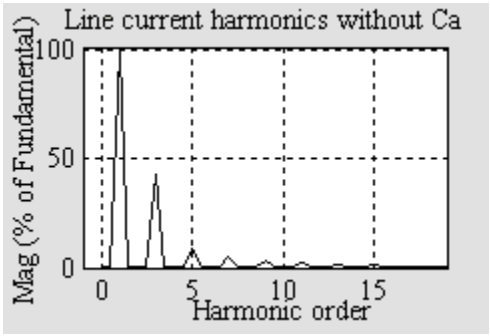


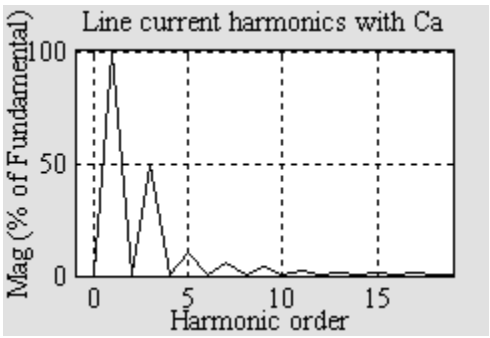


(d)



(c)





(e)

Fig. 3.1 (b) Line voltage and output voltage (upper plot) and line current (lower plot); with AC input voltage V_1=230Vrms 50Hz, resistive load R=500Ω, inductance L_a=200mH, filter Capacitance C_f=470μF and firing angle = 36 degree. Line current has K_p=0.9161, cosΦ=0.8490 and power factor=0.7778. (c) Line voltage and output voltage (upper plot) and line current (lower plot); with additional capacitance Ca. Line current has K_p=0.8892, cosΦ=0.9978 and power factor=0.8873. (d) Power factor Vs firing angle for different values of inductance (upper plot) and vice versa, (e) Line current harmonics without and with capacitance Ca.

This solution offers controllable output voltage, is simple, reliable, and uses low cost thyristors. On the negative side, the output voltage regulation is low and a relatively large inductance L_a is still required. The basic DC-DC converters can be used as active PFC. They are mainly used at high switching frequencies. However, it is also possible to use them at low switching frequencies as explained next.

3.1.2 Low frequency switching buck converter:

The low-frequency switching Buck converter is shown in Fig. 3.2(a). Fig.3.2 (b to c) represents the simulation results. Theoretically, the inductor current is constant for a near-infinite inductance L_a. The switch is turned on for the time duration Ton and the on-time intervals are symmetrical with respect to the zero crossings of the line voltage, as illustrated in Fig. 3.2(c). In this solution the power factor depends on the firing instance and duty cycle of the active switch S. For a lower harmonic content of the line current, multiple switching per line-cycle can be used. However the required inductance L_a is large and impractical.

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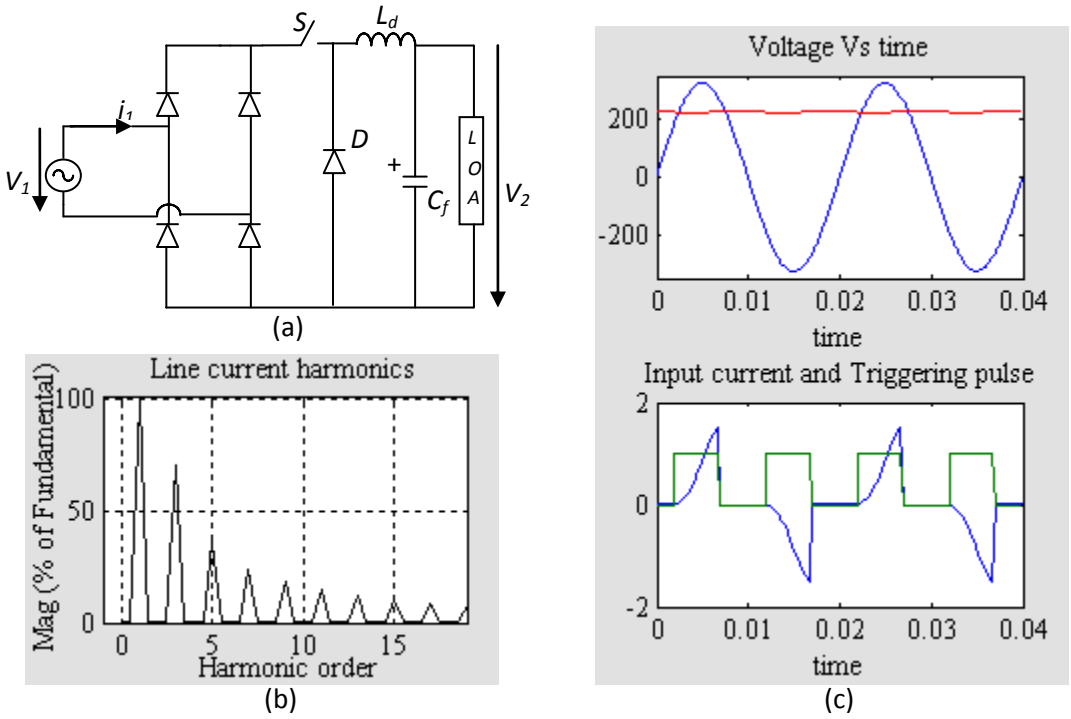


Fig.3.2 Low-frequency switching buck converter. a) Schematic; b) Line current harmonics; c) Line voltage and output voltage and line current and firing pulse (lower plot) for AC input voltage Vin=230Vrms 50Hz, filter Capacitance C_f=470µF, resistive load R=500Ω,Inductance L_d=200mH. Firing instance 2msec (i.e. 36 degree) and duty cycle=50% and the line current has K_p=0.7468, cosΦ=0.9870 and power factor= 0.7371.

3.1.3 Low-frequency switching boost converter:

The low-frequency switching Boost converter and its simulation results are shown in Fig. 3.3. The active switch S is turned on for the duration T_{on}, so as to enlarge the conduction interval of the rectifier diodes. It is also possible to have multiple switching per half line-cycle, at low switching frequency, in order to improve the shape of the line current. Nevertheless, the line current has a considerable ripple.

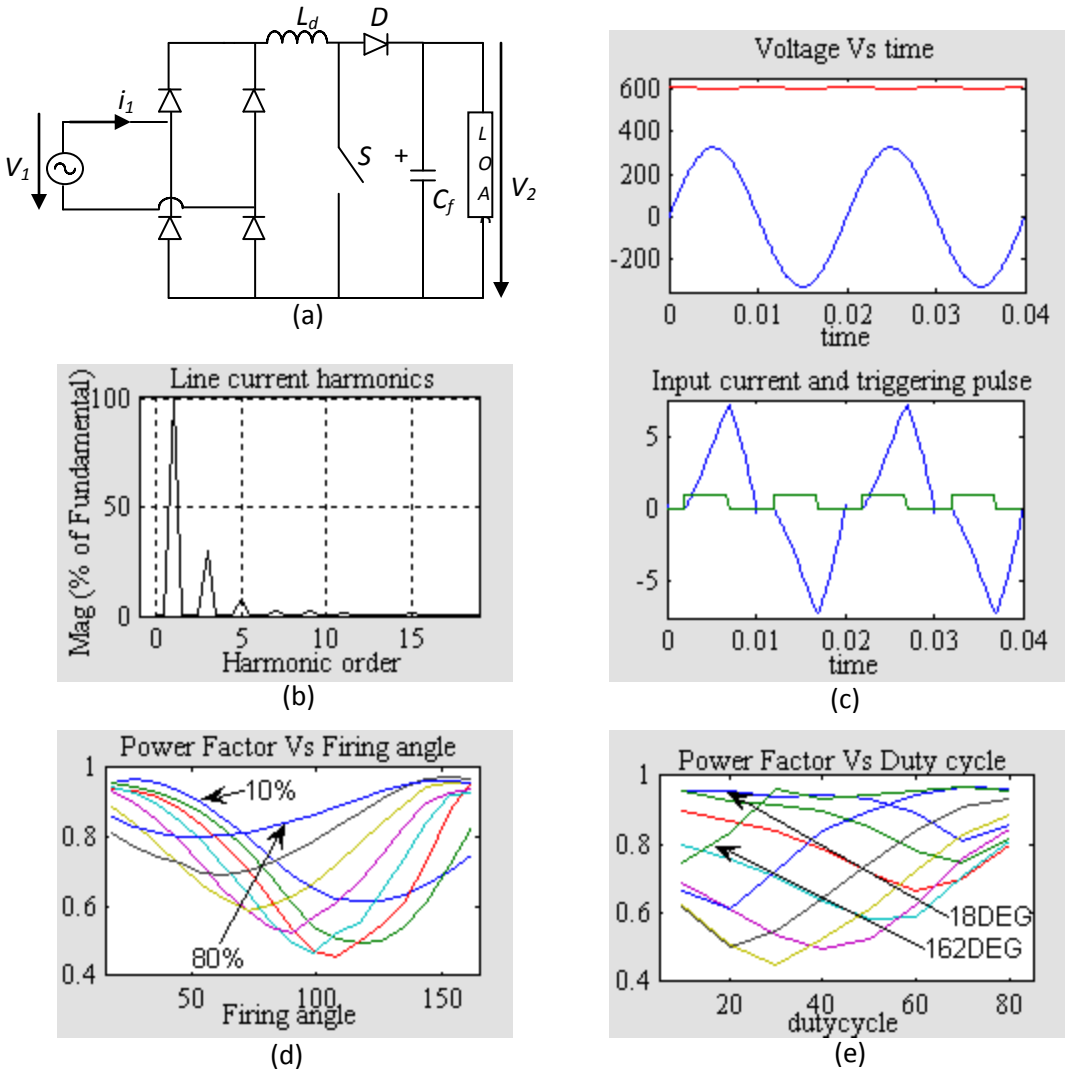


Fig.3.3 Low-frequency switching boost converter. (a) Schematic; (b) Line current harmonics; (c) Line voltage, output voltage (upper plot), line current and firing pulse (lower plot); for AC line voltage V_1=230V_{rms} 50Hz, resistive load R=500Ω, C_f=470μF, L_d=200mH and firing angle 36^0 and duty cycle=50%, the line current has K_p=0.9551, cosΦ=0.8896 and power factor=0.8497; (d) & (e) Power factor Vs firing angle for different values of duty cycles and vice versa respectively.

3.1.4 Low frequency switching buck-boost converter:

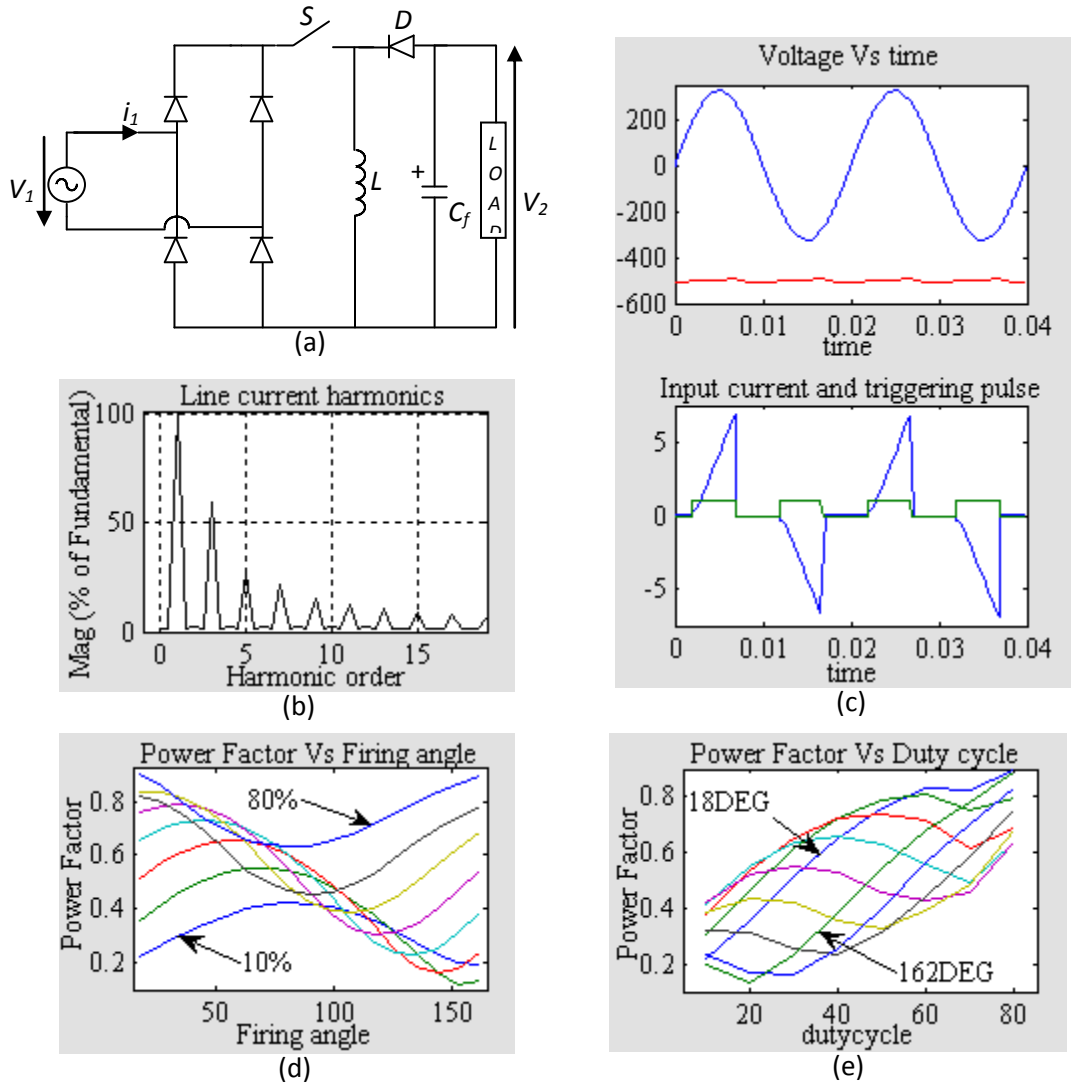


Fig.3.4 Low-frequency switching buck-boost converter.(a) Schematic;(b)Line current harmonics; (c) Line voltage, output voltage (upper plot), line current and firing pulse (lower plot); for AC line voltage V_1=230V_{rms} 50Hz, resistive load R=500Ω, C_f=470μF, L=200mH and firing angle 36^0 and duty cycle=50%, the line current has K_p= 0.7938, cosΦ= 0.9924 and power factor= 0.7878; (d) & (e) Power factor Vs firing angle for different values of duty cycles and vice versa respectively.

The low-frequency switching Buck-Boost converter is shown in Fig. 3.4. The active switch *S* is turned on for the duration T_{on}, so as to enlarge the conduction interval of the rectifier diodes. It is also possible to have multiple switching per half line-cycle, at low switching frequency, in order to improve the shape of the line current. Nevertheless, the line current has a considerable ripple.

Low-frequency switching PFC offers the possibility to control the output voltage in certain limits. In such circuits, switching losses and high-frequency EMI are negligible. However, the reactive elements are large and the regulation of the output voltage is slow.

3.2 HIGH-FREQUENCY ACTIVE PFC:

Active high frequency power factor correction makes the load behave like a resistor leading to near unity load power factor and the load generating negligible harmonics. The input current is similar to the input voltage waveform's wave shape.

The PFC stage can be realized by using a diode bridge and a DC/DC converter with a switching frequency much higher than the line-frequency. In principle, any DC/DC converter can be used for this purpose, if a suitable control method is used to shape its input current or if it has inherent PFC properties. Regardless of the particular converter topology that is used, the output voltage carries a ripple on twice the line-frequency. This is because, on the one hand, in a single-phase system the available instantaneous power varies from zero to a maximum, due to the sinusoidal variation of the line voltage. On the other hand, the load power is assumed to be constant. The output capacitor of the PFC stage buffers the difference between the instantaneous available and consumed power, hence the low-frequency ripple. In this thesis, the application of only "*second-order switching converter*" for PFC will be presented.

3.2.1 Second-order switching converters applied to PFC:

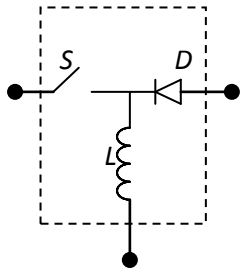


Fig. 3.5 First-order switching cell

The first-order switching cell is shown in Fig.3.5. The active switch *S* is controlled by an external control input. In a practical realization, this switch would be implemented, for example, by a MOSFET or an IGBT. The state of the second switch, which is diode *D*, is indirectly controlled by the state of the active switch and other circuit conditions. The switching cell also contains a storage element, which is the inductor *L*.

The basic Buck, Boost and Buck-Boost converters are generated from this switching cell. Considering also the output filtering capacitor, they are second-order circuits. The output filtering capacitor can be assimilated to a voltage source. Hence, the ports of the switching cell are connected to voltage sources, a fact which explains why the storage element of the switching cell is an inductor and not a capacitor.

First let us describe three characteristics that are important for a PFC application, which are dependent mainly on the specific topology. In a PFC application, the input voltage is the rectified line voltage, $V_1(t) = V_1.Sin(w_L t)$, and the output voltage V_2 is assumed to be constant.

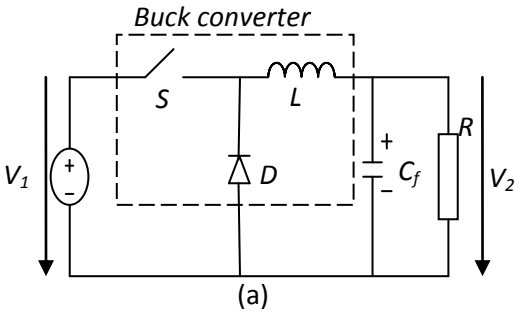
The first characteristic, which is determined by the conversion ratio of the converter, is the relation between the obtainable output voltage V_2 and the amplitude V_1 of the sinusoidal input voltage.

The second characteristic refers to the shape of the filtered (line-frequency) input current. If the converter is able to operate throughout the entire line-cycle, a sinusoidal line current can be obtained. Otherwise the line current is distorted, being zero in a region around the zero-crossings of the line voltage where the converter cannot operate.

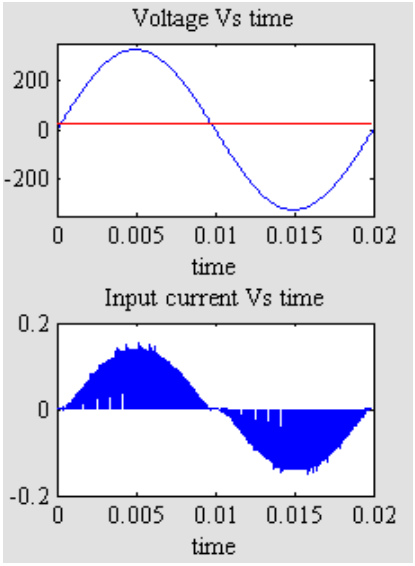
The third characteristic is related to the high-frequency content of the input current. We consider that the input current is continuous if it is not interrupted by a switching action. This means that if the inductor is placed in series at the input, then only the inductor current ripple determines the high-frequency content of the input current. Conversely, the input current is discontinuous if it is periodically interrupted by the switching action of a switch placed in series at the input. In such a case, the high-frequency content of the input current is large. Now second-order converters will be briefly characterized in the light of these topology-specific characteristics without any feedback controller.

3.2.1.1 Buck converter:

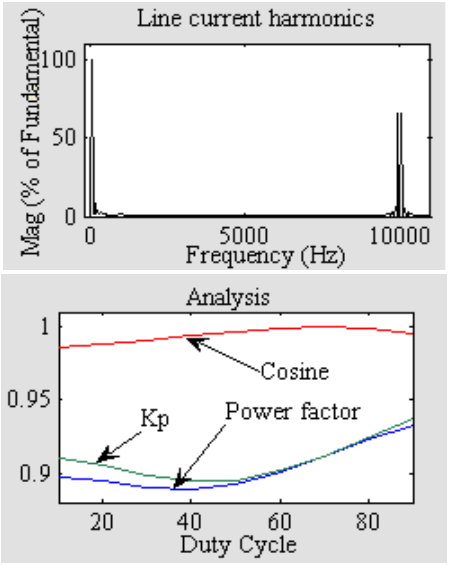
The Buck converter, shown in Fig. 3.6, together with the simulation results has step-down conversion ratio. Therefore, it is possible to obtain an output voltage V_2 lower than the amplitude V_1 of the input voltage. However, the converter can operate only when the instantaneous input voltage v_1 is higher than the output voltage V_2, i.e. only during the interval $\omega_L t \in (\alpha, \pi - \alpha)$, where $\alpha = \sin^{-1}(V_2/V_1)$ Hence, the line current of a power factor corrector based on a Buck converter has crossover distortions. Moreover, the input current of the converter is discontinuous.



(a)



(b)



(c)

Fig.3.6 High-frequency switching buck converter. (a) Schematic; (b) Line voltage, output voltage (upper plot), Line current (lower plot); for AC input voltage V_{in}=230V_{rms}, inductance L=200mH, filter Capacitance C_f=470µF, resistive load R=500Ω, and triggering pulse: switching frequency f_s=10 kHz. And line current has K_p=0.9591, cosΦ=0.9975 and PF=0.9367. (c) Line current harmonics (upper plot) and Variation of different parameters as a function of duty cycle of active switch (lower plot).

3.2.1.2 Boost converter:

The Boost converter is shown in Fig. 3.7. It has a step-up conversion ratio; hence the output voltage V_2 is always higher than the amplitude V_1 of the input voltage. Operation is possible throughout the line-cycle so the input current does not have crossover distortions. As illustrated in Fig. 3.7(b), the input current is continuous, because the inductor is placed in series at the input. Hence, an input current with reduced high-frequency content can be obtained when operating in continuous conduction mode. For these reasons, the Boost converter is widely used for PFC.

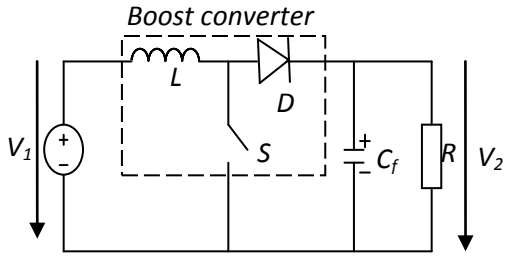
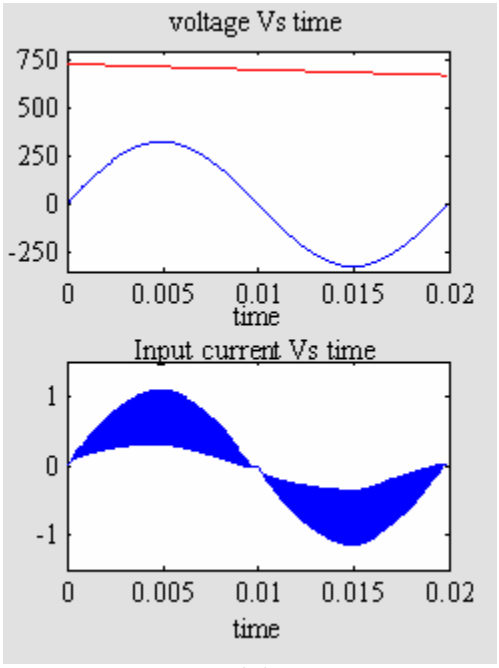
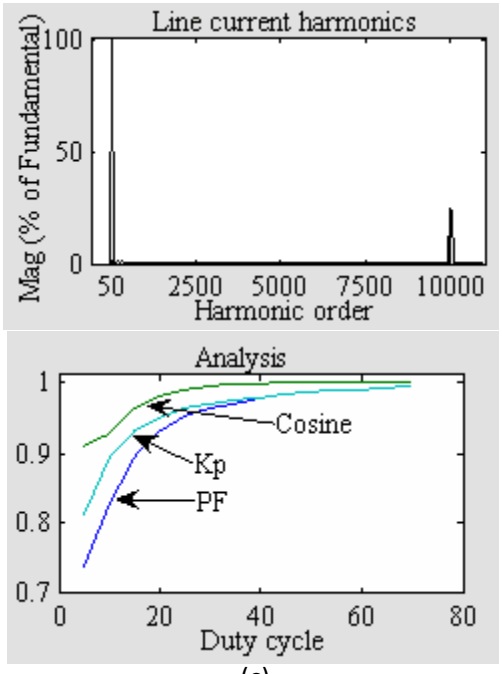


Fig. 3.7 High-frequency switching boost converter. (a) Schematic;



(b)



(c)

Fig. 3.7 (continued...) High-frequency switching boost converter. (b) Line voltage, output voltage (upper plot) and Line current (lower plot); for AC input voltage V_{in}=230Vrms, inductance L=200mH, filter capacitance C_f=470µF, resistive load R=500Ω and triggering pulse: switching frequency f_s=10kHz and duty cycle=50%. Line current has Kp= 0.9857, cosΦ=0.9999 and PF=0.9856. (c) Line current harmonics (upper plot) and variation of different parameters as a function of duty cycle of active switch (lower plot).

3.2.1.3 Buck-boost converter:

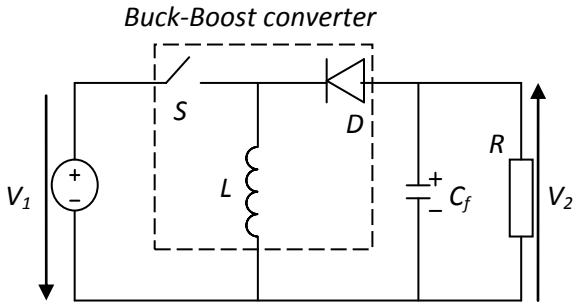
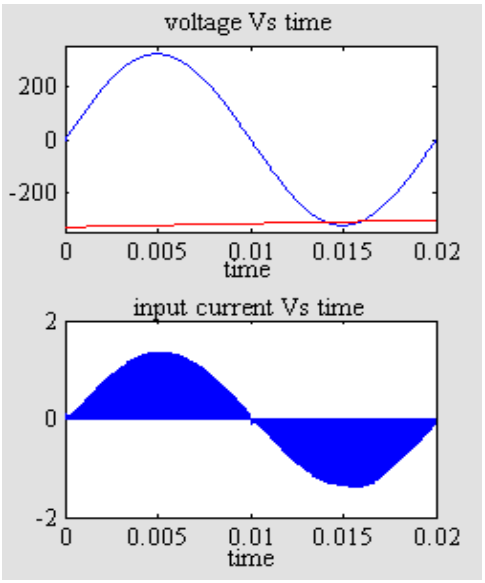
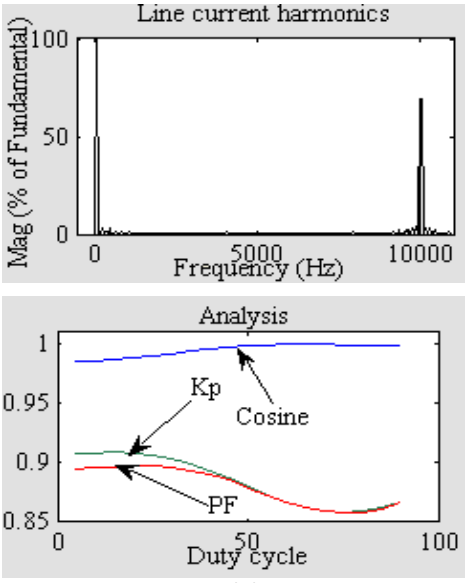


Fig. 3.8 High-frequency switching buck-boost converter. (a) Schematic.

The Buck-Boost converter, shown in Fig.3.8, can operate either as a step-down or a step-up converter. This means that the output voltage V_2 can be higher or lower than the amplitude V_1 of the input voltage, which gives freedom in specifying the output voltage. Operation is possible throughout the line-cycle and a sinusoidal line current can be obtained. However, the output voltage is inverted, which translates into higher voltage stress for the switch. Moreover, similar to the buck converter, the input current is discontinuous with significant high-frequency content, as illustrated in Fig. 3.8.



(b)



(c)

Fig. 3.8 (continued…) High-frequency switching buck-boost converter. (b) Line voltage, output voltage (upper plot) and line current (lower plot); for AC input voltage V_{in}=230V_{rms}, inductance L=200mH, filter capacitance C_f=470µF, resistive load R=500Ω and Triggering pulse: switching frequency f_s=10kHz, duty cycle =50%.Line current has Kp=0.88, cosΦ=0.9989 and PF= 0.8790. c) Line current harmonics (upper plot) and variation of different parameters as a function of duty cycle of active switch (lower plot).

The topology-specific characteristics are summarized in Table 3.1.

Table 3.1. Topology-specific characteristics.

	Conversion characteristic	Crossover distortion	Input current
Buck converter	Step-down $V_2<V_1$	Yes, because operation is possible only for $\omega_L t \in (\alpha, \pi-\alpha)$ where $\alpha=sin^{-1}(V_2/V_1)$	Discontinuous
Boost converter	Step-up, $V_2>V_1$	No	Continuous
Buck-boost	Step-down/up	No	Discontinuous

The converters can operate in Continuous Inductor Current Mode – CICM, where the inductor current never reaches zero during one switching cycle, or Discontinuous Inductor Current Mode - DICM, where the inductor current is zero during intervals of the switching cycle, which will be discussed in the next chapters.

Summary:

The preferable type of PFC is Active Power Factor Correction (Active PFC) since it provides more efficient power frequency. Because Active PFC uses a circuit to correct power factor, Active PFC is able to generate a theoretical power factor of over 95%. Active Power Factor Correction also markedly diminishes total harmonics, automatically corrects for AC input voltage, and is capable of a full range of input voltage. Since Active PFC is the more complex method of Power Factor Correction, it is more expensive to produce an Active PFC power supply.

Some of the techniques to implement "*Low-frequency switching active PFC*" have been presented in this chapter. An active low frequency approach can be implemented up to about

1000 watts. Power factors as high as 0.95 can be achieved with an active low frequency design. To conclude, low-frequency switching PFC offers the possibility to control the output voltage in certain limits. In such circuits, switching losses and high-frequency EMI are negligible. However, the reactive elements are large and the regulation of the output voltage is slow.

Nearly unity power factor can be obtained by "*high-frequency switching active PFC*", if a suitable control method is used to shape its input current or if it has inherent PFC properties. The converters can operate in Continuous Inductor Current Mode – CICM, where the inductor current never reaches zero during one switching cycle, or Discontinuous Inductor Current Mode - DICM, where the inductor current is zero during intervals of the switching cycle, which will be discussed in the next chapters.

CHAPTER 4

OPERATION IN DISCONTINUOUS

INDUCTOR CURRENT MODE – DICM

Average input resistance

Input voltage-current characteristics of basic converter topologies

Design procedure

Summary

OPERATION IN DISCONTINUOUS INDUCTOR CURRENT MODE – DICM:

In this chapter, basic types of dc-dc converter topologies are studied to investigate their self-PFC capabilities [12]. Basic types of dc-dc converters, when operating in discontinuous inductor current mode, have self power factor correction (PFC) property, that is, if these converters are connected to the rectified ac line, they have the capability to give higher power factor by the nature of their topologies. Input current feedback is unnecessary when these converters are employed to improve power factor.

This property of DICM input circuit can be called “self power factor correction” because no control loop is required from its input side. This is also the main advantage over a CICM power factor correction circuit, in which multi-loop control strategy is essential. The peak of the inductor current is sampling the line voltage automatically. However, the input inductor operating in DICM cannot hold the excessive input energy because it must release all its stored energy before the end of each switching cycle. As a result, a bulky capacitor is used to balance the instantaneous power between the input and output. In addition, if discontinuous inductor current mode is applied, the input current is normally a train of triangle pulse with nearly constant duty ratio. In this case, an input filter is necessary for smoothing the pulsating input current into a continuous one. Obviously, to ensure high power factor, the average current of the pulsating current should follow the input voltage in both shape and phase.

In this operating mode, the inductor current i_L varies from zero to a maximum and returns back to zero before the beginning of the next switching cycle.

4.1 Input Voltage-Current Characteristics of Basic Converter Topologies:

In order to examine the self-PFC capabilities of the basic converters, we first investigate their input characteristics. Because the input currents of these converters are discrete when they are operating in DICM, only averaged input currents are considered. Since switching frequency is much higher than the line frequency, let’s assume the line voltage is constant in a switching cycle. In steady state operation, the output voltage is nearly constant and the variation in duty ratio is slight. Therefore, constant duty ratio is considered in deriving the input characteristics.

4.1.1 Buck converter:

The basic buck converter topology and its input current waveform when operating in DICM are shown in Fig. 4.2(a) and (b), respectively. It can be shown that the average input current in one switching cycle is given by the equation:

$$i_{1,avg}(t) = \frac{1}{T_s}\left[\frac{1}{2} DT_s \frac{v_1(t)-V_0}{L} DT_s\right] = \frac{T_s D^2}{2L} v_1(t) - \frac{T_s D^2}{2L} V_0 \qquad (4.1)$$

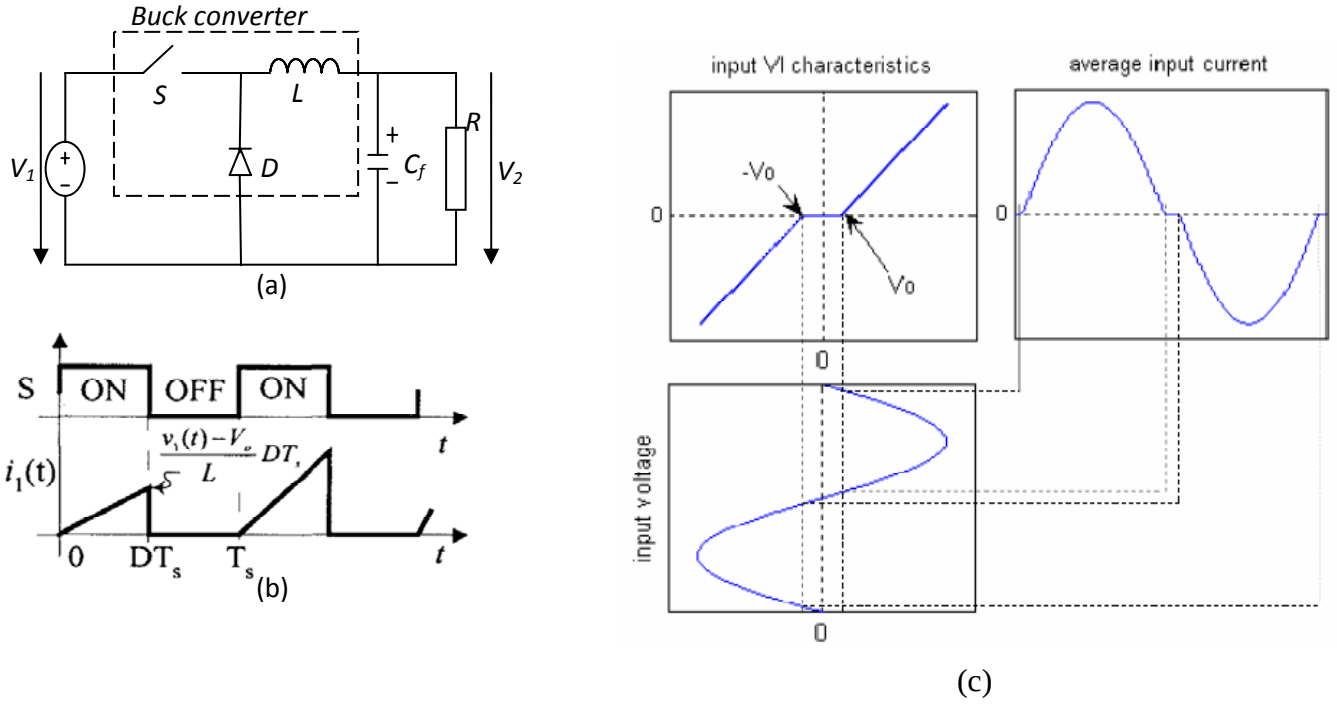


Fig.4.2 (a) Buck converter Schematic; (b) Input current, (c) Input VI Characteristic of basic buck converter operating in DICM for AC input voltage V_{in}=230Vrms, inductance L=200mH, filter Capacitance C_f=470μF, resistive load R=500 ohms.

Figure 4.2(c) shows that the input voltage-input current V-I characteristics is a straight line. It should be note that this straight line does not go through the origin. When the rectified line voltage $v_1(t)$ is less than the output voltage V_o, negative input current would occur. This is not allowed because the bridge rectifier will block the negative current. As a result, the input current is zero near the zero cross point of the line voltage, as shown in Fig.4.1(c). Actually, the input current is distorted simply because the buck converter can work only under the condition that the input voltage is larger than the output voltage. The input resistance of the Buck converter is not constant throughout the line-cycle. However, its variation decreases and “inherent” PFC property

improves, when the ratio V_2/V_1 is decreased. As explained previously, the line current has crossover distortions too, which are however less disturbing when the ratio V_2/V_1 is decreased. However, compliance with standard IEC 1000-3-2 can be obtained up to a relatively high power, when the output voltage V_2 is low enough when compared to the amplitude V_1 of the sinusoidal input voltage Therefore the basic buck converter is not a good candidate for DICM input power factor correction.

4.1.2 Boost converter:

The basic boost converter and its input current waveform are shown in Fig. 4.3(a) and (b) respectively.

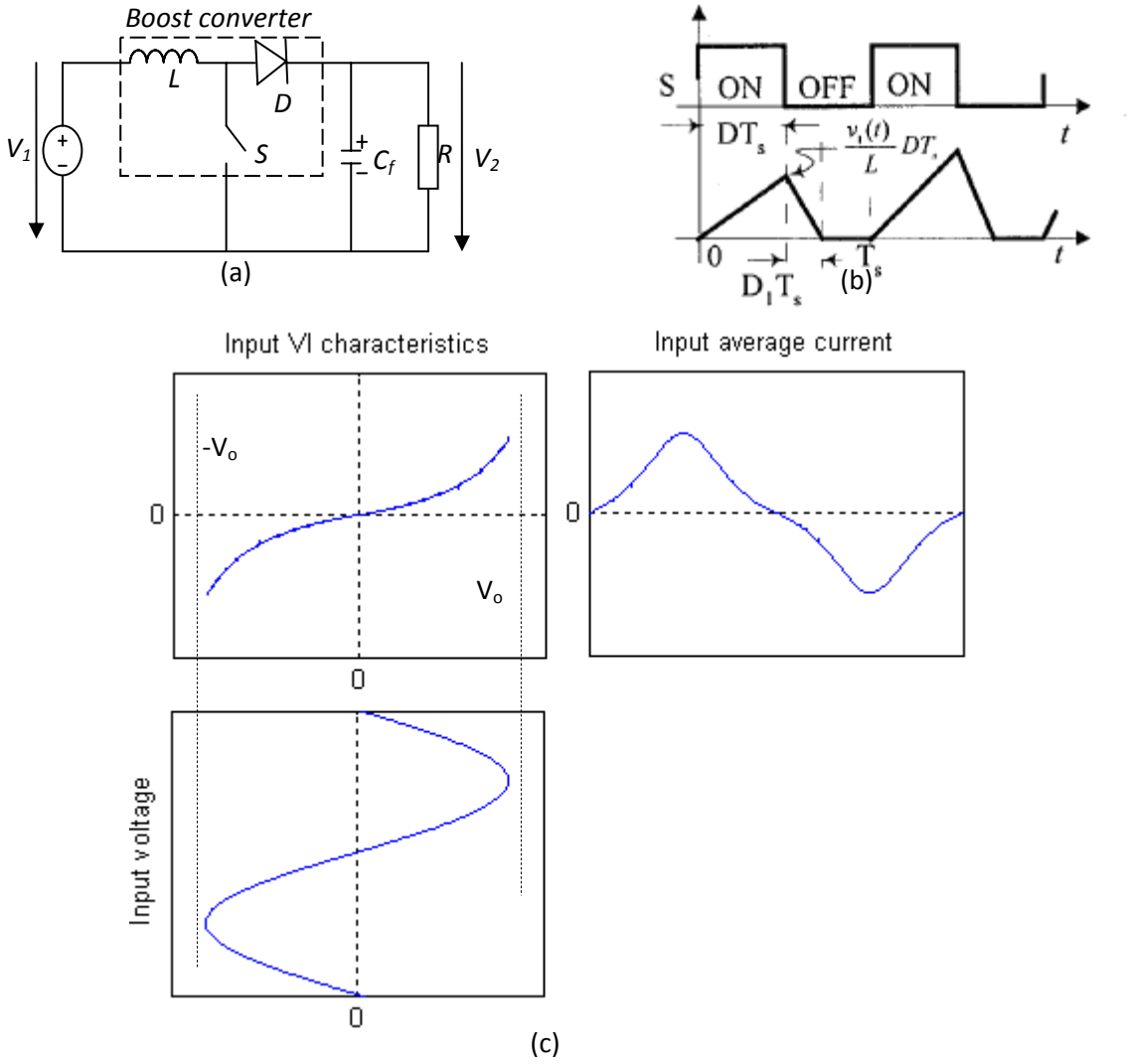


Fig.4.3 Boost converter (a) Schematic; (b) Input current; (c) Input V-I Characteristic of basic boost converter operating in DICM for AC input voltage V_{in}=230Vrms, inductance L=200mH, filter Capacitance C_f=470μF, resistive load R=500 ohms.

The input V-I characteristic of Boost converter can be found as follows:

$$i_{1,avg}(t) = \frac{1}{T_s}\left[\frac{1}{2}(D + D_1)T_s\frac{v_1(t)}{L}DT_s\right] = \frac{T_sD^2}{2L}v_1(t)\frac{1}{V_0 - v_1(t)}V_0 \quad (4.2)$$

By plotting Eq. (4.2), we obtain the input V-I characteristic curve as given in Fig.4.3(c). As we can see that as long as the output voltage is larger than the peak value of the line voltage in certain extent (depending on D_1), the relationship between v_1(t) and i_1,avg(t) is nearly linear. When the boost converter connected to the line, it will draw almost sinusoidal average input current from the line, shown as in Fig. 4.3(c).

As one might notice from Eq. (4.2) that the main reason to cause the non-linearity is the existence of D_1. Ideally, if D_1 = 0, the input V-I characteristic will be a linear one. In practice, to reduce the discharge period D1, by properly configuring the circuit topology, a higher voltage, instead of V_o, can be created to be applied to the inductor during D_1 to discharge the inductor.

The Boost converter has an imperfect "inherent" PFC property, as well. Its input resistance changes throughout the line-cycle, but the variation decreases and inherent PFC property improves when the ratio V_2/V_1 is increased. Taking into account the fact that the line current does not have crossover distortions, compliance with the standard is achieved comfortably. Because of the above reasons, boost converter is comparably superior to most of the other converters when applied to do PFC [13-15]. However, it should be noted that boost converter can operate properly only when the output voltage is higher than its input voltage.

4.1.3 Buck-boost converter:

Figure 4.4(a) shows a basic buck-boost converter. The averaged input current of this converter can be found according to its input current waveform, shown in Fig. 4.4(b).

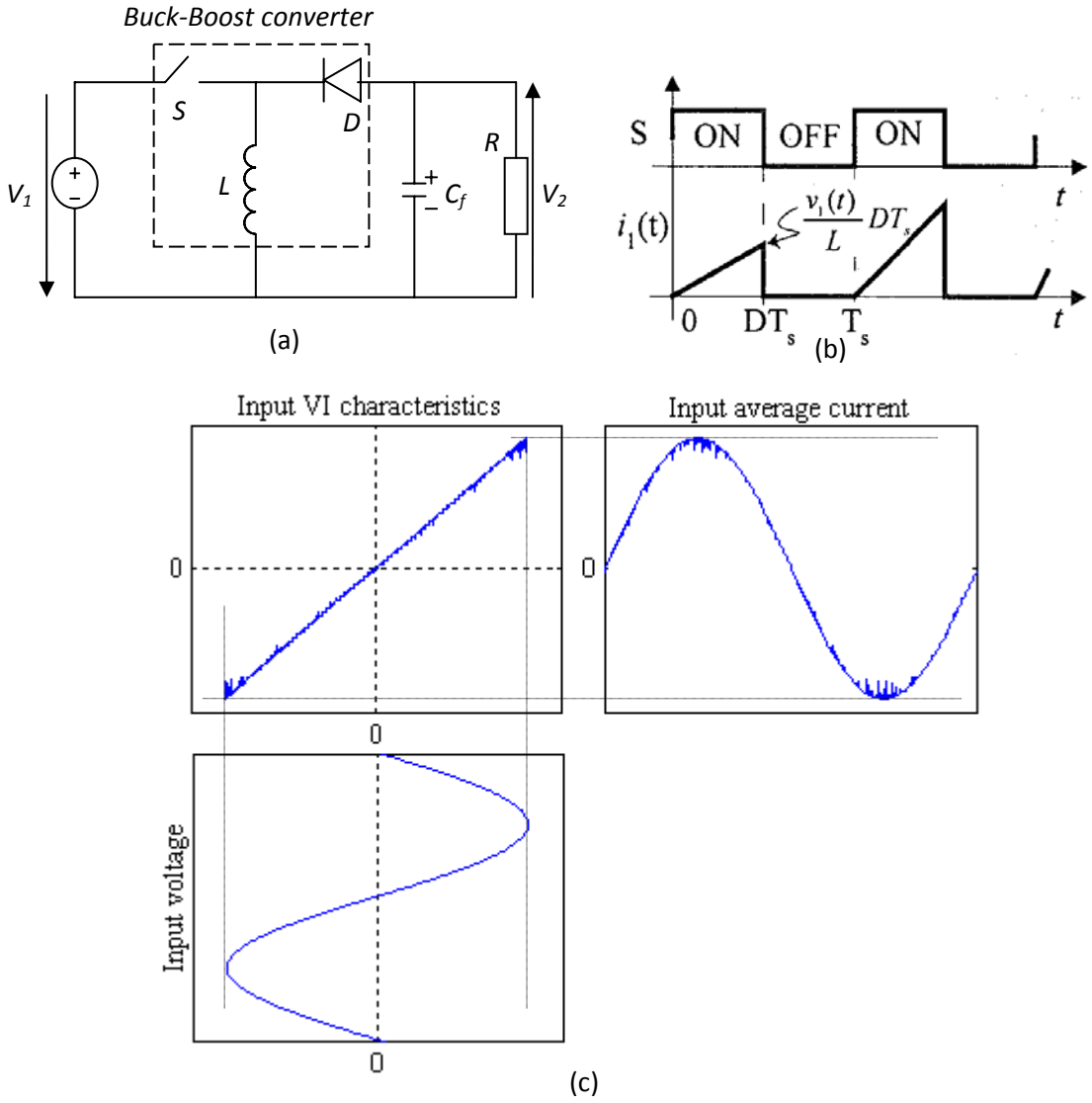


Fig. 4.4 Buck-boost converter. (a) Schematic; (b) Input current; (c) Input V-I Characteristic of basic boost converter operating in DICM for AC input voltage V_{in}=230Vrms,inductance L=200mH, filter Capacitance C_f=470μF, resistive load R=1000 ohms.

For this converter the average current is :

$$i_{1,avg}(t) = \frac{T_s D^2}{2L} v_1(t) \qquad (4.3)$$

Equation (4.3) gives a perfect linear relationship between $i_1$avg(t) and v_1(t) which proves that a buck-boost has excellent self-PFC property. This is because the input current of buck-boost converter does not related to the discharging period D_1. Its input V-I characteristics and input Voltage and current waveforms are shown in Fig.4.4(c).

The input resistance of the Buck-Boost converter depends only on inductance L, switching period Ts and duty-cycle d. If operation in DICM is ensured throughout the line-cycle and if d is kept constant, then the input resistance r1 is constant. As a consequence, the average input current ($i_1(t)_{T_s}$) tracks the shape of the input voltage and the converter has an "inherent" PFC property. In contrast to CICM operation, in DICM there is no need for the controller to adjust the duty-cycle over the line-cycle to perform PFC. Furthermore, because the output voltage of buck-boost converter can be either larger or smaller than the input voltage, it demonstrates strong availability for DICM input technique to achieve power factor correction. So, theoretically buck-boost converter is a perfect candidate. Unfortunately, this topology has two limitations:

1) The polarity of its output voltage is reversed, i.e., the input voltage and the output voltage don't have a common ground; and

2) It needs floating drive for the power switch. The first limitation circumscribes this circuit into a very narrow scope of applications.

As a result, it is not widely used.

4.2 Design Procedure:

4.2.1 Summary: Mode boundary

$K > K_{crit}(D)\ or\ R < R_{crit}(D)$ for CICM

$K < K_{crit}(D)\ or\ R > R_{crit}(D)$ for DICM

Table 4.2 CICM-DICM mode boundaries for the buck, boost, and buck-boost converters.

CONVERTER	$K_{crit}(D)$	$\max_{0 \le D \le 1}(K_{crit})$	$R_{crit}(D)$	$\max_{0 \le D \le 1}(R_{crit})$
Buck	$(1-D)$	1	$\frac{2L}{(1-D)T_S}$	$2\frac{L}{T_S}$
Boost	$D(1-D)^2$	4/27	$\frac{2L}{D(1-D)^2 T_S}$	$\frac{27}{2}\frac{L}{T_S}$
Buck-boost	$(1-D)^2$	1	$\frac{2L}{(1-D)^2 T_S}$	$2\frac{L}{T_S}$

The main advantage of using switching converters operating in DICM for PFC applications is the simplicity of the control method. Since there is no need to continuously adjust the duty-cycle D to perform PFC, only a voltage loop is needed to regulate the voltage across the storage capacitor. The bandwidth of the voltage loop has to be low (e.g. 10-15Hz),in order to filter out the output voltage ripple at twice the line-frequency. The simple control of converters with inherent PFC makes them attractive for low-cost applications.

But the main disadvantage of using switching converters operating in DICM for PFC application is the input current is normally a train of triangle pulse with nearly constant duty ratio. As a result the high-frequency EMI is very high. In this case, an input filter is necessary for smoothing the pulsating input current into a continuous one.

Summary:

According to the above discussion, we may conclude that the basic boost converter and buck-boost converter have excellent self-PFC capability naturally. Among them, boost converter is especially suitable for DICM PFC usage. Hence, this converter is the most preferable by the designers for power factor correction purpose. Other converters may be used only if their input V-I characteristics have been modified (linearized), or when they operate in continuous inductor conduction mode, which will be discussed in the next chapter.

In addition, if discontinuous inductor current mode is applied, the input current is normally a train of triangle pulse with nearly constant duty ratio. In this case, an input filter is necessary for smoothing the pulsating input current into a continuous one.

CHAPTER 5

Operation In Continuous Inductor Current Mode – CICM

Control scheme for CICM operation

Peak current control

Average current mode control

Hysteresis control

Borderline control

Simulation results

Summary

OPERATION IN CONTINUOUS INDUCTOR CURRENT MODE – CICM:

The DC-DC converters can operate in Continuous Inductor Current Mode – CICM, where the inductor current never reaches zero during one switching cycle. In CICM, different control techniques are used to control the inductor current. Some of them are (1) peak current control (2) average current control (3) Hysteresis control (4) borderline control. These control techniques specifically developed for PFC boost converters are analyzed.

5.1 CONTROL SCHEME FOR CICM OPERATION:

In this operating mode, the inductor current never reaches zero during one switching cycle and there is always energy stored in the inductor. The volt-seconds applied to the inductor must be balanced throughout the line-cycle by continuously changing the duty-cycle of the converter using an appropriate control method.

An example of a control scheme is shown in Fig. 5.1. The low-bandwidth outer loop with characteristic G_L(s) is used to keep the output voltage of the PFC stage constant and to provide the error signalv_ε. The high-bandwidth inner loop with characteristic G_H(s) is used to control the input current. A multiplier is used to provide a referencev_{xy}, which is proportional to the error signal v_ε and which has a modulating signal with the desired shape for the input current.

Fig. 5.1 shows the most common situation, where the modulating signal is the rectified-sinusoid input voltage v_1. Depending on the topology of the PFC stage, it may be beneficial to use as a modulating signal the difference between the input voltage and the output voltage. The control circuit can be simplified by eliminating the multiplier and the sensing of the line voltage. In this case the modulating signal is $v_{xy} = v_\varepsilon$, and it is essentially constant over the line cycle, because v_ε is the control signal from the low-bandwidth output voltage controller. Therefore, the input current is clamped to a value proportional with v_ε and its shape approaches a square waveform. The simplification of the control circuit leads to a more 48 distorted line current, but compliance with the standard can be obtained up to approximately 500W for a 230Vrms input voltage. Furthermore, if the edges of the line current waveform are softened, thus obtaining a nearly trapezoidal waveform, compliance up to several kW can be obtained.

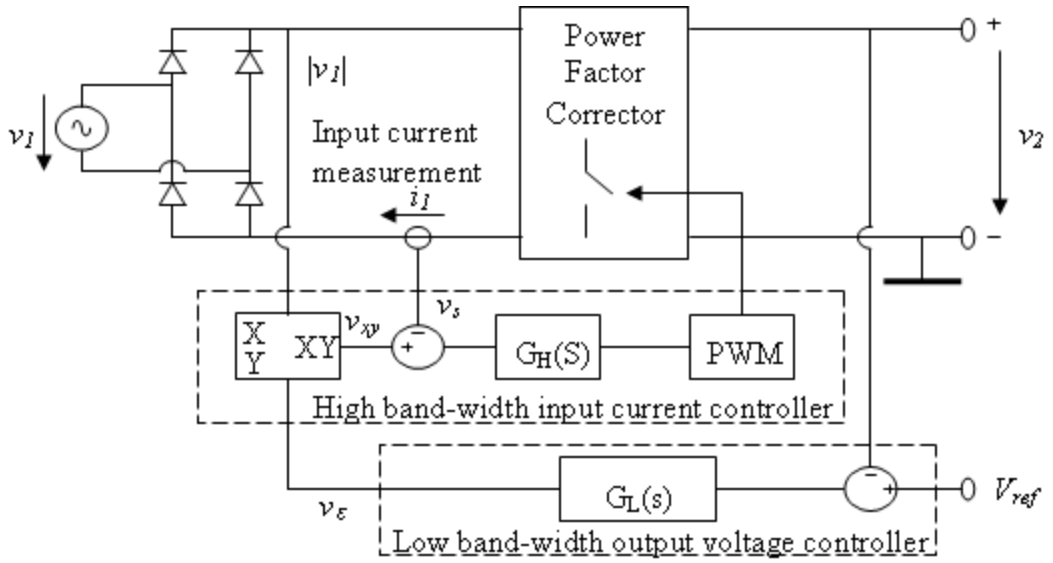


Fig. 5.1 Control scheme for PFC using a switching converter operating in CICM.

There are several ways to implement the high-bandwidth inner loop [16] [5], [17]. Some of them are:

1. Peak current control.
2. Average current control.
3. Hysteresis control.
4. Borderline control.

Even though these control techniques can be used for all DC-DC converters, only boost converter has been taken for the study because of the continuous input current. The boost converter is designed for an input voltage, V=230Vrms, output voltage Vo=500V dc, resistive load R=500 ohm, at switching frequency 10kHz. The design values of filter capacitor C_L and filter inductor L are:

$$L = \frac{(V_O - V)\times T}{2 * \Delta i_{in}} = \frac{(500 - 111.47)\times 0.1\times 10^{-3}}{2\times 0.1} = 194.5\times 10^{-3} H$$

$$C_L = \frac{\Delta\, i_{in} \times T}{8 * \Delta\, V} = \frac{0.2 \times 0.1 \times 10^{-3}}{8 \times .05} = 250 \times 10^{-6} F$$

5.2 PEAK CURRENT CONTROL [A1]:

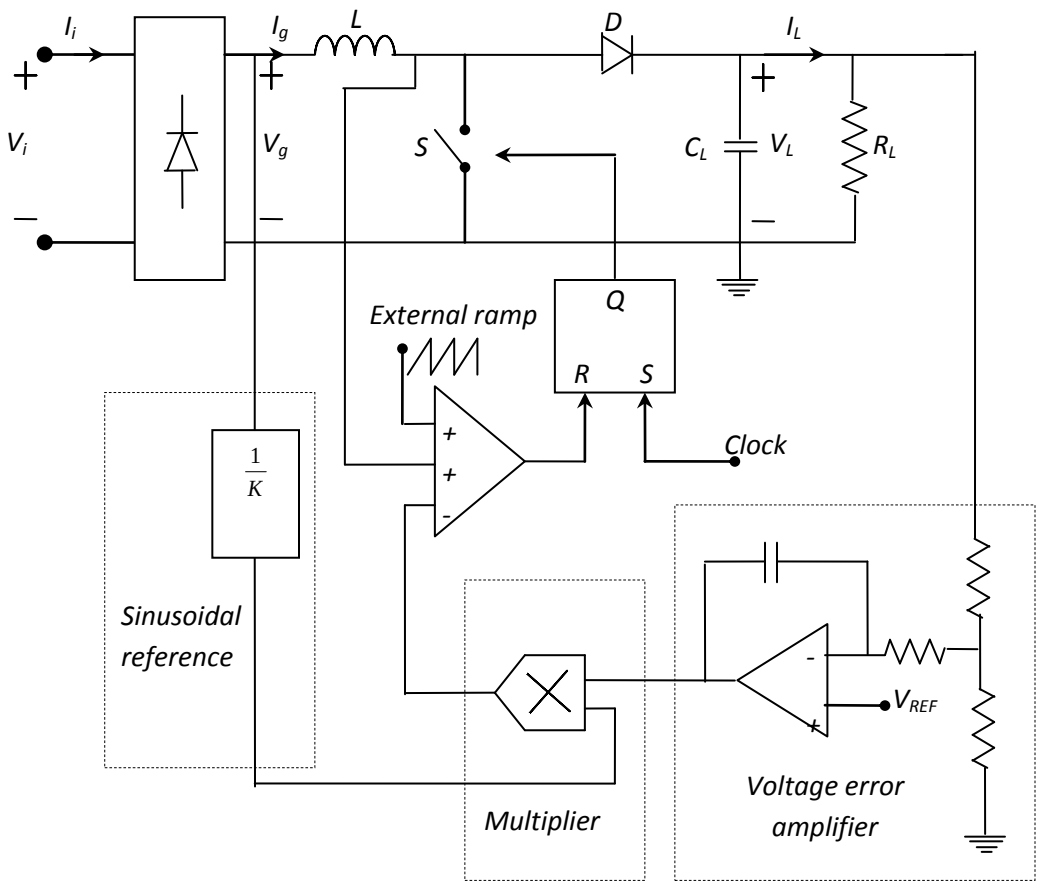
The basic scheme of the peak current controller is shown in Fig. 5.2, together with a typical input current wave form. As we can see, the switch is turned on at constant frequency by a clock signal, and is turned off when the sum of the positive ramp of the inductor current (i.e. the switch current) and an external ramp (compensating ramp) reaches the sinusoidal current reference. This reference is usually obtained by multiplying a scaled replica of the rectified line voltage v_g times the output of the voltage error amplifier, which sets the current reference amplitude.

The power switch is closed at every positive edge of the clock signal. The inductor current increases practically linearly until it reaches the reference value I_{ref}. Then the output of the flip-flop is cleared and the switch opens. During the off-state the current i_L decreases until the next clock pulse sets the flip-flop again. Output voltage regulation is obtained by an additional feedback loop, which adjusts the current reference I_{ref} depending on the voltage deviation from the set point.

In this way, the reference signal is naturally synchronized and always proportional to the line voltage, which is the condition to obtain unity power factor. As Fig. 5.2 reveals, the converter operates in Continuous Inductor Current Mode (CICM); this means that devices current stress as well as input filter requirements are reduced.

Moreover, with continuous input current, the diodes of the bridge can be slow devices (they operate at line frequency). On the other hand, the hard turn-off of the freewheeling diode increases losses and switching noise, calling for a fast device. However, if the simplicity of the control circuit is of primary interest, rather than the quality of the line current waveform, then peak current mode control with input current clamping is attractive [19], [20].

The input current distortion can be reduced by changing the current reference wave shape, for example introducing a dc offset, and/or by introducing a soft clamp. These provisions are discussed in [21] and [18]. In [22] it is shown that even with constant current reference, good input current waveforms can be achieved. Moreover, if the PFC is not intended for universal input operation, the duty-cycle can be kept below 50% so avoiding also the compensation ramp.



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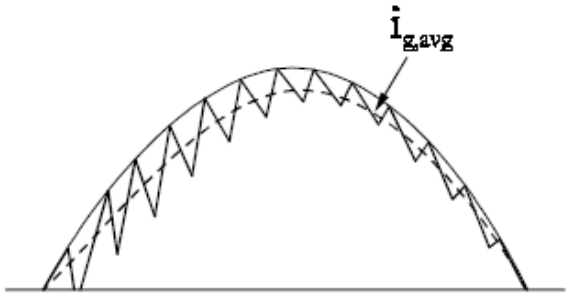


(b)

Fig. 5.2 Peak current control scheme.

5.2.1 Advantages:

1. Constant switching frequency.
2. Only the switch current must be sensed and this can be accomplished by a current transformer,

thus avoiding the losses due to the sensing resistor.

3. No need of current error amplifier and its compensation network.
4. Possibility of a true switch current limiting.
5. As there is an instantaneous pulse-by-pulse current limit, the reliability is improved and the response speed is increased.

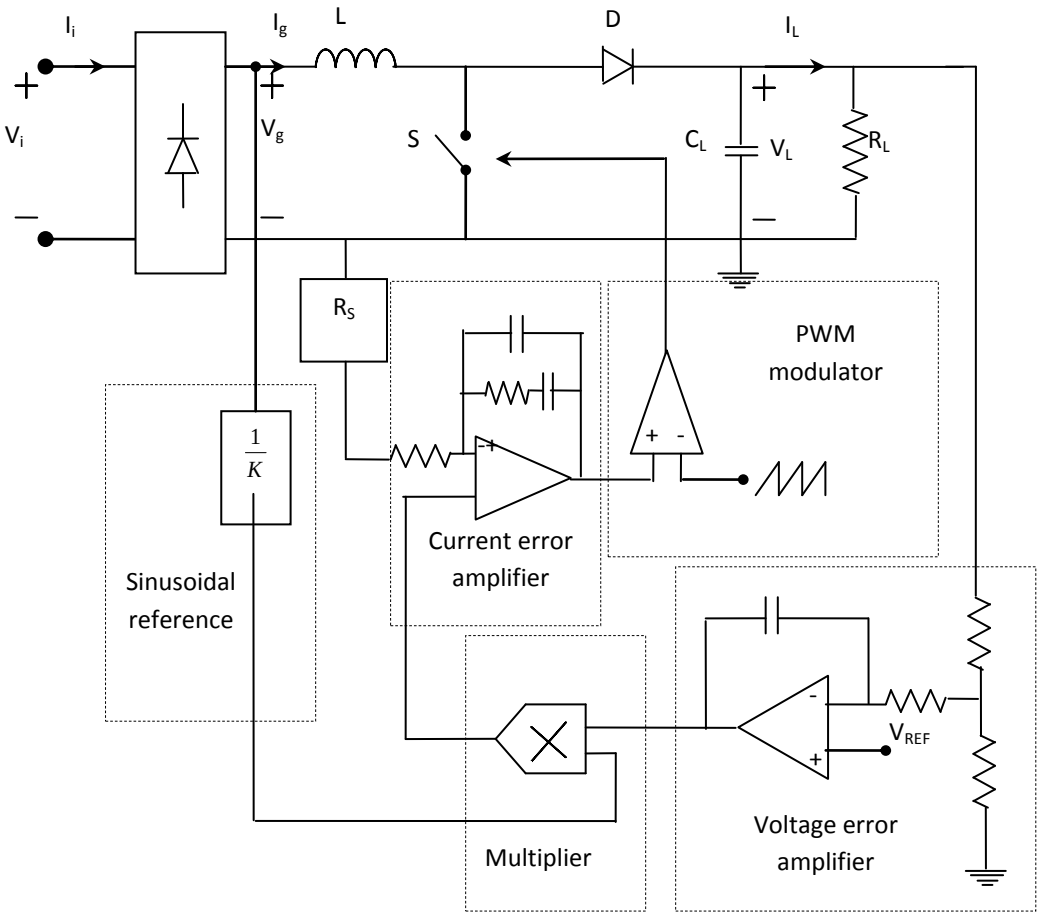
5.2.2 Disadvantages:

1. Presence of sub-harmonic oscillations at duty cycles greater than 50%, so a compensation ramp is needed.
2. Input current distortion which increases at high line voltages and light load and is worsened by the presence of the compensation ramp [21], [18].

5.3 AVERAGE CURRENT MODE CONTROL:

Another control method, which allows a better input current waveform, is the average current control represented in Fig.5.3 [21, 23-25]. Here the inductor current is sensed and filtered by a current error amplifier whose output drives a PWM modulator. In this way the inner current loop tends to minimize the error between the average input current ig and its reference. This latter is obtained in the same way as in the peak current control.

The converter works in CICM, so the same considerations done with regard to the peak current control can be applied. The technique of average current mode control overcomes the problems of peak current mode control by introducing a high gain integrating current error amplifier (CA) into the current loop. The gain-bandwidth characteristic of the current loop can be tailored for optimum performance by the compensation network around the CA. Compared with peak current mode control, the current loop gain crossover frequency fc, can be made approximately the same, but the gain will be much greater at lower frequencies.



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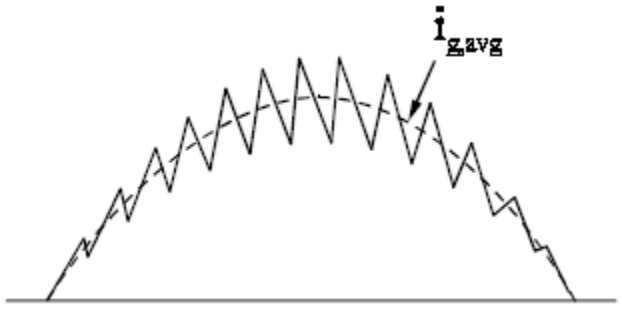

(b)

Fig.5.3 Average current control scheme.

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The results are:

1. Average current tracks the current program with a high degree of accuracy. This is especially important in high power factor pre-regulators, enabling less than 3% harmonic distortion to be achieved with a relatively small inductor. In fact, average current mode control functions well

even when the mode boundary is crossed into the discontinuous mode at low current levels. The outer voltage control loop is oblivious to this mode change.

2. Slope compensation is not required, but there is a limit to loop gain at the switching frequency in order to achieve stability.

3. Noise immunity is excellent. When the clock pulse turns the power switch on, the oscillator ramp immediately dives to its lowest level, volts away from the corresponding current error level at the input of the PWM comparator.

4. The average current mode method can be used to sense and control the current in any circuit branch. Thus it can control input current accurately with buck and flyback topologies, and can control output current with boost and flyback topology.

5.3.1 Advantages:

1. Constant switching frequency;
2. No need of compensation ramp;
3. Control is less sensitive to commutation noises, due to current filtering;
4. Better input current waveforms than for the peak current control since, near the zero crossing of the line voltage, the duty cycle is close to one.

5.3.2 Disadvantages:

1. Inductor current must be sensed.
2. A current error amplifier is needed and its compensation network design must take into account the different converter operating points during the line cycle.

5.4 HYSTERESIS CONTROL [A3]:

Fig. 5.4 shows this type of control in which two sinusoidal current references $I_{P,ref,}$ $I_{V,ref}$ are generated, one for the peak and the other for the valley of the inductor current. According to this control technique, the switch is turned on when the inductor current goes below the lower reference $I_{V\ ref}$ and is turned off when the inductor current goes above the upper reference I_{Pref}, giving rise to a variable frequency control [26-27].In order to avoid too high switching frequency, the switch can be kept open near the zero crossing of the line voltage so introducing dead times in the line current. An analysis of the power factor as a function of these dead times can be found in [26].

5.4.1 Advantages:

1. No need of compensation ramp;

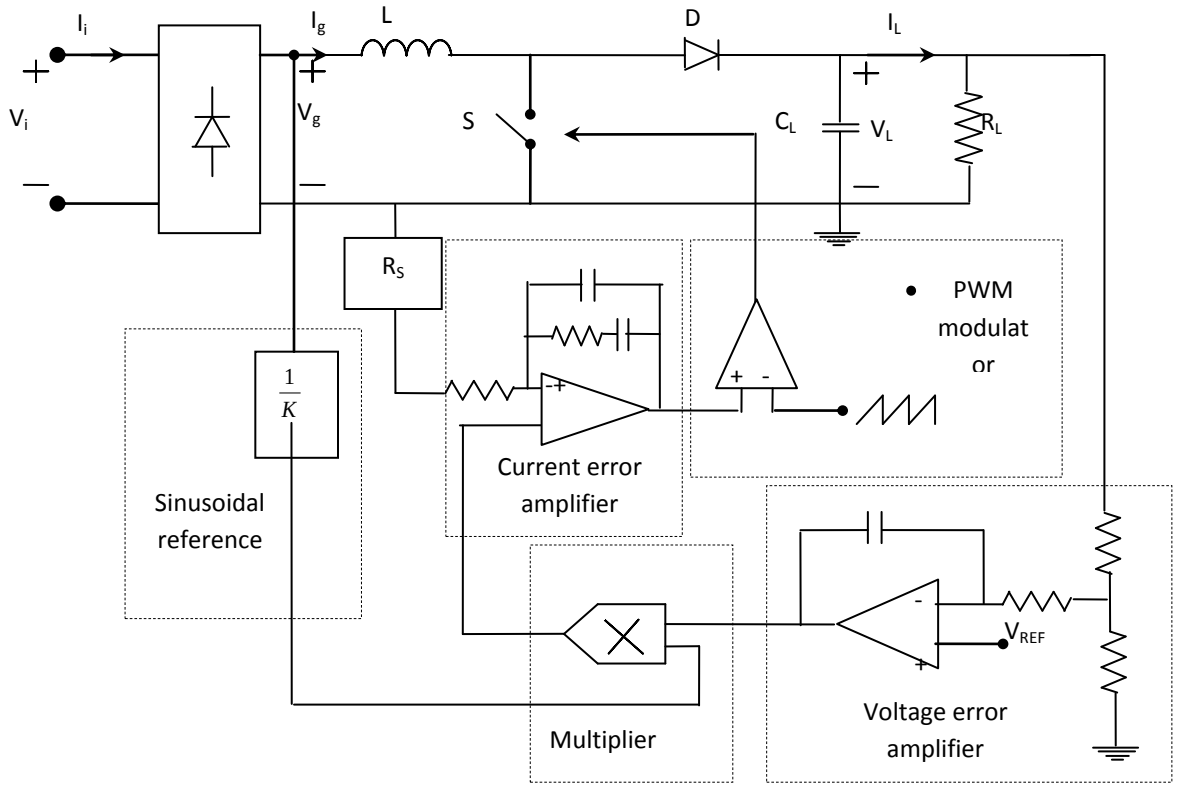
2. Low distorted input current waveforms.

5.4.2 Disadvantages:

1. Variable switching frequency;

2. Inductor current must be sensed;

3. Control sensitive to commutation noises.



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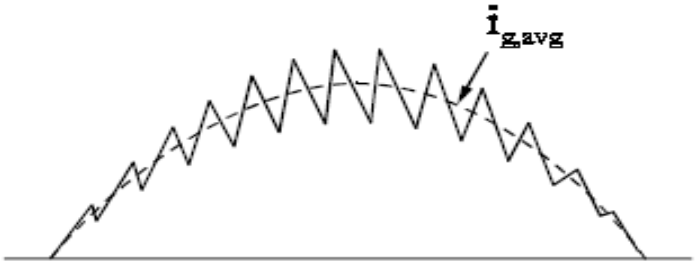


(b)

Fig. 5.4 Hysteresis control scheme.

5.5 BORDERLINE CONTROL :

In this control approach the switch on-time is held constant during the line cycle and the switch is turned on when the inductor current falls to zero, so that the converter operates at the boundary between Continuous and Discontinuous Inductor Current Mode (CICM,DICM) [28]. In this way, the freewheeling diode is turned off softly (no recovery losses) and the switch is turned on at zero current, so the commutation losses are reduced. On the other hand the higher current peaks increase device stresses and conduction losses and may call for heavier input filters (for some topologies).

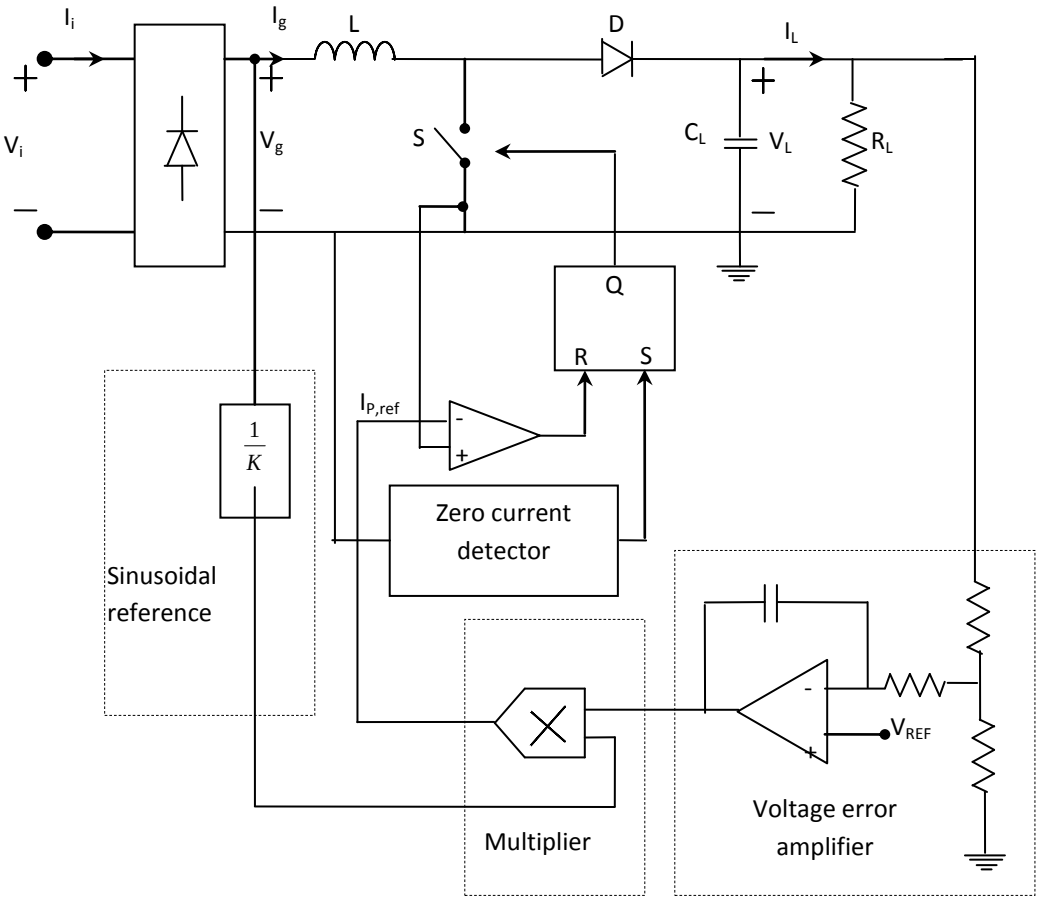
This type of control is a particular case of hysteresis control in which the lower reference I_V,ref is zero anywhere. The principle scheme is shown in Fig.5.5. The instantaneous input current is constituted by a sequence of triangles whose peaks are proportional to the line voltage. Thus, the average input current becomes proportional to the line voltage without duty-cycle modulation during the line cycle. This characterizes this control as an "automatic current shaper" technique. Note that the same control strategy can be generated, without using a multiplier, by modulating the switch on-time duration according to the output signal of the voltage error amplifier. In this case switch current sensing can be eliminated.

5.5.1 Advantages:

1. No need of a compensation ramp;
2. No need of a current error amplifier;
3. For controllers using switch current sensing, switch current limitation can be introduced.

5.5.2 Disadvantages:

1. Variable switching frequency;
2. Inductor voltage must be sensed in order to detect the zeroing of the inductor current;
3. For controllers in which the switch current is sensed, control is sensitive to commutation noises.



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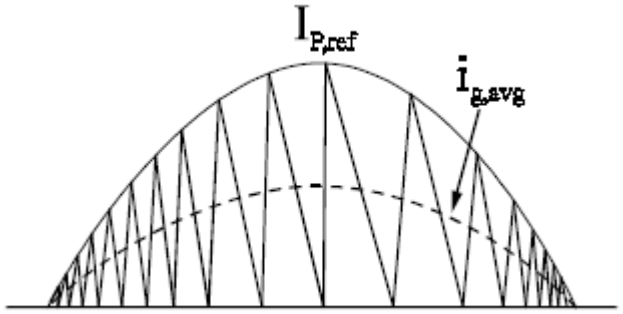

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Fig. 5.5 Borderline control scheme.

5.6 SIMULATION RESULTS:

5.6.1 Peak current control:

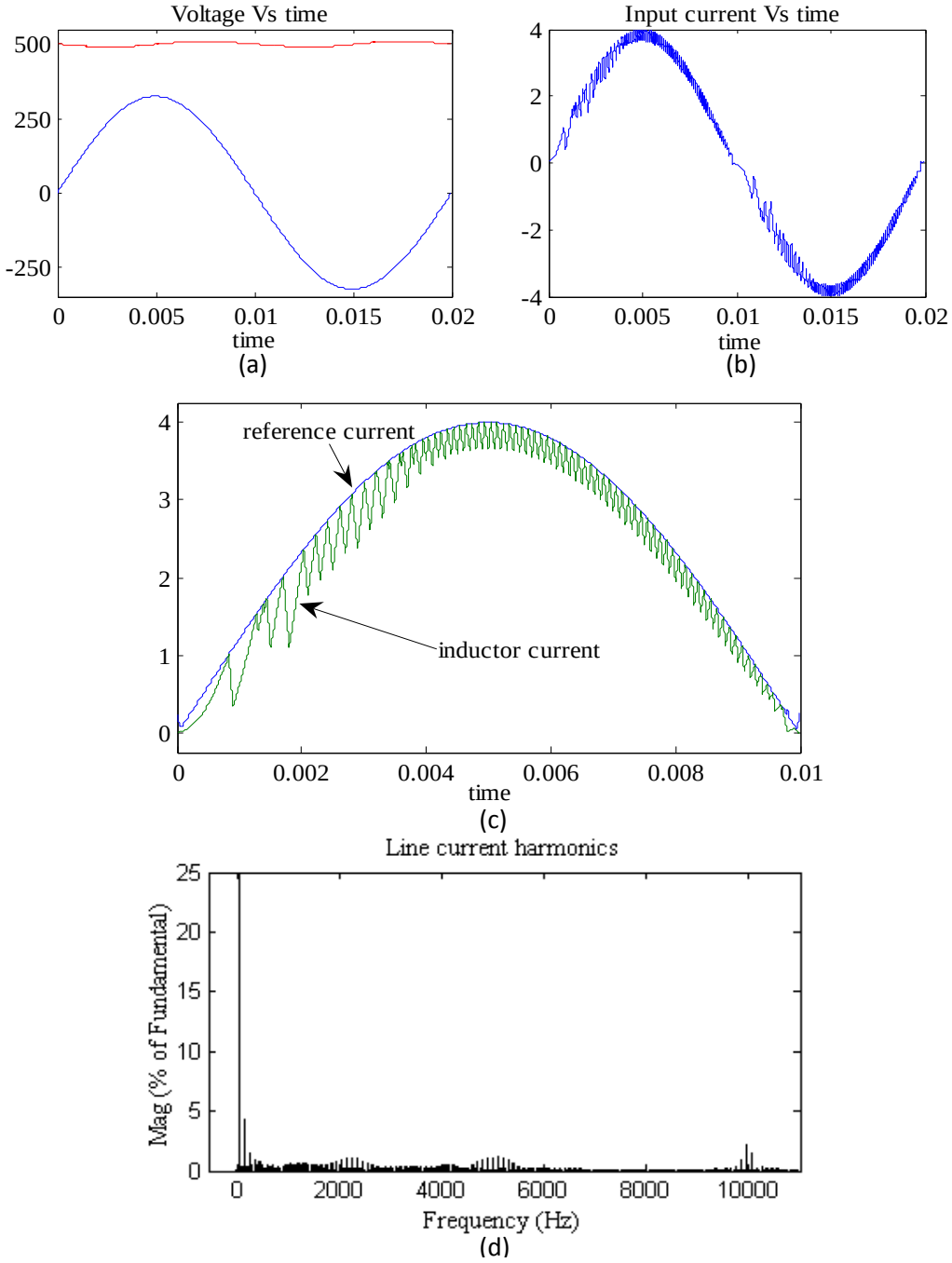


Fig. 5.6 peak current controlled boost converter. (a)Input voltage and output voltage; (b) Input current; (c) Inductor current and reference current; (d) Line current harmonics for AC line voltage V=230Vrms, output voltage Vo=500V, resistive load R=500 ohm, C_L=200μF,L=200mH operating at switching frequency 10kHz, the line current has THD=7.10%,Kp=0.9975, cosΦ=0.9999 and power factor=0.9975.

5.6.2 Average current control:

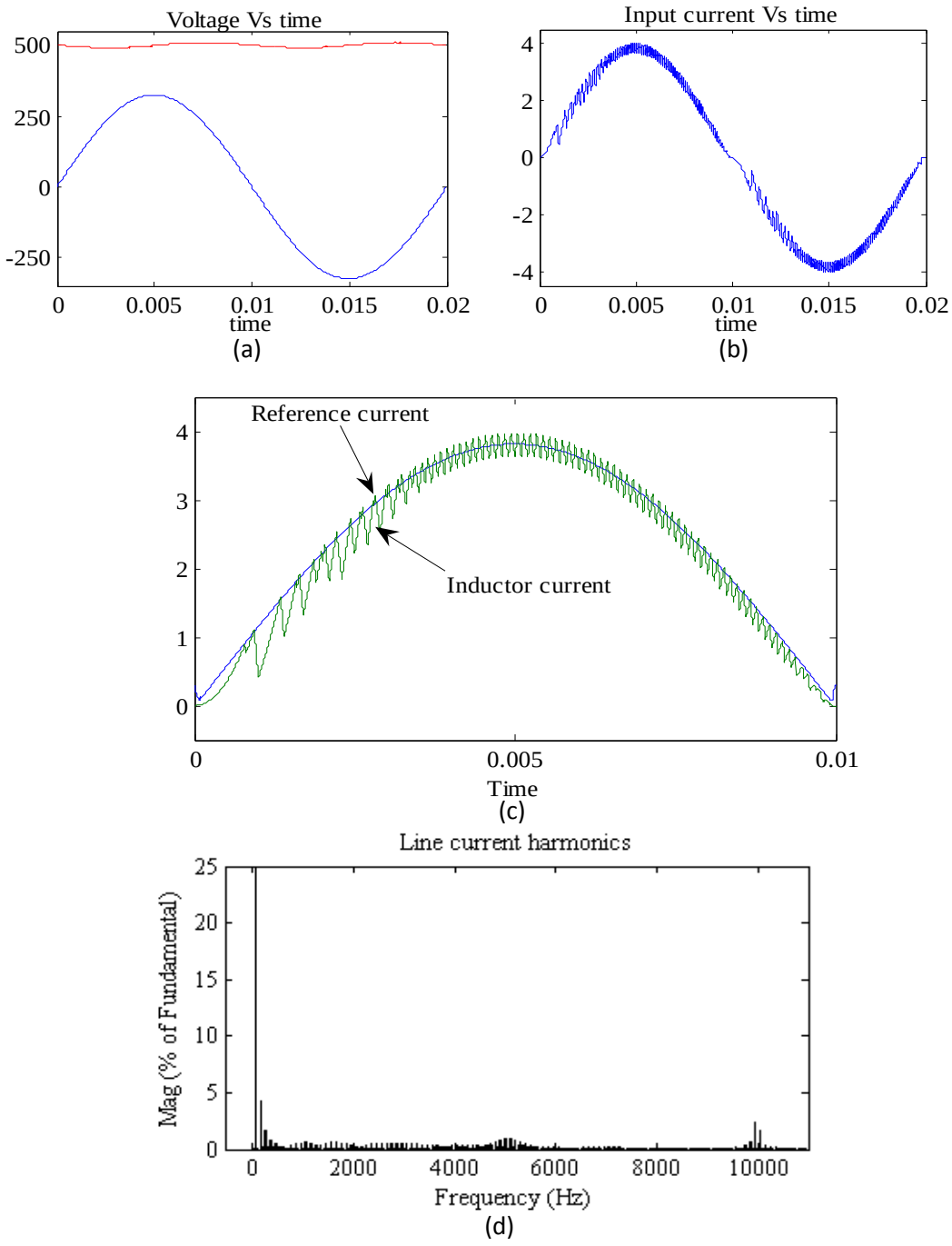


Fig. 5.7 Average current mode controlled boost converter. (a) Input voltage and output voltage; (b) Input current; (c) Inductor current and reference current; (d) Line current harmonics for AC line voltage V=230Vrms, output voltage V_0=500V, resistive load R=500 ohm, C_L=200μF, L=200mH operating at switching frequency 10kHz, the line current has THD= 6.8175%, Kp= 0.99768, cosΦ=0.9999 and power factor= 0.99768.

5.6.3 Hysteresis control:

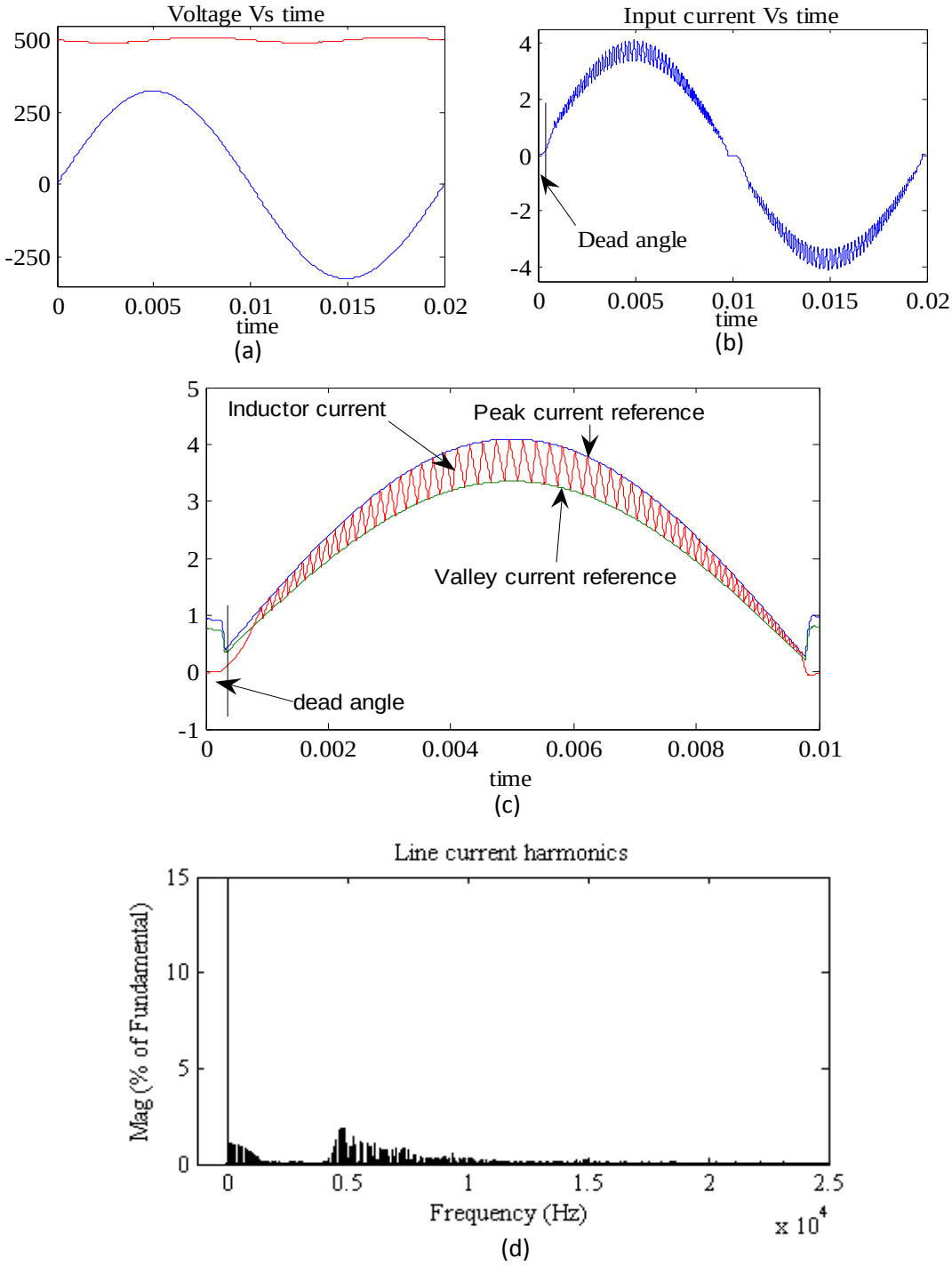


Fig. 5.8 Hysteresis control boost converter. (a) Input voltage and output voltage; (b)Input current; (c) Inductor current and reference current; (d) Line current harmonics for AC line voltage =230Vrms, output voltage V_0=500V, resistive load R=500 ohm, C_L=200μF,L=200mH, dead angle θ=5°, current ripple 10% and the line current has THD= 6.4967%,Kp= 0.9979, cosΦ=0.99999 and power factor= 0.9978

5.6.4 Borderline control:

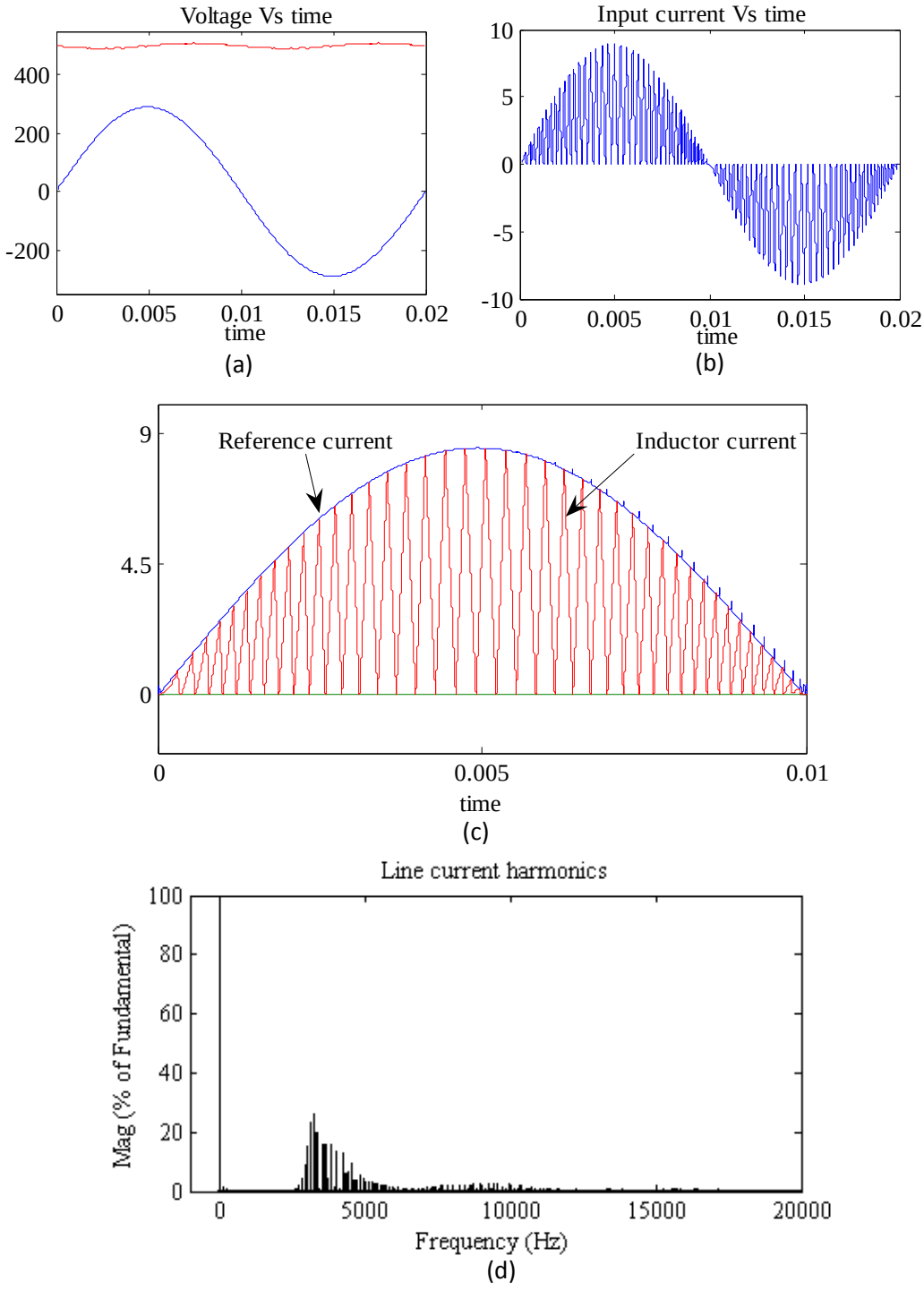


Fig. 5.9 Borderline controlled boost converter. (a) Input voltage and output voltage; (b)Input current; (c) Inductor current and reference current; (d) Line current harmonics for AC line voltage =230Vrms, output voltage V_0=500V, resistive load R=500Ω ohm, C_L=200μF, L=200mH and the line current has THD=0.5892, Kp=0.8615, cosΦ=0.9999 and power factor=0.8615.

Summary:

In this chapter, several control techniques specifically developed for PFC boost converters are analyzed. For each control strategy advantages and drawbacks are highlighted and information on available commercial IC's is given.

Even though peak current control gives better characteristics, it has several drawbacks, such as: poor noise immunity, need of slope compensation, peak to average current error. These problems can be eliminated by average current control at the cost of increased circuit complexity.

Hysteresis control and borderline control leads to variable frequency operation which may create sub-harmonic components. In borderline control, due to the presence of high current ripple it has high harmonic distortion. Hence the maximum power factor obtained will be limited to 0.87.Hence, peak and average current control techniques are the most preferable control techniques.

These converters operating in CICM reduces the line current harmonics, it also has Drawbacks, such as:

1) It increases the EMI, due to the high-frequency content of the input current.
2) It introduces additional losses, thus reducing the overall efficiency and
3) It increases the complexity of the circuit, with negative effects on the reliability of the instrument, as well as on its size, weight and cost.

The high frequency EMI can be eliminated by introducing an EMI filter between AC supply and diode bridge rectifier. The additional losses will be reduced by using soft switching techniques such as ‘ZVS’, ‘ZCS’ and ‘ZVT’. Some of the basic EMI filter requirements and a novel Zero Voltage Transition – ZVT technique, which can be applied to boost converter used in the PFC.

CHAPTER 6

METHODS FOR IMPROVING THE EFFICIENCY

An improved ZVT technique

Simulation results

Experimental Results

Summary

The commutation process of switching devices takes a certain time, during which the instantaneous power dissipated in the device can be very large. Therefore, switching losses are a major reason for decreased efficiency in converters. It was concluded from literatures in the previous chapter that the high side switching loss is highly dominant compared to the low side switching loss. This chapter presents the implementation of ZVT technique in a single phase active power factor correction circuit based on an ac-dc boost converter topology and operating in a continuous inductor current mode with peak current control method. The proposed converter achieves zero voltage or zero current turn-on and turn-off for the main switch as well as the soft-switching for the auxiliary switch. A 500 W, 40 kHz ZVT PWM boost PFC converter has been simulated and experimentally verified.

6.1 The Proposed Improved ZVT Converter:[A1]

The circuit scheme of the proposed converter is shown in Fig.6.1, which consists of main switch S_1, auxiliary switch S_2, main diode D, auxiliary diodes D_1 and D_2, two capacitors C_1, C_2 resonant inductor L_r and resonant capacitor C_r. The converter operates in a continuous inductor current mode (CICM).

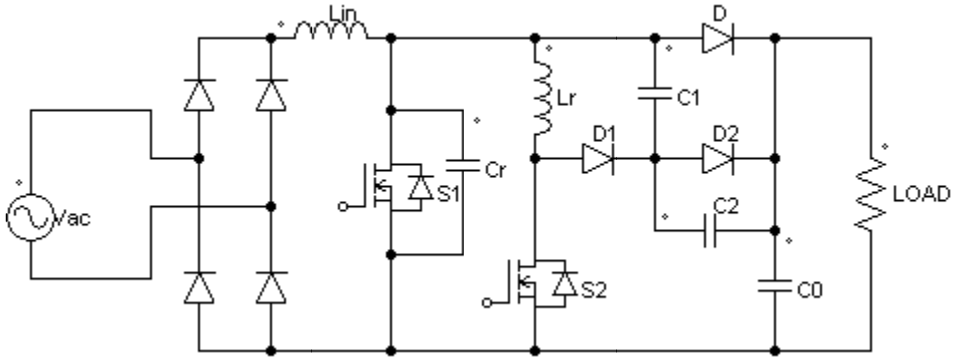


Fig.6.1. ZVT PWM boost PFC converter:

During one switching cycle, the following assumptions are made in order to simplify the steady state analysis of the circuits.

1. Input ac voltage is kept constant.

2. Output voltage is constant or output capacitor is large enough.

3. Output current is constant or inductor is large enough.

4. Reverse recovery time of diodes is ignored.

6.1.1 Modes of Operation:

The proposed converter has eight operating modes. The equivalent circuit of each mode are shown in fig 6.2. The key waveforms of these stages are given in fig.6.3.The detailed analysis of every stage is presented below:

Mode 1 [t_0-t_1]:

Prior to t = t_0, the main switch S_1 and the auxiliary switch S_2 are turned-off, and main diode D was conducting. At t = t_0, S_2 is turned-on, resonant occurs between L_r and C_r, the resonant inductor current i_{Lr} ramp up until it reaches I_{in} at t_1 ,where main diode D is turned-off with soft-switching. This mode ends when V_{Cr} becomes V_o. The voltage and current expressions which govern this circuit mode are given by:

$$V_O = L_r \frac{di_{L_r}}{dt} \tag{6.1}$$

$$\int V_O \, dt = \int L_r \, di_{L_r} \tag{6.2}$$

$$V_O t = L_r i_{L_r} \tag{6.3}$$

$$i_{L_r} = \frac{V_O}{L_r} t \tag{6.4}$$

$$V_{cr} = V_{Lr} = V_0 \tag{6.5}$$

Mode 2 [t_1- t_2]:

At t_1, the resonant inductor current reaches I_{in}. L_r and C_r continue to resonate. The resonant capacitor voltage V_{Cr} becomes equal to V_c .The voltage and current expressions are given by:

$$L_r \frac{di_{Lr}}{dt} + \frac{1}{C_r} \int i_{L_r} dt = 0 \quad (6.6)$$

$$I_{L_r}(S)SL_r + \frac{1}{C_r}\left[\frac{I_{L_r}(s)}{S} - \frac{C_r}{S}V_O\right] = 0 \quad (6.7)$$

$$I_{L_r}(S)\{ SL_r + \frac{1}{C_r S}\} = \frac{V_O}{S} \quad (6.8)$$

$$I_{L_r}(S) = \frac{V_0}{(L_r + \frac{1}{C_r S})S} = \frac{V_O}{\sqrt{\frac{L_r}{C_r}}} sin\, \omega_n\, (t - t_1) \quad (6.9)$$

$$I_{L_r}(S) = \frac{V_O}{Z_n} sin\, \omega_n\, (t - t_1) \quad (6.10)$$

Where $Z_n = \sqrt{\frac{L_r}{C_r}}$ and $\omega_n = \frac{1}{\sqrt{(L_r C_r)}}$

Now $I_{Lr} = I_{in} + \frac{V_0}{Z_n} sin\, \omega_n\, (t - t_1)$ (6.11)

$$V_{cr} = V_O - V_c \quad (6.12)$$

The negative sign of voltage across capacitor is due to its opposite polarity.

$$V_{cr} = V_O - \frac{1}{C_r}\int_0^t i_{L_r} dt = V_0\, cos\, \omega_n\, (t - t_1) \quad (6.13)$$

$$V_{cr} = V_0\, cos\, \omega_n\, (t - t_1) \quad (6.14)$$

Where $Z_n = \sqrt{\frac{L_r}{C_r}}$ and $\omega_n = \frac{1}{\sqrt{(L_r C_r)}}$

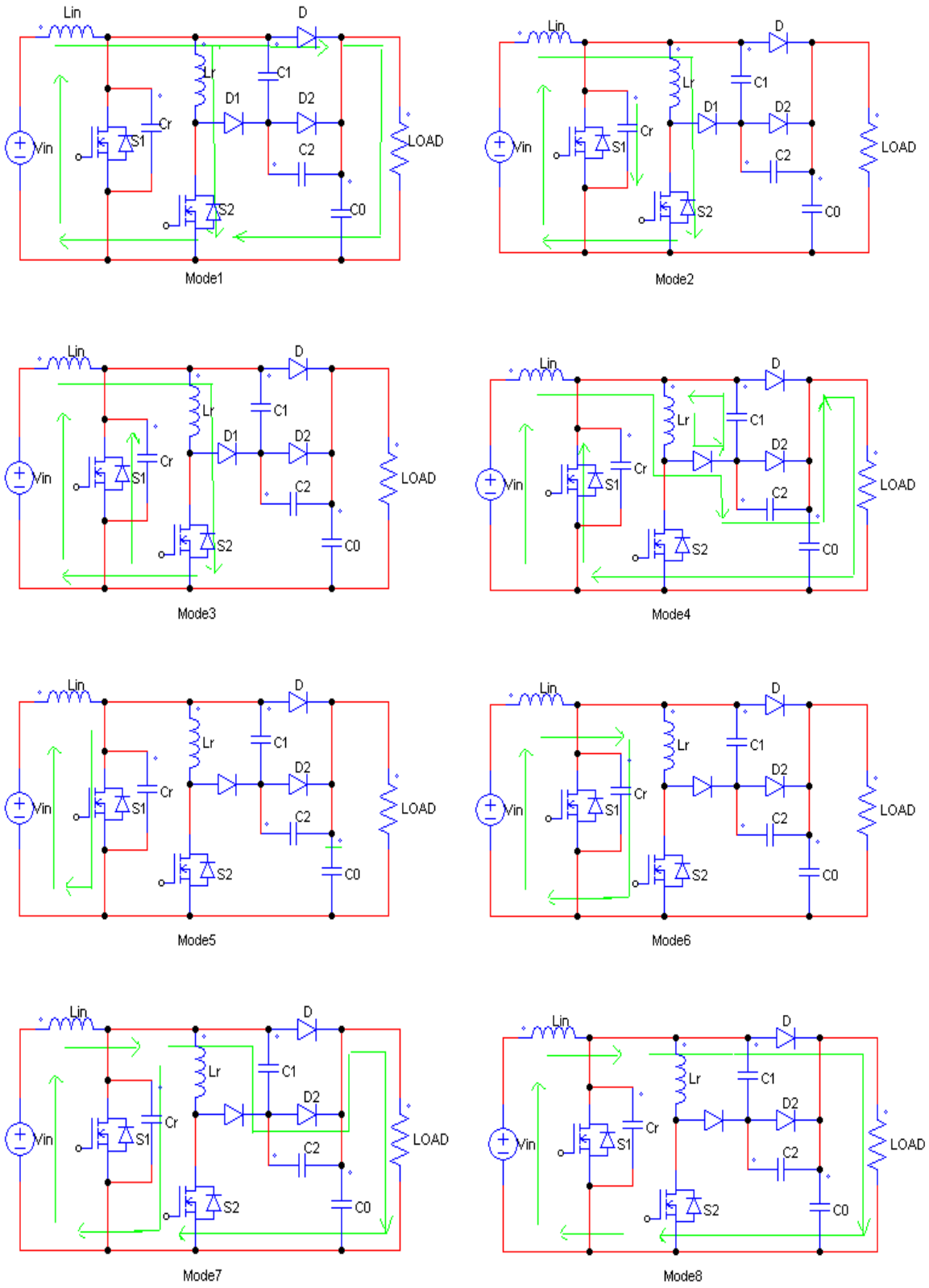


Fig.6.2 Equivalent circuit of each operating mode.

Mode 3 [t_2- t_3]:

When V_{cr} reaches zero at t_3 the body diode D_{S1} of the main switch conducts providing a freewheeling path for i_{Lr}. At this instant, main switch S_1 can be turned on at zero voltage. The current I_{DS1} is given by

$$I_{DS1} = \left[I_{in} + \frac{V_0}{Z_n}\right] - I_{in} = \frac{V_0}{Z_n} \tag{6.15}$$

Mode 4 [t_3- t_4]:

Auxiliary switch S_2, is turned off with near ZVS at t = t_3. The energy stored in the resonant inductor Lr is transferred to the capacitors C_1 and C_2. Then the voltage polarity of the capacitor C_1 is reversed. The energy stored in the capacitor C_2 will be recycled and used to suppress the turn-off voltage spike of the main switch S_1. The voltage and the current expressions of this mode are given by:

$$\frac{1}{2}L_r \mathrm{I_{L_r}}^2 = \frac{1}{2}C_r \mathrm{V_{C_r}}^2 \tag{6.16}$$

$$I_{Lr} = \sqrt{\frac{L_r}{C_r}} V_O \cos \omega_n(\mathrm{t} - \mathrm{t_3}) \tag{6.17}$$

$$I_{Lr} = I_{Lr}(t_2)\cos\ \omega_n(\mathrm{t} - \mathrm{t_3}) \tag{6.18}$$

Where $\mathrm{Z_n} = \sqrt{\frac{\mathrm{L_r}}{\mathrm{C_1}+\mathrm{C_2}}}$,$\omega_\mathrm{n} = \frac{1}{\sqrt{(\mathrm{L_r}(c_1+c_2))}}$

$$V_{c1} = \frac{1}{\mathrm{C_r}}\int_0^{\mathrm{t}} I_{L_r}\,\mathrm{dt} = Z_n I_{Lr}(t_2)\sin\omega_n(\mathrm{t} - \mathrm{t_3}) \tag{6.19}$$

$$V_{c1} = Z_n I_{Lr}(t_2)\sin\omega_n(\mathrm{t} - \mathrm{t_3}) \tag{6.20}$$

Where

$$Z_n = \sqrt{\frac{L_r}{C_1+C_2}}\ ,\omega_n = \frac{1}{\sqrt{(L_r(c_1+c_2))}}$$

Mode 5 [t_4- t_5]:

During this period the inductor L_{in} is charged from input dc voltage source while the main switch S_1 continues to conduct and the auxiliary switch S_2 is turned off with ZVS.

Mode 6 [t_5- t_6]:

At t_5, the main switch S_1 turns-off with ZCS, the resonant capacitor C_r charges through L_{in} and the voltage across the capacitor increases. The current in L_r falls zero and the voltage across C_r is given by

$$V_{Cr} = \frac{L_{in}}{C_r} t = \frac{I_l}{C_r} t \tag{6.21}$$

Mode 7 [t_6- t_7]:

When the voltage across C_r is greater than (V_0+V_{C1}), the capacitor C_1 begins to discharge through the diode D_2 .This discharge of C_1, can slow down the rising voltage slope of the voltage across C_r, i.e. the voltage across the main switch S_1.

The voltage across C_r is given by:

$$V_{Cr} = (V_0 + V_{c1}) \tag{6.22}$$

Mode 8 [t_7– t_8]:

This stage begins when the diode D is turned-on under ZVS. The operation of the circuit at this stage is identical to the normal turned off operation of a PWM boost converter. This mode ends when S_2 is turned on to begin a new switching cycle.

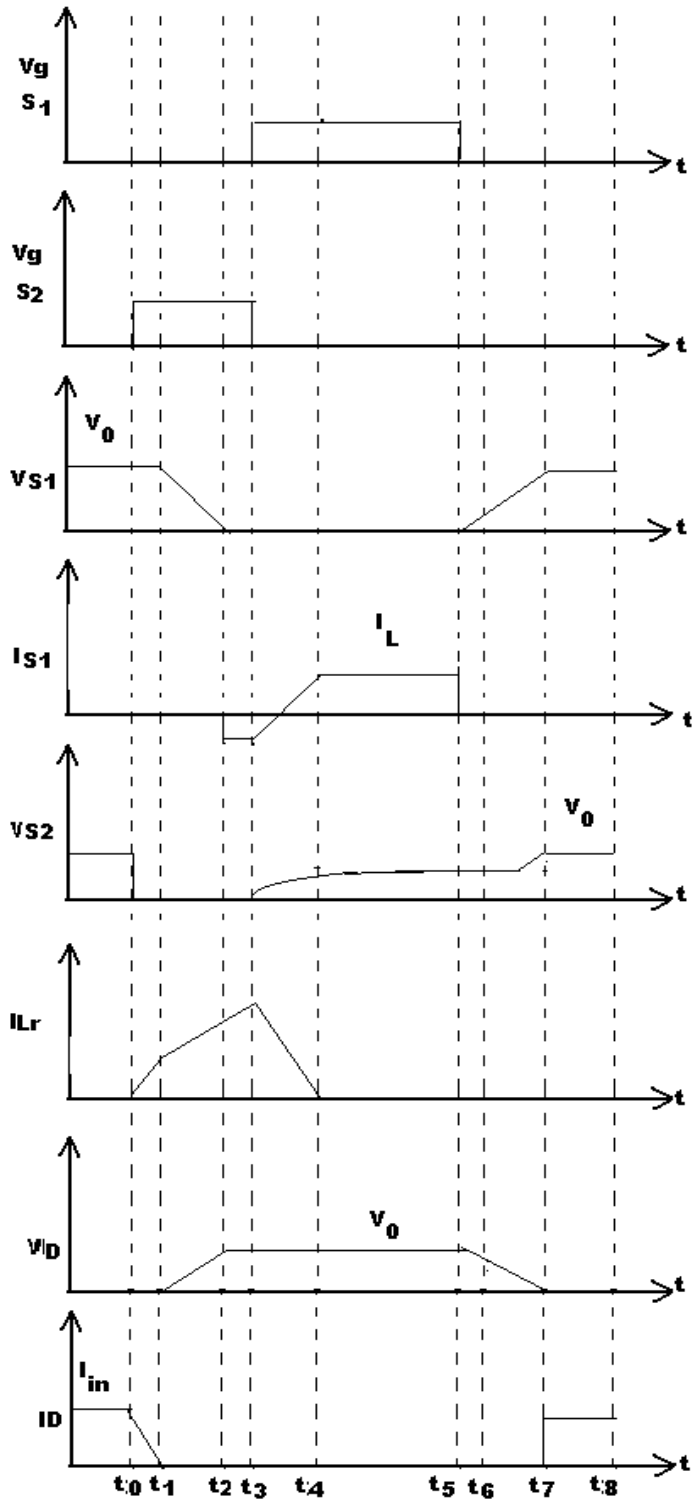


Fig.6.3 Theoretical waveforms.

6.2 Design Considerations:

6.2. 1 Switching Frequency (f_s)

Determination of switching frequency plays a most important role in the design of the power converter. There are many factors influence its proper selection. However, the determination of switching frequency is still a compromise between theoretical analysis and practical implementation.

6.2.2 Minimum Duty Ratio (D_{min})

The minimum duty ratio occurs when the input voltage gets the maximum and this is equal to :

$$D_{min} = \frac{V_0 - V_{in(max)}}{V_0} \tag{6.23}$$

6.2.3 Primary Input Inductor (L_{in})

The primary input inductor must satisfy a constraint governing to meet the requirement on maximum allowable ripple current. The input inductor (L_{in}) is given by

$$L_{in} = \frac{V_{in(min)} D_{min} T_s}{\Delta I_{in}} \tag{6.24}$$

Where ΔI_{in} is the input ripple current and

$$T = \frac{1}{f_s}$$

6.2.4 Output Capacitor (C_o)

The selection of the output capacitor depends on the output ripple voltage (ΔV_0) as follows:

$$C_0 \geq \frac{P_0}{2\omega_s V_0 \Delta V_0} \tag{6.25}$$

Where $\omega_s = 2\pi f_{line}$

6.2.5 Delay Time (T_D):

The on-time of auxiliary switch (S_2) must be shorter than one tenth of the switching period.

$$t_D \geq \frac{I_{in}L_r}{V_0} + \frac{\pi}{2}\sqrt{L_r}C_r \tag{6.26}$$

6.2.6 Resonant Capacitor (C_r)

The resonant capacitor (C_r) can be expressed **as:**

$$C_r = \frac{(a-1)^2 I_{in(max)} T_D}{V_0[1+\frac{\pi}{2}(a-1)]} \tag{6.27}$$

6.2.7 Resonant Inductor (L_r)

The resonant inductor is given by

$$L_r = \frac{V_0 T_D}{I_{in(max)}\left[1+\frac{\pi}{2}(a-1)\right]} \tag{6.28}$$

Where a is greater than one (1‹a‹1.5*)* and is desired to be as small as possible. This factor can be used for the selection of the auxiliary switch

(6.29)

6.2.8. Additional Capacitor (C_1, C_2)

To guarantee a soft-switching of the auxiliary switch the required capacitance C_1 should be selected according to the expression:

$$C_1 < \frac{L_r[I_{in(min)}+V_0\sqrt{\frac{L_r}{C_r}}]^2}{{V_0}^2} - C_2 \quad \text{, Where } \; C1 > C2 \tag{6.30}$$

6.2.9 Design specifications of Boost ZVT Converter:

The converter is designed for the following specifications:

Input ac voltage V_{in}=230 volt (rms)

Output dc voltage V_0=400 volt

Output power $P_0 = 500\ watt$

Switching frequency(f_s) =40 kHz

Output voltage ripple=5%

Input current ripple=20%

The detailed design values of the circuit parameters are as follows:

$D_{min} = \frac{V_0 - V_{in(max)}}{V_0} = \frac{(400-117)}{400} \times 100 = 70\%$

$L_{in} = \frac{V_{in(min)} D_{min} T_s}{\Delta I_{in}} = \frac{(106 \times 0.7 \times 25\mu S)}{0.2} = 0.0093H$

$C_o = \frac{\Delta\, i_{in} \times T}{8 \times \Delta\, V} = \frac{0.2 \times 0.1 \times 10^{-3}}{8 \times .05} = 250 \times 10^{-6} F$

$C_0 \geq \frac{P_0}{2\omega_s V_0 \Delta\, V_0}$

$t_D \geq \frac{I_{in} L_r}{V_0} + \frac{\pi}{2}\sqrt{L_r C_r} = \frac{(2 \times 2 \times 10^{-3})}{400} + (1.8 \times 10^{-9} \times 80 \times 10^{-6}) = 1.1025 \times 10^{-7} Sec$

$C_r = \frac{(a-1)^2 I_{in(max)} T_D}{V_0[1 + \frac{\pi}{2}(a-1)]} = \frac{(1.5-1)^2 \times 2.04 \times 1.1025 \times 10^{-7}}{400 \times \{1 + 1.57 \times (1.5-1)\}} = 10^{-9} F$

$L_r = \frac{V_0 T_D}{I_{in(max)}\left[1+\frac{\pi}{2}(a-1)\right]} = \frac{400 \times 1.1025 \times 10^{-7}}{\{1+1.57 \times (1.5-1)\}} = 80 \times 10^{-6} H$

$C_1 < \frac{L_r [I_{in(min)} + V_0 \sqrt{\frac{L_r}{C_r}}]^2}{{V_0}^2} - C_2$, Where C1 > C2

$C_1 = 4.7 \times 10^{-9} F$

$C_2 = 1.5 \times 10^{-9} F$

6.3 Selection of Devices

6.3.1 MOSFET Selection

When selecting the MOSFETs, there is a fundamental choice of whether to use an N-channel or P channel device for the upper switch. N channel MOSFETs have the advantage of lower on resistance for a given die size and often have lower gate charge. They also tend to be relatively inexpensive. Their chief drawback is that they need a bootstrapped drive circuit or a special bias supply for the driver to work, since the gate drive must be several volts above the input voltage to the converter to enhance the MOSFET fully. Conversely, P channel MOSFETs has simpler gate drive requirements. They require that their gate be pulled a few volts below the input voltage for them to be turned on. Their disadvantage is that their cost is higher as compared to their N channel counterpart for an equivalent R_{ds} (on), and they generally have slower switching times. For soft switching applications, C_{oss} is important because it can affect the resonance of the circuit.

6.3.2 Inductor and Capacitor Selection

The optimum inductor value for a particular supply is dependent on the switching frequency, transient performance, and the conduction losses in the inductor and other components. Some of the merits for selecting a low vs. high inductor value for a given core size and geometry are summarized below:

A. Benefits of Lower Inductor Values

1. Low DCR: lower DC inductor losses in windings
2. Fewer turns: higher DC saturation current
3. High di/dt: faster response to load step / dump
4. High di/dt: fewer output capacitors required for good load transient recovery

B. Benefits of Higher Inductor Values

1. Low ripple: lower AC inductor losses in core (flux) and windings (skin effect)
2. Low ripple: lower conduction losses in MOSFETs
3. Low ripple: lower RMS ripple current for capacitors
4. Low ripple: continuous inductor current flow over wider load range

In general, lower inductor values are best for higher frequency converters, since the peak-to peak ripple current decreases linearly with switching frequency. A good rule of thumb is to select

an inductor that produces a ripple current of 10% to 30% of full load DC current. Too large an inductance value leads to poor loop response, and too small an inductance value leads to high AC losses. The capacitor value is chosen based on L. A high value of output capacitance gives fewer ripples and vice-versa.

6.3.3 Diode selection

While selecting the diodes, the reverse recovery characteristic is taken into account. Due to low stored charge and ultrafast recovery with soft recovery characteristics, ringing and electrical noise can be minimized, Thus power loss in the switching transistor can be reduced. The MURP8100 is an ultrafast diode (t_{rr} < 75ns) with soft recovery characteristics. It has a low forward voltage drop.

The designed values are summarizes below:

Table.6.1.Designed Values for the converter

Parameter	Value
L_{in}	1mH
R	500 Ω
L_r	$80\mu H$
C_1	4.7nF
C_2	1.5nF
C_0	250 μF

The simulation results of the proposed converter have been presented from Fig. 6.4 to Fig.6.9.The simulation is carried out in MATLAB7.0/SIMULINK.

6.4 Simulation results:

The proposed circuit is simulated with Matlab-Simulink and simulation results are presented in Fig.6.4 to Fig.6.9 and in table 6.2.

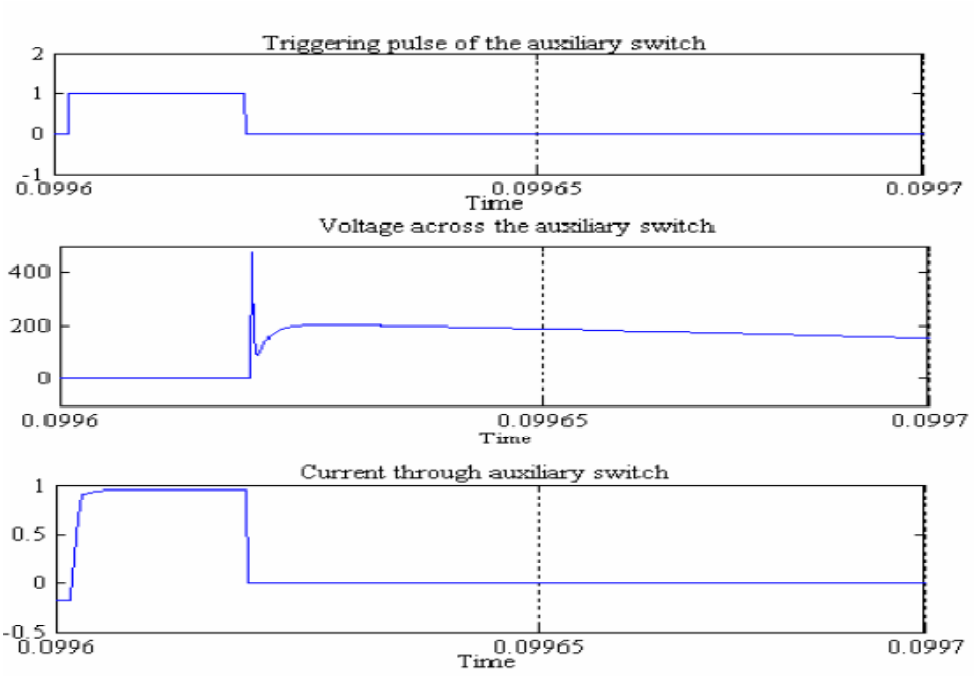


Fig.6.4 Triggering pulse of auxiliary switch and the voltage across it and the current through the auxiliary switch for the proposed ZVT converter.

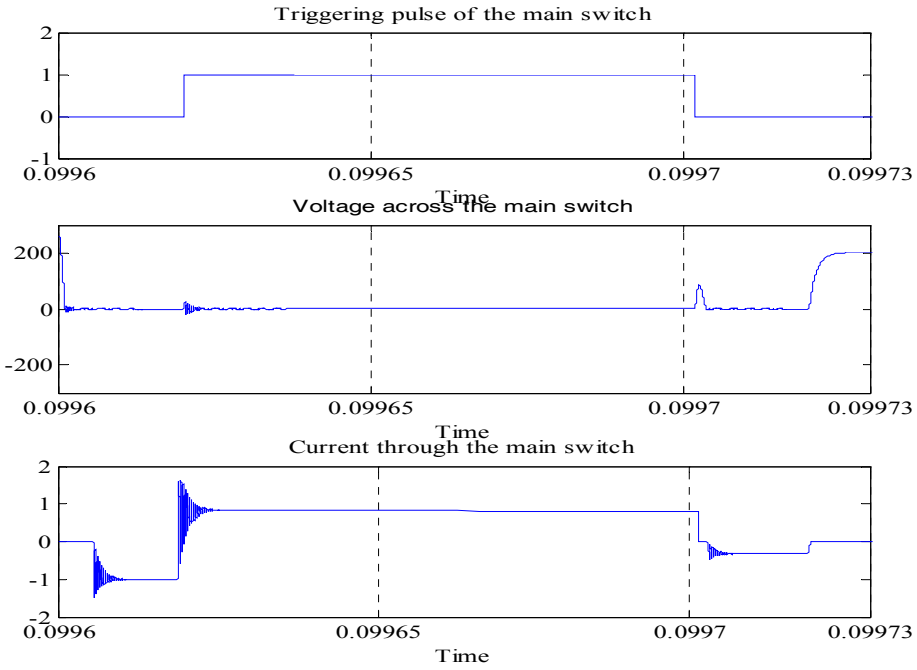


Fig 6.5 Triggering pulse of the main switch, the voltage across it and the current through the main switch for the proposed ZVT converter.

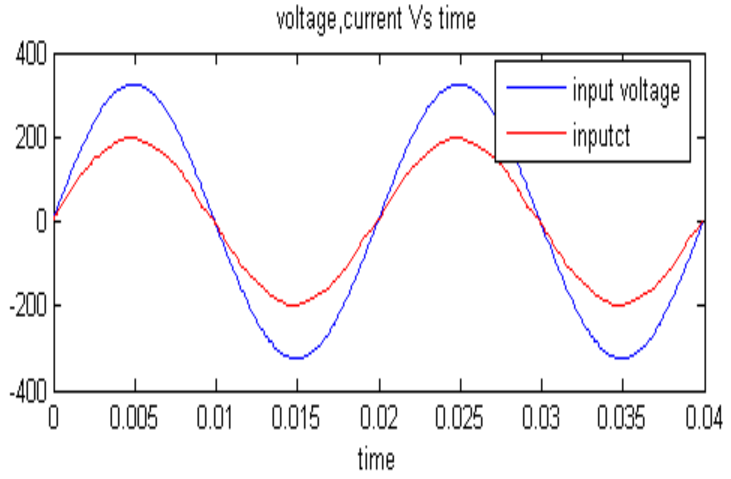


Fig.6.6 Input voltage and input current (input current multiplying factor is 100)

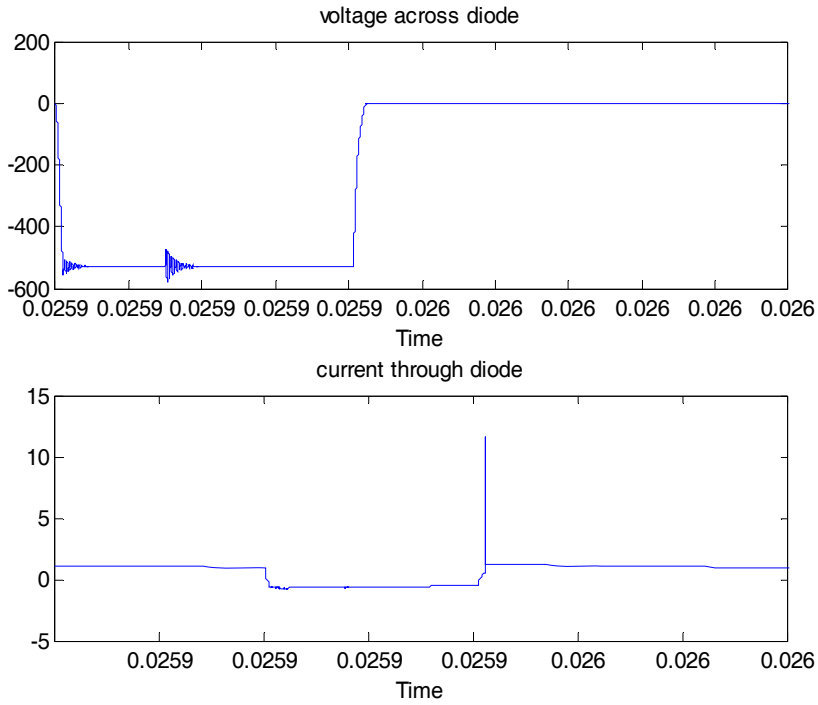


Fig. 6.7 Voltage across the diode and Current through the diode

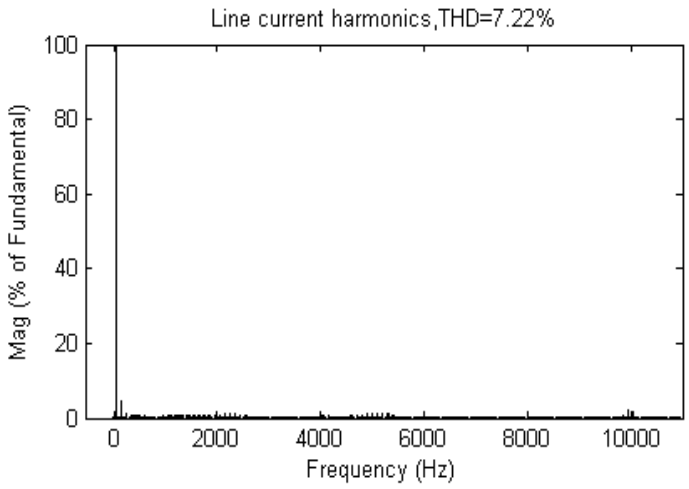


Fig 6.8 Harmonic distortion Without ZVT

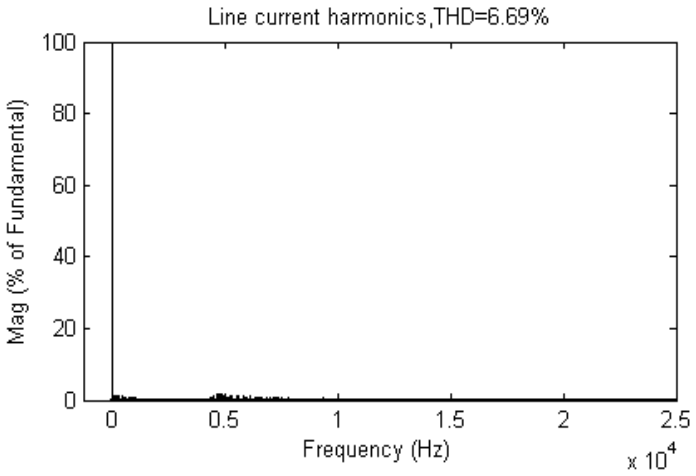


Fig 6.9 Harmonic distortion With ZVT

Table.6.2. Comparison of different parameters without and with soft-switching:

Parameters	Without ZVT	With ZVT
THD	0.072	0.066
K_P	0.997	0.997
CosΦ	1.000	1.000
Power factor	0.9974	0.9977
P_{ac}	575.48W	510.22W
P_{dc}	499.78W	499.887W
Efficiency	86.86%	98 %

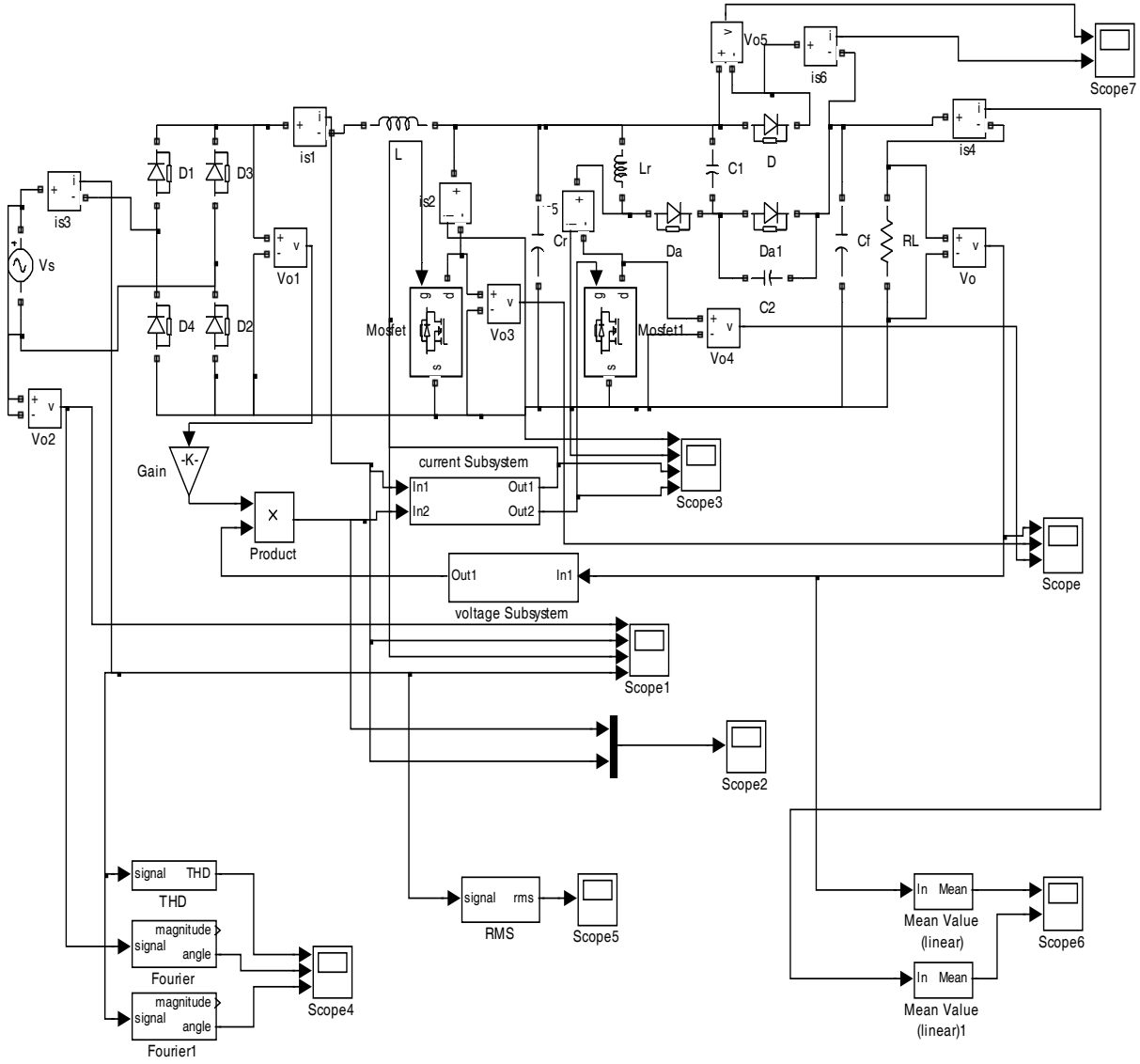


Fig.6.10. Simulation model of the proposed ZVT converter

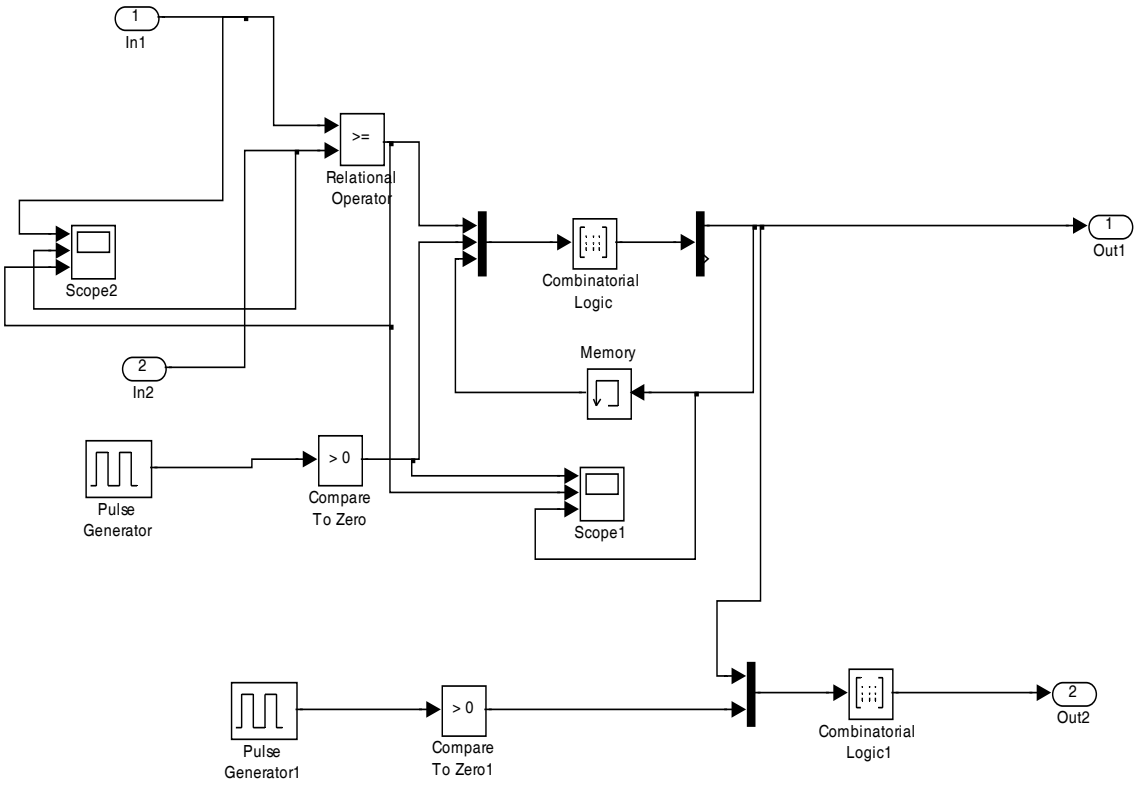


Fig.6.11. Current sub system of the proposed ZVT converter

6.5 Experimental Verifications:

A Prototype of the circuit is developed in the laboratory. MOSFET (APT5025) for main and auxiliary switch, diodes (MURP8100) and controller chip (UC3854),Electronic load ELHC300 are used. The experimental circuit is shown in fig.6.12. The experimental results are presented in Fig.6.13 to Fig.6.16.

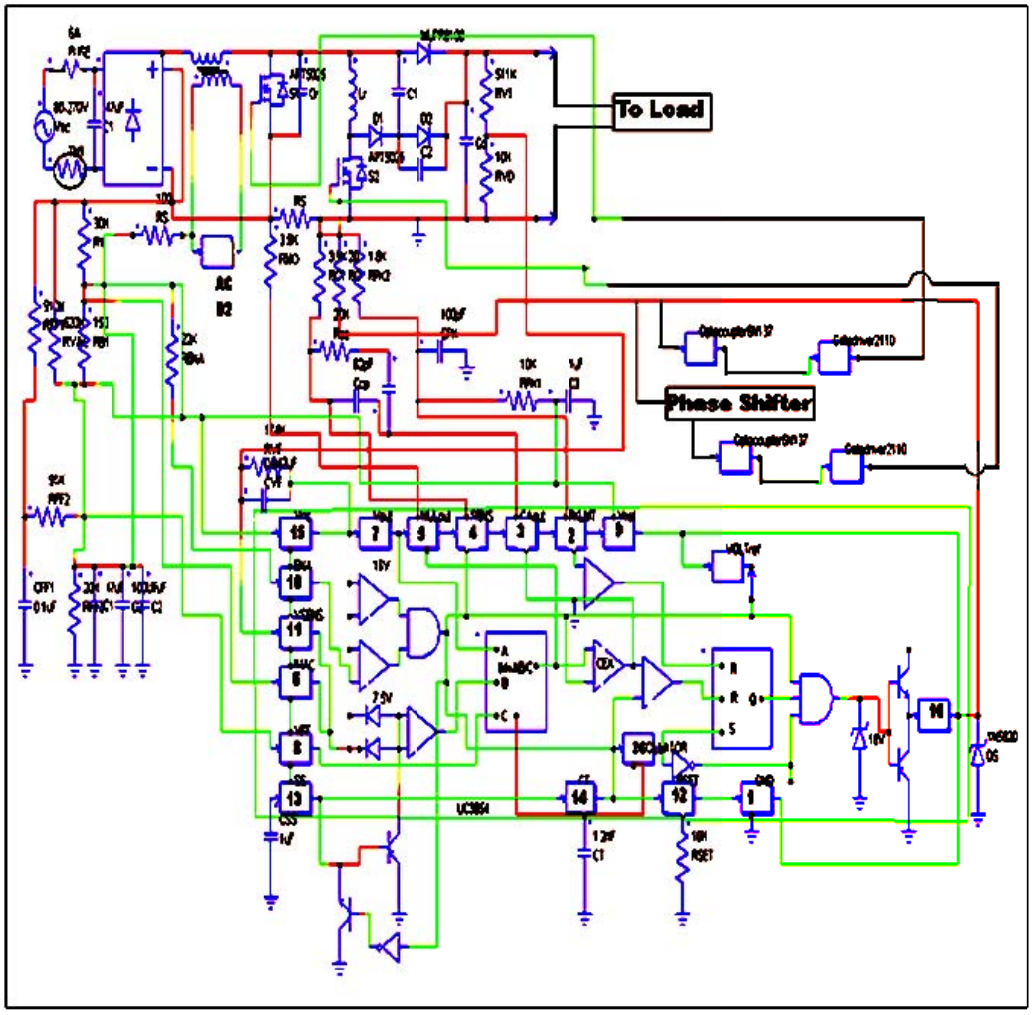


Fig.6.12. Experimental Circuit

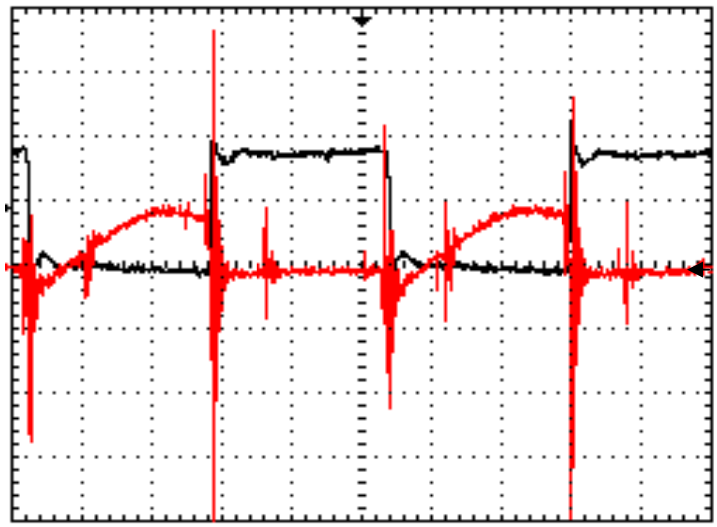


Fig. 6.13 Current and voltage waveforms of auxiliary switch S2, for the proposed ZVT PFC converter, Voltage: 200V/div (Black), Current: 2A/Div (Red), Time: 5µs /div.

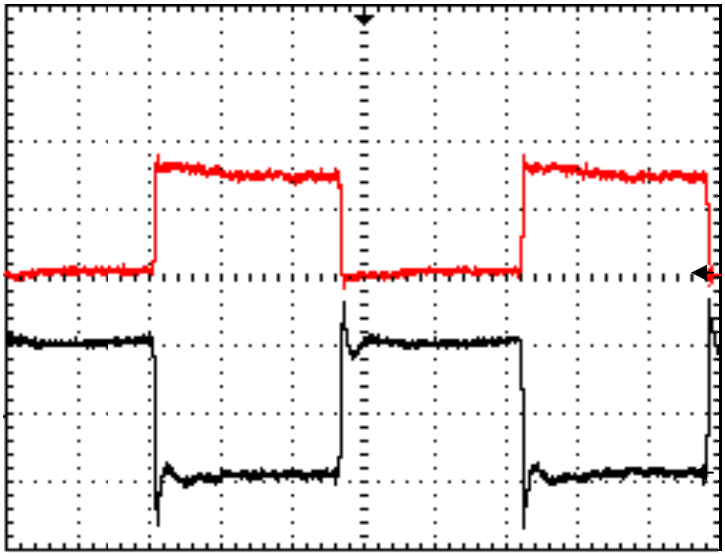


Fig. 6.14 Current and voltage waveforms of main switch S1 for the proposed ZVT PFC converter, Voltage: 200V/div (Black), Current: 1A/div (Red), Time: 5µs/div.

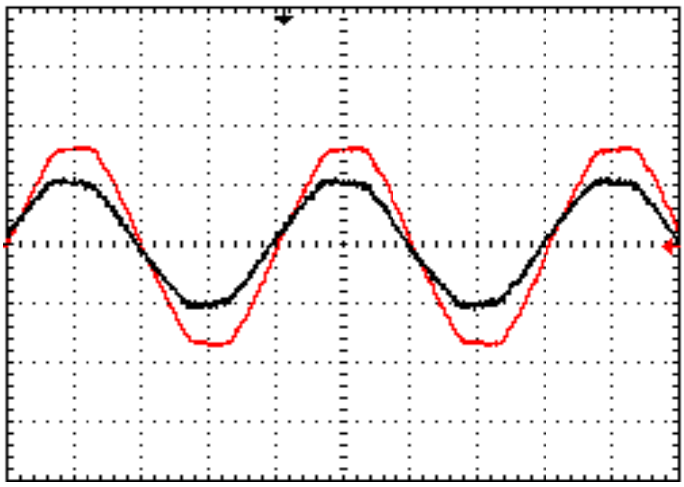


Fig.6.15. Experimental results of the input voltage and current waveform for the Proposed ZVT PFC converter, voltage: 200V/div (Red), Current: 2A/div (Black), time: 5ms/div.

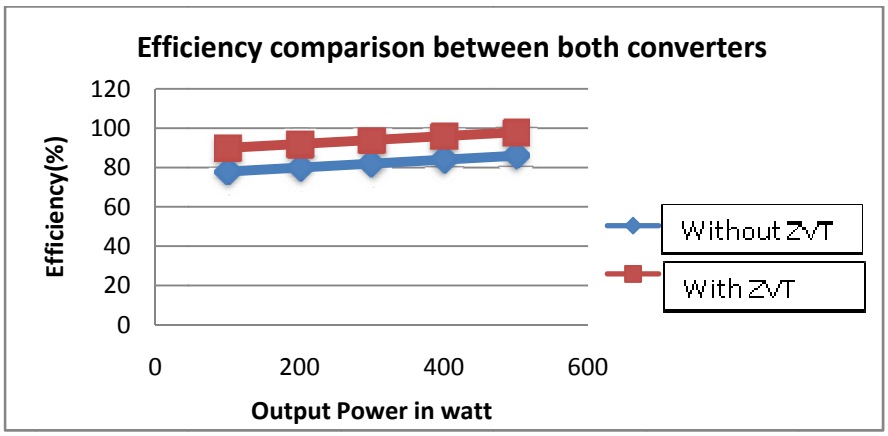


Fig.6.16.Efficiency plot

Summary:

The ZVT technique has been implemented in PFC converter to achieved soft switching by using an active auxiliary circuit. Besides the main switch ZVS turned-on and ZCS turned-off, the auxiliary switch also turned-on with ZCS and turned-off with ZVS, which can be observed from Figs.6.13 and 6.14. Since the active switches are turned-on and turned-off under soft switching condition, the switching losses are reduced and the higher efficiency of the system is achieved. The results have been compared with the PFC stage with hard switching. Figs.6.15 and 6.16 suggest that with Peak current control and ZVT technique nearly unity power factor is achieved and efficiency is improved. The simulation results (Figs. 6.4 to 6.7) are in close agreement with the experimental results.

CHAPTER 7

CONCLUSION

Conclusion

Future work

CONCLUSION

Reduction of line current harmonics is needed in order to comply with the standard. This is commonly referred to as the Power Factor Correction – PFC. Power factor correction (PFC) is a technique of counteracting the undesirable effects of electric loads that create a power factor less than one. There are several solutions to achieve PFC. Depending on whether active switches (controllable by an external control input) are used or not, PFC solutions can be categorized as "Passive" or "Active".

Passive PFC:

The passive PFC circuit uses low-frequency filter components to reduce harmonics. This approach typically meets EN standards for Class-A equipment up to 250W, at a much lower cost than a comparable switch mode power supply (SMPS) employing active PFC techniques. They typically yield less PF's compared to active topologies; they require a voltage doubler circuit for universal operation on most topologies above 150W. Different techniques to implement "Passive PFC" have been discussed.

Active PFC:

The preferable type of PFC is Active Power Factor Correction (Active PFC). Active PFC able to generate a theoretical power factor of over 95%. Active Power Factor Correction also markedly diminishes total harmonics, automatically corrects for AC input current, and is capable of a full range of input voltage. Since Active PFC is the more complex method of Power Factor Correction, it is more expensive to produce an Active PFC power supply.

Low-frequency active PFC:

Some of the techniques to implement "Low-frequency switching active PFC" have been presented. An active low frequency approach can be implemented up to about 1000 watts. Power factors as high as 0.95 can be achieved with an active low frequency design. To conclude, low-frequency switching PFC offers the possibility to control the output voltage in certain limits. In such circuits, switching losses and high-frequency EMI are negligible. However, the reactive elements are large and the regulation of the output voltage is slow.

High-frequency active PFC:

Nearly unity power factor can be obtained by "high-frequency switching active PFC", if a suitable control method is used to shape its input current or if it has inherent PFC properties. The converters can operate in Continuous Inductor Current Mode – CICM, where the inductor current never reaches zero during one switching cycle, or Discontinuous Inductor Current Mode - DICM, where the inductor current is zero during intervals of the switching cycle.

Operation in discontinuous inductor current mode – DICM:

In DICM, the input inductor is no longer a state variable since its state in a given switching cycle is independent on the value in the previous switching cycle. The peak of the inductor current is sampling the line voltage automatically. This property of DICM input circuit can be called "self power factor correction" because no control loop is required from its input side.

We can conclude that the basic boost converter and buck-boost converter have excellent self-PFC capability naturally. Among them, boost converter is especially suitable for DICM PFC usage and buck-boost is not widely used because of the drawbacks such as: the input voltage and the output voltage don't have a common ground due to the reversed output voltage polarity, etc. Hence, this converter is the most preferable by the designers for power factor correction purpose. Other converters may be used only if their input V-I characteristics have been modified (linear zed), or when they operate in continuous inductor conduction mode.

In addition, if discontinuous inductor current mode is applied, the input current is normally a train of triangle pulse with nearly constant duty ratio. In this case, an input filter is necessary for smoothing the pulsating input current into a continuous one.

Operation in continuous inductor current mode – CICM:

In CICM, different control techniques are used to convert the non-sinusoidal input current into sinusoidal. Some of them are (1) peak current control (2) average current control (3) Hysteresis control (4) borderline control. Even though these control techniques can be used for all DC-DC converters, only boost converter has been taken for the study because of the continuous input current. These control techniques specifically developed for PFC boost converters are analyzed. For each control strategy advantages and drawbacks are highlighted.

Even though peak current control gives better characteristics, it has several drawbacks, such as: poor noise immunity, need of slope compensation, peak to average current error. These problems can be eliminated by average current control at the cost of increased circuit complexity.

Hysteresis control and borderline control leads to variable frequency operation which may create sub-harmonic components. In borderline control, due to the presence of high current ripple it has high harmonic distortion. Hence the maximum power factor obtained will be limited to 0.87.Hence, peak and average current control techniques are the most preferable control techniques.

This high frequency switching PFC stage also has drawbacks, such as: it introduces additional losses, thus reducing the overall efficiency; it increases the EMI, due to the high frequency content of the input current.

Some of the EMI requirements have discussed. But the level of high-frequency EMI is much higher with a considerable amount of conduction and switching losses. This high frequency EMI will be eliminated by introducing an EMI filter in between AC supply and the diode bridge rectifier. Finally, to improve the efficiency of the PFC stage, operation of ZVT converter has been discussed, in which the switching losses are minimized by using an additional auxiliary circuit. Besides the main switch ZVS turned-on and ZCS turned-off, the auxiliary switch also turned-on at ZCS and turned-off near ZVS. Since the main switch and auxiliary switch are turned-on and turned-off softly, the switching losses are reduced and the higher efficiency of the system is achieved. The results have been compared with the PFC stage with hard switching.

To conclude, a 500 W, 40 kHz ZVT PWM boost PFC converter has been analyzed, simulated and results are validated with experimental results. The proposed converter gives around 0.9977 (almost unity) power factor with an efficiency of around 98%.

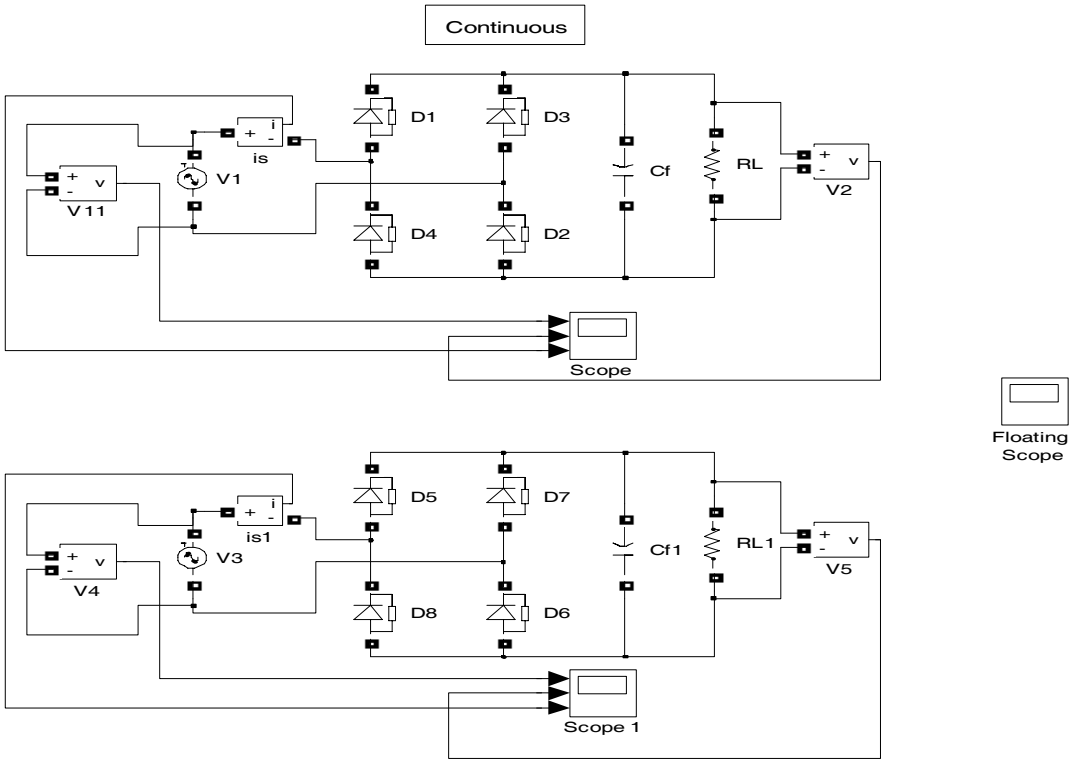
7.2 FUTURE WORK:

Throughout this thesis work, we have discussed only the second order converters applied for PFC. Better characteristics can be obtained by using fourth-order converters for PFC.

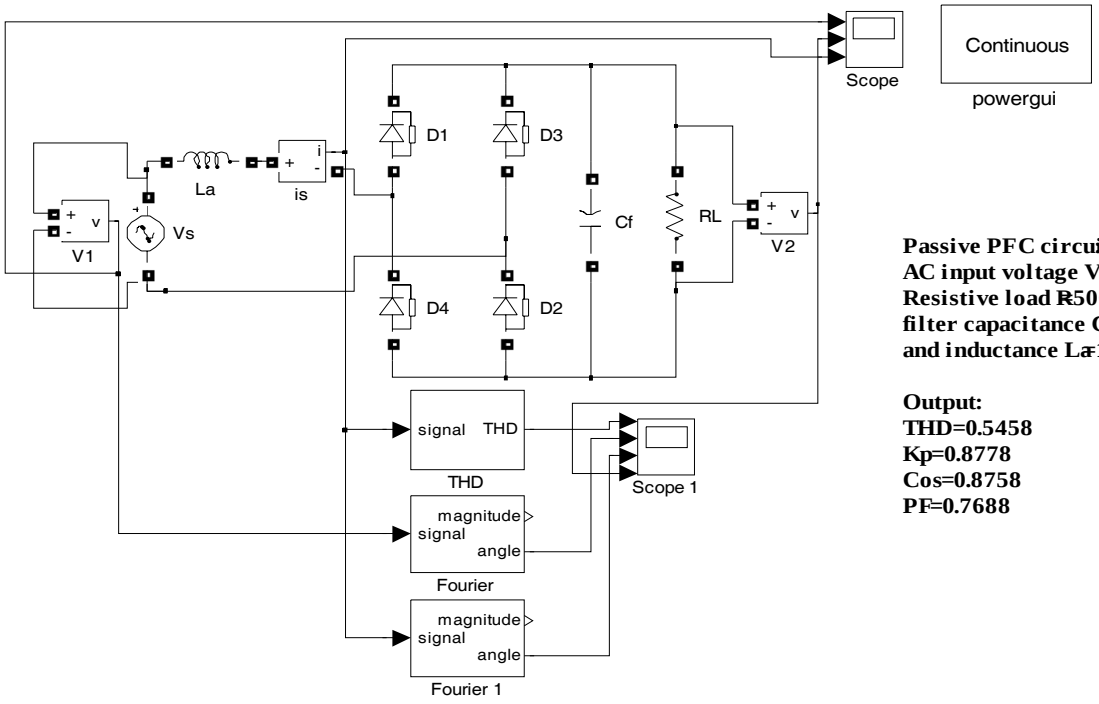
Appendix-I

The following Simulink models have been used for simulating the circuits given in chapter-2.

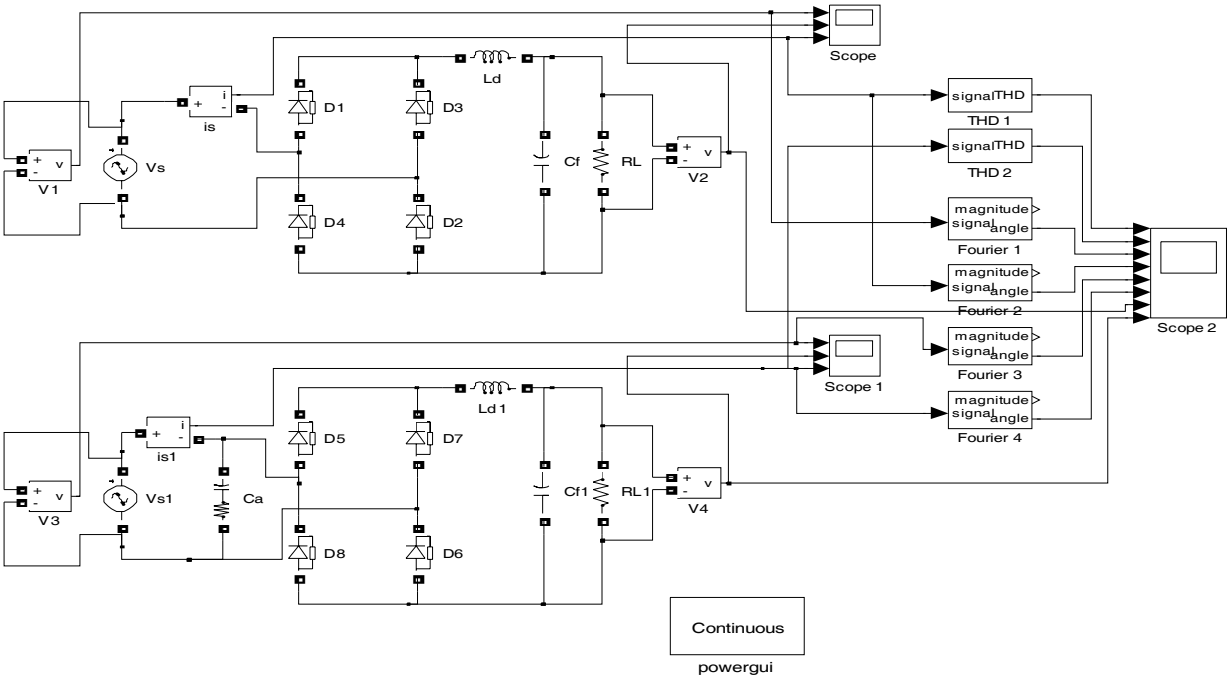
1. SImulink model for figure 2.1



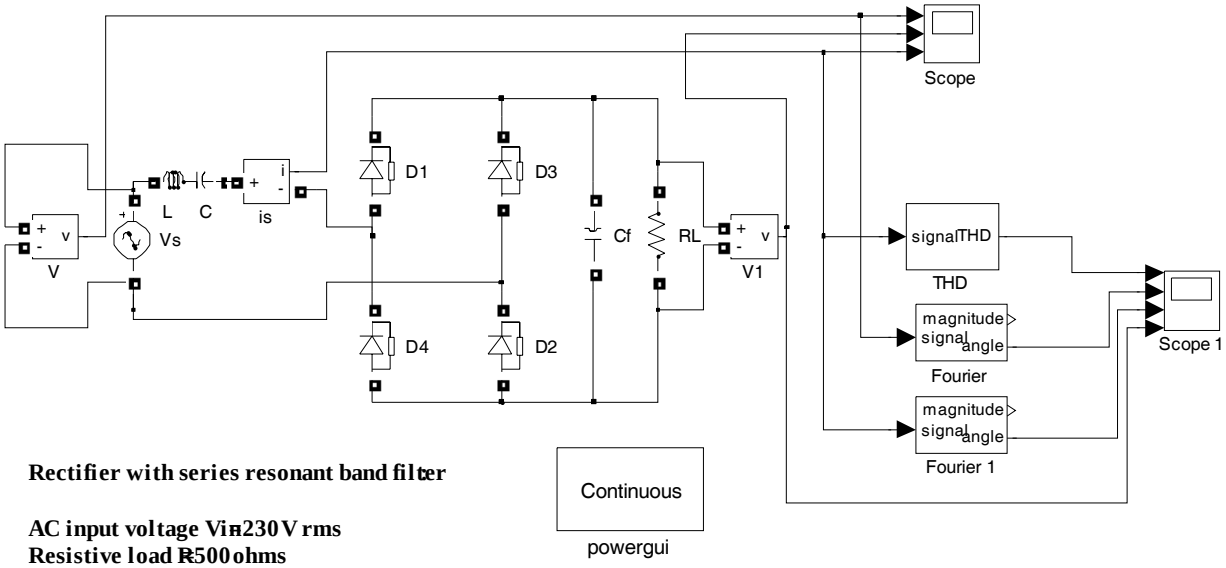
2. SImulink model for figure 2.2



3. Simulink model for fig 2.3



4. Simulink model for fig 2.4



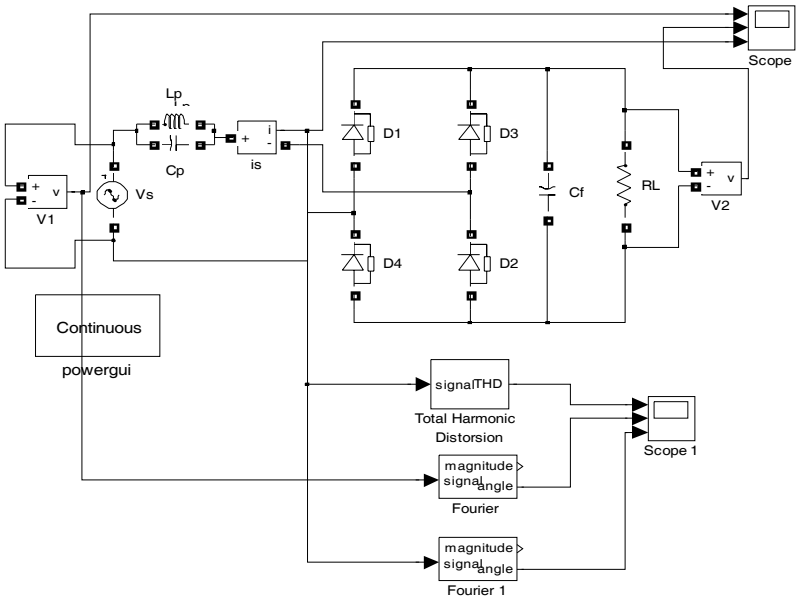
Rectifier with series resonant band filter

AC input voltage Vin=230 V rms
Resistive load R=500 ohms
Flter Capacitance Cf=470e-6 F
series inductance L=1.5H
series capacitance C=6.75e-6F

Output:

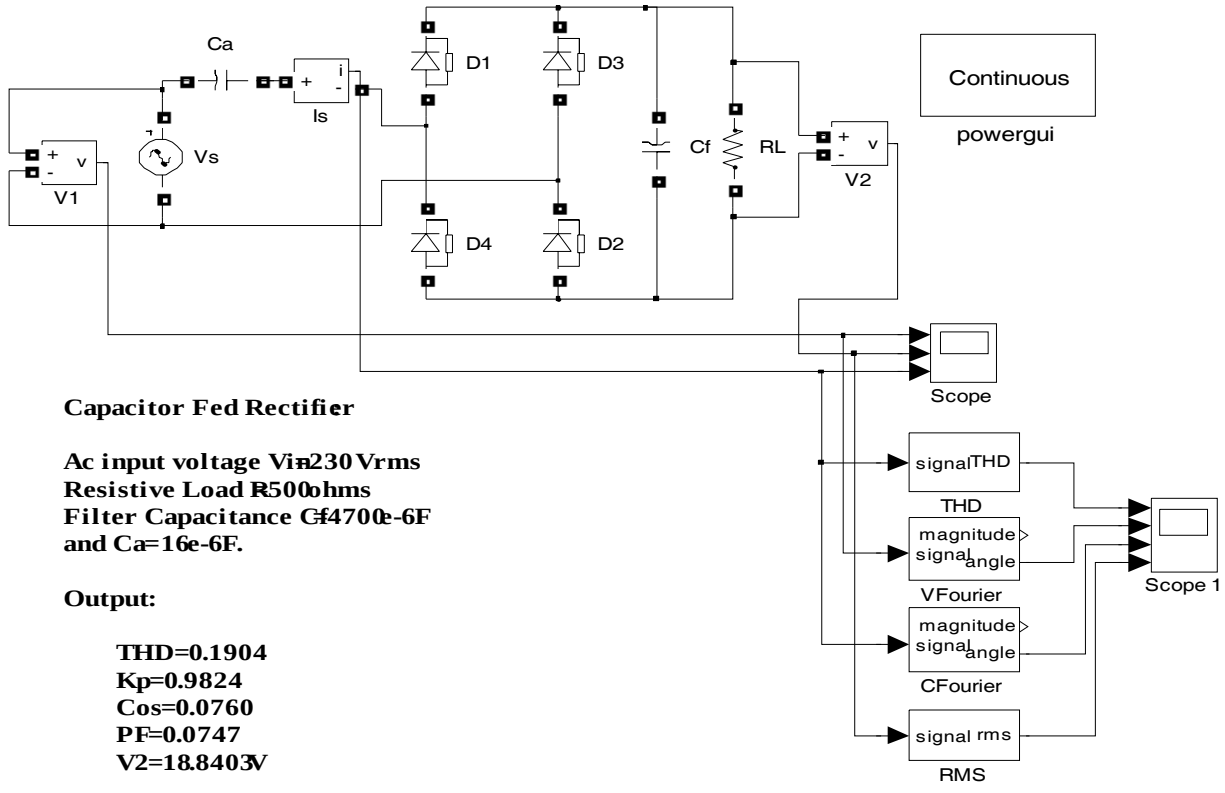
THD =0.1126
Kp = 0.9937
Cosine = 0.9997
PF= 0.9934
V2 =254.2617V

5. Simulink model for fig 2.5



Rectifier with parallel resonant bandstop filter
input:
Vin=230Vrms50Hz
resistive load R=500ohm
filter capacitance Cf=470e-6F
band-stop filter Lp=240e-3H
Cp=470e-6F
output:
THD=0.2969
Kp=0.9586
Cos=0.9987
PF=0.9574

6. Simulink model for fig 2.6



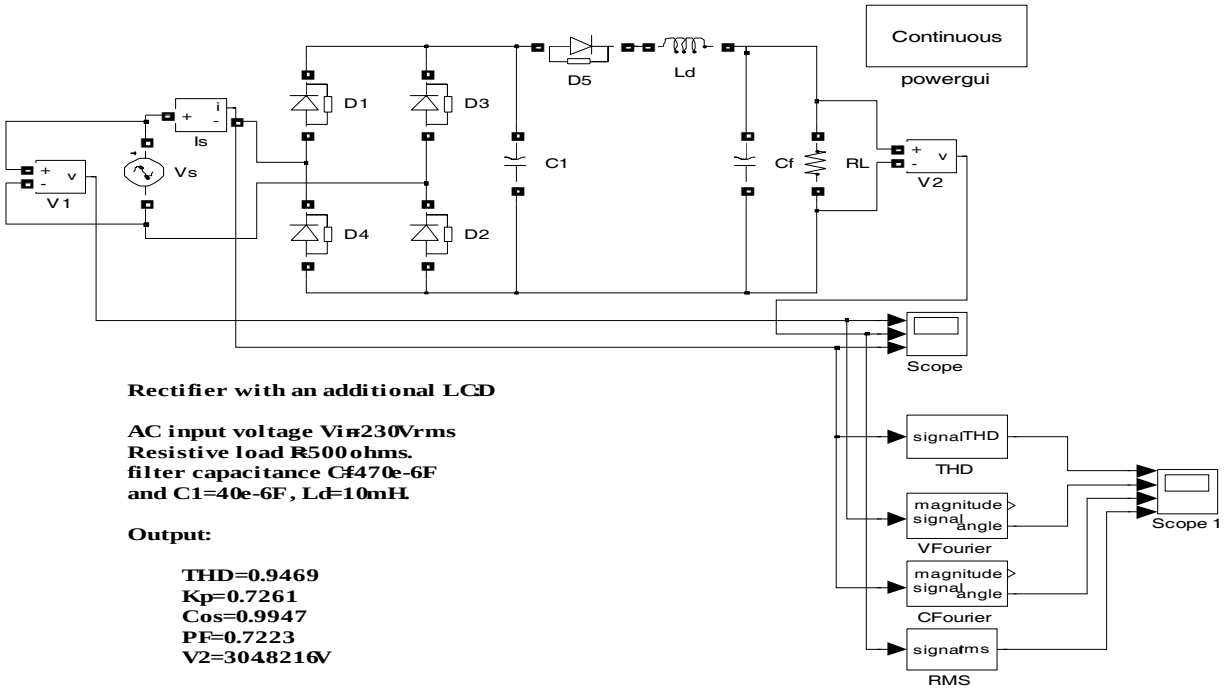
Capacitor Fed Rectifier

Ac input voltage Vin=230 Vrms
Resistive Load R=500ohms
Filter Capacitance Cf=4700e-6F
and Ca=16e-6F.

Output:

THD=0.1904
Kp=0.9824
Cos=0.0760
PF=0.0747
V2=18.8403V

7. Simulink model for fig 2.7



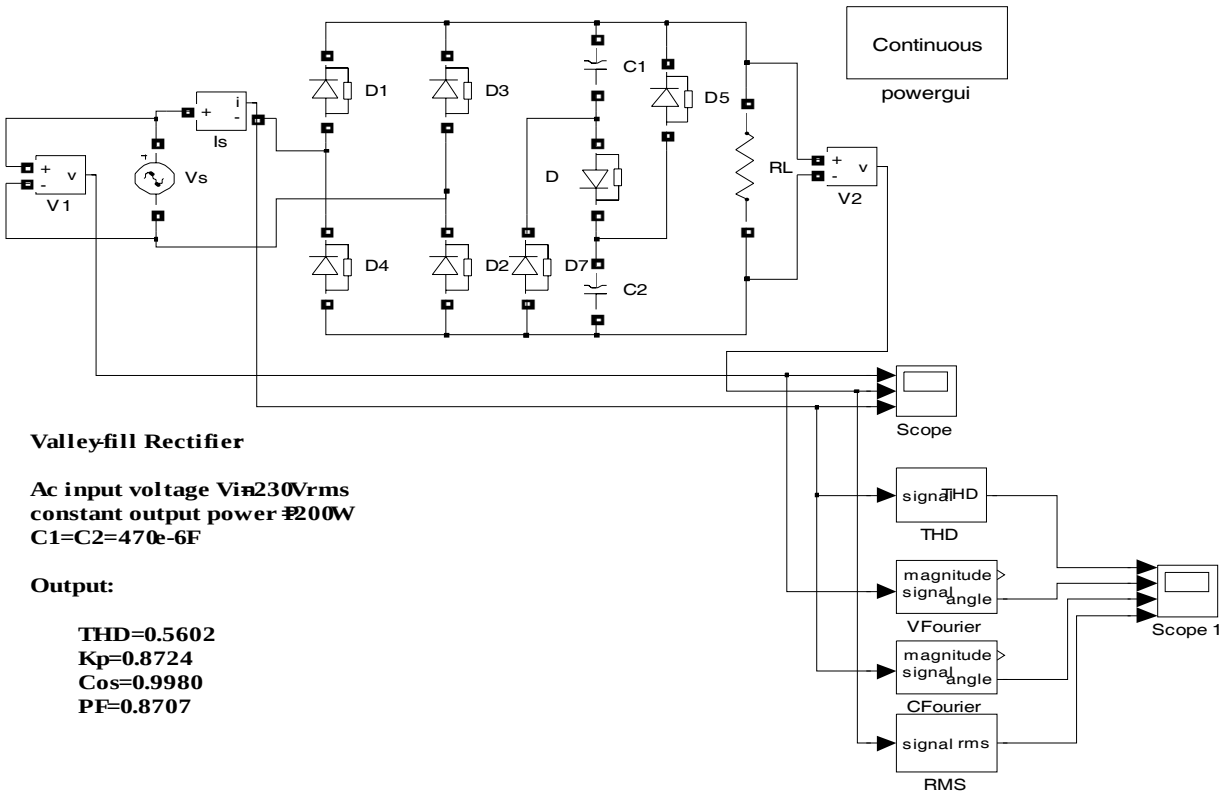
Rectifier with an additional LCD

AC input voltage Vin=230Vrms
Resistive load R=500 ohms.
filter capacitance Cf=470e-6F
and C1=40e-6F, Ld=10mH

Output:

THD=0.9469
Kp=0.7261
Cos=0.9947
PF=0.7223
V2=3048216V

8. Simulink model for fig 2.8



Valley-fill Rectifier

Ac input voltage Vin=230Vrms
constant output power =200W
C1=C2=470e-6F

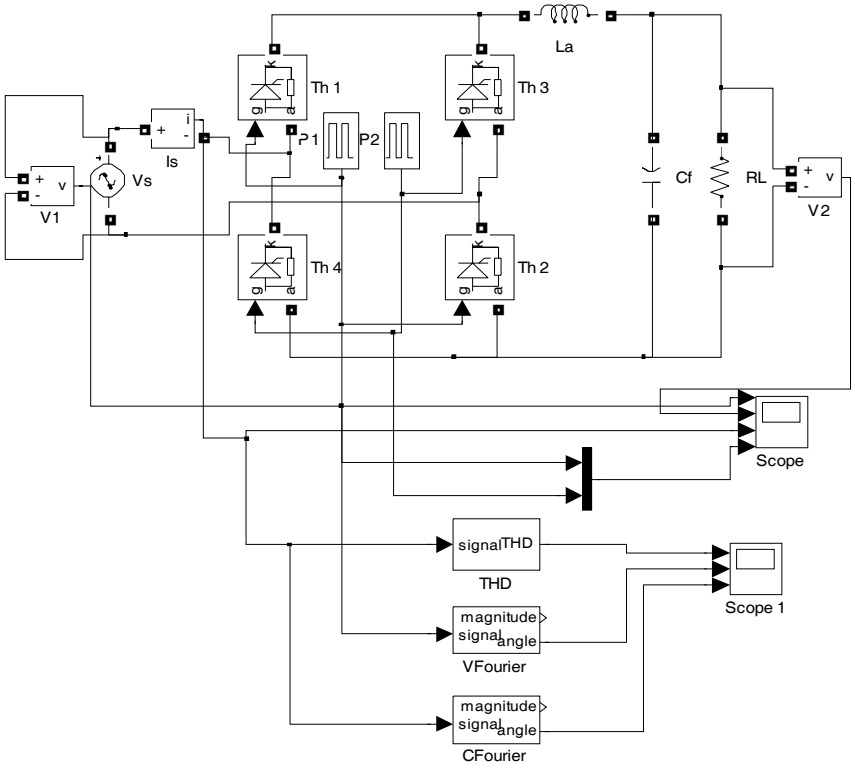
Output:

THD=0.5602
Kp=0.8724
Cos=0.9980
PF=0.8707

Appendix-II

The following Simulink models have been used for simulating the circuits given in chapter-3.

1. SImulink model for figure 3.1

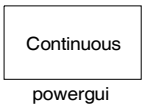


Low-frequency active PFC

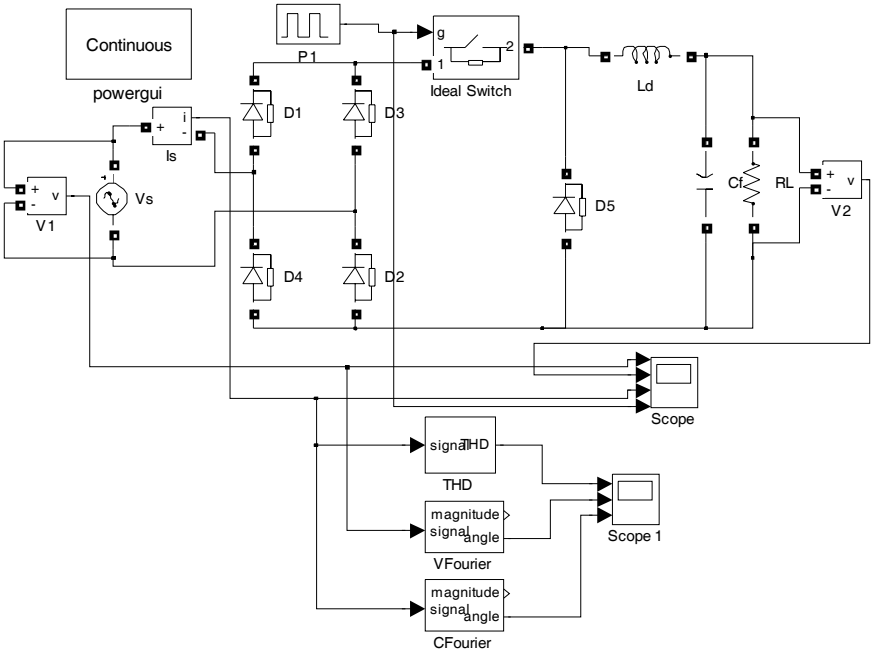
AC input voltage Vin=230Vrms
resistive load R=500 ohms
inductance La=200mH
filter Capacitance Vf=470e-6F
firing angle= 90deg

Output:

THD= 0.4375
Kp= 0.9161
Cos=0.8490
PF=0.7778



2. Simulink model for figure 3.2



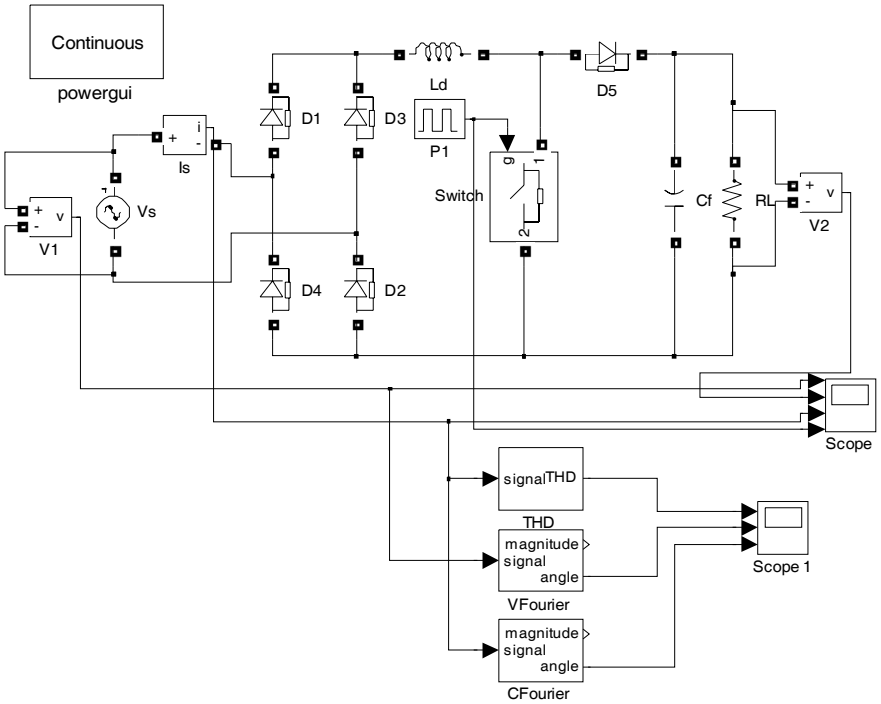
Low-frequency active PFC

AC input voltage Vin=230Vrms
filter Capacitance Cf=470e-6F
resistive load R=500ohms
Inductance Ld=200mH
Firing instance2e-3sec(i.e 36DEG)
duty cycle=50%

Output:

THD=0.8906
Kp=0.7468
Cos=0.9870
PF= 0.7371

3. Simulink model for figure 3.3



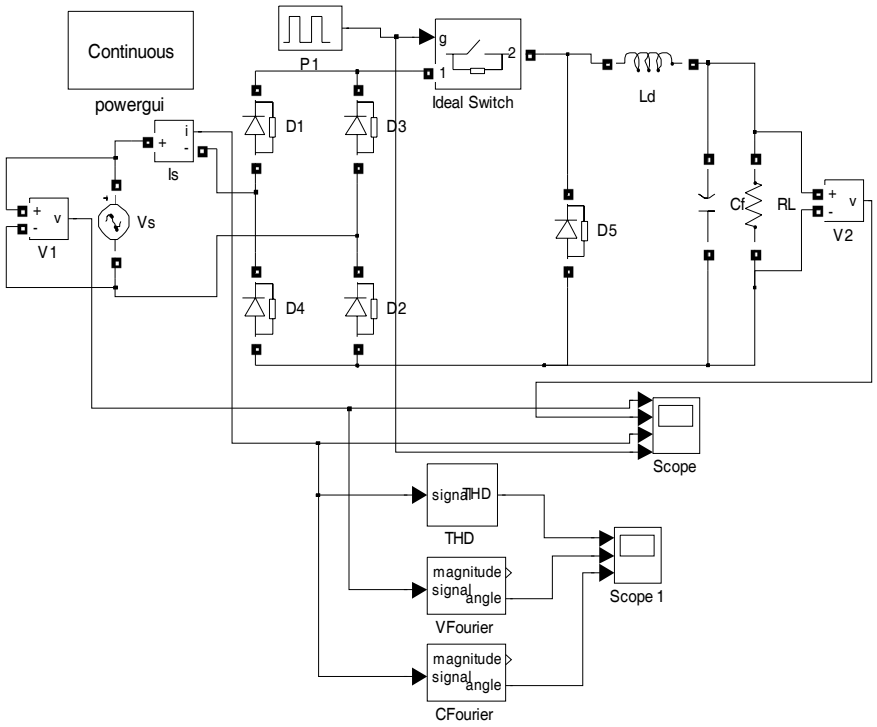
Low-frequency active PFC

AC input votlage Vin=230Vrms
filter capacitance Cf=470e-6F
resistive load R=500ohms
inductance Ld=200mH
firing instance2e-3sec(i.e 36DEG)
duty cycle= 50%

Output:

THD=0.3101
Kp=0.9551
Cos=0.8896
PF=0.8497

4. Simulink model for figure 3.5



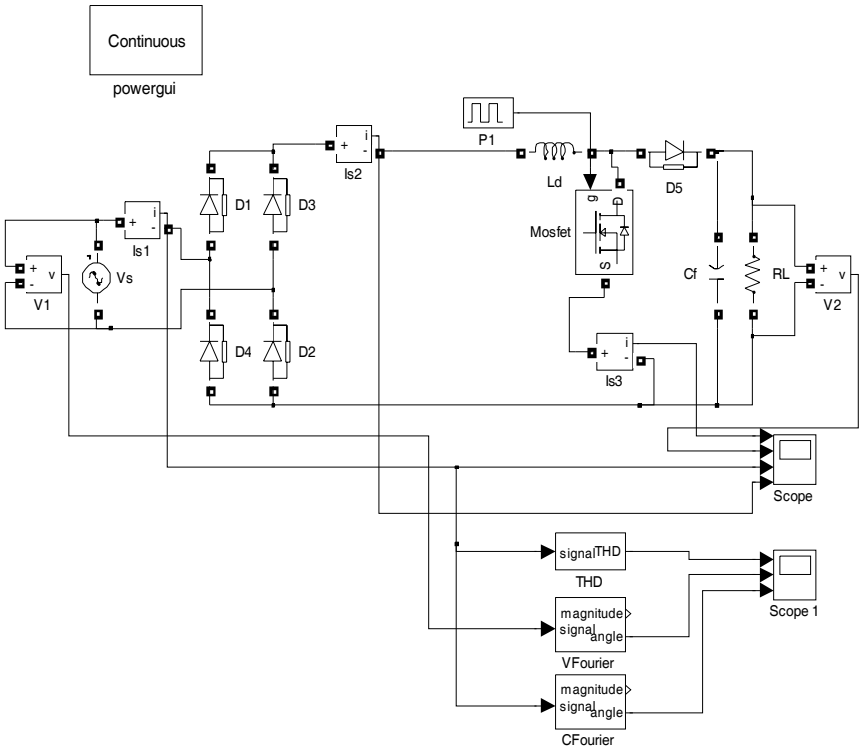
High-frequency active PFC
Buck converter

AC input voltage Vin=230Vrms
filter Capacitance Cf=470e-6F
resistive load R=500ohms
Inductance Ld=200mH
Firing instance=2e-3sec(i.e 36DEG)
duty cycle=90%

Output:

Kp=0.9591
Cos=0.9975
PF= 0.9367

5. Simulink model for figure 3.6



High-freq active PFC
Vin=230Vrms
Ld=50mH
Cf=470e-6F
R=500ohms
triggering pulse
period=1e-4sec
duty cycle=50%

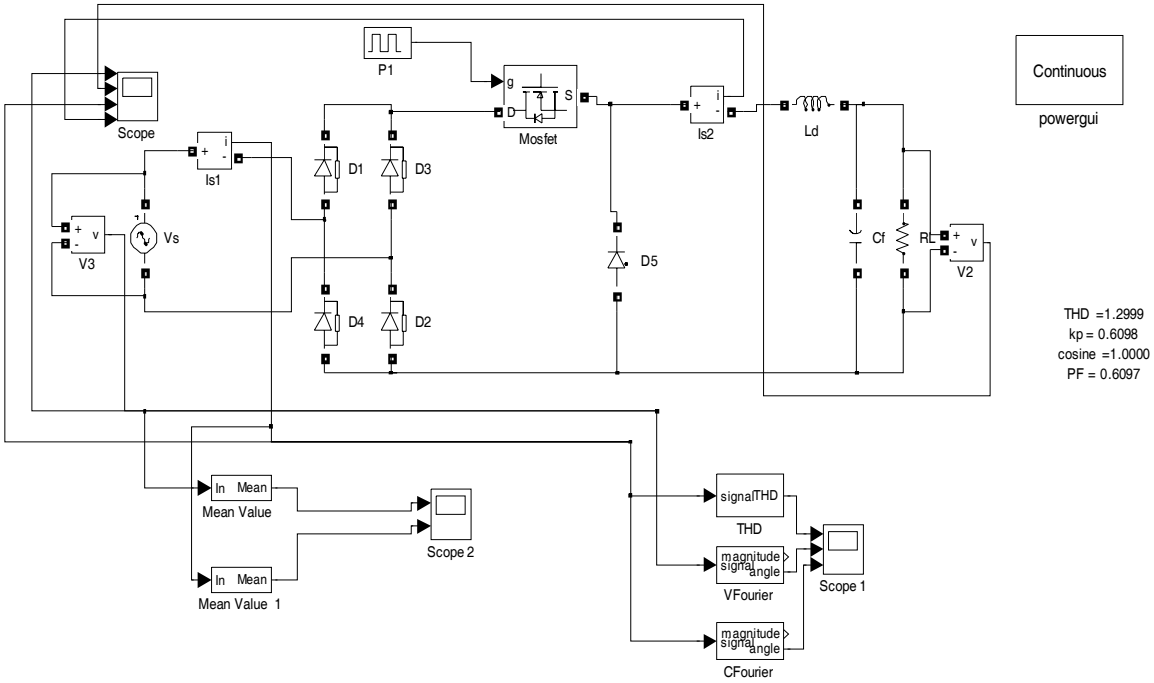
output

THD=0.1709
Kp=0.9857
Cos=0.9999
PF=0.9856

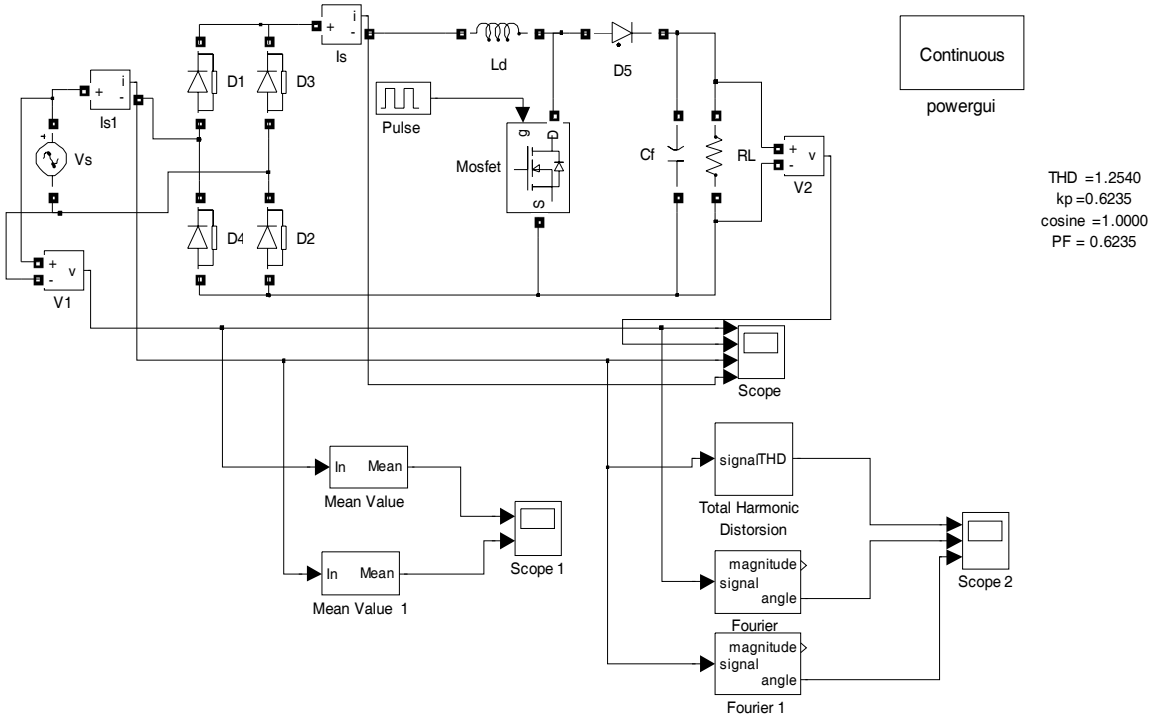
Appendix-III

The following Simulink models have been used for simulating the circuits given in chapter-4.

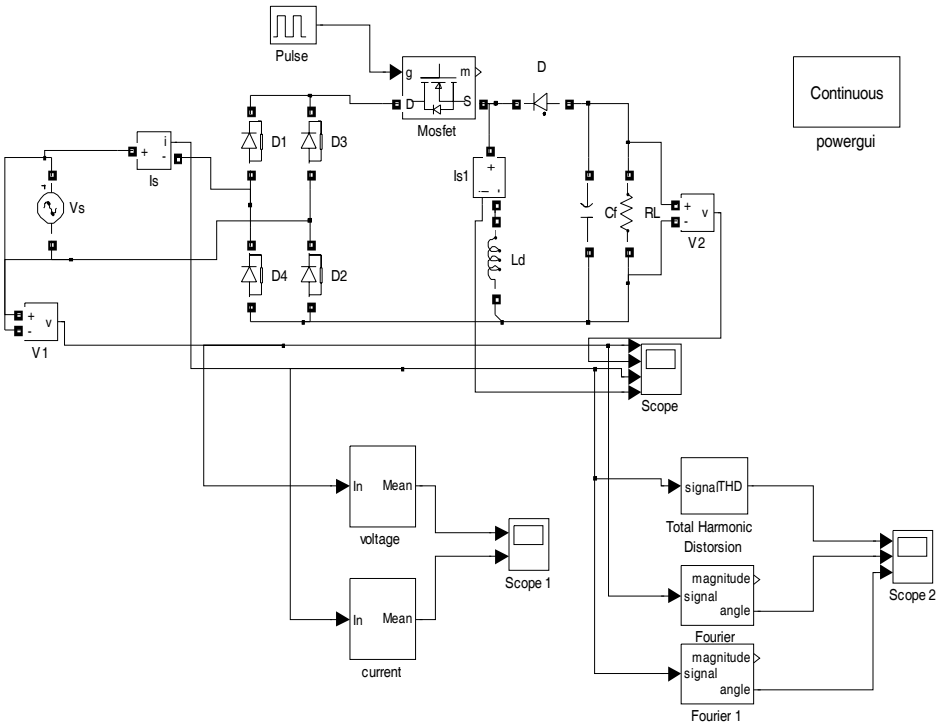
1.SImulink model for figure 4.2



2.SImulink model for figure 4.3



3.SImulink model for figure 4.4

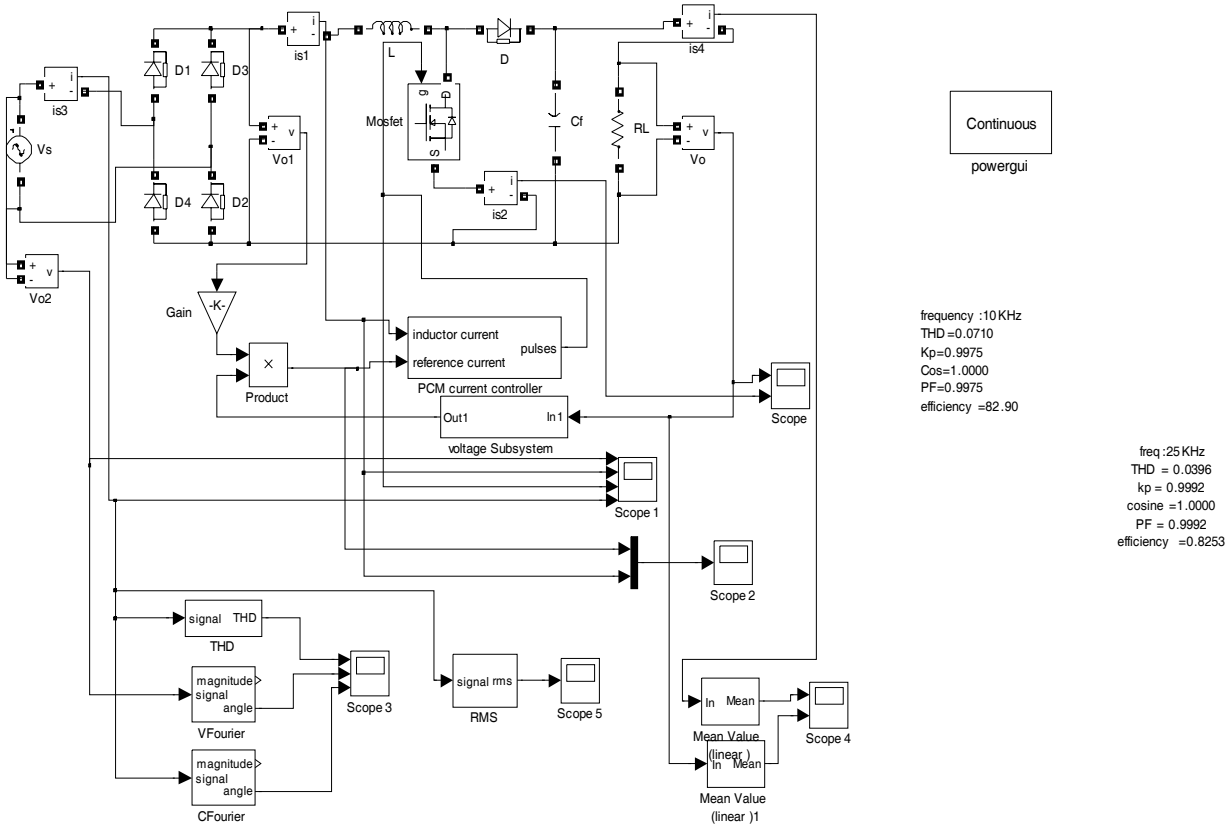


THD =1.2000
kp = 0.6402
cosine =1.0000
PF = 0.6402

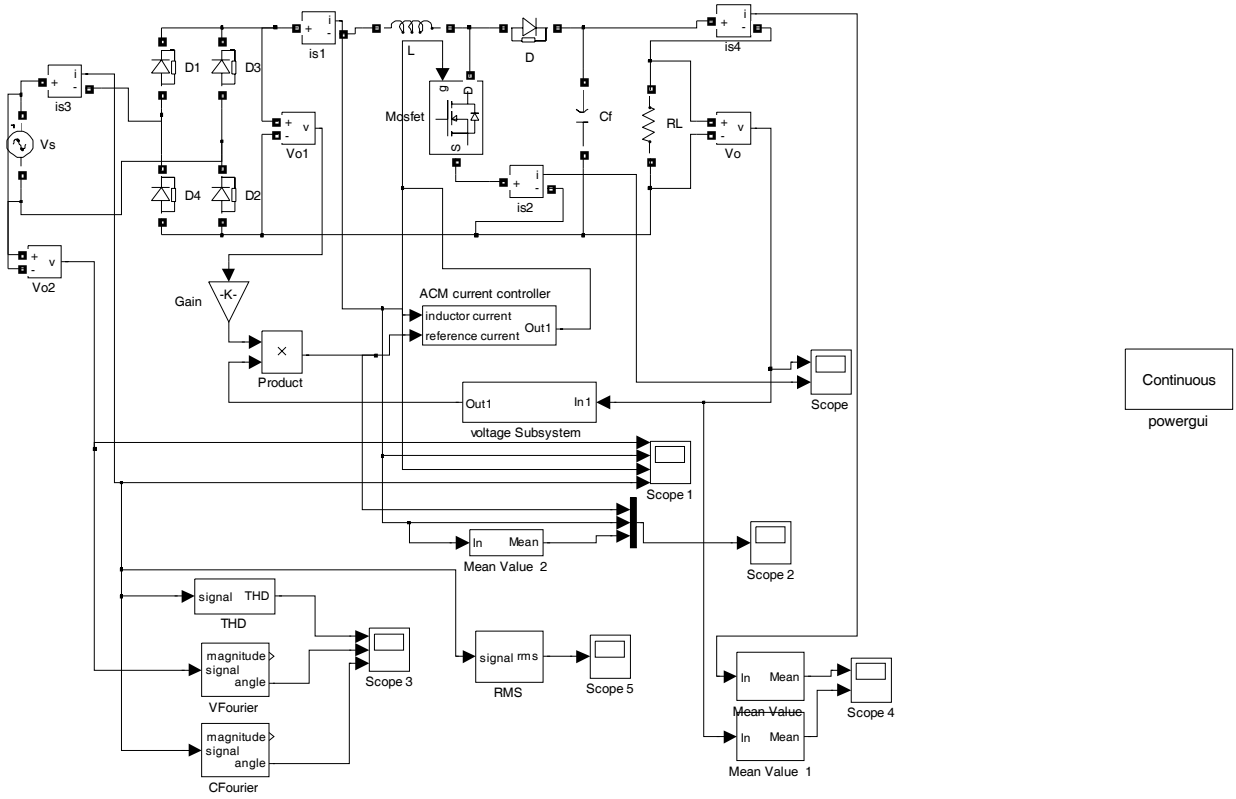
Appendix-IV

The following Simulink models have been used for simulating the circuits given in chapter-5.

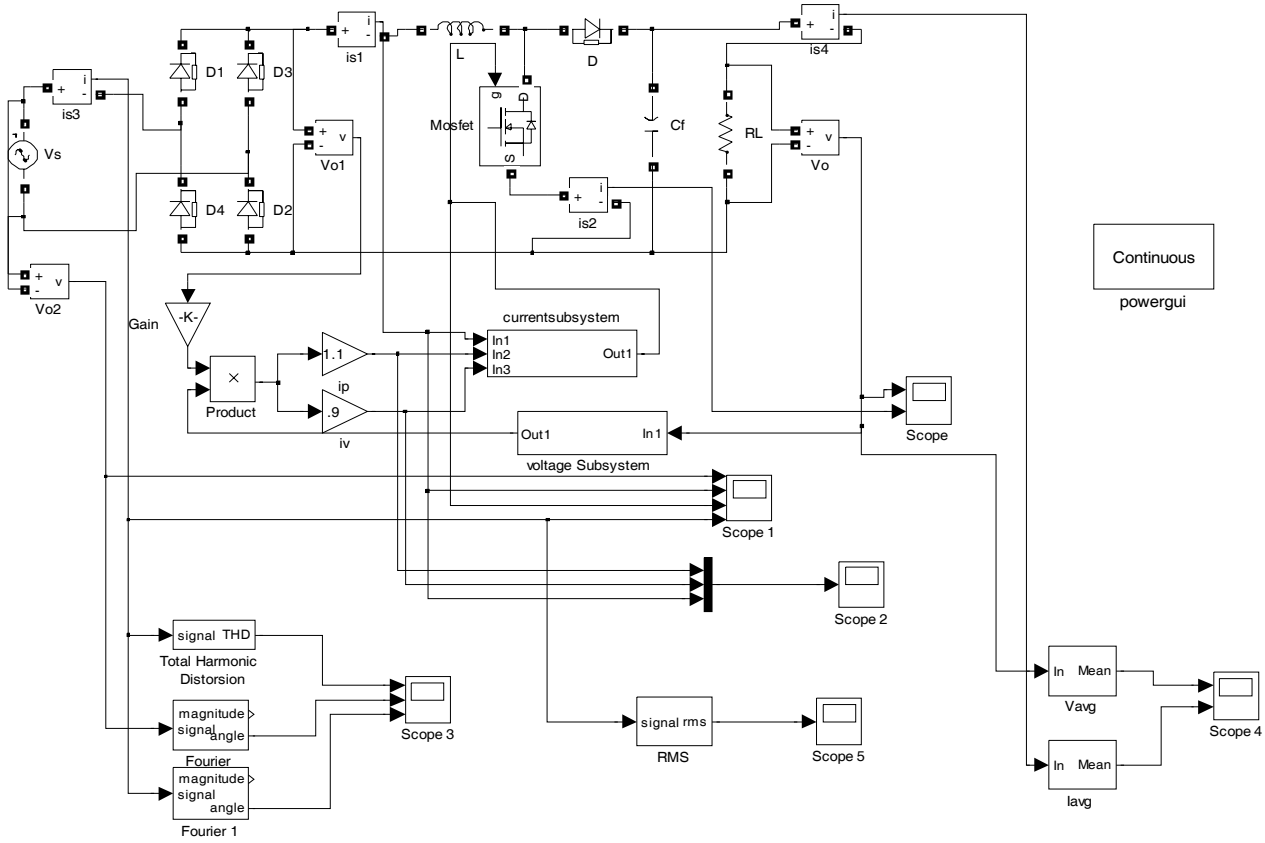
1.SImulink model for figure 5.2



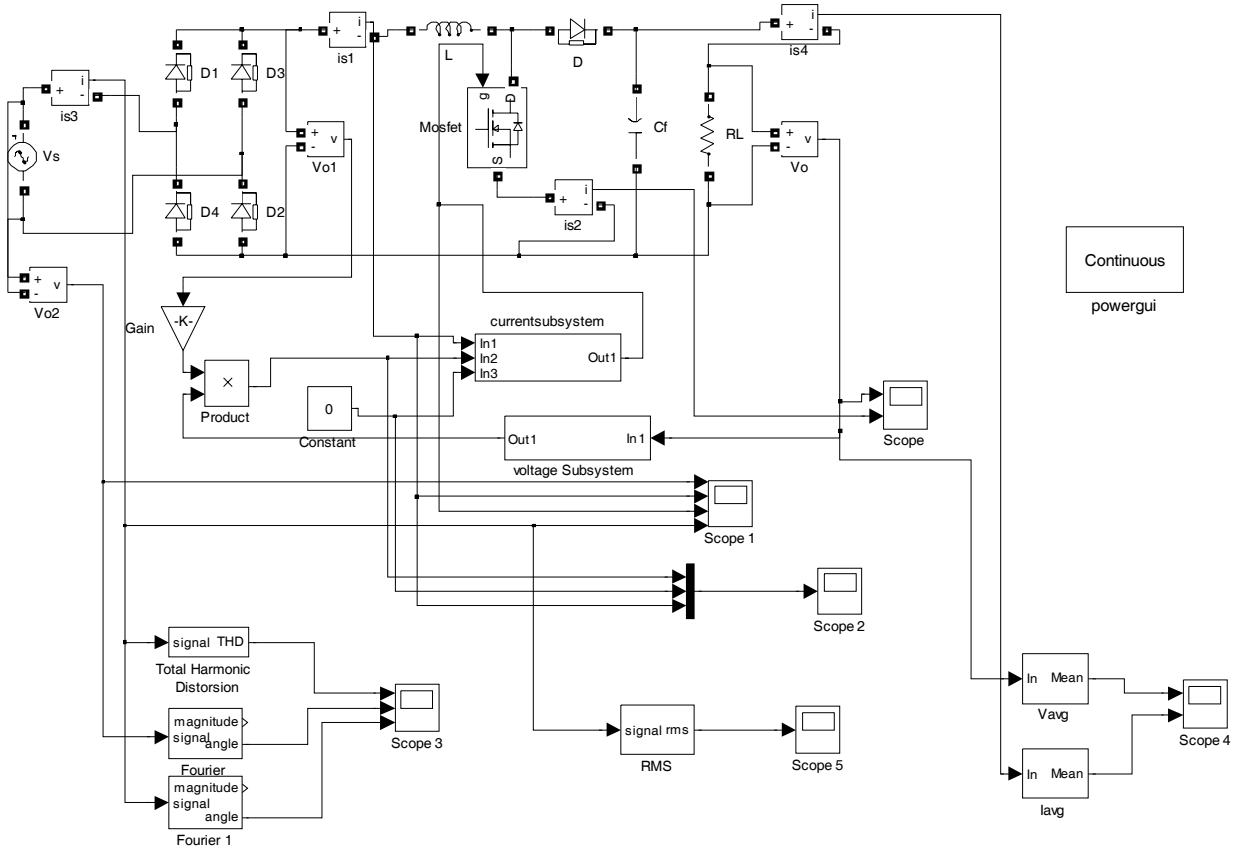
2.SImulink model for figure 5.3



3.SImulink model for figure 5.4



4.SImulink model for figure 5.5



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