DESIGN AND ANALYSIS OF EFFICIENT PHASE LOCKED LOOP FOR FAST PHASE AND FREQUENCY ACQUISITION

A THESIS SUBMITTED IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF

Master of Technology

in

VLSI Design and Embedded Systems

By

BIBHU PRASAD PANDA

ROLL NO. 209EC2132

Department of Electronics and Communication Engineering

National Institute Of Technology

Rourkela

2011

DESIGN AND ANALYSIS OF AN EFFICIENT PHASE LOCKED LOOP FOR FAST PHASE AND FREQUENCY ACQUISITION

A THESIS SUBMITTED IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF

Master of Technology

in

VLSI Design and Embedded Systems

By

BIBHU PRASAD PANDA
ROLL NO. 209EC2132

Under the Guidance of

Prof. D. P. ACHARYA

Department of Electronics and Communication Engineering

National Institute Of Technology

Rourkela
2011

National Institute Of Technology
Rourkela

CERTIFICATE

This is to certify that the thesis entitled, **"Design and Analysis of an Efficient Phase Locked Loop for Fast Phase and Frequency Acquisition "** submitted by **Bibhu Prasad Panda** in partial fulfillment of the requirements for the award of Master of Technology Degree in Electronics & Communication Engineering with specialization in **"***VLSI Design and Embedded System***"** at the National Institute of Technology, Rourkela is an authentic work carried out by him under my supervision and guidance.

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other University / Institute for the award of any Degree or Diploma.

Date:

Prof. D. P. Acharya
Dept. of Electronics & Communication Engg.
National Institute of Technology
Rourkela-769008

Acknowledgement

This project is by far the most significant accomplishment in my life and it would be impossible without people (especially my family) who supported me and believed in me.

I am thankful to **Prof. D. P. Acharya,** Associate Professor in the Department of Electronics and Communication Engineering, NIT Rourkela for giving me the opportunity to work under him and lending every support at every stage of this project work. I truly appreciate and value him esteemed guidance and encouragement from the beginning to the end of this thesis. I am indebted to his for having helped me shape the problem and providing insights towards the solution. His trust and support inspired me in the most important moments of making right decisions and I am glad to work with him.

I want to thank all my teachers **Prof. K.K. Mahapatra, Prof. S.K. Patra, Prof. G.S. Rath, Prof. S. Meher, Prof. N.V.L.N. Murthy** and **Prof. S. Ari** for providing a solid background for my studies and research thereafter.

I am also very thankful to all my classmates and seniors of VLSI lab-I especially Mr Ayaskanta, Mr Prakash, Mr Jaganath and all my friends who always encouraged me in the successful completion of my thesis work.

BIBHU PRASAD PANDA

ROLL No: 209EC2132

Dedicated to my Parents

Table of Contents

Abstract

The most versatile application of the phase locked loops (PLL) is for clock generation and clock recovery in microprocessor, networking, communication systems, and frequency synthesizers. Phase locked-loops (PLLs) are commonly used to generate well-timed on-chip clocks in high-performance digital systems. Modern wireless communication systems employ Phase Locked Loop (PLL) mainly for synchronization, clock synthesis, skew and jitter reduction. Because of the increase in the speed of the circuit operation, there is a need of a PLL circuit with faster locking ability. Many present communication systems operate in the GHz frequency range. Hence there is a necessity of a PLL which must operate in the GHz range with less lock time. PLL is a mixed signal circuit as its architecture involves both digital and analog signal processing units. The present work focuses on the redesign of a PLL system using the 90 nm process technology (GPDK090 library) in CADENCE Virtuoso Analog Design Environment. Here a current starved ring oscillator has been considered for its superior performance in form of its low chip area, low power consumption and wide tuneable frequency range. The layout structure of the PLL is drawn in CADENCE VirtuosoXL Layout editor. Different types of simulations are carried out in the Spectre simulator. The pre and post layout simulation results of PLL are reported in this work. It is found that the designed PLL consumes 11.68mW power from a 1.8V D.C. supply and have a lock time 280.6 ns. As the voltage controlled oscillator (VCO) is the heart of the PLL, so the optimization of the VCO circuit is also carried out using the convex optimization technique. The results of the VCO designed using the convex optimization method is compared with traditional method.

Table of Figures

List of Tables

CHAPTER 1

INTRODUCTION

1.1 Motivation

Phase locked loop (PLL) [1-3] is the heart of the many modern electronics as well as communication system. Recently plenty of the researches have conducted on the design of phase locked loop (PLL) circuit and still research is going on this topic. Most of the researches have conducted to realize a higher lock range PLL with lesser lock time [4] and have tolerable phase noise. The most versatile application of the phase locked loops (PLL) is for clock generation and clock recovery in microprocessor, networking, communication systems, and frequency synthesizers. Phase locked-loops (PLLs) are commonly used to generate well-timed on-chip clocks in high-performance digital systems. Modern wireless communication systems employ Phase Locked Loop (PLL) mainly for synchronization, clock synthesis, skew and jitter reduction [5]. Phase locked loops find wide application in several modern applications mostly in advance communication and instrumentation systems. PLL being a mixed signal circuit involves design challenge at high frequency.

Since its inspection in early 1930s, where it was used in the synchronization of the horizontal and vertical scans of television, it has come to an advanced form of integrated circuit (IC). Today found uses in many other applications. The first PLL ICs were available around 1965; it was built using purely analog component. Recent advances in integrated circuit design techniques have led to the development of high performance PLL which has become more economical and reliable. Now a whole PLL circuit can be integrated as a part of a larger circuit on a single chip.

There are mainly five blocks in a PLL. These are phase frequency detector (PFD), charge pump (CP), low pass loop filter (LPF), voltage controlled oscillator (VCO) and frequency divider. Presently almost all communication and electronics devices operate at a higher

frequency, so for that purpose we need a faster locking PLL. So there are a lot of challenges in designing the mentioned different blocks of the PLL to operate at a higher frequency. And these challenges motivated me towards this research topic. In this work mainly the faster locking of the PLL is concentrated by properly choosing the circuit architectures and parameters. The optimization of the VCO circuit is also carried out in this work to get a better frequency precision.

1.2 Organization of Thesis

Before going into the details of the PLL, the motivation behind this work is mentioned in the Chapter 1 of the thesis. Chapter 2 briefly describes the whole PLL system. An introduction to the PLL circuit is mentioned in the section 2.1. Section 2.2 contains the detail architecture of the whole PLL system. Different types of PLLs are mentioned in the section 2.3. Section 2.4 explains the basic terms used in the PLL system while the consecutive sections give the details about the noise and application of the PLL.

Chapter 3 builds the concepts of optimization. Definition of optimization technique and different circuit optimization techniques are presented in section 3.1 and 3.2 respectively. Section 3.3 gives the brief outline of the concept of geometric programming and convex optimization. The optimization of the CSVCO circuit is explained in section 3.4.

The design and synthesis of the PLL is described in Chapter 4. The different design environments used in this work is mentioned in the section 4.1. The adopted design procedure is explained in section 4.2. Section 4.3 gives the design specifications and parameters of the work.

The simulation results of the different circuits used in the PLL are depicted in the different sections of the Chapter 5. The performance of the CSVCO designed using convex optimization is compared with that of the traditional method in section 5.3. Section 5.5 gives the different

simulation results of the PLL and its performance comparison between schematic and post layout level. At last Chapter 6 provides the conclusion that inferred from the work.

CHAPTER 2

PHASE LOCKED LOOP

2.1 Introduction

A PLL is a closed-loop feedback system that sets fixed phase relationship between its output clock phase and the phase of a reference clock. A PLL is capable of tracking the phase changes that falls in this bandwidth of the PLL. A PLL also multiplies a low-frequency reference clock CK_{ref} to produce a high-frequency clock CK_{out} this is known as clock synthesis.

A PLL has a negative feedback control system circuit. The main objective of a PLL is to generate a signal in which the phase is the same as the phase of a reference signal. This is achieved after many iterations of comparison of the reference and feedback signals. In this lock mode the phase of the reference and feedback signal is zero. After this, the PLL continues to compare the two signals but since they are in lock mode, the PLL output is constant.

The basic block diagram of the PLL is shown in the Figure 2.1. In general a PLL consists of five main blocks:

1. Phase Detector or Phase Frequency Detector (PD or PFD)
2. Charge Pump (CP)
3. Low Pass Filter (LPF)
4. Voltage Controlled Oscillator (VCO)
5. Divide by N Counter

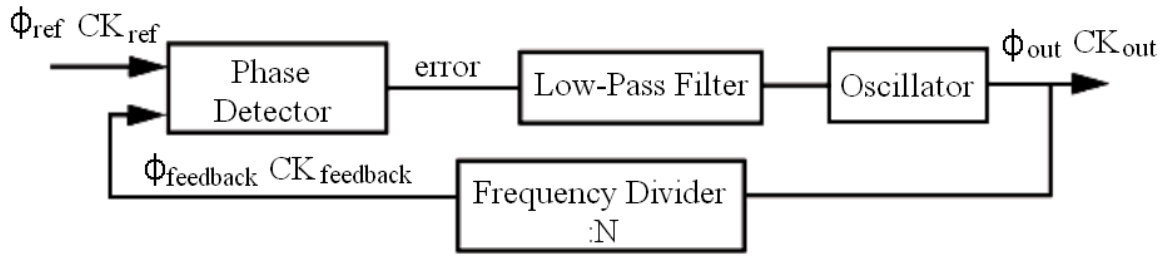

Figure2.1 Basic block diagram of a PLL

The “Phase frequency Detector” (PFD) is one of the main parts in PLL circuits. It compares the phase and frequency difference between the reference clock and the feedback clock. Depending upon the phase and frequency deviation, it generates two output signals “UP” and “DOWN”. The “Charge Pump” (CP) circuit is used in the PLL to combine both the outputs of the PFD and give a single output. The output of the CP circuit is fed to a “Low Pass Filter” (LPF) to generate a DC control voltage. The phase and frequency of the “Voltage Controlled Oscillator” (VCO) output depends on the generated DC control voltage. If the PFD generates an “UP” signal, the error voltage at the output of LPF increases which in turn increase the VCO output signal frequency. On the contrary, if a “DOWN” signal is generated, the VCO output signal frequency decreases. The output of the VCO is then fed back to the PFD in order to recalculate the phase difference, and then we can create closed loop frequency control system.

2.2 PLL Architecture

The architecture of a charge-pump PLL is shown in Figure 2.2. A PLL comprises of several components. They are (1) phase or phase frequency detector, (2) charge pump, (3) loop filter, (4) voltage-controlled oscillator, and (5) frequency divider. The functioning of each block is briefly explained below.

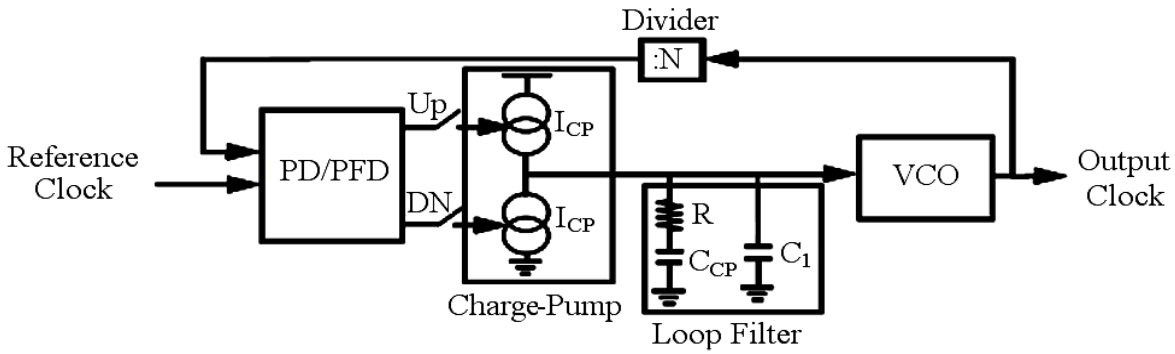

Figure2.2 Architecture of a PLL

2.2.1 Phase Frequency Detector

The “Phase frequency Detector” (PFD) is one of the main part in PLL circuits. It compares the phase and frequency difference between the reference clock and the feedback clock. Depending upon the phase and frequency deviation, it generates two output signals “UP” and “DOWN”. Figure 2.3 shows a traditional PFD circuit.

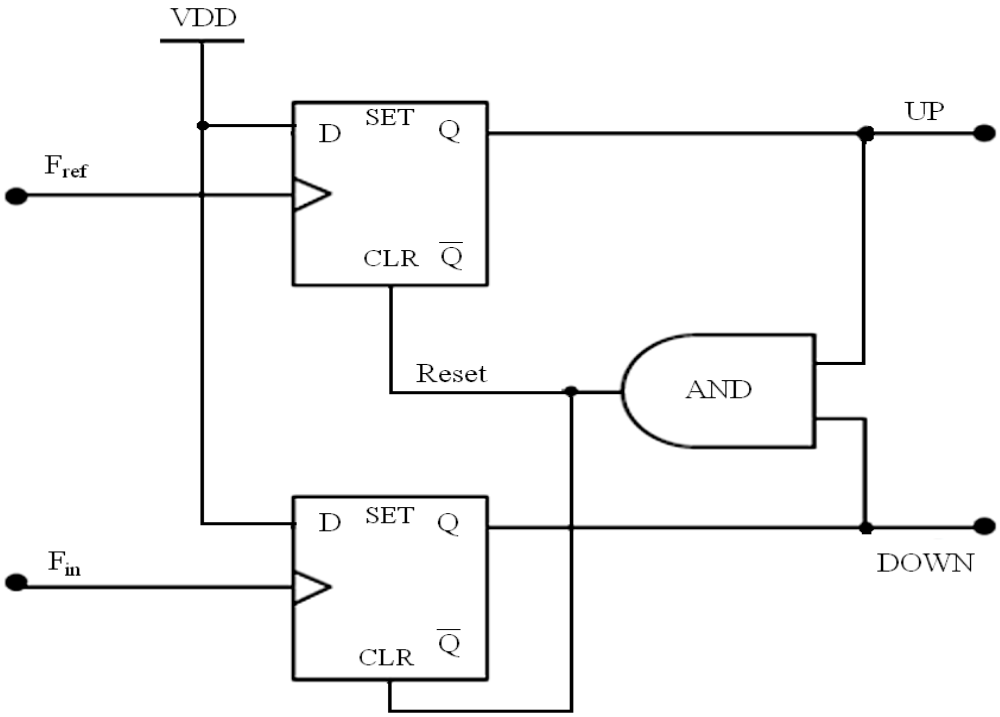

Figure2.3 Block diagram of a traditional PFD circuit

If there is a phase difference between the two signals, it will generate “UP” or “DOWN” synchronized signals. When the reference clock rising edge leads the feedback input clock rising edge “UP” signal goes high while keeping “DOWN” signal low. On the other hand if the feedback input clock rising edge leads the reference clock rising edge “DOWN” signal goes high and “UP” signal goes low. Fast phase and frequency acquisition PFDs [6-7] are generally preferred over traditional PFD.

2.2.2 Charge Pump and Loop Filter

Charge pump circuit is an important block of the whole PLL system. It converts the phase or frequency difference information into a voltage, used to tune the VCO. Charge pump circuit is used to combine both the outputs of the PFD and give a single output which is fed to the input of the filter. Charge pump circuit gives a constant current of value I_{PDI} which should be insensitive to the supply voltage variation [8]. The amplitude of the current always remains same but the polarity changes which depend on the value of the "UP" and "DOWN" signal. The schematic diagram of the charge pump circuit with loop filter is shown in the Figure 2.4.

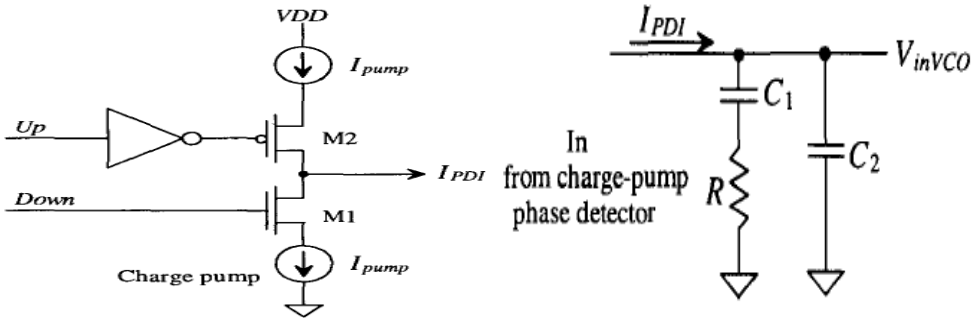

Figure2.4 Schematic diagram of the charge pump circuit with loop filter

When the UP signal goes high M2 transistor turns ON while M1 is OFF and the output current is I_{PDI} with a positive polarity. When the down signal becomes high M1 transistor turns ON while M2 is OFF and the output current is I_{PDI} with a negative polarity. The charge pump output current [3] is given by

$$I_{PDI} = \frac{I_{PUMP} — (I_{PUMP})}{4\pi} \times \Delta\Phi$$

$$= \frac{2I_{PUMP}}{4\pi} \times \Delta\Phi$$

$$= \frac{I_{PUMP}}{2\pi} \times \Delta\Phi$$

$$= K_{PDI} \times \Delta\Phi \quad (1)$$

$$\text{Where } K_{PDI} = \frac{I_{PUMP}}{2\pi} \text{ (amps/radian)} \quad (2)$$

The passive low pass loop filter is used to convert back the charge pump current into the voltage. The filter should be as compact as possible [9].The output voltage of the loop filter controls the oscillation frequency of the VCO. The loop filter voltage will increase if F_{ref} rising edge leads F_{in} rising edge and will decrease if F_{in} rising edge leads F_{ref} rising edge. If the PLL is in locked state it maintains a constant value.

The VCO input voltage is given by

$$V_{invco} = K_F \times I_{PDI} \quad (3)$$

Where K_F is the gain of the loop filter.

2.2.3 Voltage Controlled Oscillator

An oscillator is an autonomous system which generates a periodic output without any input. The most popular type of the VCO circuit is the current starved voltage controlled oscillator (CSVCO). Here the number of inverter stages is fixed with 5. The simplified view of a single stage current starved oscillator is shown in the Figure 2.5.

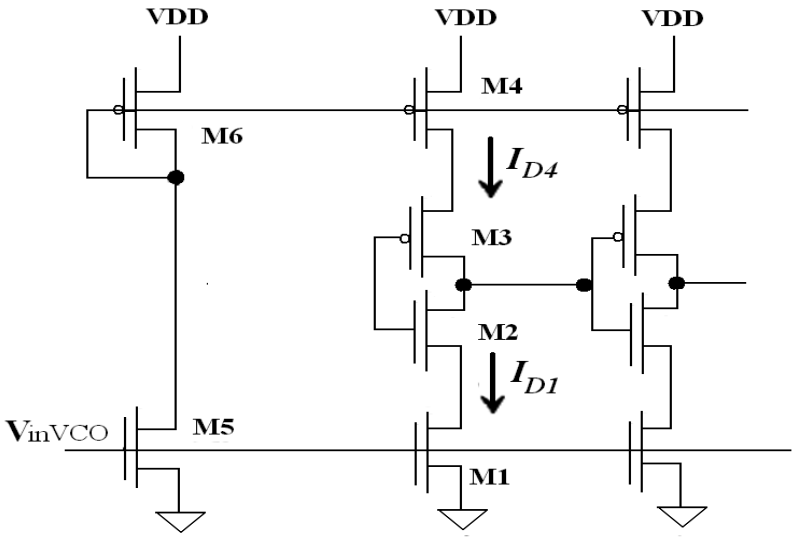

Figure2.5 Simplified view of a current starved VCO

Transistors M2 and M3 operate as an inverter while M1 and M4 operate as current sources. The current sources, Ml and M4, limit the current available to the inverter, M2 and M3; in other words, the inverter is starved for current. The desired center frequency of the designed circuit is 1GHz with a supply of 1.8V. The CSVCO is designed both in usual manner as mentioned in [3], [10, 11]. The general circuit diagram of the current starved voltage controlled oscillator is shown in the Figure 2.6.

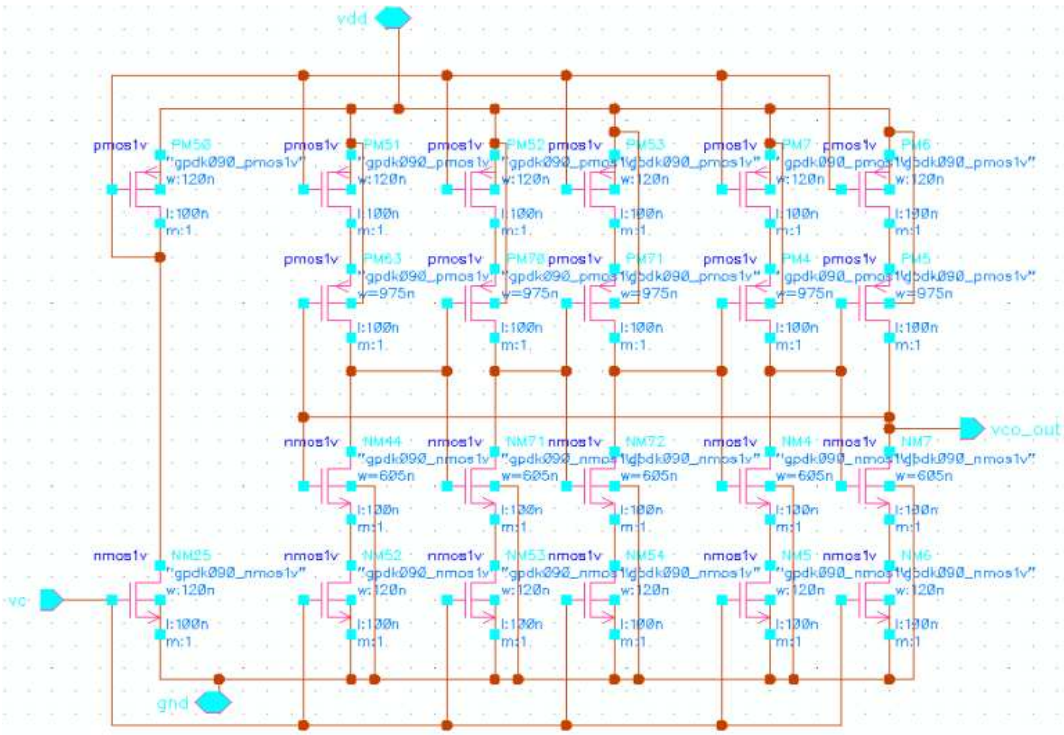

Figure2.6 Circuit diagram of a current starved VCO

To determine the design equations for the CSVCO, consider the simplified view of VCO in Figure 2.5. The total capacitance on the drains of M2 and M3 is given by

$$C_{tot} = \frac{5}{2} C_{ox}(L_p W_p + L_n W_n) \tag{4}$$

The time it takes to charge C_{tot} from zero to V_{SP} with the constant current I_{D4} is given by

$$t_1 = \frac{V_{SP}}{I_{D4}} \times C_{tot} \tag{5}$$

While the time it takes to discharge C_{tot} from V_{DD} to V_{SP} is given by

$$t_1 = \frac{V_{DD} - V_{SP}}{I_{D1}} \times C_{tot} \quad (6)$$

If we set $I_{D4} = I_{D1} = I_D$ then the sum of t_1 and t_2 is given by

$$t_1 + t_2 = \frac{V_{DD}}{I_D} \times C_{tot} \quad (7)$$

The oscillation frequency of CSVCO for N number of stage is

$$f_{osc} = \frac{1}{N(t_1 + t_2)} = \frac{I_D}{NC_{tot}V_{DD}} \quad (8)$$

This is equal to f_{center} when $V_{invco} = \frac{V_{DD}}{2}$ (9)

The gain of the VCO is given by

$$K_{VCO} = \frac{f_{max} - f_{min}}{V_{max} - V_{min}} \ {}^{Hz}/_{V} \quad (10)$$

2.2.4 Frequency Divider

The output of the VCO is fed back to the input of PFD through the frequency divider circuit. The frequency divider in the PLL circuit forms a closed loop. It scales down the frequency of the VCO output signal. A simple D flip flop (DFF) acts as a frequency divider circuit. The schematic of a simple DFF based divide by 2 frequency divider circuit is shown in the Figure 2.7.

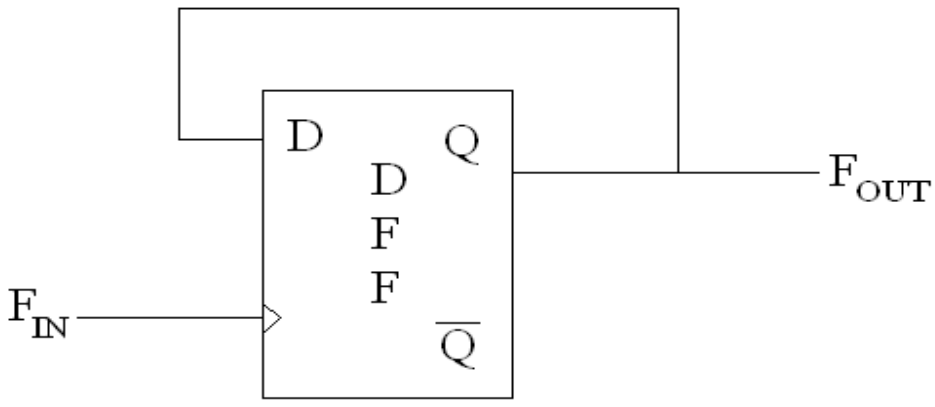

Figure2.7 Schematic of a simple DFF based divide by 2 frequency divider circuit

2.3 Types of PLL

There are mainly 4 types of PLL are available. They are

1. Liner PLL
2. Digital PLL
3. All Digital PLL
4. Soft PLL

2.4 Terms in PLL

2.4.1 Lock in Range

Once the PLL is in lock state what is the range of frequencies for which it can keep itself locked is called as lock in range. This is also called as tracking range or holding range.

2.4.2 Capture Range

When the PLL is initially not in lock, what frequency range can make PLL lock is called as capture range. This is also known as acquisition range. This is directly proportional to the LPF bandwidth. Reduction in the loop filter bandwidth thus improves the rejection of the out of band signals, but at the same time the capture range decreases, pull in time becomes larger and phase margin becomes poor.

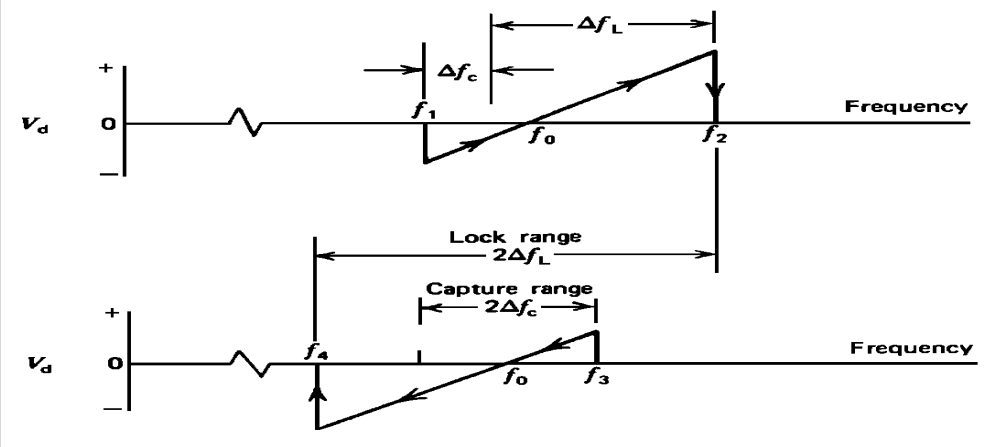

Figure2.8 Illustration of lock and capture range

2.4.3 Pull in Time

The total time taken by the PLL to capture the signal (or to establish the lock) is called as Pull in Time of PLL. It is also called as Acquisition Time of PLL.

2.4.4 Bandwidth of PLL

Bandwidth is the frequency at which the PLL begins to lose the lock with reference.

2.5 Noises in PLL

The output of the practical system deviates from the desired response. This is because of the imperfections and noises in the system. The supply noise also affects the output noise of the PLL system [12]. There are mainly 4 types of noises. They are explained below.

2.5.1 Phase Noise

The phase fluctuation due to the random frequency variation of a signal is called as phase noise. This is mostly affected by oscillator's frequency stability. The main sources of the phase noise in PLL are oscillator noise [12-15], PFD and frequency divider circuit. The main components of the phase noise are thermal and flicker noise.

2.5.2 Jitter

A jitter is the short term-term variations of a signal with respect to its ideal position in time [16-19]. This problem negatively impacts the data transmission quality. Jitter and phase noise are closely related and can be computed one from another [18]. Deviation from the ideal position can occur on either leading edge or trailing edge of signal. Jitter may be induced and coupled onto a clock signal from several different sources and is not uniform over all frequencies. Excessive jitter can increase bit error rate (BER) of communication signal [19]. In digital system Jitter leads to violation in time margins, causing circuits to behave improperly.

2.5.3 Spur

Non-desired frequency content not related to the frequency of oscillation and its harmonics is called as “Spur”. There are mainly two types of spur. They are reference spur and fractional spur. Reference spur comes into picture in an integer PLL while fractional spur plays a major role in fractional PLL. When the PLL is in lock state the phase and frequency inputs to the PFD are essentially equal. There should not be any error output from the PFD. Since this can create problem, so the PFD is designed such that, in the locked state the current pulses from the CP will have a very narrow width as shown in the Figure 2.9. Because of this the input control voltage of the VCO is modulated by the reference signal and thus produces “Reference Spur” [20].

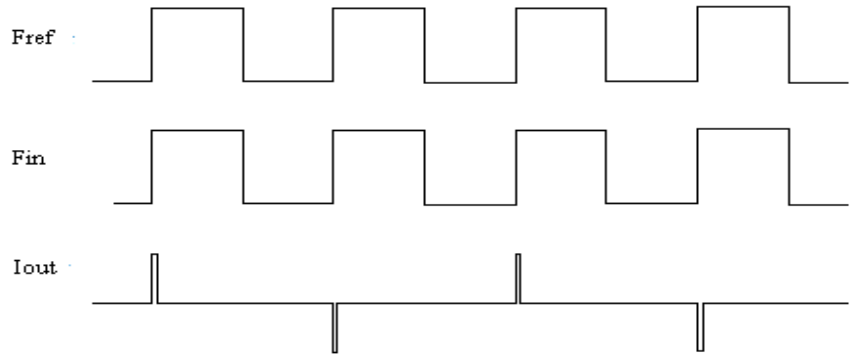

Figure2.9 Output current pulses from charge pump in the lock state

2.5.4 Charge Pump Leakage Current

When the CP output from the synthesizer is programmed to the high impedance state, in practice there should not be any current flow. But in practical some leakage current flows in the circuit and this is known as “charge pump leakage current” [20].

2.6 Applications of PLL

The demand of the PLL circuit increases day by day because of its wide application in the area of electronics, communication and instrumentation. The recent applications of the PLL circuits are in memories, microprocessors, hard disk drive electronics, RF and wireless transceivers, clock

recovery circuits on microcontroller boards and optical fiber receivers. Some of the PLL applications are mentioned below.

1. Frequency Synthesis

A frequency synthesizer is an electronic system for generating a range of frequencies from a single fixed time base or oscillator.

2. Clock Generation

Many electronic systems include processors of various sorts that operate at hundreds of megahertz. Typically, the clocks supplied to these processors come from clock generator PLLs, which multiply a lower-frequency reference clock (usually 50 or 100 MHz) up to the operating frequency of the processor. The multiplication factor can be quite large in cases where the operating frequency is multiple GHz and the reference crystal is just tens or hundreds of megahertz.

3. Carrier Recovery (Clock Recovery)

Some data streams, especially high-speed serial data streams (such as the raw stream of data from the magnetic head of a disk drive), are sent without an accompanying clock. The receiver generates a clock from an approximate frequency reference, and then phase-aligns to the transitions in the data stream with a PLL. This process is referred to as clock recovery.

4. Skew Reduction

This is one of the very popular and earliest uses of PLL. Suppose synchronous pair of data and clock lines enter a large digital chip. Since clock typically drives a large number of transistors and logic interconnects, it is first applied to large buffer. Thus, the clock distributed on chip may suffer from substantial skew with respect to data. This is an undesirable effect which reduces the timing budget for on-chip operations.

5. Jitter and Noise Reduction

One desirable property of all PLLs is that the reference and feedback clock edges be brought into very close alignment. The average difference in time between the phases of the two signals when the PLL has achieved lock is called the static phase offset. The variance between these phases is called tracking jitter. Ideally, the static phase offset should be zero, and the tracking jitter should be as low as possible.

CHAPTER 3

CONVEX OPTIMIZATION OF VCO IN PLL

3.1 What is an optimization technique?

Optimization technique is nothing but the finding of the action that optimizes i.e. minimizes or maximizes the result of the objective function. Optimization technique is applied to the circuits aiming at finding out the optimized circuit design parameter to achieve either the best performance or the desired performance. Optimization techniques are a set of most powerful tools that are used in efficiently handling the design resources and there by achieve the best result. Mainly optimization techniques are applied to the circuit for the selection of the component values, devices sizes, and value of the voltage or current source.

3.2 Types of circuit optimization method

There are mainly four types of circuit optimization methods exist. They are

1. Classical optimization
2. Knowledge based optimization
3. Global optimization method
4. Convex optimization and geometric programming

3.2.1 Classical Optimization Methods:

In case of analog circuit CAD, classical optimization methods [21], such as steepest descent, sequential quadratic programming, and Lagrange multiplier methods are mainly used. These methods are used with more complicated circuit models, including even full SPICE simulations in each iteration. This method can handle a wide variety of problem. For this there is a need of a set of performance measures and computation of one or more derivatives. The main disadvantage of the classical optimization methods is that the global optimal solution is not possible. This method fails to find a feasible design even one exist. This method gives only the local minima instead of global solution. Since many different initial designs are considered to get the global optimization, the method becomes slower. Because of the human intervention (to give “good”

initial designs), the method becomes less automated. The classical methods become slow if complex models are used.

3.2.2 Knowledge-Based Methods:

Knowledge-based and expert-systems methods such as genetic algorithm or evolution systems, systems based on Fuzzy logic, and heuristics-based systems have also been widely used in analog circuit CAD [21]. In case of knowledge based methods, there are few limitations on the types of problems, specifications, and performance measures that are to be considered. These methods do not require the computation of the derivatives. This is not possible to find a global optimal design solution using these methods. The final design is decided on the basis of the initial design chosen and the algorithm parameters. The disadvantage of the knowledge based methods is that they simply fail to find a feasible solution even when one may exist. There is a need of human intervention during the design and the training process.

3.2.3 Global Optimization Methods:

Global optimization methods such as branch and bound and simulated annealing are also used in analog circuit design [21]. These methods are guaranteed to find the global optimal design solution. The global optimal design is determined by the branch and bound methods unambiguously. In each iteration, a suboptimal feasible design and also a lower bound on the achievable performance is maintained by this method. This enables the algorithm to terminate non-heuristically, i.e., with complete confidence that the global design has been found within a given tolerance. The branch and bound method is extremely slow, with computation growing exponentially with problem size. The trapping in a locally optimal design can be avoided by using simulated annealing (SA). This method can compute the global optimal solution but not guaranteed. Since there is no real-time lower bound is available, so termination is heuristic. This

method can also handle a wide variety of performance indices and objects. The main advantage of SA is that it handles the continuous variables and discrete variables problems efficiently and reduces the chances of getting a non-globally optimal design. The only problem with this method is that it is very slow and can not guarantee a global optimal solution.

3.2.4 Convex Optimization and Geometric Programming Methods:

Geometric programming methods are special optimization problems in which the objective and constraint functions are all convex [22-24]. Convex optimization technique can solve the problems having a large number of variables and constraints very efficiently [22]. The main advantage of this method for which people generally adopt is that the method gives the global solution. Infeasibility is unambiguously detected. Since a lower bound on the achievable performance is given, so the method uses a completely non- heuristic stopping criterion.

3.3 Geometric programming and convex optimization

Geometric programming is a special type of optimization technique in which all the objective must be convex. Before applying this technique it has to confirm that whether the given problem is convex optimization problem or not. Convex optimization problem means the problem of minimizing a convex function subject to convex inequality constraints and linear equality constraints. In IC integration convex optimization and geometric programming has become a more efficient computational tool for optimization purpose. This method has an ability to handle thousands of variables and constraints and solve efficiently. The main advantage of convex optimization technique is that it gives the global optimized value and the robust design. The fact that geometric programs can be solved very efficiently has a number of practical consequences. For example, the method can be used to simultaneously optimize the design of a large number of circuits in a single large mixed-mode integrated circuit. The designs of the individual circuits are

coupled by constraints on total power and area, and by various parameters that affect the circuit coupling such as input capacitance, output resistance, etc. Convex optimization is used to find out the optimized value of these parameter and sizing of the devices in the circuit [25]. Another application is to use the efficiency to obtain robust designs i.e., designs that are guaranteed to meet a set of specifications over a variety of processes or technology parameter values. This is done by simply replicating the specifications with a (possibly large) number of representative process parameters, which is practical only because geometric programs with thousands of constraints are readily solved. A real valued function $f(x)$ defined on an interval (space) is called convex if

$$f(tx_1 + (1-t)x_2) \leq tf(x_1) + (1-t)f(x_2) \tag{11}$$

For every $t, 0 < t < 1$ and $x_1 \neq x_2$

In the Figure 3.1 function $f(x)$ is represented as a convex function on an interval.

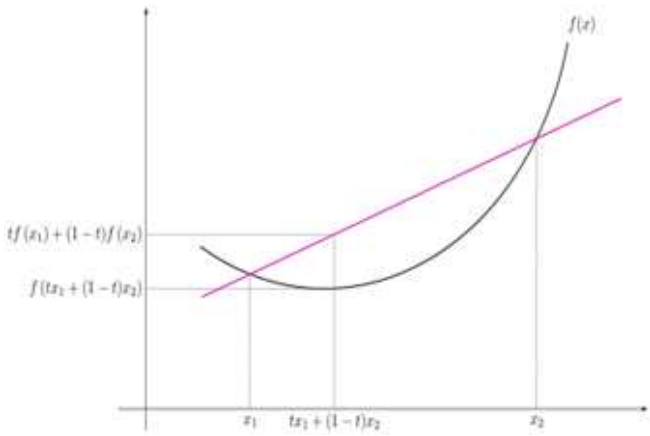

Figure3.1 Convex functions on an interval [26]

The convex optimization problem is in the form of minimize $f_0(x)$

Subjected to $f_i(x) \leq 1$, i=1, 2, 3…, m

$g_i(x) = 1$, i=1, 2, 3…, p

$x_i > 1$, i=1, 2, 3…, n

Where $f_i(x)$ is a posynomial function

$g_i(x)$ is a monomial function

Let $x_1, x_2 \dots \dots x_n$ be n real positive variables. We can denote the vector $(x_i, x_i \dots \dots x_i)$ of these variables as$x$. A function f is called a posynomial function of x if it has the form

$$f_i(x_1, x_2 \dots \dots x_n) = \sum_{k=1}^{t} C_k x_1^{\alpha_{1k}} x_2^{\alpha_{2k}} \dots \dots x_n^{\alpha_{nk}} \quad (12)$$

Where $C_j \geq 0$ and $\alpha_{ij} \epsilon \boldsymbol{R}$. The coefficients C_j must be nonnegative but the exponents α_{ij} can be any real numbers including negative or fractional. When there is exactly one nonzero term in the sum i.e. $t = 1$ and $C_1 > 0$, we call f is a monomial function.

3.3.1 Advantages:

- Handle thousands of variables and constraints and solve efficiently.
- Global optimization can be obtained.

3.3.2 Disadvantages:

- Strictly limited to types of problems, performance specification and objectives that can be handled.

3.4 Optimization of the VCO circuit

In my earlier design of the VCO circuit, the sizes of all the five inverter stages are same. Now the convex optimization technique is applied to find out the optimal scaling ratio of the different inverter stages to get the optimal design with a better performance. There are 5 inverter stages and the design has to give a delay of 100ps. The load capacitance of the VCO circuit is 65 fF. All these design constraints are formulated and applied to the convex optimization technique. Mainly optimization techniques are applied for selection of component values and transistor sizing.

In this work I have used the geometric programming technique to find out the optimized scaling ratio of the different stages in CSVCO to meet the desired center frequency with lesser deviation. Let x_i is the scaling ration of the ith stage, C_L is the load capacitance, and D is the total delay of the inverter stages then optimization problem is in the form of

Minimize sum (x_i)

Subjected to $C_L \leq C_{Lmax}$

$D \leq D_{max}$

Where C_{Lmax} and D_{max} are required design parameters and has a constant value.

CHAPTER 4

DESIGN AND SYNTHESIS OF PLL

4.1 Design Environment

The schematic level design entry of the circuits is carried out in the CADENCE Virtuoso Analog Design Environment. The layout of the PLL is designed in Virtuoso XL using GPDK090 library. In order to analyze the performances, these circuits are simulated in the Spectre simulator of CADENCE tool. Different performance indices such as phase noise, power consumption and lock time are measured in this environment. Transient, parametric sweep and phase noise analyses are carried out in this work to find out the performances of the circuit. The optimization of the current starved VCO circuit, the scale factor for transistor sizing is found out using the MATLAB environment.

4.2 Design Procedure

4.2.1 VCO Design

Since VCO is the heart of the whole PLL system, it should be designed in a proper manner. The design steps for the current starved VCO are as follows.

Step 1

Find the value of the propagation delay for each stage of the inverter in the VCO circuit using the following equation.

$$\tau_p = \frac{1}{Nf} \tag{13}$$

Where $\tau_p = \tau_{phl} = \tau_{plh}$ = half of the propagation delay time of the inverter

N= no of inverter stages

f= required center frequency of oscillation

Step 2

Find the $\left(W/L\right)$ ratio for the transistors in the different inverter stages using the equation in below.

$$\left(W/L\right)_n = \frac{C_{load}}{\tau_{phl}\mu_n C_{ox}(V_{dd}-V_{T,n})}\left(\frac{2V_{T,n}}{V_{dd}-V_{T,n}} + \ln\left(\frac{4(V_{dd}-V_{T,n})}{V_{dd}} - 1\right)\right) \quad (14)$$

$$\left(W/L\right)_p = \frac{C_{load}}{\tau_{plh}\mu_p C_{ox}(V_{dd}-|V_{T,p}|)}\left(\frac{2|V_{T,p}|}{V_{dd}-|V_{T,p}|} + \ln\left(\frac{4(V_{dd}-|V_{T,p}|)}{V_{dd}} - 1\right)\right) \quad (15)$$

Step 3

After finding the $\left(W/L\right)$ ratio, find the values for W and L.

Step 4

Find the value of the total capacitance form the expression

$$C_{tot} = \frac{5}{2}C_{ox}(L_pW_p + L_nW_n) \quad (16)$$

Where C_{ox} is the oxide capacitance

L_p, W_p, L_n, W_n is the width and length of the PMOS and NMOS transistors in the inverter stages.

Step 5

Calculate the value of drain current for the center frequency which is given by

$$I_{Dcenter} = NC_{tot}V_{dd}f \quad (17)$$

Step 6

Find the $\left(W/L\right)$ ratio for the current starving transistors in the circuit from the drain current expression which is represented as

$$\left(W/L\right)_n = \frac{2\times I_{Dcenter}}{\mu_n C_{ox}(V_{gs}-V_{T,n})^2} \quad (18)$$

Similarly $\left(W/L\right)_p = 2.5 \times \left(W/L\right)_n$ (19)

4.2.2 Design of Phase Locked Loop

The value of the charge pump current and the component parameters of the loop filter play a major role in the design of the phase locked loop circuit. The value of the lock time mainly depends upon these parameters. So while designing the circuit proper care should be taken in calculating these parameters. For the given values of reference(F_{ref}) and output frequency(F_{out}) as well as the lock in range, the following steps to be carried out in designing the filter circuit.

Step 1

Find the value of the divider circuit to be used which is given by

$$n = \frac{F_{out}}{F_{ref}} \tag{20}$$

Step 2

Find the value of the natural frequency (ω_n) from the lock in range as given below

$$lock\ in\ range = 2 \times \xi \times \omega_n \tag{21}$$

Step 3

Find the value of the charge pump gain (K_{PDI}) from the charge pump current used in the circuit which is given by

$$K_{PDI} = \frac{I_{pump}}{2\pi}\ \text{(Amps/radian)} \tag{22}$$

Step 4

Find the value of the gain of the VCO (K_{vco}) circuit from the characteristics curve using the following expression.

$$K_{vco} = \frac{f_{max} - f_{min}}{V_{max} - V_{min}}\quad \text{(Hz/V)} \tag{23}$$

Step 5

Find the values of the loop filter component parameters using the following expressions.

$$C_1 = \frac{K_{PDI} \times K_{vco}}{N\omega_n{}^2} \quad (24)$$

$$C_2 = \frac{C_1}{10} \quad (25)$$

$$R = \frac{2\xi}{\omega_n C_1} \quad (26)$$

4.3 Design Specifications and Parameters

4.3.1 VCO Design Specification

The current starved VCO design specifications are mentioned in the following table.

Table 1 VCO design specifications

Parameter	Value
Center frequency	1GHz
No. of inverter stage	5
Inverter delay	100ps
Load capacitance	65fF
Supply voltage	1.8V

4.3.2 VCO Design Parameters

Table 2 List of design parameters of the CSVCO circuit

Parameter	Value
Width of Current starved PMOS(W_{PCS})	2.33µm
Width of Current Starved NMOS(W_{nCS})	140nm
Width of PMOS in Inverter(W_P)	2.44µm
Width of NMOS in Inverter(W_n)	150nm
$L_{PCS} = L_{nCS} = L_P = L_n = L$	100nm

4.3.3 PLL Design Parameters

The whole PLL system design specifications and parameters are shown in the Table 3.

Table 3 PLL design specifications and parameters

Parameter	Value
Reference frequency((F_{ref})	500 MHz
output frequency(F_{out})	1 GHz
Lock in range	100 MHz
Supply voltage	1.8 V
Divider circuit	By 2
Charge pump current(I_{pump})	600 µA
Capacitor (C_1)	15 pF
Capacitor (C_2)	1.5 pF
Resistor (R)	1.384 KΩ

CHAPTER 5

SIMULATION RESULTS AND DISCUSSION

5.1 Phase Frequency Detector

The Pass Transistor DFF PFD circuit is shown in Figure 5.1. The PFD is same as to a dynamic two-phase master-slave pass-transistor flip-flop. The clock skew is minimized by using single edge clocks. In this design synchronous reset is used for master while asynchronous reset is used for slave. i.e., the reset is allowed only when the slave latch is transparent. The operating range of the design is increased with the help of synchronous resetting and also the power consumption is reduced compared to the traditional PFD. If the master latch is reset while it is transparent, then there will be significant short-circuit current will produce, resulting in more power. The output of the PFD when F_{ref} signal rising edge leads F_{in} signal rising edge and vice versa is shown in the Figure 5.2 and Figure 5.3 respectively.

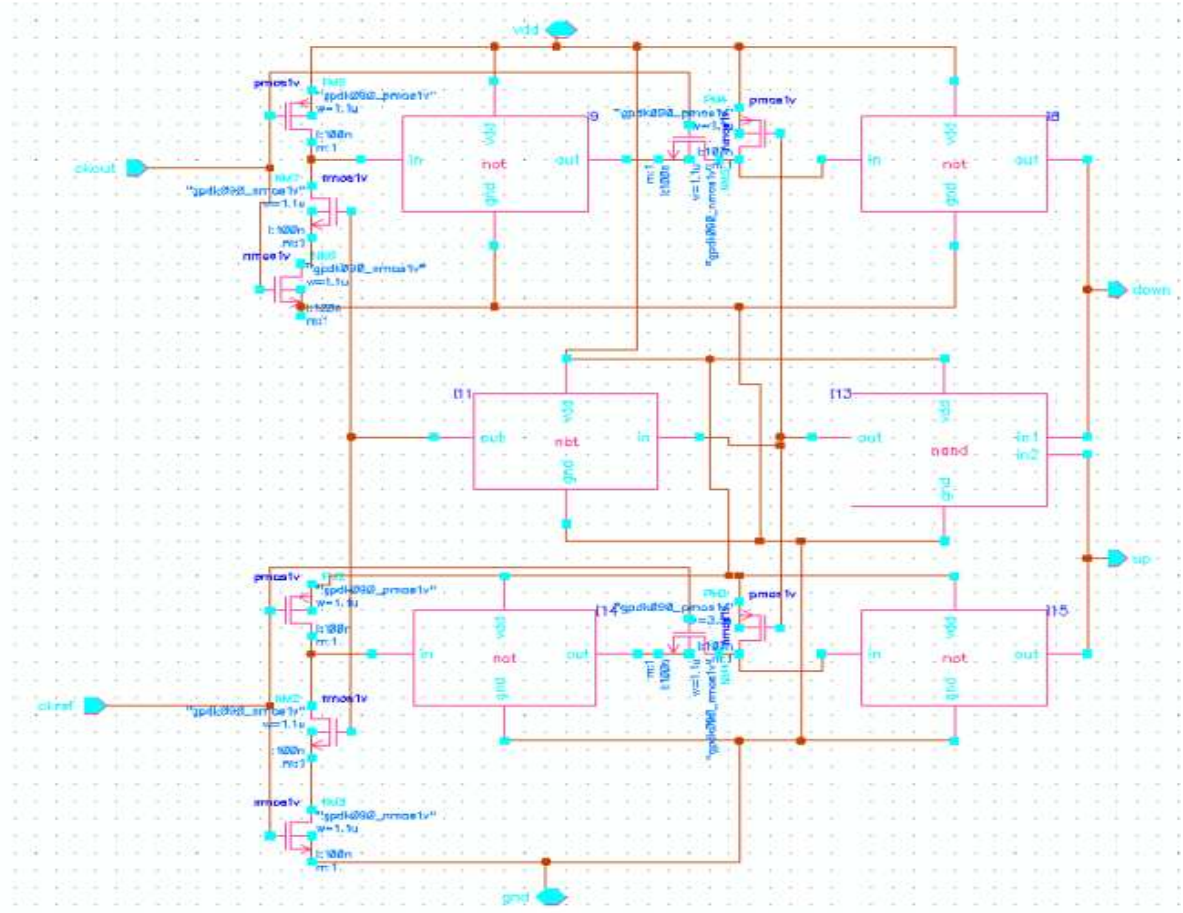

Figure5.1 Circuit diagram of a pass transistor based DFF PFD

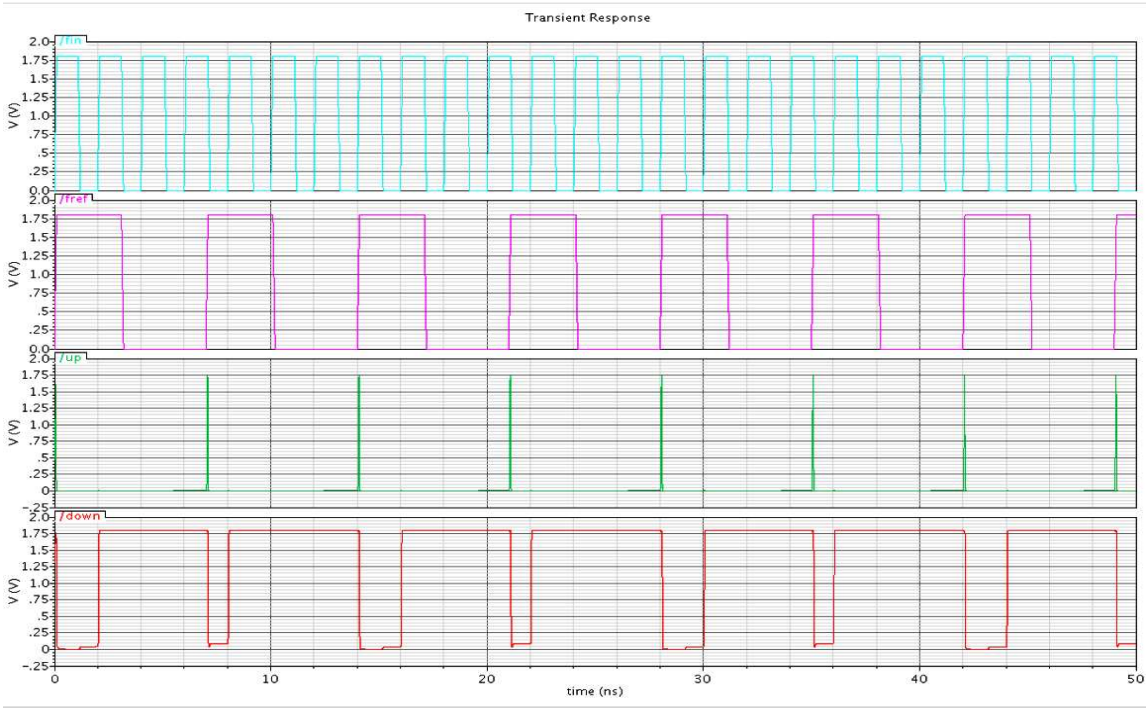

Figure5.2 Simulation result of PFD when F_{in} rising edge leads F_{ref} rising edge

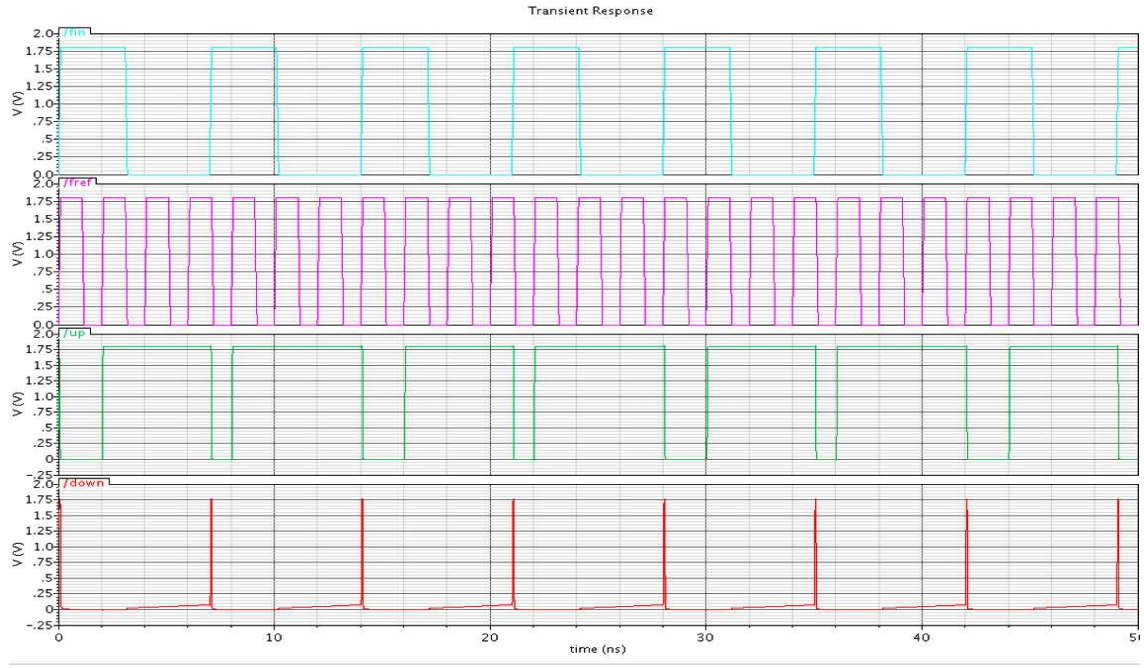

Figure5.3 Simulation result of PFD when F_{ref} rising edge leads F_{in} rising edge

5.2 Charge Pump and Loop Filter

When the reference signal clock edge leads the feedback clock edge, the UP signal of the PFD goes high. So to make both the clock have rising edge at the same time the VCO output signal frequency has to be increased. For this purpose an increase in control voltage is needed from the output of charge pump and loop filter circuit. The simulation result which is shown in the Figure 5.4 below gives an increase in the control voltage at the output of the loop filter circuit. From the Figure 5.4 it's clear that the control voltage increases for a period during which the UP signal of the PFD remains high. In the other case a decrease in the control voltage is produced at the output of the filter circuit which is shown in the Figure 5.5. When the rising of feedback signal leads the reference signal rising edge the control voltage decreases for the period during which the DOWN signal of the PFD remains high.

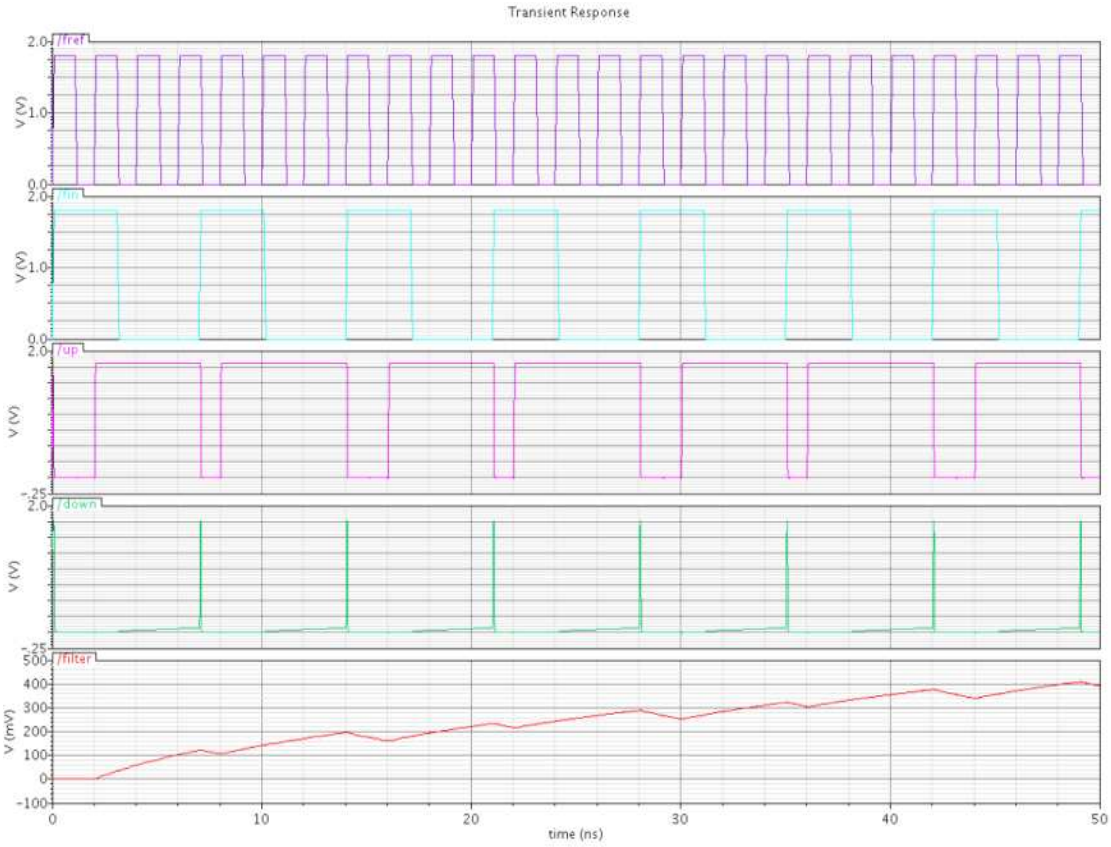

Figure5.4 Simulation result for loop filter with PFD when F_{ref} clock edge leads F_{in} clock edge

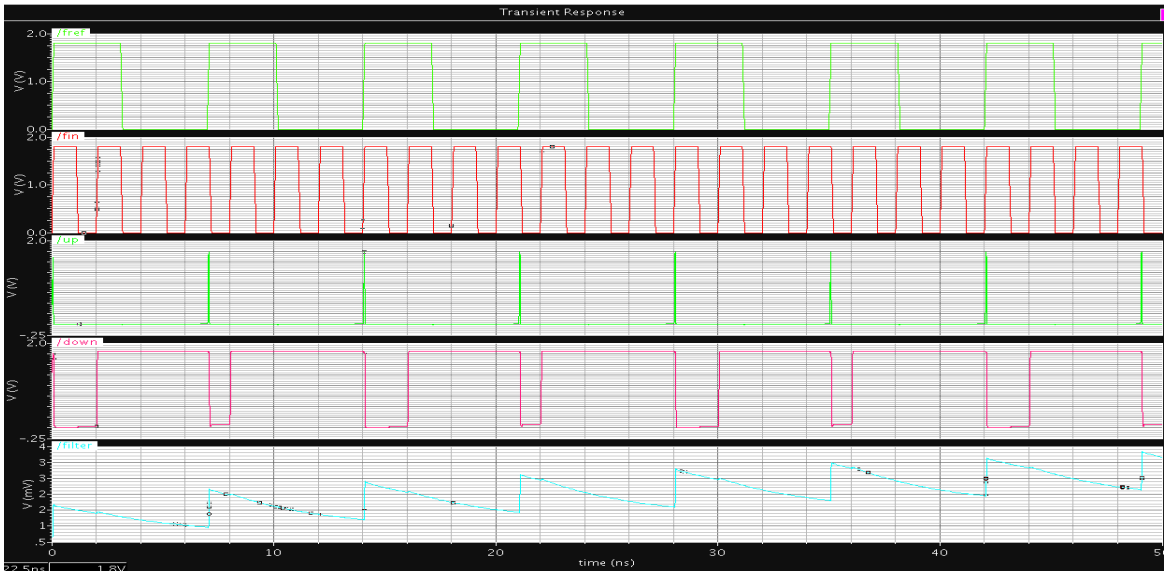

Figure5.5 Simulation result for loop filter with PFD when F_{in} clock edge leads F_{ref} clock edge

5.3 Voltage Controlled Oscillator

5.3.1 Result using traditional method

The heart of the PLL circuit is the voltage controlled oscillator. The circuit is designed to give a center frequency of oscillation of 1 GHz. The frequency of oscillation of the output signal for the different input control voltage is mentioned in the Table 4. The center frequency of oscillation at an input control voltage of $V_{DD}/2$ is 1.012 GHz. The output signal of the VCO at a control voltage of $V_{DD}/2$ is shown in the Figure 5.6.

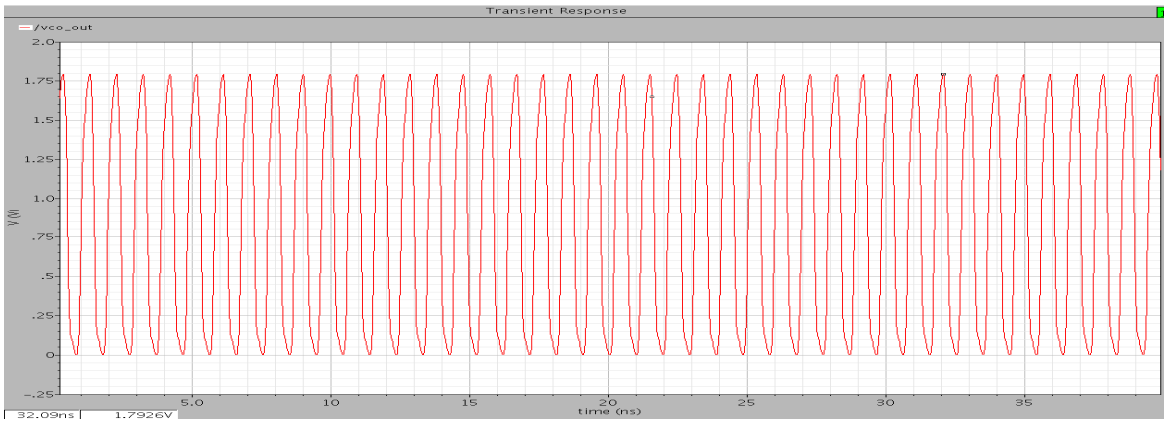

Figure5.6 Output signal of the VCO at a control voltage of $V_{DD}/2$

Table 4 Oscillating frequency of the VCO output signal for different control voltage

Control Voltage (V_C)(in volt)	Frequency of Oscillation (f) (in MHz)
0.103	24.415
0.154	50.929
0.206	91.05
0.257	139.32
0.309	188.179
0.36	234.277
0.411	282.125
0.463	342.256
0.514	412.889
0.566	489.48
0.617	569.178
0.669	650.037
0.720	731.72
0.771	812.946
0.823	893.63
0.874	973.461

Control Voltage	Frequency of Oscillation
0.926	1051.851
0.977	1128.02
1.03	1200.67
1.08	1271.818
1.13	1338.398
1.18	1401.32
1.23	1460.798
1.29	1517.121
1.34	1570.371
1.39	1620.798
1.44	1668.416
1.49	1713.913
1.54	1757.073
1.59	1798.081
1.65	1836.986
1.7	1873.865
1.75	1909.109
1.8	1943.021

The VCO characteristics curve is shown in the Figure 5.7. The X-axis of the curve represents the input control voltage while the Y-axis represents the corresponding frequency of oscillation. The gain of the CSVCO circuit is 1.531 GHz/V. The phase noise of the VCO in the schematic level is found to be -82.87 dBc/Hz. The phase noise plot for schematic level is shown in the Figure 5.8. The layout of the 5 stage current starved VCO is shown in the Figure 5.9. The schematic and post layout level simulation results are compared in the Table 5.

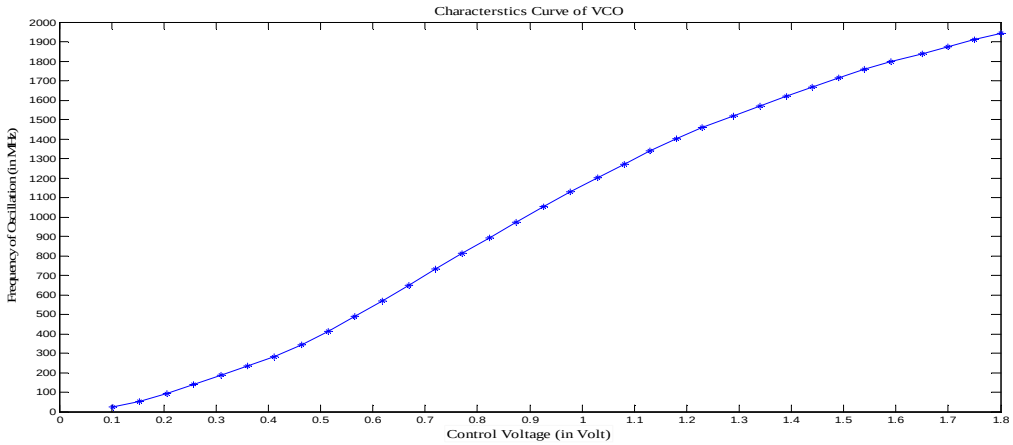

Figure5.7 VCO characteristics curve

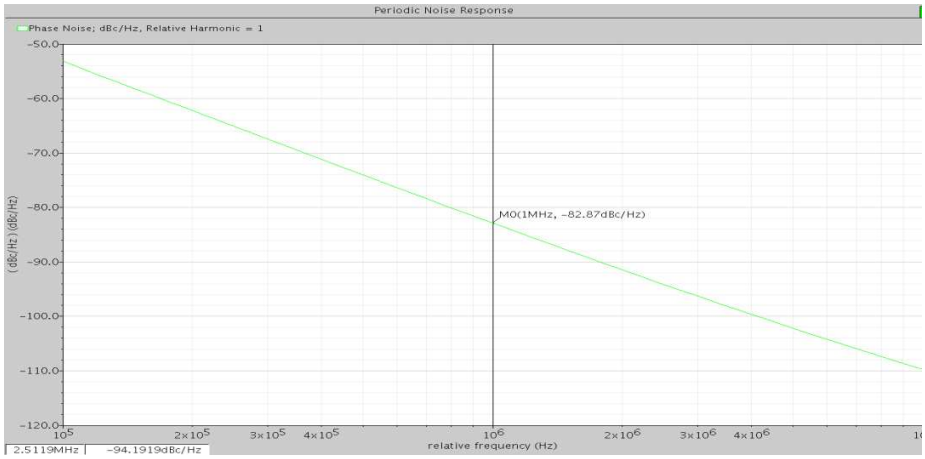

Figure5.8 Phase noise plot of VCO for schematic level

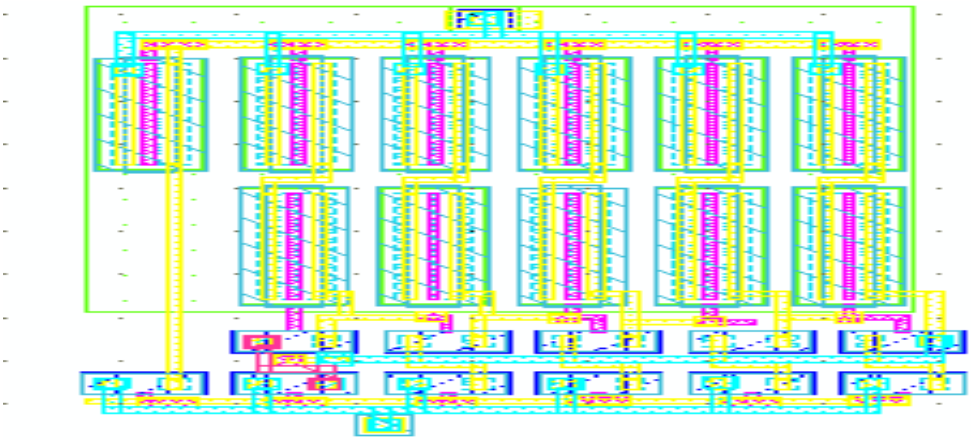

Figure5.9 Layout of the 5 stage current starved VCO

Table 5 Comparison of schematic and post layout level simulation results

Parameter	Schematic Result	Post-Layout Result
Frequency(f)	1.012 GHz	1.00256 GHz
Frequency Deviation(Δf)	12 MHz	2.56 MHz
Power(P)	432.456 µW	480.63 µW
Phase Noise @1MHz offset	-82.7 dBc/Hz	-84.88 dBc/Hz

5.3.2 Result using convex optimization method

Using convex optimization method the scaling ratio is found out to satisfy the center frequency of oscillation (i.e. delay of the circuit) from the MATLAB environment. The scaling ratio for different stages of the inverter in the VCO is 1,1,1,1 and 1.4058. The scaling ratio result is shown in the Figure 5.10.

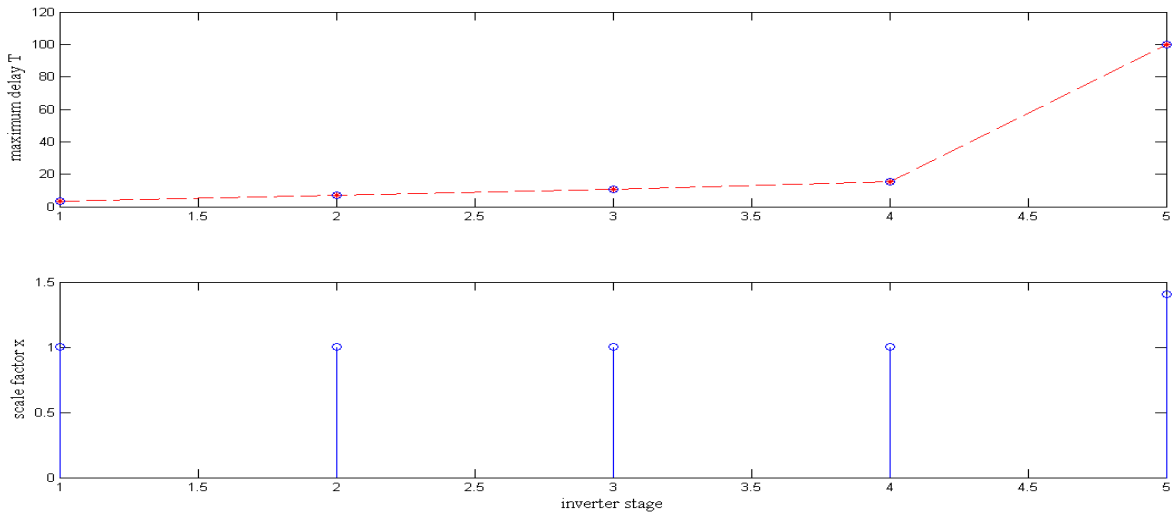

Figure5.10 Simulation results of scaling ratio and corresponding delay

Now the transistor sizes are modified according to the scaling ratio. Since the scaling factor of all the stages are 1 except 5th stage, so the transistor sizing of the 5th stage has only changed to get the better frequency precision. The sizes of the transistors of CSVCO optimized using

convex optimization technique are listed out in the Table 6. Before optimization the centre frequency of the oscillation is found out 1.012GHz. And after applying the convex optimization and geometric programming to this circuit, the centre frequency of oscillation is 1000.0457MHz. So the frequency deviation from its centre frequency is reduced to .00457% from 1.2%. The performance of CSVCO for both traditional and geometric programming is compared in the Table 7. The comparison of control voltage versus oscillating frequency characteristics of the CSVCO circuit is shown in the Figure 5.11.

Table 6 Size of the transistors of CSVCO circuit after optimization

Stage	Parameter	value
1	W_{PCS}	2.33µm
	W_{nCS}	140nm
	W_P	2.44µm
	W_n	150nm
2	W_{PCS}	2.33µm
	W_{nCS}	140nm
	W_P	2.44µm
	W_n	150nm
3	W_{PCS}	2.33µm
	W_{nCS}	140nm
	W_P	2.44µm
	W_n	150nm
4	W_{PCS}	2.33µm
	W_{nCS}	140nm
	W_P	2.44µm
	W_n	150nm
5	W_{PCS}	3.28µm
	W_{nCS}	195nm
	W_P	3.435µm
	W_n	215nm

Table 7 Performance comparison of CSVCO designed using traditional method and convex optimization

Factor	CSVCO using traditional method	CSVCO using convex optimization method
Frequency(f)	1.012GHz	1.0000457GHz
Frequency Deviation(Δf)	12MHz	45.7KHz
Power(P)	432.456µW	539.65µW
Phase Noise @1MHz offset	-82.7 dBc/Hz	-82.6 dBc/Hz
K_{VCO}	1.531GHz/V	1.5926GHz/V

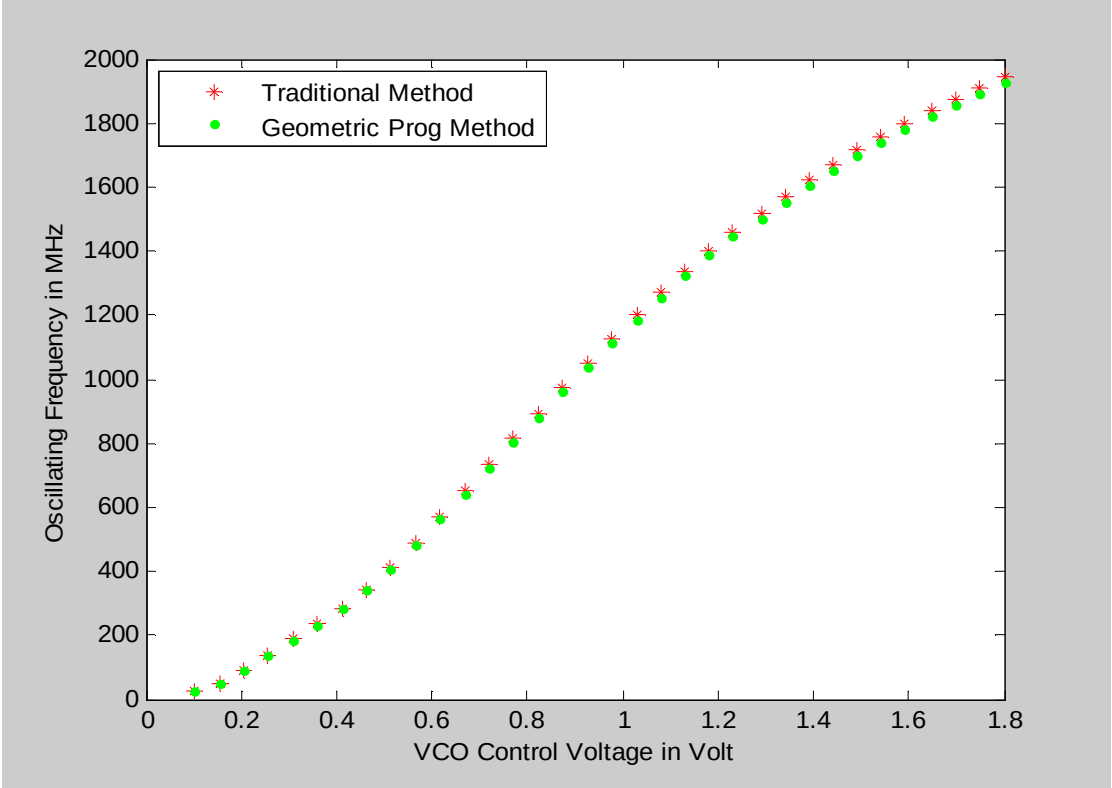

Figure5.11 Ccomparisons of control voltage versus oscillating frequency characteristics of the CSVCO circuit

5.4 Frequency Divider

The circuit diagram of a pass transistor based DFF frequency divider circuit is shown in the Figure 5.12. The circuit divides the frequency by a factor of 2. The simulation result of the divide by 2 circuits is shown in the Figure 5.13

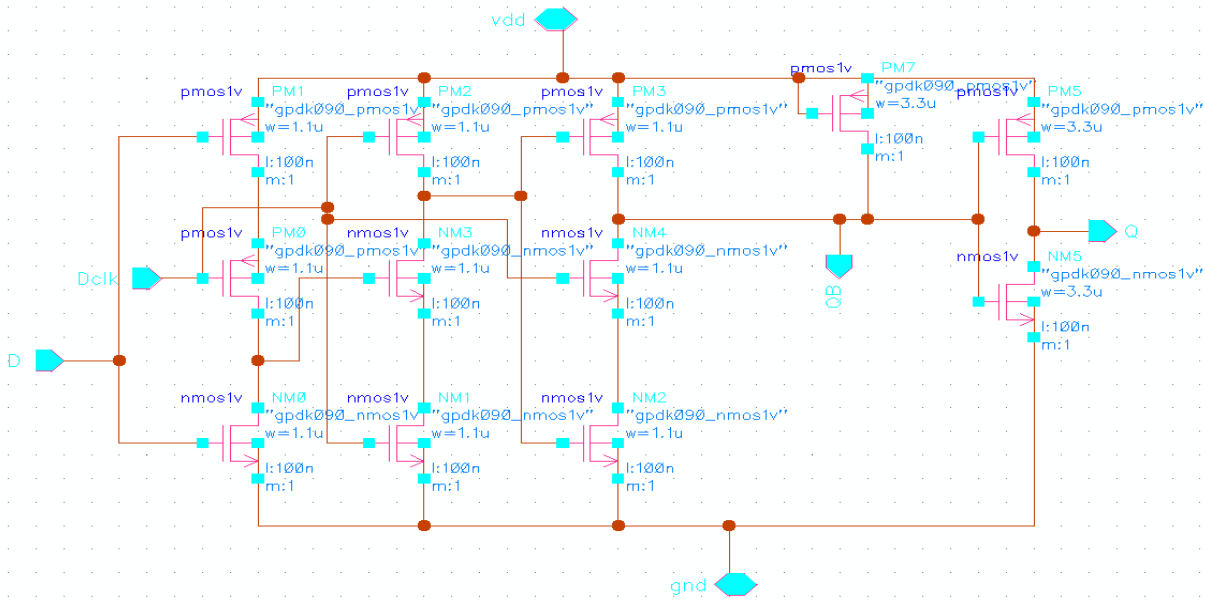

Figure5.12 Circuit diagram of a pass transistor based DFF frequency divider circuit

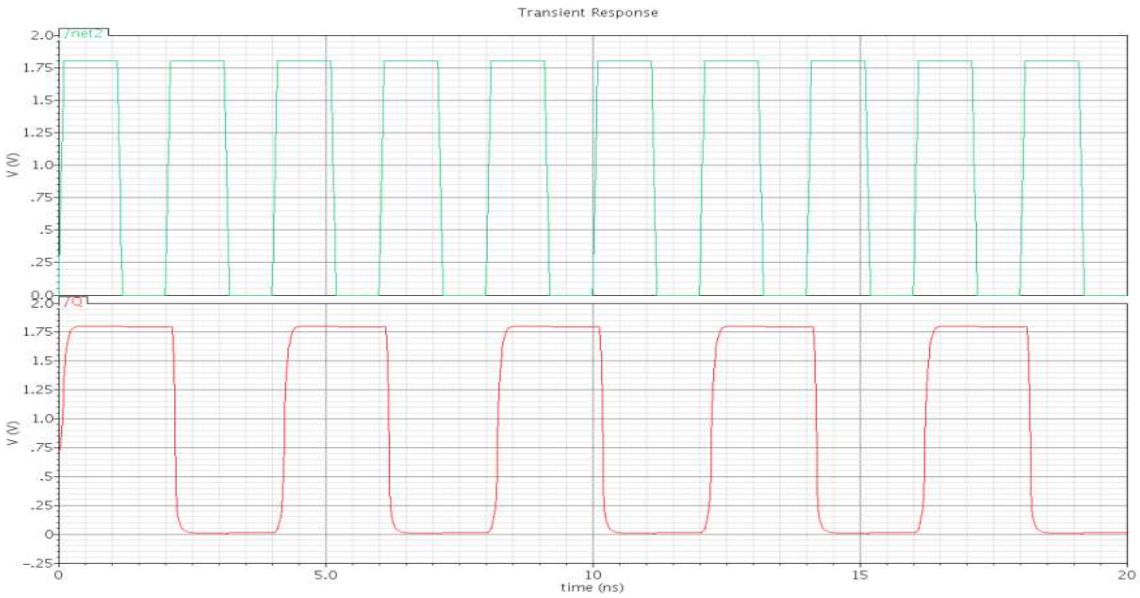

Figure5.13 Simulation result of the divide by 2 circuits

5.5 Phase Locked Loop

The output of the charge pump and loop filter circuit i.e. the control voltage will maintain a constant value when the references signal and feedback signal are in lock. The control voltage of PLL for the schematic level is shown in the Figure 5.14. From the Figure 5.14 it's clear that the control maintains the constant value of 0.9 V at time 280.6 ns. So the lock time of PLL is 280.6 ns.

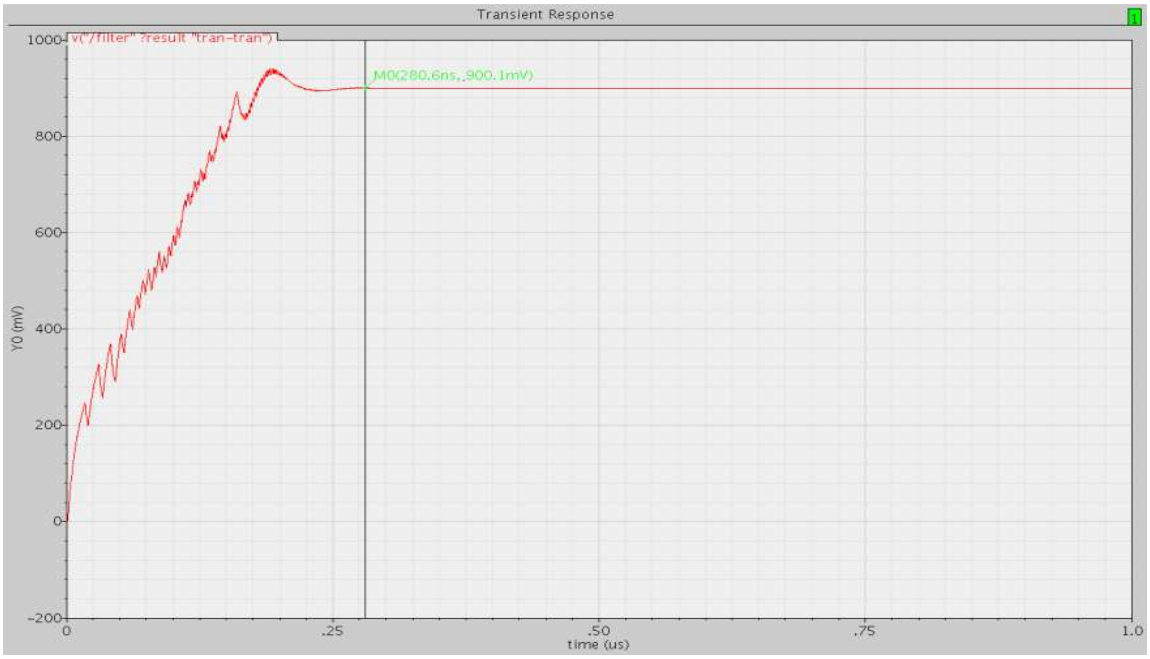

Figure5.14 Variation of the control voltage w.r.t. time

The layout of the PLL is shown in the Figure 5.15. The most of the area of the PLL is consumed by the resistor and capacitor used in the filter network. Different signals like UP, DOWN, Control Voltage, reference signal and feedback input signal of the PLL in the lock state are shown in the Figure 5.16 and Figure 5.17 for schematic level and post layout level respectively. From the Figure 5.16 and 5.17 it's clear that when the control voltage is constant, the reference signal and the feedback input signal are almost similar as their phase and frequency are approximately same.

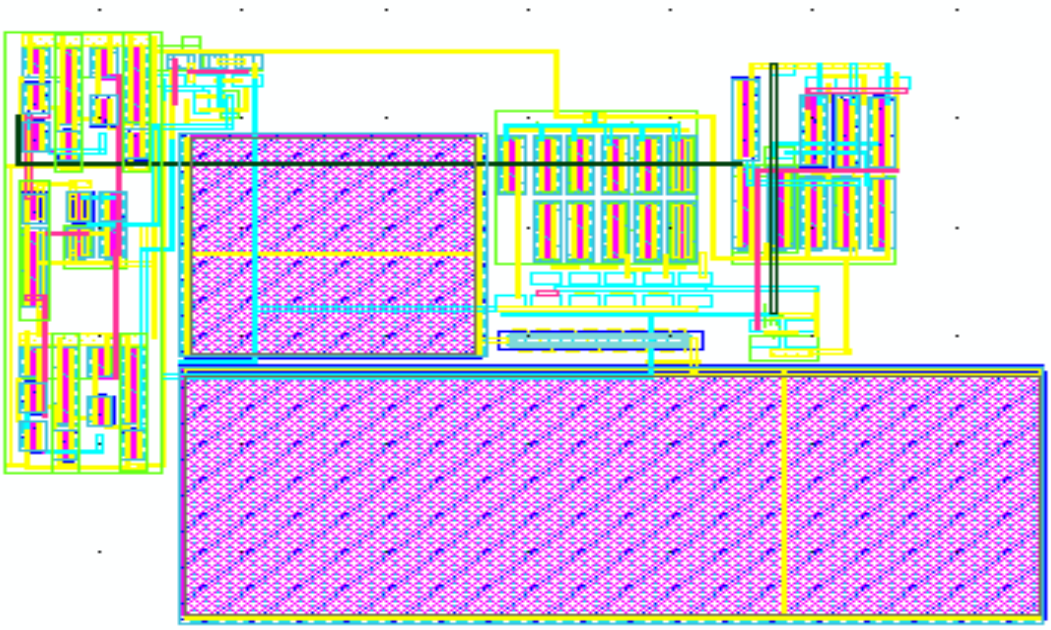

Figure5.15 Layout of the PLL circuit

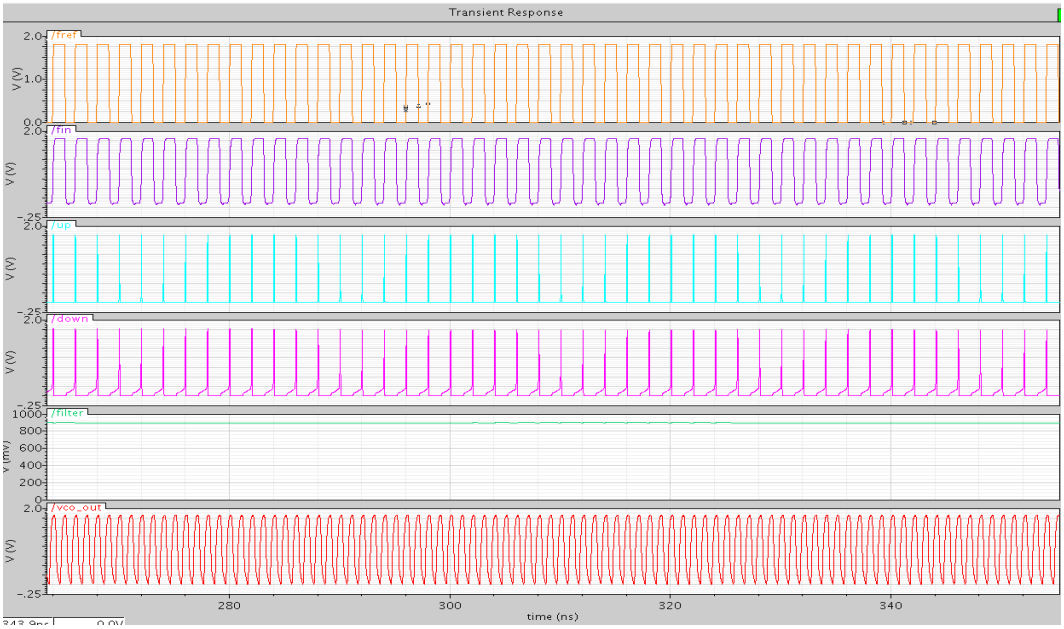

Figure5.16 Different signals of PLL in lock state for schematic level

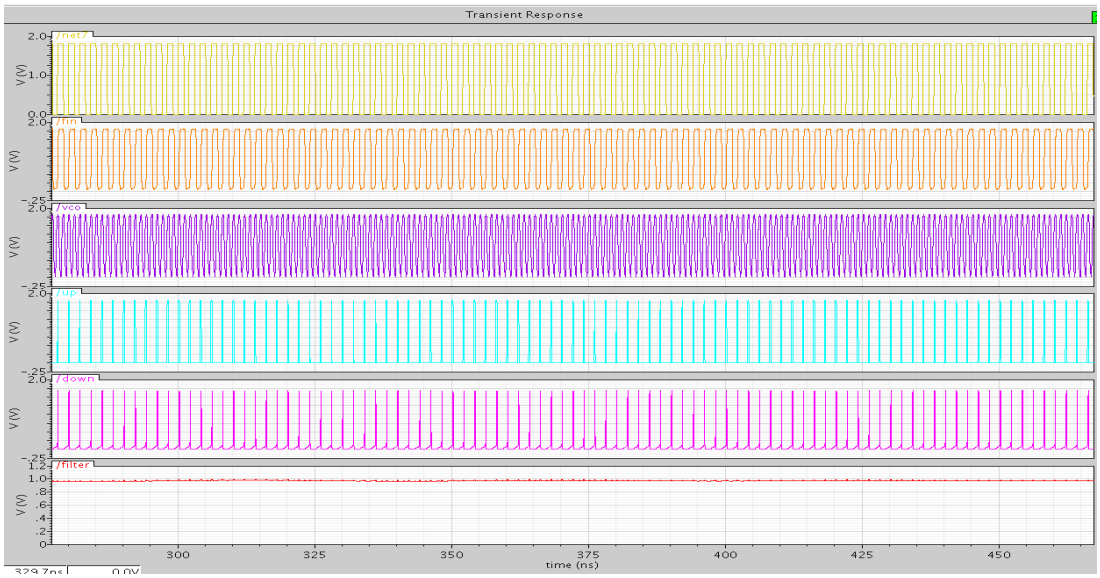

Figure5.17 Different signals of PLL in lock state for post layout level simulation

The phase noise analysis of the PLL is carried out both in the schematic as well as in the post layout level. The phase noise is found to be -86.21 dBc/Hz and -101.7 dBc/Hz in schematic and post layout level respectively. The phase noise variation of the PLL both in schematic and post layout level simulation are shown in the Figure 5.18 and 5.19 respectively.

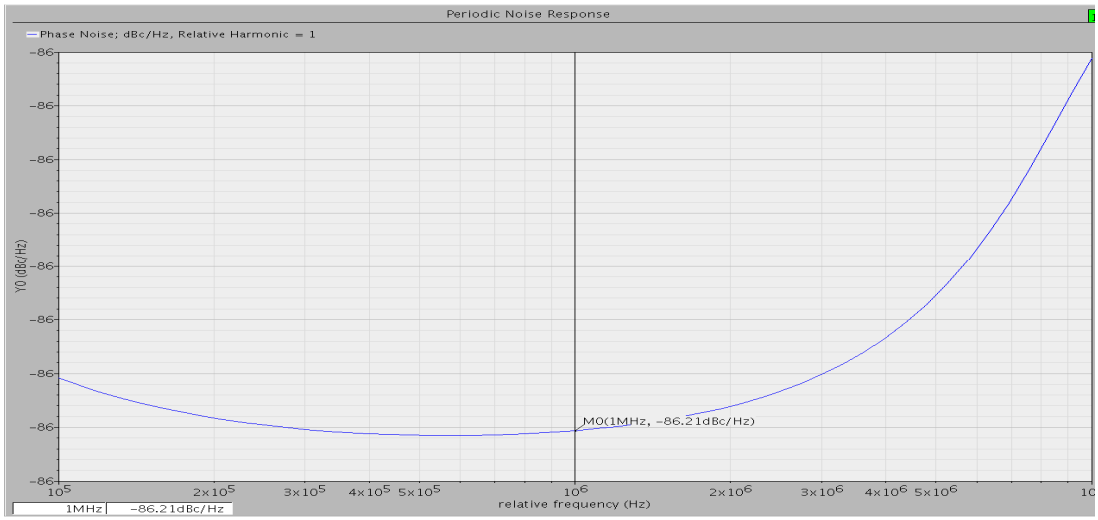

Figure5.18 Phase noise variation of PLL w.r.t. offset frequency for schematic level simulation

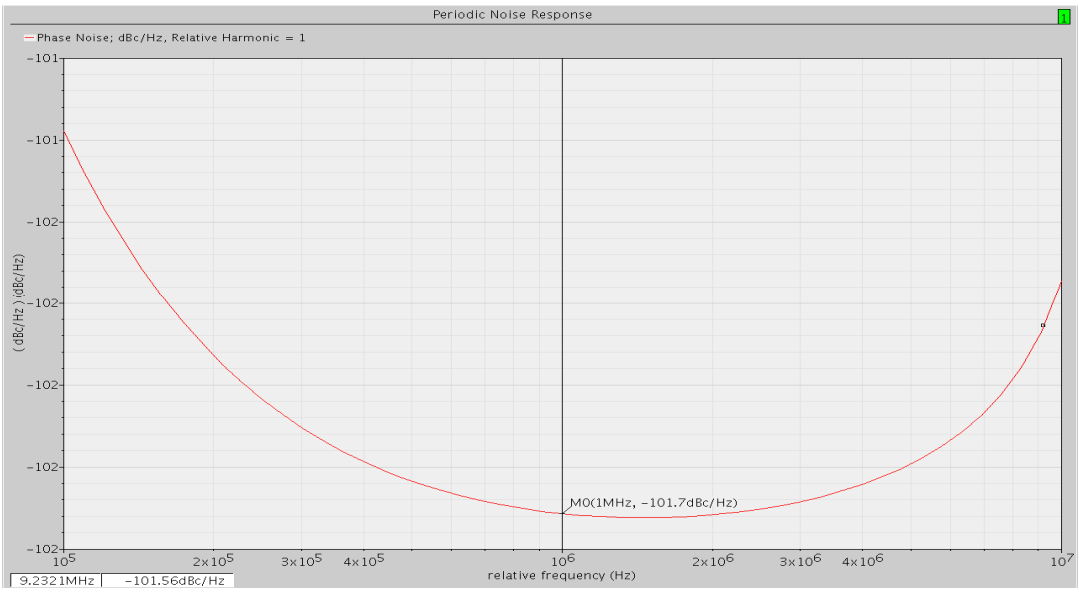

Figure5.19 Phase noise variation of PLL w.r.t. offset frequency for post layout level simulation

The performance comparison of the PLL both in schematic and post layout level simulation are mentioned in the Table 8.

Table 8 Performance comparison of PLL circuit

Parameter	Result of Schematic Level Simulation	Result of Post Layout Level Simulation
Technology	90 nm	90 nm
VDD	1.8 V	1.8 V
Lock Time	280.6 ns	345.5 ns
Frequency	1 GHz	1 GHz
Maximum Power Consumption	11.9 mW	10.408 mW
Phase Noise @ 1MHz offset	-86.21 dBc/Hz	-101.7 dBc/Hz

CHAPTER 6

CONCLUSION AND FUTURE WORK

Conclusion and Future Work

1. In this work a PLL with a better lock time is presented. The lock time of the PLL is found to be 280.6 ns.
2. The PLL circuit consumes a power of 11.9 mW from a 1.8 V D.C. supply
3. The lock time of the PLL mainly depends upon the type of PFD architecture used and the parameters of the charge pump and loop filter. So by properly choosing the PFD architecture and adjusting the charge pump current and the loop filter component values a better lock time can be achieved.
4. The centre frequency of oscillation of the VCO depends upon the sizing of the transistors. The frequency deviation from the desired value can be reduced by properly choosing the transistor sizes.
5. By applying the convex optimization technique with frequency of oscillation as the main objective function, the deviation of oscillation frequency is minimized to 0.00457% from 1.2%.
6. Here the convex technique is used to find out the transistor sizing to meet only the desired frequency specification. The other constraints like area, power and phase noise can also be applied.

References

[1] R.E. Best, "Phase Locked Loops Design, Simulation and Applications," *McGraw-Hill Publication*, 5th Edition, 2003.

[2] Dan H. Wolaver, "Phase Locked Loop Circuit Design," *Prentice Hall Publication*, 1991.

[3] R.J.Baker, H.W.Li, and D.E.Boyce, "CMOS Circuit Design, Layout, and Simulation," *IEEE Press Series on Microelectronic Systems*, 2002.

[4] S. M. Shahruz, "Novel phase-locked loops with enhanced locking capabilities," *Journal of Sound and Vibration*, Vol. 241, Issue 3, 29 March 2001, Pages 513-523.

[5] B. Razavi, "Design of Analog CMOS Integrated Circuits," *Tata McGraw Hill Edition*,2002

[6] M.Mansuri, D.Liu, and C.K.Yang, "Fast Frequency Acquisition Phase Frequency Detector for GSamples/s Phase Locked Loops," *IEEE Journal of Solid State Circuit*, Vol. 37, No. 10, Oct., 2002.

[7] Youngshin Woo, Young Min Jang and Man Young Sung, "Phase-locked loop with dual phase frequency detectors for high-frequency operation and fast acquisition," *Microelectronics Journal*, Vol. 33, Issue 3, March 2002, Pages 245-252.

[8] Quan Sun, Yonguang Zhang, Christine Hu-Guo, Kimmo Jaaskelainen and Yann Hu, "A fully integrated CMOS voltage regulator for supply-noise-insensitive charge pump PLL design," *Microelectronics Journal*, Vol. 41, Issue 4, April 2010, Pages 240-246

[9] S.J.Li, and H.H.Hsieh," A 10 GHz Phase-Locked Loop with a Compact Low-Pass Filter in 0.18 μm CMOS Technology", *IEEE Microwave and Wireless Components Letters*, VOL. 19, NO. 10, OCTOBER 2009

[10] H.Janardhan, and M.F.Wagdy "Design of a 1GHz Digital PLL Using 0.18 μm CMOS Technology," *IEEE Proc. of the Third International Conference on Information Technology*, 2006.

[11] S.M.Kang, and Y.Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design," *McGraw-Hill Publication*, 3rd Edition, 2003.

[12] A. Arakali, S. Gondi, and P. K.Hanumolu, "Analysis and Design Techniques for Supply-Noise Mitigation in Phase-Locked Loops", *IEEE Transactions on Circuits and Systems—I: Regular Papers*, Vol. 57, No. 11, Nov. 2010.

[13] T.H. Lee and A. Hajimiri, "Oscillator Phase Noise: a Tutorial," *IEEE Journal of Solid-State Circuits*, vol. 35, March 2000, pp. 326 – 336.

[14] B. Razavi "A Study of Phase Noise in CMOS Oscillators", *IEEE Journal of Solid-State Circuits*, Vol. 31, No. 3, March 1996.

[15] A.Mehrotra, "Noise Analysis of Phase-Locked Loops", *IEEE Tran. On Circuits and Systems-I: Fundamental Theory and Applications*, Vol. 49, No. 9, Sept. 2002.

[16] A.Hajimiri, S.Limotyrakis, and T.H.Lee, "Jitter and Phase Noise in Ring Oscillators", *IEEE Journal of Solid-State Circuits*, Vol. 34, No. 6, March 1999.

[17] Martin John Burbidge and J. Tijou, "Towards generic charge-pump phase-locked loop, jitter estimation techniques using indirect on chip methods," *Integration, the VLSI Journal*, Volume 40, Issue 2, February 2007, Pages 133-14.

[18] Alper Demir, "Computing Timing Jitter From Phase Noise Spectra for Oscillators and Phase-Locked Loops with White and 1/f Noise", *IEEE Tran. On Circuits and Systems-I: Regular Papers*, Vol. 53, No. 9, Sept. 2006.

[19] X.Gao, Eric A.M.Klumperink, Paul F.J.Geraedts, and B.Nauta, “Jitter Analysis and a Benchmarking Figure-of-Merit for Phase-Locked Loops”, *IEEE Transactions on Circuits and Systems-II: Express Briefs*, Vol. 56, No. 2, Feb. 2009.

[20] M. Curtin and P. O’Brien, “Phase locked Loops for High Frequency Receivers and Transmitters”, *Analog Dialogue*, VOL 33.3,1999.

[21] M.D.M.Hershenson,T.H.Lee and S.P.Boyd,“Optimal Design of CMOS Op-Amp via Geometric Programming,” *IEEE Journal of Solid State Circuit*, Vol. 37, No. 10, Oct., 2002.

[22] H. Hindi,”A Tutorial on Convex Optimization”, *Palo Alto Research Center*, Palo Alto, California

[23] S.P.Boyd,S.J.Kim,D.D.Patil, and M.A.Horowitz, “ Digital Circuit Optimization via Geometric Programming”, *Operations Research*, VOL. 53, NO.6,pp.892-932,Nov.2005.

[24] D.Ghai,S.P.Mohanty, and E. Kougianos, “ Design of Parasitic and Process Variation Aware Nano-CMOS RF Circuits: A VCO Case Study”, *IEEE Tran. On Very Large Scale Integration (VLSI) Systems*, Vol. 17, No. 9, Sep., 2009.

[25] P. C. Maulik, L. R. Carley, and D. J. Allstot, “Sizing of cell-level analog circuits using constrained optimization techniques,” *IEEE Journal of Solid-State Circuits*, vol. 28, pp. 233–241, Mar. 1993.

List of Publications

Conference:

1. **B.P.Panda**, P.K.Rout, D.P.Acharya, and G.Panda "**Analysis and Design of 1GHz PLL for Fast Phase and Frequency Acquisition**"*Proc. of International Conference on Electronic System, India*", pp 212-215, Jan 2011.
2. **B.P.Panda**, P.K.Rout, D.P.Acharya, and G.Panda "**Design of a Novel Current Starved VCO via Constrained Geometric Programming** "*Proc. of International Symposium on Devices MEMS Intelligent Systems and Communication*", pp 224-228, Sikkim, India, April, 2011.

Journal:

1. **B.P.Panda**, P.K.Rout, D.P.Acharya, and G.Panda "**Analysis and Design of 1GHz PLL for Fast Phase and Frequency Acquisition"** *International Journal of Signals and Imaging Systems Engineering*, May, 2011(In Press).
2. **B.P.Panda**, P.K.Rout, D.P.Acharya, and G.Panda **"Design of a Novel Current Starved VCO via Constrained Geometric Programming**" *International Journal of Computer Application*", April, 2011. (In Press)