FPGA IMPLEMENTATION OF DIGITAL CONTROLLER FOR SHUNT ACTIVE POWER FILTER TO REDUCE HARMONICS AND REACTIVE POWER

A THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE

REQUIREMENTS FOR THE DEGREE OF

Master of Technology

In

VLSI Design and Embedded System

By

Saswat Kumar Ram

Department of Electronics and Communication Engineering

National Institute of Technology

Rourkela

2011

FPGA IMPLEMENTATION OF DIGITAL CONTROLLER FOR SHUNT ACTIVE POWER FILTER TO REDUCE HARMONICS AND REACTIVE POWER

A THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE

REQUIREMENTS FOR THE DEGREE OF

Master of Technology

In

VLSI Design and Embedded System

By

Saswat Kumar Ram

Under the Guidance of

Prof. K.K.Mahapatra

Department of Electronics and Communication Engineering

National Institute of Technology

Rourkela

2011

CERTIFICATE

This is to certify that the thesis entitled, "**FPGA Implementation of digital controller for shunt active power filter to reduce harmonics and reactive power**" submitted by Sri **Saswat Kumar Ram** in partial fulfillment of the requirements for the award of **MASTER OF TECHNOLOGY** Degree in **Electronics and communication Engineering** with specialization in "**VLSI Design and Embedded System**" at the National Institute of Technology, Rourkela (Deemed University) is an authentic work carried out by him under my supervision and guidance.

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other Institute for the award of any degree.

Date:

Prof. K.K.Mahapatra
Department Of Electronics and Communication Engineering
National Institute of Technology
Rourkela - 769008

Dedicated To My Mother

ACKNOWLEDGEMENT

I would like to articulate my profound gratitude and indebtedness to my thesis guide **Prof. K.K.Mahapatra** who has always been a constant motivation and guiding factor throughout the thesis time in and out as well. It has been a great pleasure for me to get an opportunity to work under him and complete the project successfully.

I wish to extend my sincere thanks to **Prof. S.K.Patra**, Head of our Department, for approving our project work with great interest.

I feel a deep sense of gratitude for my father Sri. Chandradeo Ram and mother Smt. Gita Ram who formed a part of my vision and taught me the good things that really matter in life. I would like to thank my brother and my sister for their support.

An undertaking of this nature could never have been attempted with our reference to and inspiration from the works of other engineers whose details are mentioned in references section. I acknowledge my indebtedness to all of them. Last but not the least, my sincere thanks to all of my friends who have patiently extended all sorts of help and motivate for accomplishing this undertaking.

Saswat Kumar Ram

CONTENTS

LIST OF FIGURES

LIST OF TABLES

ABSTRACT

Most of the pollution issues created in power systems are due to the non-linear characteristics and fast switching of power electronic equipment. Power quality issues are becoming stronger because sensitive equipment will be more sensitive for market competition reasons, equipment will continue polluting the system more and more due to cost increase caused by the built-in compensation and sometimes for the lack of enforced regulations. Efficiency and cost are considered today almost at the same level. Active power filters have been developed over the years to solve these problems to improve power quality. Among which shunt active power filter is used to eliminate and load current harmonics and reactive power compensation. The active power filter (APF) is implemented with PWM based current controlled voltage source inverter (VSI). This VSI switching signals are generated through proposed three-level hysteresis current controller (HCC) that achieves significant reduction in the magnitude and variation of the switching frequency; it is indicating improved performance compared to 2-level HCC. The shunt APLC system is modeled and investigated under different unbalanced non-linear load conditions using MATLAB programs. The simulation results reveal that the active power filter is effectively compensating the current harmonics and reactive power at point of common coupling. The active power line conditioner system is in compliance with IEEE 519 and IEC 61000-3 recommended harmonic standards. Due to non-linear characteristics the load current gets distorted which causes undesirable effects like heating, equipment damages, EMI effects etc. in power network. The active power filter (APF) is the best solution for eliminating the harmonics caused by the non-linear loads. This work presents the three-phase four-wire active filter for power line conditioning (PLC) to improve power quality in the distribution network and implementation of a digitally controlled APF. Designed in Hardware Description Language (VHDL or VERILOG), the controller becomes independent of process technology. Synchronous reference frame is used for generation of reference current. PI currents algorithm and hysteresis current controller (HCC) together is written in VHDL code and is implemented using FPGA platform. Various simulation results are presented under steady state and transient state condition and performance is analyzed. Simulation results obtained shows that the performance of three phase system with APF is found to be better and digital controller add a new aspect for the controller from low cost, high speed and hardware implementation point.PWM and hysteresis based current control is used to obtain the switching signals to the voltage source inverter(VSI).

Chapter 1

INTRODUCTION

Background

Objective

Thesis Outline

INTRODUCTION

The large usages of power electronic devices cause disturbances on the electrical supply network. The disturbances are due to the use of non-linear devices .These will introduce harmonics in the power system thereby causing equipment overheating ,damage devices ,EMI related problems etc. Several methods are described in various papers to solve these problems [1-2].

The concept of using APF to mitigate harmonics and to compensate reactive power was proposed more than two decades ago[3-6].Continuing proliferation of nonlinear loads such as power converters, SMPS, photo copiers, printer, UPS, ASDs are creating disturbances like harmonic pollution and reactive power problems in the power distribution lines [3-5]. Conventionally these problems are solved by passive L-C filters. But these L-C filters introduce tuning, aging, resonance problems and these filters are large in size and are suited for fixed harmonic compensation. So active power-line conditioners have become popular than passive filters; it compensates the harmonics and reactive power simultaneously. The active power filter topology can be connected in series or shunt and combinations of both (unified power quality conditioners). Passive filters combined with active shunt and series are some typical (hybrid) configurations that can be used for the same purpose. Shunt active filter is more popular than series filter, because most of the industrial applications require current harmonics compensation [6-11]. The shunt active power converter can be executed with current source inverter (CSI) or voltage source inverter (VSI). The voltage source inverter has three coupling inductors in series in the ac-side and an energy storage capacitor on the dc-side. Similarly, the current source inverter has three coupling capacitors in parallel in the ac-side and an energy storage inductor in series with the dc-side[13-14]. In general the voltage source inverter type is preferred for the shunt active power circuit due to the lower losses in the dc-side and it is possible to create multilevel inverter topologies for higher power level applications. The current control techniques of the voltage source inverters can be broadly classified into linear and non-linear controller. The SRF (synchronous reference frame) theory is used for generation of reference currents from distorted load currents [15]. The control scheme is based on sensing line currents only; an approach different from convention ones, which are based on sensing harmonics and reactive volt-ampere requirements of the nonlinear load. The three-phase currents/voltages are detected

using only two current/voltage sensors. The DC capacitor voltage is regulated to estimate the reference current template. The role of the DC capacitor is described to estimate the reference current [16-20]. The hysteresis and adaptive hysteresis method is used for gating pulse generation [21-28]. The digital controller plays a great role for this application due to numbers of advantages such as FPGA's provide reconfigurable hardware designs, Low cost development (reprogram ability), FPGA's can process information faster than a general purpose DSP, Bit widths for data registers are selected based on application needs. Designed in Hardware Description Language (VHDL or VERILOG) the controller becomes independent of process technology [29-32].

This work presents the MATLAB code simulation of three phase four wire system APF, comparative study of HCC and AHCC and implementation of a fully digital controller for shunt active power filter (APF).The controller uses a PI-regulator and a Hysteresis current controller. VHDL codes are written for each module in XILINX and verified by writing test bench. The codes are imported to FPGA (SPARTRAN-3E) by using chip-scope pro analyzer and then to C.R.O. The result obtained from the MATLAB/SIMULINK environment will be validated with experimental result using field programmable gate array (FPGA).

1.1 Background

1.1.1 Power quality

The PQ issue is defined as "any occurrence manifested in voltage, current, or frequency deviations that results in equipment overheating, damage devices, EMI related problems etc." Almost all PQ issues are closely related with Power Electronics in almost every aspect of commercial, domestic, and industrial application. Equipment using power electronic devise are residential appliances like TVs, PCs etc. business and office equipment like copiers, printers etc. industrial equipment like programmable logic controllers (PLCs), adjustable speed drives (ASDs), rectifiers, inverters, CNC tools and so on. The Power Quality (PQ) problem can be detected from one of the following several symptoms depending on the type of issue involved[1].

• Lamp flicker

• Frequent blackouts

• Sensitive-equipment frequent dropouts

• Voltage to ground in unexpected

• Locations

• Communications interference

• Overheated elements and equipment.

Harmonics are produced by rectifiers, ASDs, soft starters, electronic ballast for discharge lamps, switched-mode power supplies, and HVAC using ASDs. Equipment affected by harmonics includes transformers, motors, cables, interrupters, and capacitors (resonance). Notches are produced mainly by converters, and they principally affect the electronic control devices. Neutral currents are produced by equipment using switched-mode power supplies, such as PCs, printers, photocopiers, and any triplet's generator. Neutral currents seriously affect the neutral conductor temperature and transformer capability. Inter harmonics are produced by static frequency converters, cyclo-converters, induction motors & arcing devices. Equipment presents different levels of sensitivity to PQ issues, depending on the type of both the equipment and the disturbance. Furthermore, the effect on the PQ of electric power systems, due to the presence of PE, depends on the type of PE utilized. The maximum acceptable values of harmonic contamination are specified in IEEE standard in terms of total harmonic distortion[2-3]. Power electronics are alive and well in useful applications to overcome distribution system problems. Power electronics has three faces in power distribution: one that introduces valuable industrial and domestic equipment; a second one that creates problems; and, finally, a third one that helps to solve those problems. On one hand, power electronics and microelectronics have become two technologies that have considerably improved the quality of modern life, allowing the introduction of sophisticated energy-efficient controllable equipment to industry and home. On another hand, those same sensitive technologies are conflicting with each other and increasingly challenging the maintenance of quality of service in electric energy delivery, while at the same time costing billions of dollars in lost customer productivity.

1.1.2 Solutions to power quality problems

There are two approaches to the mitigation of power quality problems. The first approach is called load conditioning, which ensures that the equipment is made less sensitive to power disturbances, allowing the operation even under significant voltage distortion. The other solution is to install line-conditioning systems that suppress or counteract the power system disturbances. Passive filters have been most commonly used to limit the flow of harmonic currents in distribution systems. They are usually custom designed for the application. However, their performance is limited to a few harmonics, and they can introduce resonance in the power system. Among the different new technical options available to improve power quality, active power filters have been proven to be an important and flexible alternative to compensate for current and voltage disturbances in power distribution systems (i.e. at PCC). The idea of active filters is relatively old, but their practical development was made possible with the new improvements in power electronics and microcomputer control strategies as well as with cost reduction in electronic components. Active power filters are becoming a viable alternative to passive filters and are gaining market share speedily as their cost becomes competitive with the passive variety. Through power electronics, the active filter introduces current or voltage components, which cancel the harmonic components of the nonlinear loads or supply lines, respectively. Different active power filters topologies have been introduced and many of them are already available in the market [4].

1.1.3 Power filter topologies

Depending on the particular application or electrical problem to be solved, active power filters can be implemented as shunt type, series type, or a combination of shunt and series active filters (shunt-series type like UPQC). These filters can also be combined with passive filters to create hybrid power filters. The shunt-connected active power filter, with a self-controlled dc bus, has a topology similar to that of a static compensator (STATCOM) used for reactive power compensation in power transmission systems. Shunt active power filters compensate load current harmonics by injecting equal-but opposite harmonic compensating current. In this case the shunt active power filter operates as a current source injecting the harmonic components generated by the load but phase-shifted by 180°.

Series active power filters were introduced by the end of the 1980s and operate mainly as a voltage regulator and as a harmonic isolator between the nonlinear load and the utility system. The series-connected filter protects the consumer from an inadequate supply- voltage quality. This type of approach is especially recommended for compensation of voltage unbalances and voltage sags from the ac supply and for low-power applications and represents an economically attractive alternative to UPS, since no energy storage (battery) is necessary and the overall rating of the components is smaller. The series active filter injects a voltage component in series with the supply voltage and therefore can be regarded as a controlled voltage source, compensating voltage sags and swells on the load side. In many cases, series active filters work as hybrid topologies with passive LC filters [5]. If passive LC filters are connected in parallel to the load, the series active power filter operates as a harmonic isolator, forcing the load current harmonics to circulate mainly through the passive filter rather than the power distribution system. The main advantage of this scheme is that the rated power of the series active filter is a small fraction of the load kVA rating, typically 5%. However, the apparent power rating of the series active power filter may increase in case of voltage compensation.

The series-shunt active filter is a combination of the series active filter and the shunt active filter. The shunt active filter is located at the load side and can be used to compensate for the load harmonics. On the other hand, the series portion is at the source side and can act as a harmonic blocking filter. This topology has been called the Unified Power Quality conditioner (UPQC). The series portion compensates for supply voltage harmonics and voltage unbalances, acts as a harmonic blocking filter, and damps power system oscillations. The shunt portion compensates load current harmonics, reactive power, and load current unbalances. In addition, it regulates the dc link capacitor voltage. The power supplied or absorbed by the shunt portion is the power required by the series compensator and the power required to cover losses [6].

Hybrid power filters are a combination of active and passive filters. With this topology the passive filters have dynamic low impedance for current harmonics at the load side, increasing their bandwidth operation and improving their performance. This behavior is reached with only a small power rating PWM inverter, which acts as an active filter in series with the passive filter. Multilevel inverters are being investigated and recently used for active filter topologies. Three-level inverters are becoming very popular today for most inverter applications, such as machine

drives and power factor compensators. The advantage of multilevel inverters is that they can reduce the harmonic content generated by the active filter because they can produce more levels of voltage than conventional inverters (more than two levels)[7-8]. This feature helps to reduce the harmonics generated by the filter itself. Another advantage is that they can reduce the voltage or current ratings of the semiconductors and the switching frequency requirements. The more levels the multilevel inverter has, the better the quality of voltage generated because more steps of voltage can be created.

1.1.4 Voltage source inverters

Most of the active power filter topologies use voltage source Inverters, which have a voltage source at the dc bus, usually a capacitor, as an energy storage device. This topology, shown in Figure 1.1, converts a dc voltage into an ac voltage by appropriately gating the power semiconductor switches (IGBT). Although a single pulse for each half cycle can be applied to synthesize an ac voltage, for most applications requiring dynamic performance, pulse width modulation (PWM) is the most commonly used today. PWM techniques applied to a voltage source inverter consist of chopping the dc bus voltage to produce an ac voltage of an arbitrary waveform. There are a large number of PWM techniques available to synthesize sinusoidal patterns or any arbitrary pattern. With PWM techniques, the ac output of the filter can be controlled as a current or voltage source device.

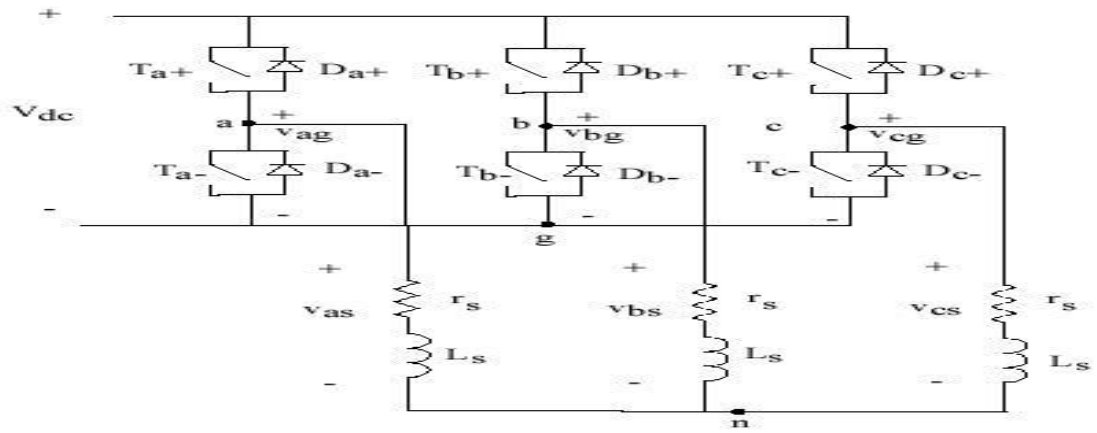


Figure 1.1 Voltage source inverter topology for active filters.

Voltage source inverters are preferred over current source inverter because it is higher in efficiency and lower initial cost than the current source inverters. They can be readily expanded in parallel to increase their combined rating and their switching rate can be increased if they are carefully controlled so that their individual switching times do not coincide. Therefore, higher-order harmonics can be eliminated by using inverters without increasing individual inverter switching rates [9-10].

1.1.5 Control strategies

Most of the active filters developed are based on sensing harmonics and reactive volt-ampere requirements of the non-linear load [11-12].and require complex control. In some active filters, both phase voltages and load currents are transformed into the α-β orthogonal quantities, from which the instantaneous real and reactive power is estimated. The compensating currents are calculated from load currents and instantaneous powers. The harmonic components of power are calculated using high pass filters in the calculation circuit. The control circuit of the dc capacitor voltage regulates the average value of the voltage to the reference value [4]. Reactive power compensation is achieved without sensing and computing the reactive current component of the load, thus simplifying the control circuit. Current control is achieved with constant switching frequency producing a better switching pattern. An active filter based on the instantaneous active and reactive current component in which current harmonics of positive and negative sequence including the fundamental current of negative sequence can be compensated. The system therefore acts as a harmonic and unbalanced current compensator. A comparison between the instantaneous active and reactive current component - method and the instantaneous active and reactive power method is realized [13].

Control scheme based on sensing line currents is described in [14]. The 3-phase currents/voltages are detected using only two current/voltage sensors compared to three used in [15]. DC capacitor voltage is regulated to estimate the reference current template. Selection of dc capacitor value has been described in [16]. Conventional solutions for controller requirements were based on classical control theory or modern control theory. Widely used classical control theory based design of PID family controllers requires precise linear mathematical models. The PID family of controllers failed to perform satisfactorily under parameter variation, non linearity, load disturbance, etc.

During the past several years, Digital Controllers has emerged as one of the most active and fruitful areas for research in the applications of FPGA, especially in the realm of industrial processes, which do not lend themselves to control by conventional methods because of a lack of quantitative data regarding the input-output relations. The Digital Controller is based on FSMD Architecture (Finite State Machine with DATAPATH) that is much closer in spirit to human thinking and natural language than traditional logical systems. The FSMD Architecture is based on Finite State Machine (FSM) that is used to control the DATAPATH. Recently, Digital controllers have generated a good deal of interest in certain applications. The advantages of Digital controllers over the conventional controllers are:

- ✓ FPGA's provide reconfigurable hardware designs.
- ✓ Low cost development (reprogrammable ability).
- ✓ FPGA's can process information faster than a general purpose DSP.
- ✓ Bit widths for data registers can be selected based on application needs.
- ✓ Designed in Hardware Description Language (VHDL or VERILOG) the controller becomes independent of process technology.

1.2 Objective

In modern electrical distribution systems there has been a sudden increase of single phase and three-phase non-linear loads. These non-linear loads employ solid state power conversion and draw non-sinusoidal currents from AC mains and cause harmonics and reactive power burden, and excessive neutral currents that result in pollution of power systems. They also result in lower efficiency and interference to nearby communication networks and other equipments. Active power filters have been developed to overcome these problems. Shunt active filters based on current controlled PWM converters or with hysteresis current controller are seen as viable solution. The techniques that are used to generate desired compensating current are based on instantaneous extraction of compensating commands from the distorted currents or voltage signals in time domain. Time domain compensation has fast response, easy implementation and less computation burden compared to frequency domain. In this work both conventional and digitally controlled shunt active power filter for the harmonics and reactive power compensation

of a nonlinear load are implemented. Both controllers performance under certain conditions and different system parameters is studied. The advantages of Digital controller over conventional controllers like PI controllers are that FPGA's provide reconfigurable hardware designs, Low cost development (reprogrammable ability),FPGA's can process information faster than a general purpose DSP, Bit widths for data registers can be selected based on application needs, Designed in Hardware Description Language (VHDL or VERILOG) the controller becomes independent of process technology, they can work with imprecise inputs, can handle non-linearity, load disturbances etc.

1.3 Thesis outline

The body of this thesis consists of the following seven chapters including first chapter:

• In Chapter 2, a description of the structure of the shunt active power filter, the basic compensation principle, reference and source current estimation and role of DC side capacitor is given.

• Chapter 3 gives the description of Synchronous Reference Theory (SRF) and its requirement application in designing a shunt active filter and the Hysteresis current controller and its type .In this chapter the rules of HCC to control the switching action of APF is also described.

• Chapter 4gives detail idea to implement a processor /controller using FSMD architecture. In this chapter finite state machine and DATAPATH is described to implement a controller for shunt APF.

• In chapter 5, design of digital controller for shunt active power filter is described using PI-controller (uses FSMD architecture) and the HCC module is described, both written in RTL level VHDL code for FPGA implementation.

• Chapter 6 deals with simulation results, obtained from the simulation of a three phase shunt APF using HCC and AHCC ,MATLAB simulation of three phase four-wire system and results after implementing the digital controller using FPGA.

• The conclusions of the thesis and recommendations for future work are summarized in Chapter 7.

Chapter 2

SHUNT ACTIVE POWER FILTER

Basic compensation principle

Estimation of reference current

Estimation of source current

Role of DC side capacitor

Selection of Lc and Vdc,ref

Design of DC side capacitor (Cdc)

SHUNT ACTIVE POWER FILTER

The shunt-connected active power filter, with a self-controlled dc bus, has a topology similar to that of a static compensator (STATCOM) used for reactive power compensation in power transmission systems. Shunt active power filters compensate load current harmonics by injecting equal-but opposite harmonic compensating current. In this case the shunt active power filter operates as a current source injecting the harmonic components generated by the load but phase-shifted by 180°.Figure 2.1 shows the connection of a shunt active power filter and Figure 2.2shows how the active filter works to compensate the load harmonic currents [1-5].

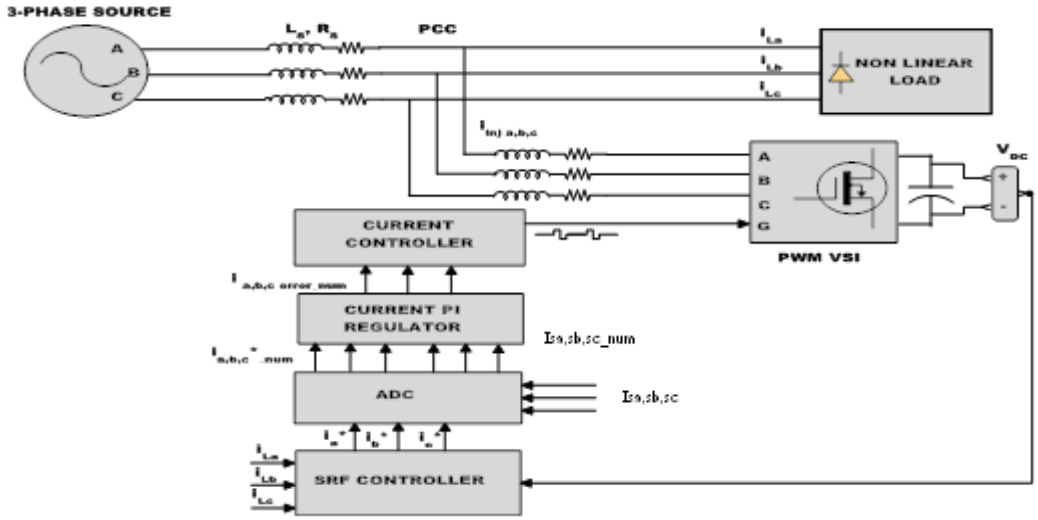


Figure 2.1 SRF with HCC based APF implementation.

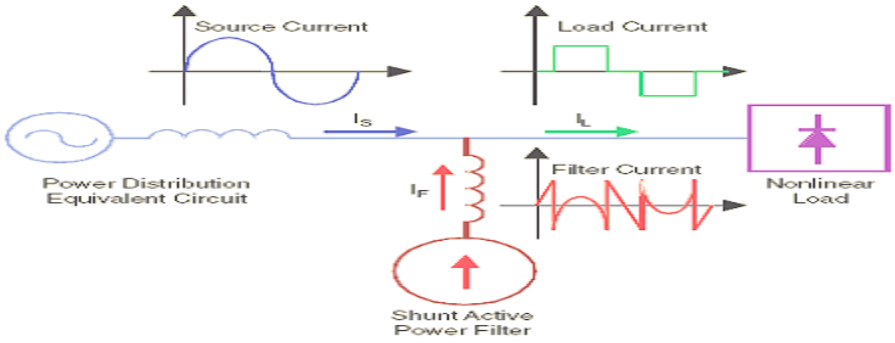


Figure 2.2 Basic Compensation Principles.

2.1 BASIC COMPENSATION PRINCIPLE

Figure 2.2.Shows the basic compensation principle of a shunt active power filter. It is controlled to draw/supply a compensating current ic from / to the utility, so that it cancels current harmonics on the AC side, and makes the source current in phase with the source voltage. The load current waveform, the desired mains current and compensating current injected by the active filter containing all the harmonics, to make mains current sinusoidal [6].

2.2ESTIMATIONOF REFERENCE CURRENT

From Figure.2.1.1, the instantaneous currents can be written as

$$I_s(t) = i_l(t) - i_c(t) \qquad (2.2.1)$$

Source voltage is given by

$$V_s(t) = V_m \sin wt \qquad (2.2.2)$$

If a non-linear load is applied, then the load current will have a fundamental component and harmonic components which can be represented as

$$I_l(t) = \sum (In \sin (nwt+\Phi_n)$$

$$= I_1(x) \sin (nwt+ \Phi_n) + \sum_{n=2} \sin (nwt+ \Phi n) \qquad (2.2.3)$$

The instantaneous load power can be given as

$$P_l(t) = V_s(t) * I_l(t) \qquad (2.2.4)$$

$$= VmI_1 \sin^2 wt * \cos\Phi 1 + VmI_1 \sin wt * \cos wt * \sin\Phi 1 + Vm \sin wt * \sum I_n \sin (nwt+\Phi n)$$

$$= P_f(t) + P_r(t) + P_h(t) \qquad (2.2.5)$$

From (2.2.4), the real (fundamental) power drawn by the load is

$$P_f(t) = V_m I_1 \sin^2 wt * \cos\Phi 1 = Vs(t) * is(t) \qquad (2.2.6)$$

From (2.2.6), the source current supplied by the source, after compensation is

$$Is(t) = Pf(t)/Vs(t) = I_1 \cos\Phi 1 \sin wt = I_m \sin wt \qquad (2.2.7)$$

Where $I_{sm} = I_1 \cos\Phi 1$

There are also some switching losses in the PWM converter, and hence the utility must supply a small overhead for the capacitor leakage and converter switching losses in addition to the real power of the load. The total peak current supplied by the source is therefore

$$I_{sp} = I_{sm} + I_{s1} \quad (2.2.8)$$

If the active filter provides the total reactive and harmonic power, then is(t) will be in phase with the utility voltage and purely sinusoidal. At this time, the active filter must provide the following compensation current:

$$I_c(t) = I_l(t) - I_s(t) \quad (2.2.9)$$

Hence, for accurate and instantaneous compensation of reactive and harmonic power it is necessary to estimate, i.e. the fundamental component of the load current as the reference current.

2.3 ESTIMATIONOF SOURCE CURRENT

The peak value of the reference current Isp can be estimated by controlling the DC side capacitor voltage. Ideal compensation requires the mains current to be sinusoidal and in phase with the source voltage, irrespective of the load current nature. The desired source currents, after compensation, can be given as

$$I_{sa}^{*}(t) = I_{sp}\sin wt \quad (2.3.1)$$

$$I_{sb}^{*}(t) = I_{sp}\sin(wt - 120^0) \quad (2.3.2)$$

$$I_{sc}^{*}(t) = I_{sp}\sin(wt + 120^0) \quad (2.3.3)$$

Where I_{sp} $(=I_1\cos\Phi_1 + I_{sl})$ the amplitude of the desired source current, while the phase angle can be obtained from the source voltages. Hence, the waveform and phases of the source currents are known, and only the magnitudes of the source currents need to be determined. This peak value of the reference current has been estimated by regulating the DC side capacitor voltage of the PWM inverter. This capacitor voltage is compared with a reference value and the error is processed in a PI controller. The SRF theory is used for reference current generation and

also the reference currents can be estimated by multiplying this peak value with unit sine vectors in phase with the source voltages [7-9].

2.4 ROLE OF DC SIDE CAPACITOR

The DC side capacitor serves two main purposes: (i) it maintains a DC voltage with small ripple in steady state, and (ii) serves as an energy storage element to supply real power difference between load and source during the transient period. In the steady state, the real power supplied by the source should be equal to the real power demand of the load plus a small power to compensate the losses in the active filter. Thus, the DC capacitor voltage can be maintained at a reference value. However, when the load condition changes the real power balance between the mains and the load will be disturbed. This real power difference is to be compensated by the DC capacitor. This changes the DC capacitor voltage away from the reference voltage. In order to keep satisfactory operation of the active filter, the peak value of the reference current must be adjusted to proportionally change the real power drawn from the source. This real power charged/discharged by the capacitor compensates the real power consumed by the load. If the DC capacitor voltage is recovered and attains the reference voltage, the real power supplied by the source is supposed to be equal to that consumed by the load again. Thus, in this fashion the peak value or the reference source current can be obtained by regulating the average voltage of the DC capacitor. A smaller DC capacitor voltage than the reference voltage means that the real power supplied by the source is not enough to supply the load demand. Therefore, the source current (i.e. the real power drawn from the source) needs to be increased, while a larger DC capacitor voltage than the reference voltage tries to decrease the reference source current. This change in capacitor voltage has been verified from the simulation results. The real/reactive power injection may result in the ripple voltage of the DC capacitor. A low pass filter is generally used to filter these ripples, which introduce a finite delay. To avoid the use of this low pass filter the capacitor voltage is sampled at the zero crossing of the source voltage. A continuously changing reference current makes the compensation non-instantaneous during transient. Hence, this voltage is sampled at the zero crossing of one of the phase voltage, which makes the compensation instantaneous. Sampling only twice in cycle as compared to six times in a cycle leads to a slightly higher DC capacitor voltage rise/dip during transients, but settling time is less.

The design of the power circuit includes three main parameters:

• Selection of filter inductor, Lc.

• Selection of DC side capacitor, Cdc.

• Selection of reference value of DC side capacitor voltage, Vdcref.

2.5 SELECTION OF Lc AND Vdc,ref

The design of these components is based on the following assumptions:

1. The AC source voltage is sinusoidal.

2. To design of Lc, the AC side line current distortion is assumed to be 5%.

3. Fixed capability of reactive power compensation of the active filter.

4. The PWM converter is assumed to operate in the linear modulation mode (i.e. $0 \leq ma \leq 1$).

2.6 DESIGN OF DC SIDE CAPACITOR (Cdc)

The design of the DC side capacitor is based on the principle of instantaneous power flow. The selection of Cdc can be governed by reducing the voltage ripple [2]. As per the specification of the peak to peak voltage ripple (Vdc p-p (max)) and rated filter current (Ic1, rated), the DC side capacitor Cdc can be found from equation

$$C_{dc}=(\Pi * I_{c1rated})/\sqrt{3}WV_{dc,p\text{-}p(max)}) \quad (2.6)$$

Chapter 3

SYNCHRONOUS REFERENCE FRAME (SRF) THEORY

And HYSTERESIS CURRENT CONTROLLER

Basic Principle

SRF Controller Implementation

2-Level hysteresis current controller

3-Level hysteresis current controller

Adaptive hysteresis current controller

3. SRF CONTROLLER

The synchronous reference frame theory or d-q theory is based on time-domain reference signal estimation techniques. It performs the operation in steady-state or transient state as well as for generic voltage and current waveforms. It allows controlling the active power filters in real-time system. Another important characteristic of this theory is the simplicity of the calculations, which involves only algebraic calculation. The basic structure of SRF methods consists of direct (d-q) and inverse (d-q)-1 park transformations as shown in Figure 3.1, which allows the evaluation of a specific harmonic component of the input signals [15].

3.1 BASIC PRINCIPLE

The reference frame transformation is formulated from a three-phase a−b−c stationary system to the direct axis (d) and quadratic axis (q) rotating coordinate system. In a-b-c, stationary axes are separated from each other by 120^0as shown in Figure 3.1.

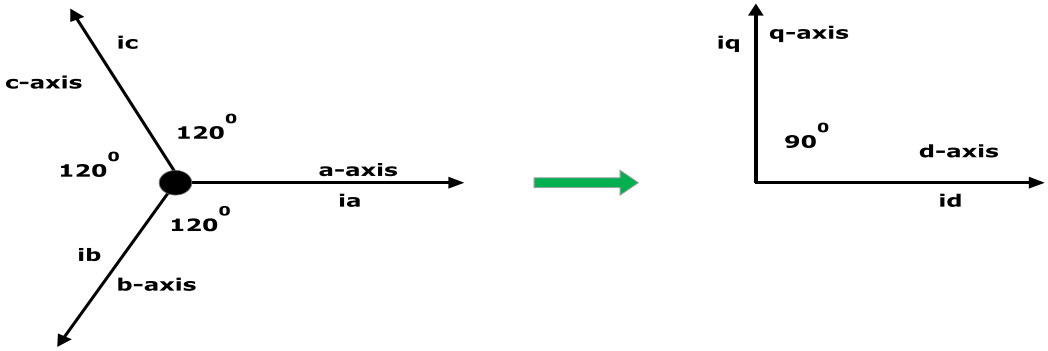


Figure 3.1 a-b-c to d-q-0 transformation.

3.2 SRF CONTROLLER IMPLEMENTATION

The instantaneous space vectors, va and ia are set on the a-axis, vb and ib are on the b axis, similarly Vc and ic are on the c axis. These three phase space vectors stationary coordinates are easily transformed into two axis d-q rotating reference frame transformation. This algorithm facilitates deriving id-iq (rotating current coordinate) from three-phase stationary coordinate load current iLa, iLb, iLc.

$$\begin{pmatrix} iLd \\ iLq \\ iL0 \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} \cos(\theta) & \cos(\theta - 2\pi/3) & \cos(\theta + 2\pi/3) \\ \sin(\theta) & \sin(\theta - 2\pi/3) & \sin(\theta + 2\pi/3) \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{pmatrix} \begin{pmatrix} iLa \\ iLb \\ iLc \end{pmatrix} \quad (3.2)$$

The d-q transformation output signals depend on the load current (fundamental and harmonic components) and the performance of the Phase Locked Loop (PLL). The PLL circuit provides the rotation speed (rad/sec) of the rotating reference frame, where t is set as fundamental frequency component [15]. The PLL circuit provides the vectorized 50 Hz frequency and 300 phase angle followed by sinϴ and cosϴ for synchronization. The id-iq current are passed through low pass filter (LPF) for filtering the harmonic components of the load current, which allows only the fundamental frequency components. The LPF is a second order Butterworth filter, whose cut off frequency is selected to be 50 Hz for eliminating the higher order harmonics. The PI controller is used to eliminate the steady state error of the DC component of the d-axis reference signals. Furthermore, it maintains the capacitor voltage nearly constant. The DC-side capacitor voltage of PWM-voltage source inverter is sensed and compared with desired reference voltage for calculating the error voltage. This error voltage is passed through a PI controller whose propagation gain (KP) and integral gain (KI) is 0.1 and 1 respectively.

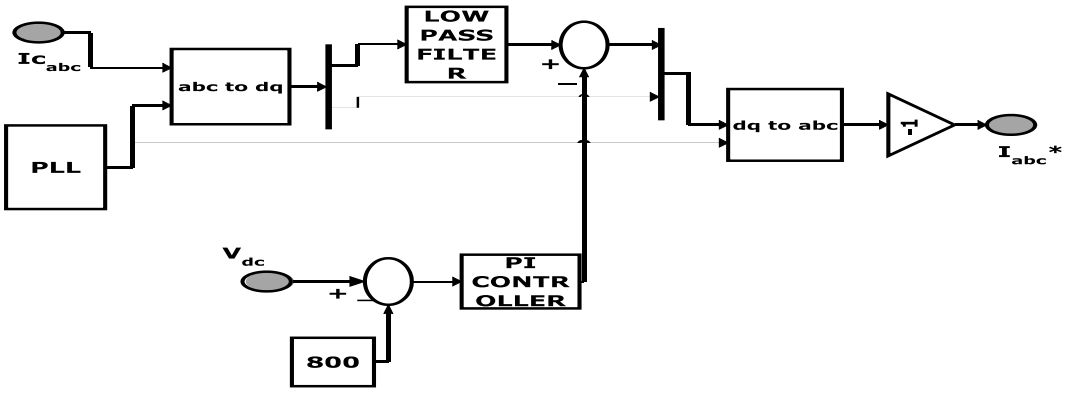


Figure 3.2 Synchronous d-q-0 reference frame based compensation algorithm.

3.3 HYSTERESIS CURRENT CONTROLLER

The hysteresis band current control for active power filter is used to generate the switching pattern of the inverter. There are various current control methods proposed for active

power filter configurations; but the hysteresis current control method is proven to be the best among other current control methods, because of quick current controllability, easy implementation and unconditioned stability. The hysteresis band current control is robust, provides excellent dynamics and fastest control with minimum hardware. This work also presents two-level and three-level hysteresis current controller for proposed active power filter and a comparison between them [21-28].

3.4 TWO-LEVEL HYSTERESIS CURRENT CONTROLLER:

Conventional hysteresis current control operates the PWM voltage source inverter by comparing the current error $e(t)$ against fixed hysteresis bands. This current error is difference between the desired current $i_{ref}(t)$ and the current being injected by the inverter $i_{actual}(t)$ as shown in Figure 3.3.

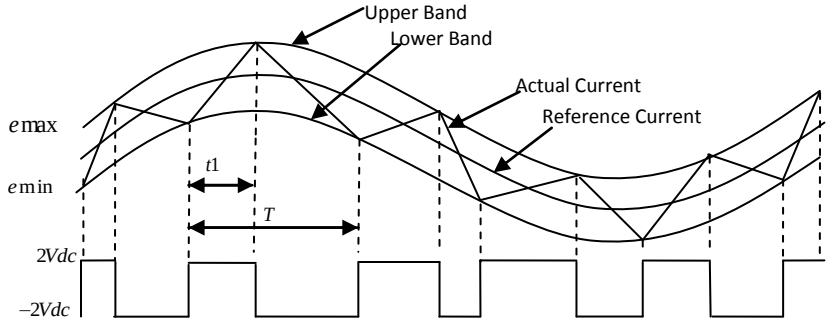


Figure 3.3 Diagram of two-level hysteresis current control.

If the error current exceeds the upper limit of the hysteresis band, the upper switch of the inverter arm is turned OFF and the lower switch is turned ON. If the error current crosses the lower limit of the hysteresis band, the lower switch of the inverter arm is turned OFF and the upper switch is turned ON. These two level switching strategies does not use the inverter zero output condition, but the 3-level switching is possible by incorporating zero level [21-22].

This control strategy of the switching frequency is determined as follows. The rate of change of phase current at any point of time is written as

$$\frac{dI}{dt} = \frac{\Delta I}{\Delta t} = \frac{\pm 2V_{dc}}{L} \Rightarrow \Delta t = \frac{\Delta I\, L}{\pm 2V_{dc}} \qquad (3.4.1)$$

Where $\pm 2V_{dc}$ is depending on inverter switching state, ΔI is rate of change of inverter current, Δt is rate of change of time period and L is the series inductance of the filter. A complete switching cycle goes from $0 \rightarrow t_1 \rightarrow T$.

For the period $0 \rightarrow t_1$, $\Delta t = t_1$ and therefore:

$$t_1 = \frac{+\Delta I\, L}{2V_{dc}} \qquad (3.4.2)$$

For the period $t_1 \rightarrow T/2$, $\Delta t = T - t_1$ and therefore:

$$T - t_1 = \frac{-\Delta I\, L}{-2V_{dc}} \qquad (3.4.3)$$

The total switching time is obtained by combining these two equations and it give as:

$$f_s = \frac{1}{T} = \frac{{V_{dc}}^2}{\Delta I\, L V_{dc}} \rightarrow f_{\max} = \frac{V_{dc}}{\Delta I\, L} \qquad (3.4.4)$$

Here $f_{\max}$ is maximum switching frequency of the inverter. The variation in the switching frequency influences the performance of the current controller, both in terms of harmonics and the maximum switching frequency.

3.5 THREE-LEVEL HYSTERESIS CURRENT CONTROLLER

The implementation of three level modulation hysteresis controller are set as upper and lower band overlap boundaries and displacement by a small offset current. Whenever the current error $e(t)$ crosses an outer hysteresis boundary, that time the inverter output is set to an active positive or negative output to force a reversal of the current error. Similarly whenever the current error reaches an inner hysteresis boundary, that time the inverter output is set to a zero condition and the current error will be forced to reverse direction without reaching the next outer boundary. If the selection of a zero output does not reverse the current error, it will continue through the inner boundary to the next outer hysteresis boundary, at which point an opposite polarity inverter output will be commanded and the current will reverse anyway [23-25].

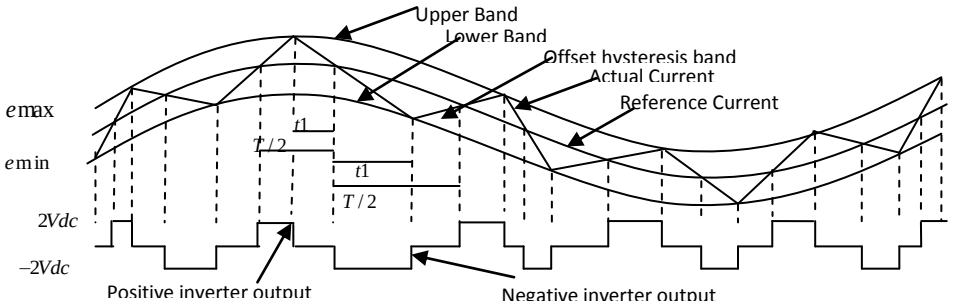


Figure 3.4 Diagram of three-level hysteresis current control.

This switching process is shown in Figure 3.4, where the current error is bounded between the upper-inner and lower-outer hysteresis boundaries for a positive inverter output, similarly the lower-inner and upper-outer hysteresis boundaries for a negative inverter output. This new switching process introduces a positive or negative dc offset error into the average output current that is depending on the active output voltage [13-16]. However, this error can be corrected by adding a compensation factor of hysteresis band offset magnitude to the reference current; it is positive when a positive inverter output is in utilize and negative when a negative inverter output is in utilize. The MATLAB program for a-phase switching operation of the inverter is given as

```
If errora>0
If errora>=(h)
swa=0;
end
if errora<=del
swa=1;
end
if errora<0
if errora<=(-h)
swa=2;
end
if errora>=(-del)
swa=1;
end
```

If swa=0 implies the switch state is +Vdc; else if swa=1 is implies the switch state is 0; else if swa=2 is implies the switch state is -Vdc; Similarly the b-phase and c-phase switching function can be performed to the three phase voltage source inverter.

The switching frequency for the three level controllers can be derived as follows; a three level switching cycle goes from $0 \rightarrow t_1 \rightarrow T/2$.

For the period $0 \rightarrow t_1, \Delta t = t_1$ and therefore:

$t_1 = -\Delta I\, L$

For the period $t_1 \rightarrow T/2,\ \Delta t = T/2 - t_1$ and therefore:

$$T/2 - t_1 = \frac{+\Delta I\, L}{+2V_{dc}} \qquad (3.5.1)$$

The total switching time is obtained by combining these two equations and it becomes:

$$f_s = \frac{2V_{dc}}{8\Delta I\, L V_{dc}} \rightarrow f_{\max} = \frac{V_{dc}}{4\Delta I\, L} \qquad (3.5.2)$$

Here $f_{\max}$ is maximum switching frequency of the inverter. Comparing equation (3.4.4) with (3.5.2), it can be seen that the maximum switching frequency has been reduced by a factor of 4 for the three level hysteresis controllers. Therefore, it will have a significantly reduced harmonic bandwidth compared to a two level hysteresis controller at the same average switching frequency and an expected improvement in harmonic performance.

3.6 ADAPTIVE HYSTERESIS CURRENT CONTROLLER

The hysteresis band current control is characterized by unconditioned stability, very fast response, and good accuracy. On the other hand, the basic hysteresis technique exhibits the difference between i and i_{ref} is referred to as δ. The hysteresis band current controller assigns the switching pattern of APF [26-28].

$$\delta = i - i_{ref} \qquad (3.6.1)$$

The switching logic is formulated as follows:

If δ >HB upper switch is OFF and lower switch is ON

(S_4=1, S_1=0).

If δ <-HB upper switch is ON and lower switch is OFF

(S_4=0, S_1=1).

The switching logic for phase B and C is similar as phase A, using corresponding reference and measured currents and hysteresis bandwidth (HB). In case of hysteresis band current control the rate of change of the line current vary the switching frequency, therefore the switching frequency does not remain constant throughout the switching operation, but varies along with the current waveform. Furthermore, the line inductance value of the APF and the capacitor voltage are the main parameters determining the rate of change of line currents.

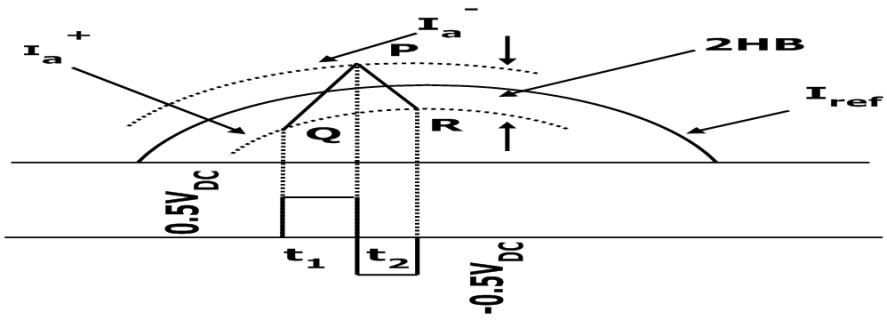


Figure 3.5 Current and voltage waves with hysteresis band current controller.

The following equations can be written in the respective switching intervals t_1 and t_2 from Figure 3.5.

$$di_a^+ = \frac{1}{L}\ 0.5V_{DC} - V_a \tag{3.6.2}$$

$$di_a^- = -\frac{1}{L}\ 0.5V_{DC} + V_a \tag{3.6.3}$$

From Figure 3.5.

$$\frac{di_a^+}{dt}t_1 - \frac{di_{aref}}{dt}t_1 = 2HB \tag{3.6.4}$$

$$\frac{di_a^-}{dt}t_2 - \frac{di_{aref}}{dt}t_2 = -2HB \tag{3.6.5}$$

$$t_1 + t_2 = T_c = \frac{1}{f_c} \tag{3.6.6}$$

Where t_1 and t_2 are the respective switching intervals and f_c is the switching frequency.

Adding equation (3.6.4) and (3.6.5) and substituting in equation (3.6.6) we can write,

$$\frac{di_a^+}{dt}t_1 + \frac{di_a^-}{dt}t_2 - \frac{1}{f_c}\frac{di_{aref}}{dt} = 0 \tag{3.6.7}$$

Subtracting equation (3.6.5) from (3.6.4)

$$\frac{di_a^+}{dt}t_1 - \frac{di_a^-}{dt}t_2 - \left(t_1 - t_2\right)\frac{di_{aref}}{dt} = 4HB \tag{3.6.8}$$

Substituting equation (3.6.6) in (3.6.8)

$$\left(t_1 + t_2\right)\frac{di_a^+}{dt} - \left(t_1 - t_2\right)\frac{di_{aref}}{dt} = 4HB \tag{3.6.9}$$

Substituting equation (3.6.6) in equation (3.6.9) and solving

$$t_1 - t_2 = \frac{di_{aref}/dt}{f_c\ di_a^+/dt} \tag{3.6.10}$$

Substituting equation (3.6.3) in (3.6.7)

$$HB = \frac{0.125V_{DC}}{f_c L}\left[1 - \frac{4L^2}{{V_{DC}}^2}\left(\frac{V_a}{L} + m\right)^2\right] \tag{3.6.11}$$

Where f_c is modulation frequency, m = di_{aref} /dt is the slope of command current wave.

.

Chapter 4

FSMD ARCHITECTURE

Finite State Machine

Datapath Description

Description of RAM, ALU, REGISTER, MULTIPLEXER

FSMD ARCHITECTURE

The Von Neumann model of a computer, picture in Figure 4.1, consists of four main components: the input, the output, the memory and the CPU (central processing unit). In order for the DATAPATH to execute the operations automatically, the control unit is required. The control unit, also known as the controller, controls the operations of the DATAPATH, and therefore, the operations of the entire microprocessor. The controller is a finite state machine (FSM) because it is a machine that executes by going from one state to another and the fact that there are only a finite number of states for the machine to go to. The controller is made up of three parts: the next-state logic, the state memory, and the output logic. The purpose of the state memory is to remember the current state that the FSM is in. The next-state logic is the circuit for determining what the next state ought to be for the machine and the output logic is the circuit for generating the actual control signals for controlling the DATAPATH.

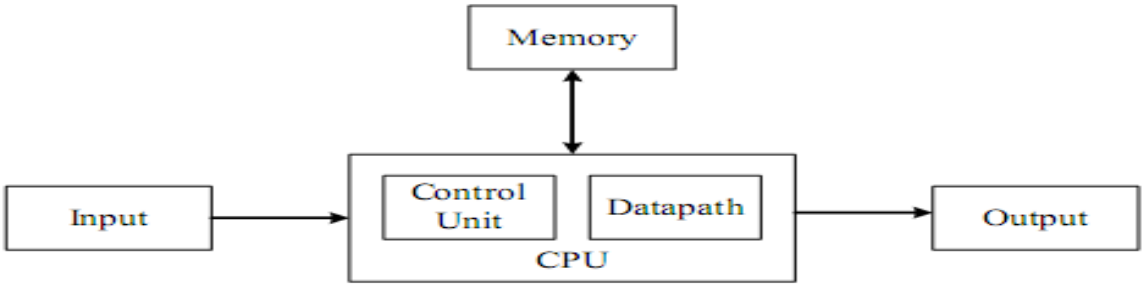


Figure 4.1 Von Neumann model of a computer.

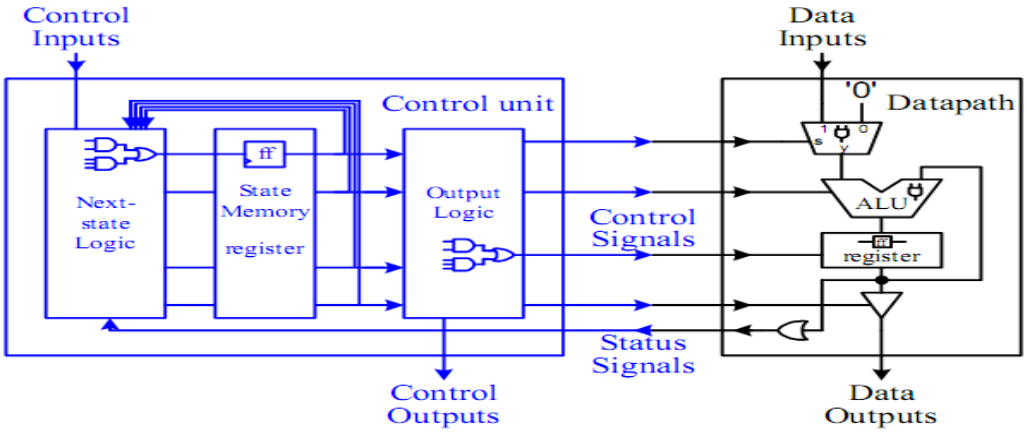


Figure 4.2 Internal parts of a FSMD.

4.1 FINITE-STATE-MACHINE (FSM) MODEL

A sequential circuit operates by stepping through a sequence of states. Since the state memory is finite, therefore the total number of different possible states is also finite. For this reason, a sequential circuit is also referred to as a finite-state machine (FSM). Although there is only a finite number of a different state, the FSM can go to any of these states as many times as necessary [28].

Figure 4.3 (a) shows the general schematic for the Moore FSM where its outputs are dependent only on its current state. Figure 4.3 (b) shows the general schematic for the Mealy FSM where its outputs are dependent on both the current state of the machine and also the inputs. In both figures, we see that the inputs to the next-state logic are the primary input signals and the current state of the machine. The next-state logic generates excitation values to change the contents of the state memory.

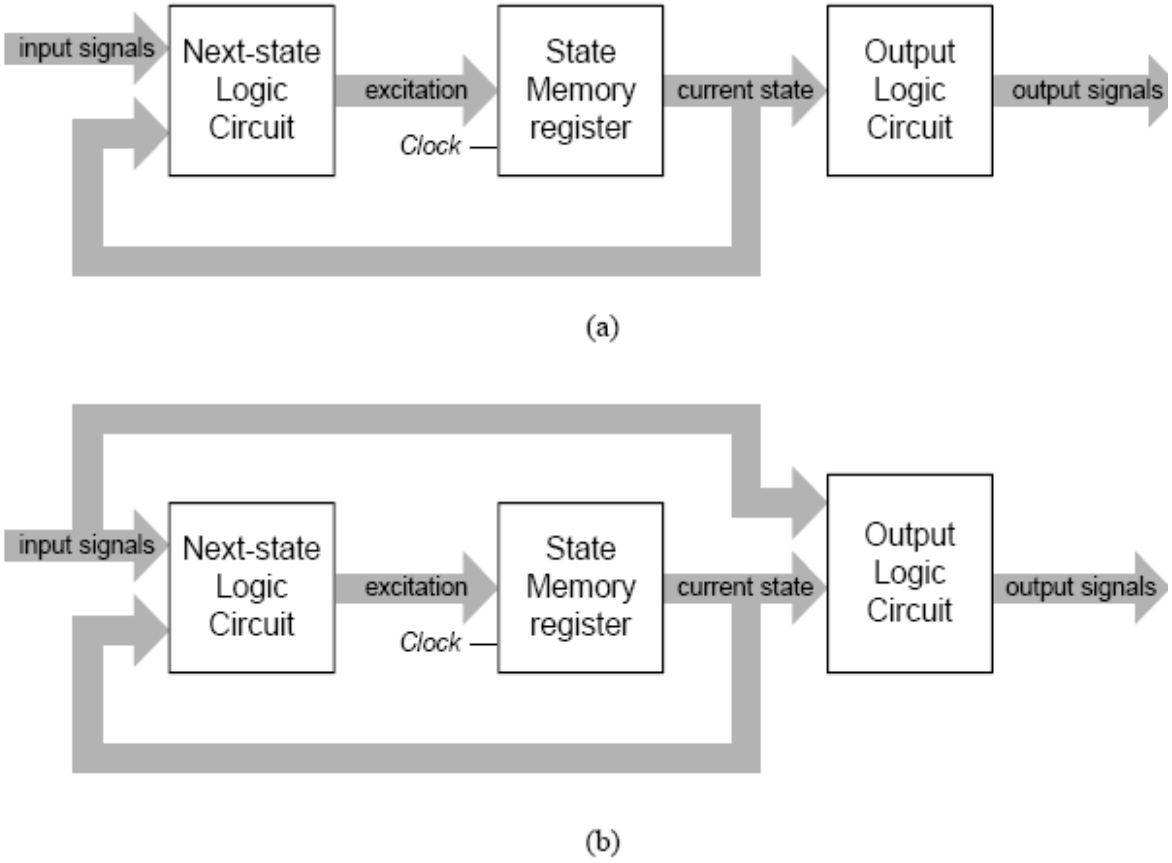


Figure 4.3 Finite-state machine models: (a) Moore FSM; (b) Mealy FSM.

4.2 DATAPATH DESCRIPTION

The DATAPATH includes (1) functional units such as adders, shifters, multipliers, ALUs, and comparators, (2) registers and other memory elements for the temporary storage of data, and (3) buses and multiplexers for the transfer of data between the different components in the DATAPATH. External data can be entered into the DATAPATH through the data input lines. Results from the computation are provided through the data output lines. In order for the DATAPATH to function correctly; appropriate control signals must be asserted at the right time. Control signals are needed for all the select and control lines for all the components used in the DATAPATH. This includes all the select lines for multiplexers, ALU and other functional units having multiple operations, all the read/write enable signals for registers, address lines for memory and enable signals. The operation of the DATAPATH is determined by which control signals are asserted and at what time. In a controller, these control signals are generated by the control unit. In return, the DATAPATH needs to supply status signals back to the control unit in order for it to operate correctly. [28-30]

4.3 DESCRIPTIONOF RAM, ALU, REGISTER, MULTIPLEXER

4.3.1 RANDOM ACCESS MEMORY

Another main component in a computer system is memory. This can refer to as either random access memory (RAM) or read-only memory (ROM). We can make memory the same way we make the register file but with more storage locations. However, there are several reasons why we don't want to. One reason is that we usually want a lot of memory and we want it very cheap, so we need to make each memory cell as small as possible. Another reason is that we want to use a common data bus for both reading data from, and writing data to the memory.

4.3.2 ARITHMETIC LOGIC UNIT

The arithmetic logic unit (ALU) is one of the main components inside a controller that is responsible for performing arithmetic and logic operations such as addition, subtraction, multiplication, shifting, delay etc. It turns out that in constructing the circuit for the ALU, we can use the same idea as for constructing the adder/subtractor combination circuit .The primary inputs will be modified accordingly depending on the operations being performed before being passed to the full adder. The general overall circuit for a 25-bit ALU is shown in Figure 4.8.

4.3.3 REGISTER

When we want to store a byte of data, we need to combine eight flip-flops together, and have them work as a unit. A register is just a circuit with two or more D flip-flops connected together in such a way that they all work exactly the same way, and are synchronized by the same clock and enable signals. The only difference is that each flip-flop in the group is used to store a different bit of the data. Figure shows a 4-bit register with parallel load and asynchronous clear.

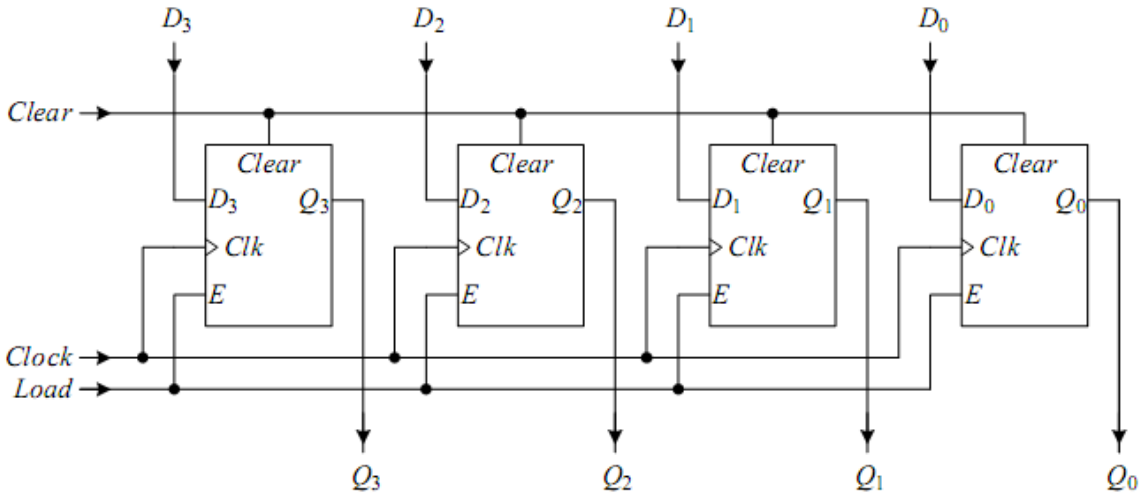


Figure 4.4 A 4-bit register with parallel load and asynchronous clear.

4.3.4 MULTIPLEXER

The multiplexer, or mux for short, allows the selection of one input signal among n signals, where n > 1 and is a power of two. Select lines connected to the multiplexer determine which input signal is selected and passed to the output of the multiplexer.

y = s'd1'd0 + s'd1d0 + sd1d0' + sd1d0

= s’d0 (d1' + d1) + sd1 (d0' + d0)

= s'd0 + sd1

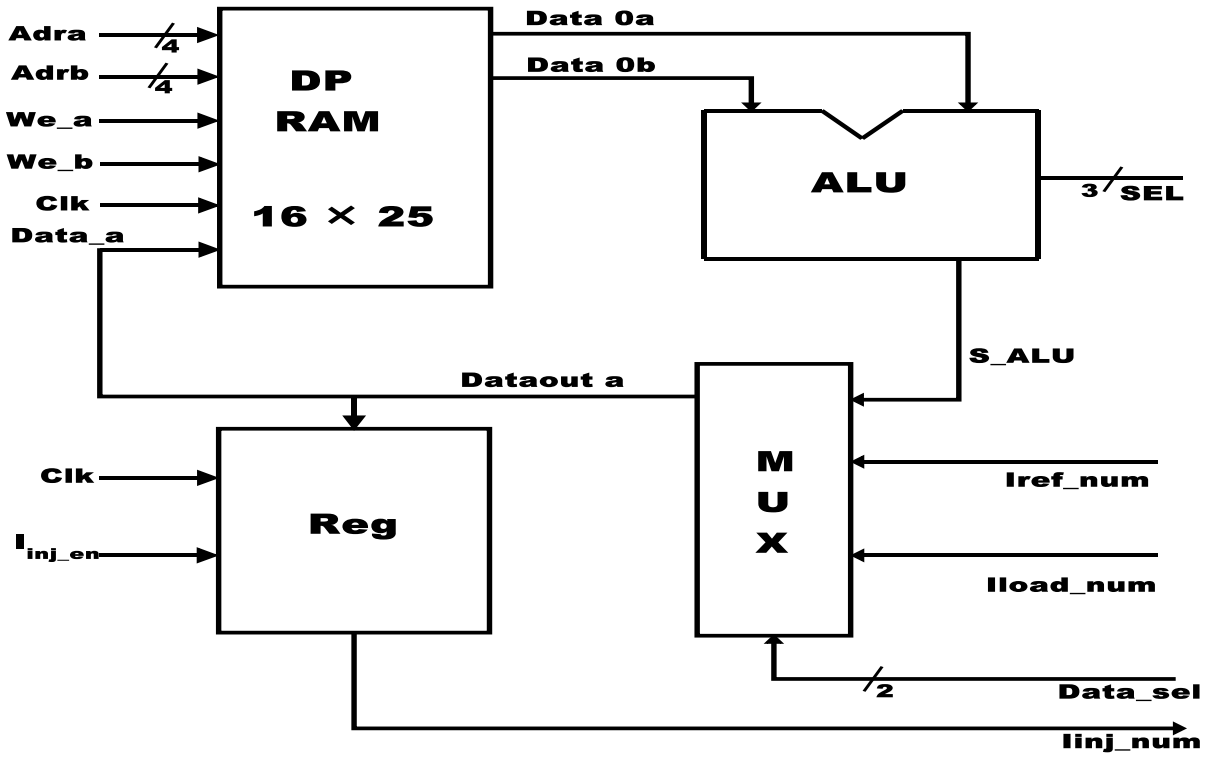


Figure 4.5DATAPATH consisting of RAM, ALU, MULTIPLEXER, REGISTER.

Chapter 5

CONTROLLER DESIGN

FSMD Model

HCC Block Description

Digital Controller Design and Operation

CONTROLLER DESIGN

The controller is designed using FSMD architecture, which consists of FSM and DATAPATH. This FSMD is used to implement the PI-Regulator. The regulator block is implemented using a DFG and it uses FSMD architecture. The various operations are controlled by state machines and operations are performed within the DATAPATH. The FSM provides control signal to DATAPATH and the DATAPATH provides status signal to FSM. The PI-regulator as well as the HCC block is developed in RTL level using VHDL code.

5.1 FSMD MODEL

Till now we have learned how to design the DATAPATH and the control unit separately. Now we will learn how to put them together to form a dedicated controller. There are several levels at which a controller can be designed. At the lowest level, we manually construct the circuit for both the control unit and the DATAPATH and then connect them together. This method of construction uses the FSM+D (FSM plus DATAPATH) model since the FSM and the DATAPATH are constructed separately. The next level of controller design also uses the FSM+D model. However, instead of manually constructing the FSM, we synthesize the FSM from behavioral VHDL. There will be a next-state process and an output process in the behavioral code. The next-state process will generate the next-state logic and the output process will generate all the control signals for driving the DATAPATH. The FSM and the DATAPATH are connected together in an enclosing entity module using the control and status signals. The advantage of using the FSM+D model is that we have full control as to how the control unit and the DATAPATH are built. However, instead of constructing the DATAPATH manually as a separate module, all the DATAPATH operations are embedded within the FSM entity using the built-in VHDL operators. During the synthesis process, the synthesizer will automatically generate a separate FSM and DATAPATH. The advantage of this model is that we do not have to design the DATAPATH, but we still have full control as to what operation is executed in which state or in which clock cycle. In other words, we have control over the timing of the circuit. Finally, a controller can be described completely at the behavioral level using VHDL. This process synthesizes the full controller with its control unit and DATAPATH automatically. Keep in mind that whether we write VHDL code for a controller using the FSM+D model.

However, since we are still writing the FSM process code manually, we still have full control as to what instructions are executed in what state and how many states are used (S0-S28).[28-31]

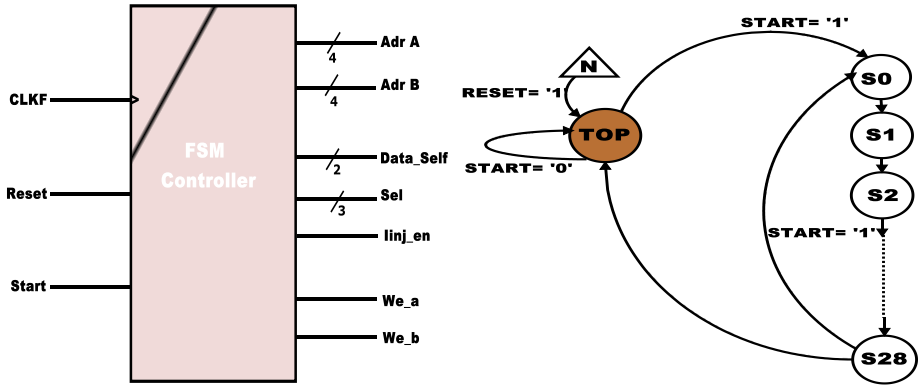


Figure 5.1 FSM (finite state machine) with states.

5.2 HCC BLOCK DESCRIPTION

The HCC block consists of three identical HCC block. Each one is developed in RTL level VHDL code. This module consists of the following signals.

- CLK : Basic clock signal.
- RESET: Asynchronous reset activates at high state.
- LOAD: Load the counter.
- DOWN: Enable for up/down counter.
- Ena : Enable for the comparator.
- C, C^{I} : Complementary control signal

The HCC block consists of an up/down counter and a comparator along with a clock divider to control the frequency of switching pulses. The output of the PI-controller blocks i.e. FSMD output I_{inj_num} is compared with the band created by up/down counter as shown in Figure. When the error exceeds the lower limit switch is ON and when it exceeds the upper limit switch is OFF. The C' is complementary of C pulse and delayed to take account of switching times in the power converters with the help of a dead band.

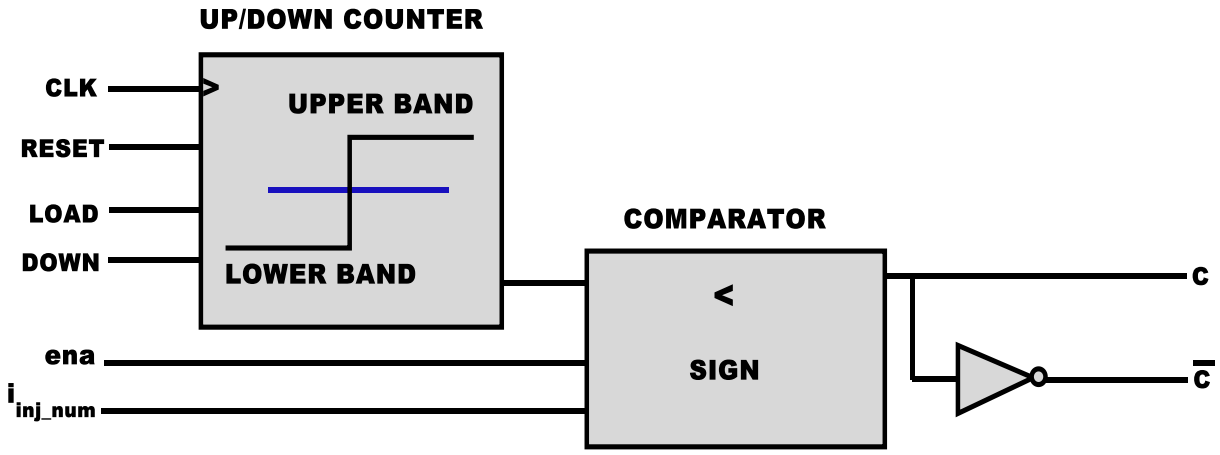


Figure 5.2 Hysteresis current controllers.

5.3 DIGITAL CONTROLLER DESIGN AND OPERATION

5.3.1 REGULATOR DESCRIPTION

The regulator block is implemented using a PI-controller that is based on a recurrent equation 5.3.1 and shown in Figure 5.3.Here 16-bit signed bits integer coding is used with thousand order precision.

$$U(n)=U(n-1)+K*E(n)+K(h/T-1)*E(n-1) \quad (5.3.1)$$

$$Error=(I_{ref}–I_{source})$$

$$I_{source}=\{(I_{mag}*I_{source})/2^{15}\}$$

$$I_{ref}=\{(I_{mag}*I_{ref\_num})/2^{15}\}$$

$$Error\_num=1024*error$$

$$=1024*(I_{ref}-I_{source})$$

$$=1024*[\{(I_{mag}*I_{ref\_num})/2^{15}\}-\{(I_{mag}*I_{source})/2^{15}\}$$

$$=2^{-5}*I_{max}*(I_{ref\_num}- I_{source})$$

$$=[I_{max}*I_{ref\_num}(>>5)]+[-I_{max}*I_{source}(>>5)] \quad (5.3.2)$$

5.3.2 BEHAVIORAL DESCRIPTION

The behavioral description of the PI-controller is implemented by using control device algorithm. It is implemented by a data flow graph (DFG).The DFG is implemented with the help of FSMD architecture for FPGA implementation.

5.3.3 FSMD ARCHITECTURE

The FSMD includes finite state machine (FSM) along with data path to implement a controller. Here space optimized FSMD architecture is used. The FSMD consist of a control unit and a data path, where the data path Operates under the control of control unit (FSM).The FSM provides control signals to the data path and data path provides status signals to the FSM. Input data are given to the data path as shown in Figure 5.3. The DATAPATH consist of RAM, ALU, MUX and RESISTER. The control unit consists of finite state machine that includes 29 states for calculating the error signal. The mathematical calculation using the data path is achieved using the following stages [28-31].

Stage-1.Acquisition:

The Iref_num and Iload_num are loaded to the memory from input via mux by choosing appropriate select line of MUX.

Stage-2 Calculation:

For the arithmetic operations, i used one state to read operands and select operators for ALU operation and next state is used to save the computed result in memory location (RAM). At the end of S28 the command value is loaded to register by making $I_{inj_en}$to become high and I_{inj_num} is available. This is the steady state error updated by PI-controller at the end of S28 as shown in Table 5.1.

Stage-3 (update):

The transition from one state to another state in FSM is occurred on positive edge of the clock input. There 29 states are used and initial state is TOP, When START = ‘0’ or RESET= ‘1’ then state is TOP else under normal case RESET=’0’ and START=’1’ the control unit undergoes through S0 to S28 for calculating the error as shown in the Figure 5.1.

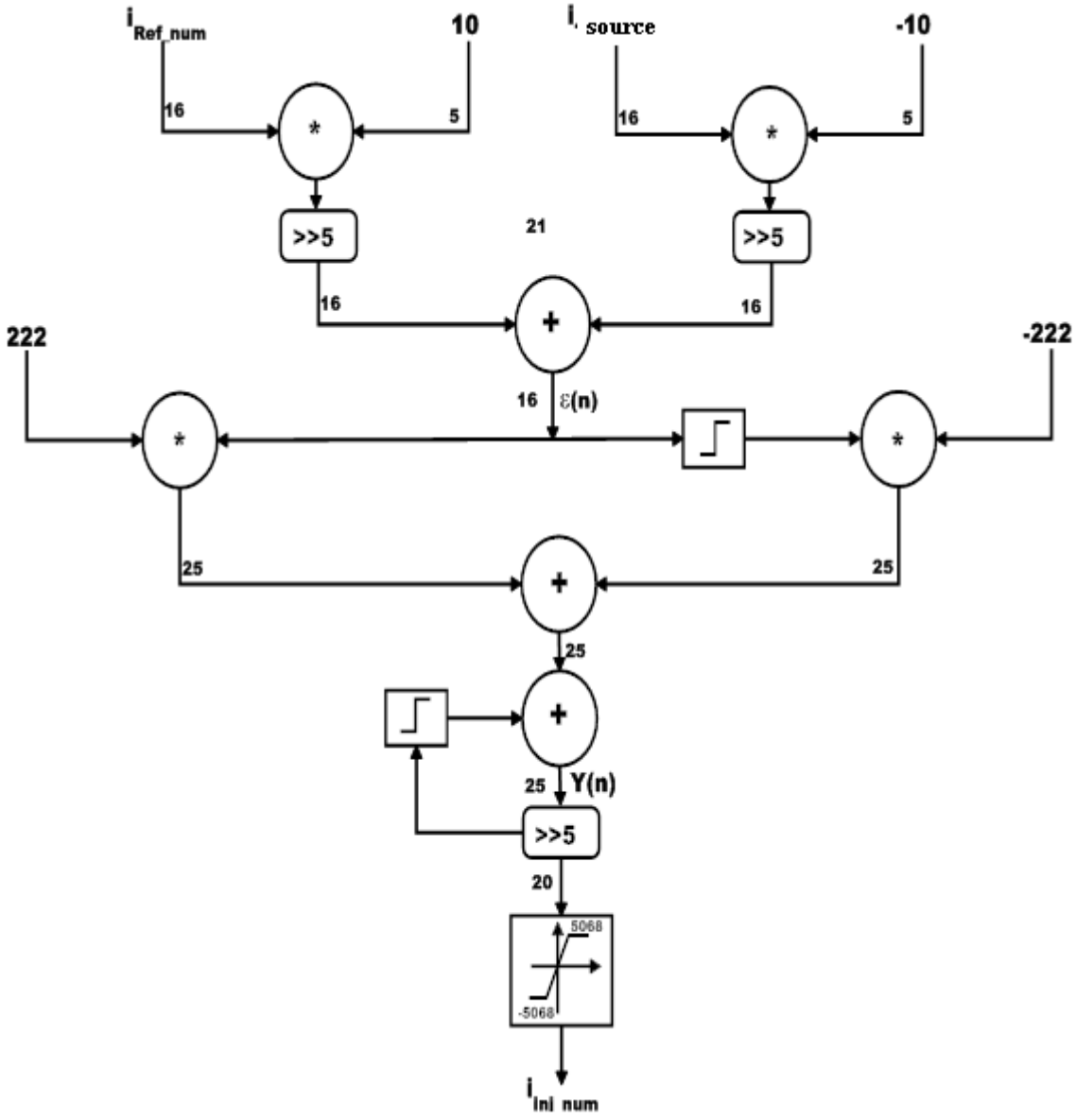


Figure 5.3 DFG of PI Regulator.

Table 5.1State updation inside FSM

STATE	Adra	Adrb	We_a	We_b	Data_sel (MUX)	Sel (ALU)	Iinj_en	Comments
S0	0	0	1	0	01	-	0	Adra(0) ←I_{ref_num}
S1	1	-	1	0	10	-	0	Adra(1) ←I_{load_num}
S2	0	2	0	0	00	001	0	Da←I_{ref_num}, Db← I_{max}
S3	8	-	1	-	-	-	0	Adra(8)←I_{ref_num}* I_{max}
S4	1	3	0	0	00	001	0	Da←I_{load_num}, Db← I_{max}
S5	9	-	1	-	-	-	0	Adra(9)←I_{load_num}* -I_{max}
S6	8	-	0	-	00	011	0	D a←Adra(8 bit * I_{max})
S7	10	-	1	-	-	-	0	>>5
S8	9	-	0	-	00	011	0	Da←I_{load}*(- I_{max})
S9	-	8	-	1	-	-	0	>>5
S10	10	8	0	0	00	000	0	Da← Adr_10, Db←Adr_8
S11	11	-	1	-	-	-	0	ξ(n)
S12	11	5	0	0	00	010	0	Da← ξ(n), Db←K(h/T)
S13	12	-	1	-	-	-	0	ξ(n)*K(h/T) ← Adra12
S14	11	-	0	-	00	100	0	Data 0a ← ξ(n)
S15	4	-	1	-	-	-	0	(4) ξ(n-1) ← ξ(n)
S16	4	6	0	0	00	010	0	Da← ξ(n-1) Db← -K(h/T)
S17	-	9	-	1	-	-	0	Adr 9 ← ξ(n-1)* -I_{max}
S18	12	9	0	0	00	000	0	Da ← 12Adra,Db←Adrb 9
S19	13	-	1	-	-	-	0	ξ(n)* K(h/T) + ξ(n-1)*K(h/T)➔13
S20	13	-	0	-	00	100	0	Da ← y(n)
S21	-	10	-	1	-	-	0	Y(n-1)← y(n)
S22	13	10	0	0	00	000	0	Da ←y(n), Db←y(n-1)
S23	14	-	1	-	-	-	0	y(n)+y(n-1)← y(n)
S24	14	-	0	-	00	011	0	Y(n)➔Da
S25	15	-	1	-	-	-	0	Y(n)>>5
S26	15	-	0	-	00	101	0	Limiter
S27	-	-	0	0	-	-	0	REG.← Result
S28	-	-	-	-	-	-	1	I_{inj_num}← REG.

Chapter 6

SIMULATION RESULTS

The performance of the three-phase four-wire shunt APLC system is evaluated through MATLAB programs in order to program and test the system under unbalanced non-linear load conditions. The system parameters values are; Line to line source voltage is 440 V; System frequency (f) is 50 Hz; DC-link capacitor C1=1100 μF and C2=1100 μF ; Reference dc voltage 600 V; Interface inductor is 2 mH and 1 Ω full bridge rectifier load 168 + j 16 Ω.

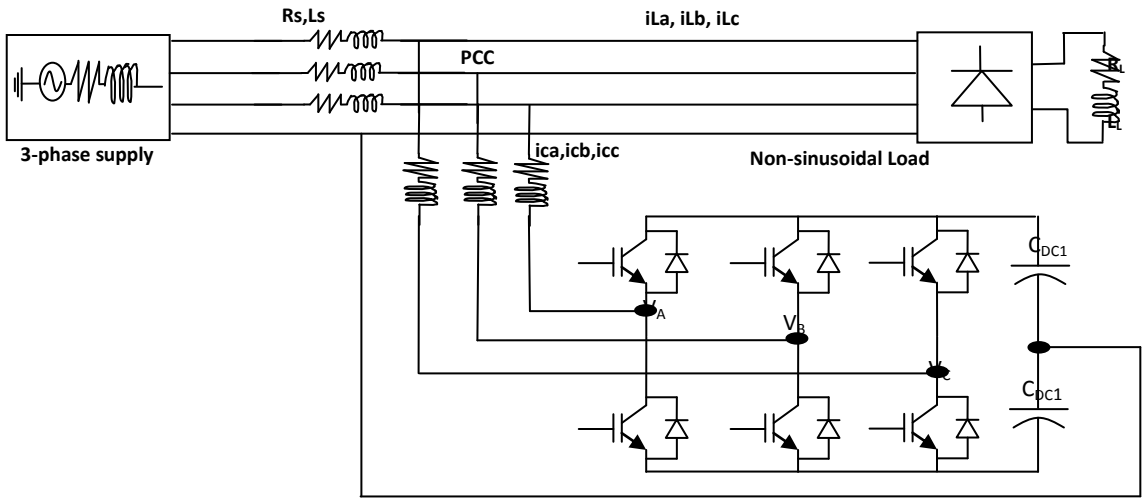


Figure 6.1 APLC system implemented with voltage source inverter.

The conventional power circuit of the voltage source inverter based active power filter connected at the point of common coupling, as shown in Figure 6.1. The voltage source inverter has six power transistors with freewheeling diodes and two energy storages capacitor on DC-side that is implemented as a four-wire active power filter [16-20].

The three-phase four-wire AC power supply connected to the unbalanced non-linear load as shown in Figure 6.1. The supply voltage is balanced and that is defined as $v_s(t) = V_m \sin \omega t$ .The measurement of the 3-phase instantaneous supply voltage is shown in Figure 6.1.

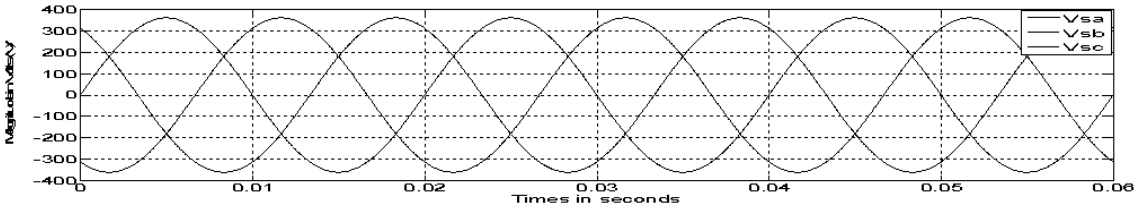


Figure 6.2 3-phase supply voltage using MATLAB.

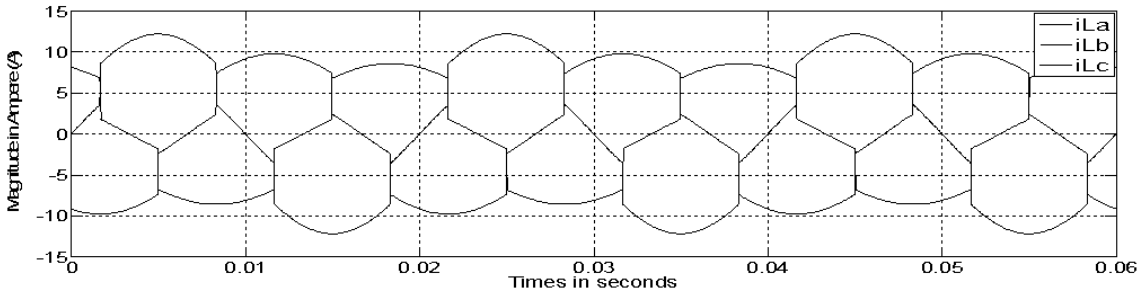


Figure 6.3 source current before compensation using MATLAB.

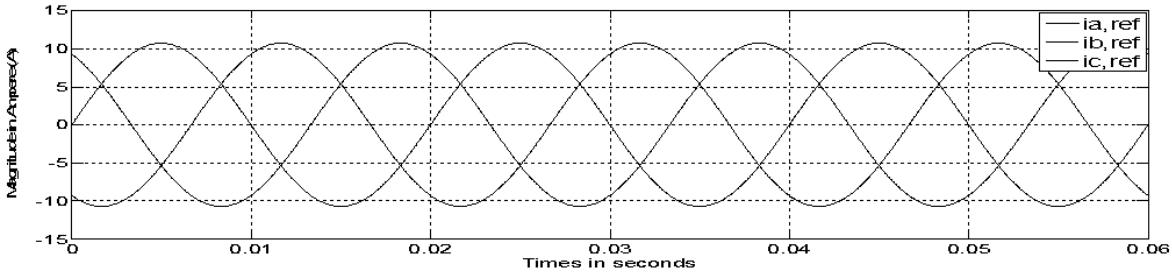


Figure 6.4 reference currents using MATLAB.

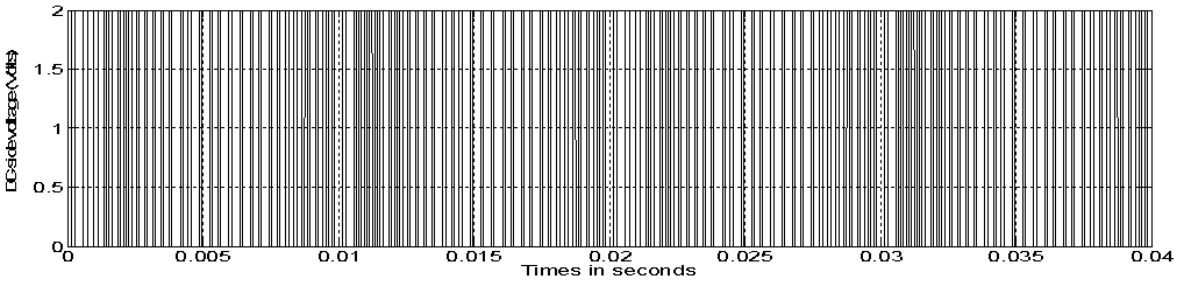


Figure 6.5switching pattern 2-level HCC using MATLAB.

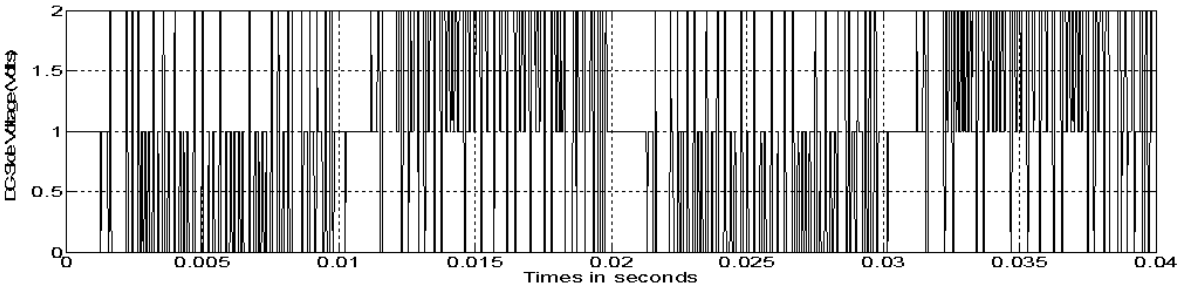


Figure 6.6switching pattern 3-level HCC using MATLAB.

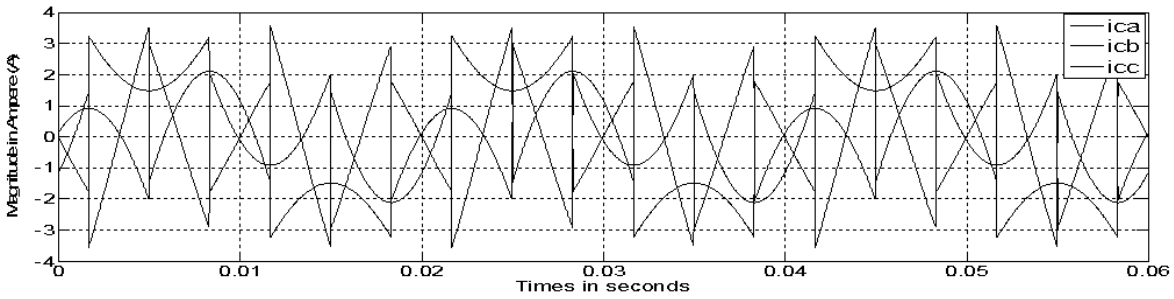


Figure 6.7compensation current using MATLAB.

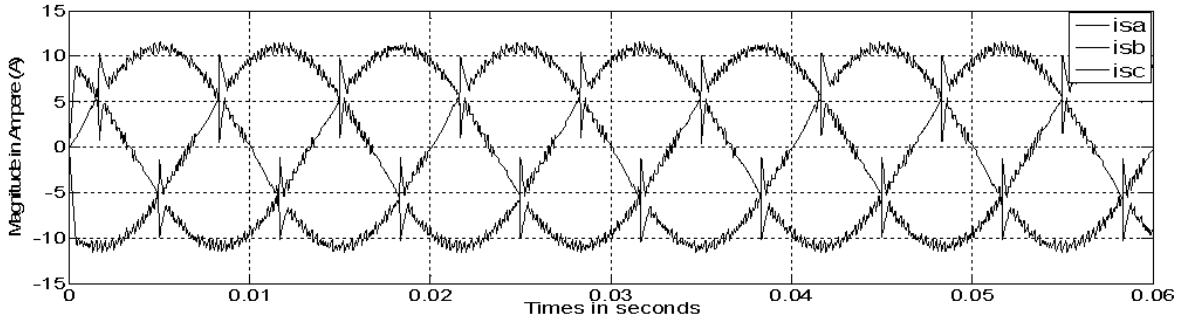


Figure 6.8 source current after compensation using MATLAB.

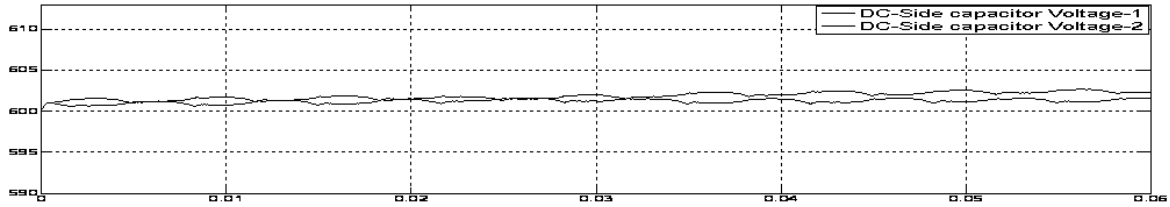


Figure 6.9DC capacitor voltage using MATLAB.

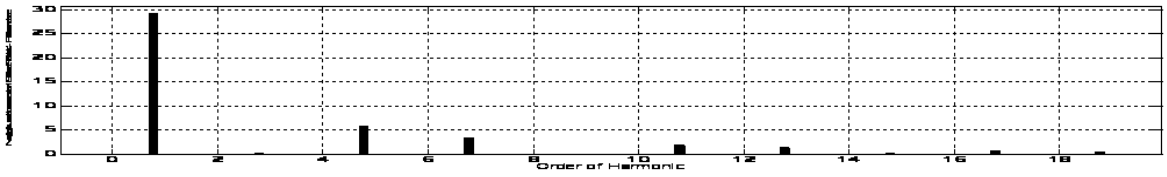


Figure 6.10 Order of harmonics before compensation using MATLAB (THD=25.41%).

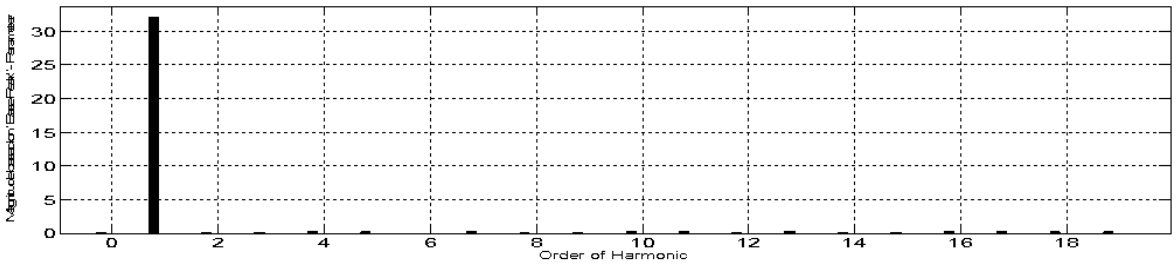


Figure 6.11 Order of harmonics with active power filter using MATLAB (THD=3.74%).

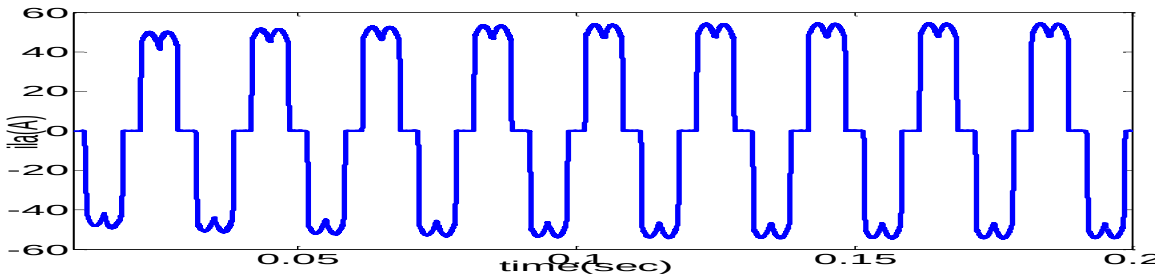


Figure 6.12Source current before Compensation for phase-a using MATLAB/SIMULINK.

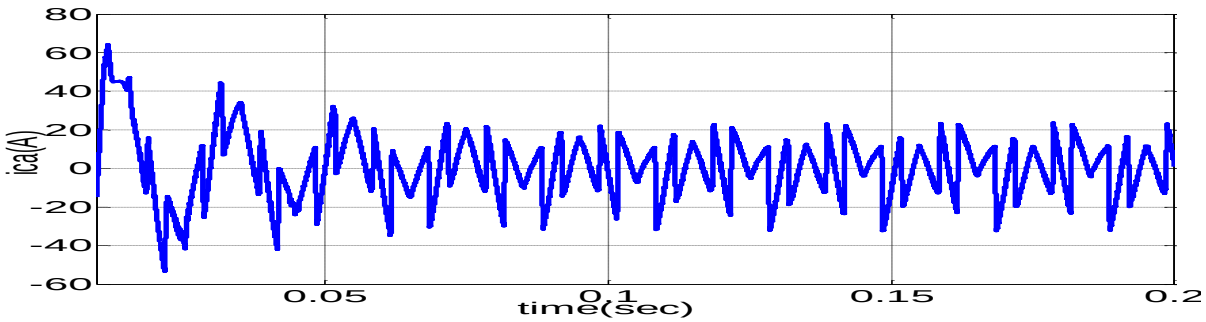


Figure 6.13Compensation current form APF for phase-a using MATLAB/SIMULINK.

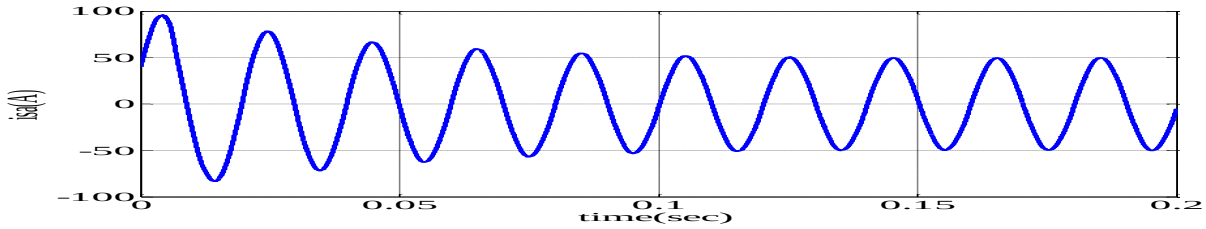


Figure 6.14 Reference current for phase-a using MATLAB/SIMULINK.

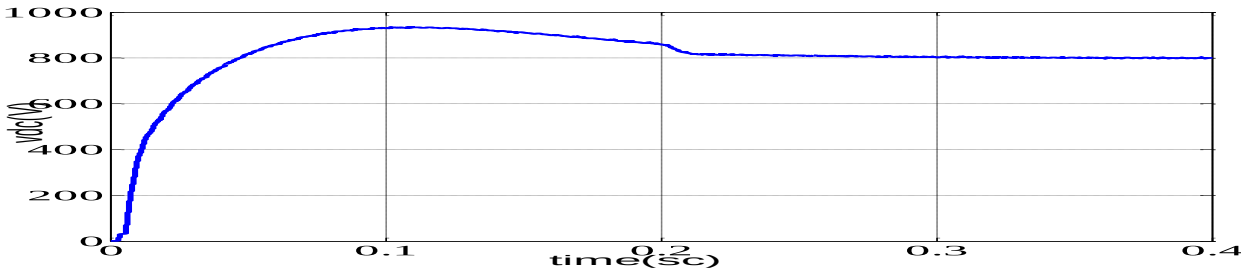


Figure 6.15DC Capacitor voltage using MATLAB/SIMULINK.

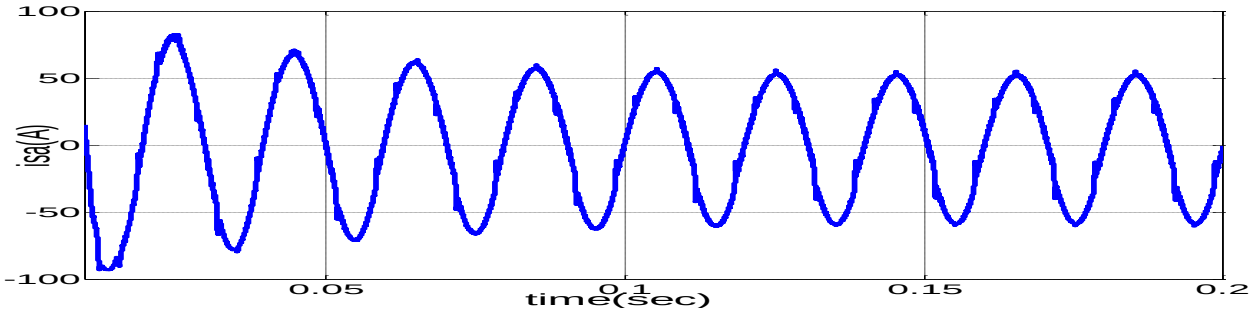


Figure 6.16Source current after Compensation for phase-a using MATLAB/SIMULINK

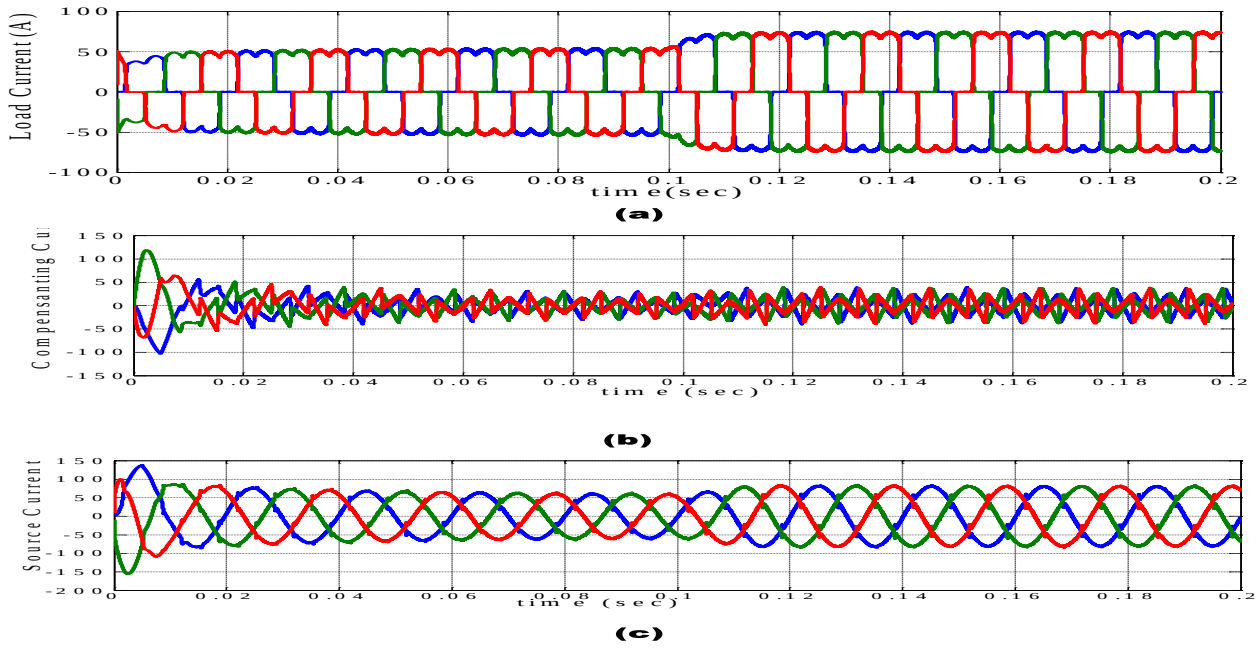


Figure 6.17Simulation results for three-phase active-power-filter under the transient state condition (a) Load currents, (b) Compensation current by APF (c) Source current after APF using MATLAB/SIMULINK.

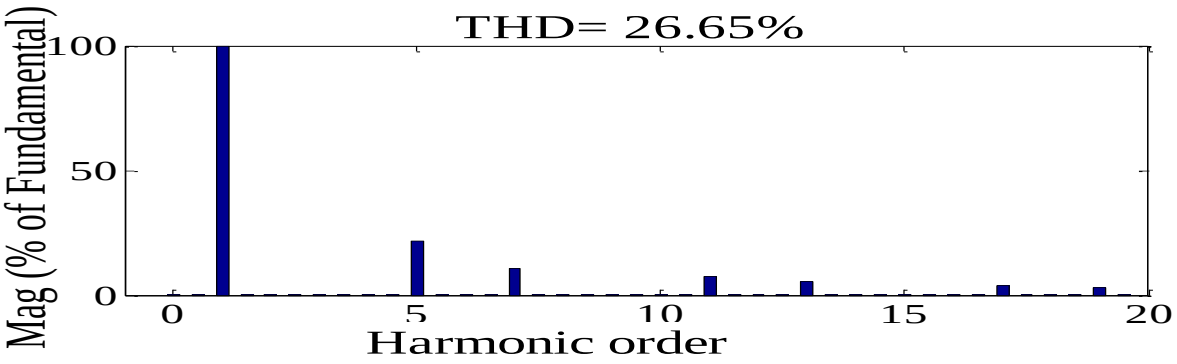


Figure 6.18 Order of harmonics without active power filter (THD=26.65%) using MATLAB/SIMULINK.

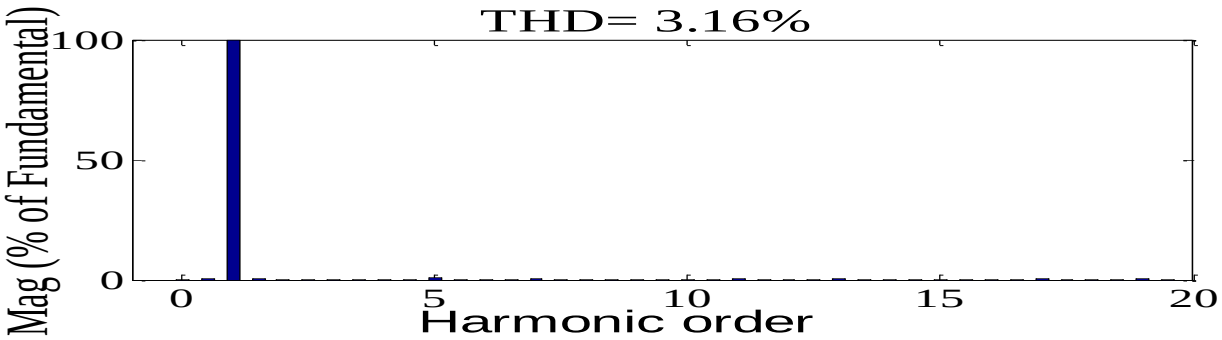


Figure 6.19 Order of harmonics with active power filter using HCC (THD=3.16%) using MATLAB/SIMULINK.

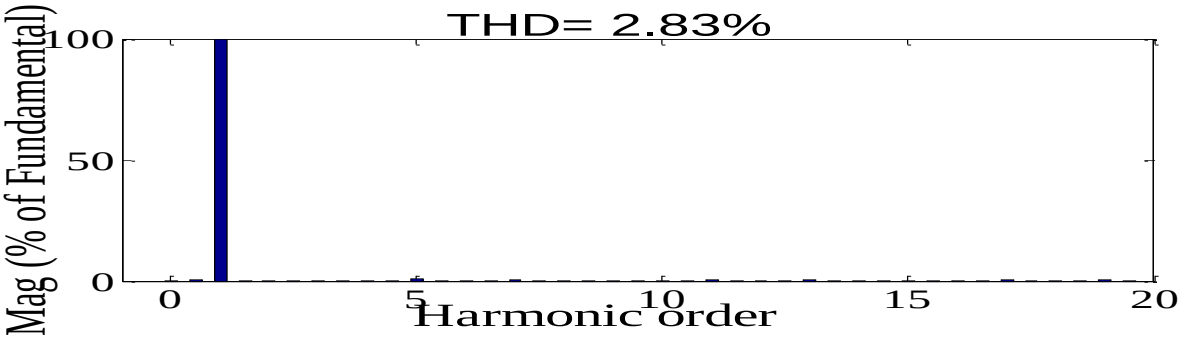


Figure 6.20 Order of harmonics with active power filter using AHCC (THD=2.83%) using MATLAB/SIMULINK.

The regulator and HCC block or modules have been implemented on Xilinx FPGA virtex 2 XC2V250 (spatran-3E) using XST synthesis tool. Table 1 and Table.2 represents the system parameters of APF with Non linear load and design utilization summary.[28-32]

Table 6.1 Parameters used in the system

Line Voltage	440 V
Supply Frequency	50 Hz
Source Impedance:(Resistance Rs, Inductance Ls)	1 Ω,0.1mH
Non-Linear load under steady state:(Resistance Rs, inductance Ls)	10 Ω,100mH
Filter Impedance:(Resistance Rs, inductance Ls)	1 Ω,2.5mH
Dc side capacitance	1400 µF
Reference Dc Voltage	800 V
Power converter	6 MOSFET/DIODE

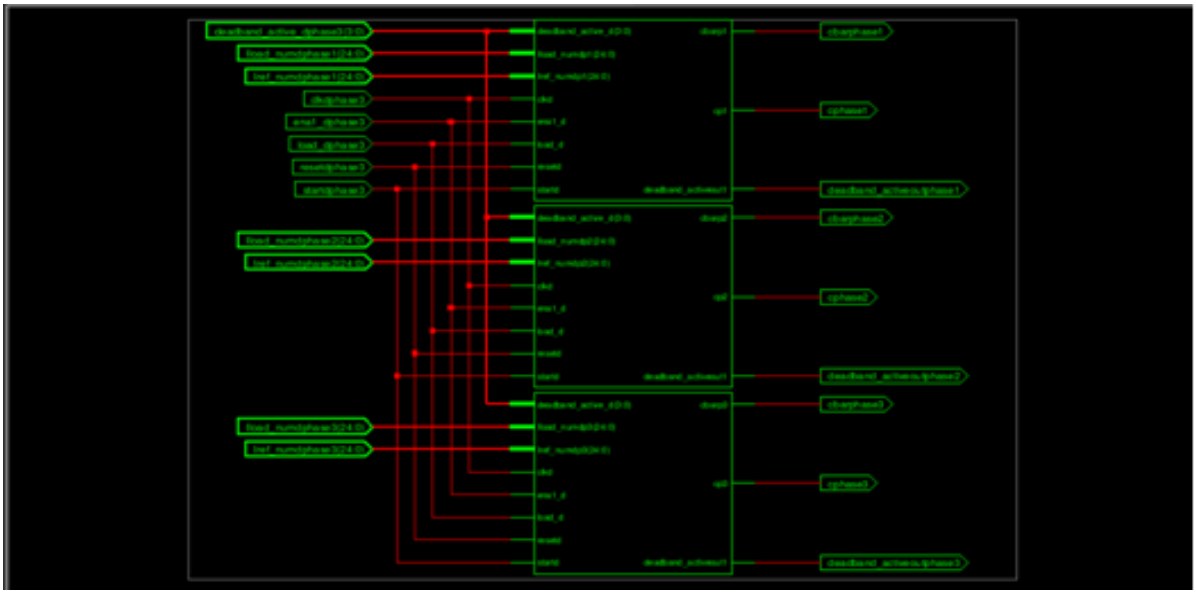


Figure 6.21 RTL of top module for three phase APF using XILINX.

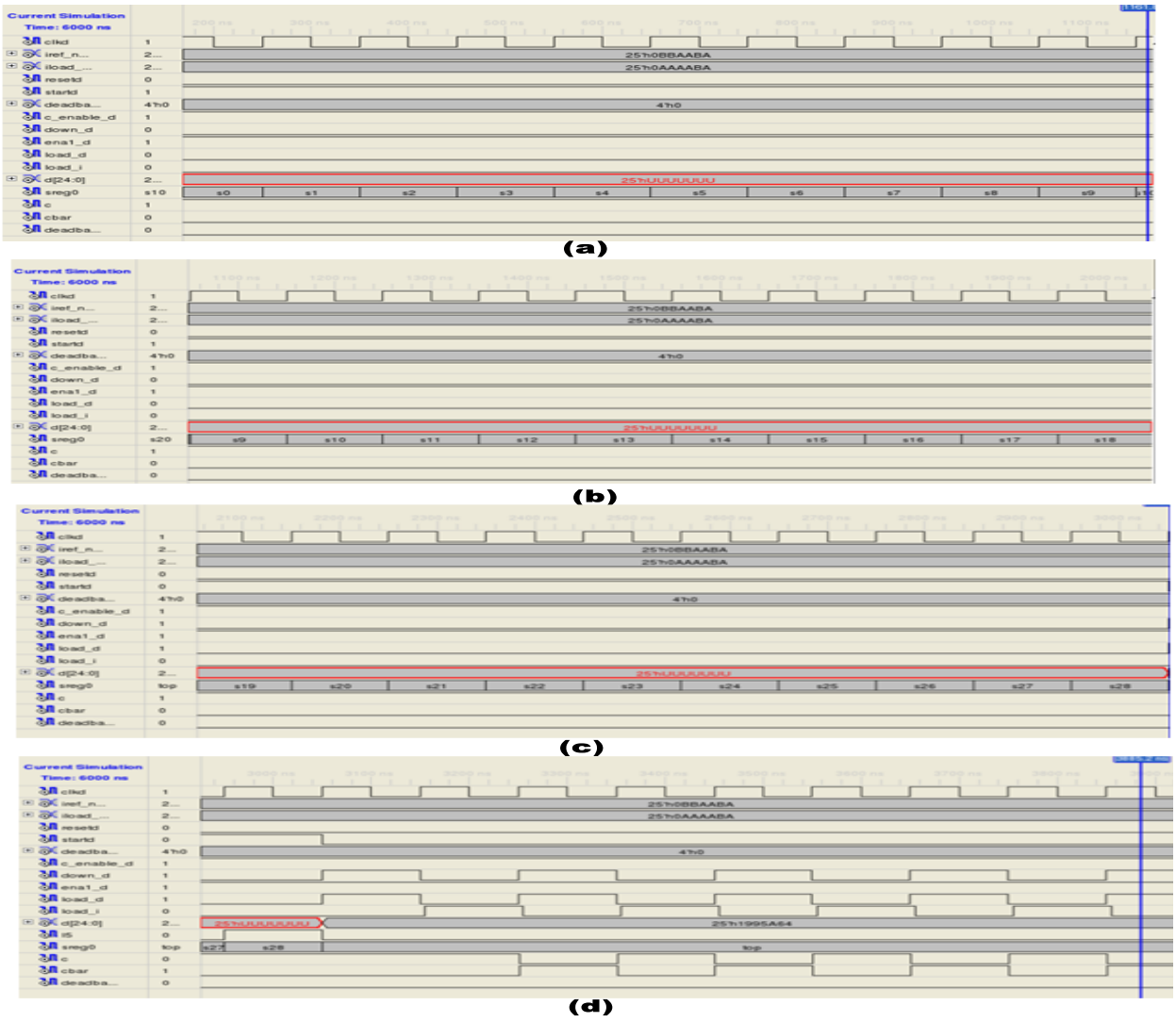


Figure 6.22Simulation results for switching pulse generation (a) state 0 to 8, (b) state 9 to 18, (c) state 19 to 28, (d) c and c' switching pulses obtained after state 28 using XILINX.

In the Figure 6.1.the values of I_{ref_num} and I_{load_num} are loaded to corresponding memory location previous to state-1, which is written in the VHDL code. The values are loaded to ALU and the operator is selected by the FSM according to the DFG in Figure 5.3. To perform the various operations in the DFG several states are needed for loading values to ALU, to calculate result and again to store it in the RAM. This will take 28 states and at state 28 the error value that is calculated which is loaded to comparator when the $I_{inj_en}$is high. The calculation of error I_{inj_num} will take 29 states from S0 to S28 as shown in Figure 6.13 (a-c).The comparator along with the

help of a up/down counter(decides the hysteresis band) gives the switching pulses C and C' by comparing the error signal (I_{inj_num}) and the band as shown in Figure 5.2.

During the period t=0 to t=0.1 sec R, L parameter of the nonlinear load are 20 Ω and 200 mH respectively. From t=0.1 to 0.2 sec the load parameters are changed to 10 Ω and 100 mH respectively. The corresponding waveforms obtained are shown in the Figure. The load current waveform is shown in Figure 6.3. The APF supplies the compensating current that is shown in Figure 6.7.The source current after compensation is presented in Figure 6.8 and Figure 6.12 that indicates the current becomes sinusoidal.

Total Harmonic distortion (THD) is measured for the source current with digital controller using SIMULINK. The THD of the source current with APF as shown in Figure 6.11 and Figure 6.14 is 2.82. This satisfies the IEEE standards.The digital controller's vhdl code written in xilinx is dumped to FPGA for hardware implementation and the gate pulses for phase A is shown in the Figure 6.15 (a-b).Similarly the pulses for phase B and phase C are obtained.

Table 6.2 Device utilization summary

Logic utilization	**Used**	**Available**	**Utilization**
Number of slices	273	4676	5%
Number of slice flip flops	206	9312	2%
Number of 4 input LUTs	504	9312	5%
Number of bonded IOBs	63	190	33%

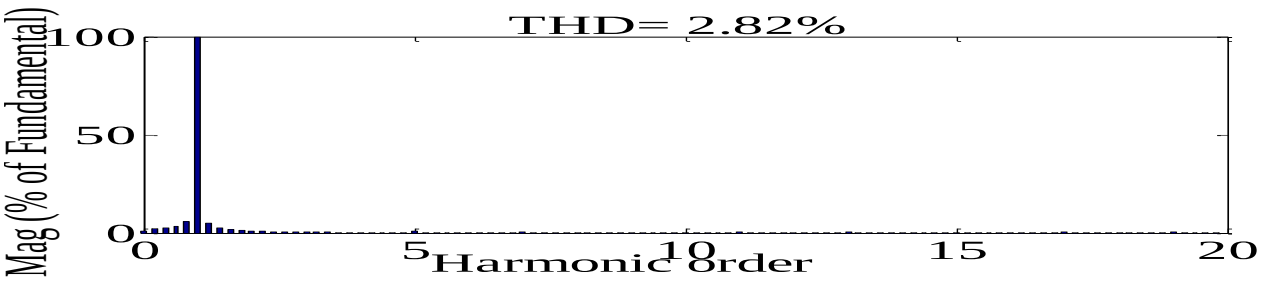
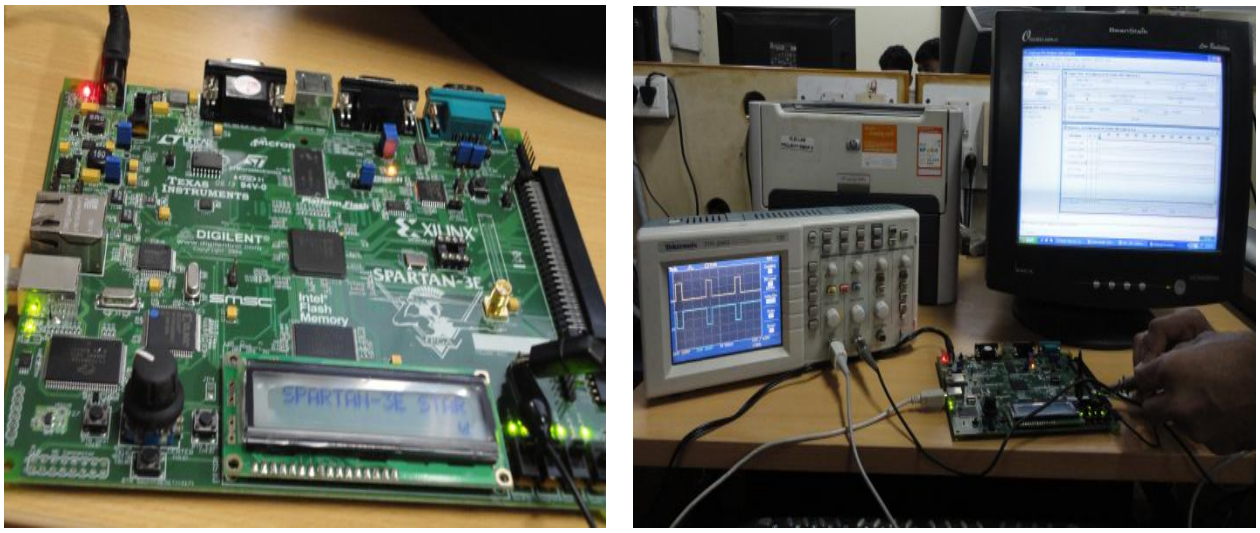


Figure 6.23 Order of harmonics of the source current with digital controller using MATLAB/SIMULINK.



(a) (b)

Figure 6.24 (a), (b) Gate pulses generated using FPGA as digital controller.

Chapter 7

CONCLUSION AND SCOPE FOR THE FUTURE WORK

CONCLUSION

This paper presents design and implementation of a three level hysteresis current control scheme for three-phase four-wire active power line conditioners. The three-level hysteresis controller reduces the variation of the switching frequency and it indicates improved performance compared to 2-level HCC. This active power filter system is tested and verified using MATLAB program. An adaptive hysteresis current controller is implemented for three phase shunt active power filter. The synchronous reference frame controller is used to extract the reference current from the distorted line current. This facilitates to improve the power quality parameters such as reactive power and harmonics due to nonlinear load. The obtained results indicate that DC-capacitor voltage and the harmonic current control can be adapted easily under non-linear load conditions. The performance of the adaptive hysteresis current controller and fixed hysteresis current controlled shunt active power filter is verified with the simulation results. These current controllers compare the transient response and steady state performance in various conditions.

A Digital Controller is implemented for three phase shunt active power filter. The synchronous reference frame controller is used to extract the reference currents from the distorted line currents. This facilitates to improve the power quality parameters such as reactive power and harmonics due to nonlinear load. The digitalcontroller (FSMD+HCC) is implemented in FPGA platform by using chip-scope pro analyzer and is imported to FPGA for hardware implementation. The results are verified using chip-scope pro analyzer and by writing the test bench code for the controller in VHDL and then in SIMULINK environment. This gives couples of advantages compare to the traditional controller. The THD of the source current after compensation is 2.82% which is less than 5%, the harmonic limit imposed by the IEEE-519 & IEC-6000-3 standard.

SCOPE FOR THE FUTURE WORK

Experimental investigations can be done on shunt active power filter by developing a prototype model in the laboratory to verify the simulation results for both Conventional and Digital controllers.

REFERENCES

[1] D.M. Brod and D.W. Novotny, "Current Control of VSI PWM Inverters", *IEEE Trans. Ind.Applic,* Vol. IA-21,no.4.pp.562-570,1985.

[2] M.takeda et al,"Harmonic Current Compensation With Active Filter", *in IEEEIIAS Ann. Meeting,*1987,pp,808.

[3] Joseph S.Subjak,J.S.Mequilkin,"Harmonics- Causes, Effects, Measurements, and Analysis: An Update" *IEEE Trans on Industry Appl,* Vol.26, No.6, pp.1034-1042, 1990.

[4] W.M.Grady, M.J.Samotyj, A.H.Noyola "Survey of Active Power Line Conditioning Methodologies*" IEEE Trans on Power Delivery,* Vol.5, No.3, pp.1536-1542, 1990 .

[5] R.D.Henderson,P.J.Rose,"Harmonics Effects on Power Quality and Transformers",*IEEE Trans. Industrial Applications,*pp 528-532,1994.

[6] Marian.P.Kaunierkowski,MaciejA.Dzieniakowslu"Review of Current Regulation Techniques For Three-phase PWM Inverters"*Conference on IECON*'94, Vol.1, pp.567 – 575,1994.

[7] H.Akagi,"Trends in Active PowerlineConditioner",*IEEE Trans. On power electronics,*vol.9.no.3.may 1994.

[8] J.C.Wu,H.L.Jou,"A Simplified Control Method for Single Phase Active Power Filter",*Proc.Inst.Elect.Engg.Electrical Power Applications,*pp.219-224,1996.

[9] B.Singh,K.AL-Haddad,AChandrs," A Review of Active Filters for Power Quality Improvements" *IEEE Trans on Industrial Electronics,* Vol.46, No.5, pp.960-970, October 1999.

[10] F.Barrero,S.Marinez,F.Yeves,P.M.Martinez,"Active Power Filters for Power Line Conditioning:A Critical Evaluation",*IEEE Trans. On Power delivery,*vol.15,no.1,pp.319-325,2000.

[11] H.L.Jou,J,C,Wu,Y.J.Chang,Y.T.Feng,"A Novel Acitve power Filter for Harmonic Supression",IEEE Trans. On Power delivery,vol.20.no.2,april 2005.

[12] S.Rahmani,K.AL-Haddad,F.Fnarech,"A Three Phase Shunt Active Power FiltersforDamping of Harmonic Propagation in Power Distribution Networks",*Proc. IEEE ISIE,*vol.3,pp.1760-1764,july 2006.

[13] Charles.s,G.Bhubaneswari,"Comparisons of Three Phase Shunt Active Power Filter Algorithms",IJCE,vol.2,no.1,February 2010.

[14] S.Rahmani,N.Mendalek,K.Al-Haddad,"Experimental Design of a Non-linear Control Technique for Three Phase Shunt Active Power Filter",*IEEE Trans. on Industrial Electronics,* Vol.57, No.10, October 2010.

[15] Bhhattacharya,M,Divan,B.Benerjee,"Synchronous Reference Frame Harmonic Isolator using Series Active Power Filter",*4thEuropean Power Electronic Conference.Florence,*vol.3,pp.30-35,1991.

[16] Prasad N. Enjeti, W.Shireen, P.Packebush and Ira J. Pitel "Analysis and Design of a New Active Power Filter to Cancel Neutral Current Harmonics in Three-phase Four-Wire Electric Distribution Systems",*IEEE Trans. on Industry appl*.Vol.30, No.6, Nov/Dec-1994.

[17] M.Isabel,M.Montero,E.R.Cadaval,F.B.Gonzalez "Comparison of Control Strategies for Shunt Active Power Filters in Three-Phase Four-Wire Systems*" IEEE Trans. on Power Elects,* Vol. 22,No.1,2007.

[18] O.Vodyakho.T.Kim,"Shunt active filter based on three-level inverter for 3-phase four-wire systems",*IET Power Electronics,*Vol.2,No.3, pp. 216–226, 2006.

[19] W.Diyun,C.Yanbo,K.W.Cheng,"Design and Performance of a Shunt Active Power Filter for Three-Phase Four-Wire Systems",IEEE Conf. ICPESA 2009.

[20] P.Salmer,S.P.Litran,"A Control Statergy for Hybrid Power Filter to Compensate Four Wire Three Phase Systems", IEEE Trans. on Power Elects, Vol. 25,No.7,july 2010.

[21] B.K.Bose,"An Adaptive Hysteresis Band Current Control Technique of a Voltage Feed PWM Inverter for Machine Drive Systems", IEEE Trans.Ind Electron.pp.402-406,1990.

[22] L.A.Moran et al,"A Three Phase Active Power Filter Operating With Fixed Switching Frequency for Reactive Power and Current Harmonic Compensation", IEEE Trans.on Indus.Elect.vol.42,pp 402-408,1995.

[23] G.H. Bode and D.G. Holmes,"Implementation of Three Level Hysteresis Current Control for a Single Phase Voltage Source Inverter*", IEEE-Conf.*pp.7803-5692, 2000.

[24] B.J.Kang,C.M.Liaw,"Random Hysteresis PWM Inverter withRobust Spectrum Shaping",*IEEETrans.Aerospace and Electronics Systems,*vol.37,pp.619-628,april 2001.

[25] J.Zeng,Chang.Yu et al,"A Novel Hysteresis Current Control for Active Power Filter with Constant Frequency",*Electrical Power Systems Reasearch* 68,pp.75-82.

[26] M.Kale,E.Ozdemir,"An Adaptive Hysteresis band Current Controller for Shunt Active Power Filter",*Electrical Power Systems Reasearch* 74,pp.113-119,2005.

[27] N.Belhaouchet,L.Rahamani,"Development of Adaptive Hysteresis band Current Control of PWM Three Phase AC Chopper withConstant Switching Frequency",*Electric Power Component and Systems,*vol.33,no.10,pp.583-598,2009.

[28] S.Gautam,R.Gupta,"Three Level Inverter based Shunt Active Power Filter using Generalized Hysteresis Current Control Method",*IEEEConf.*october 2010.

[29] B.O.Slim et al ,"Hardware Design and Implementation of digital Controller for Parallel Active Power Filters",*IEEEConf.*october 2006.

[30] J.Acosta et al,"FPGA based Control Scheme for Active Power Filter",*IEEE Conf.*2006.

[31] Y.F.Chan et al,"Design and Implementation of Modular FPGA-based PID Controllers", *IEEE Trans.on Indus.* Elect.vol.54, no.4, 2007.

[32] P.Thirumoorthi et al,"Digital Control of Active Power Line Conditioner based on Instantanious Reactive Power Theory",*IEEEConf.ICCACEC,*june 2009.

PUBLICATIONS

[1] **Saswat Kumar Ram**,KauppananP,**K.K.Mahapatra**"Three Level Hysteresis Current Controller Based Active Power Filter For Harmonic Compensation" **IEEE Conf**, ICETECT, pp.407-412,MARCH 2011.

[2] **Saswat Kumar Ram**,S.R.Prusty,**K.K.Mahapatra**,B.D.Subudhi"Performance Analysis of Adaptive Band Hysteresis Current Controller for Shunt Active Power Filter" **IEEE Conf**, ICETECT, pp.425-429,MARCH 2011.

[3] **Saswat Kumar Ram**, S.R.Prusty, P.K.Barik,**K.K.Mahapatra**,B.D.Subudhi"FPGA Implementation of Digital Controller for Active Power Line Conditioner using SRF Theory" **IEEE Conf**, EEEIC 2011.

APPENDIX-A

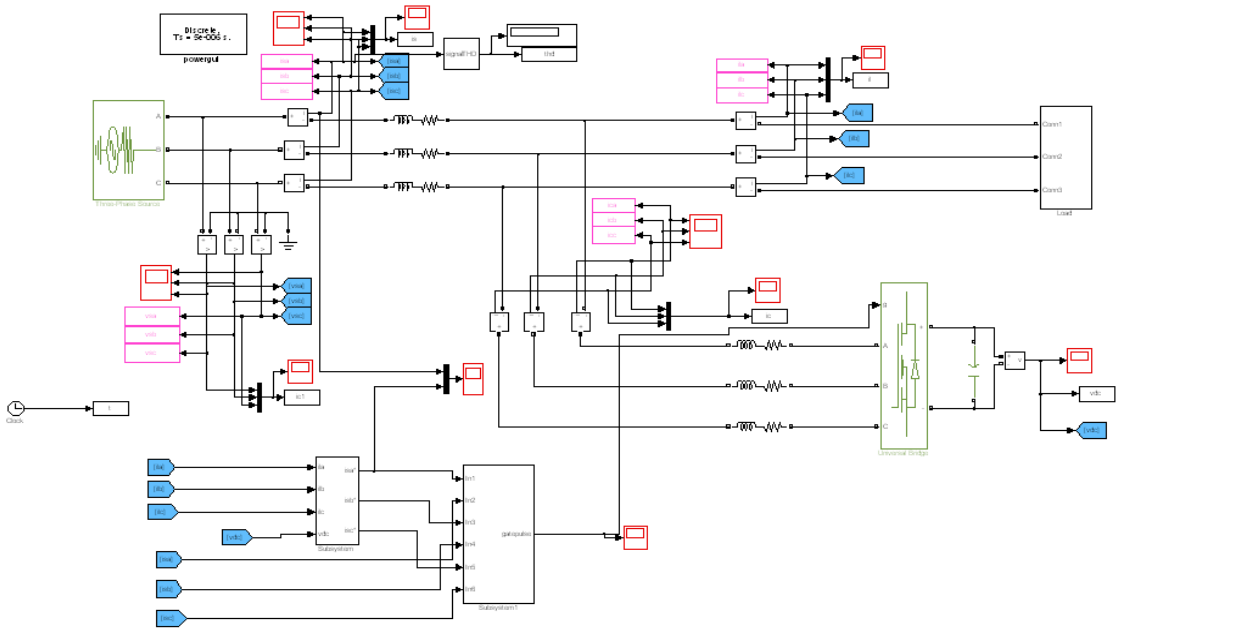


Figure 1 MATLAB SIMULINK Modelfor Shunt Active Power Filter with HCC Simulation Study.

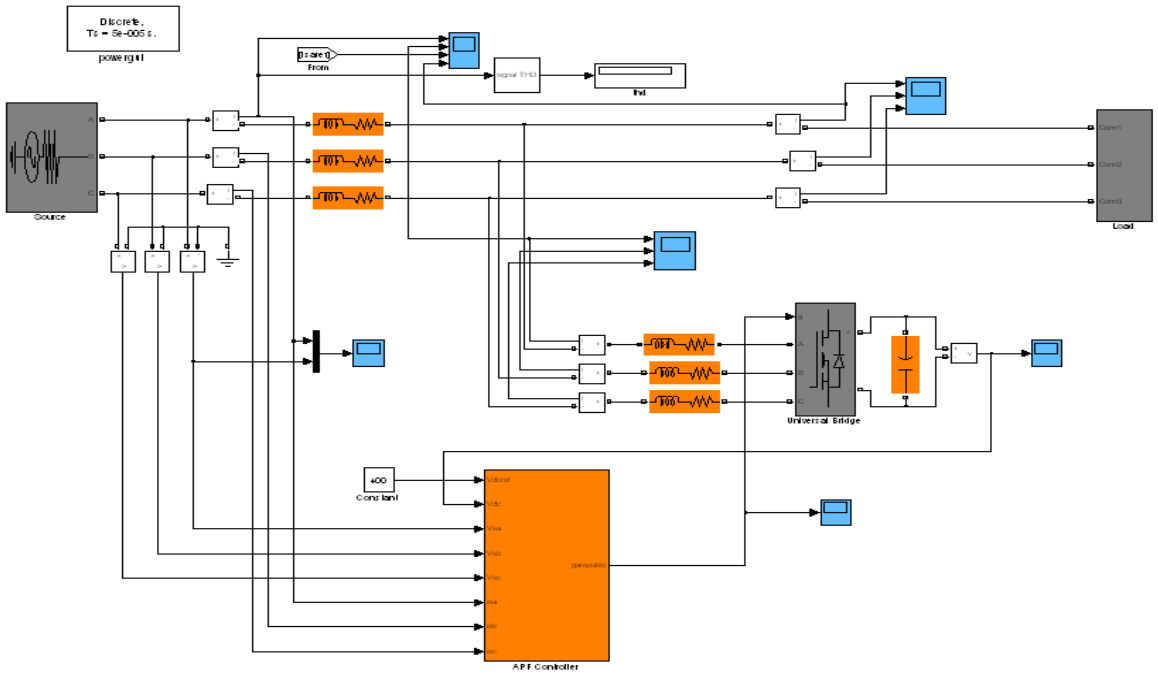


Figure 2 MATLAB SIMULINK Modelfor Shunt Active Power Filter with AHCC Simulation Study.