DIGITAL IMAGE WATERMARKING BASED ON FPGA

AND SPINTRONIC LOGIC AND STUDY OF SOME

ASPECTS OF SPINTRONIC LOGIC BASED CIRCUITS

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Certificate of Approval

This is to certify that the thesis entitled **DIGITAL IMAGE WATERMARKING BASED ON FPGA AND SPINTRONIC LOGIC AND STUDY OF SOME ASPECTS OF SPINTRONIC LOGIC BASED CIRCUITS** submitted by **Ashish Kumar Pandey , Vivek Mirdha and Siddharth Sankar Hembram** has been carried out under my supervision in partial fulfillment of the requirements for the Degree of ***Bachelor of Technology (B.Tech.)*** in ***Electrical Engineering*** at National Institute Of Technology Rourkela and this work has not been submitted elsewhere for any other academic degree/diploma to the best of my knowledge.

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ABSTRACT

The growth of high speed computer networks and that of Internet, in particular has explored means of new business , scientific , entertainment and social opportunities .Digital media offer several advantages over analog media like high quality ,easy editing ,high fidelity copying . There are enormous chances of duplicating and distribution of digital information which has led to the need for effective copyright protection tools . DIGITAL WATERMARKING is a kind of protection tool in which a data is hidden in an image ,audio file or video file .Watermarking is either "visible" or "invisible" . Albeit visible or invisible are visual terms watermarking is not limited to images , it can also be used to protect other types of multimedia object . This project work is on Spatial Domain Image Watermarking using FPGA and Spintronic logic and applications of single spin logic where the spin of electron is used in addition to its charge .For the application of spintronics MAGNETIC TUNNEL JUNCTIONS (MTJ) are used as a spintronic device and different logic and ALU operations are performed and are compared with the conventional electronic devices based operation . The spintronic devices have lots of advantages over the conventional devices like they are non-volatile ,they consume less power ,timing and area.

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1.INTRODUCTION TO WATERMARKING

The last decade has witnessed the rapid development in information technologies and the wide availability of digital consumer device such as digital cameras ,scanners etc .But at the same time this leads to the hacking vulnerability and duplicity of the original information.

The most modern solution technique to this problem is digital watermarking scheme .Digital watermarking algorithms could be considered as digital communication scheme where auxiliary message is embedded in digital multimedia signal and are available where ever the later signals move.

Watermarking is also a type of information hiding where secret codes are embedded in the hidden form inside an image file ,audio file or video file .Watermarking is a relatively new and unexplored field in which extensive research is going on all over the world and it has the potential to provide simple and easily implementable solution to provide rightful ownership.

1.1.HISTORY OF INFORMATION HIDING

The idea of communicating secretly is as old as communicating itself. Steganographic methods made a record debut a few centuries later[ref].

The origin of steganography is considered biological and physiological .A whole branch of steganography ,"linguistic steganography" , consists of linguistic or language forms of hidden writing .A semagram is a secret message that is not in a written form.

Watermarking technique has evolved from steganography .The use of watermark is almost as old as paper manufacturing.

- **STEGANOGRAPHY**:Steganograph is the art/science/study/work of communicating in a way which hides the secret message in the main information.
- **STEGANOGRAPHY vs DIGITAL WATERMARKING** :They primarily differ by intent of use . A watermark can be perceived as an attribute of the carrier . It may contain information such as copyright ,license ,tracking and authorship etc .Whereas in case of steganography , the embedded message may have nothing to do with the cover .In steganography an issue of concern is bandwidth for the hidden message whereas robustness is of more concern with watermarking.

1.2. CONCEPT OF WATERMARKING

Over the past few years ,several watermarking algorithms have been introduced and their software is accessible ,however recently some hardware realizations are being offered in the literature .Software implementations are easy to use, have upgradability and flexibility but it has limited speed problem and vulnerability to the offline attack.

Despite of that hardware implementation offer less area , low execution time and low power .Therefore , watermarking inside digital devices cannot assure the tamper proof . Hence for hardware implementation spatial domain is always preferred.

Spatial domain data embedding scheme and its hardware implementation in semi gate array ASIC(Application Specific Integrated Circuit) -VLSI(Very Large Scale on Integration) as well as using spin based logic.

The quality of transmitted is also comparable to that of the implemented by the software .This reliability is further enhanced by using private key coding scheme.

The contribution to the experimental literature should include

1. Reproducible results and descriptions.
2. An account of the key understanding or insight behind the contribution.
3. Supporting evidence.

   These motivate us to realize hardware of watermarking authentication and its VLSI architecture with the help of FPGA.

1.3. MODEL OF WATERMARKING SCHEME

Copyright information is hidden inside the original piece in an encrypted form which is inside the Watermark Insertion Block.

Watermark(W) to be embedded inside original image(I) using the secret key(K).The final image I_w contains the encrypted logo which is vulnerable to external attack and duplication.

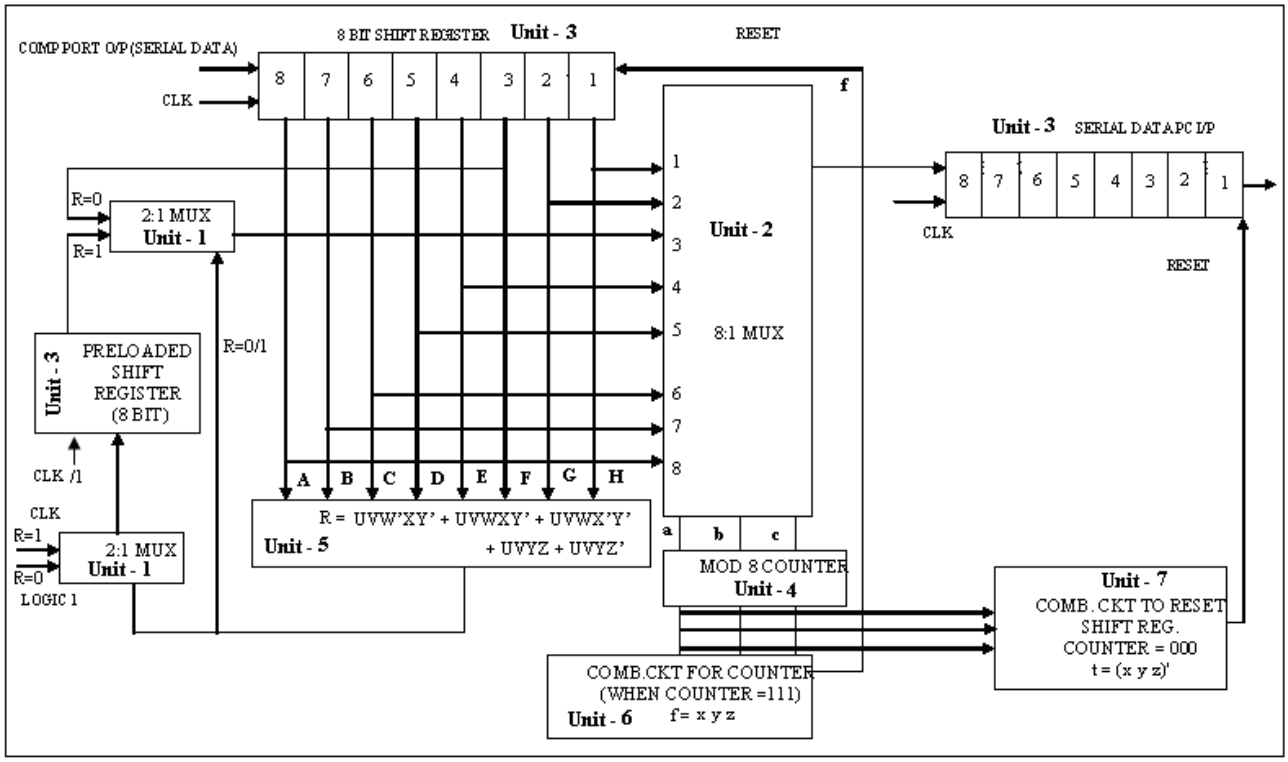
The encrypted watermark is extracted (<W>) using Watermarking Extraction Block .The better the watermarking system the more the <W> resembles W.

1.4. WATERMARKING EMBEDDING AND DETECTION

The algorithm for the scheme is a kind of digital modulation scheme which uses synchronous detection for decoding of the information .Using LSB modulation method , a gray scale stego image called as modulated signal is produced in which buffer block is transforming 2-D pixel values to 1-D and unbuffer block for transforming 1-D pixel values to 2-D pixel values .At last ,the message is extracted at the receiver from the modulated signal using synchronous detection where the same buffer and unbuffer blocks are used for the very purpose.

2.ALGORITHM FOR HARDWARE REALIZATION

ENCODER



The watermarking encoder

The watermarking encoder sets in the binary string into the grayscale host image . A shift register is used in the process .

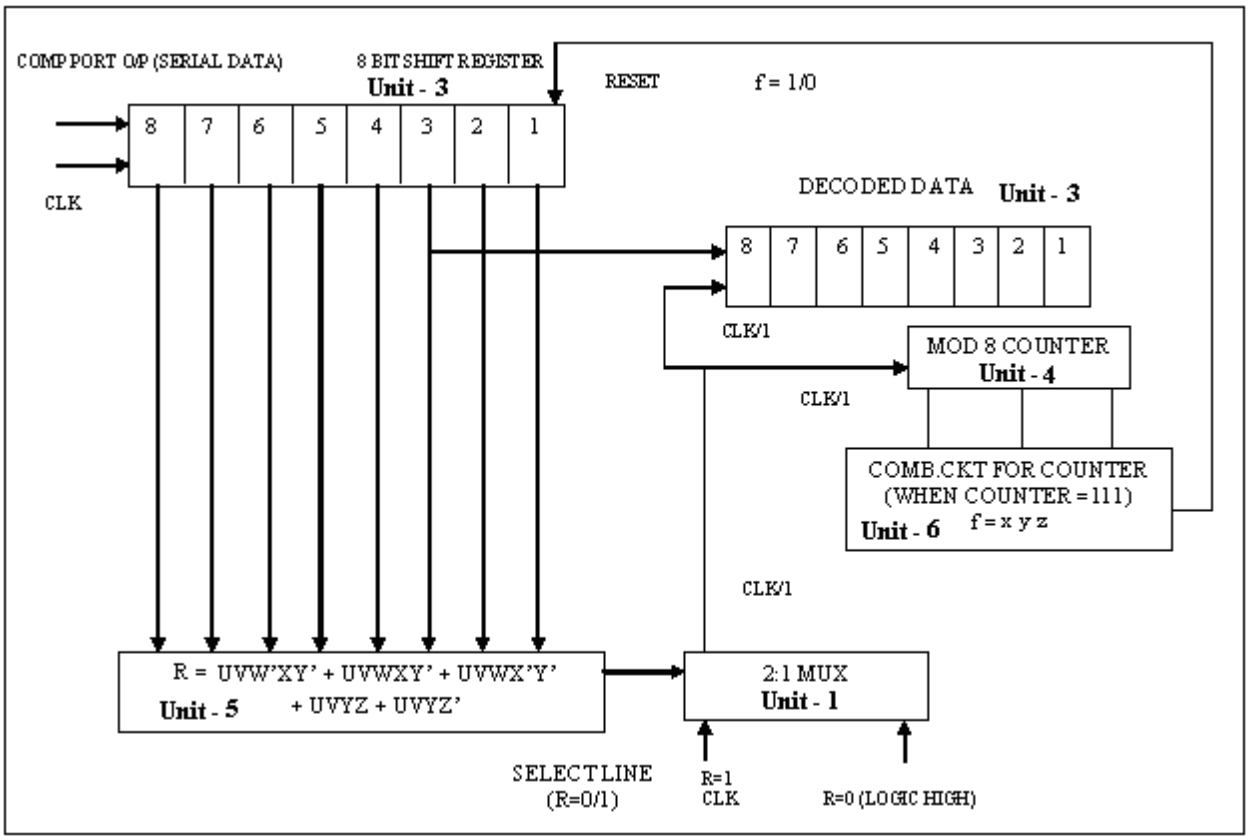
The output of the combinational circuit block

$$f(U,V,W,X,Y,Z) = (UVW'XY') + (UVWXY') + (UVWX'Y') + (UVYZ) + (UVYZ')$$

gives a selection input to a 2:1 MUX so that the output of MUX result in a clock.

Using preloaded shift register ,8:1 MUX and counter , the input signal is encoded into the image in an encrypted form.

DECODER



The watermarking decoder

The decoding operation is exactly the reverse to that of the encoding .The stego image is projected into the 8-bit shift register .The same combinational circuit used in the decoding process. With the use of multiplexer the hidden watermark in it in the 3rd bit plane is selected and projected into the output shift register .Then the mod8 counter facilitates to count the total number of counts is equal to the length of watermark , the decoding operation is stopped.

3.FIELD-PROGRAMMABLE GATE ARRAY

A **Field – programmable Gate Array** (**FPGA**) an "integrated circuit designed to be configured by the customer or designer after manufacturing—hence "field-programmable" . The FPGA configuration is generally specified using a hardware descriptilanguage(HDL),similar to that used for an application specific integrated circuit(ASIC) were previously used to specify the configuration ,as they were for ASICs, but this is increasingly rare. FPGAs can be used to implement any logical functions that an ASIC could perform . The ability to update the functionality after shippings , partial re - configuration of the portion of the design and the low non-recurring engineering costs relative to an ASIC design (notwithstanding the generally higher unit cost), offer advantages for many applications.

FPGAs contain programmable logic components called "logic blocks" , and a hierarchy of reconfigurable interconnects that allow the blocks to be "wired together" somewhat like many logic gates that can be inter-wired in different configurations"[20]. Logic blocks can be configured to perform complex combinational functions , or merely simple logic gates like AND and XOR . In most FPGAs , the logic blocks also include memory elements , which may be simple flip-flops or more complete blocks of memory.

4.IMPLEMENTATION USING MATLAB PROGRAMMING

Least Significant Bit Modification

"The most straight-forward method of watermark embedding, would be to embed the watermark into the least-significant-bits of the cover object . Given the extraordinarily high channel capacity of using the entire cover for transmission in this method , a smaller object may be embedded multiple times. Even if most of these are lost due to attacks, a single surviving watermark would be considered a success.

LSB substitution however despite its simplicity brings a host of drawbacks. Although it may survive transformations such as cropping , any addition of noise or lossy compression is likely to defeat the watermark. An even better attack would be to simply set the LSB bits of each pixel to on fully defeating the watermark with negligible impact on the cover object .Furthermore , once the algorithm is discovered, the embedded watermark could be easily modified by an intermediate party.

An improvement on basic LSB substitution would be to use a pseudo-random number generator to determine the pixels to be used for embedding based on a given seed or key . Security of the watermark would be improved as the watermark could no longer be easily viewed by intermediate parties .The algorithm however would still be vulnerable to replacing the LSB's with a constant. Even in locations that were not used for watermarking bits, the impact of the substitution on the cover image would be negligible . LSB modification proves to be a simple and fairly powerful tool for steganography , however lacks the basic robustness that watermarking applications require"[19]

5.RESULT

There are following conclusions on results. Firstly, robustness evaluations were limited to testing against JPEG compression and the addition of random noise . Evaluating each of the algorithms against all attacks across a full range of gain values is well beyond the scope of this report . The other robustness metrics will only be touched on briefly ,should the algorithm prove exceptionally resistant or exceptionally vulnerable to the attack . In general, algorithms were implemented in the most straightforward way, not the most computationally optimal. Furthermore, MATLAB may handle certain programming constructs differently from other languages, thus the best performing algorithm may vary for each language and implementation.

Three different watermarks were used, based on the theoretical and experimental information capacity of the watermarking algorithm, as shown in figures 1 and 2.

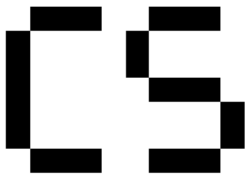


Figure 1 - Small Watermark (12 x 9 pixels)

Figure 2- Normal Watermark (50 x 20 pixels)

Not shown above is the large watermark created for the LSB embedding algorithm , which uses the normal watermark and titles it out to full image size. For our reference image, the ever-popular miss November (Lena) image is used, as shown below in figure 3.

Figure 3 - Lena Reference Image (512 x 512 Pixels)

Results from LSB substitution were as expected. The watermarked image shows little not noticeable degradation , while the large watermark was recovered perfectly.

Least Significant Bit Substitution

Figure 4a - Watermarked Image

Figure 4b - Recovered Watermark

"Although the watermark was recovered perfectly in the ideal case, the addition of any amount of noise, or compression of the image using JPEG fully destroys the embedded watermark, leaving nothing but noise . Even worse , the watermark can be removed with no perceivable change to the watermarked image. The message capacity of LSB embedding however is quite good, a 1:1 correlation with the size of the image"[19].

6.DIGITAL WATERMARKING TECHNIQUE USING SINGLE SPIN LOGIC REALISATION IN SPATIAL DOMAIN

In the current scenario the media is becoming more and more digitized . Almost all the data is now being shared digitally except one or two , this increases the vulnerability of data hacking . To prevent this various techniques of watermarking is used to hide or to copyright the data or image from external misuse.

Albeit these watermarking techniques provide security but they are also not 100 % secure. To increase the robustness of the retrieved data nowadays spin based logics are used that are less expensive, more robust and easy to implement.

As an effort towards the power efficient system , here we present an oblivious, spatial domain watermarking based authentication algorithm and its VLSI/ULSI architecture. It is realized with the help of "spintronics" or "spin based electronics" where classical binary bit '1' and '0' are encoded in orthogonal spin polarization of single electron confined in a quantum dot and placed in magnetic field. The benefit of the spintronic devices is that it needs much less power than conventional technologies whilst operating at much higher speed. As discussed earlier it utilizes the lower bit plane modulation scheme for hiding a binary image within a gray scale image.

Now all the modules of watermarking algorithm are implemented using Single Spin logic along with its computer simulation . It is known that this data embedding technique can perform watermarking much quicker than the software implementation. The quality of transmitted image is analogous to that of implemented by software algorithm.

6.1.INTRODUCTION TO SPINTRONICS

The emerging research field spin-electronics or spintronics aspirated significant current interest after a spin analog of the electronic modulator. Spintronics, also known as the magneto electronics, "is an emerging technology that exploits the intrinsic spin of the electron and its associated magnetic moment, in addition to its fundamental electronic charge, in solid state devices"[18].

Single spin based logic devices encode binary bit '1' and '0' into parallel and anti-parallel spin polarization respectively of "single electron confined in a quantum dot and placed in magnetic field . Electrons are spin-1/2 fermions and therefore constitute a two state system with spin 'up ' and spin 'down'"[18]. The prerequisites of a spintronic device are first "a system that can generate a current of spin-polarized electrons comprising more of one species-up or down-than the other and secondly a separate system sensitive to the polarization of electrons.

Spin polarization in non-magnetic materials can be achieved either through ZEEMAN's effect in large magnetic fields and low temperature or by non-equilibrium methods"[18].

In spintronic devices, logic bits can be switched simply flipping without moving charges. The spin state is communicated between the neighboring devices via the exchange interaction between the nearest , neighbor spins , without any wires. The main benefits of this technique are extremely low dynamic power dissipation during switching , ultra high gate density and relatively fast processing speed . Since the spin is somewhat immune to noise (as it does not easily couple with stray electric fields) therefore they yield practical low power and high density computing capability.

6.2.WATERMARK EMBEDDING AND DETECTION

In watermarking embedding and detection the same old technique of embedding is used i.e. first the code is embedded inside the image with the help of a secret key. When the image is to be retrieved , then with the help of the same key the secret code is detected . The latter technique is known as decoding technique. The scheme that is most commonly used is the LSB modulation scheme.

The watermarking embedding technique converts the 2-D pixel values of the gray image and binary watermark into single integer (SI) data type and then converted into 1-D pixel values . Then the buffer block reallocates these signals to a new frame size and then they are redundantly embedded using a pseudorandom sequence using a private key.

The watermark decoding is just the reverse of this process. Here the 1-D stego image is first unbuffered using the same private key and then these 1-d images are converted back into 2-d pixel values of the gray image and the binary code.

6.3.HARDWARE REALISATION USING SPINTRONIC LOGIC

Nanotechnology have made it possible to realize 'single spin logic' based low dimensional structures, also called nanostructures, provide opportunities to realize high speed, low power consuming devices. As a consequence, the search for the new principle of the small size devices are becoming more and more important . At present there are two main branches of the proposal on the suitable operation principles , so called " quantum electron devices" and "single

electron devices" . Here a spatial domain watermarking encoder and decoder are designed using single spin logic devices.

ENCODER

$$f(U, V, W, X, Y, Z) = UVW'XY' + UVWXY' + UVWX'Y' + UVYZ + UVYZ' \quad (1)$$

The above combinational function is used for the encoding of the binary watermark into a gray image.

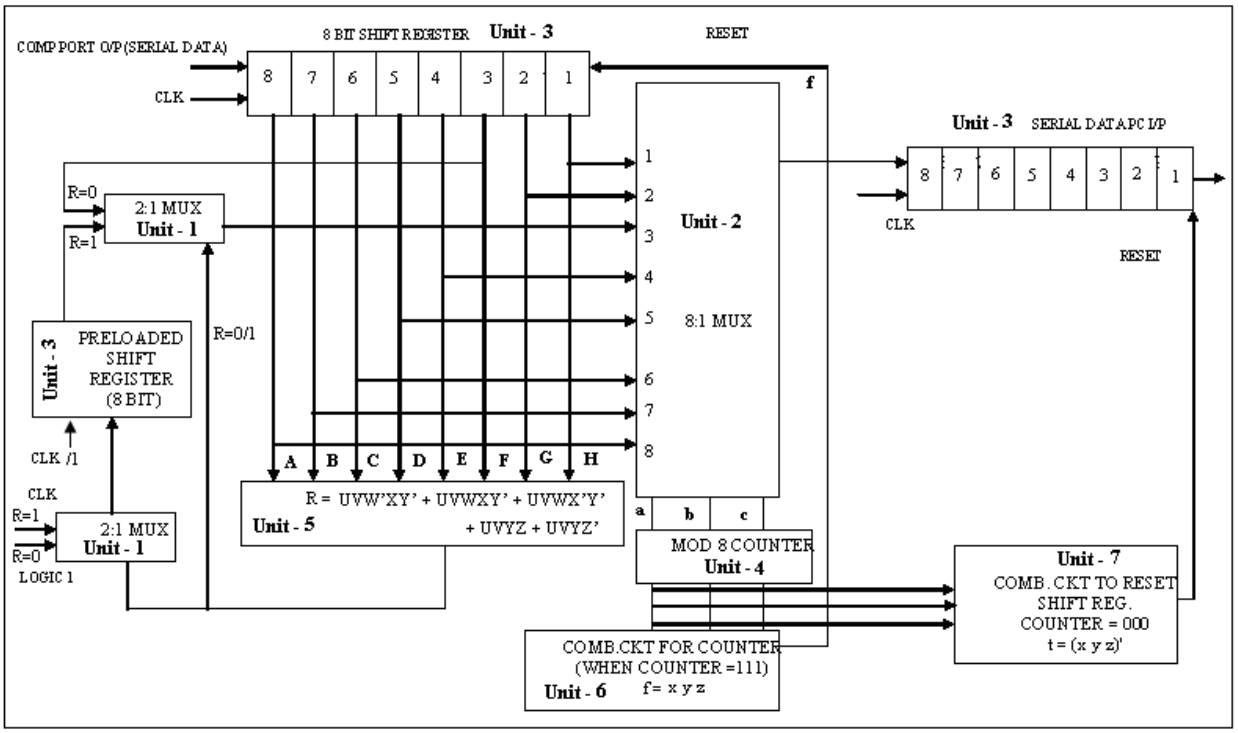


Fig. 1 The watermarking encoder

The output of this combinational block proceeds as a selection input to a multiplexer (2:1) so that this multiplexer output results in a clock (R=1) . This is further forwarded to the preloaded shift register for giving a watermark bit to the input of second multiplexer . Now, depending on the logical result of the combinational function, either multiplexer results in binary bit to replace the third bit plane position of the selected spatial pixel value or the pixel is left unaltered. The 8:1 multiplexer performs this embedding or bit replacement operation. To end

with , the changed / unchanged pixel as a watermarked is loaded into the output shift register . The mod 8 counter along with two combinational circuits calculate the total number of bit replacement operation and reset the shift register.

DECODER

The decoding operation is just the reverse of the encoding operation. The identical combinational circuit as being used in the encoder is engaged to compute the threshold limit and to choose the perceptually significant , appropriate pixels . Here the mod8 computer is used to count the number of decoding operations in the process.

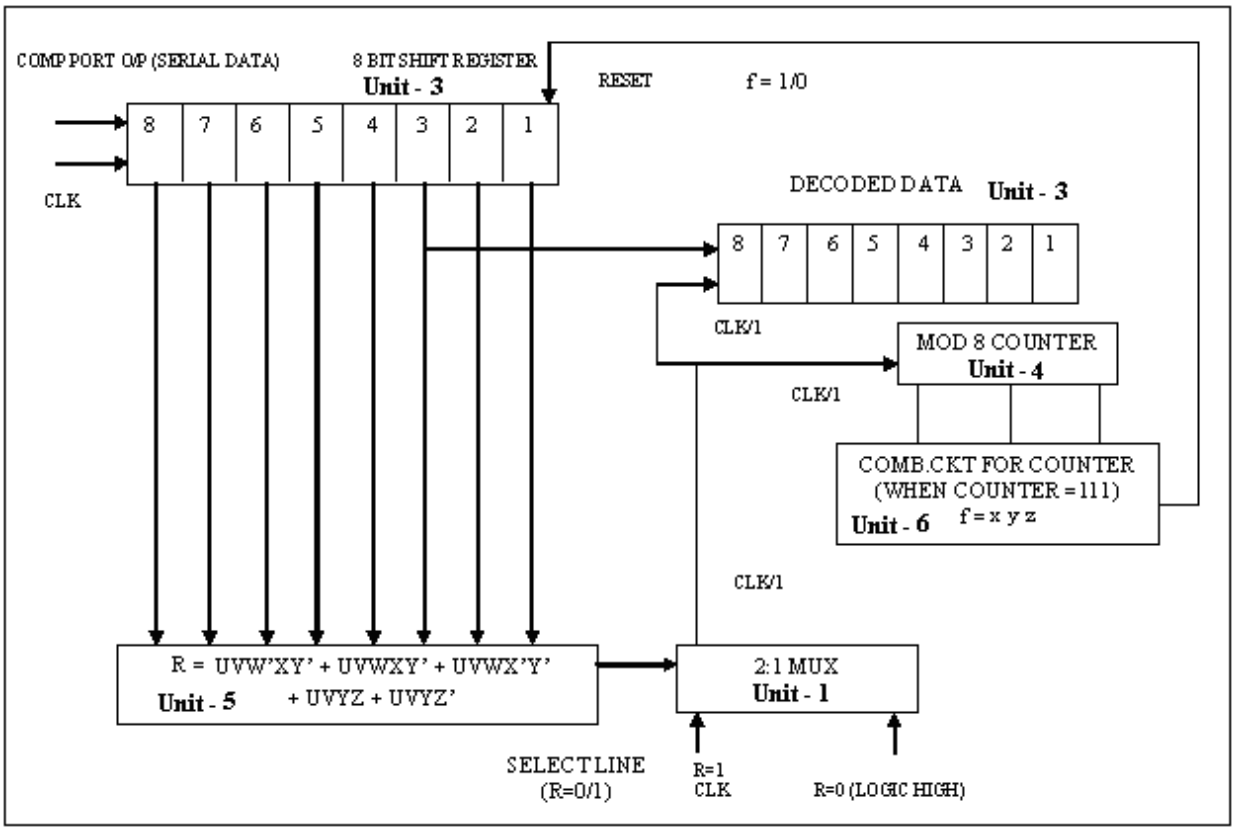


Fig. 2 The watermarking decoder

6.4.OPERATIONAL PRINCIPLE

"An electron can be considered as a small electrically charged sphere that is spinning rapidly. The circulating charges on the sphere amount to tiny loops of electric current, which create a magnetic field similar to the earth's magnetic field. Immersing the spinning sphere in an external magnetic field changes its total energy according to how its spin vector is aligned with the field"[17]. Each of these circle represents a spin polarized single electron confined in a quantum dot which is placed in a global magnetic field . In the present work we have designed a spatial domain data embedding scheme and its hardware implementation using spin based logic circuits by two-dimensional array of spin-polarized electrons (cells). SPSTM tip heads are to be used for providing inputs and getting output from this ultra small chip .Binary information is encoded by spin orientation of electron dots. The nearest neighbor dots overlap in space causing exchange coupling between them . A week global magnetic field is applied externally , thereby making the polarization in each dot either parallel or anti parallel to the global field which encode the binary bit 1 and 0, respectively.

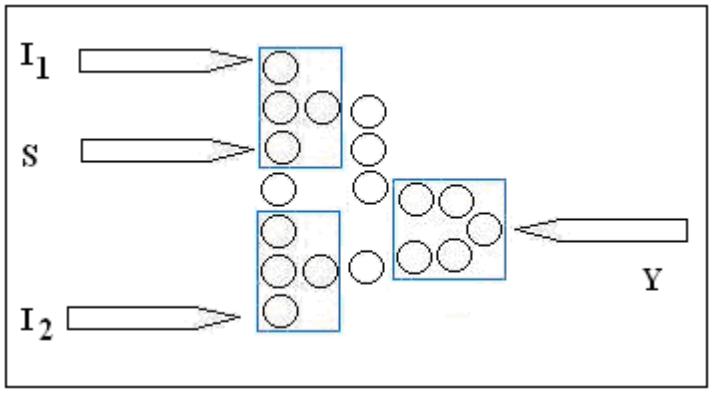
6.5.EXPLANATION OF SPIN VALUE OPERATION

A. Unit 1 (2 x 1 Multiplexer)

This unit is implemented for performing the multiplexing operation in order to generate the variable clocking / signaling prescribed for the realization of the system.

$$Y = SI_1 + SI_2 \qquad (2)$$

This logical operation is efficiently performed by the spin architecture depicted below in the figure.



B. *Unit 2 (8 x 1 Multiplexer)*

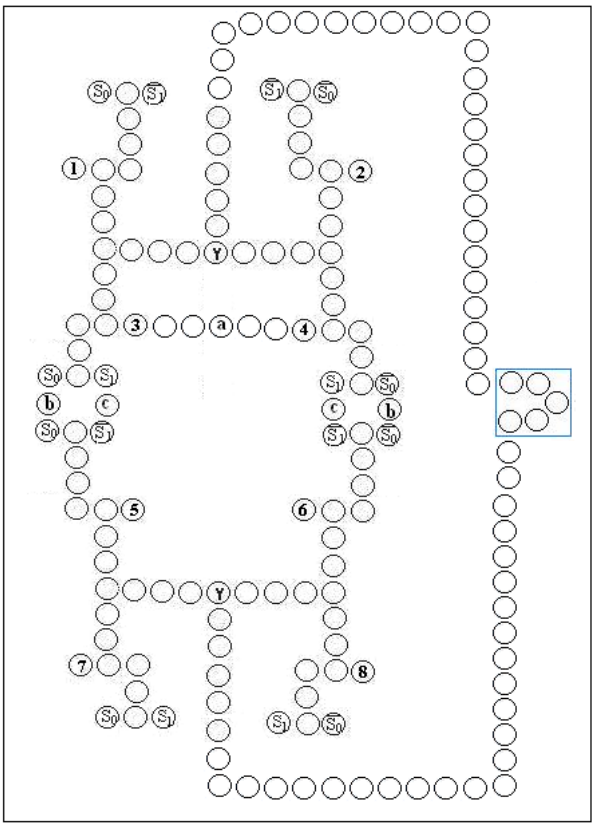
This unit is employed for performing the watermark encoding operation by selecting the proper bit plane in order to generate the watermarked signal prescribed for the realization of the system.

$$Y = S_0 S_1 I_0 + S_0 S_1 I_1 + S_0 S_1 I_2 + S_0 S_1 I_3 \quad (3)$$

This can also be written as

$$Y = ((S_0' S_1' I_0)'.(S_0 S_1' I_1)'.(S_0 S_1 I_2)'.(S_0 S_1 I_3)')' \quad (4)$$

The De Morgan's rule is applied here to convert the logical operation into blocks of AND gate. This logical operation is efficiently performed and depicted in the figure below.



C. *Unit 3(8 bit Shift Register)*

This unit imports the spatial pixel values into the subsequent encoder / decoder circuits as well as exports or loads output watermarked signal pixels or decoded data. It is composed of 8 D-flip - flops that are cascaded and connected to synchronized clocks. It is depicted in the truth table.

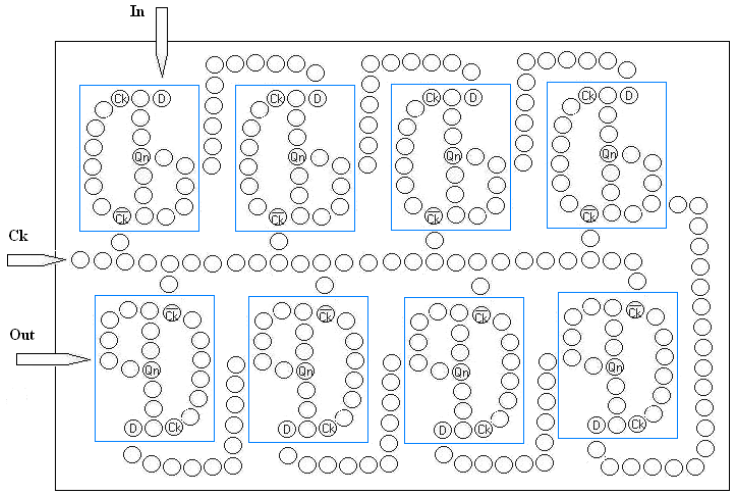
TABLE 1

Present State		Next State		D1	D0
0	0	0	1	1	1
0	1	1	0	1	0
1	0	0	0	1	0
1	1	1	0	1	0

$$D_0 = Q_1' Q_0'$$

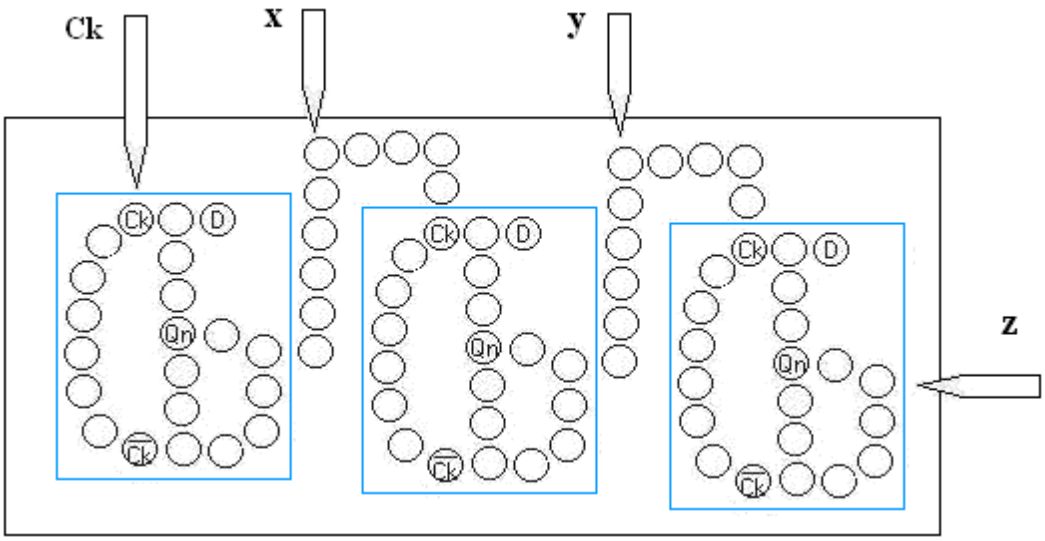
$$D_1 = Q_0$$

The spin architecture is depicted below



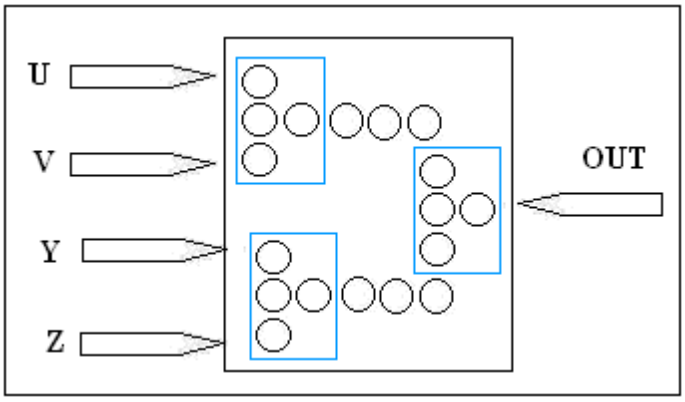
D.Unit 4 (Mod 8 Counter)

This unit simply counts the number of bit wise watermark encoding and decoding operations . The spin architecture is depicted below.



E.Unit 5 (Combination Circuit-1)

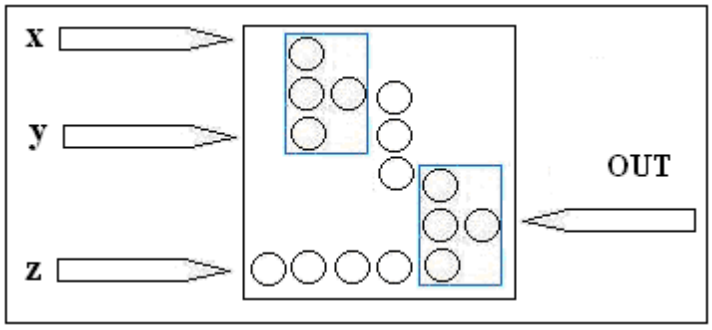
This unit is used to select the specific pixel values for data hiding. It provides a private key based adaptive threshold scheme so that perceptually significant spatial pixels can be obtained. . The spin architecture is depicted below.



F.Unit 6 (Combination Circuit-2)

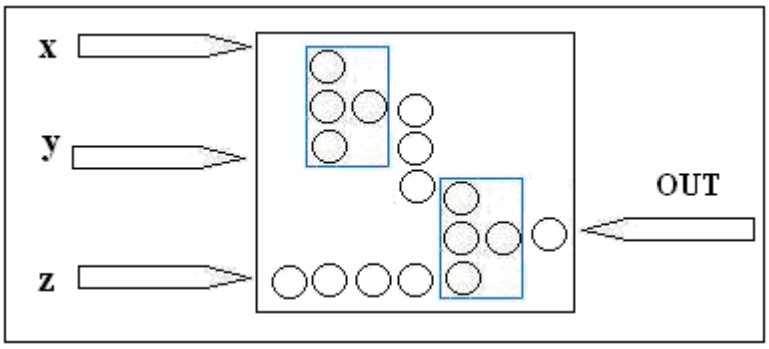
Unit 6 is an accessory block to give support to the mod 8 counter (unit 4) in order to calculate the total number of bit replacing operations .This unit is employed for a divided by 9 operation which

is realized by cascading two mod 3 counters. The spin architecture is depicted below.



G. *Unit 7 (Combination Circuit-3)*

Unit 7 is an inversion block to that of the unit 6 and helps to format the input shift register after hiding the entire message bit string into the selected pixel values .The spin architecture is depicted below.



7.FUNCTION OF SPINTRONIC LOGIC AND ITS APPLICATIONS IN DESIGN OF ALUs

Spintronics technology , in contrast to the conventional electronics technology , uses an electron 'spin' in addition to its charge to transfer and store information .Magnetic tunnel junctions (MTJs) are spintronic devices that exhibit two distinct resistance states due to tunneling magnetoresistance (TMR) effect.

We use a novel design technology ' union with neutralization ' to combine individual component designs into multi-functional units .

The spintronics based ALU has the potential to offer considerable area ,timing ,and power advantages over a conventional CMOS-based ALU.

7.1.INTRODUCTION TO SPIN-TRONIC LOGIC

There are several magnetic devices that are being investigated as alternatives to silicon - based transistors .One such device is the MTJ .

The MTJ is a device that has been made to build the magnetic memories ,commonly referred to as Magnetic Random Access Memories(MRAMs) .

An MTJ exhibits properties of non-volatility , noise-resistance and its Radiation hard.

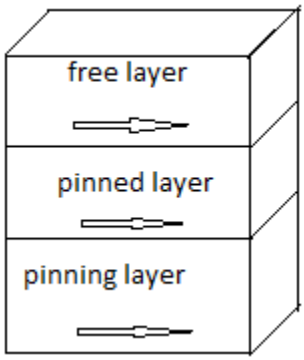
The property of non – volatility can be sensed when it eliminates the static power dissipation that imposes limits on operation of systems made out of silicon transistors .The directional spin of electrons are expected to be faster and have higher integration density than purely electronic devices .

An MTJ thus proved to be a useful and efficient element to build computational systems .

The design of ALUs using individual MTJs uses a novel design technique known as union with neutralization combines these individual functions of addition , subtraction and logical operations to get an ALU .

7.2.Operation of field driven magnetic tunnel junction

An MTJ is built from layers of ferromagnetic material like Fe , Co , Ni and their alloys .The MTJ shown below is the simplest of all these made up of two ferromagnetic layers known as free layer and pinned layer .



A simple MTJ

The pinned layer is polarized so that its magnetization direction rem--ains fixed .Normally it is achieved using another third ferromagnetic layer called as the pinning layer .The magnetization of free layer displays the effect known as TMR-'Tunneling Magneto resistance' . Under the TMR effect an MTJ show two distinct resistance states i.e. low and high , R_L and R_H

respectively with a parallel and anti-parallel relative magnetization direction of the free layer with respect to pinned layer .

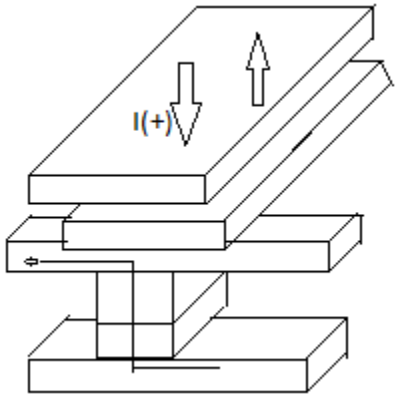
The magneto resistance ratio (MR) is defined as the ratio of differential resistance to the low resistance i.e.

$$MR = (R_H - R_L)/R_L$$

From the practical demonstration the value of MR come out to be as large as 472% at the room temperature. The R_H and R_L can be used to represent the binary states of logic0 and logic1 respectively in the digital logic. These states are non-volatile because being ferromagnetic in nature ,The free layer does not lose its magnetization even when the magnetic field used to polarize it is removed .

Normal Operation of MTJ

The below layer diagram shows the operation of two-input MTJ ,with inputs A and B .



z-plane

Two current carrying planes are placed above the free layer in such a way that when current flows through them ,they generate a magnetic field that polarizes the free layer in a direction parallel or anti-parallel to the pinned layer .

When both currents are in same direction then a net magnetic field is produced .When the additional plane z carries enough current, under an existent magnetic field due to current in input planes A and B , the pinned layer gets magnetized in same direction as free layer .

The resistance of MTJ can be measured by passing small current through the Z-plane .

The 2 - input logic function like AND ,OR ,NAND ,NOR ,XOR and XNOR can be implemented using single MTJ if fabricated in the above fashion .The table below shows the output resistance R of a 3-input MTJ ,with the pinned layer oriented as shown before .

A	B	C	R
-I(0)	-I(0)	-I(0)	L(0)
-I(0)	-I(0)	+I(0)	L(0)
-I(0)	+I(0)	-I(0)	L(0)
-I(0)	+I(0)	+I(0)	H(1)
+I(0)	-I(0)	-I(0)	L(0)
+I(0)	-I(0)	+I(0)	H(1)
+I(0)	+I(0)	-I(0)	H(1)
+I(0)	+I(0)	+I(0)	H(1)

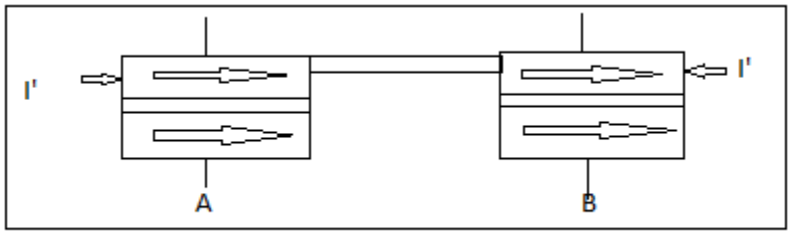
Truth table of a 3-input MTJ device

Had the pinned layer in the opposite direction, the output would have been exactly the complement ,R'.

7.3. Spin Torque Transfer

In the researches,researchers developed a novel technique that enables fan-out function for MTJs using the concept of spin torque transfer .

The below set-up is for the spin torque transfer.



Spin-torque transfer using MTJs

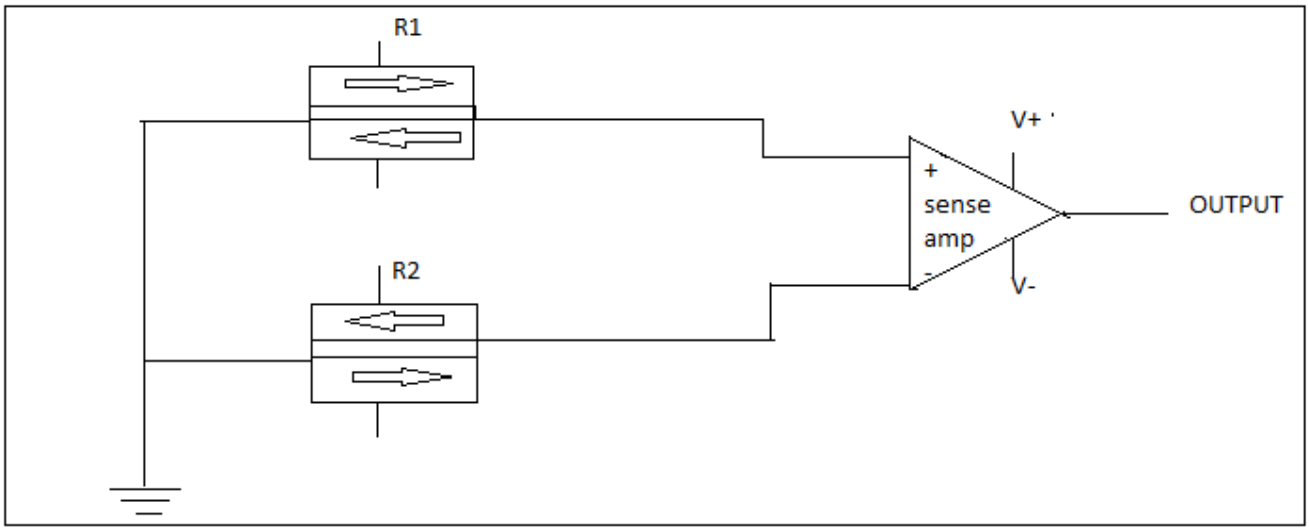
In the previous figure two MTJs are physically connected using a channel of magneto nano channel that connects the free layers of 2 MTJs .

The specially designed nano-channel isolates the two MTJs and they can be operated individually during normal operation.

The current that flows in through terminal I and I' polarizes the free layer of MTJ B in the same direction as that of MTJ A .If the pinned layers of both MTJs are oriented in the same direction , then both MTJs will have the same resistance state after the spin torque transfer .

8.DESIGNING WITH MTJs:

Sense amplifiers are used in this case .Normally one or more MTJs are connected in series to positive and negative terminals of a sense amplifier as shown below in the figure .



General MTJ setup for logic function

The output of this circuit is produced in two time steps ,they are

- Logic step
- Output generation

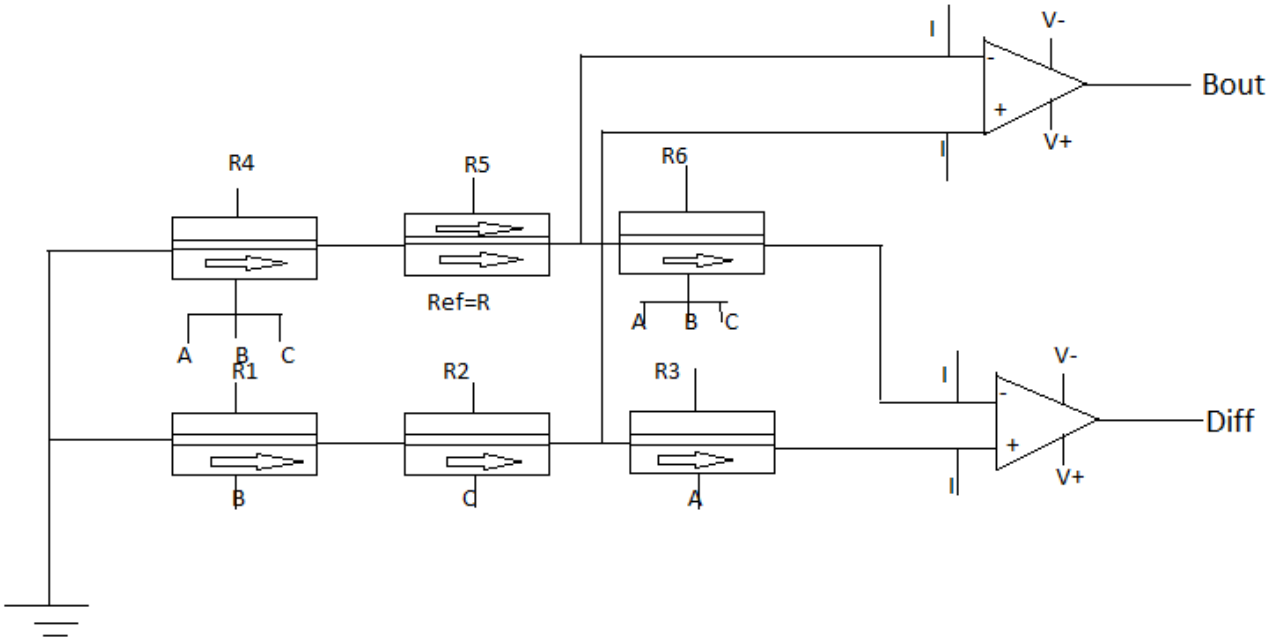
According to the respective inputs all MTJ resistance states are in the logic step .During the case of output generation ,a small sense current is applied to the MTJs which results in the generation of a small voltage whose magnitude is totally based on the combined resistance of MTJs connected to a terminal .

Now the role of the sense amplifier comes into existence ,it then amplifies the voltage difference between the +ve and –ve terminals and outputs a voltage 0V if the resistance are equal in magnitude else outputs a voltage 5V if the resistances are unequal .

8.1.Design of ALU components

The design of ALU is distributed in parts. All the components are designed so that there is no need to preset the resistance state of any MTJ before operation .

The design of 1-bit subtractor is shown in the figure along with the truth table .



A	B	C	R_4	T_1 $=R_1$ $+R_2$	T_2 $=R_4$ $+R_5$	D_{iff} $=T_1$ $–T_2$	T_3 $=R_1$ $+R_2$	T_4 $=R_4$ $+R_5$	B_{out} $=T_3$ –	

				$+R_3$	$+R_6$				T_4	
0	0	0	L	LLL	LLL	0	LL	LL	0	
0	0	1	L	LLH	LLL	1	LH	LL	1	
0	1	0	L	LHL	LLL	1	HL	LL	1	
0	1	1	H	LHH	HLH	0	HH	HL	1	
1	0	0	L	HLL	LLL	1	LL	LL	0	
1	0	1	H	HLH	HLH	0	LH	HL	0	
1	1	0	H	HHL	HLH	0	HL	HL	0	
1	1	1	H	HHH	HLH	1	HH	HL	1	

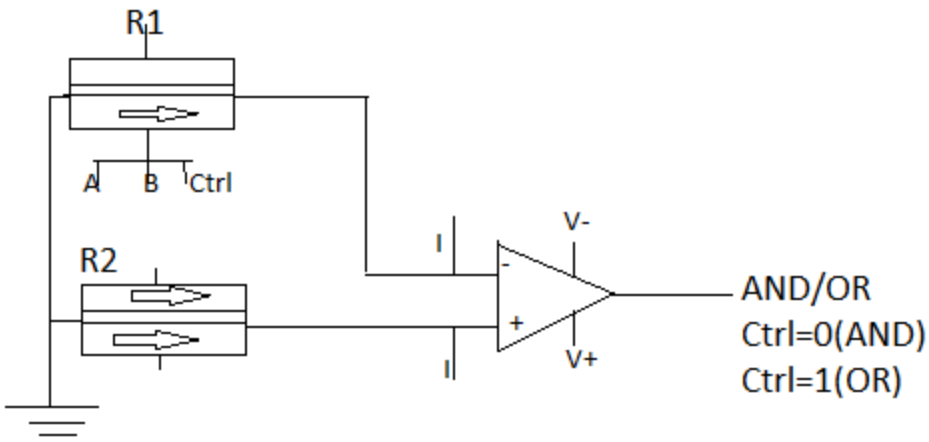
1-bit spintronic subtractor using MTJs and its truth table

Inputs A, B and C(borrow-in) are applied ,resistance states R_1 through R_6 are set .

A sense amplifier amplifies the difference $[(R_1+R_2+R_3)-(R_4+R_5+R_6)]$ and gives the output 0V i.e. logic 0 when $R_1+R_2+R_3 = R_4+R_5+R_6$. When $R_1+R_2+R_3 > R_4+R_5+R_6$,output is V_+ i.e. logic 1 .

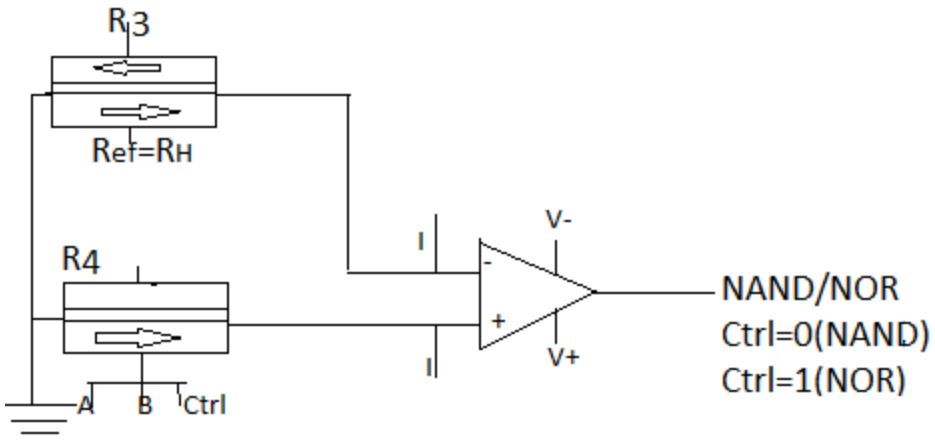
There is another sense amplifier which produces the output of logical function $[(R_1+R_2)-(R_4+R_5)$ .This function signifies B_{out} .

The design of 1-bit logical units that perform the logical function of AND , OR ,NAND ,NOR ,XOR and XNOR depicted in the following figure.



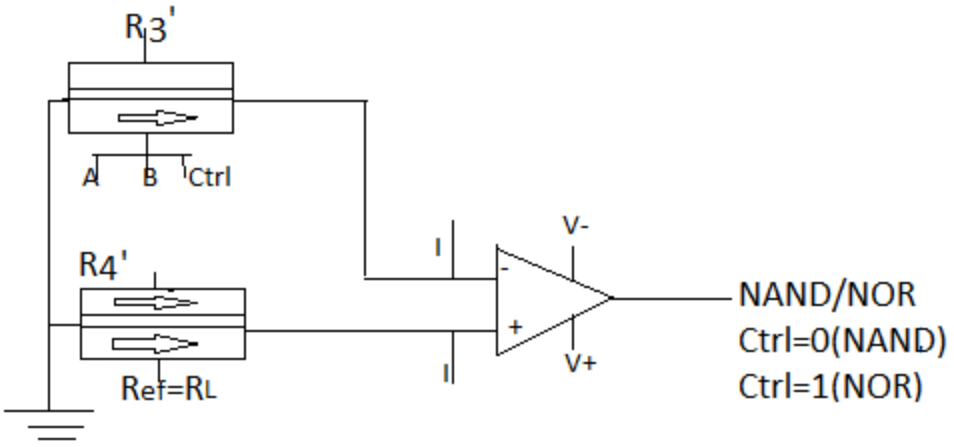
Ctrl	A	B	R_1	R_2	Out=R_1-R_2	Function
0	0	0	L	L	0	AND
	0	1	L	L	0	
	1	0	L	L	O	
	1	1	H	L	1	
1	0	0	L	L	0	
	0	1	H	L	1	
	1	0	H	L	1	OR
	1	1	H	L	1	

AND-OR gate using MTJs and truth table



Ctrl	A	B	R_3	R_4	Out=R_3-R_4	Function
0	0	0	H	L	1	NAND
	0	1	H	L	1	
	1	0	H	L	1	
	1	1	H	H	0	
1	0	0	H	L	1	
	0	1	H	H	0	
	1	0	H	H	0	NOR
	1	1	H	H	0	

NAND/NOR gate using MTJs and truth table



Ctrl	A	B	R'_3	R'_4	Out=R'_3-R'_4	Function
0	**0** **0** **1** **1**	**0** **1** **0** **1**	**H** **H** **H** **L**	**L** **L** **L** **L**	**1** **1** **1** **0**	**NAND**
1	0 0 1 1	0 1 0 1	H L L L	L L L L	1 0 0 0	NOR

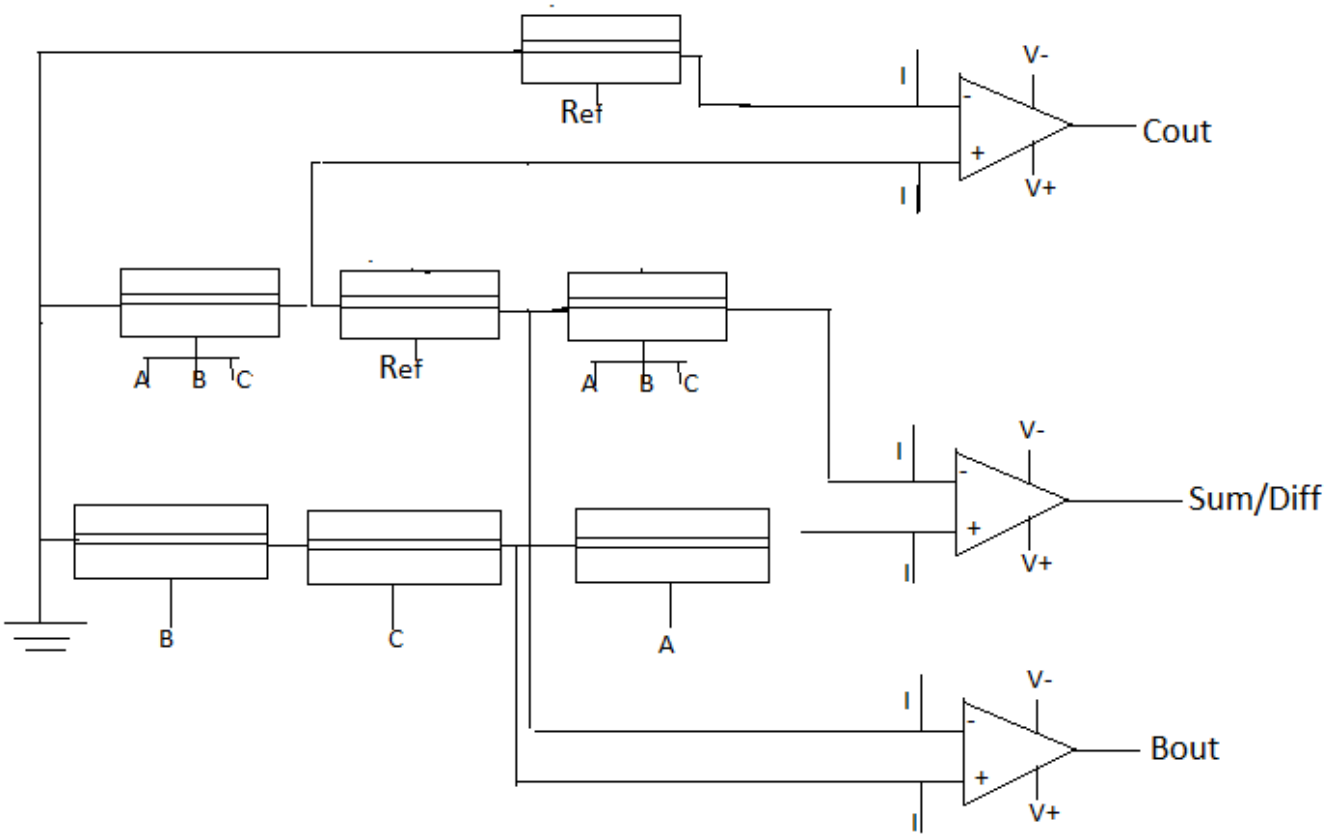
NAND/NOR gate using MTJs in another configuration

8.2.Combining logic functions into larger components

In the TMR based circuits , since output depends upon the state of every device connected in series it is not always possible to combine two circuits directly . In cases where it is possible ,there are certain challenges produced by the sensing logic .

Direct combination

By combining directly a full adder and a full subtractor an adder / subtractor may be designed .



1-bit spintronic adder/subtractor constructed from direct combination of full adder and full subtractor

In the above design seven MTJs and three sense amplifiers are used . Practically this kind of design presents certain difficulties and it should implement certain control inputs to ensure that addition is performed for a certain of control inputs and subtraction for others .

Those practical difficulties are overcome by the new following approach .

8.3.Concept of union with neutralization

By deliberately mismatching the transistors in the sense amplifiers a difference of 0 will be considered as a negative difference.

When logical output is 0 ($V_+ = V_-$) then amplifier status is V_-.

When logical output is 1($V_+ != V_-$) then amplifier status is V_+.

When V_+ is there then higher resistance will be there and then amplifier will saturate to V_+.In this way 1-bit adder/subtractor units can be connected together so that the output Cout is applied directly to the input C of the next adder to get an n-bit adder/subtractor .

For 1-bit design 12 MTJs and 2 sense amplifiers are used.

For n-bit design 12n MTJs and 2n sense amplifiers are used.

1 unit has three control steps i.e.

- Logic step
- Spin torque transfer
- Output generation

The 3rd step in the i-th unit overlaps with logic step in (i+1)th unit. Thus the design operates in exactly (2n+1) times units .In the modified design 'union with neutralization' is used to combine logic functions into single unit .Generally ,when combined directly 2 separate MTJ-based units give a truth tale entirely different from desired truth table or either of their truth table .When AND gate and NAND gate are combined they generate the output something like this

[(AandB) + (AnandB)]-[L+L]

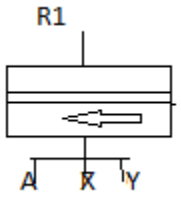
It produces an output of logic 1 for input value schemes which are not desired .This problem can be solved by isolating one of the logic gates when the other is required .This is done using the concept of 'union with neutralization' in which only one logic is forward to the output and the rest are neutralized .

There are 3 ways of performing neutralization

- Neutralization using control input.
- Neutralization using spin torque transfer.
- Neutralization through logic.

Neutralization using control input:

There are 2 control inputs i.e. X and Y or there is a control input and a static input .

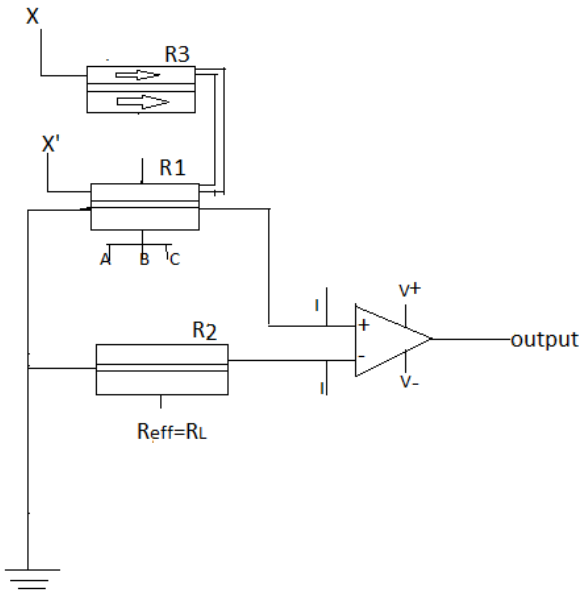


When Y is logic0 control input is high and output follows A.

When Y is logic 1 and control input is low the R1 is high output.

Neutralization using spin torque transfer:

When MTJs have more than one input then it cannot be easily neutralized using a control input .Additional MTJs are used to perform the same function as MTJs connected to opposite terminal of sense amplifier .Then by using spin torque transfer technique , this status can be transferred to MTJs ,so that MTJs on both sides are neutralized .

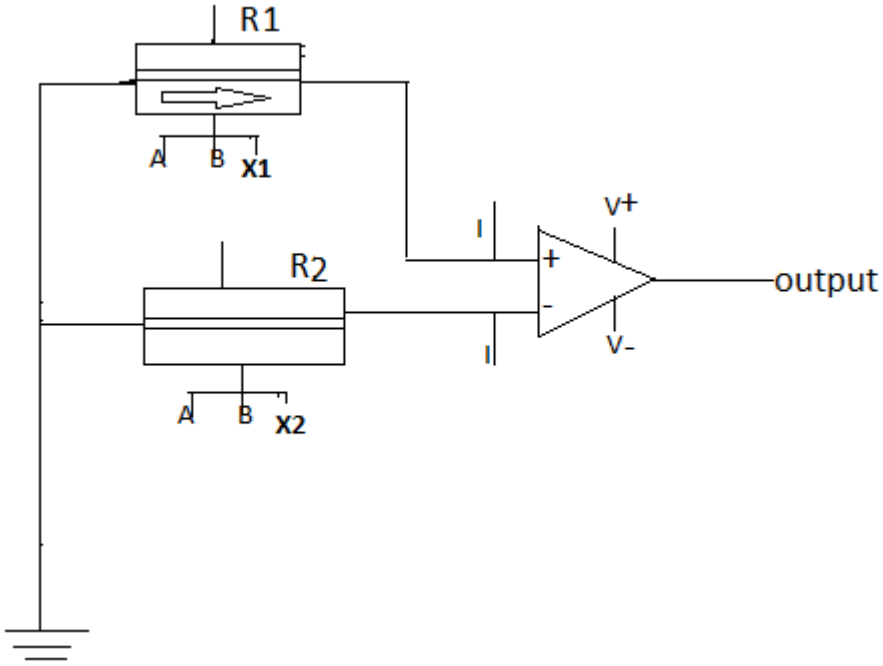


When X=0 then normal logic operation are output by the sense amplifier .

When X=1 state of R3 to R1 and the two resistances are equalized.

Neutralization through logic:

It is used for specific functions only and implemented through observation of logic function .



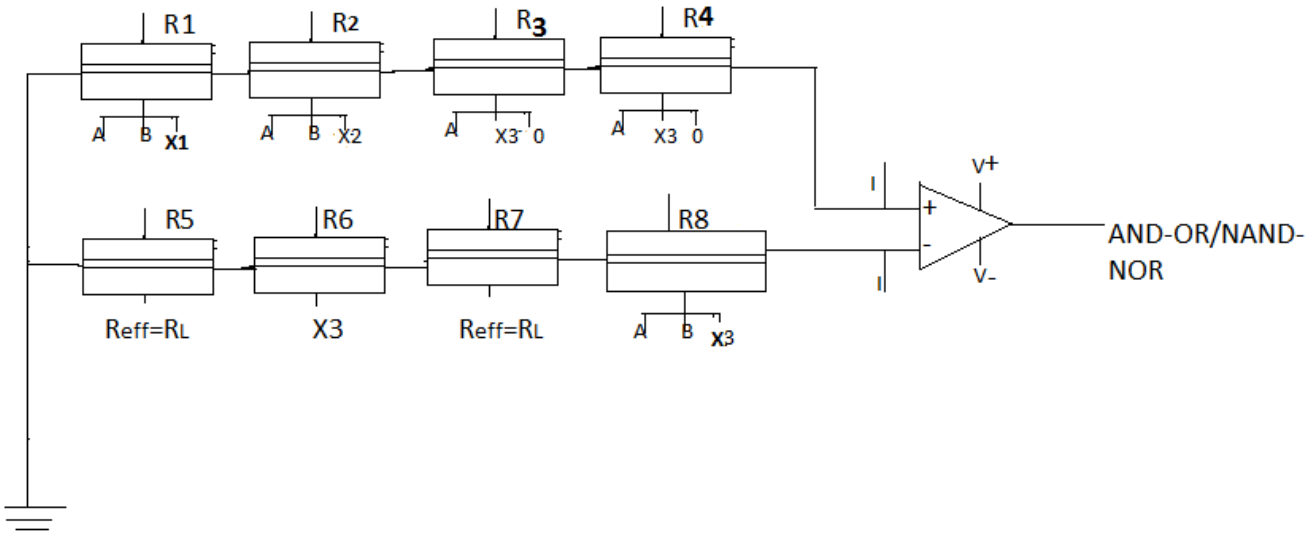
When X1=1 & X2=0 then XOR is performed.

When X1=X2 then output is 0.

There are many cases where single technique is not effective ,in that situation a combination of all these methods are used .

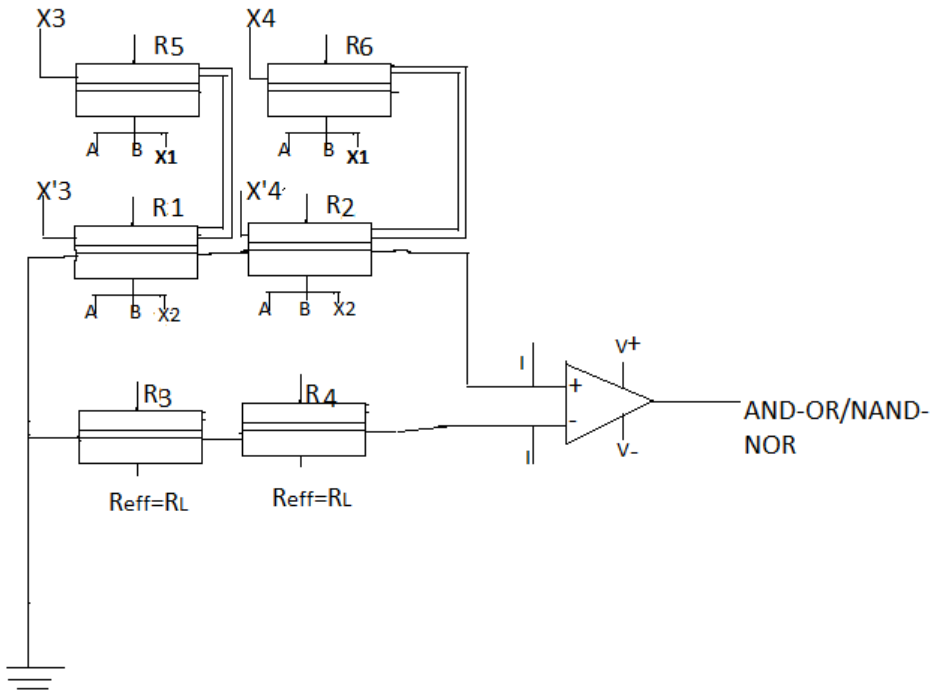
Choices of technique is based on design requirements of timing and area.

Eg: to construct logical unit that perform the operations of AND,OR, NAND and NOR ,neutralization using control input and using logic may be used.



Logical unit performing AND ,OR ,NAND and NOR using neutralization by control input through logic .

Another unit is constructed solely using neutralization with spin torque transfer.



X_1	X_2	X_3	X_4	Function
0	X	0	1	AND
1	X	0	1	OR
X	0	1	0	NAND
X	1	1	0	NOR

Logical unit performing logical functions using neutralization by STT .

The AND/OR part is due to resistance R_1 and its reference R_3.

The NAND/NOR part is due to resistance R_2 and its reference R_4.

R_5 and R_6 are additional MTJs in the circuit with low resistance.

R_5 is to neutralize R_1.

R_6 is to neutralize R_2.

8.4.Operation

- First step: MTJs that constitute R_1 and R_2 are allowed to set their outputs as a function of their inputs.

  Control inputs X_1 and X_2 are set according to desired function.
- Second step: MTJ R_2 is neutralized by transferring the state of R_6 to it .For this purpose control input X_4 is high.

Sense amplifier relies on (R_1-R_3) only to give its output.

For NAND/NOR MTJ R_1 is neutralize in similar manner.

For STT ,the complete logical operation of the circuit need at least 3 control steps i.e.

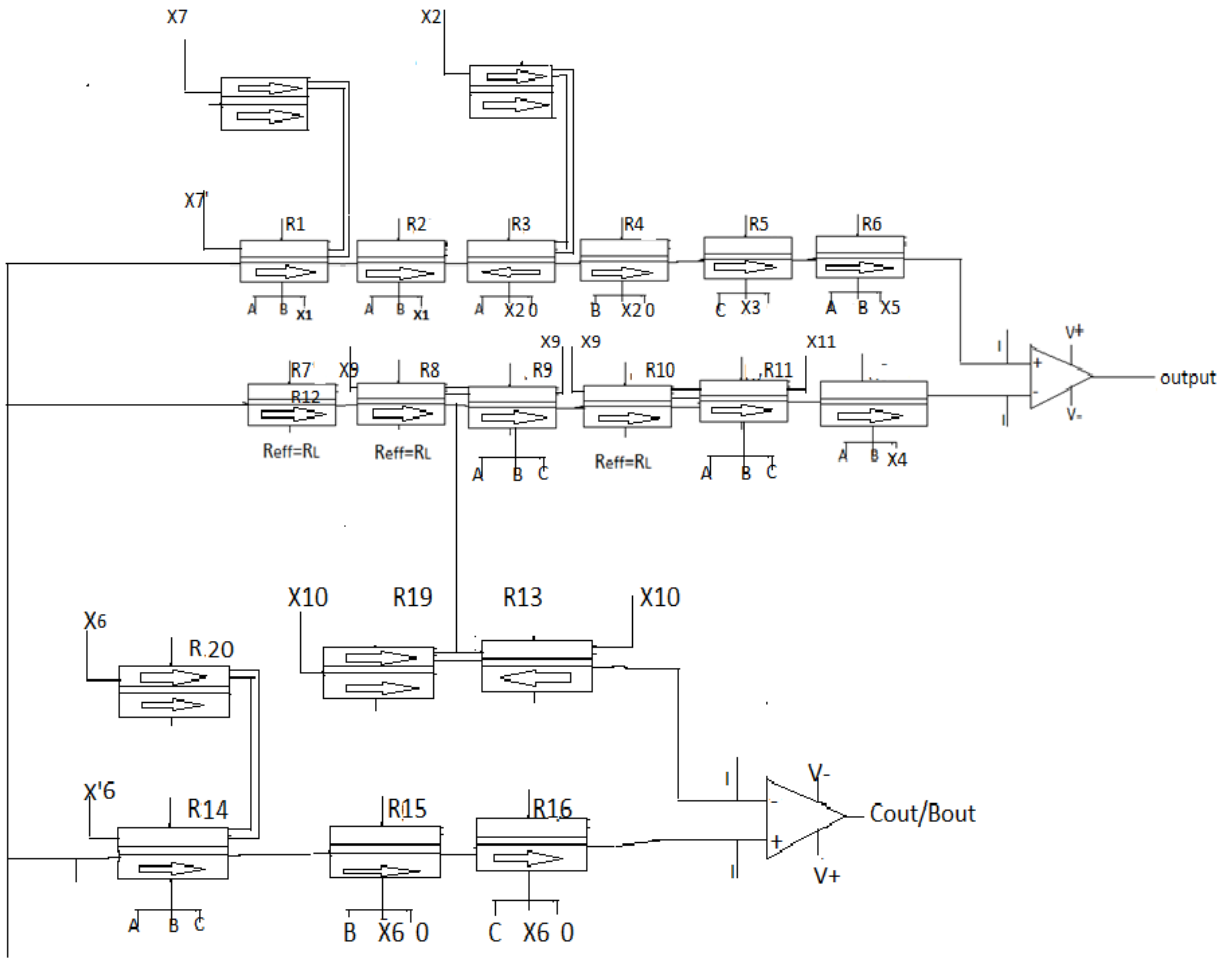
- Logic step
- Spin torque transfer
- Output generation

It is possible to generate the output in just two control steps i.e. logic step and output generation.

An ALU can b constructed using all three neutralization techniques.

9.ALU OPERATIONAL DETAILS:

The following figure describes the 1-bit ALU that is extendable up to n bits.



1-bit spintronic ALU extendable up to n bits

9.1. Description of ALU sub-units

Function	MTJ pair in ALU responsible for logic function	Number of MTJs required
AND,OR	R1 , R7	3
NAND,NOR	R2 , R8	3
XOR	R6 , R12	2
XNOR	(R5,R6) , (R7,R12)	4
ADD	(R3,R4,R5) , (R9,R10,R11) for sum (R7,R8,R13) , (R14,R15,R16) for Cout	7
SUB	(R3,R4,R5) , (R9,R10,R11) for sum (R7,R8,R13) , (R14,R15,R16) for Cout	6
Adder-sub Logical unit:4 logical fnc Logical unit:6 logical fnc ALU		12 6 10 20

The table shows the logical values of control inputs required for each function of the ALU .

X1 to X5 are current control inputs and have the value –I (logic 0) and +I (logic1).

X6 is produced as two separate kind of control signals accordingly.

When the three control steps extended to n-bits ,the last step overlaps with the first step of the next unit .

Thus n – bit consists of (2n+1) control steps to perform an n -bit operation .

10.IMPLEMENTATION OF SPINTRONIC LOGIC IN FLIP-FLOPS:

The group of gates thus far implemented are termed as combinational logic circuits .Its basic building block is the logic gate .There are some circuits which have valuable memory characteristics and these are known as sequential logic circuits .Its basic building block is the flip-flop. They are also known as "latches" and "bistable multivibrators".

The most basic flip-flop is RS flip-flop and it has two inputs, labeled set(S) and reset(R).

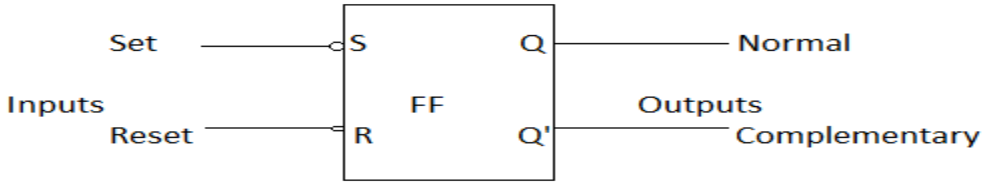
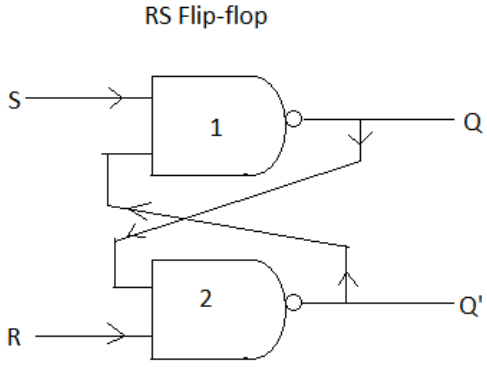


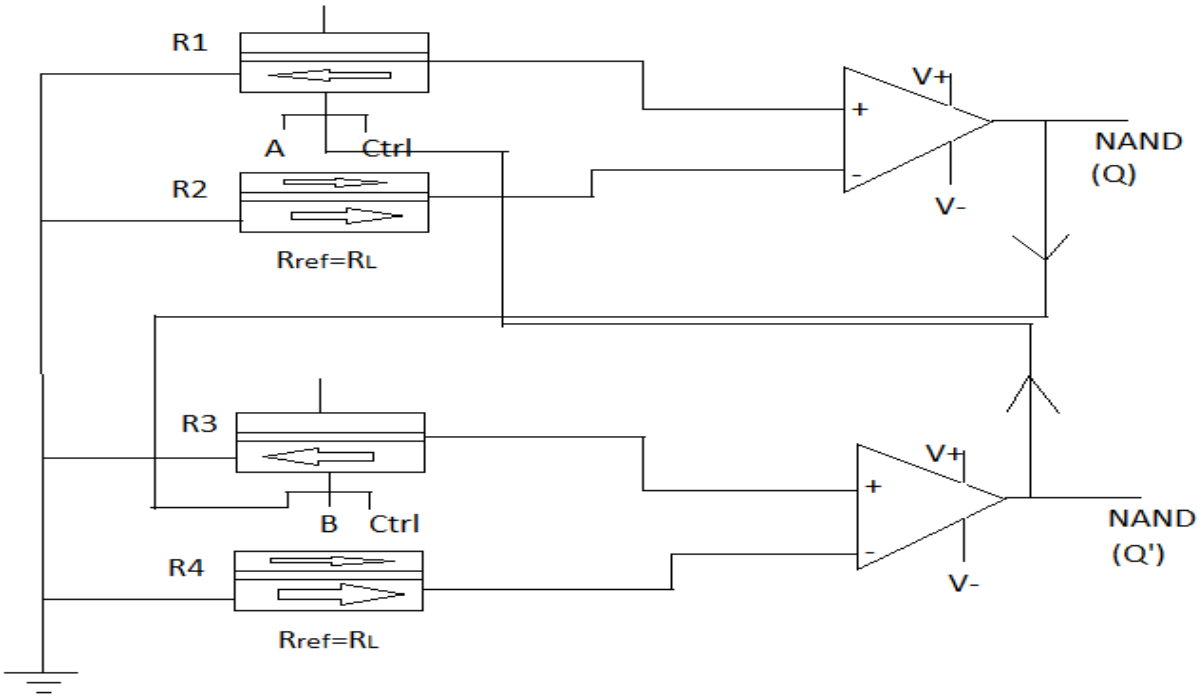
Fig. logic symbol for RS flip-flop

10.1.Construction of RS flip-flop using logic gates



Mode of operation	Inputs		Outputs	
	S	R	Q	Q’
Prohibited	0	0	1	1
Set	0	1	1	0
Reset	1	0	0	1
Hold	1	1	No change	

10.2.Using MTJs as NAND gate and implementing in RS flip-flop



When the value of Ctrl is set to logic 0 the MTJ combination as a NAND gate and combine to form an RS flip-flop .

11.COMPARISON WITH CONVENTIONAL ALU:

The fabrication of MTJ technology is still going on in laboratories .There are intensive researches going on to improve the characteristics of the device .In the arena of digital electronics spintronic logic is like an infant and only the qualitative comparison is possible with the mature CMOS technology .A 1-bit ALU that perform the 8 functions is constructed using CMOS technology requires almost 50 45nm transistors which totally depends upon the requirements and design .Currently an MTJ can be fabricated as short as 40nm in laboratories .However ,the actual dimension of the may vary and depend upon the number factors such as TMR desired ,barrier layer thickness ,material choice ,magnetic hardness of the layer etc. and are expected to be smaller .1-bit ALU using MTJs requires only 20 MTJ devices and 2 sense amplifiers where 1 unit is about equal to 4 to 7 CMOS transistors ,thus there is an area advantage over CMOS .

The propagation in the CMOS ALU is about 5 logic gates .On the contrary, the delay of the MTJ ALU is 3 control steps where each step has 1-MTJ device delay of the order of nanoseconds.

In the MRAM research ,the the write speed of 3ns could be achieved with MTJs when MTJs are combined with 180nm CMOS technology .So that is how an MTJ ALU can be expected to achieve comparable speeds to CMOS .

Unlike CMOS technology MTJs are low power devices .Thus 20 MTJ ALU is power efficient .The major disadvantage of MTJ ALU design is that it uses more control signals than a CMOS based ALU.

Overall spintronic devices have better advantages than conventional devices and they are faster, non-volatile, robust, power efficient etc .

12.CONCLUSION

The digital watermarking technique is analyzed using conventional FPGA and spintronics .The comparison has been made on the basis of analysis of results .Logic gates and flip-flops using spintronic devices are characterized by non-volatility ,noise resistance ,robustness ,programmability and low power requirements .The devices and systems built with the help of MTJ ,are expected to have these advantages over those built with the help of conventional silicon-based transistors .

An attempt has been made by us to analyze the novel area of spintronic to explore its potential in digital electronics world .We have analyzed and presented the design of 1-bit arithmetic and logical unit and RS flip-flop using MTJ elements and sense amplifiers and enumerated the control signals necessary for its operation .We have laid down a formal method in the design development for a bottom-up design with TMR devices .Still the spintronic ALU is not found on chips ,the necessary research is still going on in this field ,while this analytical work presents a chancellor step to introduce and elaborate this new technology ,while a design challenge is characterized and a solution is proposed .

13. REFERENCES:

1. Ankush Ghosh, Dept of Electronics and telecommunication,Jadavpur university "Realisation of VLSI chip using FPGA for digital image watermarking in spatial domain and single spin logic".
2. Ankush Ghosh, T. S. Das,V.H. Mankar, Subir Kumar Sarkar Dept. of Electronics and Telecomm.Engg., Jadavpur University,Kolkata-32 India ,Abhishek Basu Dept. of Radiophysics and Electronics,University of Kolkata, India ,Debasis Samanta Centre for Educational Technology,Indian Institute of Technology,Kharagpur, India "Single spin logic realization of Robust Image Watermarking in Spatial Domain " .
3. Shruti R. Patil, Xiaofeng Yao, Hao Meng, Jian-Ping Wang, David J. Lilja Dept. of Electrical and Computer Engineering University of Minnesota Twin Cities Minneapolis, MN, USA "Design of a Spintronic Arithmetic and Logical Unit Using Magnetic Tunnel Junction " .
4. S.P Mohanty ,"Watermarking of digital images",Masters project report ,Dept. of Electrical Engineering ,IISc ,Bangalore ,India ,Jan 1999.
5. Ankush Ghosh,"To study some aspects of semiconductor nanodevices including spintronic devices and explore some of their applications" ,Jadavpur university ,Jan 2010.
6. I. Cox, M. Miller, J. Bloom, "Digital Watermarking", Morgan Kaufmann Publishers, 2002.
7. M. Barni, F. Bartolini, A. Piva, "Improved Wavelet based Watermarking through Pixelwise Masking," IEEE Trans. On Image Processing, Vol. 10, No. 5, pp. 783-791, 2001.

8. H. Lim, S. Park, S. Kang, W. Chao, "FPGA Implementation of Image Watermarking Algorithm for a Digital Camera," IEEE Conf. pp. 1000- 1003, 2003.
9. S. Bandyopadhyay, B. Das and A. E. Miller, "Super computing with spin polarized single electrons in a quantum coupled architecture", Nanotechnology 5, pp. 113 (1994).
10. S. K. Sarkar, T. Basu and S. Bandyopadhyay, "Single Spin Logic Circuits", Phys. of low dim. Struc., 2005.
11. H. Agarwal, S. Pramanik, and S. Bandyopadhyay, "Single spin universal Boolean logic gate", New Journal of Physics, 10,015001,2008.
12. J. Hayakawa, Y. M. Lee, S. Ikeda, F. Matsukura, and H. Ohno. "Effect of high annealing temperature on giant tunnel magnetoresistance ratio of CoFeB/MgO/CoFeB magnetic tunnel junctions". *Applied Physics Letters*, 89:232510–232510–3, 2006.
13. H. Meng, J. Wang, and J.-P. Wang. A spintronics full adder for magnetic CPU. *IEEE Electron Device Letters*, 26(6):360–362, 2005.
14. J.-P. Wang and H. Meng. Spin torque transfer structure with new spin switching configurations. *The European Physical Journal B - Condensed Matter and Complex Systems*, 59(4):471–474, 2007.
15. http://www.ece.umd.edu/class/enee702.F2005/handout/spin/scientificamericanspintronics2003.htm
16. http://www.scribd.com/doc/46840928/Spintronics
17. http://web.vu.union.edu/~shoemakc/watermarking/watermarking.html
18. http://ethesis.nitrkl.ac.in/1960/1/final_prj.pdf