STUDY OF VOLTAGE-CONTROLLED OSCILLATOR BASED ANALOG-TO-DIGITAL CONVERTER

A THESIS SUBMITTED IN PARTIAL FULFILMENT OF THE REQUIREMENT FOR THE DEGREE OF

BACHELOR OF TECHNOLOGY

IN

ELECTRICAL ENGG.

BY

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NATIONAL INSTITUTE OF TECHNOLOGY

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NATIONAL INSTITUTE OF TECHNOLOGY ROURKELA

CERTIFICATE

This is to certify that the thesis entitled ***"Study of Voltage-Controlled Oscillator based Analog–to-Digital Converter"*** submitted by **Saptarshi Pal Choudhuri (107ee001), Supriya Sneha (107ee012) and Soumalya Adhikari (107ee054)** in the partial fulfillment of the requirement for the degree of **Bachelor of technology** in **Electrical Engineering**, **National Institute of Technology** Rourkela is an authentic work carried out by them under my supervision.

To the best of my knowledge the matter embodied in thesis has not been submitted to any other university/institute for the award of degree or diploma.

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CONTENTS

ABSTRACT

A voltage controlled oscillator (VCO) based analog-to-digital converter (ADC) is a time based architecture with a first-order noise-shaping property, which can be implemented using a VCO and digital circuits. This thesis analyzes the performance of VCO-based ADCs in the presence of non idealities such as jitter, nonlinearity, mismatch, and the metastability of D flip-flops. Based on this analysis, design criteria for determining parameters for VCO-based ADCs are described.

Further, the study involves the use of VCO based Dual-slope A/D converter and its behaviour under different input voltage level. Graph is plotted between output voltages of the integrator vs. time. Digital circuits like a bit-counter and logic circuits are used for operation mode. A normal VCO model is also done in MATLAB-simulink environment and studied under variable input frequency and corresponding output plots are viewed.

CHAPTER 1

1.1 INTRODUCTION

In present world ADCs are of great importance. ADC is a device that converts analog (continuous signal) to digital signal (discrete time signal). Hence, an ADC is an electronic device that converts an analog input voltage or analog current to a digital form whose magnitude is directly proportional to the input voltage or current.

Resolution of the converter is in binary form which indicates the number of discrete value it can produce along the range of analog values. The resolution is expressed in bits. For eg: - ADC with resolution 8 bits can produce 256 levels. These values can be ranged from 0 to 255 or -128 to 127 depending upon the application used. Resolution can be defined electrically which is expressed in volts. Most of the ADCs are of linear type. Here 'linear' means for linear input we get linear output. Like all the devices ADCs are not 100 percent accurate, it has also some sources of error like quantization error and non-linearity which are intrinsic to ADC conversion. The commercial ADCs are usually integrated circuits. The converters are of 6 to 24 bits of resolution which produce 1 mega-sample per second. Thermal noise generated by passive components (like resistor etc.) affects the high resolution output. For application in audio and at room temperatures, the noise should be less the 1 microvolt. The most expensive part of an ADC is pin which makes the package larger in size. So make it smaller or to reduce its size microprocessors are used.

1.2 APPLICATIONS OF ADC

ADCs are used in music recording applications. Since music production is done on the computer where analog signals are used. Another use of ADC is digital signal processing.

The design of ADC based on voltage-domain is difficult because of low input or supply voltage with upcoming technology. An ADC based on VCO generates a time based signal whose frequency is directly proportional to the analog input voltage. The frequency is then quantized by counting the edges of the output of VCO during a sampling period. Since the VCO produces a continuous phase output, the quantization noise of the previous sample affects the present sample, and hence, an inherent first-order quantization noise-shaping property can be achieved.

CHAPTER 2

2 DIFFERENT TYPES OF ADC

There are four different and most popular A/D converters:

A) Direct Conversion ADCs

B) Successive-approximation ADCs

C) Integrating type or Dual slope ADCs

D) Sigma –Delta ADCs

2.1 DIRECT CONVERSION ADCs

Out of four topics mentioned above, the fastest is the direct conversion. It is also known as "flash" conversion. ADCs based on this type of architecture are extremely fast and perform their direct multibit conversion. But major problem is that, it requires intense analog design to manage large number of comparator and reference voltages.

2.1.1 WORKING PRINCIPLE AND DESCRIPTION

Figure shows a simple direct conversion ADC with 2^{N-1} comparators connected in parallel and with N-bit resolution. Change in the input voltage results in the change in state of comparator output. Then these outputs are combined in logic circuits which produce a parallel N-bit output from the converter. Although these converters are the fastest type available, there resolution is constrained by the available die size by increasing the input capacitance and the power consumption by the large number of comparators. The presence of repetitive structure demands

accurate matching between the parallel comparator sections, because any mismatch can lead to static error such as a magnified input offset voltage (or current).

The flash ADCs are prone to erratic and sporadic outputs called as "sparkle codes." Sparkle codes have two major sources:

A) Thermometer-codes bubbles.

B) Metastability in the 2^N-1 comparators.

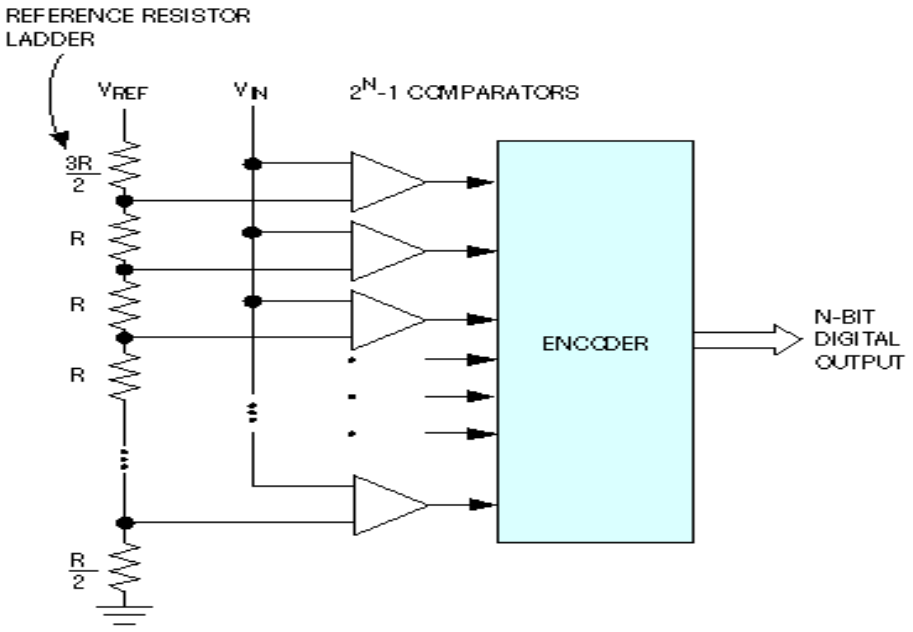


Fig.1. ADCs based on the direct-conversion architecture include 2^N-1 comparator banks and a reference resistor-divider network. [1]

The flash type ADC has resolution of 8 bits and speed of 250Mbps-1Gbps.

A) Advantages

a) Extremely fast

b) High input bandwidth

B) Disadvantages

a) Highest power consumption

b) Large die size

c) High input resistance

d) Expensive

e) Sparkle codes

2.2 SUCCESSIVE –APPROXIMATION ADCs

This conversion technique is based on a successive-approximation register, also called as bit-weighing conversion in which comparator has to weigh the applied voltage against the output of an N-bit digital to analog converter (DAC). The converters consist of one comparator, one DAC, one successive-approximation register and control logic. The sample rate is 1 Msps. The resolution is between 10-16 bits. Its speed is in the range of 76- 250ksps.

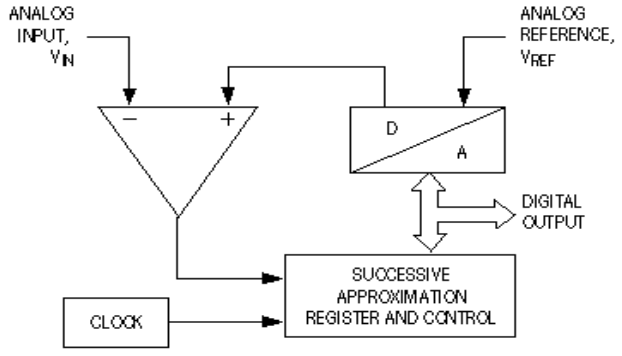


Fig.2.Typical successive-approximation ADCs consist of a single DAC, a comparator, and a successive-approximation register (SAR), plus a clock and logic control [1].

2.2.1 WORKING PRINCIPLE AND DESCRIPTION

A successive-approximation converter is comprised of a DAC, a comparator, some control logic and registers. Due to comparator signal when input is applied, the control logic initially sets all bits to zero.

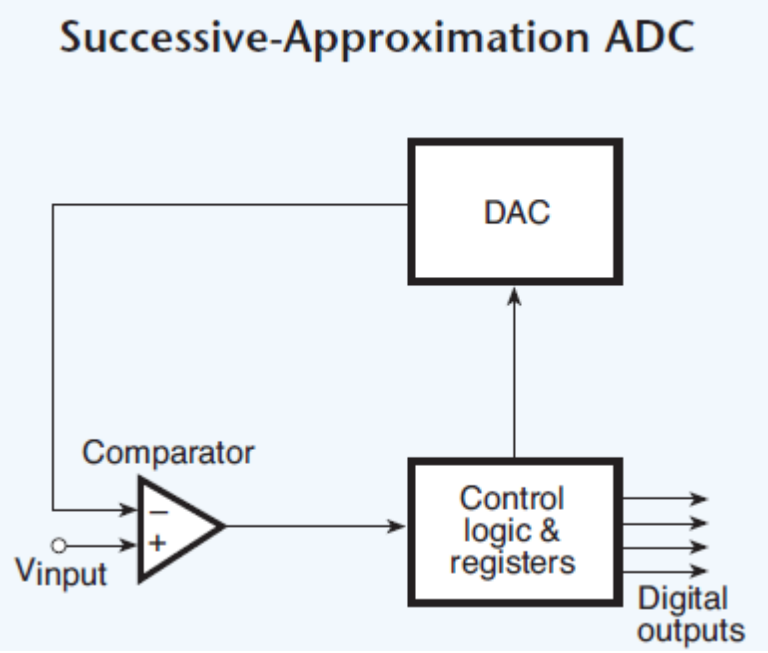


Fig.3.Successive approximation ADC

Then DAC's MSB is set to 1.So DAC output bits are like 1, 0, 0.....Hence the output is half the full scale. Then comparator compares the DAC analog output to the input signal Vin, and if the DAC output is lower than the input signal , MSB remains 1 else it resets to zero. Then the next bit on right to MSB of DAC is set to 1.hence total of $3/4^{th}$ weightage of full scale (or $1/4^{th}$, if MSB is reset to zero) is applied to comparator. Thus the process goes on like iteration until LSB is compared. At the end of approximation register gives the output.

SAR ADCs are relatively slow because the process run serially and the ADC must pause at each step to set the DAC. However, conversion rates easily can reach over 1 MHz

A) Advantage

a) Low power consumption

b) High resolution and accuracy

c) Few external components

B) Disadvantages

a) Limited sampling rate

b) Low input bandwidth

c) V_{in} must remain constant during conversion

2.3 INTEGRATING ADCs

It is also called as dual slope ADCs. It is the most popular type of ADC. It consists of two main sections: first is the circuit that acquires and digitizes the input which produces a pulse sequence and the second is the counter that converts the result into a digital value. The resolution is greater than 18 bits and speed is less than 50 ksps.

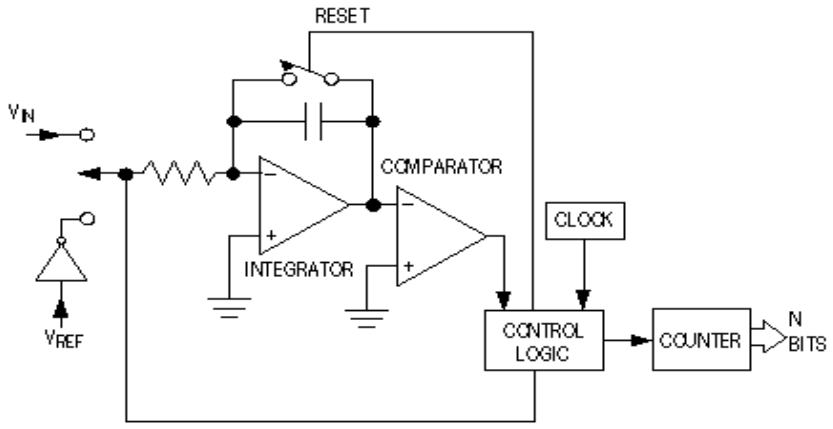


Fig.4.For slowly changing signals, one of the slowest but simplest conversion techniques employs an integrator that charges with the input voltage and discharges with an opposite-polarity reference voltage.[1]

2.3.1 WORKING PRINCIPLE AND DESCRIPTION

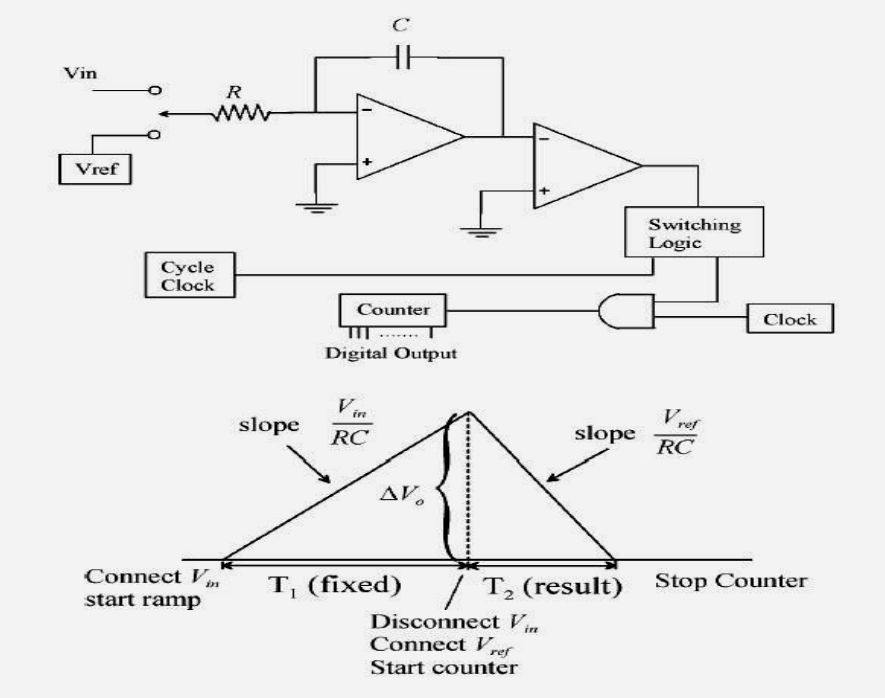


Fig.5.Working principle of Integrating ADC

The basic integrating ADC circuit consists of a switch, an integrator, a timer that determines how long to integrate the unknown and measures duration of the reference integration, a controller, and a comparator. The switch is installed between the voltage to be measured and the reference voltage (generally taken negative). Depending on the operation, a switch connected in parallel with the integrator capacitor for resetting the integrator in two consecutive rounds (by discharging the integrator capacitor). The switches are controlled by dedicated controller or by microprocessor.

The conversion takes place in two phases; one is the run-up phase, and the other is the run-down phase. In the first stage the voltage, which is supplied to the integrator is to be measured. During first part i.e. the run-up phase, the switch selects the measured voltage as the input provided to the integrator. Then the integrator is allowed to ramp for a fixed interval of

time for the charging of the capacitor. During the second part i.e. run-down phase, where the input to the integrator is a reference voltage (negative), the switch selects the reference voltage as the input voltage of integrator. The time taken for the integrator's output to return to zero value is measured during this phase.

The basic equation for the output of the integrator [2] (assuming a constant input) is:

$$V_{out} = -\frac{V_{in}}{RC} t_{int} + V_{initial} \tag{1}$$

Assuming that the initial integrator voltage at the start of each conversion is zero and that the integrator voltage at the end of the run down period will be zero, the following equations can be derived for two phases:

$$V_{out-up} = -\frac{V_{in}}{RC} t_u \tag{2}$$

$$V_{out-down} = -\frac{V_{ref}}{RC} t_d + V_{out-up} = 0 \tag{3}$$

Solving we get:

$$V_{in} = -V_{ref} \frac{t_d}{t_u} \tag{4}$$

The input signal is applied to the integrator; at the same time a counter is started, it counts up from 0000 (if 4 bit) due to the comparator output (integrator output depends on capacitor voltage charging; comparator compares the integrator output with ground level, i.e. zero volt, clock pulses being ANDed with comparator output is fed to the counter) counting clock pulses, after a pre-determined amount of time (T), as the counter reaches its maximum count, control

circuit switches a reference voltage having opposite polarity is to the integrator input. At time T+, the accumulated charge on the integrating capacitor is proportional to the average value of the input over the interval T. The integral of the reference is an opposite-going ramp having a slope of V_{REF}/RC. At the same time, the counter is reset. When the integrator output reaches zero, comparator output also reaches zero and the count is stopped, and the capacitor voltage is reset along with the switching to V_{in} from V_{ref} again. Since the charge gained is proportional to $V_{IN} \times T$, and the equal amount of charge lost is proportional to $V_{REF} \times tx$, the ratio of number of counts (no. Of counter bits set to 1) relative to the full scale count is proportional to tx / T. If the output of the counter displays a binary number, it will be the binary representation of the input voltage.

2.3.1 RESOLUTION OF DUAL-SLOPE ADC

The resolution of the dual-slope integrating ADC is determined primarily by the time for run-down period and by the frequency of the controller's clock. The required resolution (in number of bits) shows minimum length of the run-down period for a full-scale input ($V_{IN} = -V_{ref}$)-

$$t_d = \frac{2^r}{f_{clk}} \tag{5}$$

A) Advantages

a) Low supply current

b) High resolution

c) Excellent noise rejection

C) Disadvantage

a) Low speed

2.4 SIGMA-DELTA TYPE ADCs

The sigma-delta model (∑-Δ) has simple structures. These are also called as oversampling converters. These consist of delta-sigma modulator and a digital decimation filter. The architecture of delta-sigma is similar to that of dual slope ADC. The sampling frequency is very high (2MHz). Its resolution is greater than 16 bits and speed is greater than 200ksps.

A sigma-delta ADC contains an integrator, a DAC, a comparator, and a summing junction. Like the dual-slope ADC, it's often used in digital millimeters, panel meters, and data acquisition boards. Sigma delta converters are relatively inexpensive primarily because, in this complex analog building blocks are used like op-amps and DAC converter.

2.4.1 WORKING PRINCIPLE AND DESCRIPTION

The input voltage sums algebraically to output voltage of the DAC $V_d$ac, and the integrator adds the summing point output Vs to a value it stored previously.; the comparator output switches to logic one when the integrator output V_{io} >=0, and when it is less than zero, the comparator switches to logic zero.

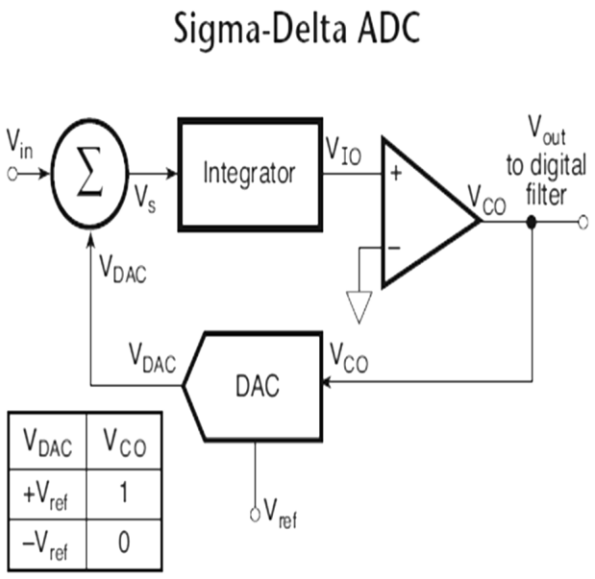


Fig.6.The principle of operation can be understood from the diagram.

The DAC modulates feedback loop, continually adjusting output of the comparator to equal the analog input and maintain the integrator output at zero. Thus the output signal becomes a one-bit data stream (at a high sample rate) that feeds a digital filter. The digital filter averages the series of logic ones and zeros and outputs multiple-bit data. The digital low-pass filter then feeds the decimation filter, which in turn, decreases the sample rate of the multi-bit data stream.

A) Advantages

a) Low cost

b) High resolution

c) Digital on-chip filtering

d) High input bandwidth

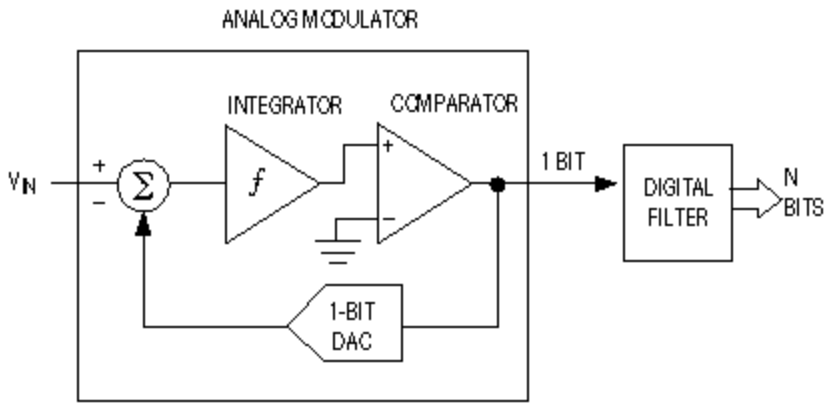


Fig.7.The two major building blocks of a sigma-delta converter are the analog modulator and the digital decimation filter [1].

B) Disadvantages

a) Limited sampling rate

b) External T/H

Besides the mentioned above four ADCs currently **"pipeline ADCs"** are used because of its size, speed, resolution, power dissipation and analog design effort.

In this project we are going to discuss the dual slope A/D converter or also known as integrating type ADC. The main benefit of using dual slope over sigma-delta is that the later one requires complex analog equipments such as op-amps and DAC, whereas the VCO based ADC can be easily implemented by using a VCO and digital circuits. Since the operating frequency is restricted by the speed of logic gates, it could reach up to gigasamples per second in advanced CMOS process. Due to all these attractive properties the VCO based ADCs are currently in the main frame.

CHAPTER 3

3. VOLTAGE CONTROLLED OSCILLATOR (VCO)

3.1 INTRODUCTION OF VCO

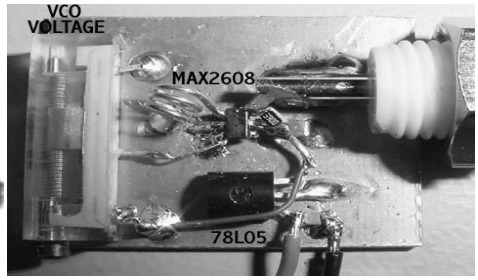


Fig.8.220px-general microwave VCO Fig.9.maxim VCO max2608

The VCO is an electrical circuit which yields an oscillatory output voltage. A VCO is an oscillator whose output frequency changes in direct proportion to the applied input voltage. VCOs can be made to oscillate from few Hertz to hundreds of GHz. The parts of a VCO has an LC tank circuit with an inductor (L) and a capacitor (C) along with one or two transistors accompanied by a buffer amplifier. It gives the periodic output signal where output signal parameter is related to the level of input control voltage directly. The center frequency of the VCO is the frequency of the periodic output signal formed by that VCO when the input control voltage is set to nominal level. The voltage-controlled oscillator has a characteristic gain, which is expressed as ratio of the VCO output frequency to the VCO input voltage [5].

VCOs utilize a variable control voltage input to give a frequency input. The control voltage input may be tuned so that a desired, operational frequency output is produced by the VCO. The input control voltage can be adjusted up or down to control the frequency of the periodic output signal. A voltage controlled oscillator can make changes in an oscillating

frequency in response to a change in control voltages. A VCO employs one or more variable capacitors called as varactors to allow the adjustment of the frequency of oscillation for the VCO. The tuning rate of a VCO refers to the range of oscillation frequencies attained by the varactors varying.

As the varactor diodes directly affect the tuning range and gain of VCO, their specifications are critical to achieve adequate performance. While most manufacturers' data sheets provide complete characteristics of the varactors at room temperature, not many provide same level of details at high temperatures. In fact, during the VCO design, no manufacturer provided any information above 100ºC. This prompted the selection of the varactors based on the relative linearity of their performance over a lower temperature range, with an assumption that the linearity would continue over a larger temperature range.[6]

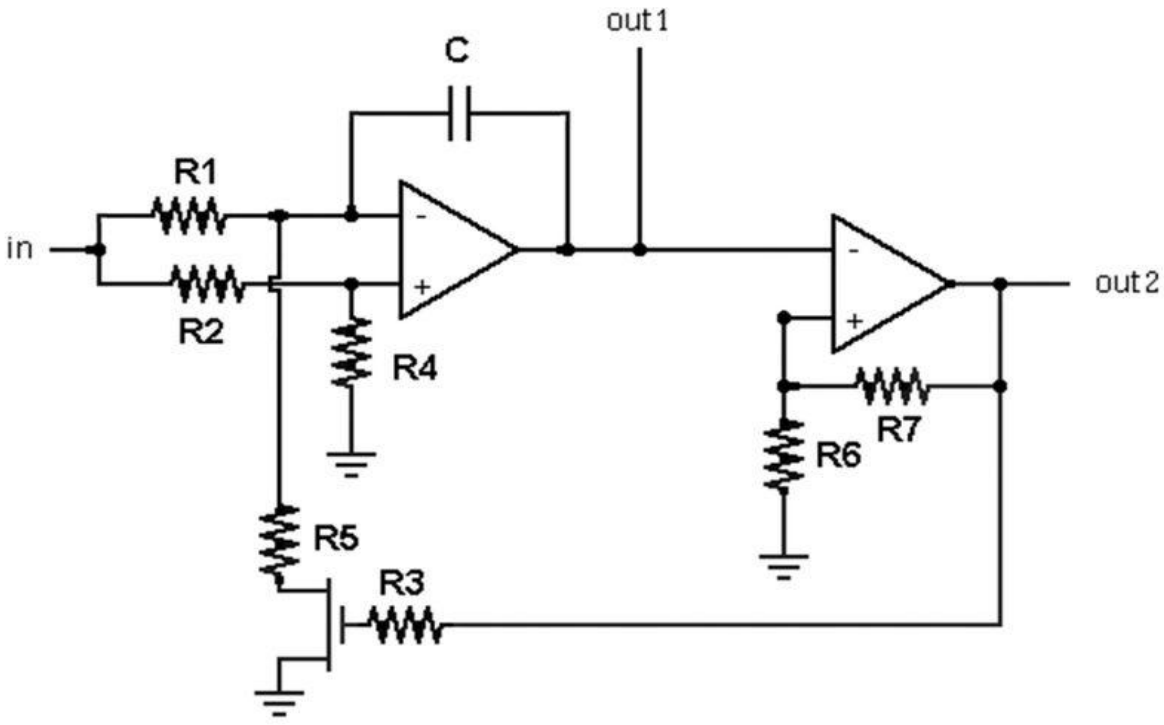


Fig.10.Voltage controlled oscillator schematic

Voltage controlled oscillators are the basic building blocks of many electronic systems especially phase-locked loops(PLL) and also, may be found in computer disk drives, wireless electronic equipment such as cellular phones, and other systems where oscillation frequency is controlled by an applied tuning voltage. Voltage oscillator components are almost an inevitable part of all the digital communication equipments. VCOs are used to produce local oscillator signals (LO) which, in turn are received by the transmitter and receiver systems for frequency up conversion and the down conversion respectively. Wireless subscriber communication units such as GSM use voltage oscillator circuits for generating the radio frequency signals. The VCOs are also employed in many synthesizer and the tunner circuits and one best example for it is television. A high frequency VCO is used in devices like processor clock distribution and generation, system synchronization and frequency synthesis [7].

Two important parameters in VCO design are sweep range and linearity.

a) The sweep range is the range of possible frequencies produced by produced by VCO control voltage. Various types of VCO's have been discovered so far.
b) Linearity correlates the changes in frequency or the VCO output to the change in the control voltage [8].

3.1.1 VOLTAGE CONTROLLED OSCILLATOR FREQUENCY

A VCO output frequency is stabilized with a Resonator. The Quality Factor (Q) of the Resonator needs to be higher for the lower close-in Phase Noise requirement. A Resonator can be very simple as an Inductor or complex as a Quartz Crystal. Some of the most popular

Resonator types with their accompanying typical Quality Factor,Q value in ascending order is as listed in the table below [9].

Resonator Type	*Quality Factor*
Inductor	20~150
Transmission Line	200~350
Coaxial	300~600
SAW	~10K
Crystal	20K~300K

3.2 TYPES OF VCO

On the basis of types of waveforms produced, there are two types of VCO:

A) Harmonic oscillator generates a sinusoidal waveform. It consists of an amplifier which provides adequate gain and a resonant circuit that feeds back signal to the input. Oscillation occurs at the resonant frequency where a positive gain arises around the loop. Some examples of harmonic oscillators are crystal oscillators and LC-tank oscillators.

B) Relaxation oscillator is able to generate sawtooth or triangular waveform. These can provide a wide range of operational frequency with minimum external components. Relaxation oscillator VCOs can have three topologies: grounded-capacitor VCOs,

emitter-coupled VCOs, and delay-based ring VCOs. The amount of time in each state depends on the time for a current to charge or discharge a capacitor.

Harmonic oscillators are better than relaxation oscillators in some following aspects:-

A) Frequency stability with respect to temperature, noise, and power supply.

B) Good accuracy for frequency control since the frequency is controlled by a crystal or tank circuit.

But, as per the implementation in monolithic IC, relaxation oscillator is better than harmonic oscillator.[10]

3.3 SIMULINK MODEL OF VCO AND OUTPUTS

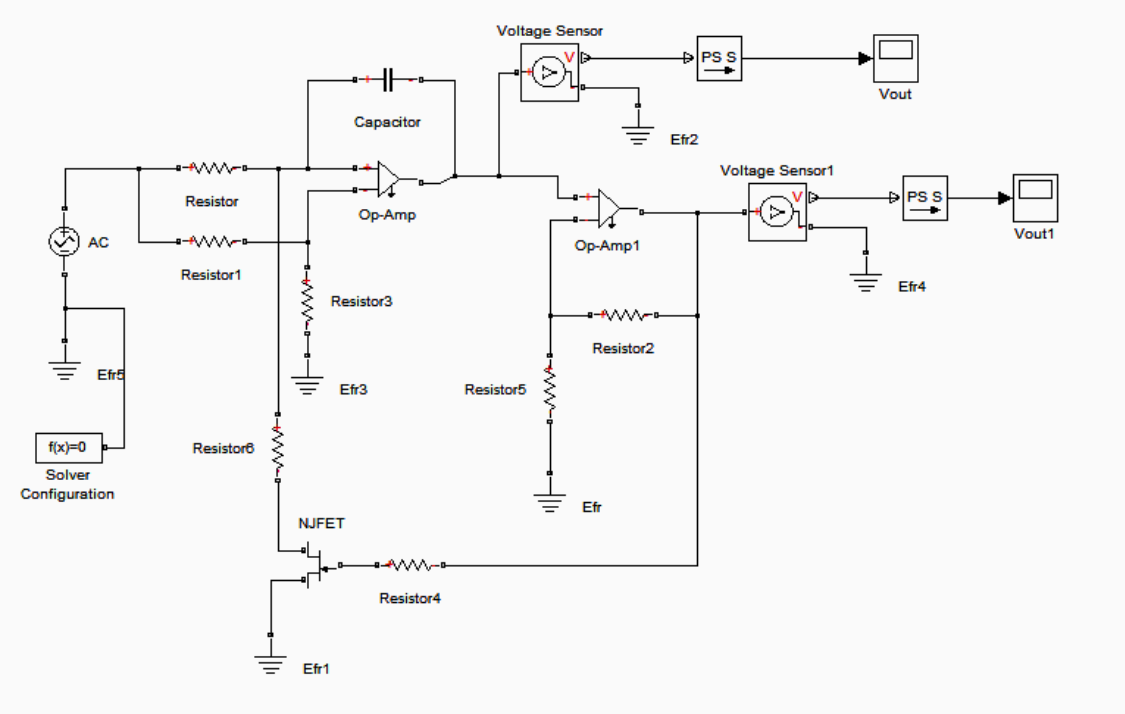


Fig.11.Simulink model of VCO in MATLAB

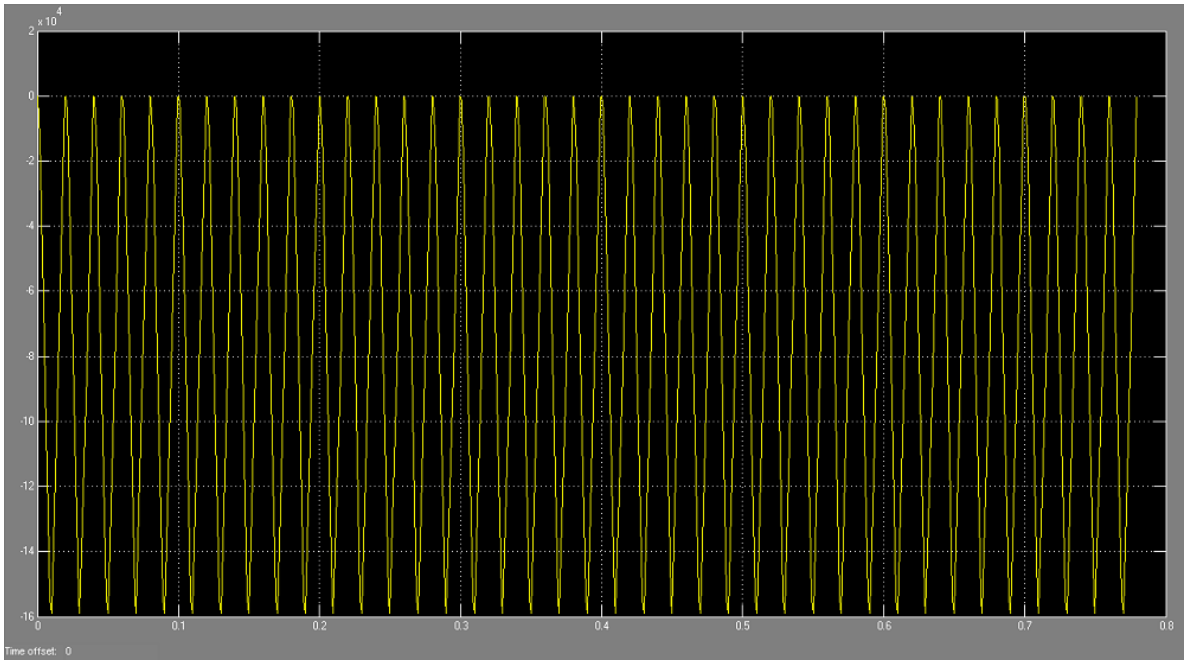


Fig.12.Output of Op-amp

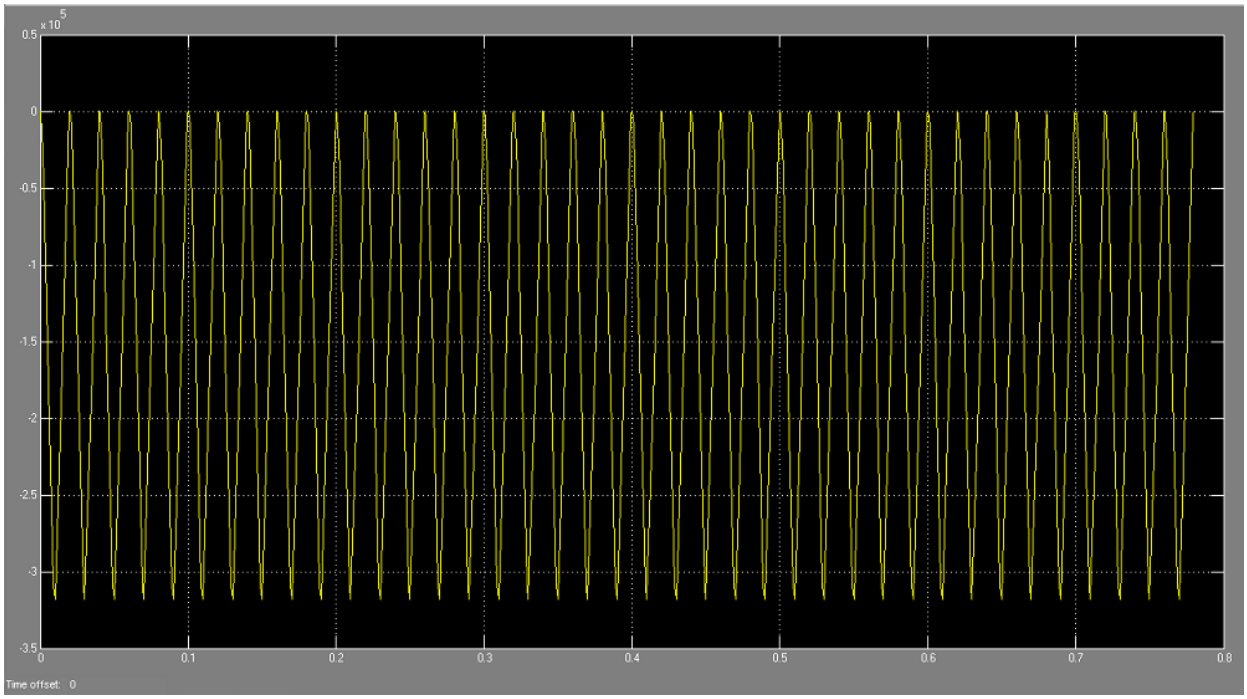


Fig.13.Output of Op-amp1

3.4 CONTROL OF FREQUENCY IN VCO

For a given control voltage, an LC oscillator can vary its frequency with the use of VCO. By varying the control voltage input, a reverse-biased semiconductor diode can change the frequency of an oscillator. For the manufacture of voltage controlled oscillator some special – purpose variable capacitance varactor-diodes are available with wide ranging values of capacitances [10].

For low- frequency VCOs, different methods of varying frequency are used, as altering the charging rate of a capacitor by means of a voltage controlled current source. The frequency of a ring oscillator is controlled by varying either the supply voltage or the capacitive loading on each stage.

3.5 APPLICATION OF VCO

A) Electronic jamming equipment.

B) Function generator.

C) Production of electronic music, for production of different types of noise.

D) Phase locked loop.

E) Frequency synthesizers, used in communication circuits.

3.5.1 ELECTRONIC JAMMING EQUIPMENTS

Electronic jamming is the transmission of electronic signal which disrupts the communication signal. Unintentional jamming occurs when an operator transmits the signal on a busy frequency without previous checking whether it is in use, or without being able to hear stations using the frequency. Another form of unintentional jamming occurs when the equipment

accidentally radiates a signal, such as a cable TV plant which accidentally emits on an aircraft emergency frequency. This concept can be used in wireless data networks to disrupt information flow. In order to prevent foreign radio stations in border areas from reaching the country, it is a common form of censorship in totalitarian countries [11].

3.5.2 FUNCTION GENERATOR

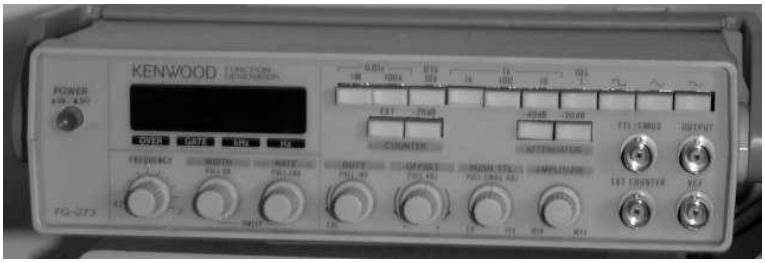


Fig.14.A typical low cost function generator

A function generator is an electronic test equipment or simple software used to generate electrical waveforms. This helps us to study and compare various waveforms of different electrical quantities. Function Generators are used in testing, development and the repairing of electronic equipment, for e.g. a signal source to introduce an error signal into a control loop, or to test amplifiers [12].

Analog function generators usually generate triangular waveforms. The triangle is generated by charging and discharging of capacitor repeatedly from a constant current source. This produces a linear ascending and a descending voltage ramp. As the output voltage reaches its upper and lower limits, the charging and discharging get reversed and by the using a comparator, a linear triangle wave is produce. By varying the current and size of the conductor we get waveforms of different frequency. Saw tooth waves can be produced by charging the capacitor slowly but when we use a diode over the current source to discharge the capacitor quickly, the polarity of the diode changes the polarity of the resulting saw tooth waveform, i.e.

fast rise and slow fall or slow rise and fast fall. A typical Function Generator can produce up to 20 MHz.

3.5.3 PHASE LOCK LOOP (PLL)

Fig.15.A simple phase lock loop

It is a control system which generates an output signal wave. The phase of the output signal wave is related to the phase of the input reference signal. It is an electronic circuit which consists of a variable frequency oscillator and a phase detector that compares the phase of signal coming from the oscillator to input signal. The signal from the phase detector is used to control the oscillator in a feedback loop. The circuit compares the phase of input analog signal with the phase of a signal derived from output oscillator and adjusts the frequency of its oscillator such that the phases should remain matched. Here frequency is the derivative of the phase. By keeping the input and output phase in lock step implies that keeping of input and output frequency in lock step as well. Since a phase locked loop can trace an input signal, it can produce an output signal for multiple input signals [13].

PLL is used in radio, telecommunication, computers and other electronic equipment.

A) Structure And Function Of PLL

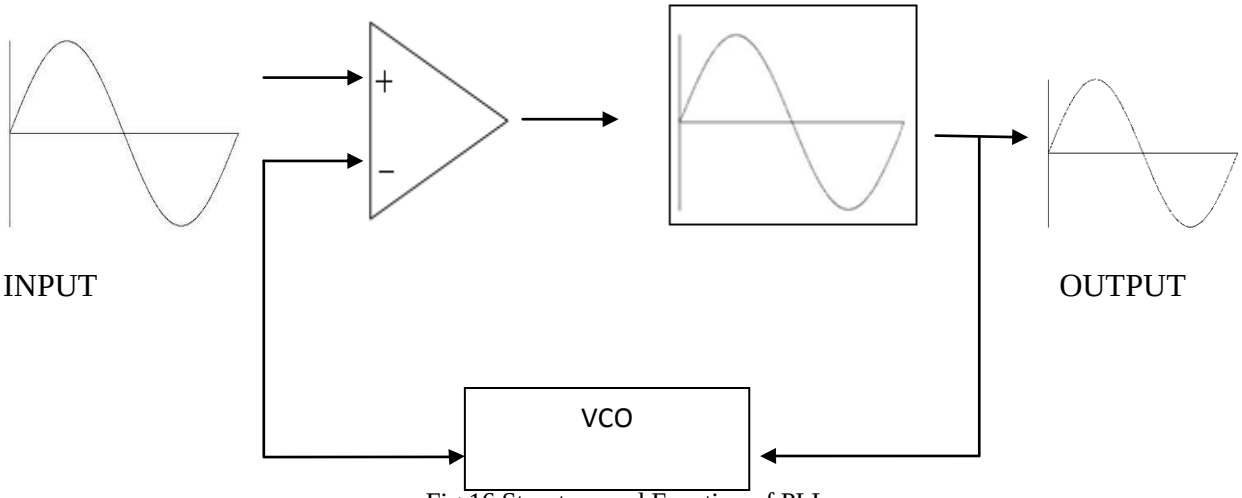


Fig.16.Structure and Function of PLL

Both analog and digital PLL consists of four elements:-

a) Phase detector

b) Low pass filter

c) Variable frequency oscillator

d) Feedback path

B) Applications Of PLL

Phase-locked loops are widely used for the synchronization purpose in various ways; in space communications for coherent demodulation and threshold extension, symbol synchronization and bit synchronization. PLL is also be used to demodulate frequency-modulated signals. In radio transmitters, phase lock loop (PLL) is used to synthesize new frequency value which is multiple of a reference frequency, with the same stability as that of reference frequency [13].

C) Other Applications Includes:

a) Demodulation of both FM and AM signals

b) Recovery of clock timing information from a data stream such as from a disk drive.

c) Recovery of small signals that otherwise would be lost in noise (lock-in amplifier).

d) DTMF decoders, modems, and other tone decoders, for remote control and telecommunications.

e) Clock multipliers in microprocessors which allows internal processor elements to run faster than external connections, while maintaining precise timing relationships

3.5.4 FREQUENCY SYNTHESIZER

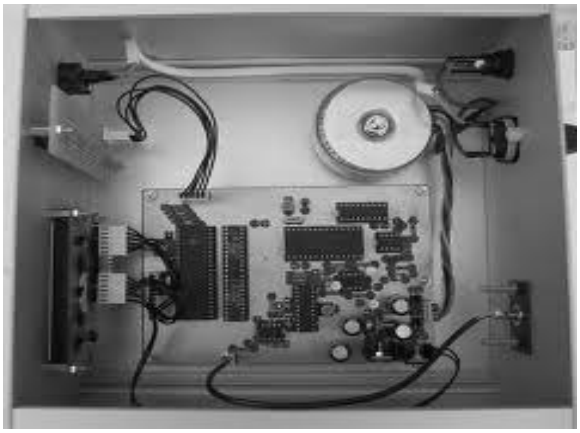


Fig.17.Frequency Synthesizer

A frequency synthesizer is an electronic system which is used for the generation of any range of frequencies from an oscillator. These are found in modern devices mobile like phones, radio receivers, CB radios, radiotelephones, walkie-talkies, GPS systems, satellite receivers, etc. A frequency synthesizer can combine frequency division, frequency multiplication, and frequency mixing operations to produce the desired output signal [14].

A) Types Of Frequency Synsthesizer

There are three types of synthesizer. The first and second types are found as stand-alone architecture: Direct Analog Synthesis (also known as mix-filter-divide architecture) and by comparison the modern Direct Digital Synthesizer (DDS). The third types are routinely used as communication system IC building-blocks: such as indirect digital (PLL) synthesizers including integer-N and fractional-N [14].

CHAPTER 4

4. ADC CONVERTER USING VCO

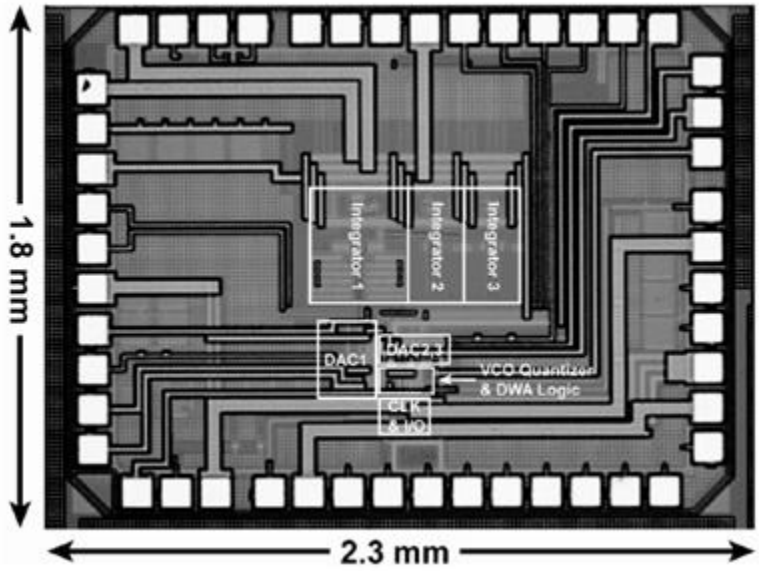


Fig.18.Die micrograph of the ADC implemented in 0.13µm CMOS. The total active area is 0.45 mm^2. DAC1 corresponds to the main NRZ feedback DAC, and DAC2 and DAC3 correspond to the minor-loop NRZ and RZ feedback DACs.

The VCO based ADC produces a single phase output whose frequency is varied proportionally to the average control voltage input. During a sampling clock period, the number of rising edges of the VCO output is recorded by means of a counter. A sampling register reads out the counter value at the end of every sampling period and resets the counter to zero. By this repetitive process the output bit stream gives quantized value of analog sampled signal .As the single phase VCO based ADC has limited resolution, multiphase VCO based ADCs are implemented [22].

Another disadvantage of single phase VCO based ADC is that the reset operation of counter takes time (delay), hence the resolution is limited even more .If a rising edge occurs near

close proximity to reset signal, then it may go undetected. Hence the noise shaping property is affected adversely [22].

The output phase of the VCO represents the average analog input during the sampling period and can be represented by following equation,

$$\Delta\phi_{out} = 2\pi \int_{T_{s1}}^{T_{s2}} (K_{vco} V_{in}(t) + f_{fr}) dt \quad [18] \qquad (6)$$

Where *Kvco* = voltage-to-frequency gain, *Ts*1, *Ts*2 = sampling times and f_{fr} = the free-running frequency of the VCO when V_{in}= 0.

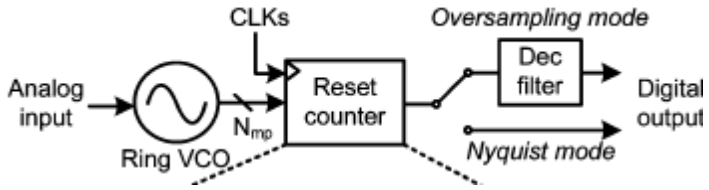


Fig.19.Figure showing VCO-based ADC including a decimation filter [23]

The output of the VCO is fed to a phase quantizer whose digital output corresponds to the analog input signal. The phase quantizer can be implemented using a counter which detects the rising edges of the VCO output, thereby quantizing the output phase by 2π. The digital output of the phase quantizer is further processed by a mapping circuit .The circuit stores the characteristics of the VCO and generates the digital code.

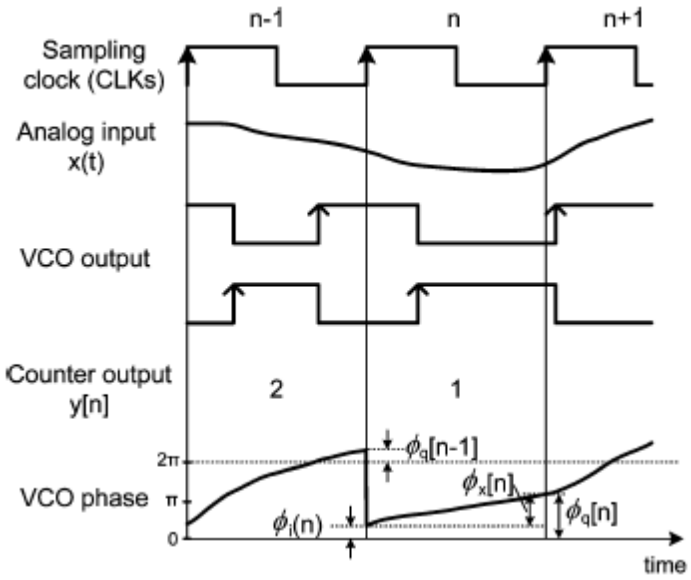


Fig.20.Characteristics of VCO based ADC. [23]

4.1 DESIGN OF INTEGRATOR BASED ADC IN MATLAB SIMULINK

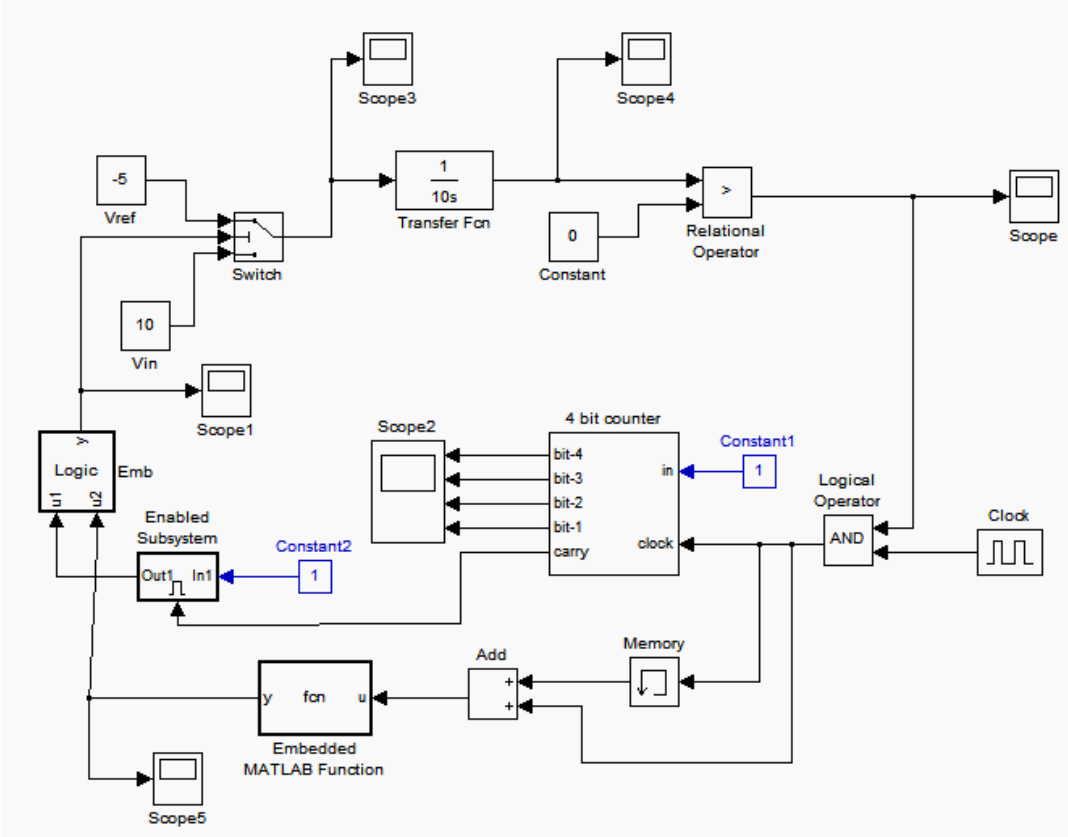


Fig.21. Simulink model of VCO based ADC

4.2 DESIGN OF 4-BIT COUNTER IN MATLAB SIMULINK

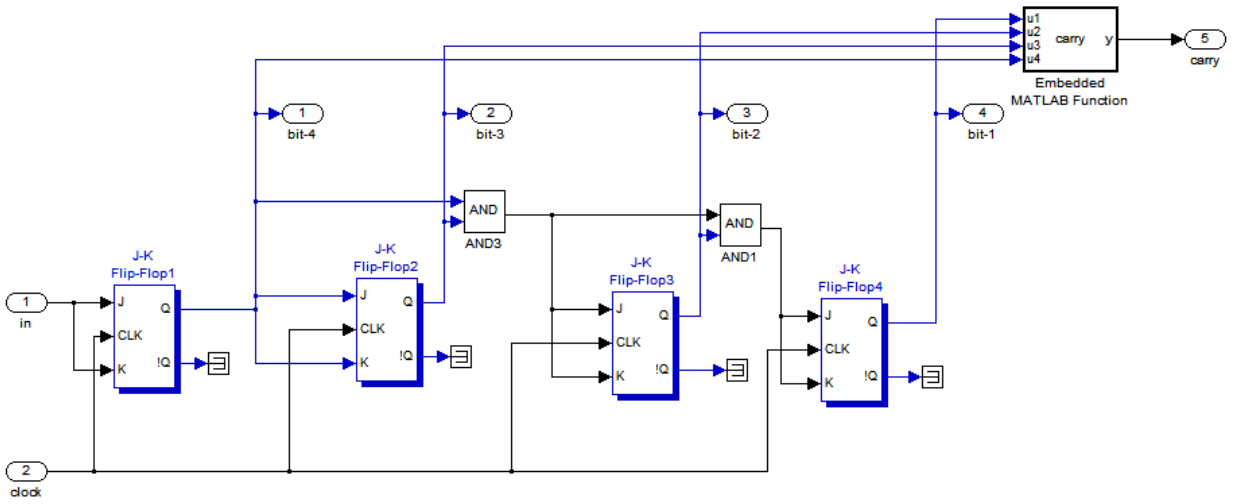


Fig.22.Simulink model of 4-bit counter

4.3 RESOLUTION OF VCO BASED ADC

Since the full scale of the ADC input is determined by the maximum frequency difference of the VCO output, the resolution can be represented by the following equation,

$$\begin{aligned} Resolution &= \log_2\left(\frac{f_{max}}{f_{sample}} - \frac{f_{min}}{f_{sample}}\right) \\ &= \log_2\left(\frac{f_{tuningrange}}{f_{sample}}\right) \end{aligned} \quad [18] \quad (7)$$

Where f_{max} and f_{min} are the maximum and minimum frequency of the VCO output and $f_{tuningrange}$ is the difference between these two values.

4.4 FIRST ORDER NOISE SHAPING PROPERTY OF VCO BASED ADC

The voltage controlled oscillator (VCO) has a differential output and the two counters that record the number of rising edges of each output. It is seen that the quantizer resolution increases if multiple output phases are available from the VCO. The VCO based architecture

discussed performs first order different or discrete time difference. Since quantization of phases is done by counting rising edges of VCO output during a sampling clock period to the value 2 π, it can be said that LSB(least significant bit) =2 π or 2 π/N(for multiphase VCO) .

Since the residual phase (i.e., quantization error) $\phi_q[n-1]$ of the previous sampling period inherently becomes the initial phase $\phi_i[n]$ of the next period, the VCO–quantizer output would be equal to [21] {Φ_x (instantaneous phase) + Φ_q (n-1) - Φ_q (n)}/2πfor multi phase, the above expression would be multiplied by N (= number Of VCO phase).

Transformation in z-domain gives

$$Y(z) = \frac{N_{\text{mp}}}{2\pi}\left(\Phi_x(z) + (z^{-1}-1)\Phi_q(z)\right). \quad [21] \qquad (8)$$

Where Y (z) =output from counter

For a general multiphase VCO with outputs, the counter quantizes the VCO phase by 2π/N . Hence, there is no correlation between the VCO and the sampling Clock quantization error can be assumed to be random .And it is uniformly distributed from 0 to 2π/N.

Here the quantization noise Φq (z) is simply shaped by a first order high pass filter with noise transfer function (NTF) of the form (z^{-1}-1) [20]. First order noise shaping of VCO based ADC (single phase) [17].

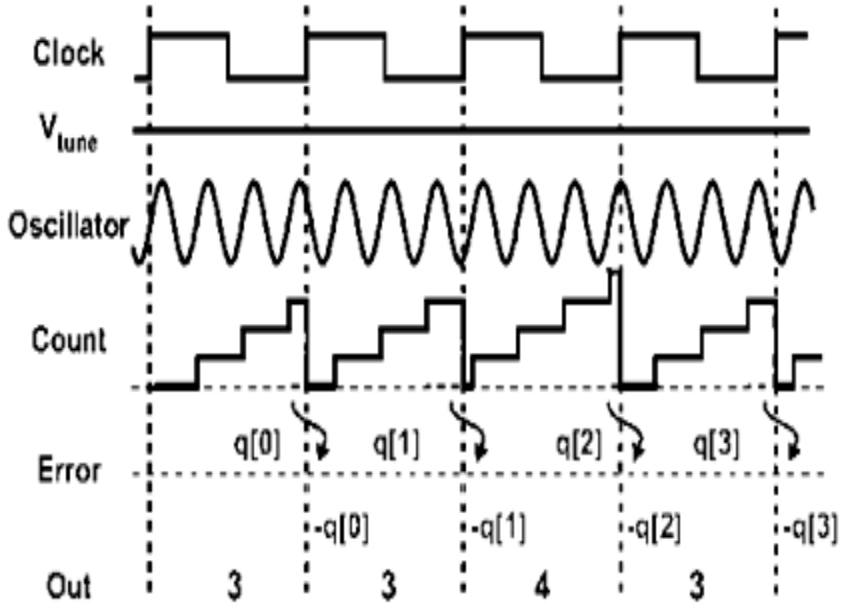


Fig.23.First-order noise shaping of a classical VCO based ADC Error[k]-q[k]-q[k-1].

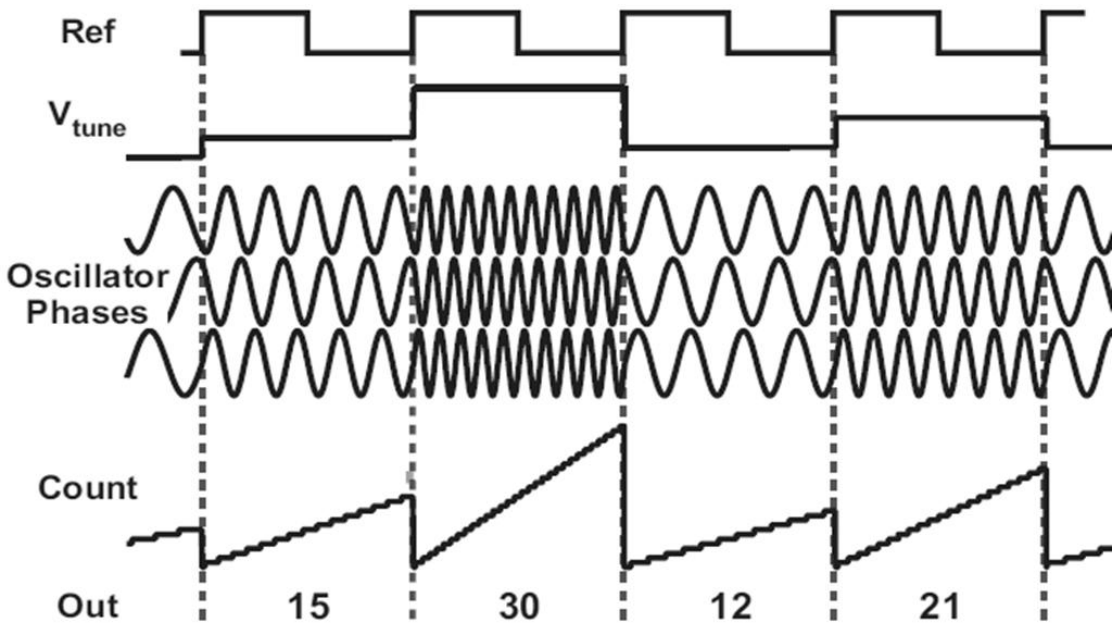
4.5 DRAWBACKS OF MULTI PHASE VCO BASED ADC

A) Reset pulse can coincide with Ring Clock Pulse (Asynchronous with Reset), the Noise shaping will disappear.[17]

B) Complex implementation for more quantization levels and for higher OSR.

4.5.1 MULTI-PHASE VCO BASED QUANTIZERS

$$f_{VCO}(max) = {}^{f_s}/_{2} \quad [17] \qquad (9)$$



[17]

Fig.24.Counting rising and falling edges

4.6 NON-IDEAL EFFECTS

Non-idealities such as jitter, VCO phase noise, Nonlinearity of VCO Tuning Characteristics, Mismatch of VCO delay cells and metastability of D- flip flops degrades the performance of the VCO-based ADC. Below all the nonlinearities are discussed briefly.

4.6.1 SAMPLING CLOCK JITTER

Jitter can be explained as deviation or displacement of some part of the pulse in a high-frequency digital signal. This deviation or displacement can be in terms of phase timing, amplitude or the width of the signal pulse. The major causes of jitter are electromagnetic interference and interference with other signals. Jitter can be easily seen like the flickering of the monitor, introduction of other undesired noises and loss of transmitted data. There are three different types of jitter:-

a) Random jitter

b) Deterministic jitter

c) Total jitter

Random jitter is also known as Gaussian jitter is an unpredictable electronic timing noise. Random jitter follows a Gaussian distribution because most noise caused due to thermal noise, which have a Gaussian distribution.

Deterministic jitter is a type of clock timing jitter which is predictable and reproducible. All peak to peak values are bounded and it is easy to determine and observed the bounded values. Example of bounded jitter is periodic jitter. The major difference between random and deterministic jitter is, random jitter is unbounded whereas deterministic jitter is bounded.

Total jitter is the combination of random and deterministic jitter.

$T = D_{peak\ to\ peak} + 2*n*R_{rms}$, in which the value of *n* is based on the bit error rate.

The sampling clock in VCO based ADC is used for sampling the input signal. Therefore, sampling clock jitter is divided into two parts: one is sampling uncertainty caused by the absolute jitter (which is also called as aperture jitter) and the second is the error in the integration time caused by the periodic jitter. Sampling clocks with and without jitter is shown below. Where the input signal is *x(t)*.

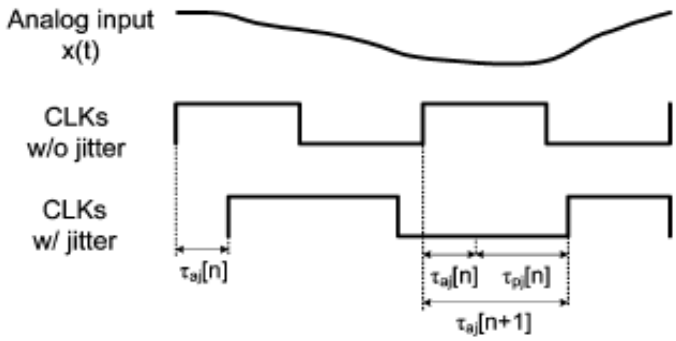


Fig.25.Sampling clock with and without jitter

It can be observe that effect of the jitter on VCO based ADC is same as that of conventional voltage-based ADC. It is seen that VCO with high free running frequency consist of larger phase error as compared to low free running frequency for the same tuning range and period jitter. Hence, to reduce the periodic jitter, the free running frequency should be minimized.

4.6.2 VCO PHASE NOISE

The short term random frequency fluctuation in a signal is used for describing phase noise. Frequency stability is a measure of the degree by which an oscillator maintains the same value of the frequency over a particular time. This can be done in various different ways.

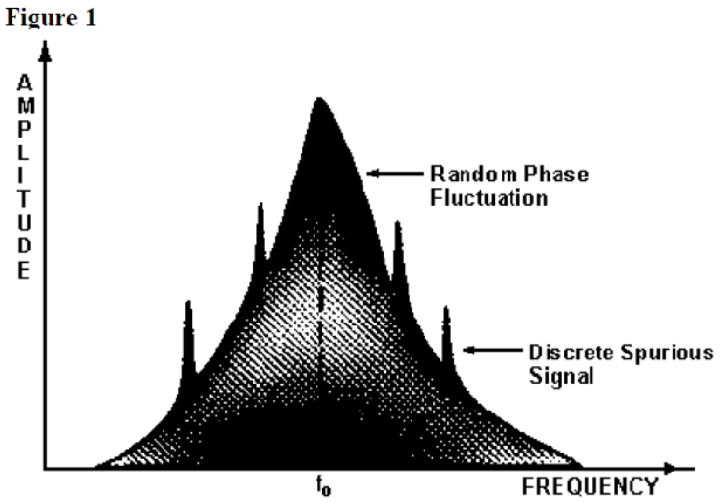


Fig.26.Spectrum analyzer display of phase noise.

The phase noise generated by VCO is determined by the Q factor of resonator and varactor diode, the supply power noise and external tuning voltage noise.

The noise contribution made by last two can be minimized by careful choice of the power supplies. Hence, the phase noise of the VCO is therefore determined primarily by the overall Q factor of the circuit. In order to design a circuit with high Q factor, the tuning bandwidth must be made to a lower value. Hence, a VCO designed for low phase noise performance will have a smaller tuning range.

A) Ways To Minimize Noise

a) Power supply voltage and tuning voltage returns must be connected to printed circuit board (it is used for mechanical support and electrically connect electronic component using conductive pathways). The VCO ground plane must be same as that of printed circuit board and hence all VCO pins are connected directly to the board ground plane.

b) Adequate radio frequency grounding is required. Decoupling capacitor chips are connected between the supply voltage and the ground.

c) Low noise power supplies should be used like DC batteries which gives an overall good performance.

d) Output must be correctly terminated with load impedance.

e) Connections to the tuning port must be as short as possible and it must be well shielded, screened and decoupled to prevent the VCO from external noise sources.

4.6.3 NONLINEARITY OF VCO TUNING CHARACTERISTICS

When VCO has nonlinearity in its tuning curve, the harmonic *spurs* are generated similar to general voltage-based ADC with nonlinearity. Since, due to the absence of sample and hold circuit in the VCO-based ADC, the harmonics are eliminated as sinc filtered just like the signal. It should be noted that due to such filtering the intermodulation product is much larger than the harmonic spurs.

4.6.4 MISMATCH OF VCO DELAY CELLS

The delay cells leads to spurious peaks in the output frequency spectrum of the output signal. Any delay mismatch between the delay cells affects the resolution of the circuit, its accuracy of measurement. Mismatch of the VCO delay cells introduce error in the propagation delay and adds phase error to the phase-domain input signal. Due to interconnection and variation in process leads to mismatch of delay cell which results in timing uncertainty in the signal leads to introduction of jitter. A multiphase ring voltage controlled oscillator with mismatch is shown below

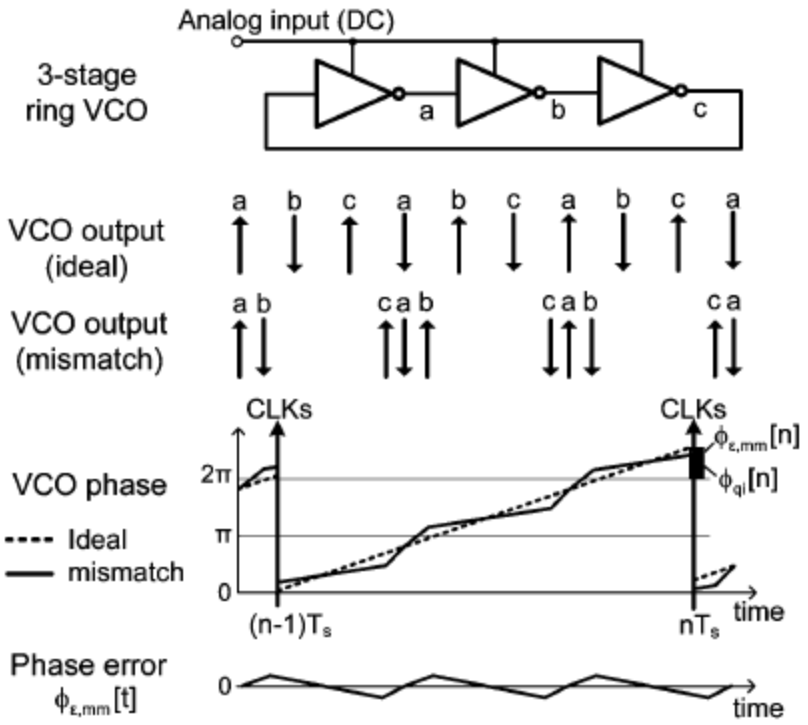


Fig.27.A Three-stage ring VCO and effect of VCO mismatch in phase diagram, where $\Phi_{e,mm[n]}$ is called phase diagram.

To avoid this problem less number of VCO delay cells are required, that means VCO operates at high speed. There is one more way to reduce the VCO mismatch is to control the free running frequency. The harmonic spurs can also be removed free running frequency is moved away from the desired frequency.

4.6.5 METASTABILITY OF D-FLIP FLOPS (DFF)

When there are set up and hold time violation in any flip flop, it enters in a position where we can easily predict the output this state is called metastability state, which is also knows as quasi stable state. After the end of this state the flip flop enters into either 0 or 1 state. Whenever the flip flops are in metastable state the output will oscillate between 0 and 1.

A) Causes In Which Metastability Occurs

a) When we using sinusoidal voltage as input voltage

b) When the skew or slew of the clock is too much

c) When the two domains interfacing each other operates in same or different frequency but in different phase.

Hence, from above details we conclude that metastablity is not desired from any circuits because of its oscillating output. D flip flops are used to get the close to desired value or the optimum value during metastability window. Below figure showing the effect of DFF metastbility.

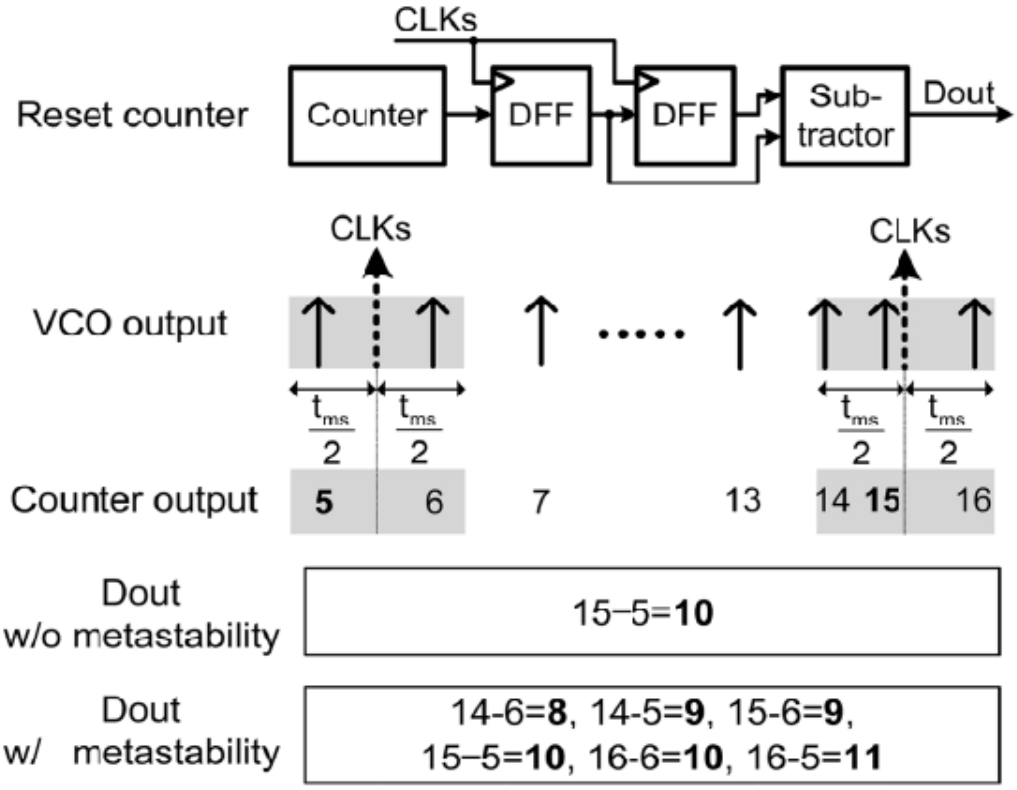


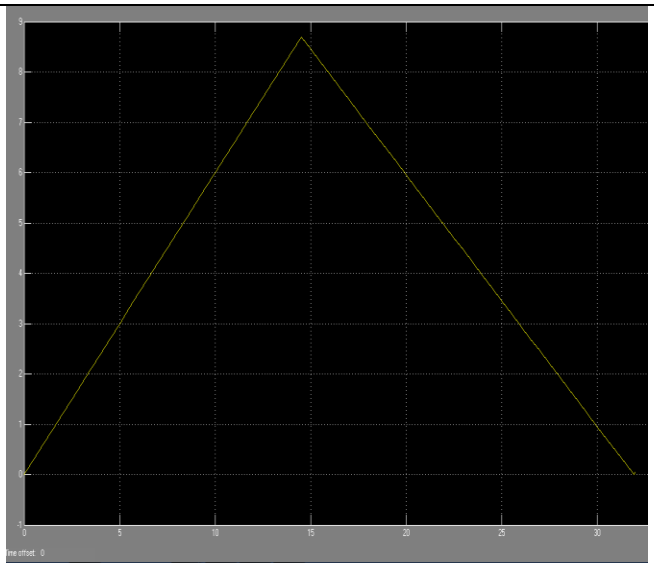
Fig.28.Effect of DFF metastability in timing diagram

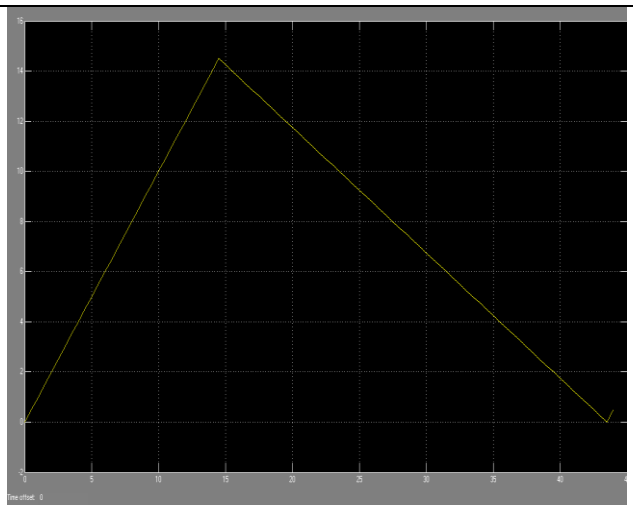
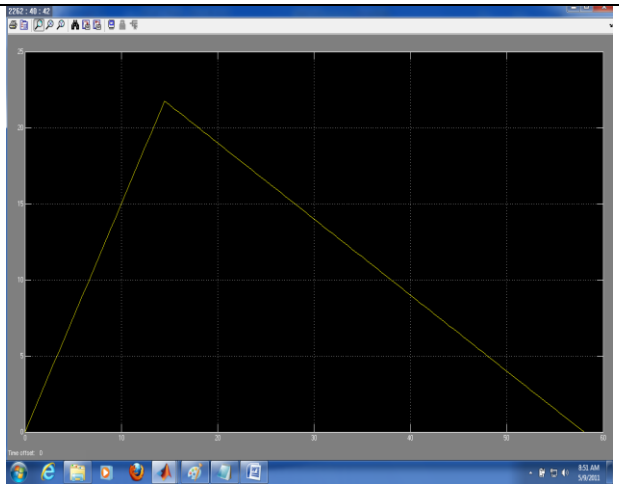
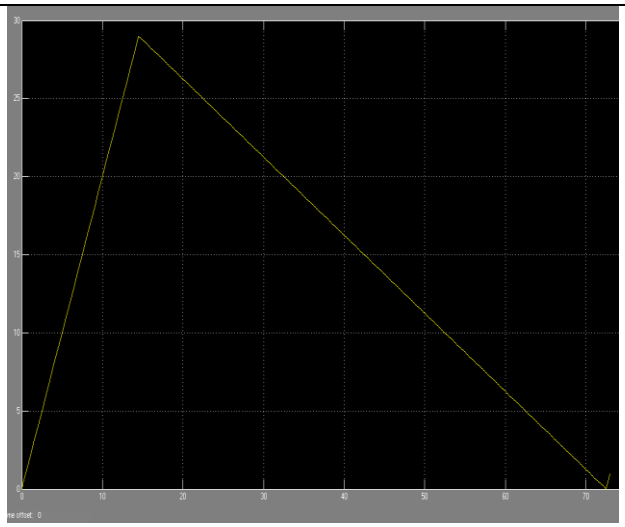
The abovementioned discussion shows that the errors are uniformly distributed in the system. However, in practical cases, errors have a particular biased distribution rather than uniform distribution.

RESULTS AND DISCUSSIONS

A simplified model of dual slope integrating ADC using an integrator (implementing transfer function of the integrator), comparator, clock, synchronous counter and a switch is simulated in matlab simulink. For undesired complexities the ADC has been designed to operate only for one cycle avoiding the use of a complicated microprocessor or dedicated control logic. Here the switch is operated on by an additional single bit as carry bit incorporated along with the synchronous 4 bit counter.

For different input voltages different plot of input voltage Vs time are shown below for reference voltage is equal to -5 volt:-

SL. NO.	INPUT VOLTAGES	PLOTS
1.	V_{IN} = 6V	

2.	V_{IN} = 10V	
3.	V_{IN} = 15V	
4.	V_{IN} = 20V	

CONCLUSION

The study of dual slope ADCs or also known as the integrating was done and the simulink model was built using MATLAB. The simulink model was studied under various input voltage by keeprng the same reference voltage. The voltage controlled oscillator model and its output waveform was studied in MATLAB simulink. Hence, a VCO based ADC is a time based architecture which offers an inherent noise shaping property, high sampling rate and digital implementation. In this paper the non linearties like jitter, metastability, phase noise and tuning characteristics were also analyzed and discussed.

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