Automatic telephone answering machine

A thesis submitted in partial fulfillment of the
requirement for the degree of

Bachelor of technology
In
Electronics & Instrumentation Engineering

by

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Roll No- 10607029
&
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Under the guidance of

Prof K.K. Mahapatra

Department of Electronics and communication Engineering
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CERTIFICATE

This is to certify that the thesis entitled "**Automatic Telephone Answering Machine**" submitted by ASHUTOSH BHUYAN, Final year student of Electronics & Instrumentation Engineering, Roll No: 10607029 and SATYANARAYAN BISHOYI, Final year student of Electronics & Instrumentation Engineering, Roll No: 10607018 in partial fulfilment of the requirements for the award of B.Tech degree at NATIONAL INSTITUTE OF TECHNOLOGY, ROURKELA is a bonafide work carried out by them under my supervision and guidance.

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other university/institute for the award of any degree or diploma.

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ABSTRACT

An automatic telephone answering machine or system is an electronic device that answers automatically to an incoming telephone call and plays a prerecorded message and is capable of recording a message the caller want to leave. These systems include message recording system having remote acess to message playback, automatic dialing, equipment to receive an alarm, automatic data entry-answering systems and other common telephone devices being used along with modem equipments. The microcontroller typically controls a number of peripherals, components of the answering machine such as an LCD or LED display, an indicator light for recording and playback options, a DTMF receiver and an audio controller.

A telephone answering machine must be capble of being remotely activated consisting of:

- A switch deciding the mode of operation either automatic or normal mode.
- Provison for receiving the calls automatically when in automatic mode.
- Provison for recording the message to be deliverd to the incoming user and also to record his mesage
- Storage for the message
- Microcontoller to deliver control signal as per the mode of operation

Commonly used telephone answering devices comprises of a number of features which allow a user to examine the presence of a call, seize calls, play back recorded voice messages, record an announcement etc. Triggering of a telephone answering machine done by counting the incoming ring signals and when the count surpass a preset number set by the user. The machine is programmed in such a way that if the user does not attain his telephone within a specified time period which is the function of number of ring signals, the call is automaticlly answered and a message is palyed back to the caller as well as asks him to leave a message.

KEY WORDS:

Answering machine, Answering system, Speech compression, ADPCM, Encoding, Decoding

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1

INTRODUCTION

Contents:

1.1 Definition
1.2 History
1.3 Components
1.4 Operation

With the development of new technologies different additional features are being added to the basic telephone. These functions include a wide range of new application which allows automation also. Starting from shortening of dialing time to answer a call automatically are some of the recent features developed. In the world of personal telecommunication this automatic answering machine has become very popular and worldwide. It is becoming the part of every house hold for communication basically to receive message in the absence of the user of the machine.

1.1 Definition:

An automatic telephone answering machine can be identified as an electronic device which has the basic feature of answering a call in the absence of the receiving user. It has some added features like plying back a pre-recorded audio message to the caller. If the caller wants to leave a voice message he can do so by accepting the option to record a message. The answering machine or system can be described as data processing system. It can be connected to multiple telephone lines. There might be also additional features like connect to another predefined number and forward the recorded message to the present location of receiving end user.

1.2 History:

Telegraphone, the first realistic telephonic setup for magnetic sound recording and reproduction, was patented in 1898 by Valdemar Poulsen, a Danish telephone engineer. It was used to record the telephonic conversations. Magnetizing a wire with different field strength was the principle. We can use this magnetized wire to play back the sound.

First Automatic Answering Machine is invented by Mr. Willy Müller in 1935. This machine was a three-foot-tall machine trendy with Orthodox Jews and they were not allowed to answer the phone on the rest days.

In 1960, the **Ansafone**, was invented by Dr. Kazuo Hashimoto. It is the first answering machine to be sold in USA.

The modern telephone answering device we are familiar with was first introduced by CASIO communications. These are the first commercially viable answering machines.

In 1971, Phone Mate brought up with one of the first commercially feasible answering machines. The Model-400 weighs around 10 pounds, able to screen calls and can hold 20 messages on a reel-to-reel tape. There is also provision for private message retrieval by using an earphone.

Dr. Kazuo Hashimoto of Japan invented the first **Digital telephone answering machine** in mid-1983. The first ever voice mail system was invented by Gordon Matthews.

1.3 Components:

The ATAM device automatically answers an incoming telephone call, plays a prerecorded message and records a message that the caller leaves. These systems include message recording system having;

- Remote acess message playback
- Automatic dial up alarm receiving equipment
- Automatic telephone message recording equipment
- Automatic telephone call forwarding equipment
- Automatic answering data entry systems
- The microcontroller to control a multiple number of peripherals, and basic components of an answering machine
- Peripherals like an LCD or LED display, an indicator light for recording and playback options, a DTMF receiver and an audio controller.

1.4 Operation:

The basic function performed by the answering machines is to automatically answer calls coming from an incoming telephone line. In the absence of user of the machine, when the call is unanswered up to a certain time interval, a pre-recorded outgoing message is being played to the calling party. Then it asks for any message to the calling party and records the message he leaves.

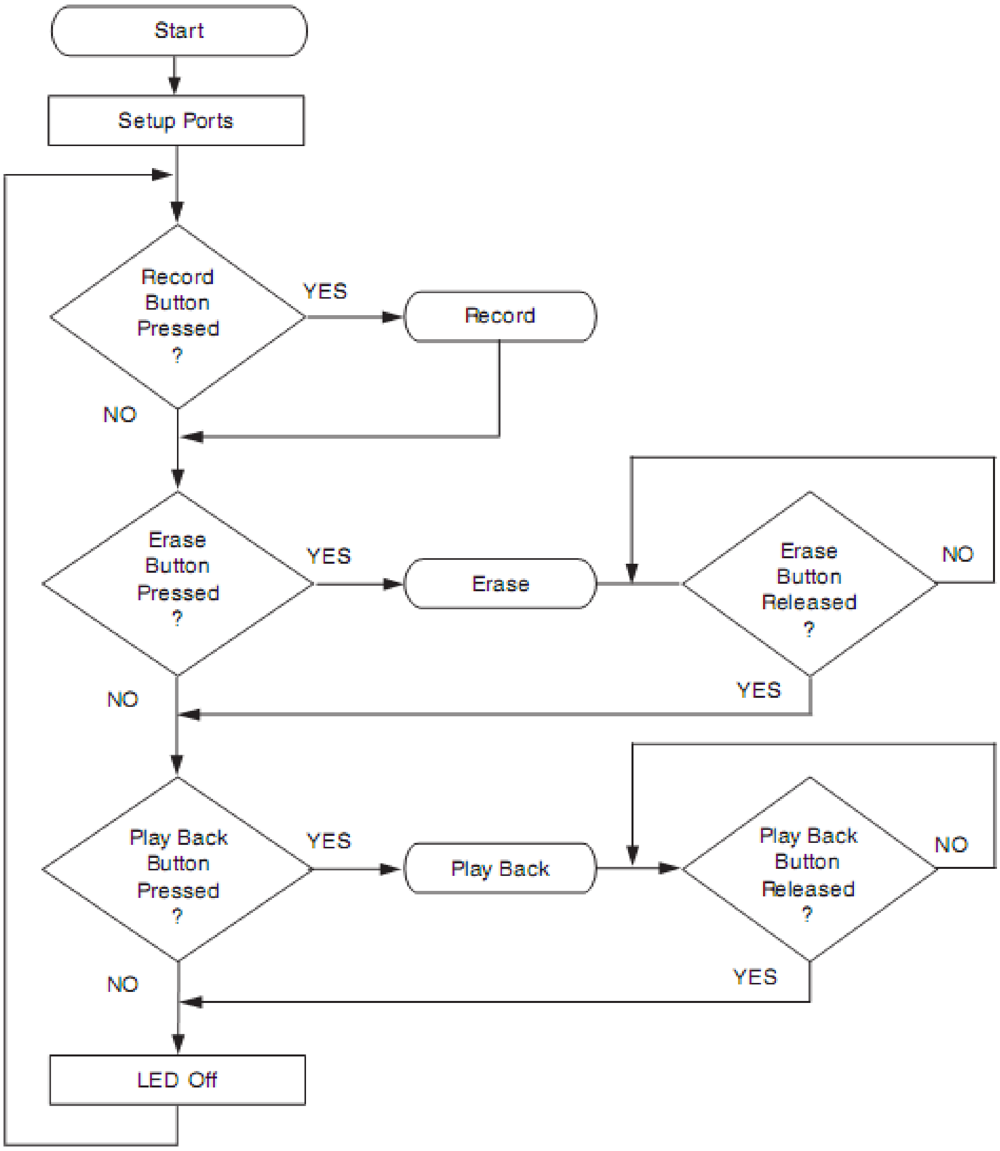


Figure:1 (flow chart of complete process)

A typical telephone answering machine is a separate device connected to a telephone line. This type of answering machines usually include circuitry for the detection of a ringing signal on the telephone line signifying the existence of an incoming call. It answers the call by taking the line off-hook, plays an outgoing message, records an incoming message if any, and hangs up the line in order to respond to subsequent telephone calls.

A digital answering machine answesr a telephone call and stores voice messages in an internal memory. The need of magnetic tape in analog domain is eliminated due to the use of an internal digital memory (RAM or ROM). As the mechanical parts required to transport the tape is discarded the digital answering machines are more reliable. Also these require less physical space with better noise immunity and audio quality. The flexibility of quick access to the specific message when a multiple messages are being received is there in digital machines. In digital answering machines, fixed data compression rate is being followed for speech recording.

In this thesis we will start with the techniques of speech compression and will elaborate the discussion on ADPCM (adaptive differential pulse code modulation). The algorithms for encoding and decoding process are being presented in form of block diagram. Then different parts of actual hardware are discussed thoroughly which includes input stage amplifer, microcontroller, output stage amplifiers, filters, microphone, speaker and display device LCD etc. Then the simulation results for the encoding and decoding of audio signal is given followed by the LCD interfacing and ADC conversions.

2

Audio Compression

Contents:

2.1 Introduction
2.2 Analog & Digital audio systems
2.3 Digital audio compression
2.4 ADPCM
    2.4.1 Definition
    2.4.2 Encoding & Decoding
    2.4.3 Algorithm

2.1 Introduction:

This section describes a process which reduces the data rate and storage size of digital audio signals. This technique allows efficient transmission of data. Different forms of audio compression techniques allow a range of encoder and decoder complexity, compressed audio quality, and differing amounts of data compression. We will start discussing about digital audio data followed by one technique for audio compression known as Adaptive differential pulse code modulation (ADPCM).

2.2 Analog & Digital Audio Systems:

Digital audio has become very important at present time due to its usefulness in the recording, manipulation, mass-production, and sound distribution. The cost of distribution has reduced remarkably by representing audio as data files rather than physical objects.

In an analog audio system, transducers like microphone is used to convert physical waveform generated in air to an electrical form which can be stored or transmitted. Again the electrical signal is passed through another output device like a loud speaker through amplification process to regenerate the sound. Throughout the entire process the fundamental wave characteristics remain unchanged. But due to the circuitry and devices involved the noise and distortion can't be avoided. In order to have high noise immunity, better stability and data reproducibility we go for digital audio system which allows efficient implementation of many audio processing.

Analog to digital data conversion process starts with sampling process where data is picked at regular & discrete intervals of time and then quantized into a discrete number of evenly spaced levels. The digital audio data is represented as a set of binary values which is stored as either of electronic, magnetic or optical signal. These digital waveforms then encoded for better error correction. The discrete time and level of the binary signal facilitate the analog signal to be recreated by a decoder.

2.3 Digital audio compression:

Audio compression is a technique of data compression, in which requirement of transmission bandwidth and memory space is reduced for digital audio streams. For the same software level implementation of various algorithms are done as audio codec. By this the amount of information required to regenerate the original data is reduced. The compression might be lossy or lossless. The audio quality might be reduced to a small extent but it is preponderated by the cost reduction due to less size and bandwidth requirement and increase in efficiency level.

Depending upon the compressed audio quality, complexity of encoder and decoder and the amount of data compression for desired application different techniques have been suggested. Some of the techniques are,

- PCM/DPCM/ADPCM
- µ-law audio compression (low complexity, low compression, medium audio quality algorithm)
- MPEG (motion picture experts group) audio compression (High complexity, high compression, high quality algorithm)

The ADPCM and µ-law audio compression techniques are lossy audio compressions which achieves far greater compression than lossless compression by discarding less-critical data.

MPEG audio compression is lossless audio compression which produces almost exact replica of the original audio stream Compression ratios are comparable to those of generic lossless data compression (about 50–60% of original size) and significantly less than for lossy compression, which usually yield 5–20% of original size.

In the following subsection, ADPCM algorithm is discussed in brief which technique is being used for the encoding voice signal in the desired telephonic answering machine.

2.4 ADPCM:

2.4.1 Definition

ADPCM (adaptive differential pulse code modulation) is a form of basic pulse code modulation along with some additional functionalities based on the signal sample prediction.

PCM represnts the input analog signal in a digital domain by capturing samples regularly at definite intervals. Then the collected set of sample magnitudes are quntaized into different predefined numeric levels (e.g. binary sequence). For digital audio and video storage and transmission thruough a computer PCM technique is granted as a standard. But the bit rate required in this case is very high. So another technique DPCM (differential pulse code modulaion) is suggested.

In case of DPCM, the input can either be an analog signal or a digital signal. When a continuous-time analog signal is the input, it must be sampled first to have a discrete-time signal as the input to the DPCM encoder. The complete compression process is carried by encoder-decoder pair. In encoder the diference between two consecutive quantized sample values are taken and output to the decoder which is responsible for faithful regeneration of original audio data.

ADPCM is the form of DPCM where the quantization step size is varied which allows further reduction of the bandwidth requirement for a given signal-to-noise ratio. This is the most widely used digital compression technique in speech compression in telecommunication industry. It is a lossy audio compression technique having low bit rate and less complex calculation for encoding and decoding.

In general ADPCM is used to compress an 8 kHz, 8-bit signal, with an inbuilt flow rate of 64 Kbit/s. The flow rate is reduced to 25% of the original signal i.e. to 16 Kbit/s using only 2 bits and being encoded at highest compression ratio. Similarly using 4-bit coding, 32 Kbit/s flow rate is achievable i.e. 50% of the original maintaining the quality of the signal as per the desired application. The on-chip timer/counter of a microcontroller is used to create a Pulse-Width Modulated (PWM) output signal, which is then passed through a simple, external filter for decoding the encoded data and to regenerate the original audio data by connecting to speakers. The block diagram for the process is shown in the figure 2.

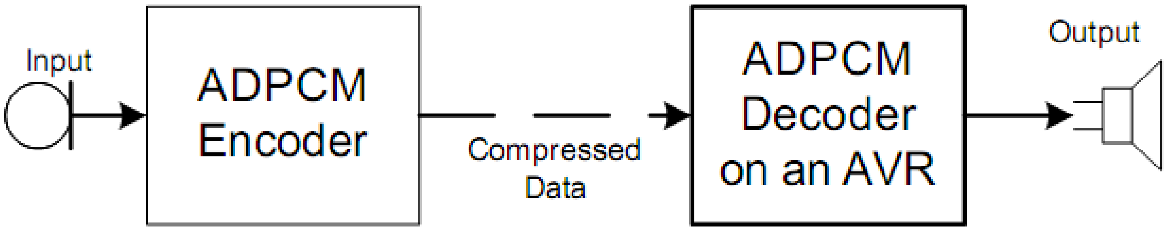


Figure: 2 (Block diagram of encoder decoder pair)

2.4.2 Encoding & Decoding

The ADPCM encoder works as follows. An estimate of sample is reconstructed by taking the difference between two consecutive samples each time an input speech sample is accepted. A valid pulse code is being assigned each of the quantized difference values. The main objective is to reduce the range of quantizer levels. They can be spaced closer by quantizing the difference values instead the original signal as there is smaller amplitude swing. This leads to reduction of quantizer noise. Hence with increasing sampling frequency the execution of the algorithm become more efficient.

The working of the ADPCM decoder is explained as follows. Mapping for each of the input pulse code is done with a sequence of predefined quantizer levels. The particular level with which the pulse is matched is then added to the current sum to produce an estimate to the original speech sample

The algorithm is adaptive because the quantizer levels change with each incoming speech sample. The quantizer level size depends upon the difference values of two consecutive signals. Thus, the algorithm should be designed in such a way that it should implicate the response specification of quantizer with changing values of differences.

2.4.3 Algorithm

Encoding process:

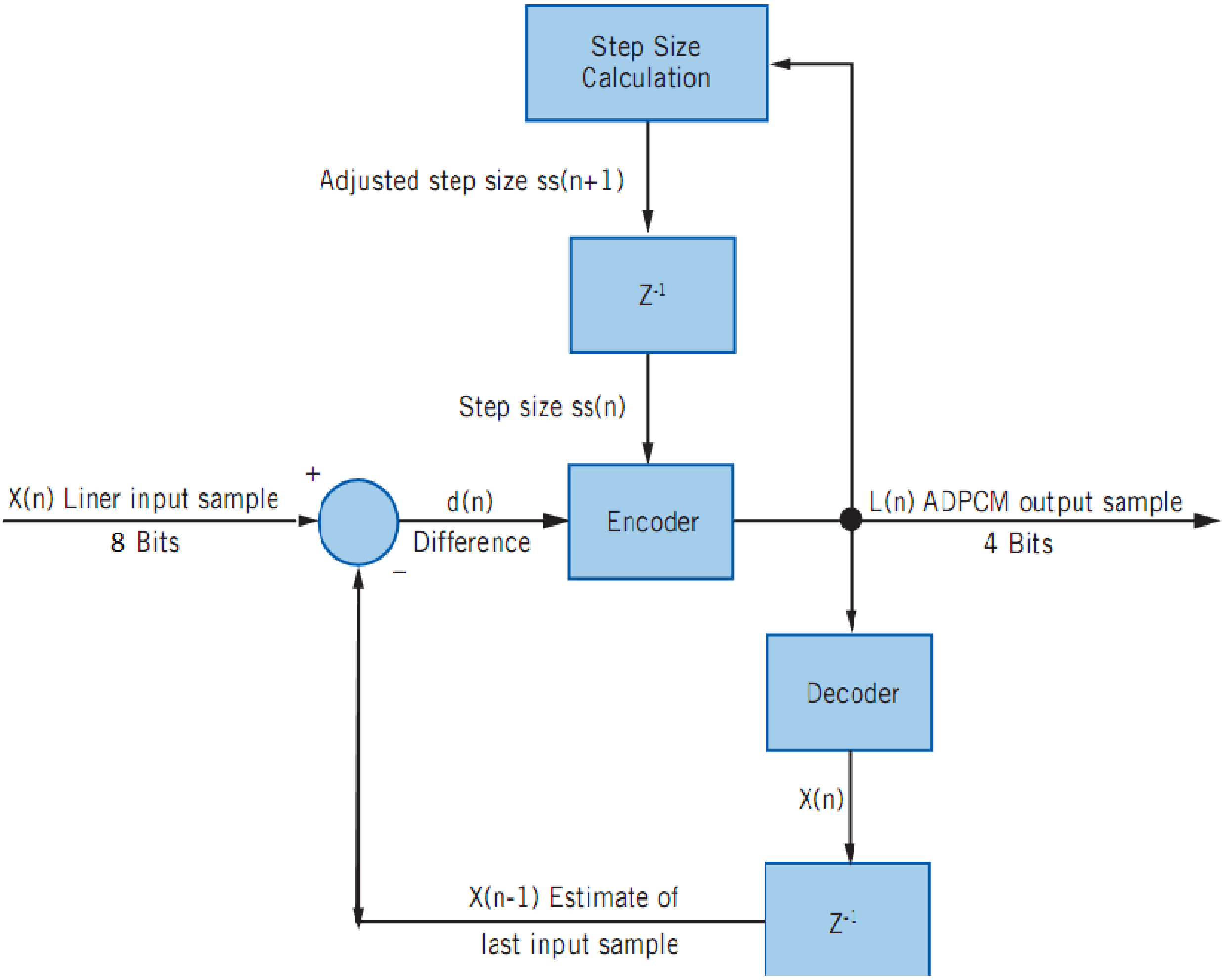


Figure: 3 (Block diagram of encodeing process)

Figure: 3 represents the block diagram of the encoding process using ADPCM algorithm. X(n), a linear input sample and the estimate of its previous input X(n-1) are compared. The encoder block is provided with the difference d(n), calculated by the compartor block and the present step size ss(n). The logic for the encoding preocess is discussed below which produces an ADPCM output sample(coded as 4-bit). Next step size ss(n+1) is updated using the output sample and is input to the decoder inorder to calculate the linear estimate of the original input sample.

Decoding process:

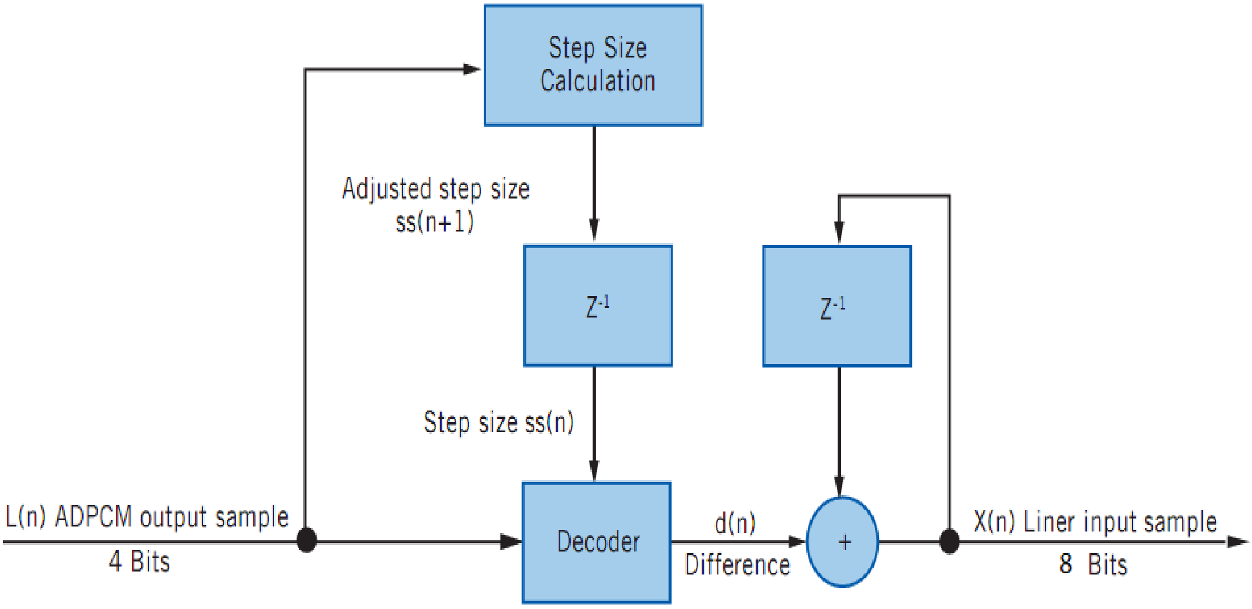


Figure: 4 (Block diagram of decoding process)

Above figure represents the block diagram of the ADPCM decoding process. An ADPCM sample is given as input to the decoder. Then the decoder calculates the difference between the expected output and prior linear output estimate. The difference is summed up with the previous estimate to generate the linear output estimate. To calculate the next step size estimate the input ADPCM sample is also given to the step size calculator.

Stepsize Calculation:

For both the encoding and decoding process, the ADPCM algorithm adjusts the quantizer step size based on the most recent ADPCM value. The step size for the next sample, n+1, is calculated with a two-stage lookup table. First the magnitude of the ADPCM code is used as an index to look up an adjustment factor as shown in indexTable. Then that adjustment factor is used to move an index pointer in stepsizeTable given in table-1. Values greater than 3 will increase the step size. Values less than 4 decrease the step size . The block diagram of stepsize adaption is given in Figure 5.

4-Bit ADPCM value	0	1	2	3	4	5	6	7	0	-1	-2	-3	-4	-5	-6	-7
Index	-1	-1	-1	-1	2	4	6	8	-1	-1	-1	-1	2	4	6	8

Table : 1(Index values for 4-bit Adpcm value)

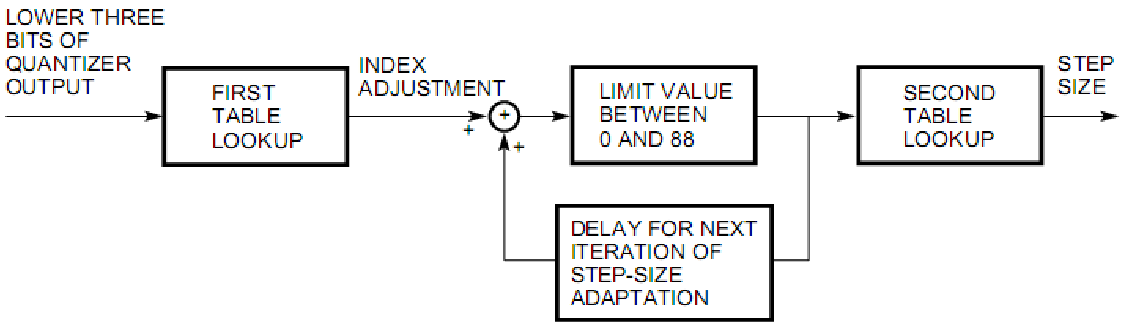
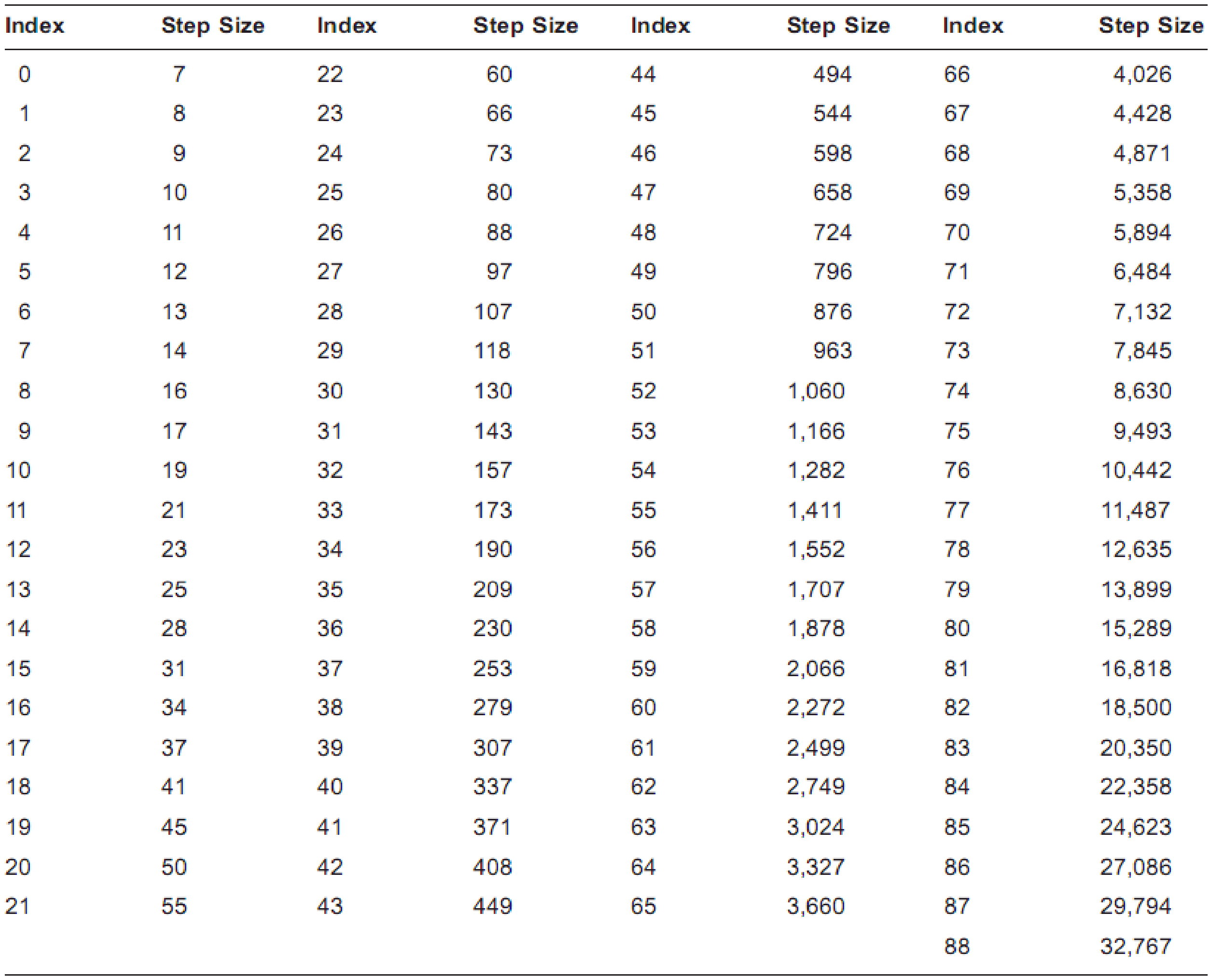

LOWER THREE BITS OF QUANTIZER OUTPUT
FIRST TABLE LOOKUP
INDEX ADJUSTMENT
+
+
+
LIMIT VALUE BETWEEN 0 AND 88
SECOND TABLE LOOKUP
STEP SIZE
DELAY FOR NEXT ITERATION OF STEP-SIZE ADAPTATION

Figure: 5 (Block diagram for step size adaption)

LOOK UP TABLE



Index	Step Size	Index	Step Size	Index	Step Size	Index	Step Size
0	7	22	60	44	494	66	4,026
1	8	23	66	45	544	67	4,428
2	9	24	73	46	598	68	4,871
3	10	25	80	47	658	69	5,358
4	11	26	88	48	724	70	5,894
5	12	27	97	49	796	71	6,484
6	13	28	107	50	876	72	7,132
7	14	29	118	51	963	73	7,845
8	16	30	130	52	1,060	74	8,630
9	17	31	143	53	1,166	75	9,493
10	19	32	157	54	1,282	76	10,442
11	21	33	173	55	1,411	77	11,487
12	23	34	190	56	1,552	78	12,635
13	25	35	209	57	1,707	79	13,899
14	28	36	230	58	1,878	80	15,289
15	31	37	253	59	2,066	81	16,818
16	34	38	279	60	2,272	82	18,500
17	37	39	307	61	2,499	83	20,350
18	41	40	337	62	2,749	84	22,358
19	45	41	371	63	3,024	85	24,623
20	50	42	408	64	3,327	86	27,086
21	55	43	449	65	3,660	87	29,794
						88	32,767

Table : 2 (look up table to determine step size)

3

HARDWARE DESIGN

CONTENTS:

3.1 Introduction
3.2 Block Diagram
3.3 Microphone
3.4 Filter and Amplifier
3.4.1 Pre-Amplifier & Anti-aliasing Filter
3.4.2 Low-pass filter & Power Amplifier
3.5 Microcontroller
3.5.1 ADC
3.5.2 PWM
3.6 External Memory Interface
3.6.1 Data Flash
3.6.2 SRAM
3.7 LCD interface
3.8 Speaker

3.1 Introduction:

This section describes the complete hardware design for this project. The main objective is to design the hardware in minimal cost for storing voice data and playing it back.

3.2 Block Diagram:

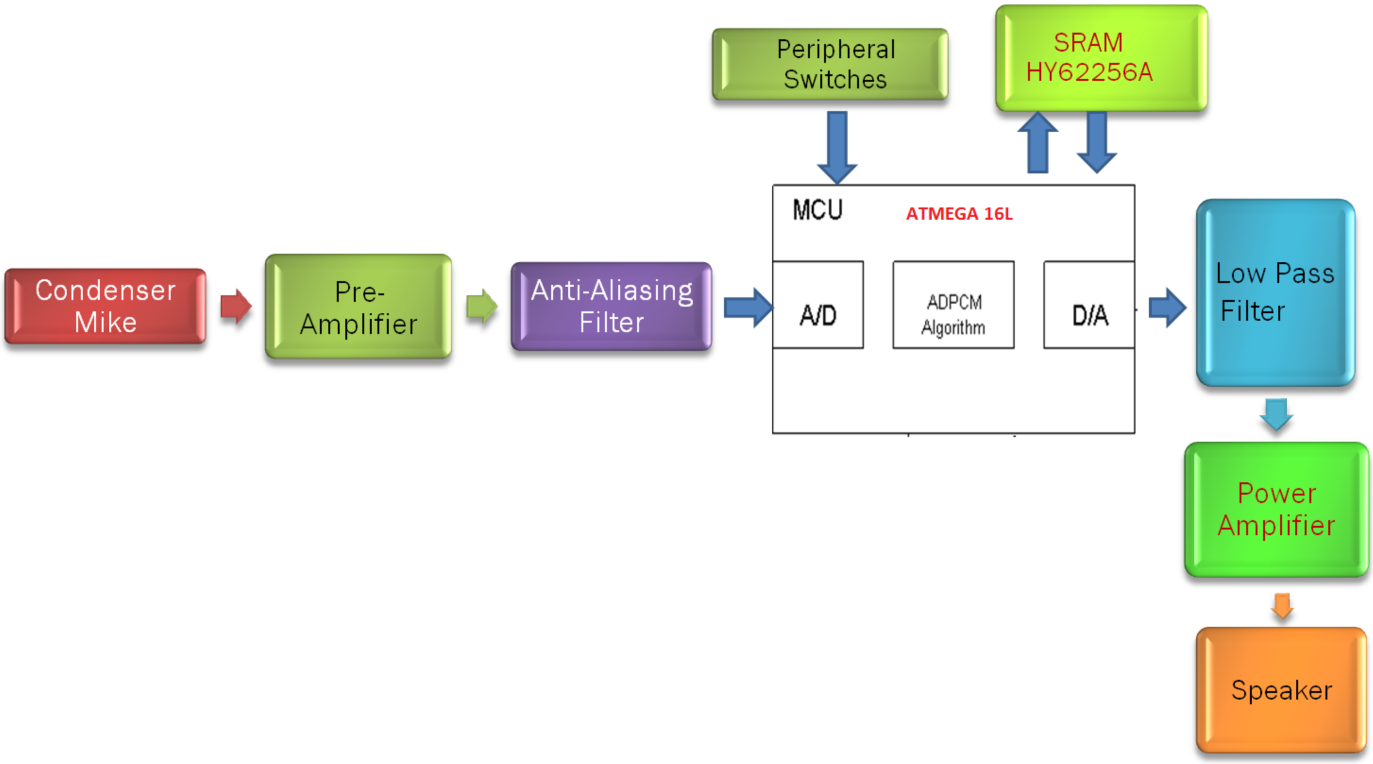


Figure: 6 (Block diagram of the hardware)

Components:

- Condenser Mike
- Pre-amplifier
- Anti-aliasing filter
- Microcontroller (ATMEGA 16)
- External memory (SRAM-HY 62256A)
- Peripheral switches
- Low pass filter
- Power Amplifier
- Speaker

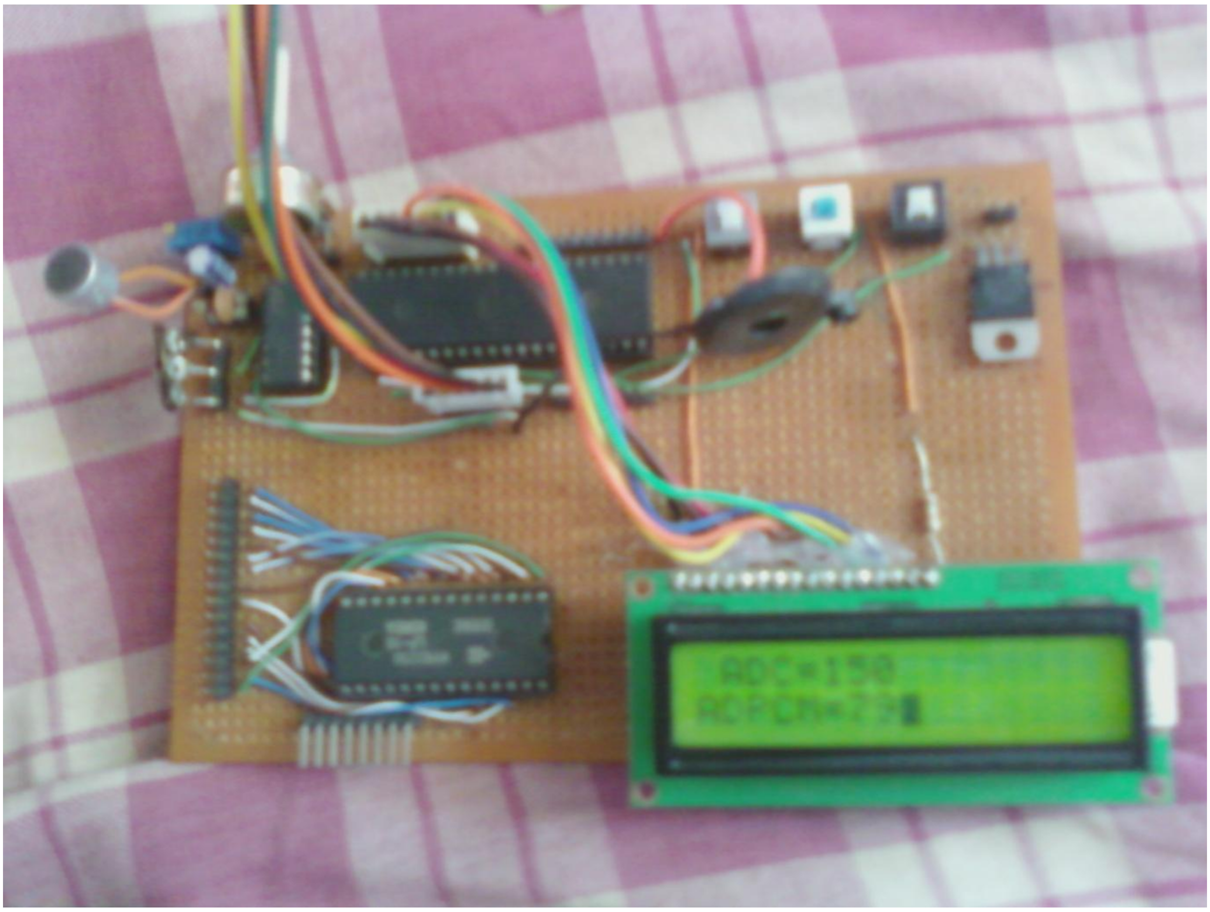


Figure: 7 (Front view of the actual hardware)

3.3 Microphone:

Here we have used CZ034A Omni directional Electret Condenser Microphone with Operation Voltage of 4.5V DC as microphone to receive the audio signal.

The input from mike is fed to B.0 of the microcontroller.

Figure: 8 (condenser mike)

Features:

For model: CZ034A, CZ034AP
Size (mm): 9.4 x 6.5
Connection: solder (CZ034A); pin (CZ034AP)
Directivity: Omni directional
Sensitivity range (0dB=1V/Pa, 1 kHz) (dB): -32dB - 46dB
Operation voltage (V DC): 4.5
External resistor (Kohm): 1.0/2.2
Impedance: low impedance
Current consumption: max. 500uA
Sensitivity reduction: within -3dB at 1.5V
S/N ratio: more than 60dB

3.4 Filter and Amplifier:

In telephony the usable voice frequency band ranges from approximately 300 Hz to 3400 Hz. It is for this reason that the ultra low frequency band of the electromagnetic spectrum between 300 and 3000 Hz is also referred to as *voice frequency* (despite the fact that this is electromagnetic energy, not acoustic energy). The bandwidth allocated for a single voice-frequency transmission channel is usually 4 kHz, including guard bands, allowing a sampling rate of 8 kHz to be used as the basis of the pulse code modulation system used for the digital PSTN.

3.4.1 Pre-amplifier & Anti-aliasing filter:

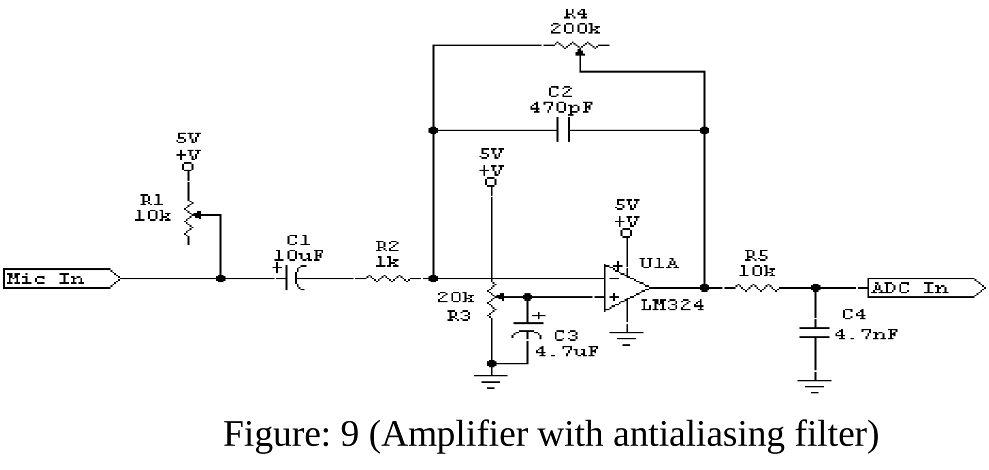


Figure: 9 (Amplifier with antialiasing filter)

The condenser microphone is biased using a variable resistor R1 and the DC component blocked by C1. The microphone amplifier and filter is implemented using an inverting op-amp amplifier configured for a high gain which is adjustable. It is set by R4 and R2 (gain = R4/R2). R3 set the offset. R5 and C4 form a simple single-stage RC filter. In addition R5 also protects from any damage if output is short circuited. The capacitor C2 in the feedback loop introduces a roll off at high frequencies, giving better stability since the gain is very high.

3.4.2 Low-pass filter:

The analog signal coming out of the D/A converter of a microcontroller generally contains a lot of high frequency components. The presence of assorted harmonics of the fundamental frequency is responsible for this. This may cause a deviation from audible frequency range. In order to avoid this, 2nd order Chebyshev filter with cutoff frequency 3.3 kHZ having 3dB pass-band ripple is designed. As the bandwidth of human voice is nearly 4 kHz, this filter is designed with a cutoff frequency of about 3.3 kHz.

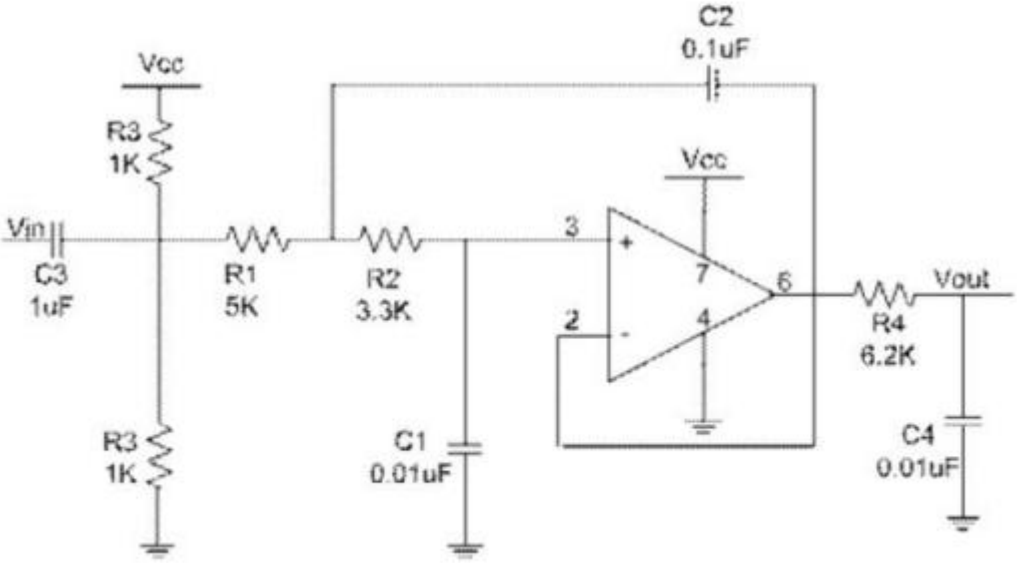


Figure: 10 (2nd order Chebyshev filter followed by RC low pass filter)

Because of its sharp transition and since its output takes less frequency range to die down after the cutoff frequency, Chebyshev filter is preferred over

Butterworth, though it carries small ripples in its pass-band which are of less magnitude to affect the output signal.

The filter constitutes of an active Device (Op-amp) LM324 (quad Op-amp) and a combination of capacitors and resistors. The D/A converted output from OC2 of the microcontroller is fed to the filter. A bias (offset) voltage of 2.5V was set to overcome the negative supply for Op-amp. The biasing is achieved by using a voltage divider and a capacitor before the filter circuit. Any DC component present in the signal coming from the microcontroller is blocked by the capacitor and hence the pre-set biased voltage is not disturbed. Another RC low-pass filter at the o/p of the Chebyshev filter is used to remove DC noise squeal (low power noise) and to get proper attenuation at 7.812 kHz (high power noise).

3.5 Microcontroller:

For this project, we have used ATMEGA 16L microcontroller from Atmel. Inbuilt ADC as well as 8 bit and 16 bit timer/counter for PWM generation, Programmable USART, SPI compatible etc. features made it the most suitable choice to be used in the circuit.

Important features:

- Advanced RISC Architecture
- Up to 16 MIPS Throughput at 16 MHz
- 16K Bytes of In-System Self-Programmable Flash
- 512 Bytes EEPROM
- 1K Byte Internal SRAM
- 32 Programmable I/O Lines
- In-System Programming by On-chip Boot Program
- 8-channel, 10-bit ADC
- Two 8-bit Timer/Counters with Separate Prescalers and Compare Modes
- One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture
- Four PWM Channels
- Programmable Serial USART

- Master/Slave SPI Serial Interface
- Byte-oriented Two-wire Serial Interface
- Programmable Watchdog Timer with Separate On-chip Oscillator
  External and Internal Interrupt Sources

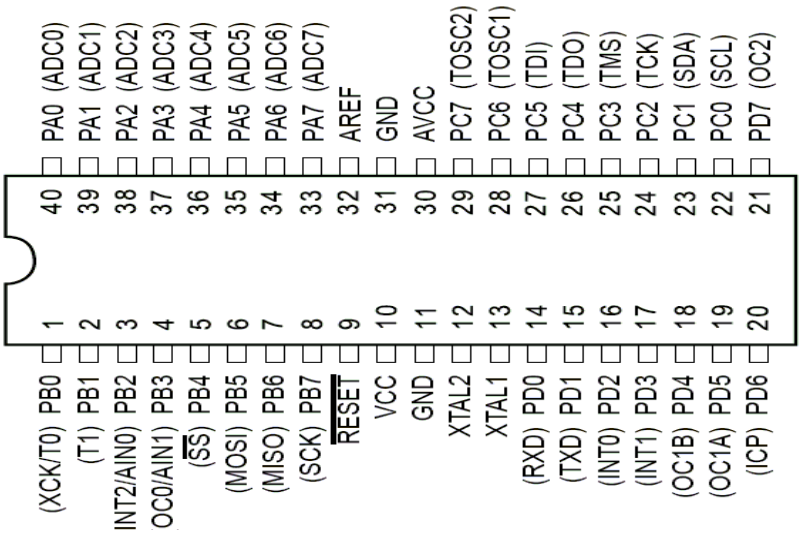
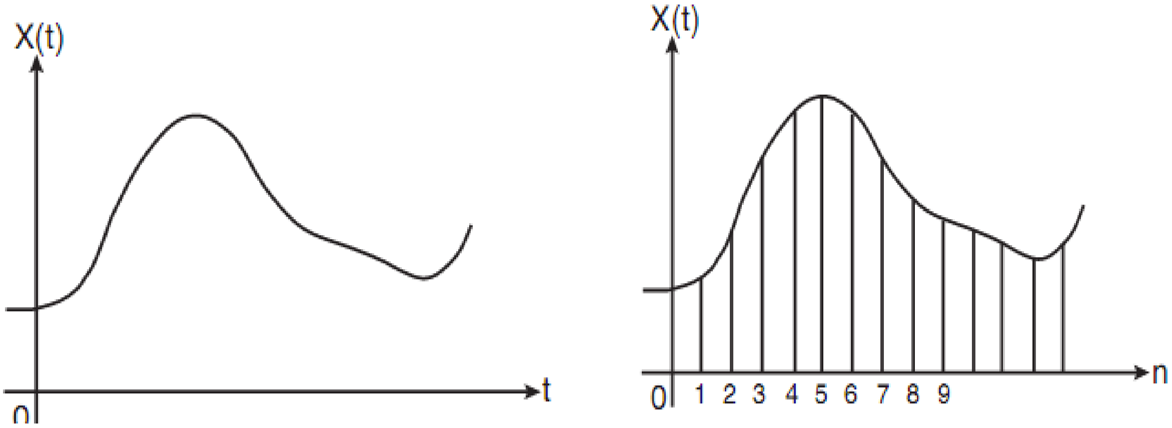


Figure: 11 (Pin configuration of ATMEGA 16L)

3.5.1 ADC (Analog to Digital Converter):

The analog speech signal can be stored in the memory by converting into a digital signal. This is done using the ADC feature of the microcontroller. The analog signal is converted into a time discrete signal by taking samples periodically.



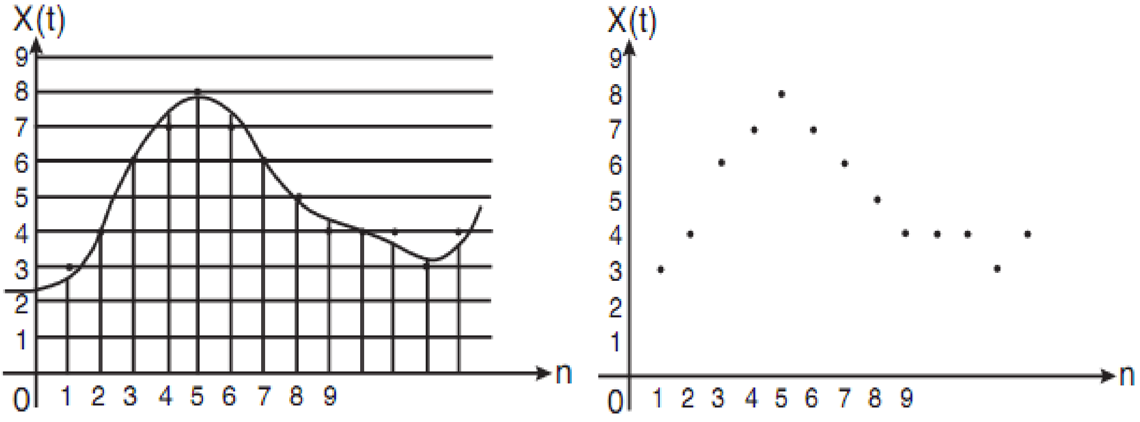
Analog signal

Time discrete signal

Figure: 12 (Analog signal and its discretized version)

The time interval between two samples is called the “sampling period” and its reciprocal the “sampling frequency”. According to the sampling theorem, the sampling frequency has to be at least double the maximum signal frequency. Otherwise the periodic continuation of the signal in the frequency domain would result in spectral overlap, called “**aliasing**”. Such an aliased signal cannot be uniquely recovered from its samples. As a speech signal contains its major information below 3 kHz, a low-pass filter is used to band-limit the signal. For an ideal low-pass filter with a cut-off frequency of 3 kHz the sampling frequency must be 6 kHz. Depending on the filter, the filter slope is more or less steep. Especially for a first order filter like the RC-filter used in this application it is necessary to choose a much higher sampling frequency. The upper limit is set by the features of the A/D-converter.

The digital values of the analog samples taken at this sampling frequency is called are quantized. The number of digital values is called “**resolution**” and depends on the number of bits. Therefore quantizations of analog signals are always associated with a loss of information. This “quantization error” is inversely proportional to the resolution of the digital signal and the signal’s “dynamic range”, the range between minimum and maximum values (3 to 8 in this example).



Quantized signal

Digital signal

Figure: 13 (Quantized signal and corresponding digital signal)

The A/D converter of the ATMEGA16L microcontroller can be adjusted to the dynamic range of the signal by setting AGND and AREF to the minimum and maximum signal values. On the other hand, the microphone amplifier can be adjusted to cover the ADC's dynamic range as presented later. Both methods reduce the quantization error. In addition, the latter method also increases the signal-to-noise ratio (SNR) and should therefore be preferred.

In this application, the signal has a minimum and a maximum value which are never exceeded. The parts of the signal below the minimum and above the maximum value do not contain any information. They can be removed in order to save memory. This is done by down shifting the whole signal and discarding the part above the maximum value.

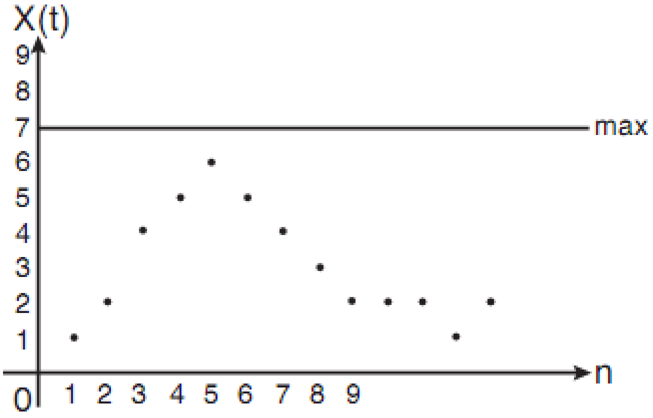


Figure: 14 (Down shifted digital signal)

The analog signal from the microphone circuit is sampled at 7,812 Hz, same frequency as the output (PWM) frequency. To achieve a sampling frequency of 7,812 Hz, a sample has to be taken every 1024 cycles (7,812 Hz x 1024 = 8 MHz). To get one A/D conversion result, each 1024 clock cycles the ADC is run in single conversion mode with an ADC clock division by 64 i.e. ADC clock frequency is 8000/64= 125 kHz

A single conversion takes 14 ADC cycles. Therefore a conversion will be ready after 14 x 64 = 896 cycles.

When a conversion is finished an interrupt occurs. The interrupt routine then performs a loop to fill in the missing 1024 – 896 = 128 cycles, before a new A/D conversion is started.

3.5.2 PWM (Pulse Width Modulation):

Timer2 in fast pwm mode is used for ADPCM encoder and decoder ensuring regular interrupts and simultaneously freeing OC2 (Output Compare) for DA conversion. There are three on/off switches for Record, Erase and Playback. The inputs from these switches are fed to B.1-B.3 pins. Depending upon which switch is pressed, it is determined whether the encoding algorithm or the decoding is to be run or if timer2 should turn itself off. Timer0 causes the changes the state of state variable.

Timer0 is used to constantly monitor two events. When Record button is pressed, the sample is taken from the microphone and A/D converter converts it to digital value and then it is encoded using ADPCM encoding followed by storing in the SRAM. When Playback button is pressed, a sample is taken from SRAM by the microcontroller. It is decoded, and being written into OC2 (the DAC). Both of this is timed by timer2 in PWM mode. The RECORD mode as well as the PLAYBACK mode runs for a fixed duration of time. After this duration is lapsed, STANDBY mode becomes active.

3.6 External Memory Interface:

To store the voice memory is required. ATMEGA 16L microcontroller has 16kB on chip flash memory which is very less to store the voice apart from storing the code itself.

Generally all analog speech signals are converted to 8 bits. So when represented by 4-bits it offers a 50% saving in memory requirement and the 2-bit representation offers a 75% savings. All speech signals are sampled approximately at 8 kHz. Thus, each second of sound consists of 8000samples. 4-bits per sample is used for 4-bit ADPCM encoding, which states that 1 second of sound needs a space of approximately 32kBits or 4kB. Similarly 2-bit ADPCM will require approximately 2kB to encode 1 second of sound. As the external SRAM we used, has 32 KB of flash memory, a bit more than 8 second can be stored using 4-bit ADPCM and it can store a bit more than 16.5 seconds of sound using 2-bit ADPCM.

3.6.1 Data Flash Interface:

Data Flash is a low pin-count serial interface for flash memory. It is an Atmel proprietary interface, compatible with the SPI standard. Information is written and read from a Data Flash chip using any microcontroller, such as the Atmel AVR, the Microchip PIC or the ARM. (E.g.: The AT45DB161B chip is an example of a 2 MB data flash chip available from Atmel.

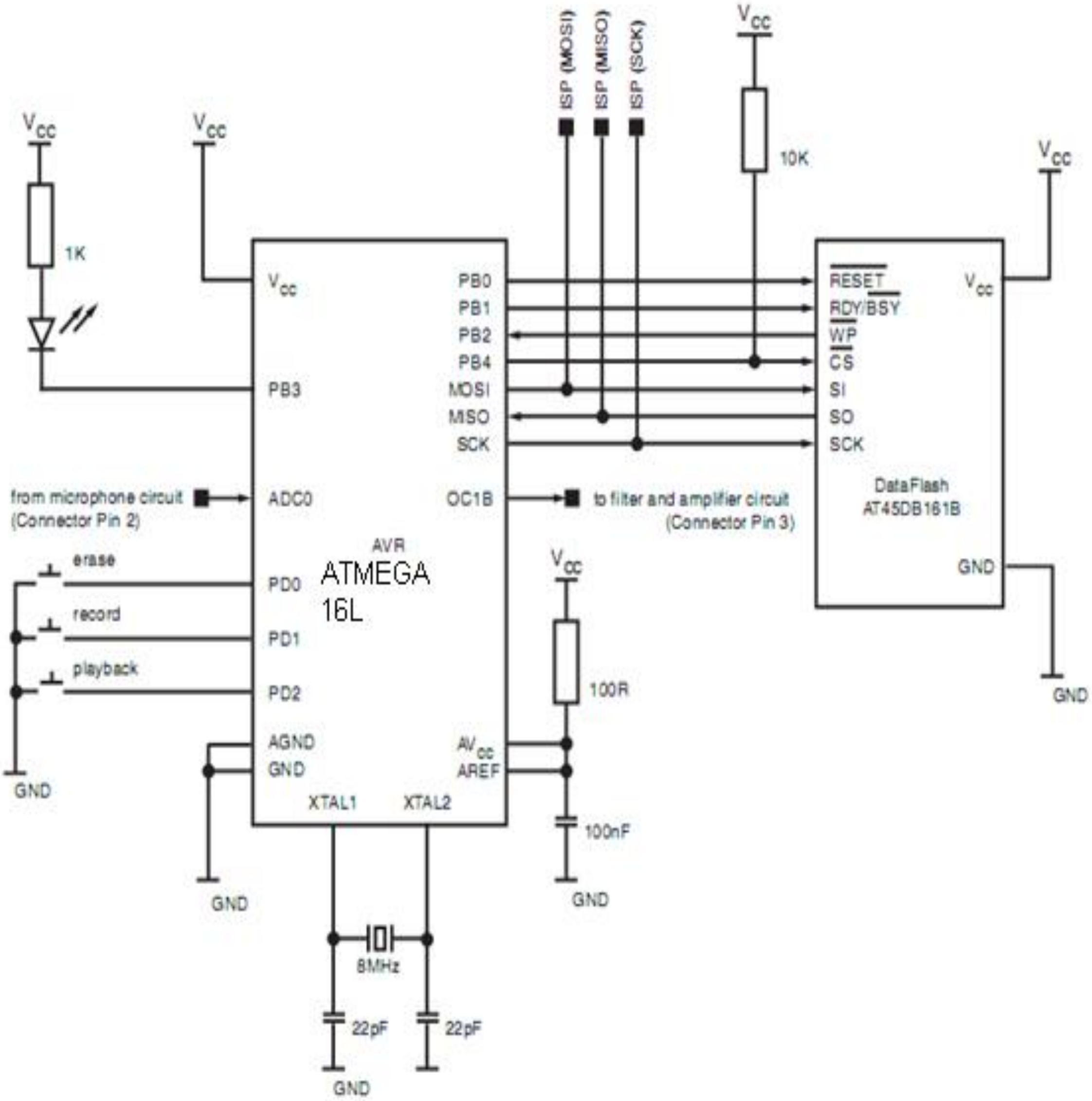
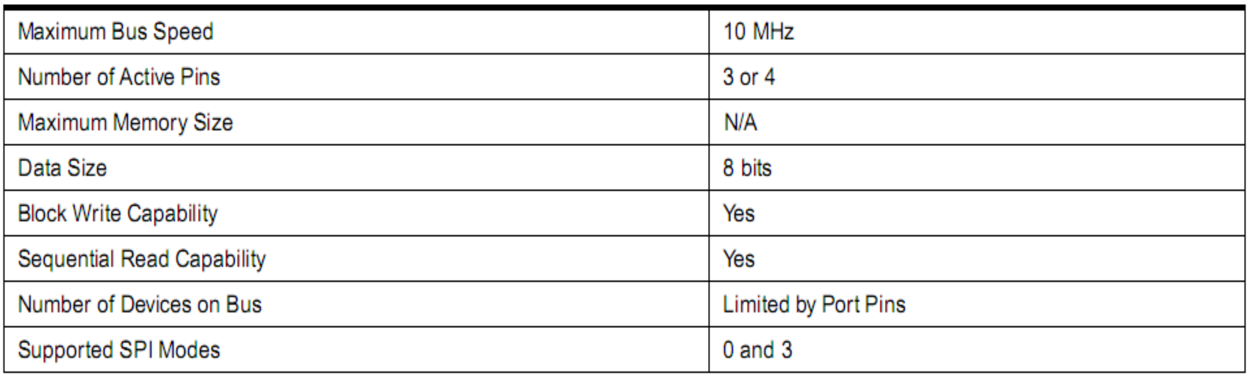


Figure: 15 (Interfacing of data flash with ATMEGA 16L)



Maximum Bus Speed	10 MHz
Number of Active Pins	3 or 4
Maximum Memory Size	N/A
Data Size	8 bits
Block Write Capability	Yes
Sequential Read Capability	Yes
Number of Devices on Bus	Limited by Port Pins
Supported SPI Modes	0 and 3

Table: 3 (Features of the serial Data Flash Interface)

3.6.2 SRAM Interface:

The challenge to using external memory comes down to basic economics-scarcity. Microcontrollers have a limited number of I/O pins and memory devices require an abundance of them, particularly for addressing. By using some of the address circuits described below it is possible to use external memory with AVR devices such as ATMEGA16L.

Interface Method	I/O pin requirements	Address Access Speed
Direct	Very High	Very Fast
Latch	High	Fast
Shift register	Medium	Slow
Ripple Counter	Very Low	Fast (sequential) Very slow(random)

Table: 4 (Comparison of External Memory Address Interfaces)

Basic Connection:

The pin connections in SRAM are the address inputs, data I/O, some type of selection input and at least one control input used to select a read or write operation.

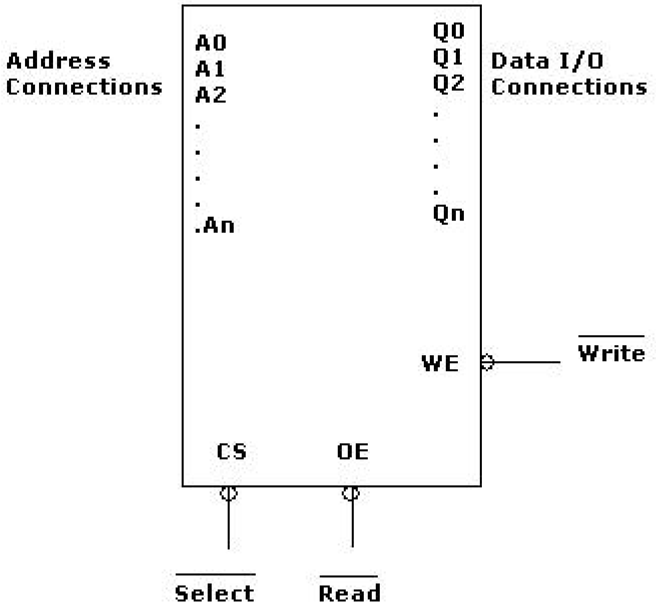


Figure: 16 (Basic memory component connections)

A memory location within the memory device is accessed by the address inputs. Depending on the number of memory locations no o address pins are selected. The data I/O connections are required to store data and read data.

The SRAM has a chip select (CS) pin to enable the memory device. This pin is activated by applying logic 0 at this pin to perform a read or a write operation.

The other two control inputs associated with SRAM are Write Enable (WE) and Output (also called read enable) Enable (OE). The write enable pin is activated by applying logic 0 to perform a memory write operation and the (OE) must be active to perform a read operation from the memory. But they must never both be active at the same time.

The following figures show the timing diagrams for a typical read and write operation.

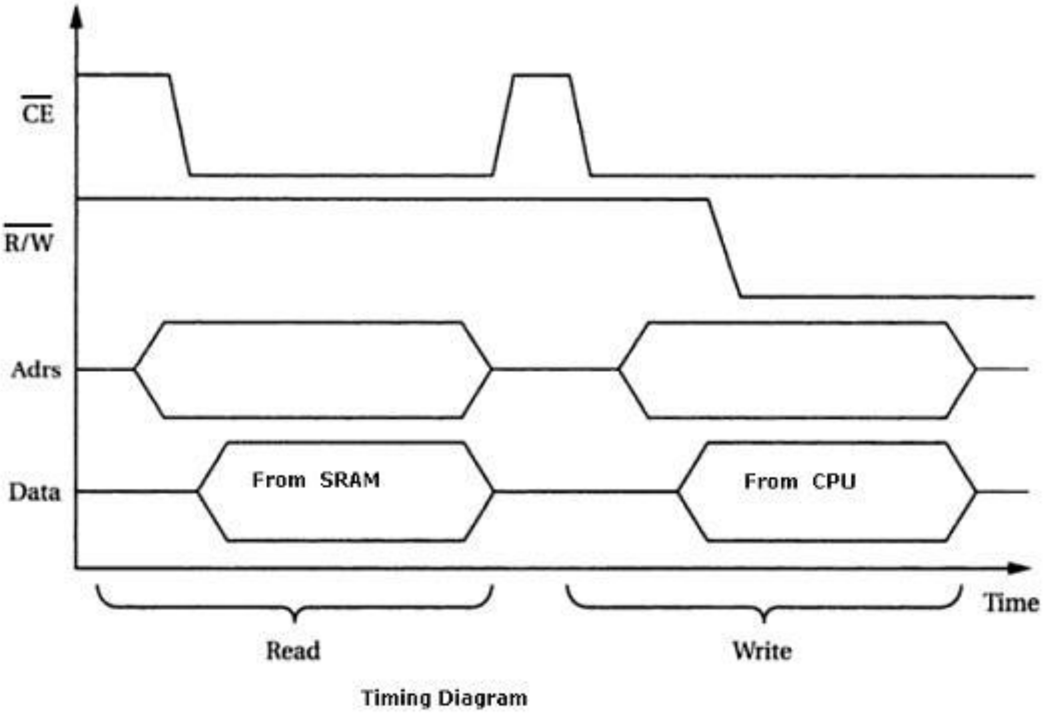


Figure: 17 (timing diagram of read write operation)

In our project we have used HY62256A SRAM from Hyundai.

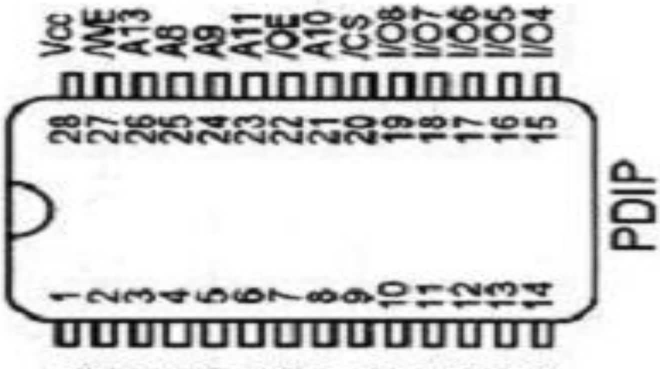
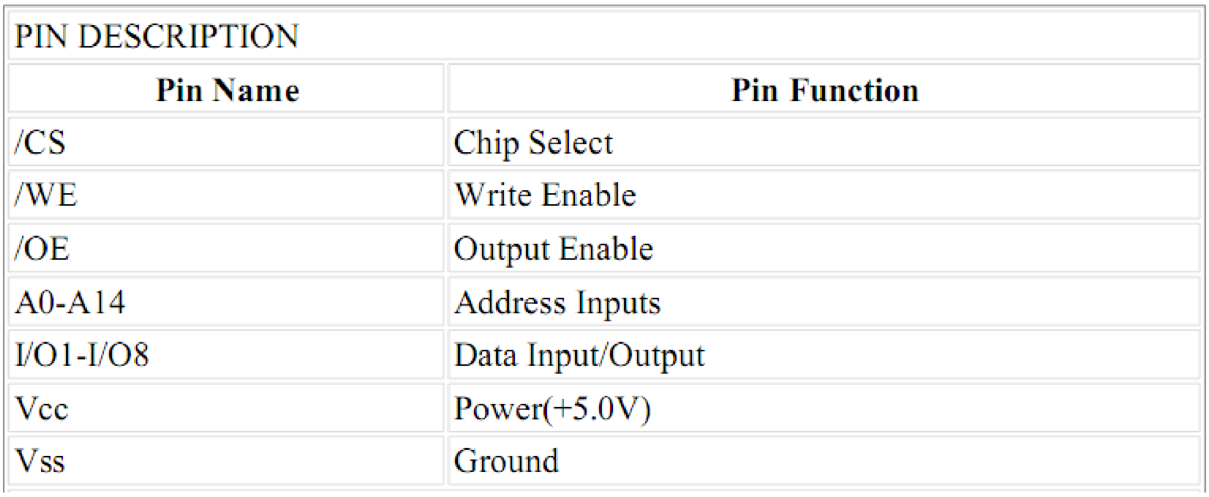
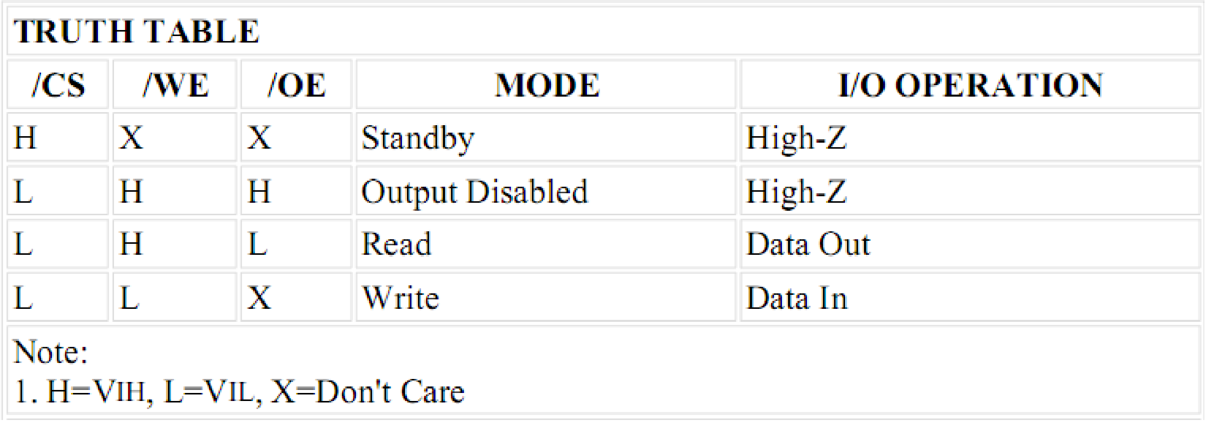


Figure: 18 (SRAM pin configuration)



PIN DESCRIPTION	
Pin Name	**Pin Function**
/CS	Chip Select
/WE	Write Enable
/OE	Output Enable
A0-A14	Address Inputs
I/O1-I/O8	Data Input/Output
Vcc	Power(+5.0V)
Vss	Ground

Table: 5 (Pin description)



TRUTH TABLE				
/CS	**/WE**	**/OE**	**MODE**	**I/O OPERATION**
H	X	X	Standby	High-Z
L	H	H	Output Disabled	High-Z
L	H	L	Read	Data Out
L	L	X	Write	Data In

Note:
1. H=VIH, L=VIL, X=Don't Care

Table: 6 (mode of operation)

Interfacing of SRAM to ATMEGA16L:

The chip contains 8 bit I/O and 15 address pins. In addition to these, it also contains a chip enable (CE) pin, a write enable (WE), and an output enable (OE) pin.

PORTC and PORTD (0-6) are interfaced to the address bits of the SRAM. PORTA connected to the IO pins (LCD is disabled at that time since LCD also uses the same port). B.0 and B.1 were connected to WE and OE.

While reading SRAM the address bits with PORTD and PORTC are set on one cycle, and on the next cycle OE is set low. The bits of PINB are read on the third cycle. To write the address bits with PORTD and PORTC are set on one cycle and on the next cycle OE is set high. WE is set low on the third cycle. On the fourth cycle data is written to PORTA. On the fifth cycle WE is set high to protect data integrity.

3.7 LCD Interface:

The most common type of controller used by character LCD modules is the Hitachi HD44780, which uses a relatively simple interface between the microcontroller and an LCD. The most commonly available character LCD display is the JHD 162A. It has a 16X2 character display.

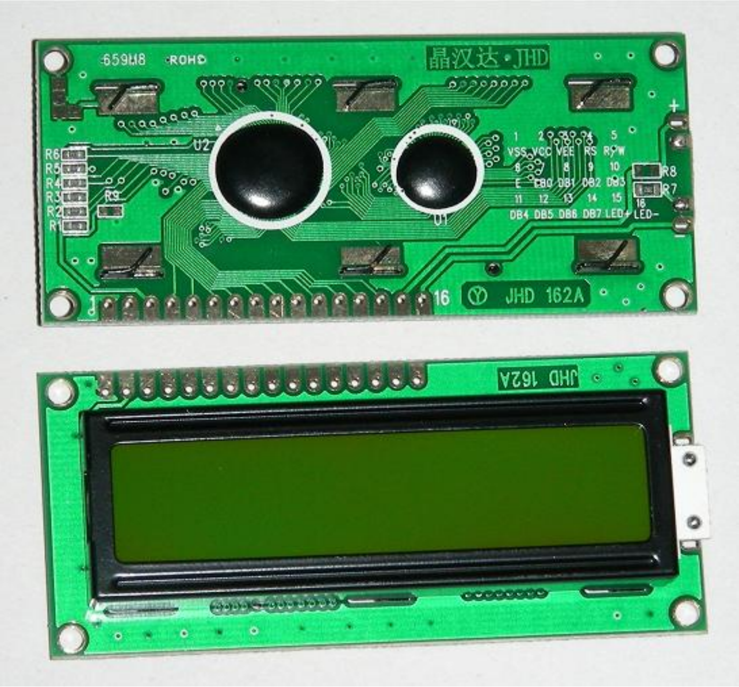


Figure: 19 (LCD front and back view)

Features:

• It has a 16X2 character LCD display. By 16X2 I mean 16 CharacterX2 Rows

• Each character is displayed in a 5X8 pixel array. 5 columns & 8 rows

• Adjustable pixel contrast

• LCD backlight

Pin Description:

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
VSS	VCC	VEE	RS	R/W	E	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	LED+	LED_

Table: 7(Pin description of LCD)

VSS (1): This pin is connected to the Ground
VCC (2): This pin is connected to a 5-Volts supply
VEE (3): This pin is for adjusting the contrast of the display. The voltage on this pin determines the darkness of the pixels. Use a potentiometer connected between VCC and GND and connects divider voltage to this pin.
RS (4): RS stands for "register select". RS=0 means that the instruction register is selected. RS=1 means that the data register is selected. In other words, according to the status of RS pin, the data on the data bus is treated either as a command or character data
R/W (5): It determines if we read from or write to the LCD
E (6): E pin enables or disables the LCD module. When Enable is low the LCD is disabled and the status of RS, R/W and the data bus will be ignored. When Enable pin is high the LCD is enabled and the status of the other control pins and data bus will be processed by the LCD
[DB0-DB7] (7-14): D0-D7 is the bi-directional data bus
LED+ & LED- : This is where we give the power supply for the backlight of the LCD display

4bit Interface:

In 4-bit mode data is sent nibble by nibble, first higher nibble and then lower nibble is sent which means while sending data and command, the higher nibble and lower nibble are to be separated.

Here we have interfaced D4-D7 with A.4 to A.7 of microcontroller and 3 control pins (RS, R/W, E) are connected with A.1 to A.3.

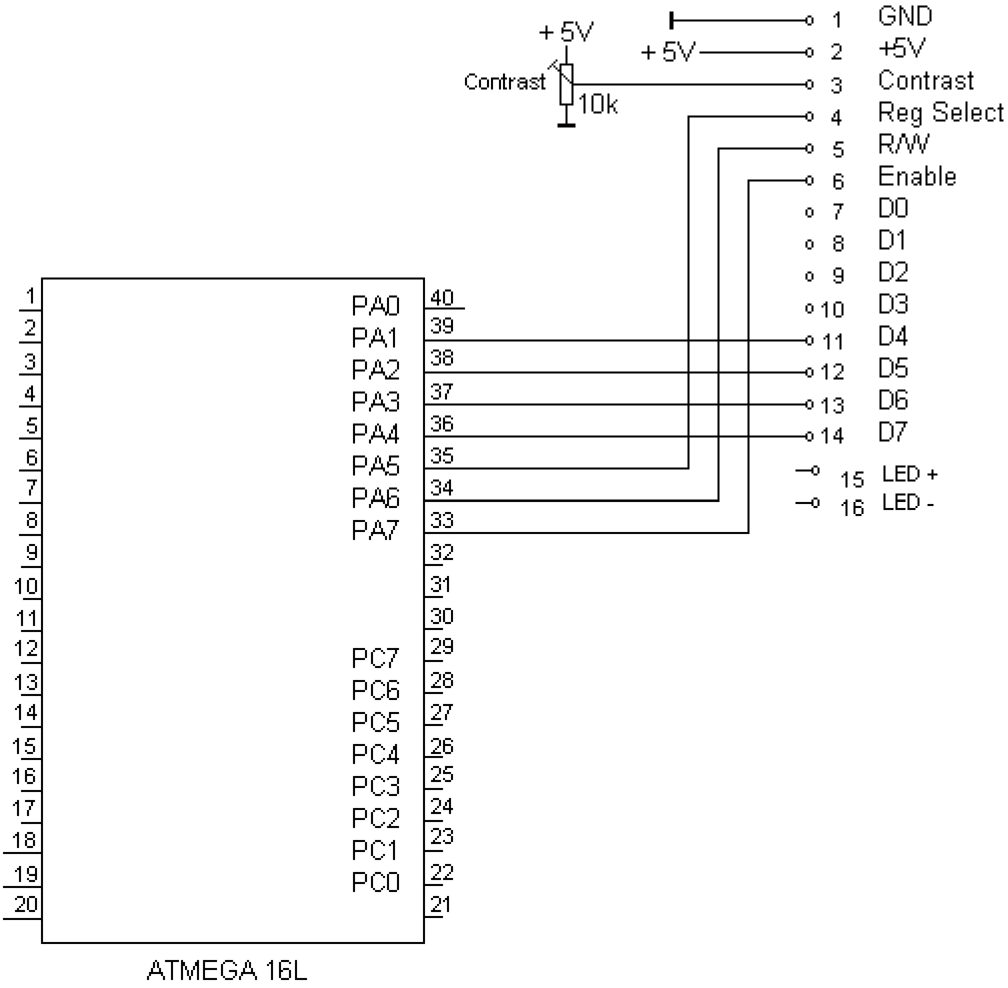


Figure: 20 (4-bit LCD interfacing)

The common steps are:

- Mask lower 4-bits
- Send to the LCD port
- Send enable signal
- Mask higher 4-bits
- Send to LCD port
- Send enable signal

The LCD is used to display the ADC value as well as corresponding ADPCM value of the input from microphone.

3.8 Speaker:

Speakers are output devices through which electrical signals come out as sound. It is in fact an electromechanical transducer, which is very much responsible for the quality of the sound that comes out.

Figure: 21 (speaker)

Piezoelectric speakers are frequently used as beepers in watches and other electronic devices, and are sometimes used as tweeters in less-expensive speaker systems, such as computer speakers and portable radios.

The speaker is connected to the output from the low-pass filter shown in fig.10.

4

RESULTS AND CONCLUSION

CONTENTS:

4.1 Simulation Result
4.2 Conclusion & future woks

4.1 Simulation Result:

The encoding and decoding of an audio signal in “.wav” format is done in MATLAB environment. An audio signal is given as input and encoded using ADPCM algorithm. Then again this encoded signal is given as input to another program of decoding and the original signal is regenerated. The waveforms of input, encoded signal and final output are given here.

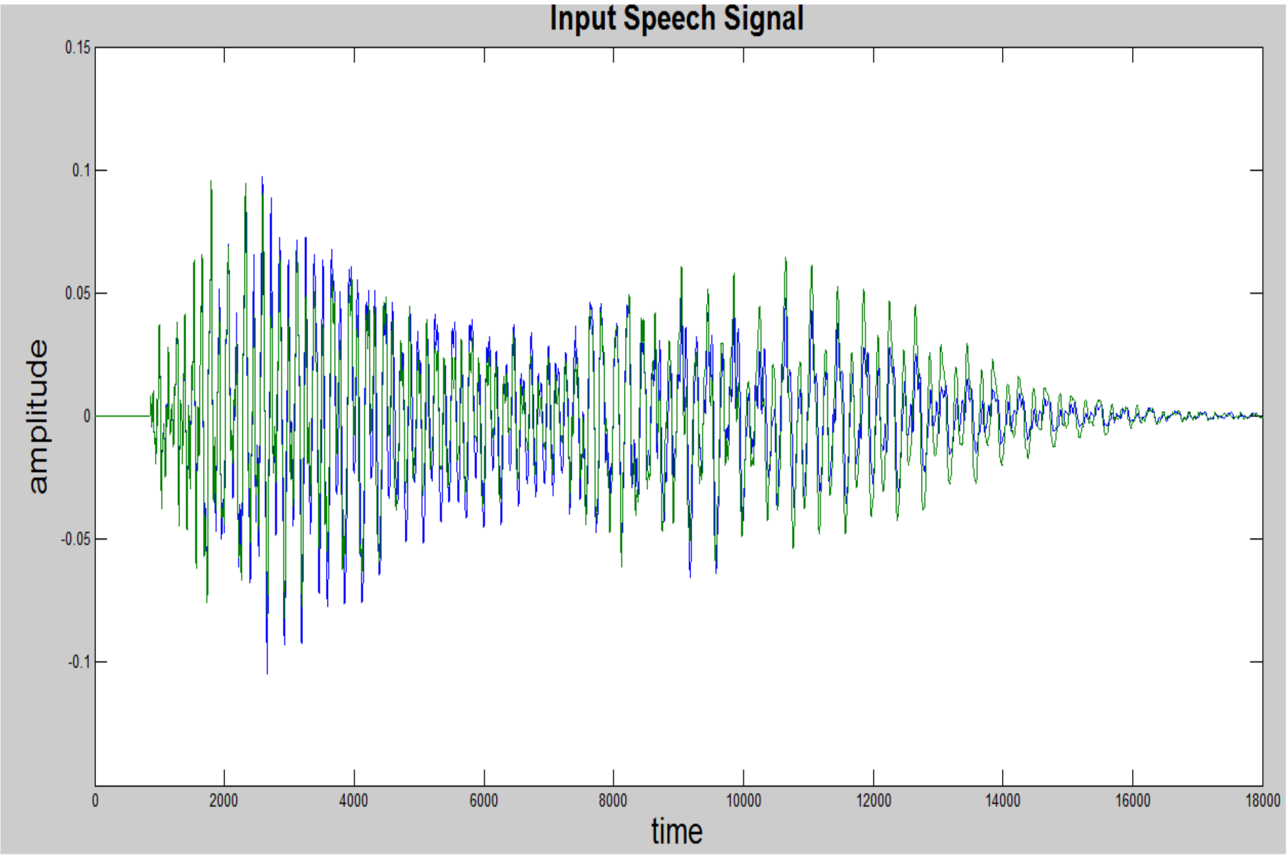


Figure: 22 (input speech signal)

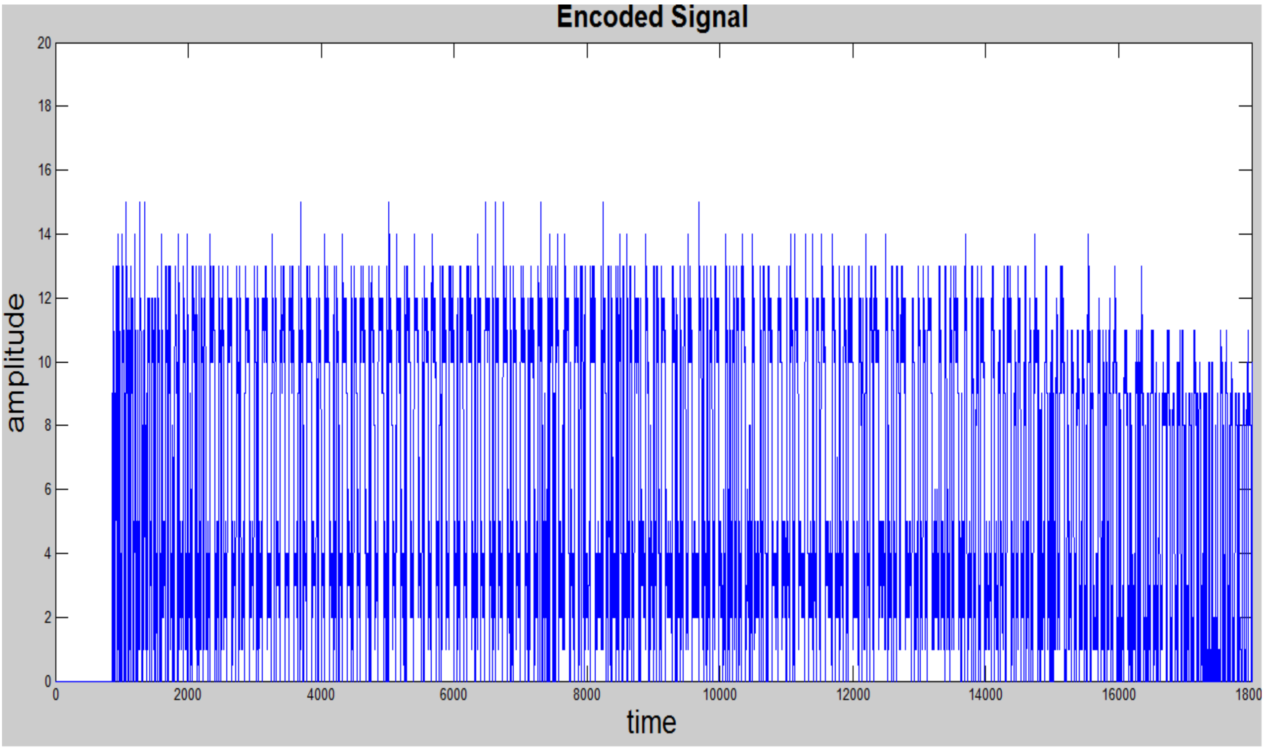


Figure: 23 (Encoded signal)

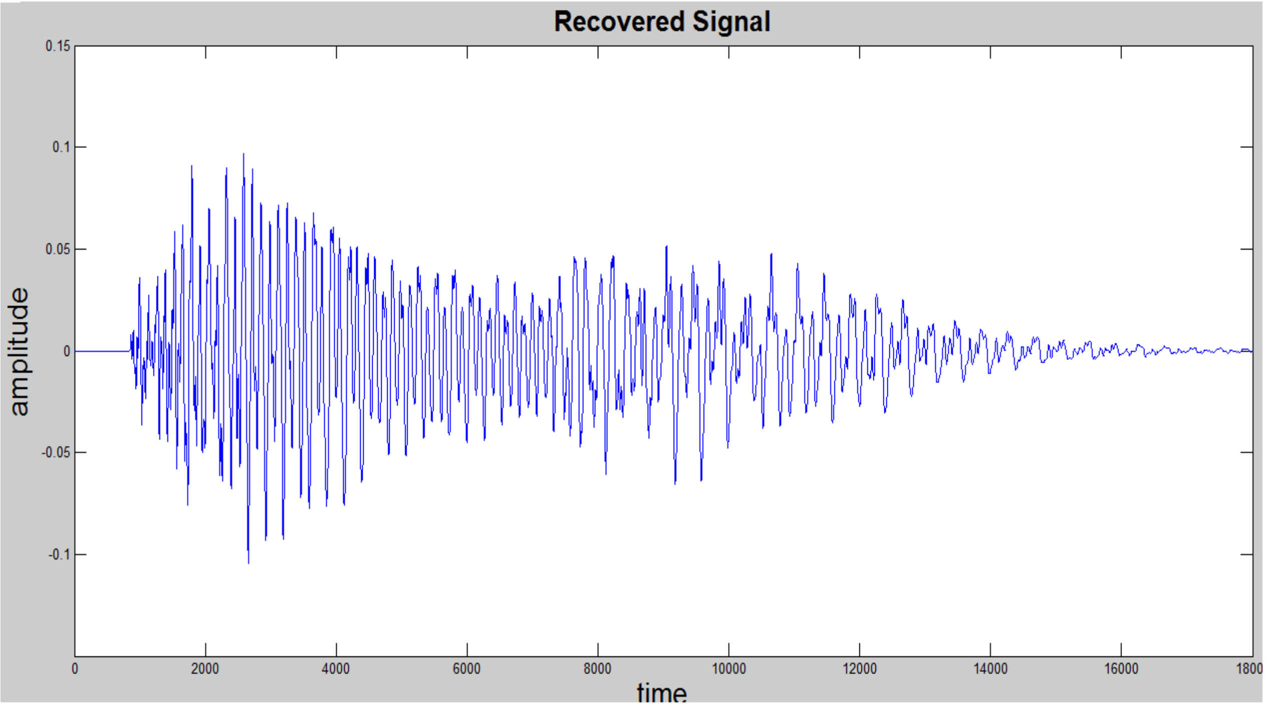


Figure: 24 (Recovered signal)

4.2 Conclusion & Future works

We have designed the hardware for input stage pre-amplifier and anti-aliasing filter. The input is given through a condenser mike and then the output of amplifier-filter pair is fed to microcontroller. This data is den converted to digital value and stored on data-flash and displayed on a LCD. Also the wave-forms are being checked in an oscilloscope.

The LCD interfacing, ADC features and PWM generation features of microcontroller ATMEGA 16L are studied and implemented successfully on hardware. External buzzer is used to check the PWM output.

SRAM and data flash interfacing is studied for the external storage of recorded message and implemented on hardware. Due to unavailability of Data flash, SRAM had to be used which consumed 23 pins of microcontroller instead of only 7 pins which had been the case for Data flash interfacing.

The testing of the data recording and recovery on giving interrupts by external switches (describing the incoming call, asking for message recording and listening to it when user is back) is yet to be done and left as future work.
There is also provision to interface a Data flash for storage of voice using less wiring which also can be taken as future work.

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