A NOVEL HIGH SPEED CMOS COMPARATOR WITH LOW POWER DISIPATION AND LOW OFFSET

A THESIS SUBMITTED IN PARTIAL FULFILLMENT

OF THE REQUIREMENTS FOR THE DEGREE OF

Master of Technology

In

VLSI Design & Embedded System

By

Debasis Parida

Roll No: 208EC206

Department of Electronics & Communication Engineering

National Institute of Technology

Rourkela

2010

A NOVEL HIGH SPEED CMOS COMPARATOR WITH LOW POWER DISIPATION AND LOW OFFSET

A THESIS SUBMITTED IN PARTIAL FULFILLMENT

OF THE REQUIREMENTS FOR THE DEGREE OF

Master of Technology

In

VLSI Design & Embedded System

By

Debasis Parida

Roll No: 208EC206

Under the guidance of

Prof. K. K. Mahapatra

Department of Electronics & Communication Engineering

National Institute of Technology

Rourkela

2010

National Institute Of Technology
Rourkela

CERTIFICATE

This is to certify that the thesis entitled, "**A NOVEL HIGH SPEED CMOS COMPARATOR WITH LOW POWER DISIPATION AND LOW OFFSET "** submitted by **Debasis Parida (208EC206)** in partial fulfillment of the requirements for the award of Master of Technology degree in Electronics and Communication Engineering with specialization in "VLSI design & Embedded systems" during session 2008-2010 at National Institute Of Technology, Rourkela (Deemed University) and is an authentic work by him under my supervision and guidance .

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other university/institute for the award of any Degree or Diploma.

Date:

Prof. K. K. Mahapatra
Dept. of Electronics and Communication Engineering
National Institute of Technology
Rourkela

Acknowledgments

First of all, I would like to express my deep sense of respect and gratitude towards my advisor and guide **Prof. K. K. Mahapatra,** who has been the guiding force behind this work. I want to thank him for introducing me to the field of Analog Design and giving me the opportunity to work under him. I consider it my good fortune to have got an opportunity to work with such a wonderful person.

I express my respects to Prof. S.K. Patra, Prof. G. S. Rath, Prof. S. Meher, Prof. S.K.Behera, Prof. Punam Singh, Prof. D.P.Acharya, Prof. S.K. Das, Prof. Murthy and Prof. Ari for teaching me and also helping me how to learn. They have been great sources of inspiration to me and I thank them from the bottom of my heart.

I would like to thank all faculty members and staff of the Department of Electronics and Communication Engineering, N.I.T. Rourkela for their generous help in various ways for the completion of this thesis.

I would like to thank my friends. I am also thankful to my classmates for all the thoughtful and mind stimulating discussions we had, which prompted us to think beyond the obvious.

Debasis Parida

CONTENTS

ABSTRACT

A Novel High Speed CMOS Comparator with low power dissipation, low offset, low noise and high speed is proposed. Inputs are reconfigured from typical differential pair comparator such that near equal current distribution in the input transistors can be achieved for a meta-stable point of the comparator. Restricted signal swing clock for the tail current is also used to ensure constant currents in the differential pairs. Nearly 18 mv offset voltage is easily achieved with the proposed structure making it favourable for flash and pipeline data conversion applications.

The proposed topology is based on hysteresis using positive feedback, has a small power dissipation, less area, and it is shown to be very robust against transistor mismatch, noise immunity. Test structures of the comparators, designed in GPDK 90 nm are measured to determine offset –voltage, power - dissipation and speed. These are compared and the superior features of the proposed comparator are established.

Chapter 1

Introduction

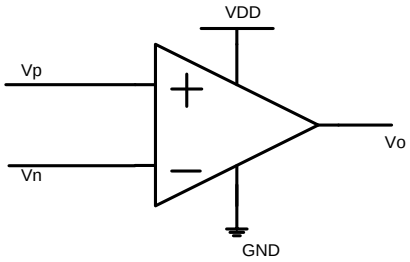
1.1. BASIC CMOS COMPARATOR:-

The schematic symbol and basic operation of a voltage comparator are shown in fig1.1 The comparator can be thought of as a decision making circuit.

Definition:-

The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison.

If the +, V_P, the input of the comparator is at a greater potential than the -, V_N, input, the output of the comparator is a logic 1, where as if the + input is at a potential less than the – input, the output of the comparator is at logic 0.



$V_P < V_N$ then V_O = VSS= logic 0.

$V_P > V_N$ then V_O = VDD= logic 1.

Fig. 1.1: Comparator operation

What is meant here by an analog signal is one that can have any of a continuum of amplitude values at a given point in time .In the strictest sense a binary signal can have only one of two given values at any point in time, but this concept of a binary signal is too ideal for real-world situations, where there is a transition region between the two binary states. It is important for the comparator to pass quickly through the transition region. The comparator is widely used in the process of converting analog signals to digital signals. In the analog-to-digital conversion process, it is necessary to first sample the input. This sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal. In its simplest form, the comparator can be considered as a 1-bit analog-digital converter. The presentation on comparators will first examine the requirements and characterization of comparators. It will be seen that comparators can be divided into open-loop and regenerative comparators. The open-loop comparators are basically op amps without compensation. Regenerative comparators use positive feedback, similar to sense amplifiers or flip-flops, to accomplish the comparison of the magnitude between two signals. A third type of comparator

emerges that is a combination of the open-loop and regenerative comparators. This combination results in comparators that are extremely fast.

1.2 Motivation:

In today's world, where demand for portable battery operated devices is increasing, a major thrust is given towards low power methodologies for high speed applications. This reduction in power can be achieved by moving towards smaller feature size processes. However, as we move towards smaller feature size processes, the process variations and other non-idealities will greatly affect the overall performance of the device. One such application where low power dissipation, low noise ,high speed ,less hysteresis ,less Offset voltage are required is Analog to Digital converters for mobile and portable devices. The performance limiting blocks in such ADCs are typically inter-stage gain amplifiers and comparators. The accuracy of such comparators, which is defined by its offset, along with power consumption, speed is of keen interest in achieving overall higher performance of ADCs. In the past, pre-amplifier based comparators have been used for ADC architectures such as flash and pipeline. The main drawback of pre-amplifier based comparators is the more offset voltage. To overcome this problem, dynamic comparators are often used that make a comparison once every clock period and require much less offset voltage. However, these dynamic comparators suffer from large power dissipation compared to pre-amplifier based comparators.

In the literature, Hysteresis comparators can be found, However, very little emphasis is placed on actual details of operation of these structures along with experimental results to compare offset values, power consumption, speed of different structures. These experimental offset values vary from 18mv to 50 mV. However, the literature is devoid of any information on how other non-idealities such as imbalance in parasitic capacitors, common mode voltage errors or clock timing errors effect these structures. In the new comparator structure, inputs are reconfigured from the typical differential pair comparator [4] so that each differential pair branch contributes equal current at the detestable operating point along with keeping the differential pair's tail current in saturation region. Comparison of the new architecture with respect to typical differential pair structure is made as both structures share the same base structure.

1.3 Thesis organization:

This thesis provides A CMOS comparator with hysteresis using positive feedback. Simulation results gives High Speed, low power dissipation. less offset, low noise. Thesis can be organized in the following manner. Chapter 2 focuses on characterisation of comparator.Chapter3 focuses on Conventional comparators of DC responses, measuring offset voltages, Delay, Speed, Power dissipation. Chapter 4 focuses on Design of Latched Comparator. Chapter 5 focuses on Hysteresis design .The experimental values of all the results are shown in table. All the layouts of Comparators are shown in the Appendix.

Chapter 2

Theory of Basic CMOS Comparator Design

2.1. CMOS COMPARATOR CHARACTERIZATION :-

A positive voltage applied at the *Vp* input will cause the comparator output to go positive, whereas a positive voltage applied at the V_N input will cause the comparator output to

go negative. The upper and lower voltage limits of the comparator Output are defined as V_{OH} and V_{OL} respectively.

Static Characteristics:-

A comparator was defined above as a circuit that has a binary output whose value is based on a comparison of two analog inputs. This is illustrated in Fig.2.1 As shown in this figure. The output of the comparator is high (V_{OH}) when the' difference between the no inverting and inverting inputs is positive, and low (V_{OL}) when this difference is negative. Even though this type of behavior is impossible in a real-world situation, it can be modeled with ideal circuit elements with mathematical descriptions. One such circuit model is shown in Fig.2.2 comprises a voltage-controlled voltage source (VCVS) whose characteristics are described the mathematical formulation given on the figure.

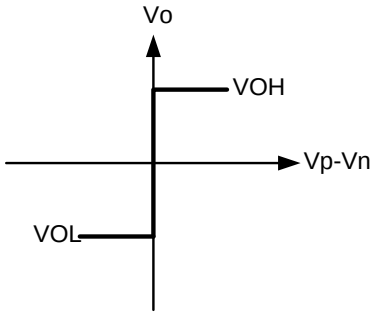


Fig.2.1. Ideal transfer curve of a Comparator

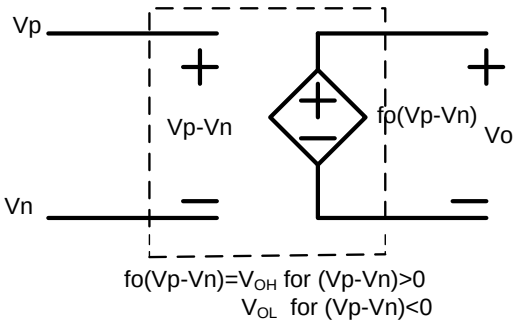


Fig. 2.2 Model for an ideal Comparator

The second no ideal effect seen in comparator circuits is input-offset voltage, *Vos.* In Fig.2.1 the output changes as the input difference crosses zero. If the output did not change until the input difference reached a value *+Vos,* then this difference would be defined as the offset voltage. This would not be a problem if the offset could be predicted, but it varies randomly from circuit to circuit [I] for a given design. Figure 2.4 illustrates offset in the transfer curve for a comparator, with the circuit model including an offset generator shown in Fig.2.5. The ± sign of the offset voltage accounts for the fact that *Vos* is unknown in polarity.

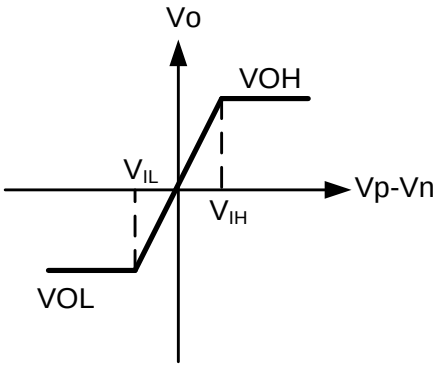


Fig. 2.3. Transfer curve of a comparator

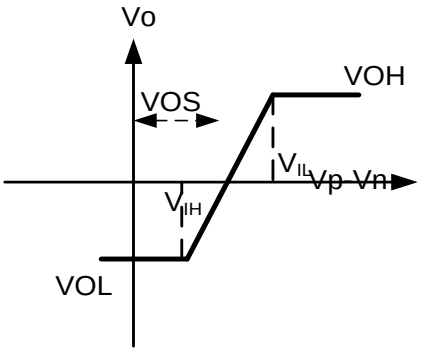
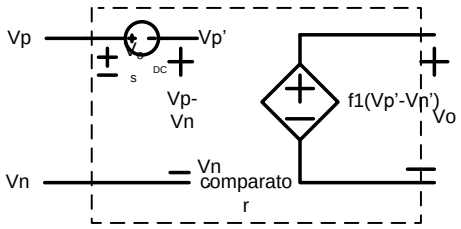


Fig. 2.4 Transfer curve of a comparator with finite gain including input – offset voltage

In addition to the above characteristics, the comparator can have a differential input resistance and capacitance and an output resistance. In addition, there will also be an input common-mode resistance, R_{icm}. All these aspects can be modeled in the same manner as was done for the opamp. Because the input to the comparator is usually differential, the input common-mode range is also important. The ICMR for a comparator would be that range of input common-mode voltage over which the comparator functions normally. This input common-mode range is generally the range where all transistors of the comparator remain in saturation. Even though the comparator is not designed to operate in the transition region between the two binary output states, noise is still important to the comparator. The noise of a comparator is modeled as if the comparator were biased in the transition region of the voltage-transfer characteristics. The noise will lead to an uncertainty in the transition region as shown in Fig.2.6. The uncertainty in the transition region will lead to jitter or phase noise in the circuits where the comparator is employed.

Dynamic Characteristics:-

The dynamic characteristics of the comparator include both small-signal and large-signal behavior. We do not know, at this point, how long it takes for the comparator to respond to the given differential input. The characteristic delay between input excitation and output transition is the time response of the comparator. Figure 2.7 illustrates the response of a comparator to an input as a function of time. Note that there is a delay between the input excitation and the output response. This· time difference is called the *propagation delay time* of the comparator. It is a very important parameter since it is often the speed limitation in the conversion rate of an



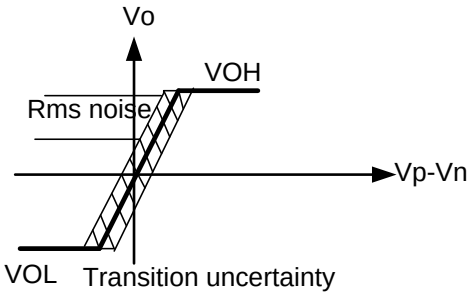


Fig. 2.5 Model for a comparator including input-offset voltage.

Fig. 2.6 Influence of noise on a Comparator.

*A/C*onverter. The propagation delay time in comparators generally varies as a function of the amplitude of the input. A larger input will result in a smaller delay time. There is an upper limit at which a further increase in the input voltage will no longer affect the delay .This mode of operation is called *slewing* or *slew rate.*

The small-signal dynamics are characterized by the frequency response of the comparator. A simple model of this behavior assumes that the differential voltage gain, $A_{v,}$ is given as

$$A_v(s) = \frac{A_v(0)}{\frac{s}{\omega_c} + 1} = \frac{A_v(0)}{s\tau_c + 1} \qquad (2.1)$$

where $\mathbf{A}_v(0)$ is the dc gain of the comparator and $\omega_C = 1/\tau_C$ is the - 3 dB frequency of the single (dominant) pole approximation to the comparator frequency response. Normally, the $\mathbf{A}_v(0)$ and

ω_c of the comparator are smaller and larger, respectively, than for an opamp.

Let us assume that the minimum change of voltage at the input of the comparator the resolution of the comparator. We will define this minimum input voltage to the comparator as

$$V_{in}(\min) = \frac{V_{OH} - V_{OL}}{A_V(0)} \qquad (2.2)$$

For a step input voltage, the output of the comparator modeled by Eq. (2.1)rises (or falls) with a first-order exponential time response from V_{OL} to V_{OH} (or V_{OH} to V_{OL}) . If *Vin* is larger than *Vin(min),* the output rise or fall time is faster. When *Vin(min)* is applied to the comparator, we can write the following equation:

$$\frac{V_{OH} - V_{OL}}{2} = A_V(0)[1 - e^{-T_P / \tau_C}]V_{in}(\min) = A_v(0)[1 - e^{-T_P / \tau_C}](\frac{V_{OH} - V_{OL}}{A_V(0)}) \qquad (2.3)$$

Therefore ,the propagation delay time for an input step of Vin(min) can be expressed as

$$t_p(\max) = \tau_c \ln(2) = 0.693\tau_c \qquad (2.4)$$

This propagation delay time will be valid for either positive-going or negative-going comparator outputs. The propagation delay time is given as

$$t_p = \tau_c \ln(\frac{2k}{2k-1}) \qquad (2.5)$$

where $k = \frac{V_{in}}{V_{in}(\min)}$ $V_{in.}$ (2.6)

Obviously, the more overdrive applied to the input of this comparator, the smaller the propagation delay time. As the overdrive increases to the comparator eventually the comparator enters a large signal mode of operation. Under large-signal operation, a slew-rate limit will occur due to limited current to charge or discharge capacitors.

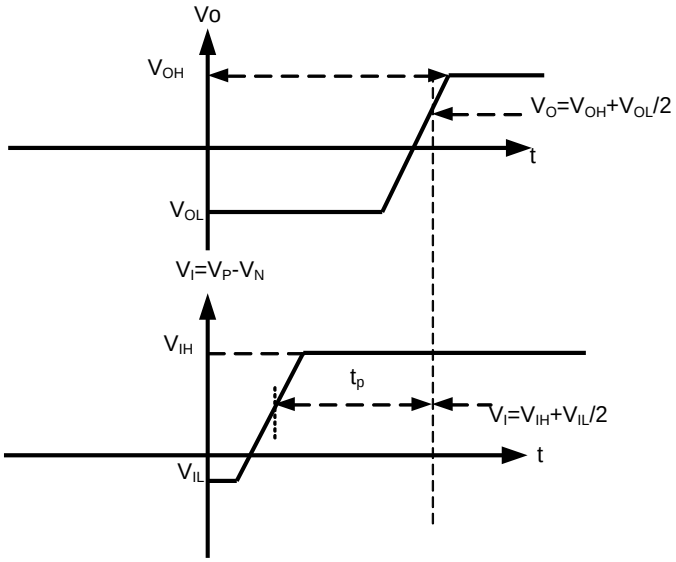


Fig.2.7. Propagation delay time of a noninverting comparator.

If the propagation delay time is determined by the slew-rate of the comparator, then this time can be written as

$$t_p = \Delta T = \frac{\Delta V}{SR} = \frac{V_{OH} - V_{OL}}{2.SR} \qquad (2.7)$$

In the case where the propagation time is determined by the slew rate, the most important factor to decrease the propagation time is increasing the sinking or sourcing capability)of the comparator. A block diagram of a high performance comparator is shown in fig.2.8

2.2. Block diagram of General Type CMOS Comparator:-

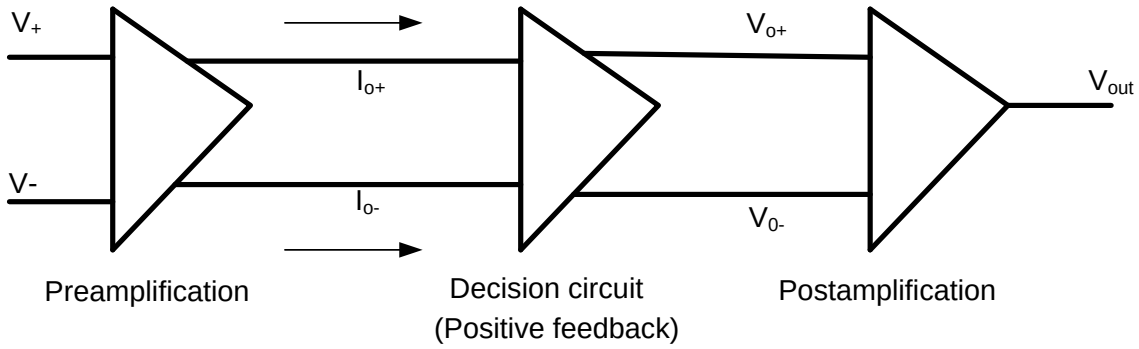


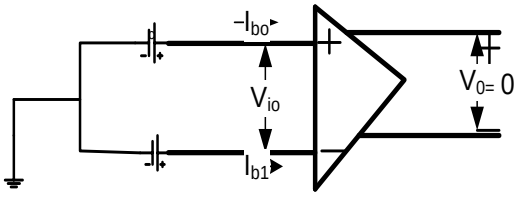
Fig. 2.8 Block diagram of Comparator

There are three stages in this comparator .The pre-amplifier, a positive feedback or decision making stage and an output buffer stage. The pre-amp stage amplifies the input signal to improve the comparator sensitivity (i.e. increases the minimum input signal with which the comparator can make a decision) and isolates the input of the comparator from switching noise coming from the positive feedback stage i.e. kick back noise effect. This noise effect is reduced by using Latched based comparator (discussed in chapter 4). The positive feedback stage is used to determine which of the input signal is larger. The output buffer amplifies this information and outputs a digital signal. Designing a comparator can begin with considering input common mode range, power dissipation, propagation delay and comparator gain. We will develop a basic comparator design using a procedure similar to the basic op-amp.

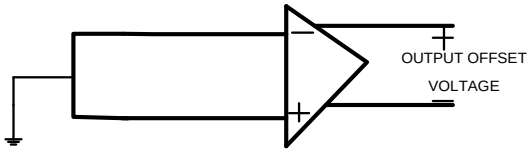
2.3. OFFSET ERROR VOLTAGES AND CURRENTS:-

The ideal operational amplifier shown in Fig. 2.9(a) is perfectly balanced, that is, *Vo* = 0 when Vl = *V2*• A real operational amplifier exhibits an unbalance caused by a mismatch of the input transistors. This mismatch results in unequal bias currents flowing through the input terminals, and also requires that an input offset voltage be applied between the two input terminals to balance the amplifier output. In this section the DC error voltages and currents that can be measured at the input and output terminals.

Input Bias Current :-The input bias current is one-half the sum of the separate currents entering the two input terminals of a balanced amplifier as shown in Fig.2.9(a) the input bias current is *I B = (I* Bl + *I B2)* /2 when *Vo* = O.



2.9 *(a)* Input offset voltage



2.9 *(b)* Output offset voltage.

Input Offset Current:- The input offset current is the difference between the separate currents entering the input terminals of a balanced amplifier. As shown in Fig, *2.9(a),* we have $Ii_o = I\ B1 - I\ B2$ when V_a = O.

Input Offset Current Drift :-The input offset current drift $\Delta I_{io}/\Delta T$ is the ratio of the change of input offset current to the change of temperature.

Input Offset Voltage :-The input offset voltage *Via* is that voltage which must be applied between the input terminals to balance the amplifier, as shown in Fig. *2.9(a).*

Input Offset Voltage Drift:- The input offset voltage drift $\Delta V_i/\Delta T$ is the ratio of the change of input offset voltage to the change in temperature.

Output Offset Voltage The output offset voltage is the difference between the dc voltages present at the two output terminals (or at the output terminal and ground for an amplifier with one output) when the two input terminals are grounded (Fig. *2.9.b).*

Power Supply Rejection Ratio :-The power supply rejection ratio (PSRR> is the ratio of the change in input offset voltage to the corresponding channel in one power supply voltage, with all remaining power supply voltage constant.

Slew Rate :-The slew rate is the time rate of change of the closed loop amplifier output voltage under large-signal conditions.

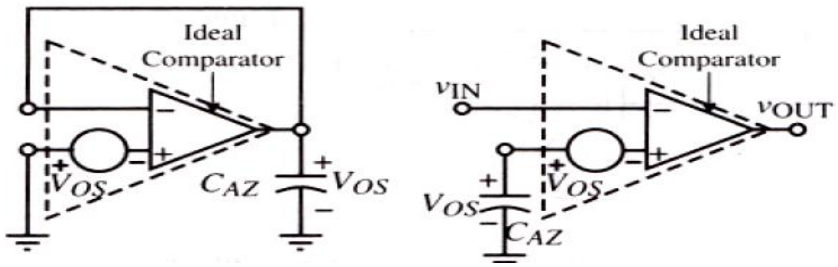
2.4. Improving the Performance of open loop comparators:-

There are two areas in which the performance of an open-loop, high-gain comparator can be improved with little extra effort. These areas are the input-offset voltage and a single transition of the comparator in a noisy environment. The first problem can be solved by *auto zeroing* and the second can be solved by the introduction of hysteresis using a bitable circuit. These two techniques will be examined in the following.

Auto zeroing Techniques:-

Input-offset voltage can be a particularly difficult problem in comparator design. In precision applications, such as high-resolution A/D converters, large input-offset voltages

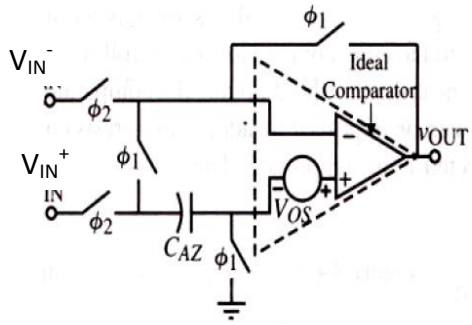
cannot be tolerated. While systematic offset can nearly be eliminated with proper design (though still affected by process variations), random offsets still remain and are unpredictable. Fortunately there are techniques in MOS technology to remove a large portion of the input offset using offset-cancellation techniques. These techniques are available in MOS because of the nearly infinite input resistance of MOS transistors. This characteristic allows long-term storage of voltages on the transistor's gate. As a result, offset voltages can be measured, stored on capacitors, and summed with the input so as to cancel the offset.[6]



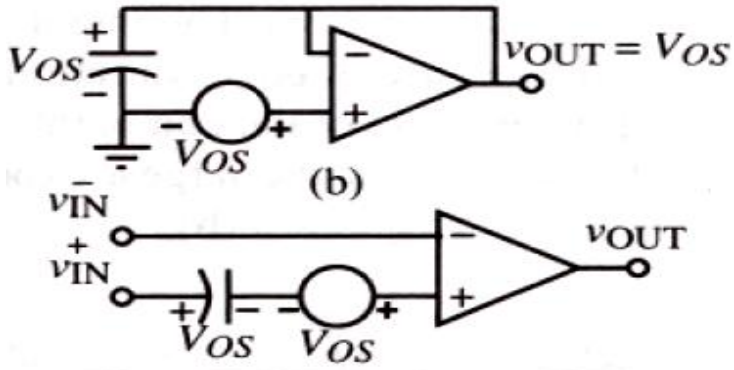
2.10 a) Comparator unity-gain configuration storing the offset on auto zero capacitor C_{AZ} during first half of the auto zero cycle. 2.10 b) Comparator in open-loop configuration offset cancellations achieved at the non inverting input during the second half of the auto zero cycle.

A model of a comparator with an input-offset voltage is shown in Fig (2.10a). A known polarity is given to the set voltage for convenience. Neither the value nor the polarity can be predicted in reality. Figure (2.10a) shows the comparator connected in the unity-gain configuration so that the input offset is available at the output. In order for this circuit to work properly, it is necessary that the comparator be stable in the unity-gain configuration. This implies that only self compensated high-gain amplifiers would be suitable for auto zeroing. One could use the two stage, open-loop comparator but a compensation circuit should be switched into the circuit during auto zeroing. In the final operation of the auto zero algorithms C_{AZ} is placed at the input of the comparator in series with *Vos.* The voltage across C_{AZ} adds to *Vos,* resulting in zero volts at the no inverting input of the comparator. Since there is no de path to discharge the auto zero capacitor, the voltage across it remains indefinitely (in the ideal case). In reality, there are leakage paths in shunt with C_{AZ} that can discharge it over a period of time. The solution to this problem is to repeat the auto zero cycle periodically.

A practical implementation of a differential-input, auto zeroed comparator is [1] shown Fig.(2.11.a). The comparator is modeled with an offset-voltage source as before. Figure (2.11.b) shows the state of the circuit during the first phase of the cycle when ϕ_1 is high. The offset is stored across



2.11 (a) implementation of a differential-input, auto zeroed comparator



(C)

2.11 (b) Comparator during phase φ1, 2.11(c) Comparator during phase φ2 C_{AZ} Figure (2.11.C) shows the circuit in the second phase of the auto zero cycle when ϕ_2 is high. The offset is canceled by the addition of *Vos* on C_{AZ} It is during this portion of the cycle that the circuit functions as a comparator.

Chapter 3

Conventional Comparators

Conventional Three stage CMOS Comparator

3.1. Preamplification

This circuit is a differential amplifier with active loads. The sizes of NM0 and NM1 are set by considering the diff-amp trans-conductance and the input resistance. The trans-conductance sets the gain of the stage, while the input capacitance of the comparator is determined by the size of NM0 and NM1. We will concentrate on speed in the design, and therefore we will set the channel lengths of the MOSFETs to 100nm. (Channel length modulation gives rise to an unwanted offset voltage). Using the sizes given in the schematic, we can relate the input voltages to output currents by

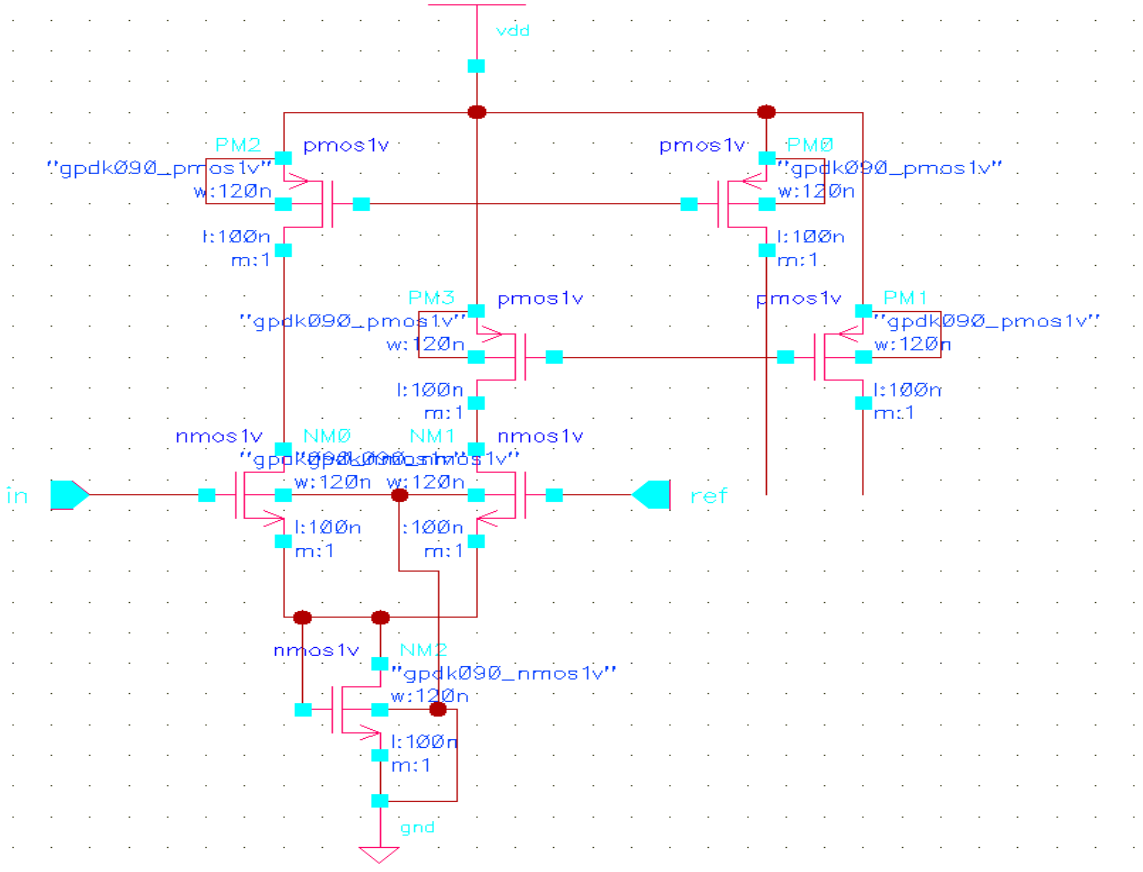


Fig.3.1 Schematic of Pre-amplification stage

$$i_{o+} = \frac{gm}{2}(v_+ - v_-) + \frac{Iss}{2} = Iss - i_{o-} \quad . \qquad (3.1)$$

$$g_m = g_{m1} = g_{m2} \qquad (3.2)$$

To further increase the gain of the first stage, we can size up the widths of MOSFETs PM3 and PM4 relative to the widths of PM0 and PM1.

3.2 Decision circuit:-

The decision circuit is the heart of the comparator and should be capable of discriminating mV level signals. We should also be able to design the circuit with some hysteresis for use in rejecting noise on a signal. The circuit uses positive feedback from the cross-gate connection of NM1 and NM2 to increase the gain of the decision element.

Let's begin by assuming that i_{o+} is much larger than i_{o-} so that M5 and M7 are ON and NM1 and NM3 are off. We will also assume that $\beta_{NM0} = \beta_{NM3} = \beta_A$ and $\beta_{NM1} = \beta_{NM2} = \beta_B$. Under these circumstances, v_{o-} is approximately 0V and v_{o+} is

$$v_{o+} = \sqrt{\frac{2io+}{\beta A}} + V_{THN} \qquad (3.3)$$

If we start to increase i_{o-} and decrease i_{o+}, switching takes place when the drain-source voltage of NM2 is equal to V_{THN} of NM1. At this point, NM1 starts to take current away from NM0. This decreases the drain-source voltage of NM0 and thus starts to turn NM2 off. If we assume that the maximum value of v_{o+} or v_{o-} is equal to $2V_{THN}$,then NM1 and NM2 operate, under steady state $\beta_A=\beta_5=\beta_8$, $\beta_B =\beta_6=\beta_7$.

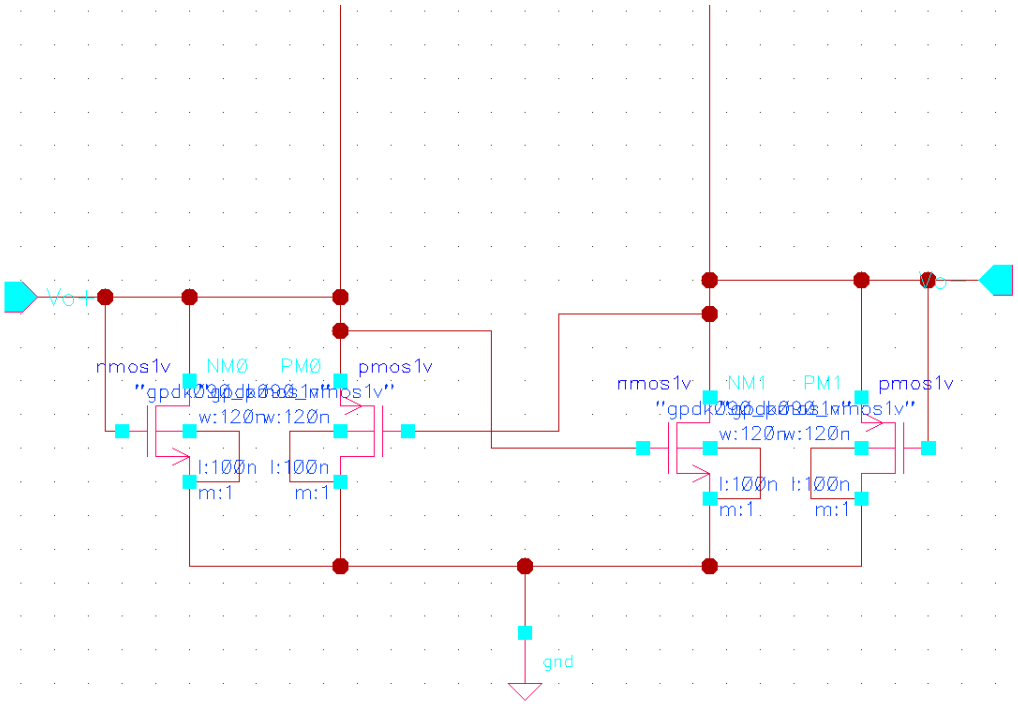


Fig. 3.2 Schematic of Decision circuit

conditions, in either cutoff or the triode regions. Under these circumstances, the voltage across NM2 reaches V_{THN}, and thus NM2 enters the saturation region, when the current through NM2 is

$$i_{o-} = \frac{\beta B}{2}(v_{o+} - V_{THN})^2 = \frac{\beta B}{\beta A}.\, i_{o+} \qquad (3.4)$$

This is the point at which switching takes place. That is , NM2 shuts off and NM1 turns on. If $\beta_A = \beta_B$, then switching takes place when the currents i_{o+} and i_{o-} are equal. Unequal βs cause the comparator to exhibit hysteresis. A similar analysis for increasing i_{o+} and decreasing i_{o-} yields a switching point of

$$i_{o+} = \frac{\beta B}{\beta A}.\, i_{o-} \qquad (3.5)$$

Relating these equations to Eq.(3.1 to 3.5) yields the switching point voltages or

$$V_{SPH} = v_+ - v- = \frac{Iss}{gm}.\frac{\frac{\beta B}{\beta A}-1}{\frac{\beta B}{\beta A}+1} \qquad \text{for } \beta_B \geq \beta_A \qquad (3.6)$$

And $$V_{SPL} = - V_{SPH} \qquad (3.7)$$

3.3 Output Buffer:-

The final component in our comparator design is the output buffer or post-amplifier. The main purpose of the output buffer is to convert the output of the decision circuit into a logic signal (i.e., 0 or 5V). The output buffer should accept a differential input signal and not have slew-rate limitations. The circuit used as an output buffer in our basic comparator design is shown in fig.5.This circuit is a self-biasing differential amplifier. We can see a problem in connecting the decision circuit directly to the output buffer. The MOSFET NM3 is added in series with the decision circuit to increase the average voltage out of the decision circuit. The size of the MOSFET is somewhat arbitrary. We will set W_{17}/L_{17} =5 µm/100nm so that the output of the decision circuit is increased by approximately V_{THN}.

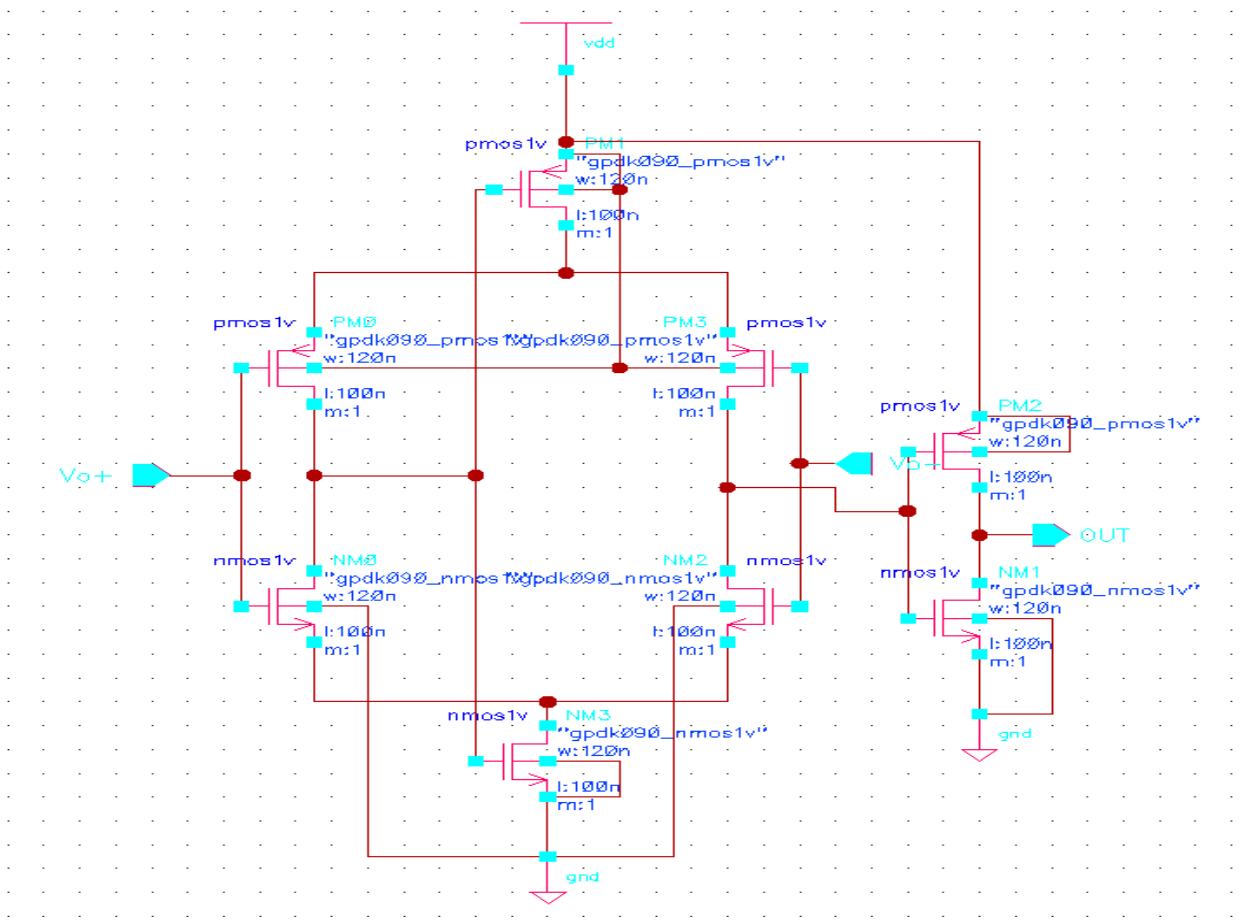


Fig 3.3 Schematic of Output Buffer Circuit

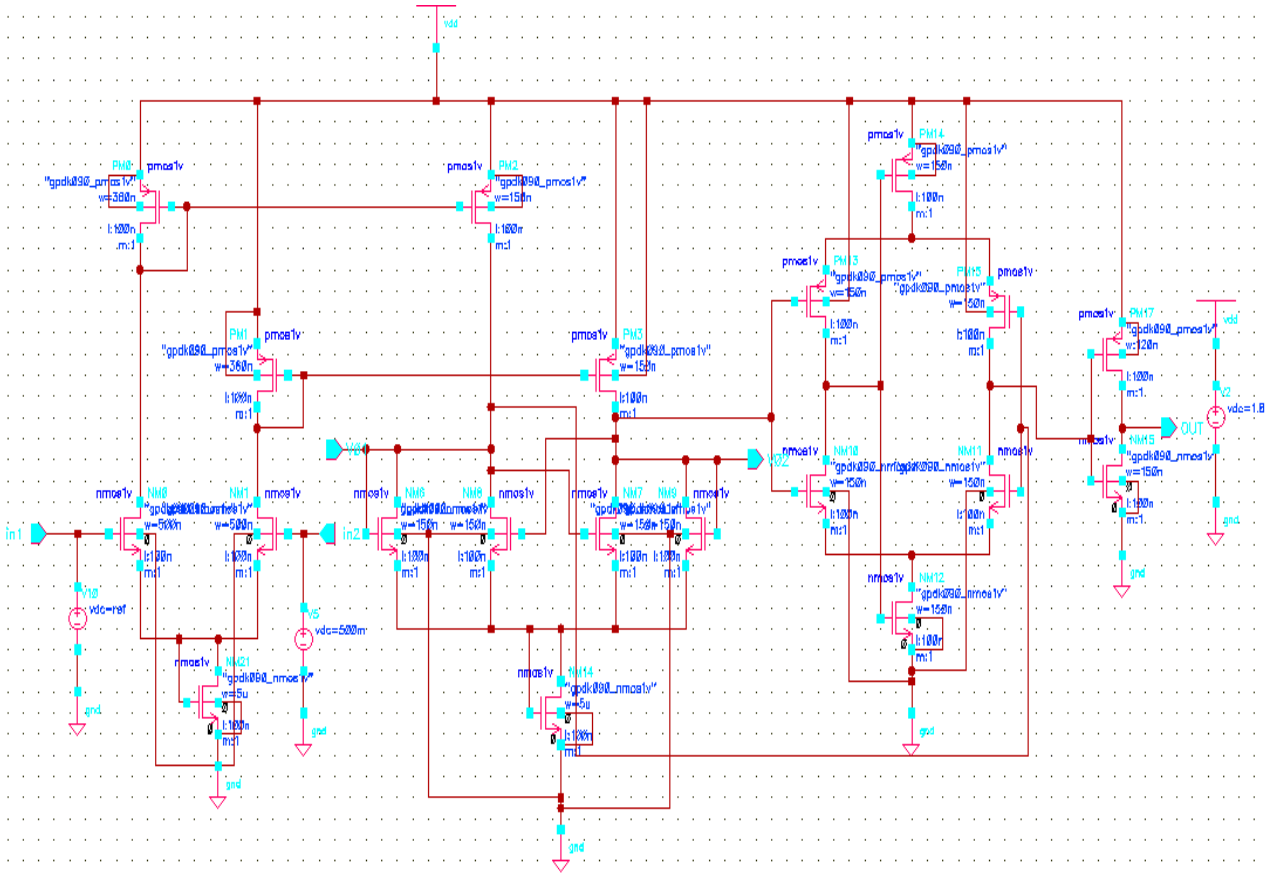


Fig .3.4 Schematic of Preamplifier based Comparator

The complete schematic of the comparator is shown in fig .3.4. Unlabeled MOSFETs are 150nm/100nm. Here the input Voltage as a ref parameter. And sweep this parameter from 0 to 1.8 V. The reference Voltage as 0.5 Volt. So as above the Circuit is connected and the wave forms of the Output Voltages of Decision Circuit and Output Buffer are shown in Fig .7.

Here the reference Voltage as 0.5V.So if the input Voltage is greater than reference Voltage it is giving output Voltage as logic 1.And if the Input Voltage is less than reference Voltage it gives the Output as logic 0.And also the output waveforms are shown. These waveforms are also changing at the reference Voltage.

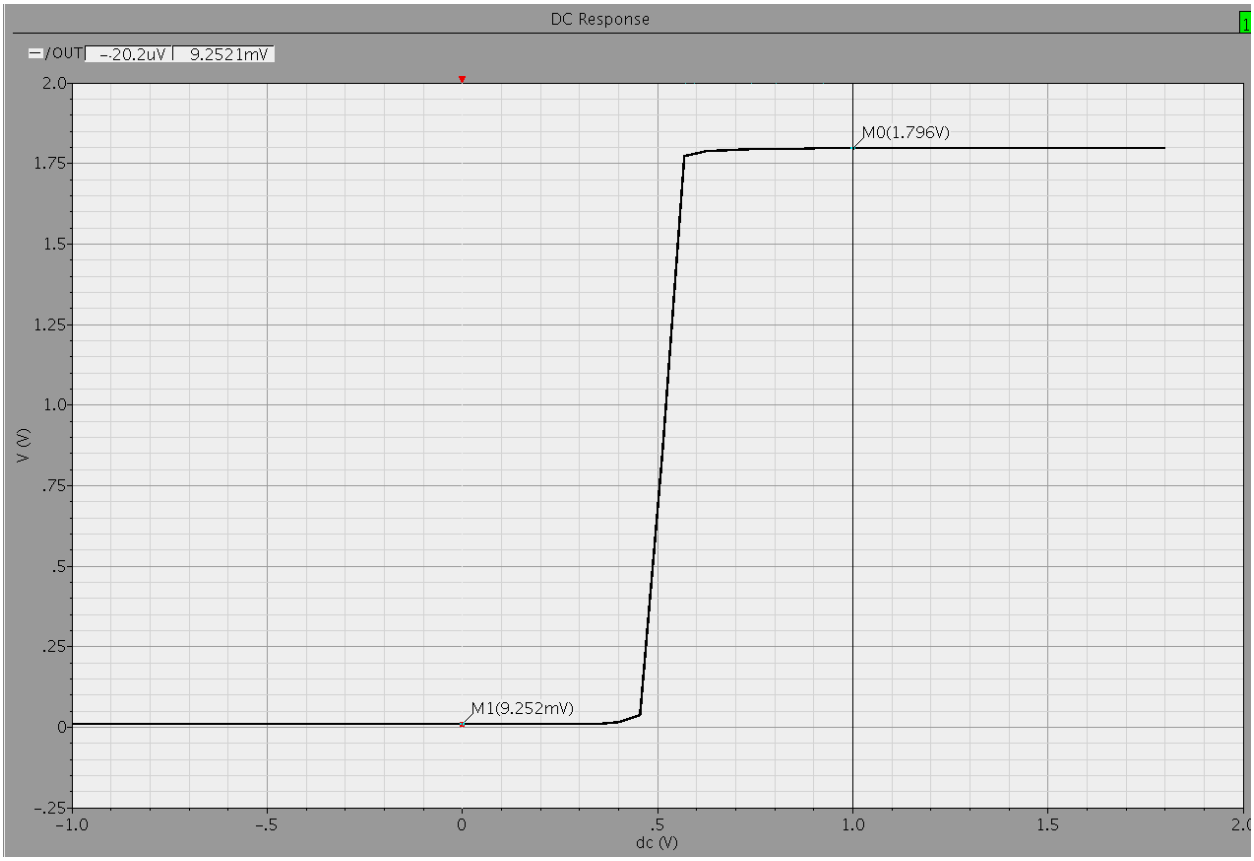


Fig 3.5 Output Waveform of Comparator and Decision Circuit

The offset Voltages are Calculated as shown in Fig.8.Here the DC voltages are connected to 0Volts.And I simulated the circuit for Zero DC voltages. The Waveform of the offset Voltage are shown.

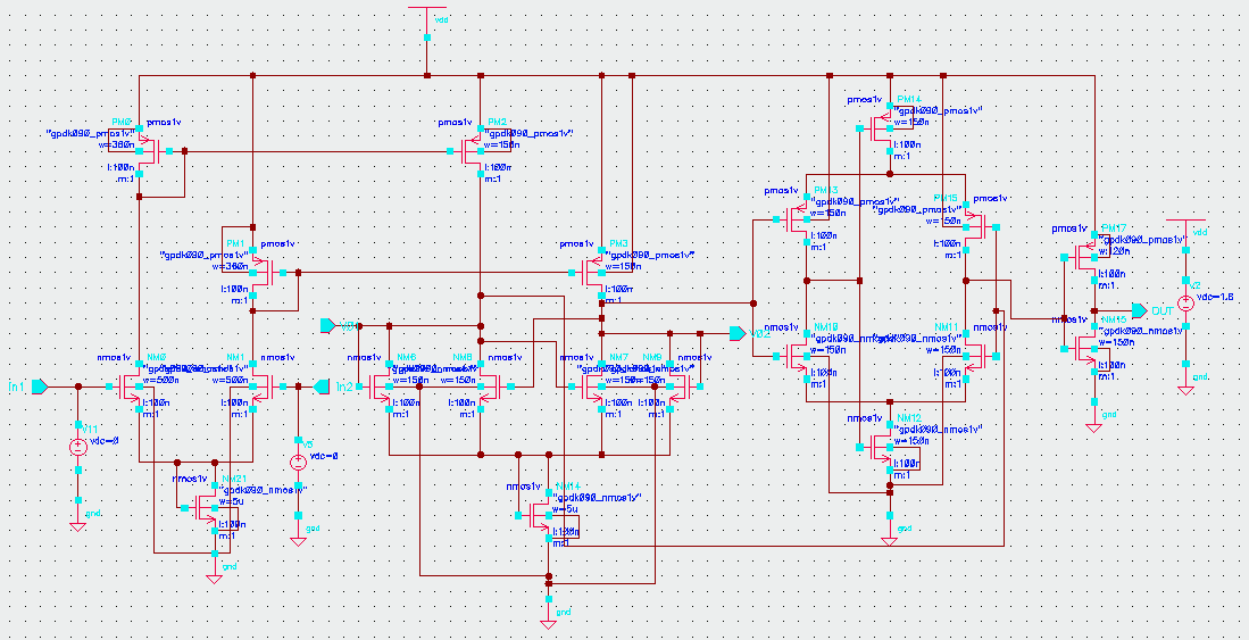


Fig.3.6 Schematic of Offset circuit for Conventional three stage Comparator

Offset voltage is nothing but distance between the origin and the output. Here the input voltage from -1V to 1.8V.If we see the waveform of the offset circuit the offset voltage is 186.1mV.

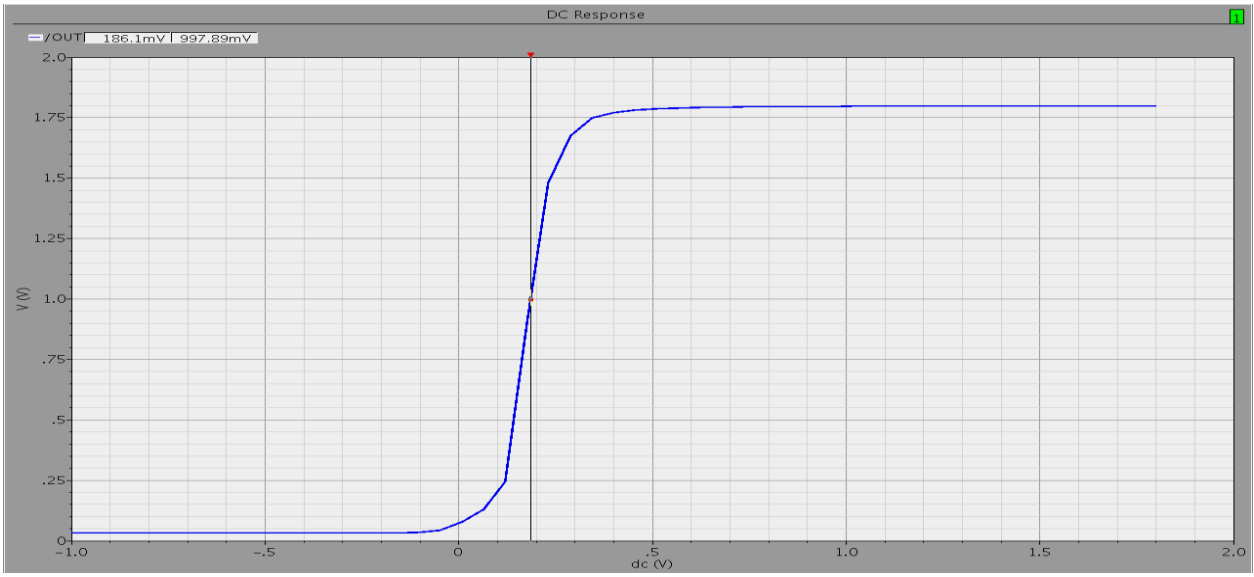


Fig .3.7 Conventional three stage Comparator offset voltage wave form

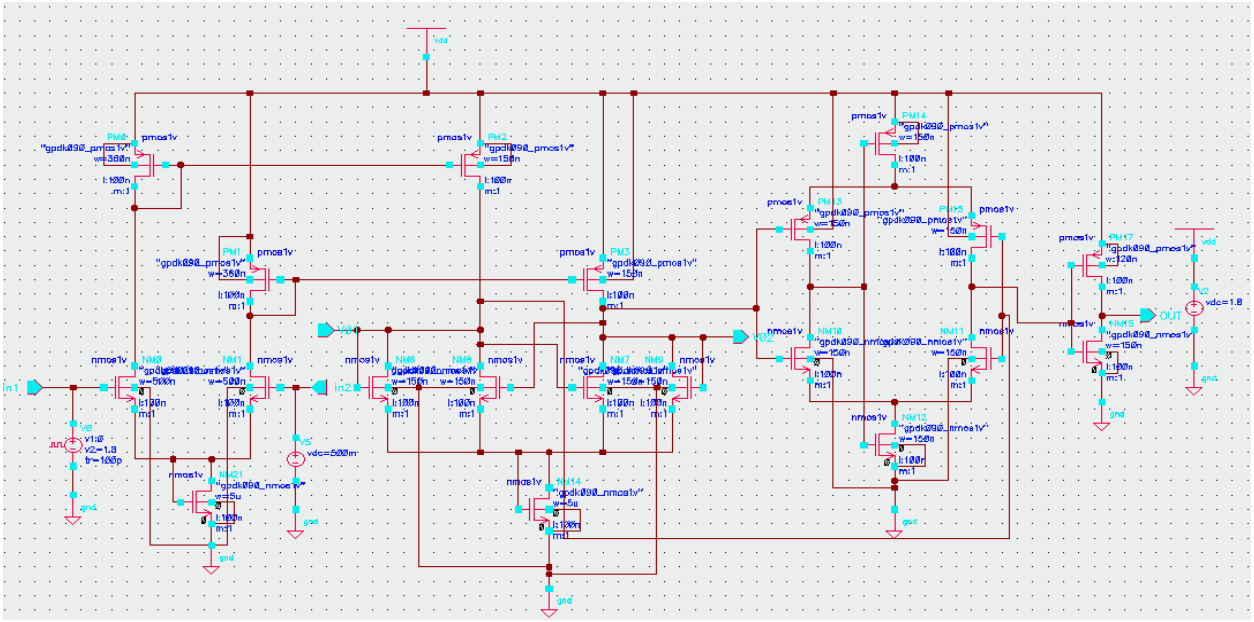


Fig.3.8 Transient analysis of Conventional three stage Comparator

This is the circuit for calculating the delay of the Comparator. So for for calculating the delay of the Comparator I did the Transient Analysis. Here I have given input pulse to the one input of the Pre-amplifier. And I have given 500mv DC Voltage to the other end of the Pre-amplifier.

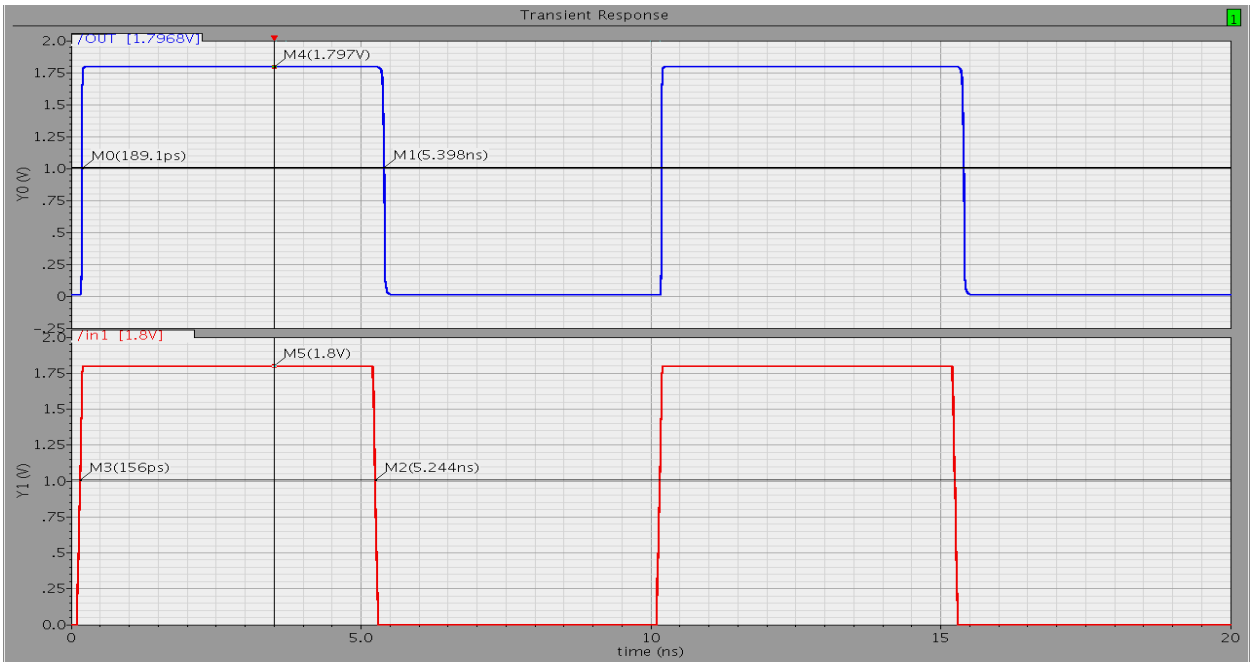


Fig.3.9 Conventional three stage Comparator based comparator transient analysis waveform

3.4 Results

Calculation for Delay and speed for Conventional three stage CMOS comparator

Vir = 158 ps Vif = 5.644ns

Vor = 189.1 ps Vof = 5.398ns

Delay =0.033ns+0.154ns/2 =0.11ns

Speed = 5.78 GHz

Power dissipation= 0.1022 mw

After post layout simulation calculation for Delay and speed for Conventional three stage Comparator

Vir = 158.3ps Vif = 5.644ns

Vor = 0.227ns Vof = 5.51ns

Delay = 0.0707+0.266/2 =0.168ns

Speed = 5.55GHz

Power dissipation = 0.1034 mw

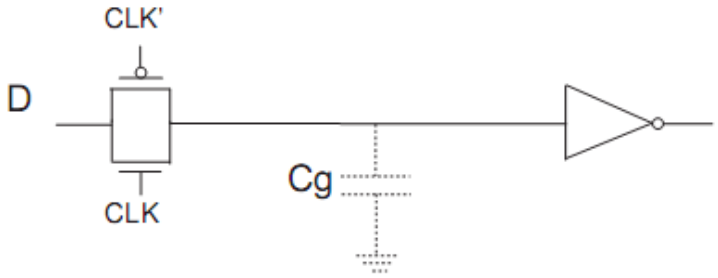
Area = 197.08um^2

Chapter 4

Design of Latched Comparator

4.1 DYNAMIC LATCH

A dynamic latch is defined as the memory unit that stores the charge on the gate capacitance of the inverter. A simple dynamic latch is shown in figure.

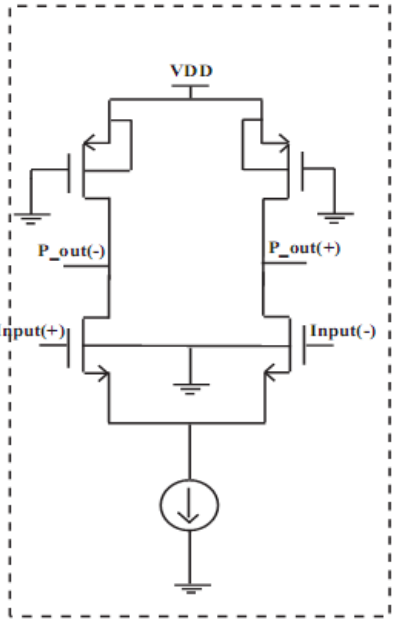


Simple dynamic latch.

The circuit is driven by a clock. During one phase of the clock (clk =1) when the transmission gate is closed, the latch acts transparent, and the inverter is directly connected to the input. In the other phase of the clock (clk = 0), the transmission gate opens and the inverter's output is determined by the node. Setup and hold times determined by the transmission gate must be taken in consideration in order to ensure proper operation of the latch i.e adequate level of voltage is stored on the gate capacitance of the latch.

4.2 PRE-AMPLIFIER

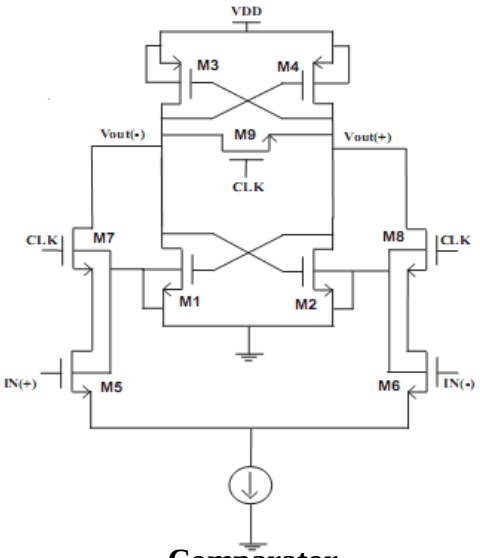
The pre-amplifier used in this design is a simple common source differential amplifier with PMOS transistors as active loads. Pre-amplifier is followed by a small circuit which is basically used for two main functions. First it is used to avoid the kick back effect from the latch to the input signal which is made possible by using two NMOS transistors which operation on the clock. Kick back is the noise observed at the input signal which is produced due to high voltage variations at the regenerative nodes of the latched and is coupled to the input through the parasitic capacitance of the transistors. The second purpose of using the kick back protection circuitry is to create charge imbalance in the latch when it switches from reset mode to regeneration mode.



Pre-amplifier circuit diagram.

4.3 COMPARATOR ARCHITECTURE

The comparator uses the regenerative structure of a dynamic latch. It consists of two inverters connected back to back with each other forming a differential comparator and an NMOS transistor is connected between the two differential nodes of the latch.



Comparator

4.4 COMPARATOR OPERATION

The comparator senses the charge imbalance produced by the input at the pre-amplifier and reacts to that imbalance to create desired digital voltage levels at the output. In this manner this comparator can also be called a current comparator. The whole operation of comparison is divided into two phases of the clock. In the first phase when the clock is high, the switch transistor closes and short-circuits both the outputs of the comparator and set them to certain DC voltage level around mid point of VCC. In the same phase the pre-amplifier creates charge imbalance at the differential nodes of the latch. In the second phase, the pre-amplifier is disconnected from the comparator and the short-circuiting transistor is also switched off. Now the comparator (or the inverter pair) amplifiers the charge imbalance into digital voltage levels on the differential nodes.

SPECIFIC REGENERATIVE STRUCTURE

The following parameters were taken into consideration before finalizing the specific chosen architecture for the latch.

1) SPEED:

   A comparator with only two inverters connected to each other in a closed loop makes the regenerative structure very fast. Primarily because of the simplicity of the circuit as only (two NMOS-PMOS pair) transistors are used in the inverter combination. This reduces the parasitic capacitance and hence high comparison speed can be achieved.

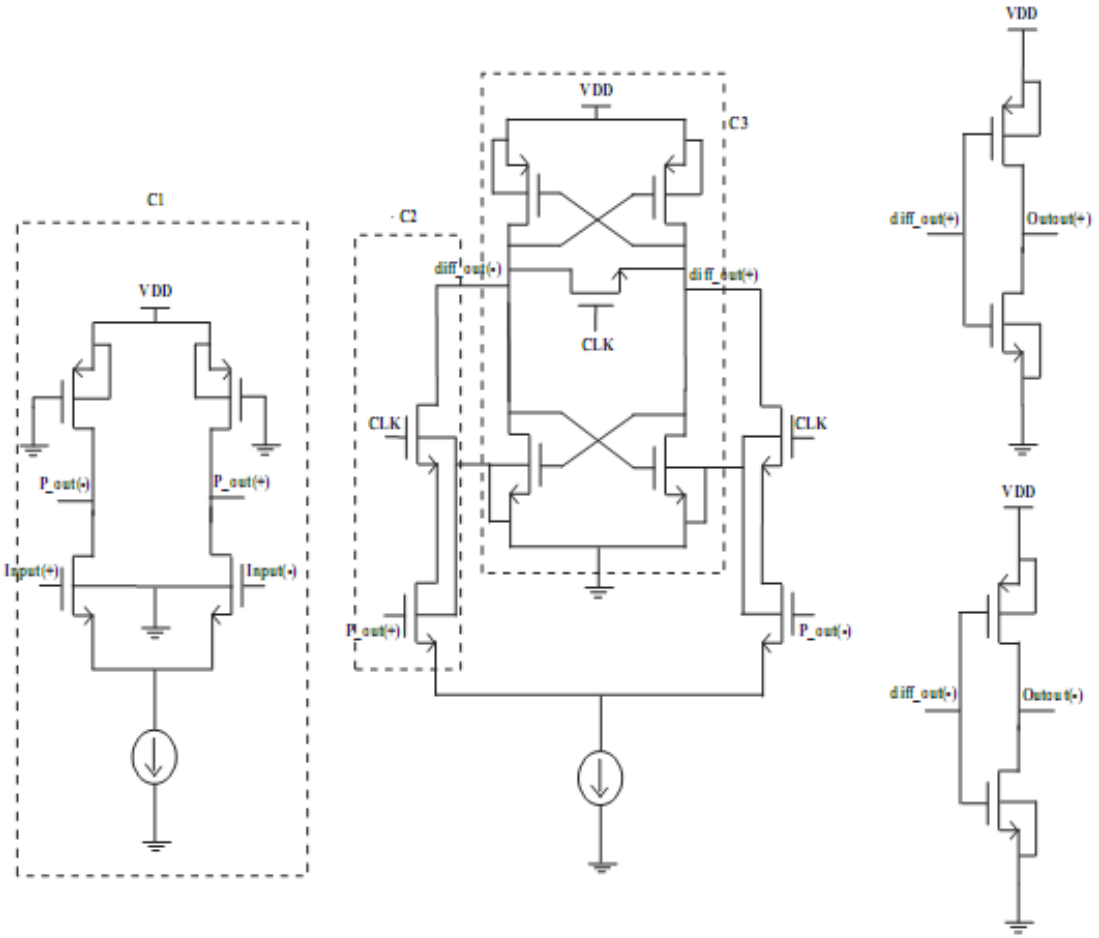
2) RAIL –TO-RAIL OUTPUT:

   As in most of the other designs of the latches, there is always a biasing transistor connected to the source of the NMOS in the regenerative loop. This raises the VOL for the latch and hence minimum value close to the VSS cannot be achieved. In this chosen architecture, the biasing transistor is eliminated and self biasing techniques are used to attain required voltage levels and therefore rail to rail output is closely achieved.

3) RESET:

During the reset phase, the switching transistor short circuits the latch's outputs and the output is set to a point approximately equal to ½ VCC. The advantage for this characteristic feature is that in the second phase the regenerative loop can easily shift the output to the corresponding digital levels as determined by the charge imbalance. This also increases the speed and performance to the comparator. In other comparator designs, the latch is usually set to a floating state in the reset mode, so then chances of correct evaluation decreases as the outputs are not short-circuited to same DC level. This leads to a memory effect in the latch.

4.5 BASIC FUNCTIONALITY



Complete circuit diagram of the latched comparator

Vin (+) and Vin (-) are the two input signals for the pre-amplifier C1. The change in these two signals is amplified by the per-amplifier. From the pre-amplifier, the amplified voltage difference is transferred to the gates of the circuit C2. C2 is a small circuit that creates charge imbalance in the latch and minimizes the kickback noise effects from latch to the pre-amplifier. The latch operates in two phases; reset and regeneration. In the reset phases the charge imbalance is created on the differential nodes of the latch proportional to the variation in the input signal. In regenerator mode, the voltage imbalance on the nodes is amplified to the rail-to-rail digital levels by the NMOS and PMOS regeneration loops.

4.6 NON-LINEARITIES AND PERFORMANCE PARAMETERS

KICK BACK

Almost all the analog to digital converters use various architectures of latched comparators. The latched comparator regenerates the input signal to a full scale digital level. These high voltage level variations at the regeneration nodes are coupled to the input of the comparator through parasitic capacitance of the transistors and disturbs the voltage level of the input signal. This effect is called kick-back. These exits numerous solutions to this problem, few of which are described as follows:

ISOLATION TRANSISTORS

This kind of design of comparator incorporates a set of NMOS transistors that isolates the input signal from the regenerative output nodes, where the voltage variations are large. Hence, this results in low kick back noise. The comparator designed in this work also includes this feature. The disadvantage of using this technique is that it adds parasitic load to the output of the latch, which reduces the operational speed of the latch.

PRE-AMPLIIFIER

The most common solution to reduce the kick back effect is to add pre-amplifier before the comparator. This would increase the power consumption but speed and gain of the system can be increased.

NEUTRALIZATION

This technique is applicable to those circuits in which the differential inputs are directly connected to the regenerative nodes. Voltage variations on the regenerative nodes cause the disturbance on the input due to non-zero impedance of the pre-amplifier mainly caused by Cgd. Adding capacitance equal to Cgd between drain and bulk of input transistor would cancel the noise because the voltage variations as complimentary due to differential signal.

SAMPLING SWITCHES

Inserting sampling switches before in the differential input of the latch reduces the kick back and also can be used in some cases where sampling is required.

CLOCK FEED THROUGH

In the latched comparator architecture[2] that is used in this work contains a single phase clock. This clock is used to set the differential nodes of the comparator to mid point of VCC to clear the memory effect during reset mode. Also this clock signal is connected to the isolation transistors. These transistors disconnect the input signal from the regenerative nodes of the latch during regeneration phase. Switching of the clock produces distortion on the input signal. The following figure (a) shows the parasitic capacitive coupling path of the transistors through which clock feed through effect is observed

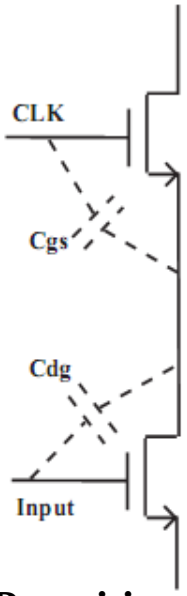


Fig.(a) Parasitic capacitance coupling

In the following figure (b), an undistorted sinusoidal signal is shown as a reference for the clock-feed through effected input signal.

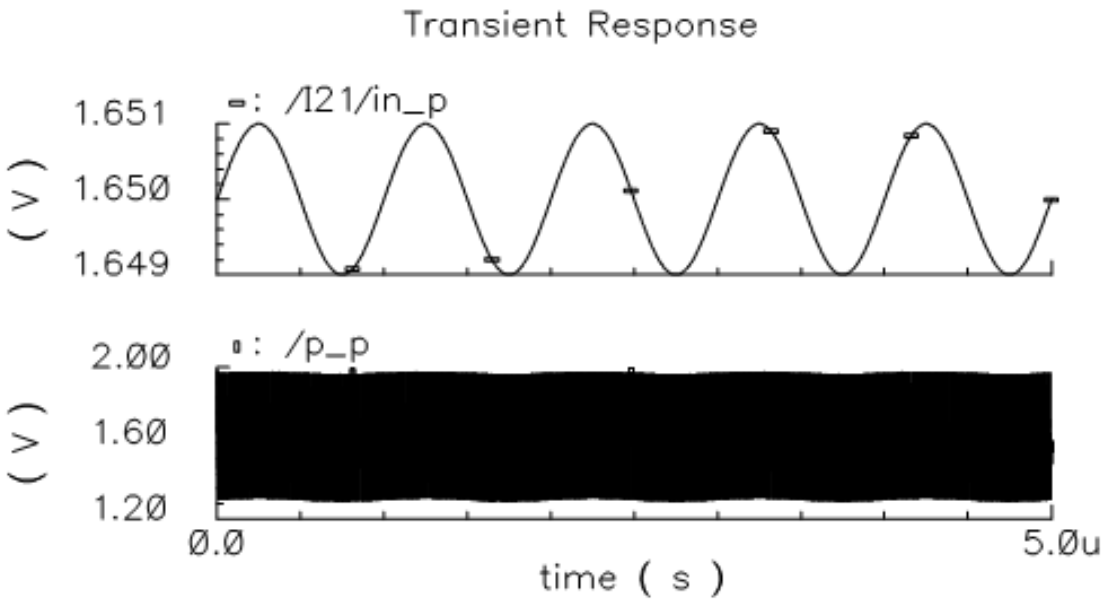
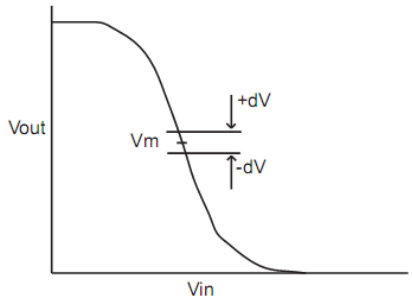


Fig. (b) Clock feed through

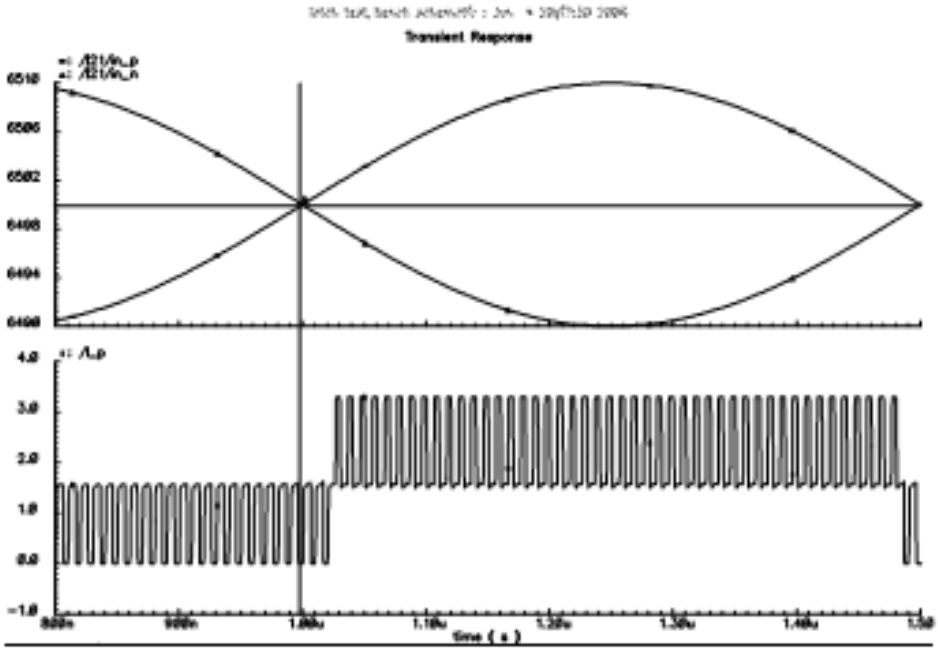
META STABILITY

Normally the output of the inverter has two stable states; either VCC or ground. If the input is set to a mind point, e.g., 'Vm', then ideally the output should also be held at the mid point. This mid point is called "metastable" point. At this point the inverter has maximum gain. If the input is slightly deviating ('Vm'+dV or 'Vm'-dV) from the 'Vm' level, then the output quickly sets either to the supply voltage or to ground. The sensitivity of the inverter is determined by these two factors: 1) gain, and 2) what magnitude of 'dV'does it require to switch its output to corresponding digital voltage level.



Voltage transfer characteristic of inverter

In the above figure, the band between '+dV'and '-dV' indicates the area for the input voltage for which the output is uncertain for its logic level. In this region, due to noise or other disturbances, the output can easily be switched to wrong logic level that is not corresponding to input. This band is basically the bottle neck for the comparator designs. Reducing this metastable band increases the reliability and performance of the comparator.



Comparator offset simulation

COMPARATOR OFFSET

Due to un-symmetries and parasitic in the design, the comparator will exhibit an input-referred offset. The above diagram is the simulation result showing the effects of comparator offset and how it affects the output of the comparator. In this particular case, the width of the 'reset switching capacitor' was slightly changed and it increased the offset error. In the ideal situation, the output should switch as soon as the input differential sinusoids cross each other, but due to the offset error, the accuracy is affected. Other than this 'reset switching capacitor', there are other factors like the bias current, the width of NMOS/PMOS transistor of the regenerative loop and input isolation transistor of the comparator that effect the offset error of the circuit. However, when used in the sigma-delta modulators, the effect of comparator offset is in general

suppressed by the noise-shaping loop and is therefore not as important as comparator memory effects and metastability.

4.7 SPEED OF THE COMPARATOR

Speed of the comparator is highly dependant on the regenerative time constant of the latch. We can model the latch with two inverters connected in the loop with positive feedback configuration as shown in figure (c).

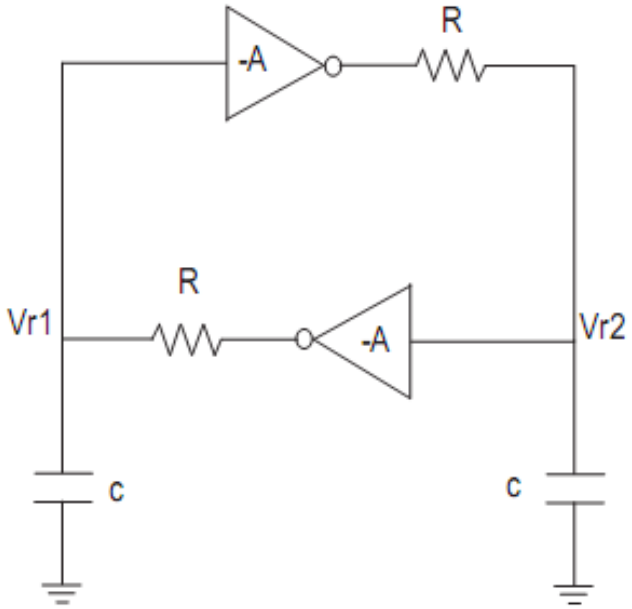


Fig. (c) Model for a comparator

The regenerative nodes are marked as Vr1 and Vr2. These nodes are capable of converting small voltage difference to a full logic level. The time required for the amplification is dependant on the initial voltage difference 'V-diff' which is produced by the pre-amplifier in the form of slight charge disturbance during reset phase. The time required for regeneration is given as:

$$t_{comp} = \frac{(RC)}{A-1}\ln\left(\frac{(Vdiff)}{Vdd}\right)$$

Where ‘A’ is the small signal gain of the inverters. From this equation , it can be observed that the time for comparison depends upon time constant RC, gain of the inverter and initial voltage difference.

4.8 MEAN TIME OF FAILURE

Mean time to failure is an estimation of the average time until a component first failure or disruption of the first operation is observed. As demonstrated in ,If the time given to make a decision is T, and the input follows the uniform distribution between the range ‘-V-diff’ to ‘V-diff’, then the probability that the comparator will not amplify to full logic levels can be written as:

$$P\left(t_{comp} > \frac{T}{2}\right) = e^{(-1)\left(\frac{T}{2}\right)\left(\frac{1}{RC}\right)(A_0 - 1)}$$

Using the above equation of probability, mean time to failure can be calculated as:

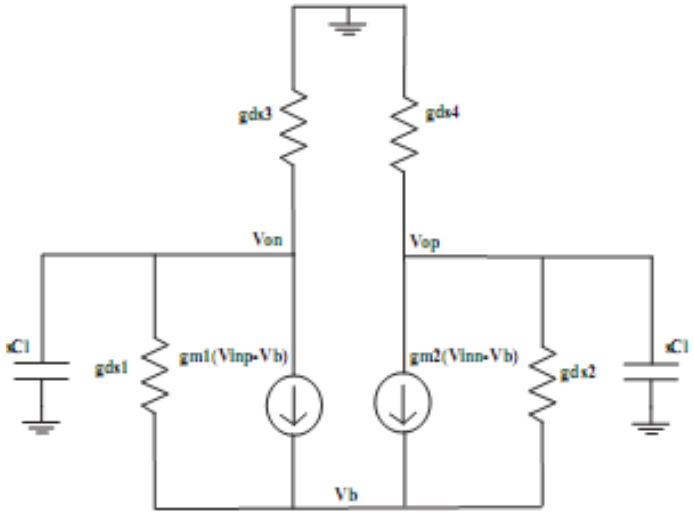
$$MTF = \frac{1}{F_s(P)}$$

Where, ‘Fs’ is the sampling frequency of the latch and ‘P’ is the probability that the comparator will not amplify to full logic levels, In this thesis work, the inverter is modeled as a latch. As inverter is a single pole system, therefore the MTF formula can be further simplified as:

$$MTF = \frac{e^{\frac{(\pi)(F_{unity})}{F_s}\left(1 - \frac{1}{A_0}\right)}}{F_s}$$

4.9 SMALL SIGNAL MODELS FOR THE COMPARATOR

SSM FOR PRE-AMPLIFIER



Small signal model for pre-amplifier

Applying KCL on the circuit, the following equations can be derived for corresponding voltage nodes:

At Von:

$$(Von)gds3 + (Von - Vb)gds1 + (Vinp - Vb)gm1 + (Von)(sCl) = 0$$

At Vop:

$$(Vop)gds4 + (Vop - Vb)gds2 + (Vinp - Vb)gm2 + (Vop)(sCl) = 0$$

At Vb:

$$(Von - Vb)gds1 + (Vop - Vb)gds2 + (Vinp - Vb)gm1$$
$$(Vinn - Vb)gm2 = 0$$

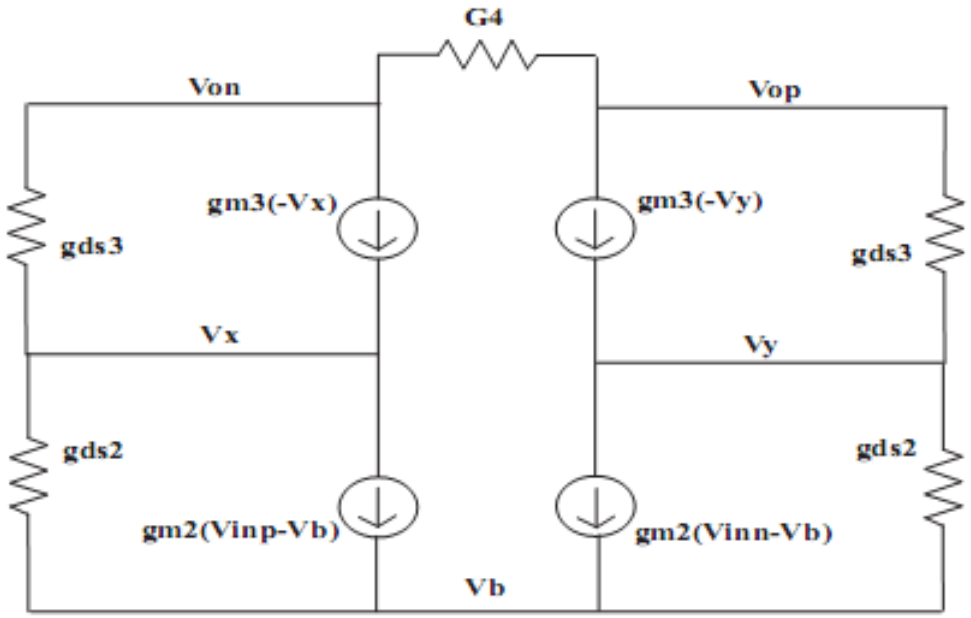
Assuming gds 1 = gds 2 and gm 1 = gm2, then the gain of the Pre-Amplifier is Calculated to be:

$$A = \frac{gm1}{gds1 + gds3 + sCl}$$

And the DC gain is given as:

$$A_0 = \frac{gm1}{gds1 + gds3}$$

SSM FOR KICK BACK CIRCUIT



Small Signal Model for Kick back protection circuitry.

Small signal analysis on this part is carried out for the reset phase of the latch when all the switching transistors are turned 'ON'. During this reset phase, the voltage difference from the pre-amplifier creates a charge imbalance on the regenerative nodes of the comparator through this protection circuitry. This stage has its own gain which is added along with the gain of the pre-amplifier after which the charge imbalance is created on the nodes of the comparator. In this way the effect of the gain of this protection circuit is added to the overall gain of the comparator.

By applying KCL to the small signal model of this circuit, the following equations can be written:

At Vop:

$$(Vop - Von)G4 + gm3(-Vy) + (Vop - Vy)gds3 = 0$$

At Von:

$$(Von - Vop)G4 + gm3(-Vx) + (Von - Vx)gds3 = 0$$

At Vx:

$$gm3(-Vx) + (Von - Vx)gds3 - gm2(Vinp - Vb) - (Vx - Vb)gds2 = 0$$

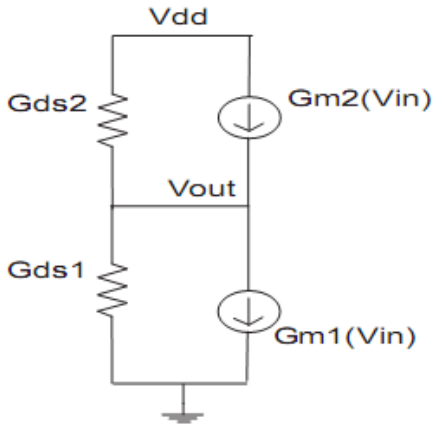
At Vy:

$$gm3(-Vy) + (Vop - Vy)gds3 - gm2(Vinn - Vb) - (Vy - Vb)gds2 = 0$$

The DC gain can be written as:

$$A_0 = \frac{((gm2)(gds3 + gm3))}{(gds2)(gds3) + 2(G4)(gds2 + gds3 + gm3)}$$

SSM FOR THE LATCH



Small signal model of an inverter modeled as latch.

We are interested in calculating the gain of the latch. In the regeneration phase of the comparator, the latch simply acts as a circuit of loop inverters. So for small signal analysis, we can model the latch as an inverter and calculate its gain by applying KCL on the small signal model circuit.

At Vout:

$$-Vout(gds1) = Vout(gds2 + sCl) + Vin(gm1 + gm2)$$

$$A = \frac{(Vout)}{(Vin)} = -\frac{(gm1 + gm2)}{(gds1 + gds2 + sCl)}$$

DC gain can be written as:

$$A_0 = -\frac{gm1 + gm2}{gds1 + gds2}$$

First pole of the latch can be derived as:

$$A = \frac{A_0}{1 + \frac{s}{p_1}}$$

By substituting the values we get:

$$p_1 = \frac{(gds1 + gds2)}{Cl}$$

OVER-ALL GAIN

The overall gain of the comparator is the product of gains of all the three stages:

$$A_{total} = A_{pre} \times A_{kickback} \times A_{latch}$$

4.10 DESIGN DETAILS

PRE-AMPLIFIER

Pre-amplifier design consists of a simple common source differential amplifier. Following the pre-amplifier is a circuit used to create charge imbalance and minimize the kick back effect from the comparator to the input signal.

BIASING TECHIQUE

The pre-amplifier is combination of two differential pairs of NMOS transistor with PMOS transistors acting as active loads. PMOS are connected in a pseudo logic configuration to make it operate in a linear region. The main objectives for proper biasing are that we achieve a high bandwidth, high cutoff frequency, approximately VCC/2DC biasing at the output, and a DC gain of around 10dB. According to the following formula of gain:

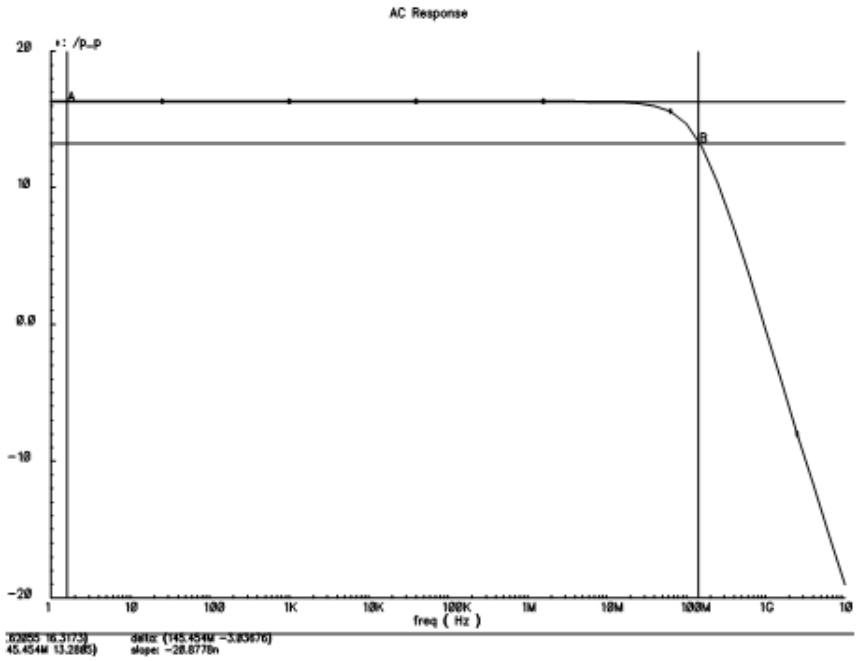
$$A = \frac{(gm1)}{gds1 + gds3 + sCl}$$

Which is derived from the small signal model analysis, the current through the circuit was properly adjusted to achieve desired DC gain. The above equation can be further simplified to give the relation between gain and biasing current

$$A = \frac{\left(\sqrt{2\mu\left(\frac{W_1}{L_1}\right)I_d C_{ox}}\right)}{I_d(\lambda_2 + \lambda_1) + sCl}$$

$$A\alpha\frac{1}{\sqrt{I_d}}$$

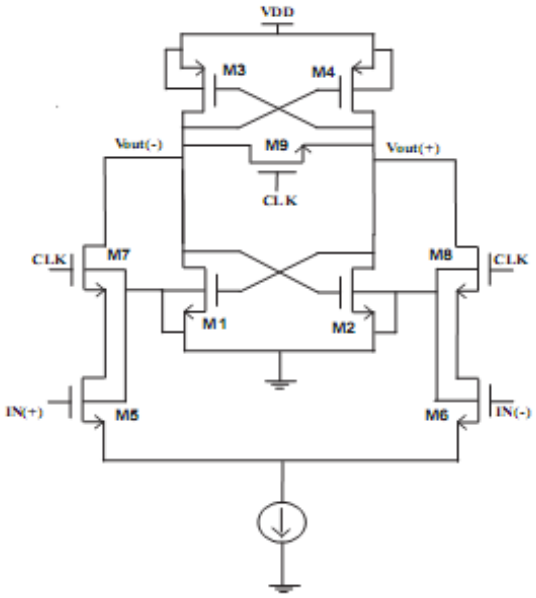
Keeping the sizes of the transistors optimized allowed the circuit to have less parasitic capacitance which increased its cut-off frequency. Increasing the size of the load PMOS takes the DC biasing closet to VCC and increasing the size of NMOS bring the DC level close to ground. Through this sizing strategy of the transistors, the output DC biasing was also set around VCC/2. The purpose of setting the output close to VCC/2 is to make the latch operate properly in its metastable region where maximum gain of the comparator could be achieved.



Gain and -3dB cut-off frequency for Pre-amplifier

LATCH DESIGN DETAILS

The Latch is the most sensitive part in the comparator design.



Comparator schematic

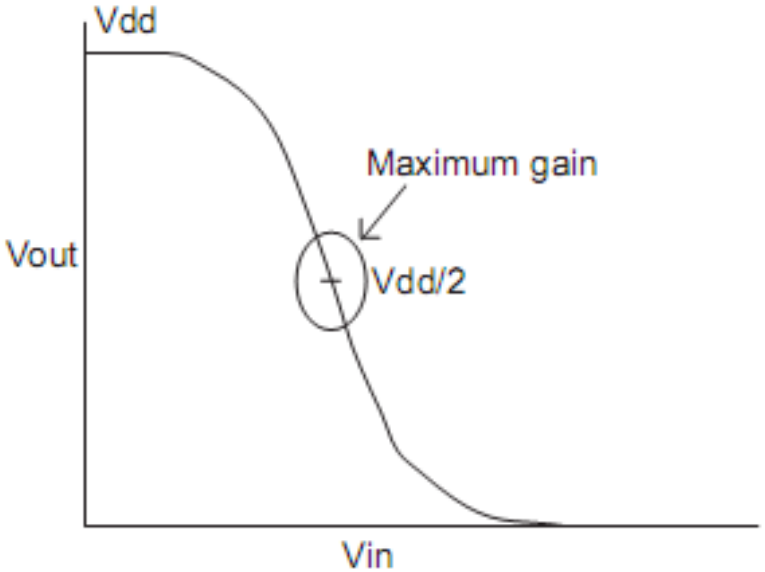
4.11 COMPARATOR DESIGN AND TRANSISTOR SIZING

Step:1

The cross coupled inverter pair was first separately designed. Each inverter following the typical rule of CMOS inverter transistor sizing i.e. the size of PMOS is almost equal to three times size of NMOS. Then the sizes of these transistors were optimized so that the DC biasing is kept a little bit more than the mid point of supply voltage. Also the widths of the transistors were kept minimum size i.e. 180 nm to cater for speed as a digital design. The sizes of the transistors were adjusted in a manner that the circuit remains self biased.

Step:2

Now the inverter pair was connected to the charge imbalance creating circuitry which consist of transistor M5-M8. A switching NMOS transistor M9 is connected between the differential output nodes of the latch. When the extra circuitry is connected to the cross coupled inverter pair, then its pulls down the DC operating point of the latch, that is why initially it was set a bit above mid point to VCC. So, after connecting the rest of the transistor i.e. M5-M10, then final DC operating point because during the reset phase the outputs are short-circuited to this voltage level just when entering into the next phase of regeneration, then at this voltage level, the latch has the maximum gain which can be observed from voltage transfer curve of an inverter.



Voltage transfer curve for a typical inverter.

TWO PHASE OPERATION

Reset and regeneration are the two phase for one comparison cycle of the comparator. In the reset phase, VCC is applied at the gates of the transistor M9, M7 and M8. M9 short circuits the differential nodes where as M6 and M8 provide a connection of input to the differential nodes of the latch.

1) RESET PHASE:

   Reset phase is regarded as the duration when clock is high. In this phase M7 and M8 are switched 'ON', connecting the output of the pre-amplifier to the differential nodes of the latch through transistor M5 and M6 respectively. Also the transistor M9 is switched 'ON' which short circuits the node Vout (-) and Vout (+) to a DC level of 1.65 Volts. The significance of having this reset phase is, first, that the differential nodes are set to a certain DC value which removes the memory effect in the latch.

2) REGENERATION PHASE:

   Regeneration phase starts as soon the clock turns from high to low. In this phase the M7, M8 and M9 and M9 turn OFF and then the inverter pair moves the either of the Vout (+) and Vout (-) nodes to VCC or GND depending upon the charge imbalance created due to the difference in the input signal. The speed of voltage transition depends upon the gain of the inverter, biasing current, and sizes of the transistors.

EFFECT OF TRANSISTOR SIZES ON THE PERFORMANCE

1) TRANSISTOR M1-M4:

   Transistor M1-M4 constitutes the cross-coupled inverter pair structure which forms the main regenerative loop for the latch. Their sizes for length and width are kept minimum for least capacitive effects, and W/L ratio is kept as for an ideal inverter. Sizes are further optimized to set the meta stable trip point of the inverter to half of the supply voltage.

2) TRANSISTOR M9:

This switching transistor M9 short circuits the latch's differential nodes to a common DC level. An advantage of increasing its width is that it brings the DC level on both nodes close to each other but on the other hand, increasing the width also increase the charge injection which degrades the sensitivity of the latch

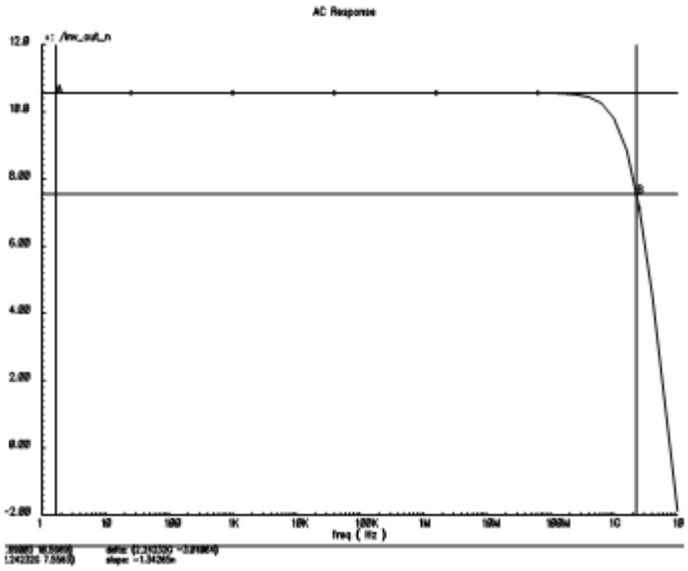
It is clear that charge injection increase by increasing the width of transistor M9, but on the other hand it improves the accuracy of the comparator. So, there exists a trade-off between charge injection and accuracy of the comparator. Ideally the width of M9 should be adjusted to a value where we can achieve minimum charge injection and reasonable accuracy.

3) TRANSISTOR M7 and M8:

These transistors are used to avoid the clock feed through and kickback effects from the latch to the input. Width of these transistors also effects the performance of the latch. If the width is increased, it adds to the equivalent capacitance on the nodes of the latch and increases the effect of clock feed through on the input; resulting in degradation in sensitivity of latch. If the width is decreased, then input signal has to be increased otherwise charge imbalance on the latch is not properly created.

4.12 GAIN AND BANDWIDTH OF COMPARATOR

The comparator is modeled as an inverter and on the output has been loaded by the capacitance of 2.1fF that is present at the regenerative node of the comparator.



Gain and bandwidth of inverter used in the latch.

The input DC biasing for the inverter is kept 1.56V which is same as the reset voltage on the regenerative nodes of the comparator. From this configuration, the result are obtained as follows: Gain is 11dB,-3dB frequency is 2.2GHz, and output resistance is calculated to be 28K Ohms.

4.13 SENSITIVITY

The current design of the latched comparator is able to respond on the differential voltage difference of around 2uV peak to pack at the input of the circuit. Any value less than 2uV is not detectable by comparator. The maximum sampling frequency observed through simulations is 125 Msps for a 50% duty-cycle of the sampling clock. If the duty-cycle is increased to 70%, the sampling frequency can be increased to 200MSps, keeping all other parameters the same. This is due to the fact that the latch part of the comparator is vary fast and this makes it possible to have a quite short regeneration phase, i.e., a short time for which the clock signal is low. With a duty-cycle larger than 50%, the time for resetting the latch to the mid-point is increased, necessary for increase sampling frequency operation.

It is observed that the inverter used in this thesis work has the maximum gain at the metastable point which is at 1.65V. But in the design, the inverters of the regenerative loops are biased at 1.561V at the reset phase. Although biasing the inverter at 1.561 V gives relatively less gain, the sensitivity of the latch is improved. At 1.65V biasing, the latch's sensitivity is degraded, compared with the current configuration, where the sensitivity is 2uV. Raising the biasing to 1.65V reduces the power consumption and increases the speed but reduces the sensitivity, so therefore there exists a trade-off between power consumption, speed and sensitivity.

4.14 MTF CALCULATION

Since the comparator is intended to be used in sigma-delta modulator loops, memory effects and meta stability is of primary interest. The mean time to failure is therefore one of the important design parameter for the latch. MTF is calculated to be nearly infinite. This is due to the high bandwidth of the latch.

4.15 DESIGN PARAMETERS AND PERFORMANCE

From the simulation results of the latched comparator, the following design and performance parameters were calculated:

Power consumption	1.58mW
Mean time to failure	Infinite
Sampling frequency	200MHz@ 70% duty-cycle
Input sensitivity	2uV (differential)
Pre-amplifier unity gain frequency	168MHz
Kickback stage gain	-8.9dB
Latch DC gain	11dB
Latch output resistance	23KOhms
Latch -3dB cutoff frequency	2.8GHz
Latch unity gain frequency	9.8GHz
Input DC offset	1.58V

SPEED OF THE DESIGNED COMPARATOR

By analyzing the frequency response of the pre-amplifier and latch, it is evident that the system can be operated at much greater frequencies than 100 MHz. However, currently the speed is limited to sampling frequencies up to 100 MHz. Here the bottle neck for the speed is the kick back protection circuit. As observed from simulation of the circuit, the unity-gain frequency of the pre-amplifier and the kick back protection circuit together is some 360 MHz which limits the sampling speed of the comparator. Therefore it can be concluded that if this circuit can be modified, then speed of the current architecture of latched comparator can be increased.

After post layout simulation calculation for Delay and speed for Latch based comparator

Vir = 0.156ns Vif = 5.244ns

Vor = 0.9712ns Vof = 5.52ns

Delay = 0.08152+0.0276 /2 =0.09532ns

Speed = 8.79GHz

Power Dissipation = 1.79 mw

Area =168.36um^2 .

Conclusion:

The latch based Comparator is simulated in GPDK 90 nm .The simulation results of latch based comparator shows that delay is 0.09532ns,Speed is 8.79GHz ,Power Dissipation is 1.79 mW. So that in this thesis Latched based comparators are chosen for less offset voltage, high Speed and these architectures are explained in the Appendix.

Chapter 5

CMOS Comparator with internal Hysteresis Design

5.1 Comparator with Hysteresis

It the input to a comparator contains a large amount of noise; the output will be erratic when V_{in} is near the trip point. One way to reduce the effect of noise is by using a comparator with positive feedback. The positive feedback produces two separate trip points that percent a noisy input from producing false transitions.

5.2 Noise

Noise is any kind of unwanted signal that is not derived from or harmonically related to the input signal. Electric motors, neon signs, power lines, car ignitions, lightning, and so on, produce electromagnetic fields that can induce noise voltages into electronic circuits. Power-supply ripple is also classified as noise since it is not related to the input signal. By using regulated power supplies and shielding, we usually can reduce the ripple and induced noise to an acceptable level.

Thermal noise, on the other hand, is caused by the random motion of free electrons inside a resistor. The energy for this electron motion comes from the thermal energy of the surrounding air. The higher the ambient temperature, the more active the electrons.

The motion of billions of free electrons inside a resistor is pure chaos. At some instants, more electrons move up than down, producing a small negative voltage across the resistor. At other instants, more electrons move down than up, producing a positive voltage. Like any voltage, noise has an rms or effective value. As an approximation, the highest noise peaks are about four times the rms value.

The randomness of the electron motion inside are resistor produces a distribution of noise at virtually all frequencies. The rms value of this noise increases with temperature, bandwidth, and resistance. For our purposes, we need to be aware of how noise may affect the output of a comparator.

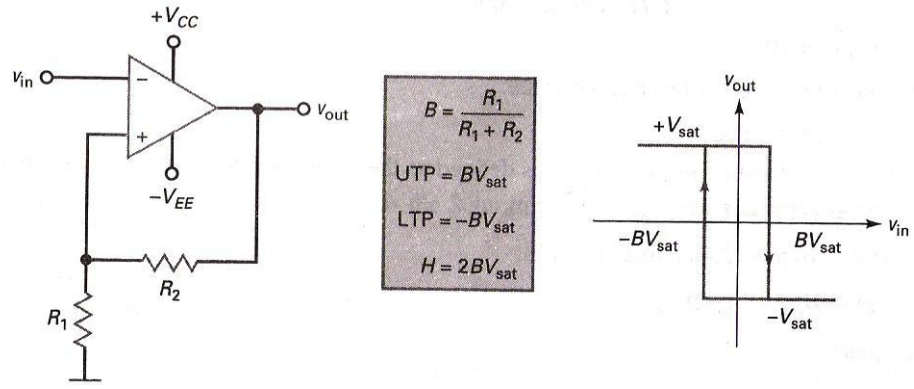
5.3 POSITIVE FEEDBACK

The standard solution for a noisy input is to use a comparator like the one shown in Fig. 5(A) (a). The input voltage is applied to the inverting input. Because the feedback voltage is aiding the

input voltage, the feedback is *positive*. A comparator using positive feedback like this is usually called a Schmitt trigger.

When the comparator is positively saturated, a positive voltage is feedback to the non-inverting input. This positive feedback voltage holds the output in the high state. Similarly, when the output voltage is

(*a*) Inverting Schmitt trigger; (*b*) input/output response has hysteresis. **Fig.5 (A)**



Negatively saturated, a negative voltage is feedback to the non-inverting input, holding the output in the low state. In either case, the positive feedback reinforces the existing output state.

$$B = \frac{R_1}{R_1 + R_2}$$

When the output is positively saturated, the reference voltage applied to the non-inverting input is:

$$V_{ref} = +BV_{sat}$$

When the output is negatively saturated, the reference voltage is:

$$V_{ref} = +BV_{sat}$$

The output voltage will remain in a given state until the input voltage exceeds the reference voltage for that state. For instance, if the output is positively saturated, the reference voltage is $+BV_{sat}$. The input voltage must be increased to slightly more than $+BV_{sat}$ to switch the output voltage from positive to negative, as shown in Fig.5(A) (b). Once the output is in the negative

state, it will remain there indefinitely until the input voltage becomes more negative than $-BV_{sat}$. Then, the output switches from negative to positive.

5.4 INVERTING CIRCUIT

The unusual response of Fig.5 (A) (b) has a useful property called hysteresis. To understand this concept, put your finger on the upper end of the graph where it says $+V_{sat}$. Assume that this is the current value of output voltage. Move your finger to the right along the horizontal line. Along this horizontal line, the input voltage is changing but the output voltage is still equal to $+V_{sat}$. When you reach the upper right corner, v_{in} equals $+BV_{sat}$. When v_{in} increases to slightly more than $+BV_{sat}$, the output voltage goes into the transition region between the high and the low states.

If you move your finger down along the vertical line, you will simulate the transition of the output voltage from high to low. When your finger is on the lower horizontal line, the output voltage is negatively saturated and equal to $-V_{sat}$.

To switch back to the high output state, move your finger until it reaches the lower left corner. At this point, v_{in} equals $-BV_{sat}$. When v_{in} becomes slightly more negative than-BV_{sat}, the output voltage goes into the transition from low to high. If you move your finger up along the vertical line, you will simulate the switching of the output voltage from low to high.

In Fig 5(A) (b) , the trip points are defined as the two input voltage where the output voltage changes states. The upper trip point (UTP) has the value:

$$\boldsymbol{UTP = BV_{sat}}$$

And the lower trip point (LTP) has the value:

$$\boldsymbol{LTP = -BV_{sat}}$$

The difference between these trip points is defined as the hysteresis (also called the deadband):

$$\boldsymbol{H = UTP-LTP}$$

With Eqs. (22-6) and (22-7), this becomes:

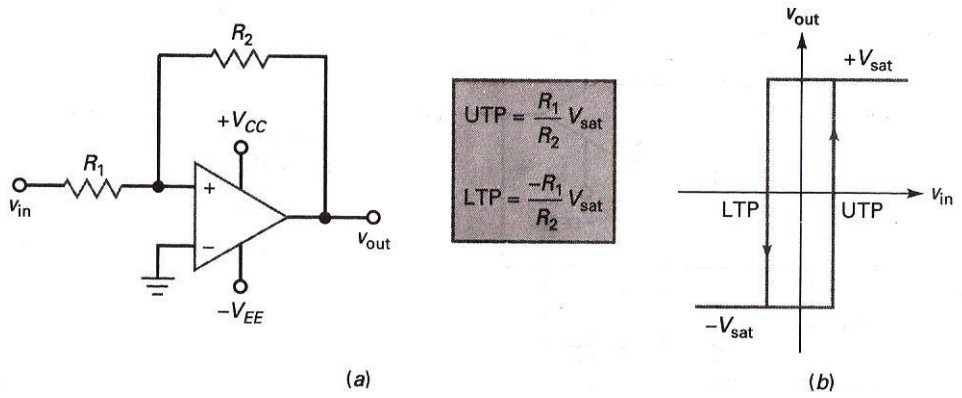
$$\boldsymbol{H = BV_{sat}- (-BV_{sat})}$$

Which equals:

$$\boldsymbol{H = 2BV_{sat}}$$

(*a*) Noninverting Schmitt trigger; (*b*) input/output response.

Fig. 5 B



Positive feedback causes the hysteresis of Fig.5 (A) (b), If there were no positive feedback, *B* would equal zero and the hysteresis would disappear, because both trip points would equal zero. Hysteresis is desirable in a Schmitt trigger because it prevents noise from causing false triggering. If the peak-to-peak noise voltage is less than the hysteresis, the noise cannot produce false trigger is immune to false triggering as long as the peak-to-peak noise voltage is less than 2 V.

5.5 Non-inverting Circuit

Figure 5 (B) shows a non-inverting Schmitt trigger. The input/output response has a hysteresis loop, as shown in fig. 5 (B). Here is how the circuit works: If the output is positively saturated in Fig5 (B)(a) , the feedback voltage to the non-inverting input is positive, which reinforces the positive saturation. Similarly, if the output is negatively saturated, the feedback voltage to the non-inverting input is negative, which reinforces the negative saturation.

Assume that the output is negatively saturated. The feedback voltage will hold the output in negative saturation until the input voltage becomes slightly more positive than UTP. When this happens, the output switches from negative to positive saturation. Once in positive saturation, the output can change back to the negative state.

The equations for the trip points of a non-inverting Schmitt trigger are given by:

$$\mathbf{UTP} = \frac{R_1}{R_2} \mathbf{V_{sat}}$$

$$\mathbf{LTP} = \frac{-R_1}{R_2} \mathbf{V_{sat}}$$

The ratio of R_1 to R_2 determines how much hysteresis the Schmitt trigger has. A designer can create enough hysteresis to prevent unwanted noise triggers.

5.6 Speed-Up Capacitor

Besides suppressing the effect of noise, positive feedback speeds up the switching of output states.

When the output voltage begins to change, is feedback to the non-inverting input and amplified, forcing the

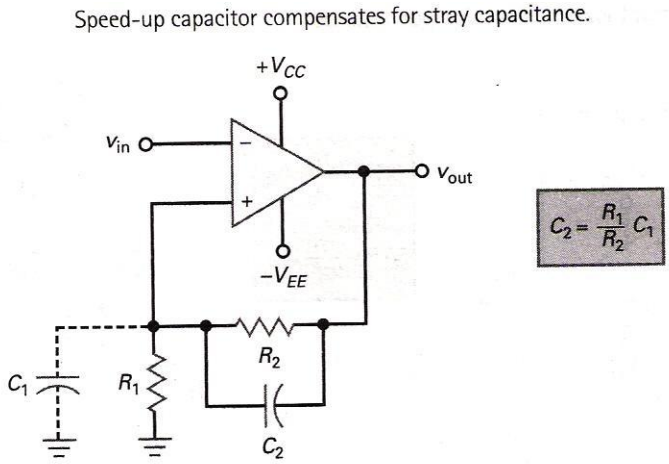


Fig.5 (C)

Output to change faster. Sometimes a capacitor C_2 is connected in parallel with R_2, as shown in Fig.5 (C) Known as a **speed-up capacitor,** it helps to cancel the bypass circuit formed by the stray capacitance across R_1. This stray capacitance C_1 has to be charged before the non-inverting input voltage can change. The speed-up capacitor supplies this charge.

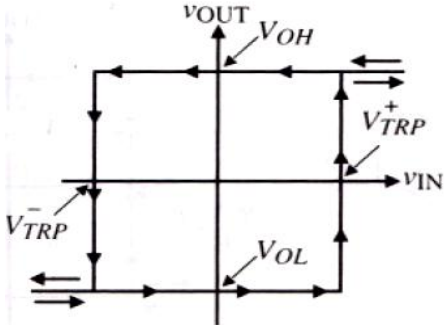
To neutralize the stray capacitance, the minimum speed-up capacitance must be at least:

$$C_2 = \frac{R_1}{R_2} C_1 \qquad \text{(a)}$$

As long as C_2 is equal to or greater than the value given by Eq.(a), the output will switch states at maximum speed. Since a designer often has to estimate the stray capacitance C1, he or she usually makes C_2 at least two times larger than the value given by Eq.(a) In typical circuits C_2 is from 10 to 100 pF.

5.7 Basic Theories

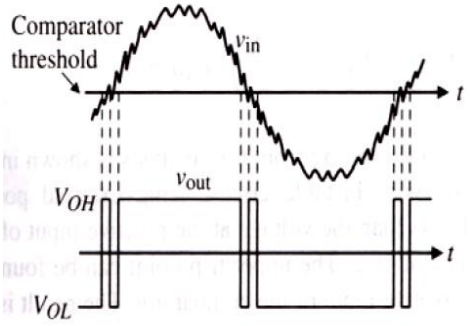
Often a comparator is placed in a very noisy environment in which it must detect signal transitions at the threshold point. If the comparator is fast enough (depending on the frequency of the most prevalent noise) and the amplitude of the noise is great enough, the output will also be noisy. In this situation, a modification on the transfer characteristic of the comparator is desired. Specifically, hysteresis is needed in the comparator. Hysteresis is the quality of the comparator in which the input threshold changes as a function of the input (or output) level. In particular, when the input passes the threshold, the output changes and the input threshold is subsequently reduced so that the input must return beyond the previous threshold before the comparator's output changes state again. This can be illustrated much more clearly with the diagram shown in Fig.(a). Note that as the input starts negative and goes positive, the output does not change until it reaches the positive trip point, V_{TRP+} . Once the output goes high, the effective trip point is changed. When the input returns in the negative direction, the output does not. Change until it reaches the negative trip point, V_{TRP-}. The advantage of hysteresis in a noisy environment can clearly be seen from the illustration given in Fig. In this figure, a noisy signal is shown as the input to a comparator without hysteresis. The intent is to have the comparator output follow the low-frequency signal. Because of noise variations near the threshold points, the comparator output is too noisy. The response of the comparator can be improved by adding hysteresis equal to or greater than the amount of the largest expected noise amplitude. The response of such a comparator is shown in Fig. (a)



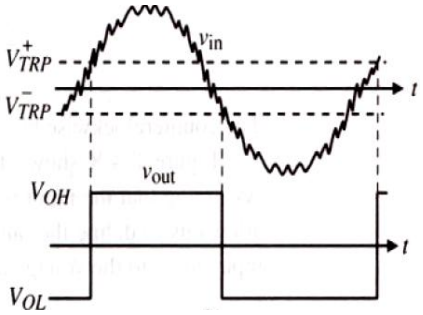
(a) Comparator transfer curve with hysteresis

The voltage-transfer function shown in Fig. is called a *bistable* characteristic. A bistable circuit can be clockwise or counterclockwise. Sometimes, the counterclockwise bistable circuit is called

noninverting and the clockwise bistable is called inverting. The bistable characteristic is defined by its width and height and whether it is clockwise or counterclockwise. The width is given by the difference between V_{TRP+} and V_{TRP-}. The height is generally the difference between V_{OH} and V_{OL} In addition, the bistable characteristic can be shifted horizontally to the left or right by addition of a dc offset voltage.



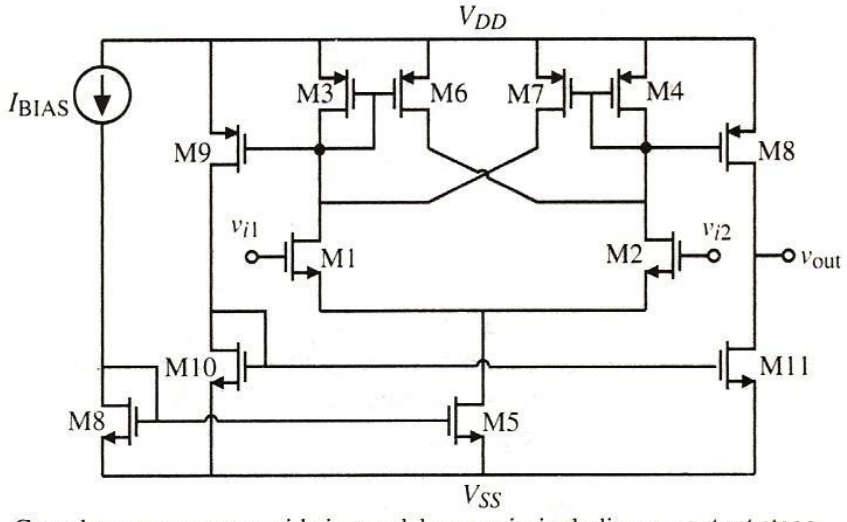
Comparator responses to a noisy input



Comparator response to a noisy Input when hysteresis is added

5.8 Circuit Diagram of comparator with internal hysteresis

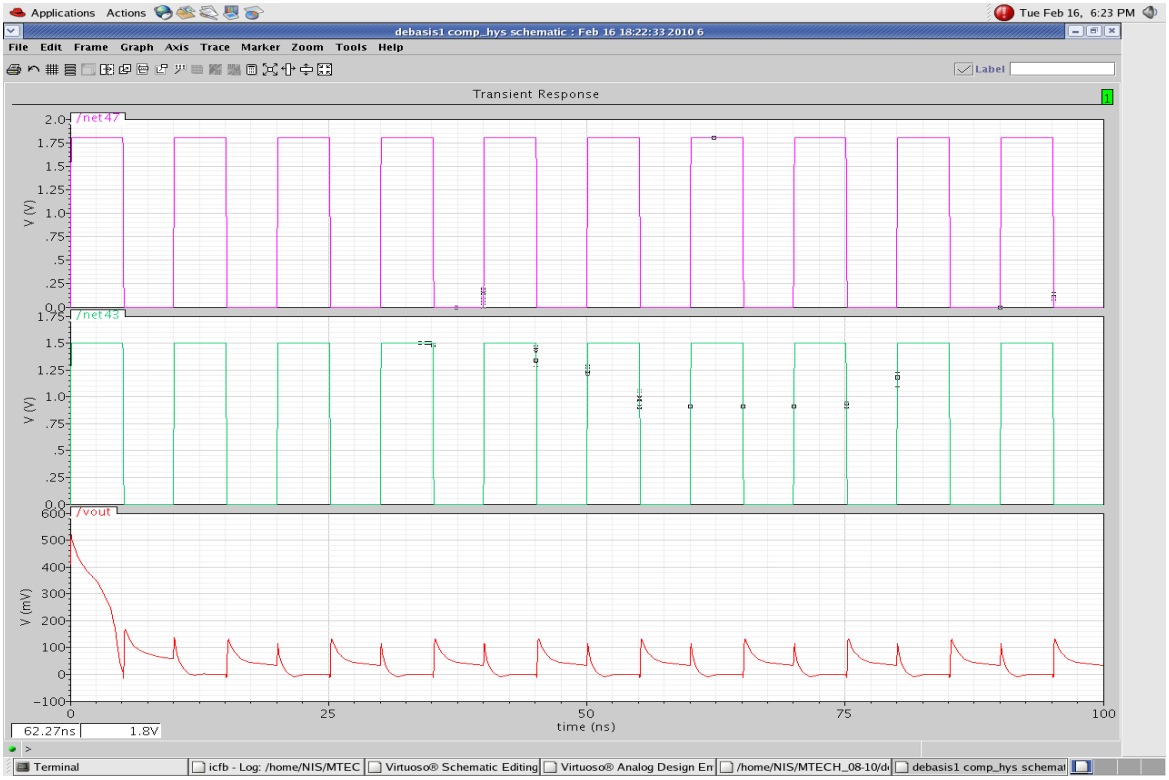
CMOS comparator using hysteresis with positive feedback which is simulated is shown in below figure with its out put.

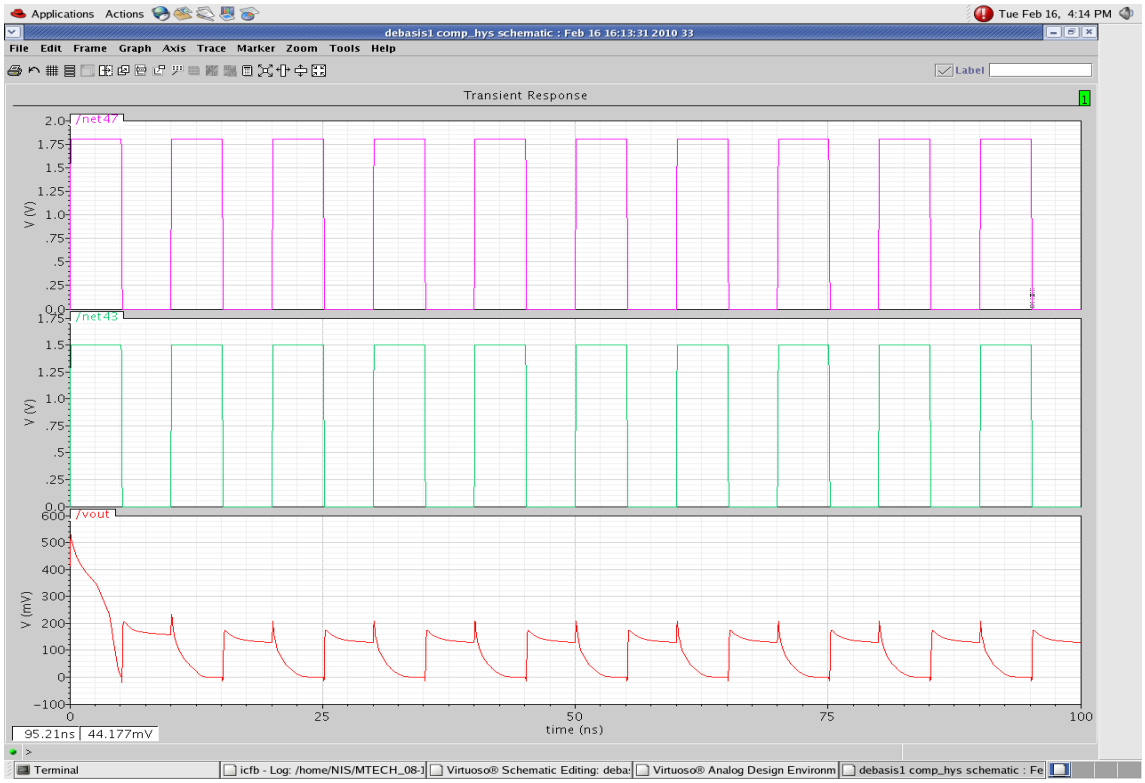


Complete comparator with internal hysteresis including an output stage.

5.9 Simulation out put

OUT PUT OF THE COMPARATOR





5.10 Comparison Results after post layout simulation :-

No	Comparator Name	Delay	Speed	Power Dissipation	Area
1	Conventional three stage comparator	0.168ns	5.59GHz	0.1034mW	197.08um^2
2	Differential Comparator	0.54ns	1.09GHz	0.338mW	213.35um^2
3	Latch based Comparator	0.09532ns	8.79GHz	1.79mW	168.36um^2
4	Comparator with Hysteresis	0.435ns	9.28GHz	2.09mW	197.134um^2

5.11 Conclusion:

Conventional three stage Comparators are simulated in GPDK 90 nm at 1.8 Supply Voltage. The simulation results shows that the offset voltages are reduced. The offset voltages of conventional comparator is less than others. The power dissipation of conventional three stage comparator, differential comparator, latch based comparator and comparator with hysteresis are 0.1034mw,0.338mw,1.79mw and 2.09mw respectively. Noise immunity of comparator with hysteresis is better than other comparators. It reduces approximately 80-85% in this design.

5.12 Scope for future work:

From simulation results shows that comparator with hysteresis gives less offset voltage, low noise ,low power dissipation compared to conventional comparators. In the future by using Auto zeroing techniques one can reduce the offset voltage, power consumption, noise response. By decreasing the number of transistors one can reduce the Area, Power dissipation. And also by reducing the size of each transistor one can get less power dissipation, high speed, matching accuracy.

References

REFERENCES

1. P Philip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design (oxford University Press,Inc,USA,2002),2nd edition,pp,259-397.

2. Noor Aizad, Design and impplementation of comparator for sigma-delata modulator.

3. B.Razavi and B.A.Wooley, "Design Techniques for High-Speed High-Resolution Comparators," IEEE J. Solid-State Circuits, vol. SC-27, pp.1916-1926, Dec 1992.

4. Vipul Katyal, Randall L. Geiger and Degang J. Chen, "Adjustable Hysteresis CMOS Schmitt Triggers," Paper submitted for International Symposium on Circuits and systems, Seattle, USA, 2008.

5. Yu Lin, Vipul Katyal and Randall L. Geiger, "KT/C Constrained Optimization of Power in Pipeline ADCs," International Symposium on Circuits and Systems, Kobe, Japan, 2005

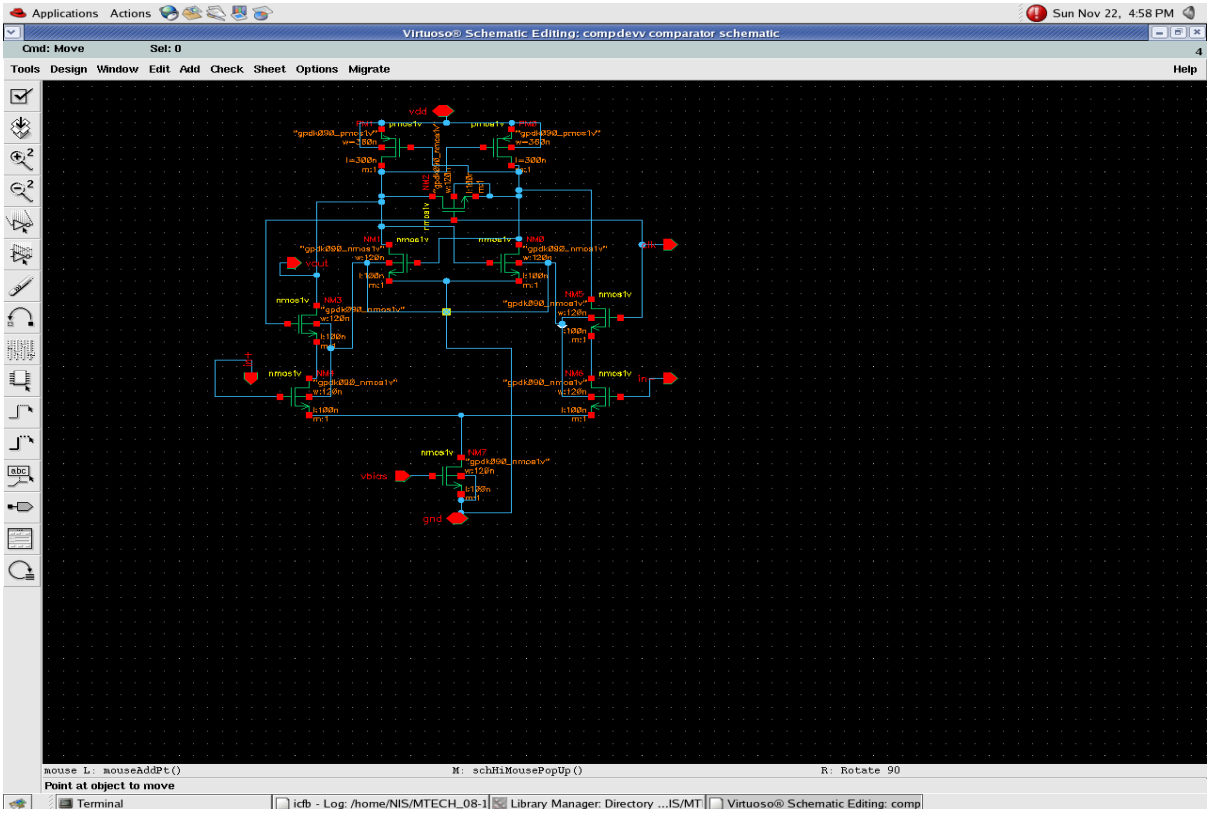
6. T. W. Matthews, P. L. Heedley, "A Simulation Method for Accurately Determining DC and Dynamic Offset in Comparators," IEEE MWSCAS, pp. 1815-1818, Aug. 2005.

7. B. M. Min, P. Kim, F. W. Bowman, D. M. Boisvert, A. J. Aude, "A 69- mW 10-bit 80-MSample/s Pipelined CMOS ADC," IEEE JSSC, vol. 38, pp. 2031-2039, Dec. 2003.

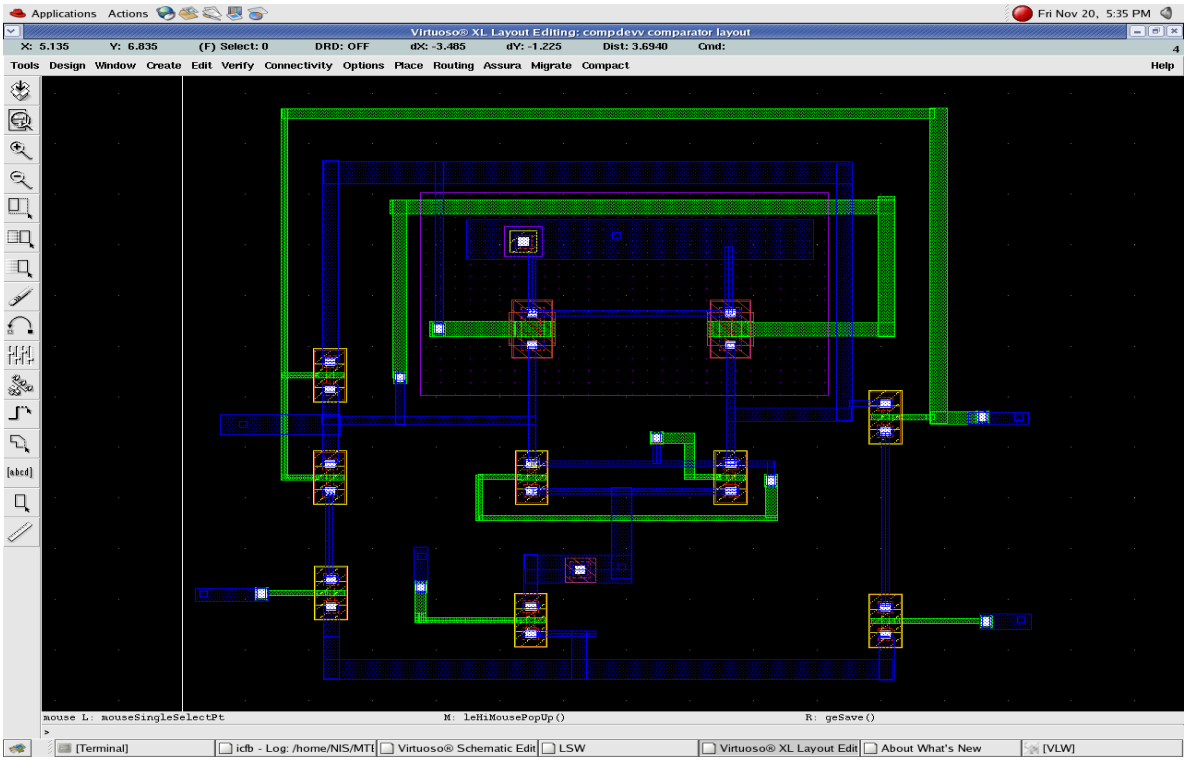
8. H.P. Le, A. Zayegh, and J. Singh, "Performance analysis of optimised CMOS comparator," *Electronics Letters*, vol. 39, pp. 833-835, May 2003.
9. S. Sheikhaei, S. Mirabbasi, and A. Ivanov, "A 0.35μm CMOS Comparator Circuit for High-Speed ADC Applications," *IEEE International Symposium on Circuits and Systems*, pp. 6134-6137, May 2005.

Appendix

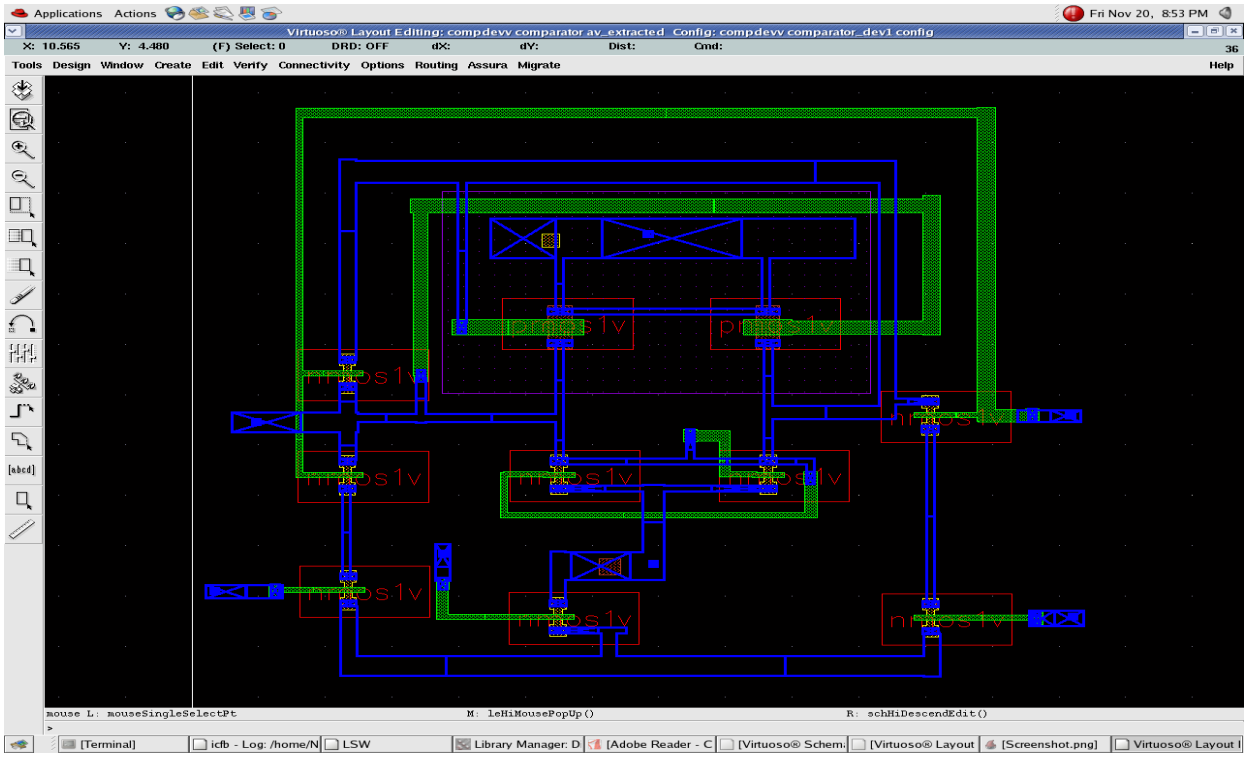
A.1. Schematic of Latch based comparator :



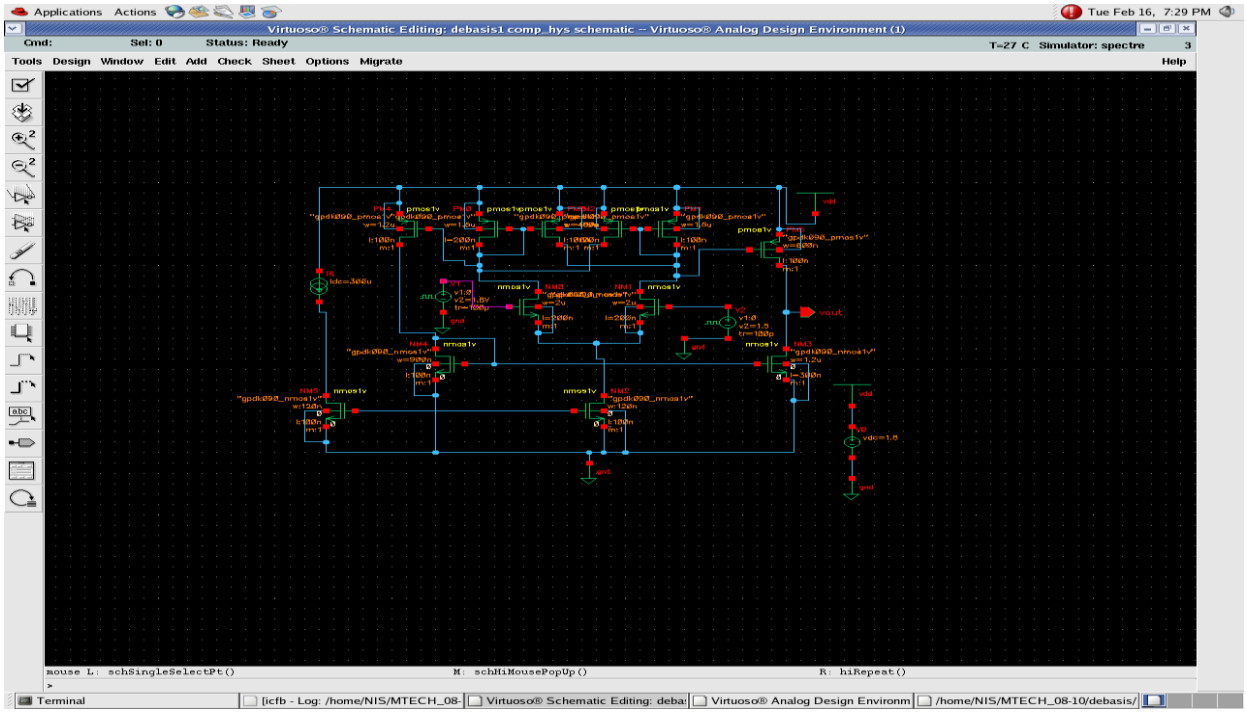
A.2. Extracted Layout:



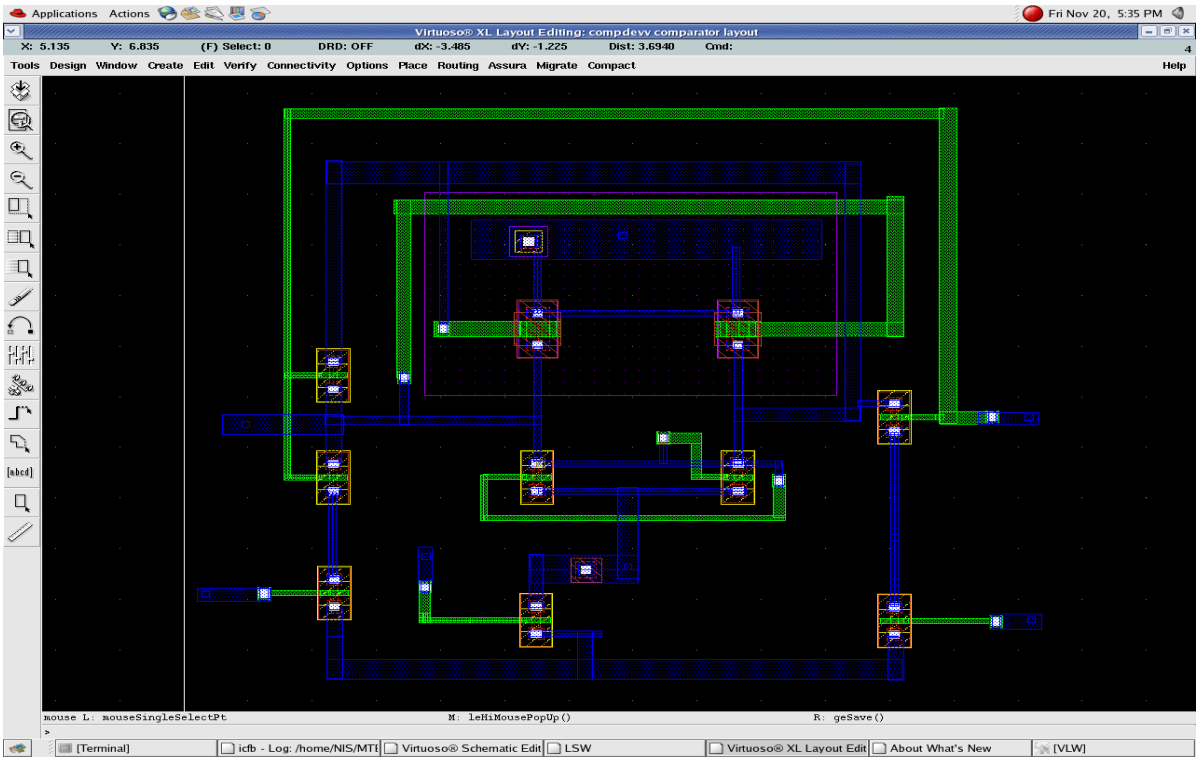
A.3. Post Layout simulation:



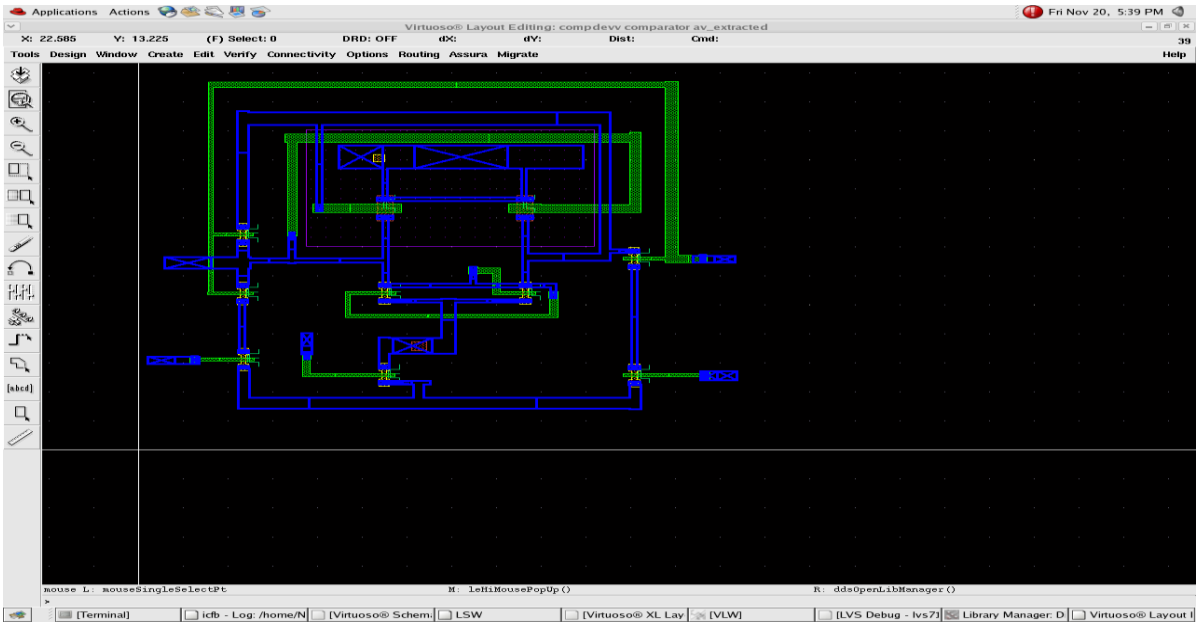
A.4. Comparator with Hysteresis:



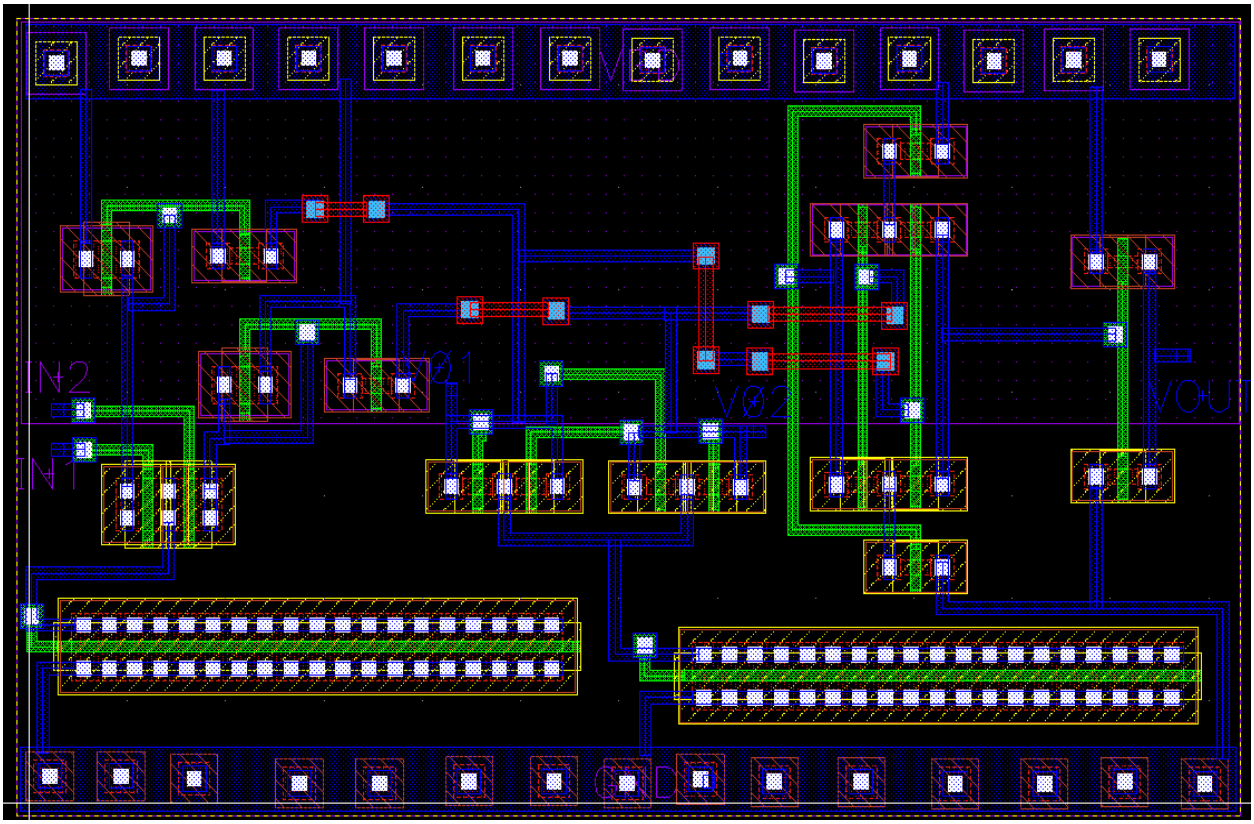
A.5. Extracted Layout of Hysteresis based comparator :



A.6. Post Layout simulation of hysteresis based comparator

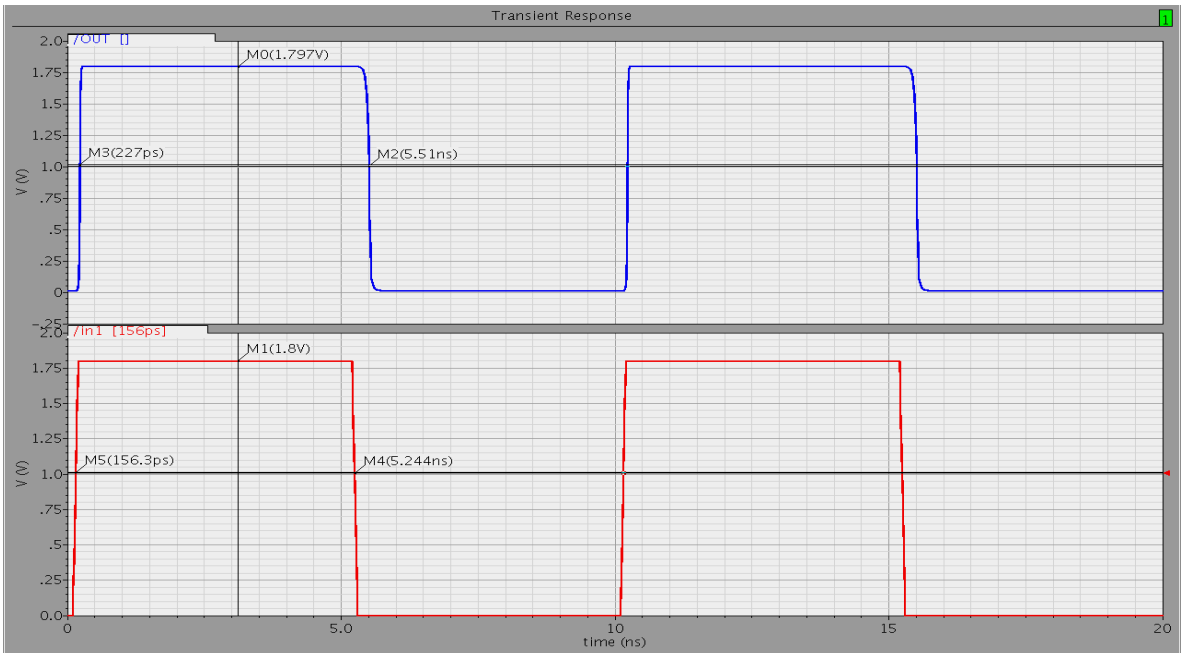


A.7. Extracted Layout conventional three stage comparator



Layout vs Schematic for Pre-amplifier based comparator

A.8. Transient wave form after post layout simulation:-



Layout vs Schematic for Differential Dynamic Comparator