A NOVEL HIGH SPEED DYNAMIC COMPARATOR WITH LOW POWER DISSIPATION AND LOW OFFSET

A THESIS SUBMITTED IN PARTIAL FULFILLMENT

OF THE REQUIREMENTS FOR THE DEGREE OF

Master of Technology

In

VLSI Design & Embedded System

By

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Roll No: 207EC211

Department of Electronics & Communication Engineering

National Institute of Technology

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Under the guidance of

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CERTIFICATE

This is to certify that the thesis entitled, "**A NOVEL HIGH SPEED DYNAMIC COMPARATOR WITH LOW POWER DISSIPATION AND LOW OFFSET"** submitted by **SILPAKESAV (207EC211)** in partial fulfillment of the requirements for the award of Master of Technology degree in Electronics and Communication Engineering with specialization in "VLSI design & Embedded systems" during session 2008-2009 at National Institute Of Technology, Rourkela (Deemed University) and is an authentic work by him under my supervision and guidance .

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other university/institute for the award of any Degree or Diploma.

Date:

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Silpakesav Velagaleti

Contents

ABSTRACT

A new fully differential CMOS dynamic comparator using positive feedback suitable for pipeline A/D converters with low power dissipation, low offset, low noise and high speed is proposed. Inputs are reconfigured from typical differential pair comparator such that near equal current distribution in the input transistors can be achieved for a meta stable point of the comparator. Restricted signal swing clock for the tail current is also used to ensure constant currents in the differential pairs. Nearly 18mV offset voltage is easily achieved with the proposed structure making it favorable for flash and pipeline data conversion applications.

The proposed topology is based on two cross coupled differential pairs positive feedback and switchable current sources, has a small power dissipation, less hysteresis band, less area, and it is shown to be very robust against transistor mismatch, noise immunity. Test structures of the comparators, designed in GPDK 90 nm are measured to determine offset power dissipation and speed with 1.8 V are compared and the superior features of the proposed comparator are established.

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Chapter 1

Introduction

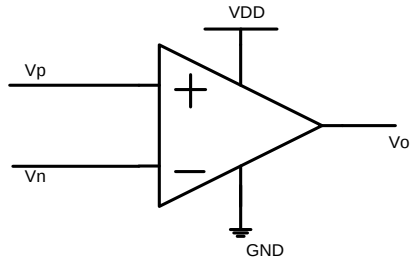
1.1. BASIC CMOS COMPARATOR:-

The schematic symbol and basic operation of a voltage comparator are shown in fig1.1, this comparator can be thought of as a decision making circuit.

Definition:-

The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison.

If the +, V_P, the input of the comparator is at a greater potential than the -, V_N, input, the output of the comparator is a logic 1, where as if the + input is at a potential less than the – input, the output of the comparator is at logic 0.



$V_P < V_N$ then V_O = VSS= logic 0.

$V_P > V_N$ then V_O = VDD= logic 1.

Figure 1 .1 Comparator operation

Fig. 1.1: Comparator operation

What is meant here by an analog signal is one that can have any of a continuum of amplitude values at a given point in time .In the strictest sense a binary signal can have only one of two given values at any point in time, but this concept of a binary signal is too ideal for real-world situations, where there is a transition region between the two binary states. It is important for the comparator to pass quickly through the transition region. The comparator is widely used in the process of converting analog signals to digital signals. In the analog-to-digital conversion process, it is necessary to first sample the input. This sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal. In its

simplest form, the comparator can be considered as a 1-bit analog-digital converter. The presentation on comparators will first examine the requirements and characterization of comparators. It will be seen that comparators can be divided into open-loop and regenerative comparators. The open-loop comparators are basically op amps without compensation. Regenerative comparators use positive feedback, similar to sense amplifiers or flip-flops, to accomplish the comparison of the magnitude between two signals. A third type of comparator emerges that is a combination of the open-loop and regenerative comparators. This combination results in comparators that are extremely fast.

1.2 Motivation:

In today's world, where demand for portable battery operated devices is increasing ,a major thrust is given towards low power methodologies for high speed applications. This reduction in power can be achieved by moving towards smaller feature size processes. However, as we move towards smaller feature size processes, the process variations and other non-idealities will greatly affect the overall performance of the device. One such application where low power dissipation, low noise ,high speed ,less hysteresis ,less Offset voltage are required is Analog to Digital converters for mobile and portable devices. The performance limiting blocks in such ADCs are typically inter-stage gain amplifiers and comparators. The accuracy of such comparators, which is defined by its offset, along with power consumption ,speed is of keen interest in achieving overall higher performance of ADCs.In the past, pre-amplifier based comparators have been used for ADC architectures such as flash and pipeline. The main drawback of pre-amplifier based comparators is the more offset voltage. To overcome this problem, dynamic comparators are often used that make a comparison once every clock period and require much less offset voltage.However,these dynamic comparators suffer from large power dissipation compared to pre-amplifier based comparators.

In the literature, a few dynamic comparators can be found, e.g. Differential pair, Dynamic comparator ,Dynamic comparator using positive feedback, Dynamic comparator using positive feedback PMOS as a switch.However,very little emphasis is placed on actual details of operation of these structures along with experimental results to compare offset values ,power consumption, speed of different structures. These experimental offset values vary from 18mv to

50 mV.However,the literature is devoid of any information on how other non-idealities such as imbalance in parasitic capacitors, common mode voltage errors or clock timing errors effect these structures. The operation and the effects of non-idealities, Hysteresis of such dynamic comparators have been investigated. A new dynamic comparator structure which achieves a low offset, low power consumption, less Hysteresis, high speed has been developed. In the new comparator structure, inputs are reconfigured from the typical differential pair comparator [4] so that each differential pair branch contributes equal current at the detestable operating point along with keeping the differential pair's tail current in saturation region. Comparison of the new architecture with respect to typical differential pair structure [4] is made as both structures share the same base structure.

1.3 Thesis organization:

This thesis provides A Novel Dynamic comparator using positive feedback .Simulation results gives High Speed, low power dissipation. less offset, low noise, less Hysteresis which is useful in Analog to Digital Converters. Thesis can be organized in the following manner. Chapter 2 focuses on characterisation of comparator, Offset voltages, Comparator using Hysteresis.Chapter3 focuses on Conventional comparators of DC responses, measuring offset voltages, Delay, Speed, Power dissipation. Chapter 4 focuses on Dynamic Comparators of DC responses, measuring offset voltages, Delay, Speed, Power dissipation, Hysteresis band .The experimental values of all the results are shown in table. All the layouts of Comparators are shown in the Appendix.

Chapter 2

Fundamentals of Comparator Design

2.1. CHAERACTERISATION OF COMPARATOR:-

A positive voltage applied at the *Vp* input will cause the comparator output to go positive, whereas a positive voltage applied at the V_N input will cause the comparator output to go negative. The upper and lower voltage limits of the comparator Output are defined as V_{OH} and V_{OL} respectively.

Static Characteristics:-

A comparator was defined above as a circuit that has a binary output whose value is based on a comparison of two analog inputs. This is illustrated in Fig.2.1 As shown in this figure. The output of the comparator is high (V_{OH}) when the' difference between the noninverting and inverting inputs is positive, and low (V_{OL}) when this difference is negative. Even though this type of behavior is impossible in a real-world situation, it can be modeled with ideal circuit elements with mathematical descriptions. One such circuit model is shown in Fig.2.2 comprises a voltage-controlled voltage source (VCVS) whose characteristics are described the mathematical formulation given on the figure.

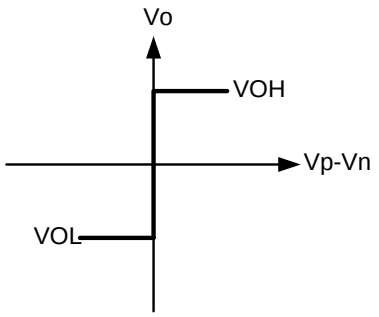


Fig.2.1. Ideal transfer curve of a Comparator

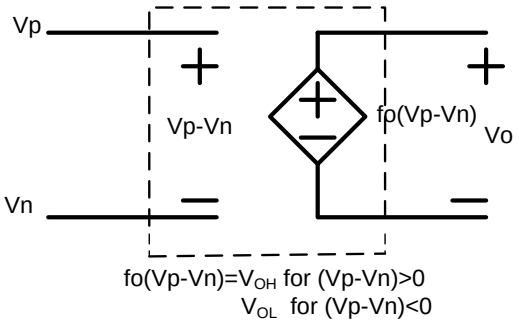


Fig. 2.2 Model for an ideal Comparator

The second no ideal effect seen in comparator circuits is input-offset voltage, *Vos.* In Fig.2.1 the output changes as the input difference crosses zero. If the output did not change until the input difference reached a value *+Vos,* then this difference would be defined as the offset voltage. This would not be a problem if the offset could be predicted, but it varies randomly from circuit to circuit [I] for a given design. Figure 2.4 illustrates offset in the transfer curve for a comparator,

with the circuit model including an offset generator shown in Fig.2.5. The ± sign of the offset voltage accounts for the fact that *Vos* is unknown in polarity.

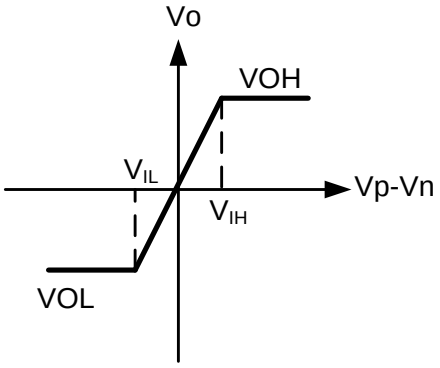


Fig. 2.3. Transfer curve of a comparator comparator with finite gain

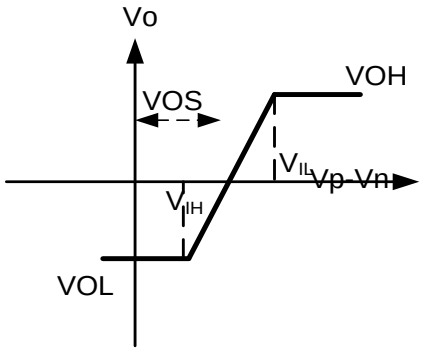
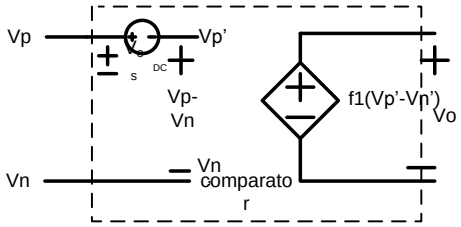


Fig. 2.4 Transfer curve of a including input – offset voltage

In addition to the above characteristics, the comparator can have a differential input resistance and capacitance and an output resistance. In addition, there will also be an input common-mode resistance, R_{icm}. All these aspects can be modeled in the same manner as was done for the opamp. Because the input to the comparator is usually differential, the input common-mode range is also important. The ICMR for a comparator would be that range of input common-mode voltage over which the comparator functions normally. This input common-mode range is generally the range where all transistors of the comparator remain in saturation. Even though the comparator is not designed to operate in the transition region between the two binary output states, noise is still important to the comparator. The noise of a comparator is modeled as if the comparator were biased in the transition region of the voltage-transfer characteristics. The noise will lead to an uncertainty in the transition region as shown in Fig.2.6. The uncertainty in the transition region will lead to jitter or phase noise in the circuits where the comparator is employed.

Dynamic Characteristics:-

The dynamic characteristics of the comparator include both small-signal and large-signal behavior. We do not know, at this point, how long it takes for the comparator to respond to the given differential input. The characteristic delay between input excitation and output transition is the time response of the comparator. Figure 2.7 illustrates the response of a comparator to an input as a function of time. Note that there is a delay between the input excitation and the output response. This· time difference is called the *propagation delay time* of the comparator. It is a very important parameter since it is often the speed limitation in the conversion rate of an



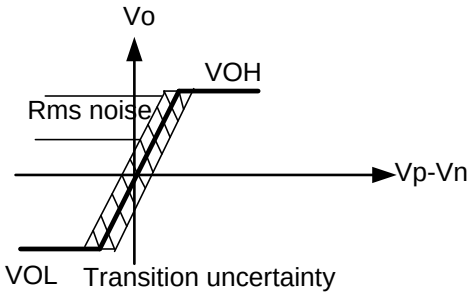


Fig. 2.5 Model for a comparator including input-offset voltage.

Fig. 2.6 Influence of noise on a Comparator.

*A/C*onverter. The propagation delay time in comparators generally varies as a function of the amplitude of the input. A larger input will result in a smaller delay time. There is an upper limit at which a further increase in the input voltage will no longer affect the delay .This mode of operation is called *slewing* or *slew rate.*

The small-signal dynamics are characterized by the frequency response of the comparator. A simple model of this behavior assumes that the differential voltage gain, $A_{v,}$ is given as

$$A_v(s) = \frac{A_v(0)}{\frac{s}{\omega_c} + 1} = \frac{A_v(0)}{s\tau_c + 1} \qquad (2.1)$$

where $\mathbf{A}_v(0)$ is the dc gain of the comparator and $\omega_C = 1/\tau_C$ is the - 3 dB frequency of the single (dominant) pole approximation to the comparator frequency response. Normally, the $\mathbf{A}_v(0)$ and

ω_c of the comparator are smaller and larger, respectively, than for an opamp.

Let us assume that the minimum change of voltage at the input of the comparator the resolution of the comparator. We will define this minimum input voltage to the comparator as

$$V_{in}(\min) = \frac{V_{OH} - V_{OL}}{A_V(0)} \qquad (2.2)$$

For a step input voltage, the output of the comparator modeled by Eq. (2.1)rises (or falls) with a first-order exponential time response from V_{OL} to V_{OH} (or V_{OH} to V_{OL}) . If *Vin* is larger than *Vin(min),* the output rise or fall time is faster. When *Vin(min)* is applied to the comparator, we can write the following equation:

$$\frac{V_{OH} - V_{OL}}{2} = A_V(0)[1 - e^{-T_P / \tau_C}]V_{in}(\min) = A_v(0)[1 - e^{-T_P / \tau_C}](\frac{V_{OH} - V_{OL}}{A_V(0)}) \qquad (2.3)$$

Therefore ,the propagation delay time for an input step of Vin(min) can be expressed as

$$t_p(\max) = \tau_c \ln(2) = 0.693\tau_c \qquad (2.4)$$

This propagation delay time will be valid for either positive-going or negative-going comparator outputs. The propagation delay time is given as

$$t_p = \tau_c \ln(\frac{2k}{2k-1}) \qquad (2.5)$$

$$\text{where} \quad k = \frac{V_{in}}{V_{in}(\min)} \mathrm{V_{in.}} \qquad (2.6)$$

Obviously, the more overdrive applied to the input of this comparator, the smaller the propagation delay time. As the overdrive increases to the comparator eventually the comparator enters a large signal mode of operation. Under large-signal operation, a slew-rate limit will occur due to limited current to charge or discharge capacitors.

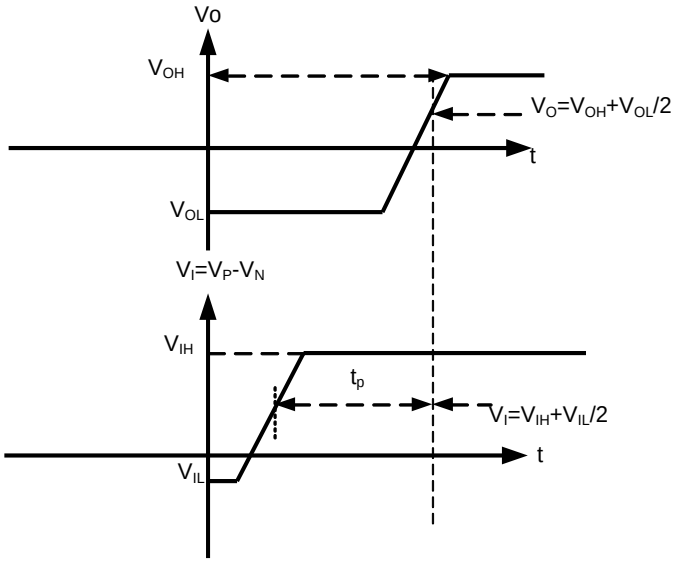


Fig.2.7. Propagation delay time of a noninverting comparator.

If the propagation delay time is determined by the slew-rate of the comparator, then this time can be written as

$$t_p = \Delta T = \frac{\Delta V}{SR} = \frac{V_{OH} - V_{OL}}{2.SR} \qquad (2.7)$$

In the case where the propagation time is determined by the slew rate, the most important factor to decrease the propagation time is increasing the sinking or sourcing capability)of the comparator. A block diagram of a high performance comparator is shown in fig.2.8

2.2. Block diagram of Comparator:-

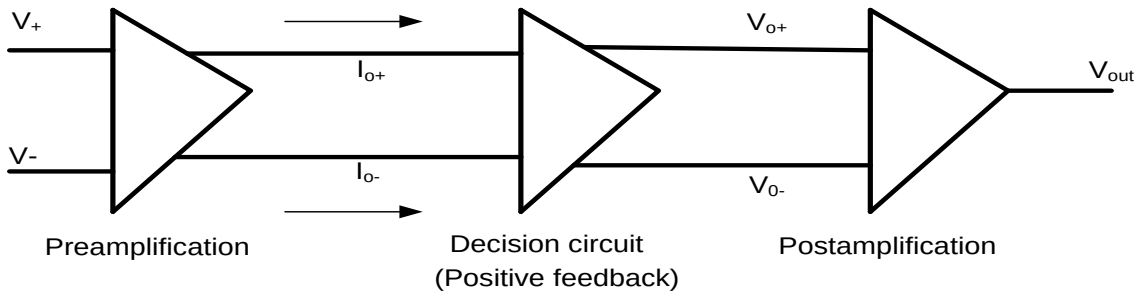


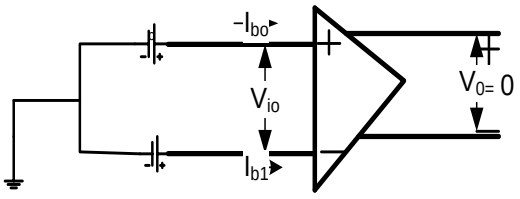
Fig. 2.8 Block diagram of Comparator

The comparator consists of three stages .The input pre-amplifier, a positive feedback or decision stage and an output buffer. The pre-amp stage amplifies the input signal to improve the comparator sensitivity (i.e. increases the minimum input signal with which the comparator can make a decision) and isolates the input of the comparator from switching noise coming from the positive feedback stage. The positive feedback stage is used to determine which of the input signal is larger. The output buffer amplifies this information and outputs a digital signal. Designing a comparator can begin with considering input common mode range, power dissipation, propagation delay and comparator gain. We will develop a basic comparator design using a procedure similar to the basic op-amp.

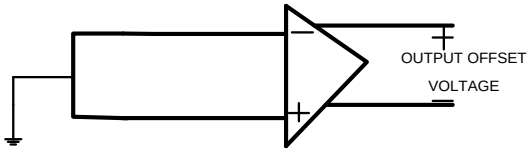
2.3. OFFSET ERROR VOLTAGES AND CURRENTS:-

he ideal operational amplifier shown in Fig. 2.9(a) is perfectly balanced, that is, *Vo* = 0 when Vl = *V2*• A real operational amplifier exhibits an unbalance caused by a mismatch[15] of the input transistors. This mismatch results in unequal bias currents flowing through the input terminals, and also requires that an input offset voltage be applied between the two input terminals to balance the amplifier output. In this section the. dc error voltages and currents that can be measured at the input and output terminals.

Input Bias Current :-The input bias current is one-half the sum of the separate currents entering the two input terminals of a balanced amplifier as shown in Fig.2.9(a) the input bias current is *I B = (I* Bl + *I B2)* /2 when *Vo* = O.



2.9 *(a)* Input offset voltage



2.9 *(b)* Output offset voltage.

Input Offset Current,:- The input offset current h is the difference between the separate currents entering the input terminals of a balanced amplifier. As shown in Fig, *2.9(a)*, we have *Iio = I Bl - I B2* when *Va* = O.

Input Offset Current Drift :-The input offset current drift $\Delta I_{io}/\Delta T$ is the ratio of the change of input offset current to the change of temperature.

Input Offset Voltage :-The input offset voltage *Via* is that voltage which must be applied between the input terminals to balance the amplifier, as shown in Fig. *2.9(a).*

Input Offset Voltage Drift:- The input offset voltage drift $\Delta V_i/\Delta T$ is the ratio of the change of input offset voltage to the change in temperature.

Output Offset Voltage The output offset voltage is the difference between the dc voltages present at the two output terminals (or at the output terminal and ground for an amplifier with one output) when the two input terminals are grounded (Fig. *2.9.b).*

Power Supply Rejection Ratio :-The power supply rejection ratio (PSRR> is the ratio of the change in input offset voltage to the corresponding channel in one power supply voltage, with all remaining power supply voltage constant.

Slew Rate :-The slew rate is the time rate of change of the closed loop amplifier output voltage under large-signal conditions.

2.4. Offset Voltage in Dynamic Comparators:-

Comparators have a crucial influence on the overall performance in high-speed analog-to-digital converters (ADCs). The comparator's accuracy, which is often defined by its input offset voltage, is essential for high performance ADCs. Dynamic comparators are widely used in the high speed ADCs due to its low power consumption and fast speed. However, there is a lack of thorough traditional comparator is built by an operational amplifier, the calculation of offset voltage is straightforward since the operation regions of all transistors are well defined.

To overcome the difficulties in determining the operation regions and bias conditions of transistors in a dynamic comparator when the mismatch exists, we propose a balanced method to calculate the input offset voltage. In this method, a voltage equal to the input offset voltage is virtually applied to one of the inputs of the comparator to cancel the mismatch effects and make

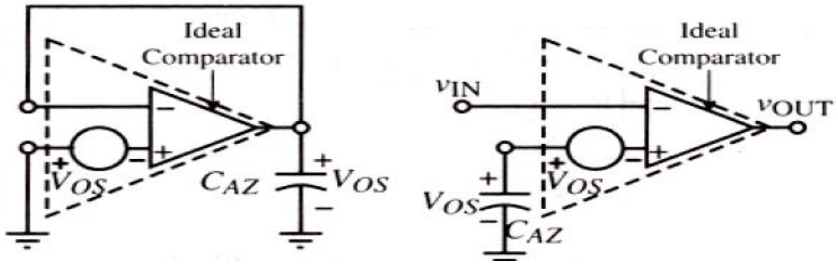
the comparator with mismatch to reach a balanced status. Under this balanced condition, the currents in the two branches are symmetric at any time. So the bias voltage and current for any transistor in the comparator are ready to be solved at any time point.

2.4.1. Improving the Performance of open loop comparators:-

There are two areas in which the performance of an open-loop, high-gain comparator can be improved with little extra effort. These areas are the input-offset voltage and a single transitiontion of the comparator in a noisy environment[6]. The first problem can be solved by *auto zeroing* and the second can be solved by the introduction of hysteresis using a bistable circuit. These two techniques will be examined in the following.

Auto zeroing Techniques:-

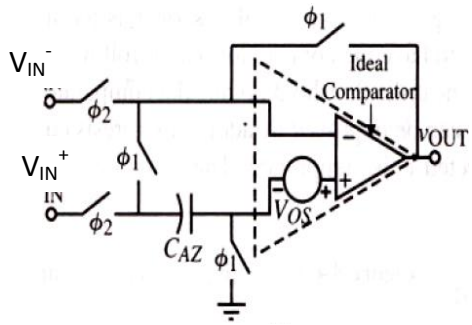
Input-offset voltage can be a particularly difficult problem in comparator design. In precision applications, such as high-resolution A/D converters, large input-offset voltages cannot be tolerated. While systematic offset can nearly be eliminated with proper design (though still affected by process variations), random offsets still remain and are unpredictable. Fortunately there are techniques in MOS technology to remove a large portion of the input offset using offset-cancellation techniques. These techniques are available in MOS because of the nearly infinite input resistance of MOS transistors. This characteristic allows long-term storage of voltages on the transistor's gate. As a result, offset voltages can be measured, stored on capacitors, and summed with the input so as to cancel the offset.[6]



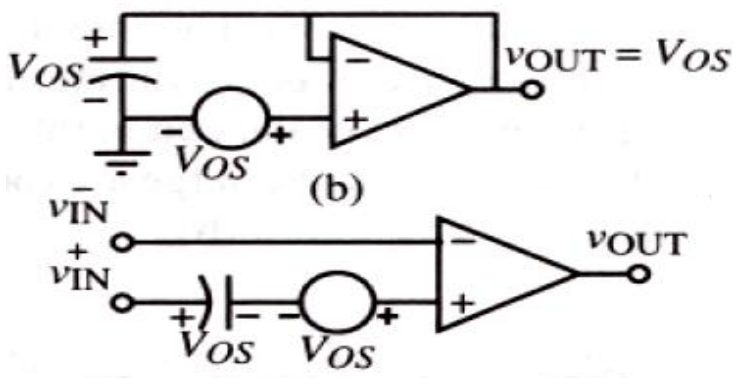
2.10 a) Comparator unity-gain configuration storing the offset on auto zero capacitor C_{AZ} during first half of the auto zero cycle. 2.10 b) Comparator in open-loop configuration offset cancellation achieved at the non inverting input during the second half of the auto zero cycle.

A model of a comparator with an input-offset voltage is shown in Fig (2.10a). A known polarity is given to the set voltage for convenience. Neither the value nor the polarity can be predicted in reality. Figure (2.10a) shows the comparator connected in the unity-gain configuration so that the input offset is available at the output. In order for this circuit to work properly, it is necessary that the comparator be stable in the unity-gain configuration. This implies that only self compensated high-gain amplifiers would be suitable for auto zeroing. One could use the two stage, open-loop comparator but a compensation circuit should be switched into the circuit during auto zeroing. In the final operation of the auto zero algorithm C_{AZ} is placed at the input of the comparator in series with *Vos.* The voltage across C_{AZ} adds to *Vos,* resulting in zero volts at the noninverting input of the comparator. Since there is no de path to discharge the auto zero capacitor, the voltage across it remains indefinitely (in the ideal case). In reality, there are leakage paths in shunt with C_{AZ} that can discharge it over a period of time. The solution to this problem is to repeat the auto zero cycle periodically.

A practical implementation of a differential-input, auto zeroed comparator is shown Fig.(2.11.a). The comparator is modeled with an offset-voltage source as before. Figure(2.11.b) shows the state of the circuit during the first phase of the cycle when ϕ_1 is high. The offset is stored across



2.11 (a) implementation of a differential-input, auto zeroed comparator



(C)

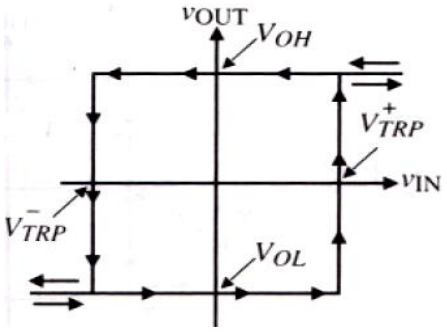
2.11 (b) Comparator during phase φ1, 2.11(c) Comparator during phase φ2

C_{AZ} Figure (2.11.C) shows the circuit in the second phase of the auto zero cycle when ϕ_2 is high. The offset is canceled by the addition of *Vos* on C_{AZ} It is during this portion of the cycle that the circuit functions as a comparator.

2.5. Comparator Using Hysteresis

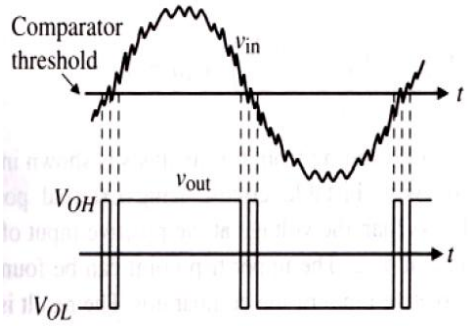
Often a comparator is placed in a very noisy environment in which it must detect signal transitions at the threshold point. If the comparator is fast enough (depending on the frequency of the most prevalent noise) and the amplitude of the noise is great enough, the output will also be noisy. In this situation, a modification on the transfer characteristic of the comparator is desired. Specifically, hysteresis is needed in the comparator. Hysteresis is the quality of the comparator in which the input threshold changes as a function of the input (or output) level. In particular, when the input passes the threshold, the output changes and the input threshold is subsequently reduced so that the input must return beyond the previous threshold before the comparator's output changes state again. This can be illustrated much more clearly with the diagram shown in Fig.2.12(a) . Note that as the input starts negative and goes positive, the output does not change until it reaches the positive trip point, V_{TRP+} . Once the output goes high, the effective trip point is changed. When the input returns in the negative direction, the output does not. change until it reaches the negative trip point, V_{TRP-}. The advantage of hysteresis in a noisy environment can clearly be seen from the illustration given in Fig. 2.12(b). In this

figure, a noisy signal is shown as the input to a comparator without hysteresis. The intent is to have the comparator output follow the low-frequency signal. Because of noise variations near the threshold points, the comparator[6] output is too noisy. The response of the comparator can be improved by adding hysteresis equal to or greater than the amount of the largest expected noise amplitude. The response of such a comparator is shown in Fig. 2.12(c).

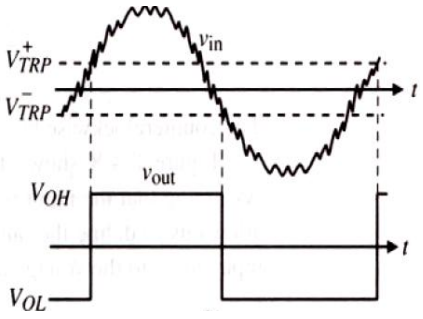


2.12 (a) Comparator transfer curve with hysteresis

The voltage-transfer function shown in Fig. 2.12(a) is called a *bistable* characteristic. A bistable circuit can be clockwise or counterclockwise. Figure 2.12(a) is an example of a counterclockwise bistable characteristic. Sometimes, the counterclockwise bistable circuit is called noninverting and the clockwise bistable is called inverting. The bistable characteristic is defined by its width and height and whether it is clockwise or counterclockwise. The width is given by the difference between V_{TRP+} and V_{TRP-}. The height is generally the difference between V_{OH} and V_{OL} In addition, the bistable characteristic can be shifted horizontally to the left or right by addition of a dc offset voltage.



2.12 (b) Comparator responses to a noisy input



2.12 (c) Comparator response to a noisy Input when hysteresis is added

Chapter 3

Conventional Comparators

3.1. Preamplifier based Comparator

3.1.1Preamplification

This circuit is a differential amplifier with active loads. The sizes of NM0 and NM1 are set by considering the diff-amp transconductance and the input resistance. The transconductance sets the gain of the stage, while the input capacitance of the comparator is determined by the size of NM0 and NM1. We will concentrate on speed in the design, and therefore we will set the channel lengths of the MOSFETs to 100nm. (Channel length modulation gives rise to an unwanted offset voltage). Using the sizes given in the schematic, we can relate the input voltages to output currents by

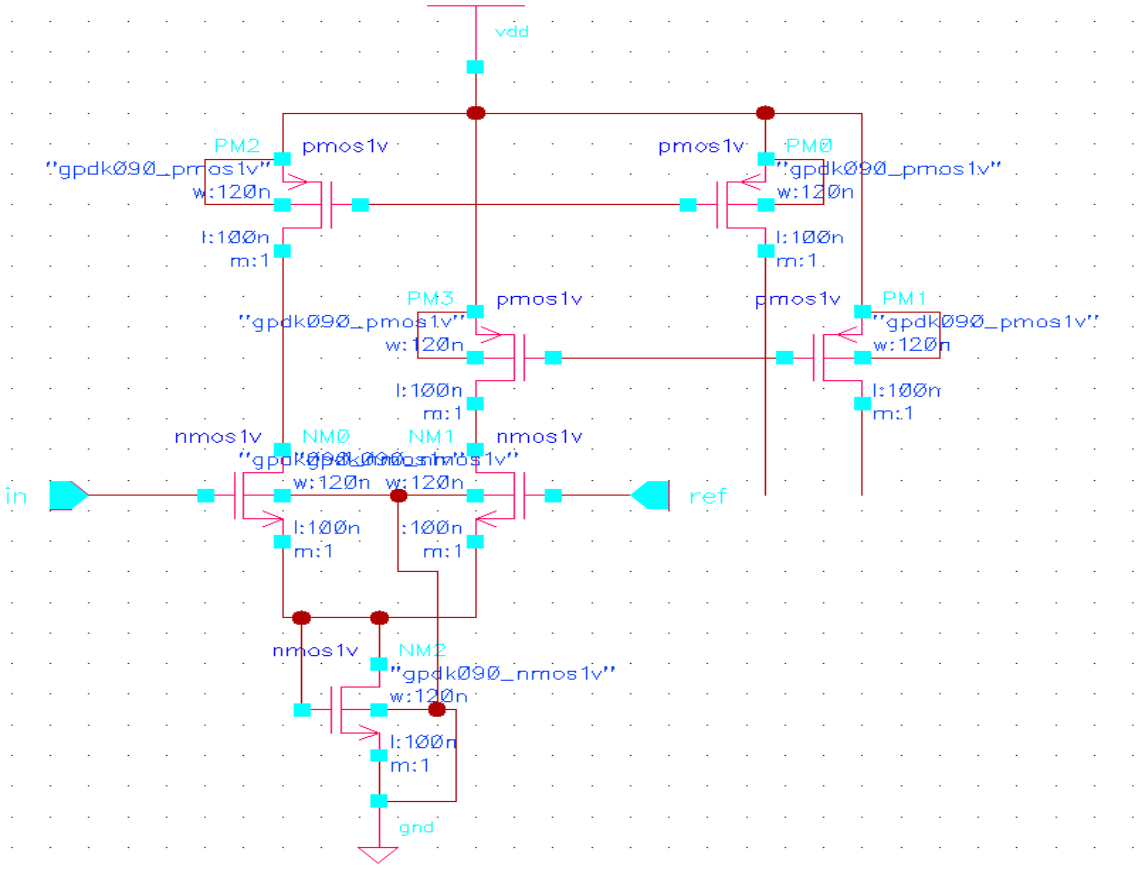


Fig.3.1 Pre-amplification stage of comparator.

$$i_{o+} = \frac{gm}{2}(\nu_+ - \nu_-) + \frac{Iss}{2} = Iss - i_{o-} \quad . \qquad (3.1)$$

$$g_m = g_{m1} = g_{m2} \qquad (3.2)$$

To further increase the gain of the first stage, we can size up the widths of MOSFETs PM3 and PM4 relative to the widths of PM0 and PM1.

3.1.2 Decision circuit:-

The decision circuit is the heart of the comparator and should be capable of discriminating mV level signals. We should also be able to design the circuit with some hysteresis for use in rejecting noise on a signal. The circuit uses positive feedback[16] from the cross-gate connection of NM1 and NM2 to increase the gain of the decision element.

Let's begin by assuming that i_{o+} is much larger than i_{o-} so that M5 and M7 are ON and NM1 and NM3 are off. We will also assume that $\beta_{NM0} = \beta_{NM3} = \beta_A$ and $\beta_{NM1} = \beta_{NM2} = \beta_B$. Under these circumstances, ν_{o-} is approximately 0V and ν_{o+} is

$$\nu_{o+} = \sqrt{\frac{2io+}{\beta A}} + V_{THN} \qquad (3.3)$$

If we start to increase i_{o-} and decrease i_{o+}, switching takes place when the drain-source voltage of NM2 is equal to V_{THN} of NM1. At this point, NM1 starts to take current away from NM0. This decreases the drain-source voltage of NM0 and thus starts to turn NM2 off. If we assume that the maximum value of ν_{o+} or ν_{o-} is equal to $2V_{THN}$,then NM1 and NM2 operate, under steady state $\beta_A=\beta_5=\beta_8$, $\beta_B =\beta_6=\beta_7$.

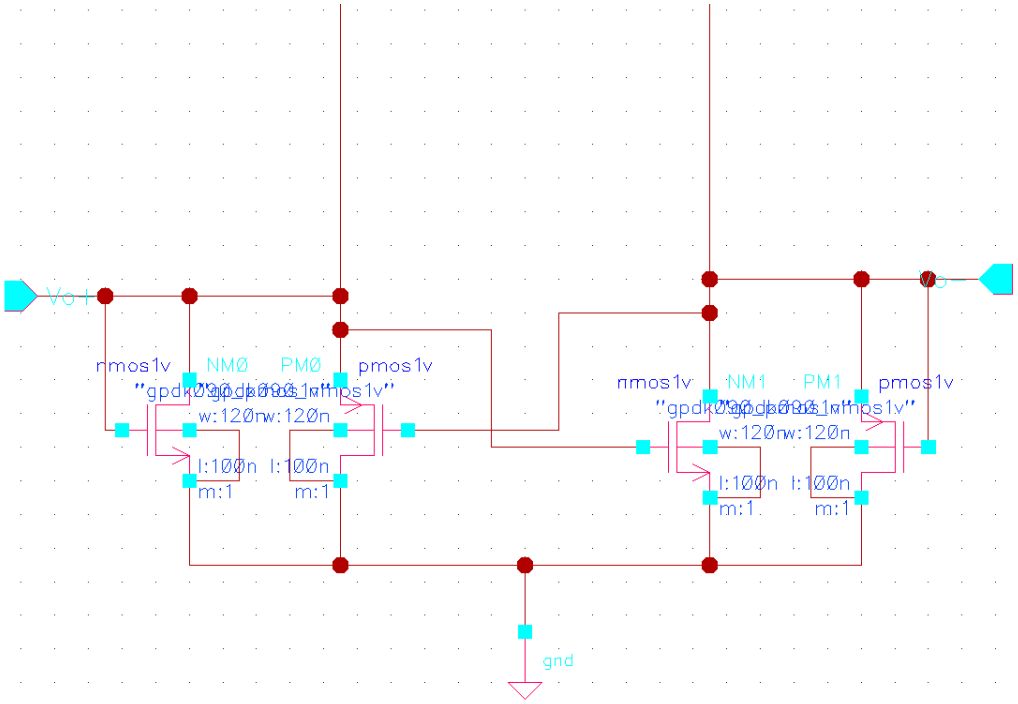


Fig. 3.2 Decision circuit

conditions, in either cutoff or the triode regions. Under these circumstances, the voltage across NM2 reaches V_{THN}, and thus NM2 enters the saturation region, when the current through NM2 is

$$i_{o-} = \frac{\beta B}{2}(v_{o+} - V_{THN})^2 = \frac{\beta B}{\beta A}.\, i_{o+} \qquad (3.4)$$

This is the point at which switching takes place. That is , NM2 shuts off and NM1 turns on. If $\beta_A = \beta_B$, then switching takes place when the currents i_{o+} and i_{o-} are equal. Unequal βs cause the comparator to exhibit hysteresis. A similar analysis for increasing i_{o+} and decreasing i_{o-} yields a switching point of

$$i_{o+} = \frac{\beta B}{\beta A}.\, i_{o-} \qquad (3.5)$$

Relating these equations to Eq.(3.1 to 3.5) yields the switching point voltages or

$$V_{SPH} = v_+ - v- = \frac{Iss}{gm}.\frac{\frac{\beta B}{\beta A}-1}{\frac{\beta B}{\beta A}+1} \qquad \text{for } \beta_B \geq \beta_A \qquad (3.6)$$

And $$V_{SPL} = - V_{SPH} \qquad (3.7)$$

3.1.3 Output Buffer:-

The final component in our comparator design is the output buffer or post-amplifier. The main purpose of the output buffer is to convert the output of the decision circuit into a logic signal (i.e., 0 or 5V). The output buffer should accept a differential input signal and not have slew-rate limitations. The circuit used as an output buffer in our basic comparator design is shown in fig.5.This circuit is a self-biasing differential amplifier. We can see a problem in connecting the decision circuit directly to the output buffer. The MOSFET NM3 is added in series with the decision circuit to increase the average voltage out of the decision circuit. The size of the MOSFET is somewhat arbitrary. We will set W_{17}/L_{17} =5 µm/100nm so that the output of the decision circuit is increased by approximately V_{THN}.

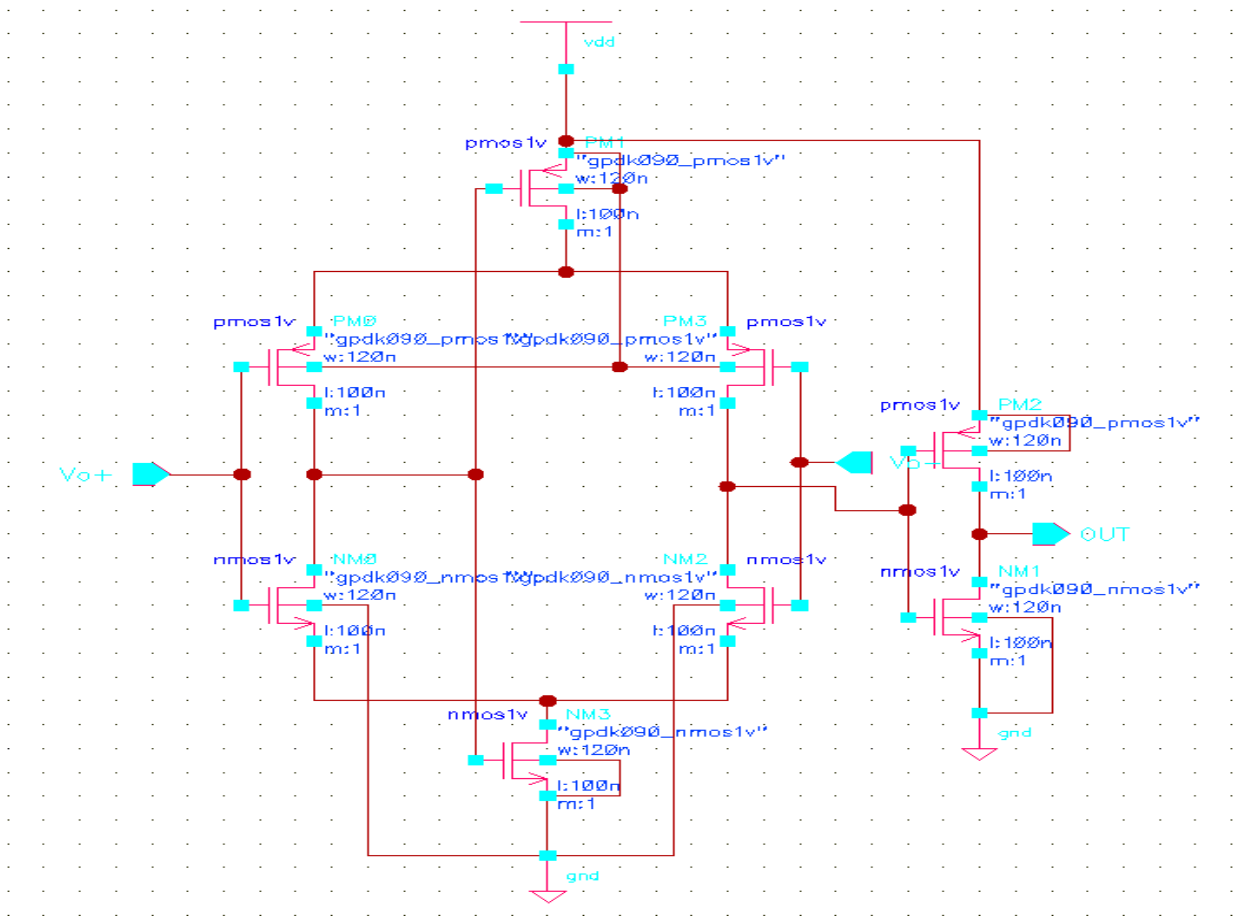


Fig 3.3 Output Buffer Circuit

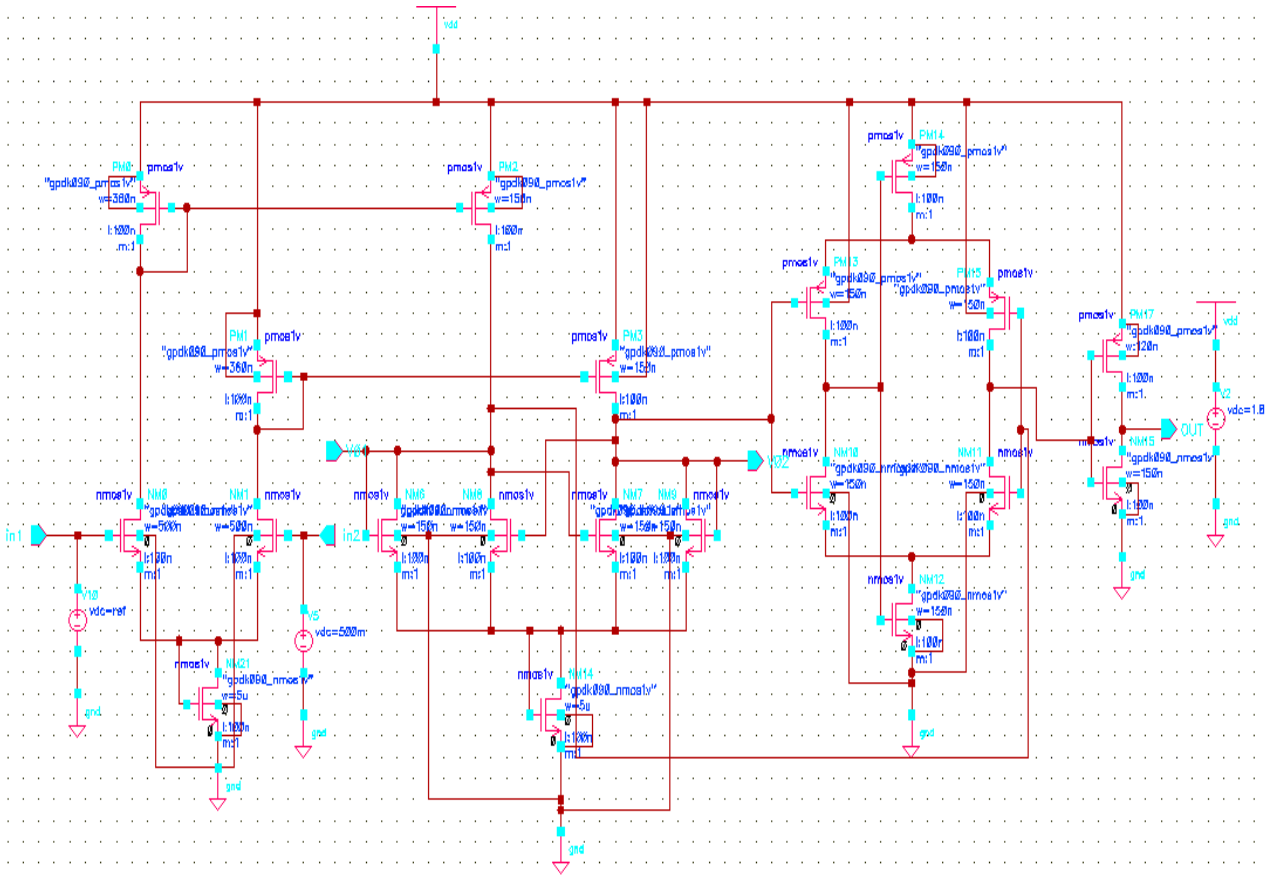


Fig .3.4 Preamplifier based Comparator

The complete schematic of the comparator is shown in fig .3.4. Unlabeled MOSFETs are 150nm/100nm. Here the input Voltage as a ref parameter. And sweep this parameter from 0 to 1.8 V. The reference Voltage as 0.5 Volt. So as above the Circuit is connected and the wave forms of the Output Voltages of Decision Circuit and Output Buffer are shown in Fig .7.

Here the reference Voltage as 0.5V.So if the input Voltage is greater than reference Voltage it is giving output Voltage as logic 1.And if the Input Voltage is less than reference Voltage it gives the Output as logic 0.And also the output waveforms are shown. These waveforms are also changing at the reference Voltage.

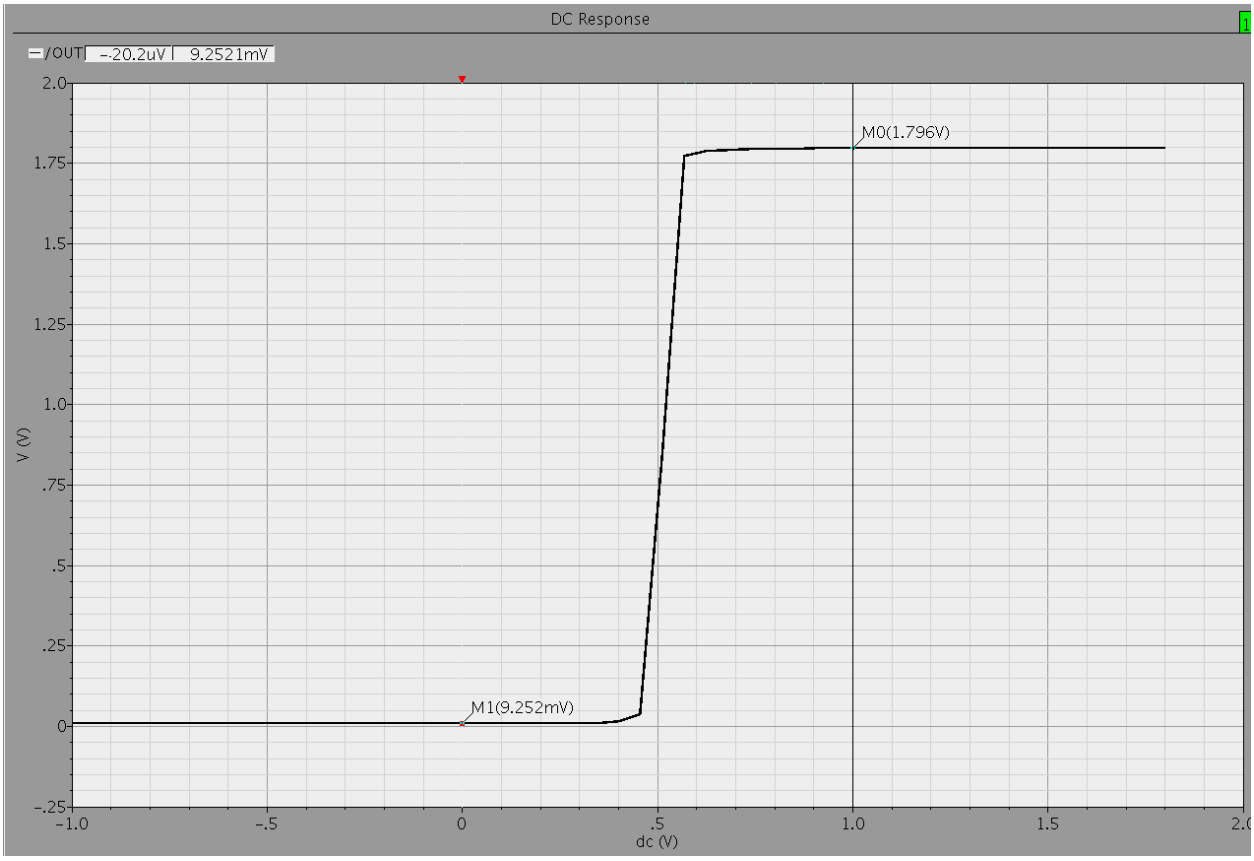


Fig 3.5 Output Waveform of Comparator and Decision Circuit

The offset Voltages are Calculated as shown in Fig.8.Here the DC voltages are connected to 0Volts.And I simulated the circuit for Zero DC voltages. The Waveform of the offset Voltage are shown.

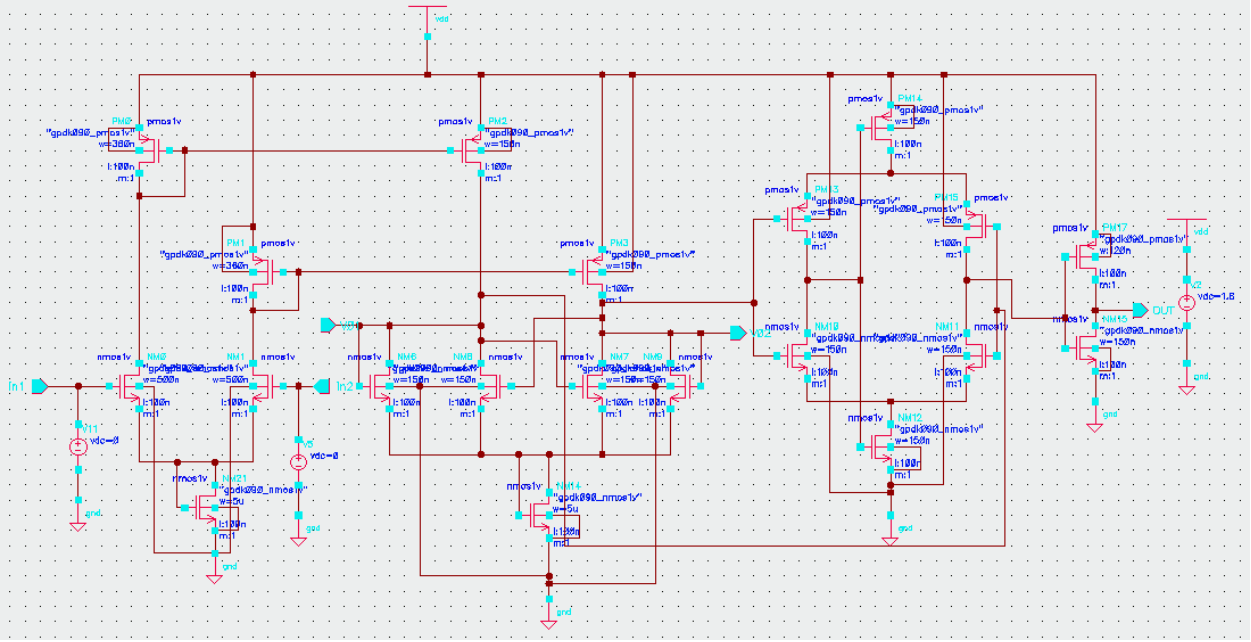


Fig.3.6 Offset circuit for preamplifier based Comparator

Offset voltage is nothing but distance between the origin and the output. Here the input voltage from -1V to 1.8V.If we see the waveform of the offset circuit the offset voltage is 186.1mV.

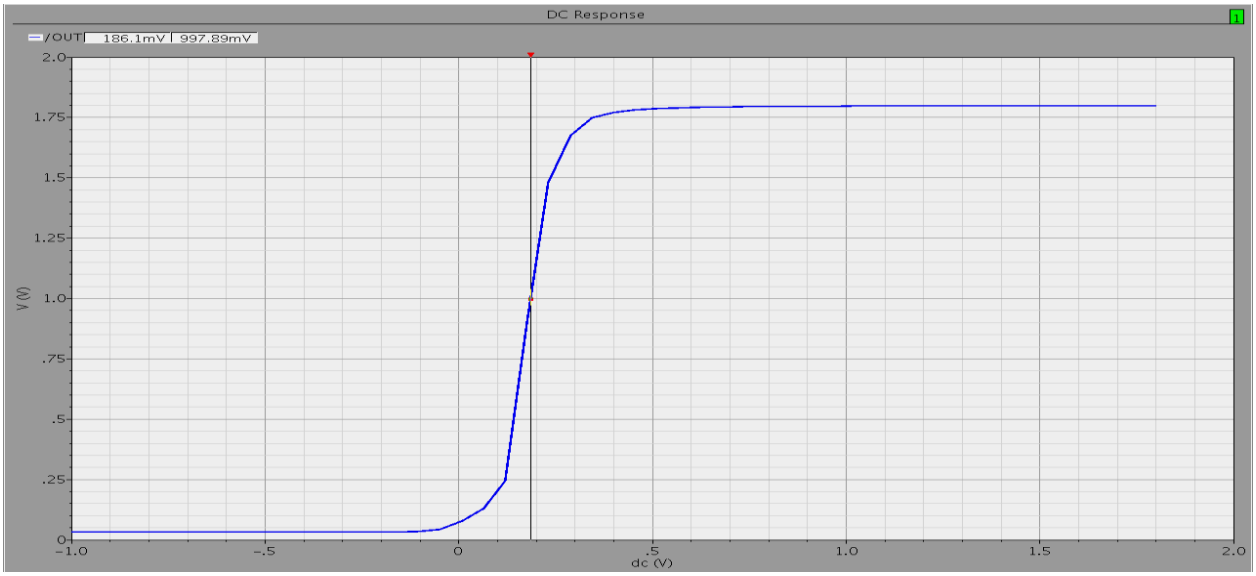


Fig .3.7 Preamplifier comparator offset voltage waveform

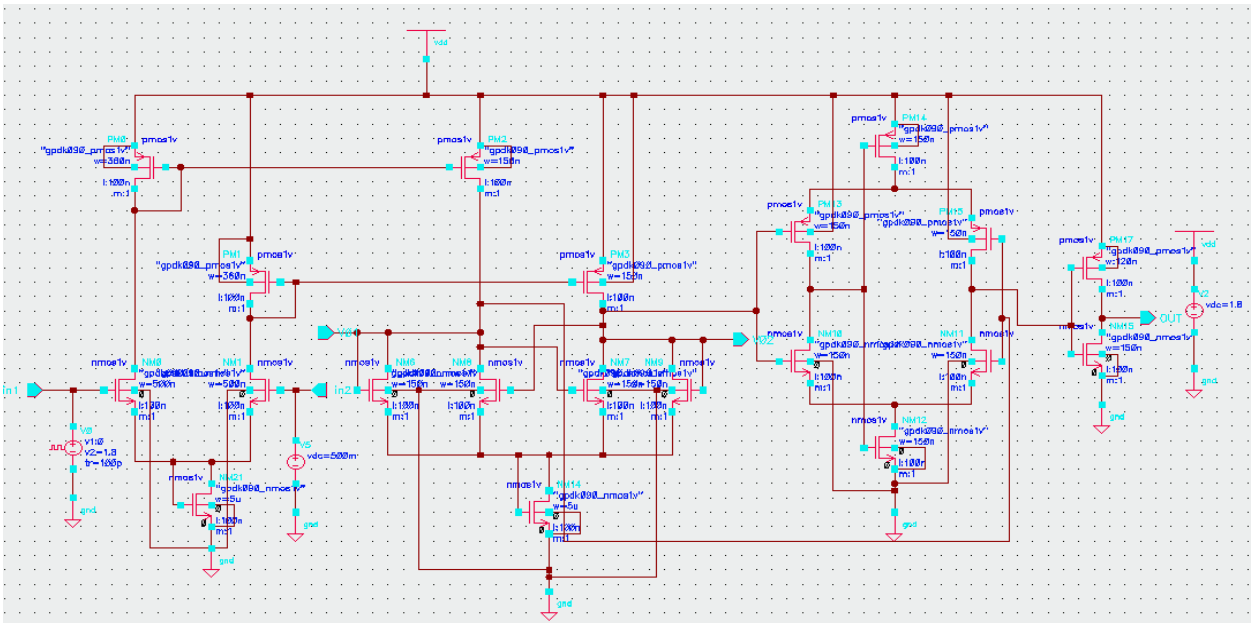


Fig.3.8 Transient analysis of Pre-amplifier based comparator

This is the circuit for calculating the delay of the Comparator. So for for calculating the delay of the Comparator I did the Transient Analysis. Here I have given input pulse to the one input of the Pre-amplifier. And I have given 500mv DC Voltage to the other end of the Pre-amplifier.

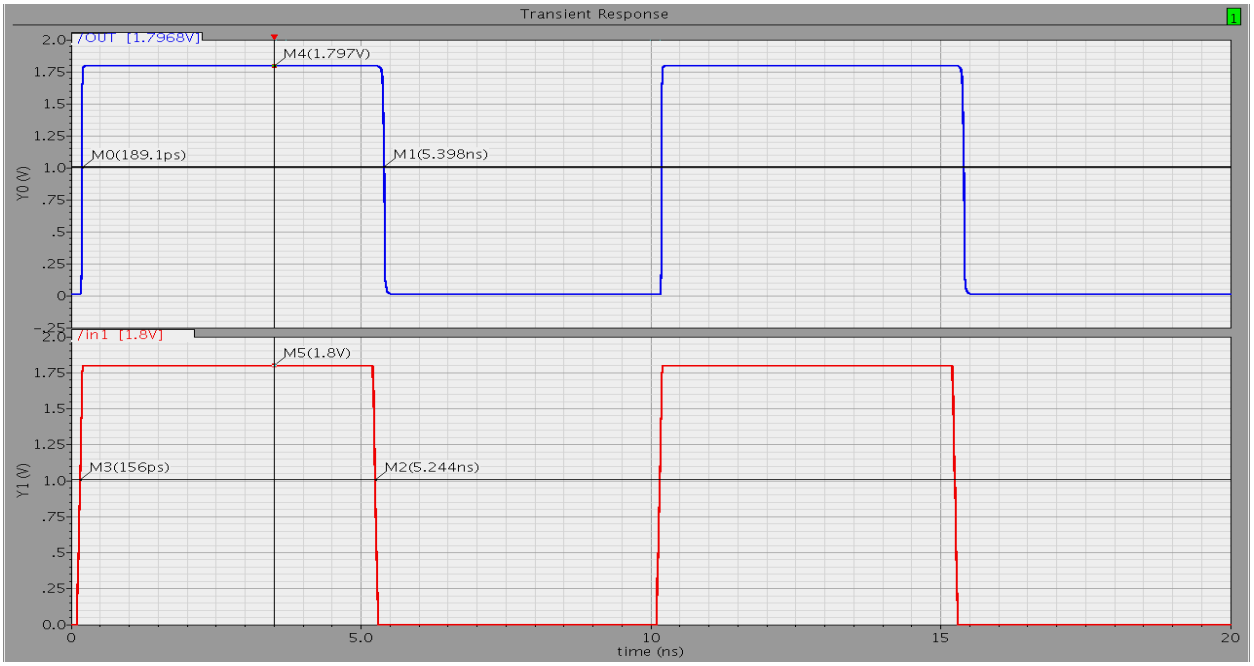


Fig.3.9 Preamplifier based comparator transient analysis waveform

3.2 Results

Calculation for Delay and speed for Pre-amplifier based comparator

Vir = 156 ps Vif = 5.244ns

Vor = 189.1 ps Vof = 5.398ns

Delay =0.033ns+0.154ns/2 =0.0935ns

Speed = 10.69 GHz

Power dissipation= 0.0922 mw

After post layout simulation calculation for Delay and speed for Pre-amplifier based comparator

Vir = 156.3ps Vif = 5.244ns

Vor = 0.227ns Vof = 5.51ns

Delay = 0.0707+0.266/2 =0.168ns

Speed = 5.952MHz

Power dissipation = 0.0924 mw

Area = 91.96um^2

3.3. DIFFERENTIAL DYNAMIC COMPARATOR

A widely used dynamic comparator in pipeline A/D converters is based on a differential sensing amplifier used in static RAM'S. This so called 'Lewis-Gray' dynamic comparator, presented in Fig.3.10, was introduced in [3]. The main advantages of this circuit are its zero DC power consumption and a linear built-in threshold adjusting circuit. TransistorsNM2-NM5 adjust the

threshold and above them transistors NM0, NM1, NM6, NM7, PM2, PM3 form a latch. The operation of the comparator is as follows.

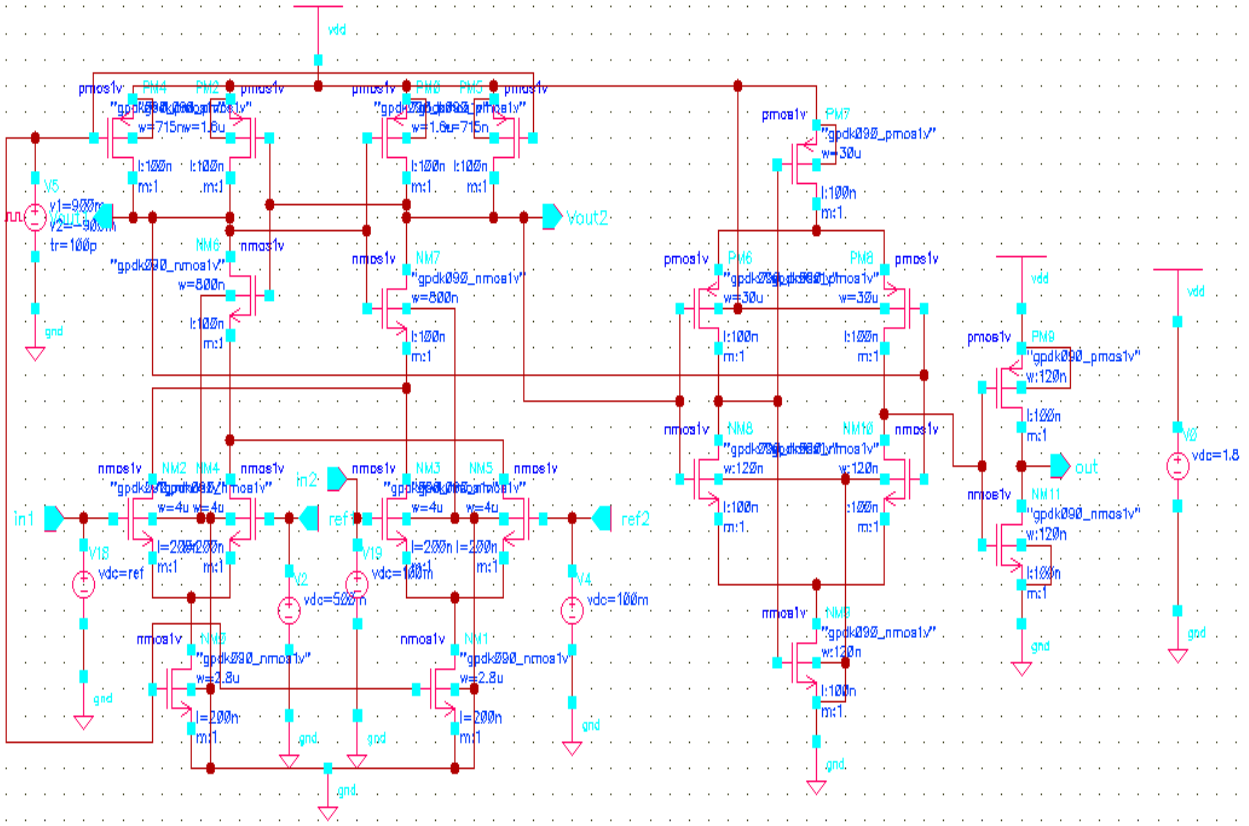


Fig. 3.10 Differential Dynamic comparator circuit

When the latch control signal is low ***(CLK** = OV)* the transistors PM4,PM5 and M12 are conducting and NM6 and NM7 are cut off, which forces both differential outputs to *Vdd* and no current path exists between the supply voltages. Simultaneously PM2 and PM3 are cut off and the transistors NM0 and NM1 conduct. This implies that NM6 and NM7 have a voltage of *Vdd* over them. When the comparator is latched the control signal goes up ***(CLK*** = Vdd), which turns NM6 and NM7 on. Immediately after the switching moment the gates of the transistors NM0 and NM1 are still at Vdd and they enter saturation. If all transistors NM0,NM1,NM6,NM7,PM2-PM5 are assumed to be perfectly matched the imbalance of the conductance of the left and right input branches, formed by NM2-NM5, determines which of the outputs goes to *Vdd* and which to *OV*. After a static situation is reached when ***CLK*** = *Vdd*, both branches are cut off and the outputs preserve their values until the comparator is reseted again by switching CLK to 0V. The transistors connected to the input and reference (NM2 – NM5) are in the triode region and act

like voltage controlled resistors. If no mismatch is present the comparator changes its output when the conductance's of the left and right input branches are equal *gL = gR.* By denoting *WA = W4and W5 and**WB*** = W2 = W3 the input voltage where the comparator changes the state is [3]:

$$V_{in}^{+} - V_{in}^{-} = \frac{W_B}{W_A}(V_{ref}^{+} - V_{ref}^{-}) \qquad (3.1)$$

By dimensioning of the transistor widths *WA* and *WB* the threshold of the comparator can be adjusted to the desired level. Eq. **(3.1)** implies that the offset of the comparator depends on the mismatch of transistors NM2 – NM5. This is true only when all other transistors NM0,NM1,NM6,NM7,PM2- PM5 are assumed to match perfectly. The transconductance of the transistors M2 –NM5 operating in the linear region can be approximately written:

$$g_{m1,2,3,4} = \mu_o C_{ox} \frac{W_{1,2,3,4}}{L} V_{ds1,2,3,4} \qquad (3.2)$$

where Vds2,3,4,5 is the drain-source voltage of the corresponding transistor. For the transistors NM0 – NM1the transconductance can be written:

$$g_{m5,6} = \mu_0 C_{ox} \frac{W_{5,6}}{L}(V_{gs5,6} - V_t) \qquad (3.3)$$

where *VT* is the threshold voltage and *Vgs0,1* are the corresponding gate-source voltages of transistors NM0 and NM1. At the beginning of the latching process Vds2,3,4 ,5= 0 while Vgs0,1 -**V**t = V*dd* . The magnitude of the transconductances gm0 and *gm1* is thus much larger than the conductance of the left and right input branches, which makes it dominant in determining the latching balance. Any mismatch between the transistors NM0 andNM1 causes large offset voltages. In order to minimize power and area consumption almost minimum size transistors are preferred, which easily results in offset voltages of a few hundred mill volts. In addition to that transistors NM0 and M1 amplify the mismatch[3]s of the input transistors NM2 – NM5. Mismatches in transistorsNM6,NM7,PM2 – PM5 are attenuated by the gain of NM0 and NM1 and are thus not so critical for the offset voltage. To scope with the mismatch problem the layout of the critical transistors must be drawn as symmetric as possible. In addition to the mismatch sensitivity the latch is also very sensitive to an asymmetry in the load capacitance. This can be avoided by adding an extra latch or inverters as a buffering stage after the comparator core outputs. The conductance's of the branches depend also from the common mode

voltage of the input and reference voltages: the lower the common mode voltage the larger the conductance's *gL* and ***gR*** are.

DC Circuit

The DC response of the above circuit is shown. Here in this circuit reference voltage is 500mV as.So above the reference voltage the Voltage is 1.779v as logic 1.and below the reference voltage the voltage is 14.39uv as logic 0.

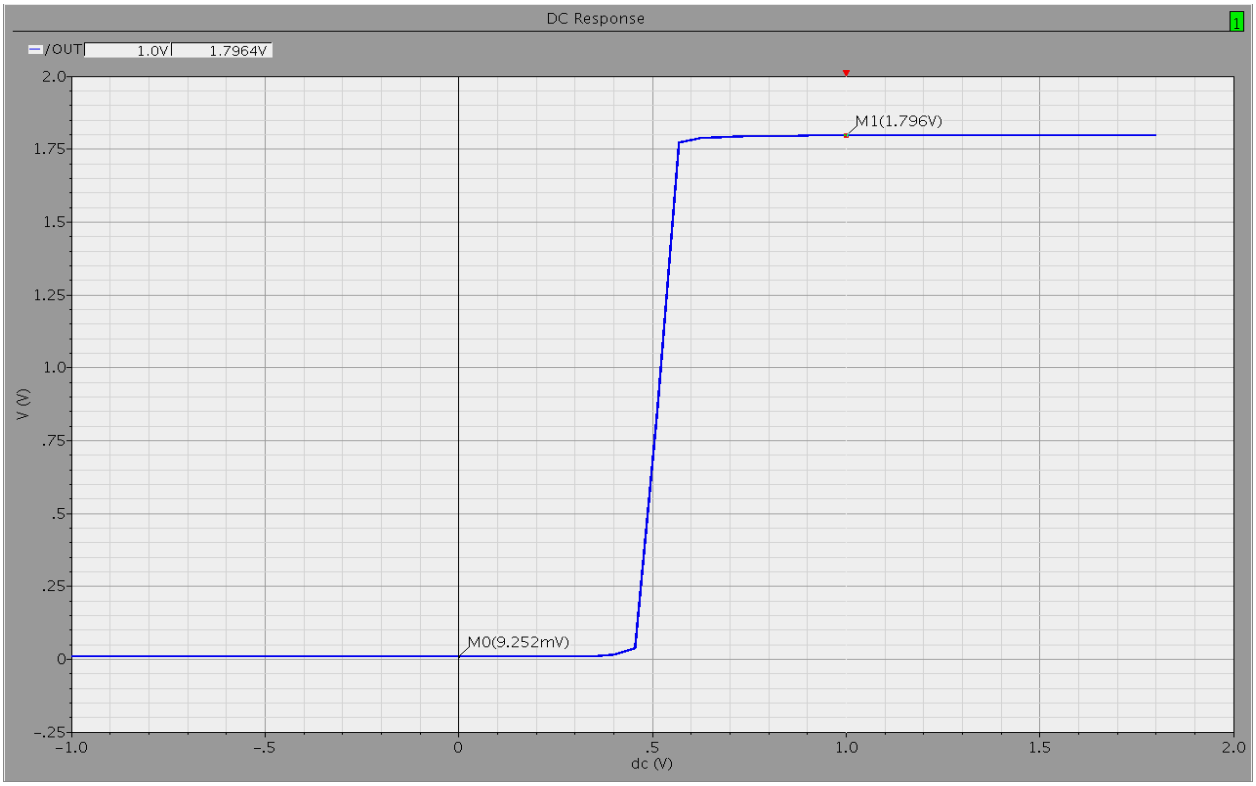


Fig. 3.11 DC Response of differential dynamic comparator

3.3.1 OFFSET CIRCUIT:-

The offset Voltages are Calculated as shown in Fig3.12.Here Zero DC voltages are connected to inputs. And the simulation are shown.

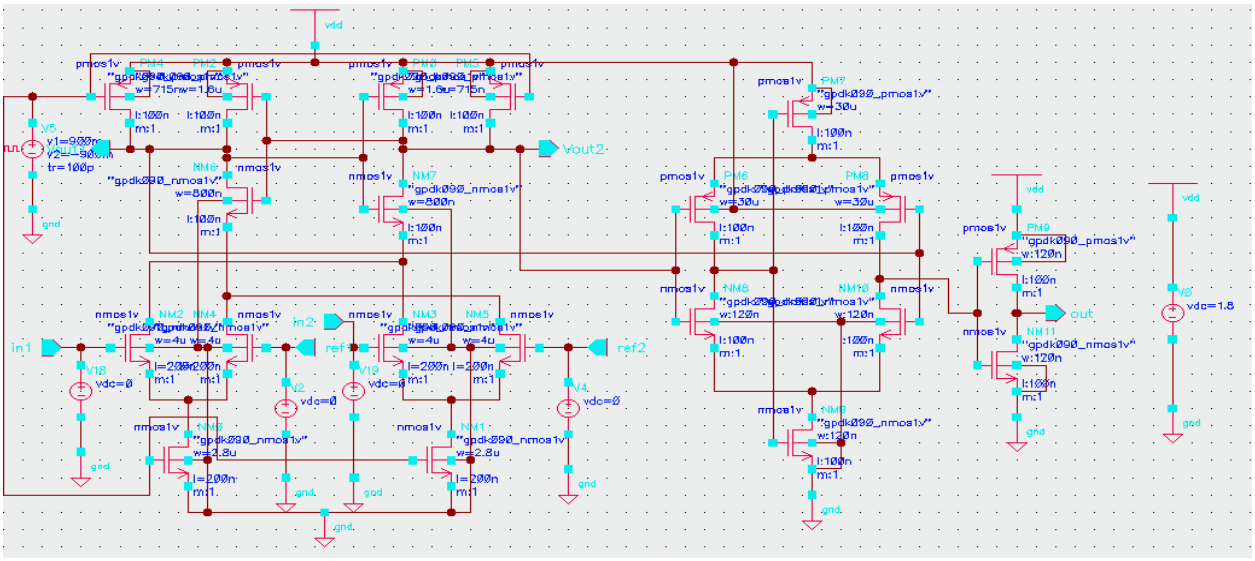


Fig. 3.12 Offset circuit for differential dynamic comparator

Offset voltage is nothing but distance between the origin and the output. Here input voltage is sweeping from -1V to 1.8V.If we see the waveform of the offset circuit the offset voltage is 208.8mV.

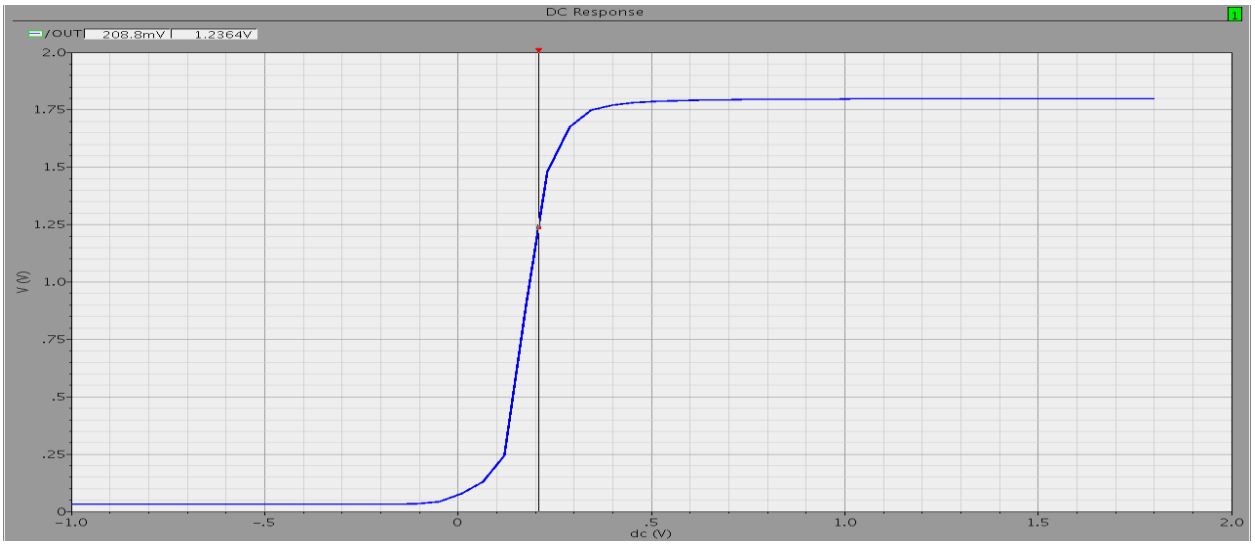


Fig. 3.13 Offset Waveform

3.3.2 Transient analysis:-

This is the circuit for calculating the delay of the Comparator. So for for calculating the delay of the Comparator the Transient Analysis is. Here the given input pulse 0 to 1.8V to the one input of the Differential Dynamic Comparator. And given 500mV as reference Voltage.

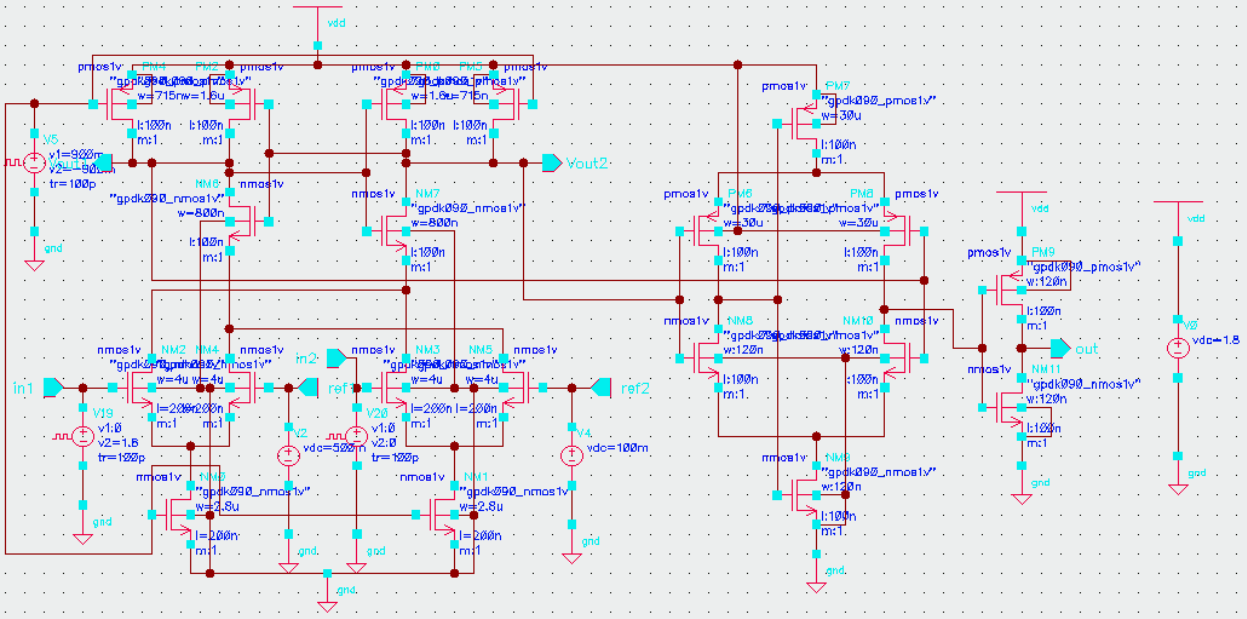


Fig. 3.14 Transient analysis circuit for Differential Dynamic Comparator

3.4 Summary of Results

Calculation for Delay and speed for Differential Dynamic comparator

V_{ir} = 156ps V_{if} = 5.244ns

V_{or} = 894.6ps V_{of} = 5.458ns

Delay = 0.7386ns+0.214ns/2 =0.476ns

Speed = 2.1 GHz

Power Dissipation= 0.34mw

The output waveforms of the circuit are shown and calculated the Delay ,Speed and Power dissipation.

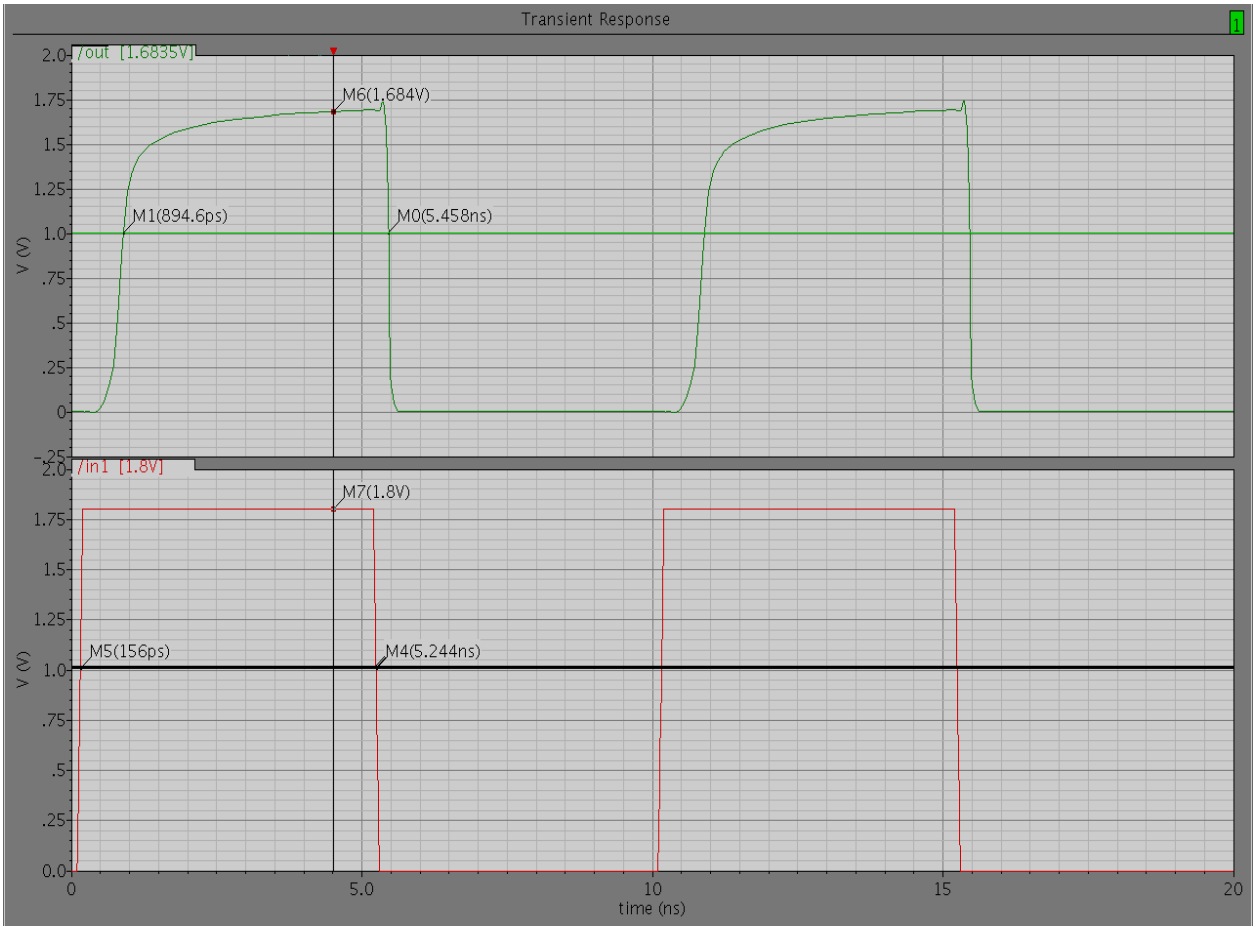


Fig. 3.15 Transient analysis waveform for Differential Dynamic Comparator

The rise time and fall time of input and output waveforms are are calculated for Delay and Speed.

After post layout simulation calculation for Delay and speed for Differential Dynamic comparator

Vir = 0.156ns Vif = 5.244ns

Vor = 0.9712ns Vof = 5.52ns

Delay = 0.8152+0.276 /2 =0.5456ns

Speed = 1.09MHz

Power Dissipation =0.338mw

Area =213.35um^2 .

3.5 Conclusion:

The conventional Comparators Preamplifier based comparator , Differential Dynamic Comparators are simulated in GPDK 90 nm .The simulation results of Preamplifier based comparator shows that the high offset voltage 186mV,and delay is 0.0935ns,Speed is 10.69GHz ,Power Dissipation is 0.0922mW.And for Differential Dynamic comparators simulation results shows that offset voltage is 208.8mV,delay is 0.476ns,Speed is 2.1 GHz, Power Dissipation is 0.34mW.This results shows high offset voltages .So that in this thesis Dynamic comparators are chosen for less offset voltage, high Speed and these architectures are explained in the Next Section.

Chapter 4

Design of Novel Dynamic Comparators

4.1 DYNAMIC COMPARATOR DESIGN:-

A fully differential typical dynamic comparator is shown in fig.4.1. The comparator consists of two cross coupled differential pairs with inverter latch at the top. Comparison is made based on the inverter currents, which are related to the inputs, when the $Ø_{clk}$ goes high. The trip point can be changed by appropriate input transistor sizing .

Few points are worth noting in regard to the problems present in this structure. The first drawback of normal differential comparator is related to the clocking of the tail current. When clock signal goes high, the tail current will go into linear region and will be function of the inputs of the respective differential pair. If there are any non-idealities or mismatches present (from the point view of symmetry), the two inverter tail currents will not be same and will result in large offset for the comparator. The second problem is related to the inputs of a differential pair. A large difference between the two inputs to a differential pair will result in the turning of one of the differential pair MOSFET and all of the tail current[3] will be drawn into the other MOSFET. Hence, in effect comparator will be only comparing V_{in}^{+} with V_{ref}^{+} (or V_{in}^{-} with V_{ref}^{-}) rather than a comparison of differential V_{in} with differential V_{ref} . The third potential problem associated with the previous code dependent biased decision. This can happen if there is some charge imbalance left from previous decision at one of the nodes of the comparator which can affect next decision.

To overcome the drawbacks of the typical differential pair comparator, a new dynamic comparator has been proposed in the next section which addresses the above listed problems.

4.1.1 Dynamic Comparator Operation:-

When the comparator is inactive the *clk* is at *OV,* means that the current source transistors NM6 and NM7are switched off and no current path between the supply voltages exists. Simultaneously the PMOS switch transistors PM1 and PM4 reset the outputs by shorting them to *Vdd.* The NMOS transistors NM0 and NM1 of the latch conduct and force also the drains of all the input transistors NM2 – NM5 to Vdd potential. When *clk* is risen to Vdd ,the outputs are disconnected from the positive supply and the switching current sources NM6 and NM7 enter saturation and begin to conduct. The waveform of the Dynamic comparator is

shown. Here the given reference voltage as 500mV.So below 500mV it should give logic0.And after reference Voltage it should give logic1.And sweeping the input Voltage as -1V to 1.8V.The wave form of the Dynamic comparator is shown in Fig.4.2.

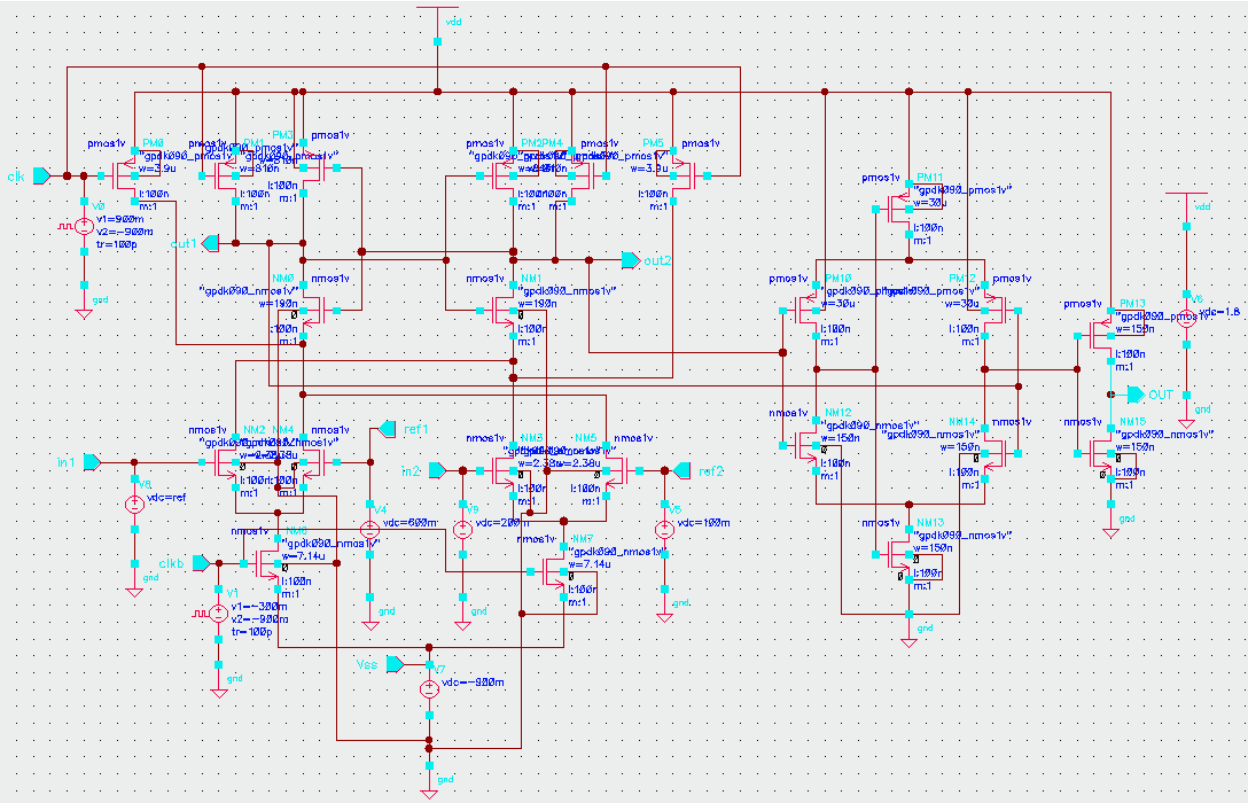


Fig.4.1 .Dynamic comparator circuit

Dynamic comparator structure is shown in fig(4.1) .Operation of this dynamic comparator is same as the typical case here also the decision is been made during the period when the $Ø_{clk}$ goes high. The comparator will have a meta-stable point when both the inverter currents are same.

Few modifications have been made to this structure as compared to the typical structure. The first modification is related to the tail current clock signal. Instead of using the same clock as that for the top switches, which goes from V_{SS} to V_{DD} , a same phase restricted voltage swing clock ($Ø_{clk,B}$) has been used, i.e. $Ø_{clk,B}$ high is less than V_{DD} , which can be easily generated from the main clock by using desired high voltage of an inverter or by using resistor ladder. The restricted swing clock is used to ensure that differential pair tail current remains in the saturation region rather than going into linear region. Thus a constant tail current is

achieved. This is very important during the time the comparator is making a decision. The second modification is related to the input signals. As pointed out in the typical differential pair comparator, one of the input transistors [3]will be turned off if there is a large input differential and will result in the comparison of two signals rather than comparison of the two differential signals. To address this problem V_{in}^{+} and V_{ref}^{+}(and V_{in}^{-} and V_{ref}^{-}) are combined in one differential pair as compared to V_{in}^{+} and V_{in}^{-}(and V_{ref}^{+} and V_{ref}^{-}). Hence, for a case where all the input transistors are of the same size and no imbalance is present, at the trip point of the comparator, the transistors NM0 and NM1 will have same current, as well as, NM2 and NM3 will have same current. Therefore, all four input transistors will contribute respective currents for making a decision.

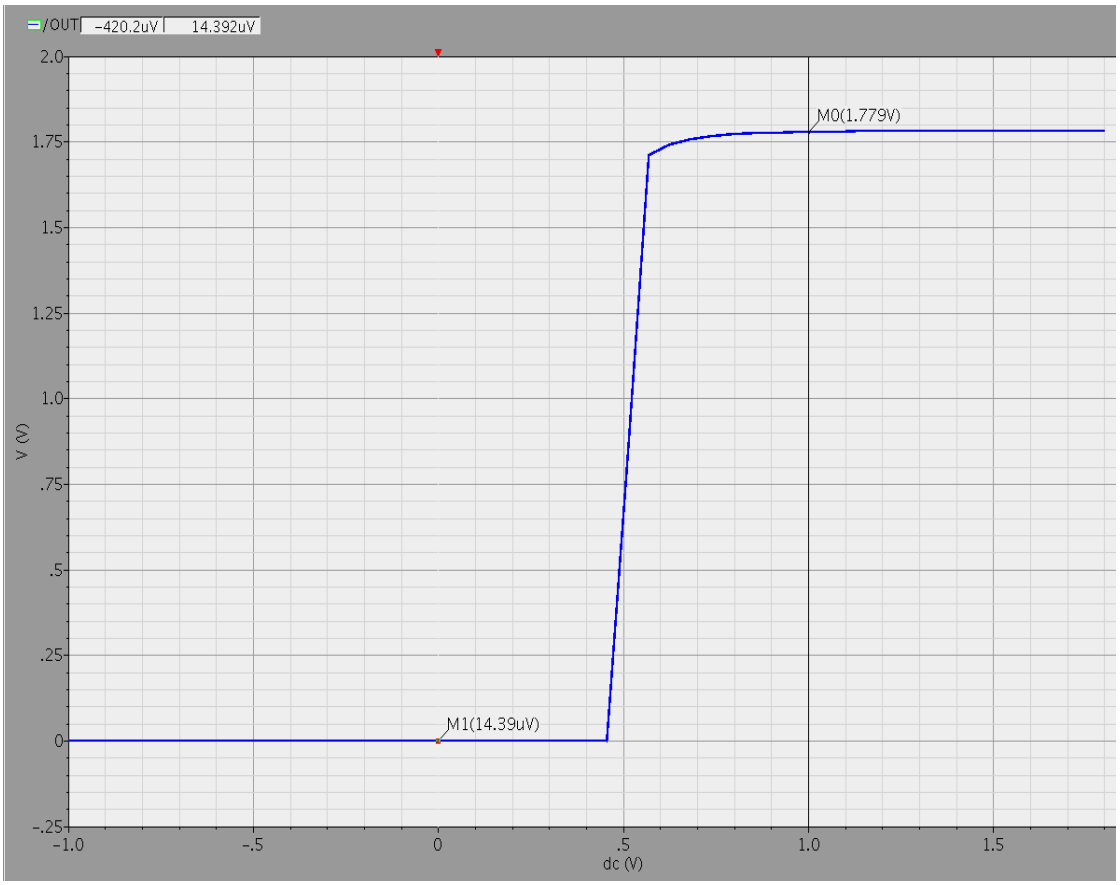


Fig.4.2 .DC analysis of dynamic comparator wave form

4.1.2 Dynamic comparator transient response:-

This is the circuit for calculating the delay of the Comparator. So for calculating the delay of the Comparator the Transient Analysis is done. Here I have given input pulse from 0 to 1.8V to the one input of the Differential pair. And 100mV DC Voltage to the other end of the differential pair. The output wave forms are shown in Fig.4.4.the comparison the input pulse and output waveform some delay is there. So the average of the two ends of the output waveform as Speed of the Comparator. So the average speed of the Comparator is 0.4618nS.

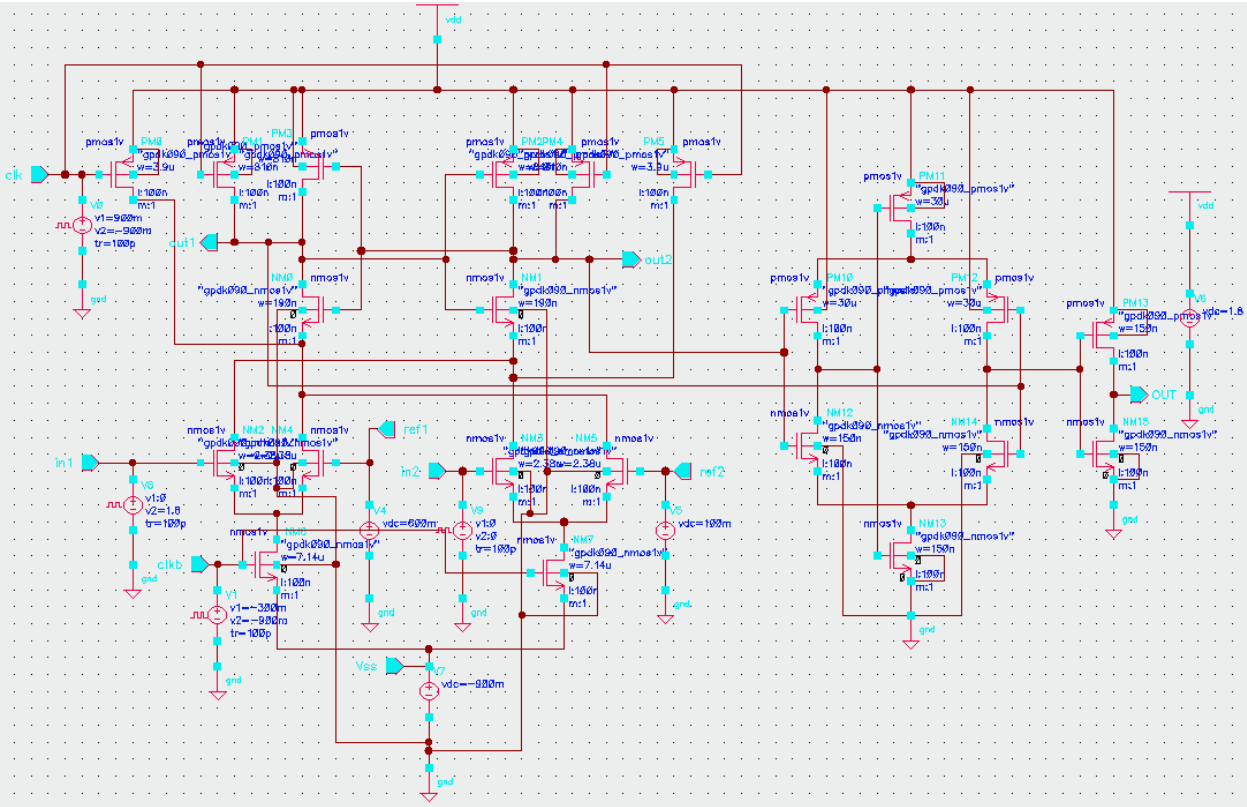


Fig.4.3 Dynamic comparator transient response circuit

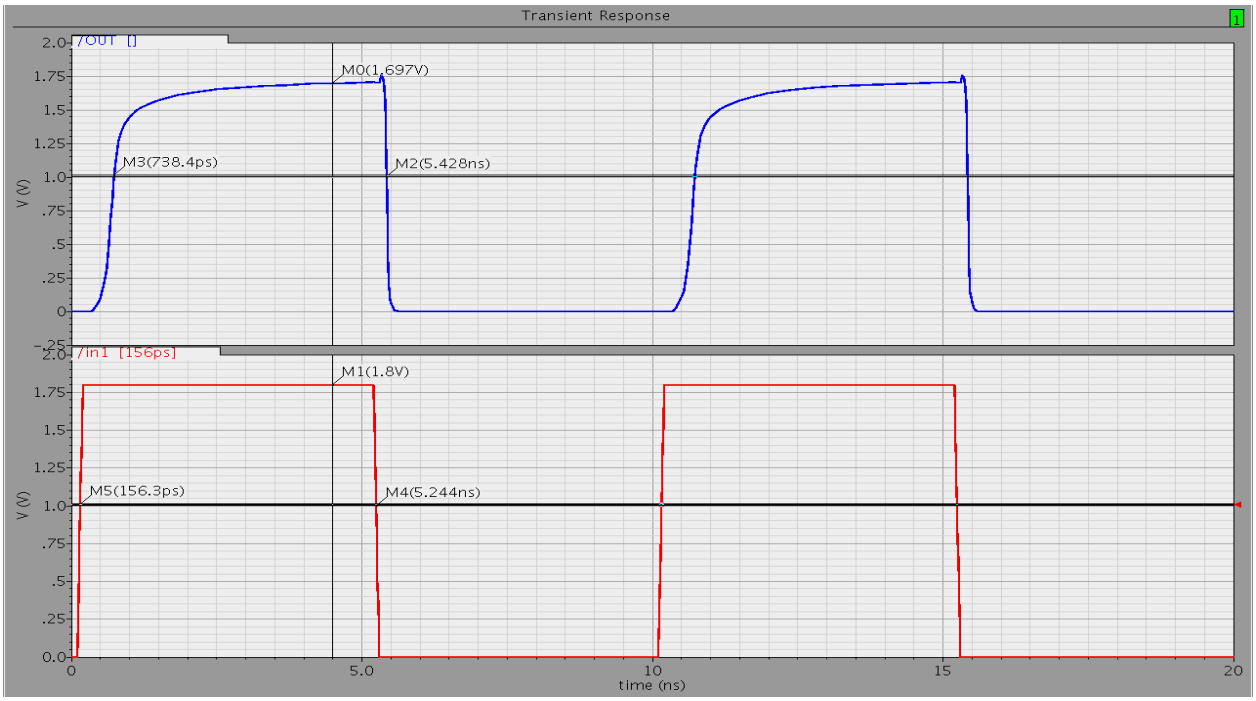


Fig.4.4 Transient response of dynamic comparator

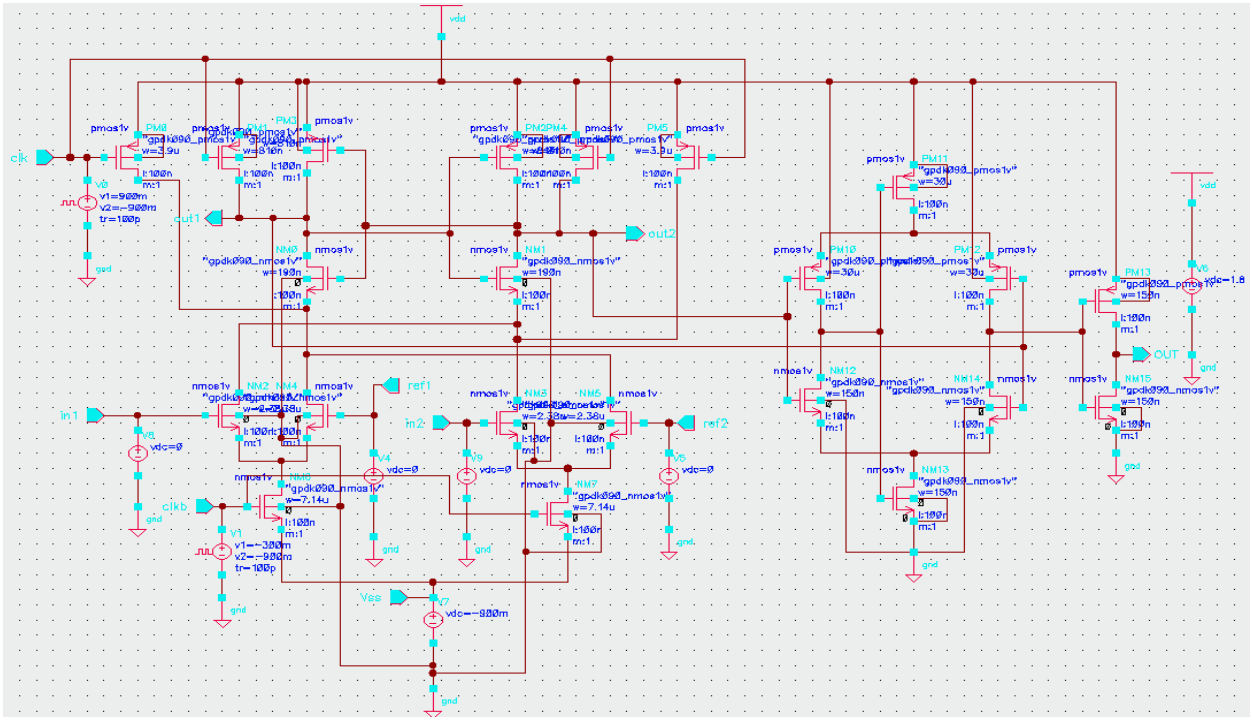


Fig.4.5.Offset voltage circuit for dynamic comparator

4.2 Summary of Results

Calculation for Delay and speed for Dynamic comparator

Vir = 156.3ps Vif = 5.244ns

Vor = 738.4ps Vof = 5.428ns

Delay = 0.5821ns+0.184ns/2 =0.383ns

Speed = 1.83 GHz

Power Dissipation= 0.34mw

This circuit is the offset of the Dynamic Comparator. Here for finding the offset all the input voltages are given to 0 DC Voltage. The offset waveform is shown in the figure. and calculated offset as 48.32mv.

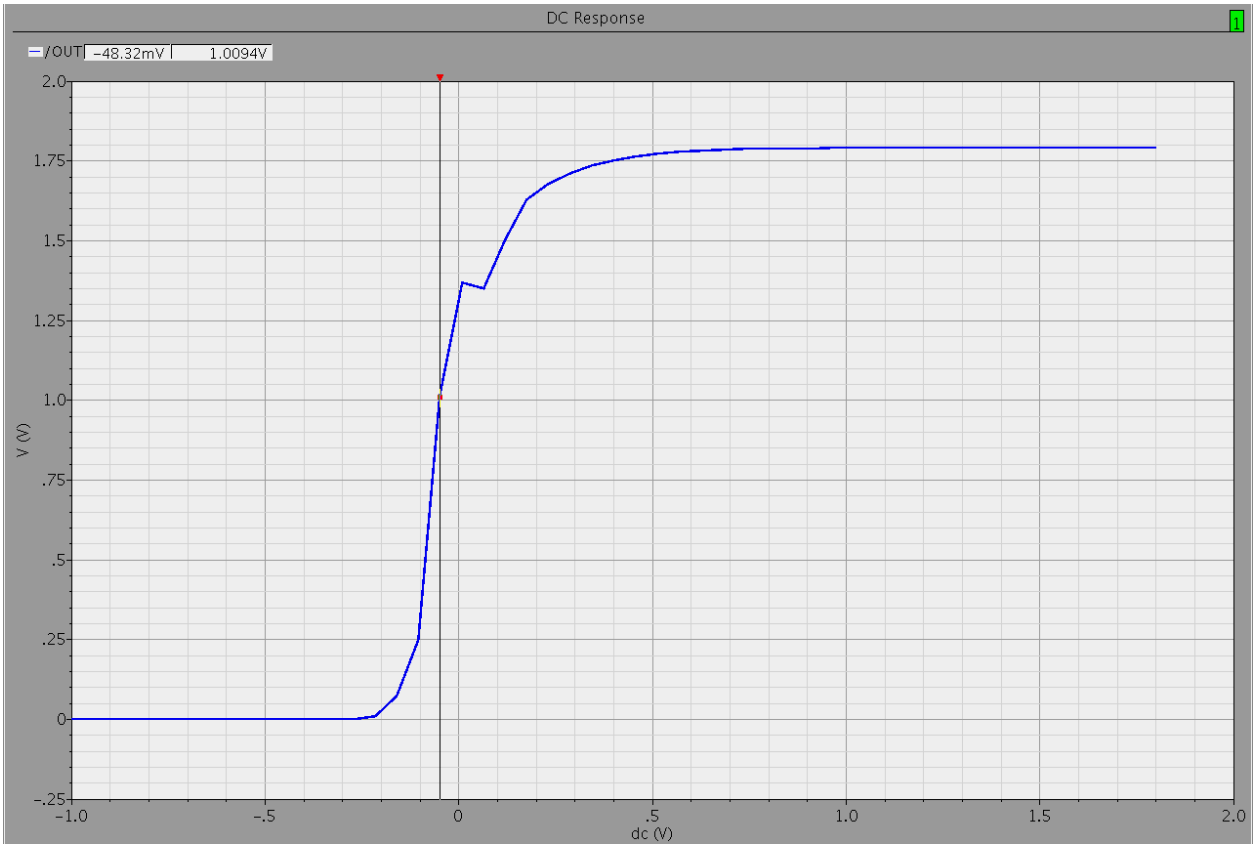


Fig. 4.6 Offset circuit for dynamic comparator

After post layout simulation calculation for Delay and speed for Dynamic comparator

Vir = 156.3ps Vif = 5.244ns

Vor = 824ps Vof = 5.5ns

Delay = 0.6677ns+0.256 ns/2 =0.4618ns.

Speed = 2.16MHz.

Power Dissipation = 3.543 mw.

Area =232.35um^2

4.3 DYNAMIC COMPARATOR USING POSITIVE FEEDBACK

This is the circuit of Dynamic comparator using positive feedback. The hysteresis can also be accomplished by using internal positive feedback. Figure 4.13 shows the differential input stage of a comparator . In this circuit there are two paths of feedback. The first is current-series [15,16] feedback through the common-source node of transistors NM2 and NM5. This feedback path is negative. The second path is the voltage-shunt feedback through the gate-drain connections of transistors PM14 and PM16.[6] This path of feedback is positive. If the positive-feedback factor is less than the negative-feedback factor, then the overall feedback will be negative and no hysteresis will result. If the positive-feedback factor becomes greater, the overall feedback will be positive, which will give rise to hysteresis in the voltage-transfer curve. As long as the ratio $\beta_{NM14}/\beta_{NM17}$ is less than one, there is no hysteresis in the transfer function. When this ratio is greater than one, hysteresis will result.

The following analysis will develop the equations for the trip points when there is hysteresis Assume that plus and minus supplies are used and that the gate of NM2 is tied to grouond.In this input and reference voltages we are giving here are differential stages. So With the input of NM5 much less than zero, NM2 is on and NM5 is off, thus turning on PM17 and PM14 and turning off PM15 and PM16. All of i_6 flows through NM2 and NM17, so V_{out2} is high.

Note that NM5 is shown even though it is off. At this point. NM14 is attempting to source the following amount of current:

$$i_{PM14} = \frac{(W/L)_{PM14}}{(W/L)_{PM17}} i_{PM17} \qquad (4.3.1)$$

As Vin increases toward the threshold point (which is not yet known), some of the tail current is begins to flow through NM5. This continues until the point where the current throughNM5 equals the current in PM14. Just beyond this point the comparator switches state.To approximately calculate one of the trip points, the circuit must be analyzed right at the point where i_{NM5} equals $i_{PM14.}$

Mathematically this is

$$i_{PM14} = \frac{(W/L)_{PM14}}{(W/L)_{PM17}} i_{PM17} \qquad (4.3.2)$$

$$i_{NM5} = i_{PM14} \qquad (4.3.3)$$

$$i_{NM6} = i_{NM5} + i_{NM2} \qquad (4.3.4)$$

$$\therefore i_{PM17} = \frac{i_{NM6}}{1 + [(W/L)_{PM14} \,/\, (W/L)_{PM17}]} = i_{NM2} \qquad (4.3.5)$$

$$i_{NM5} = i_{NM6} - i_{NM2} \qquad (4.3.6)$$

Knowing the currents in both NM2 and NM5, it is easy to calculate their respective V_{Gs} voltages. Since the gate of NM2 is at ground, the difference in their gate-source voltages will yield the positive trip point as given below:

$$(V_{GS})_{NM2} = \sqrt{\frac{2i_{NM2}}{\beta_{NM2}}} + V_{T1}$$

$$(V_{GS)})_{NM5} = \sqrt{\frac{2i_{NM5}}{\beta_{NM5}}} + V_{T2} \qquad (4.3.7)$$

$$V_{TRP+} = (V_{GS})_{NM5} - (V_{GS})_{NM2} \qquad (4.3.8)$$

Once the threshold is reached, the comparator changes state so that the majority of the tail current now flows through NM5 and PM15. As a result, PM16 is also turned on, thus turning off PM17, PM14, and NM2. As in the previous case, as the input decreases the circuit reaches a point at which the current in NM2 increases until it equals the current in PM16. The input voltage at this point is the negative trip point V_{TRP-} To calculate the trip point[6], the following equations apply:

$$i_{PM16} = \frac{(W/L)_{PM16}}{(W/L)_{PM15}} i_{PM15}$$

$$i_{NM2} = i_{PM16}$$

$$i_{NM6} = i_{NM5} + i_{NM2}$$

Therefore, $i_{PM16} = \frac{i_{NM6}}{1 + [(W/L)_{PM16} / (W/L)_{PM15}]} = i_{NM5}$, $i_{NM2} = i_{NM6} - i_{NM5}$

to calculate V_{GS}, the trip point is

$$V_{TRP-} = (V_{GS})_{NM5} - (V_{GS})_{NM2}$$

4.3.1 DC CIRCUIT:-

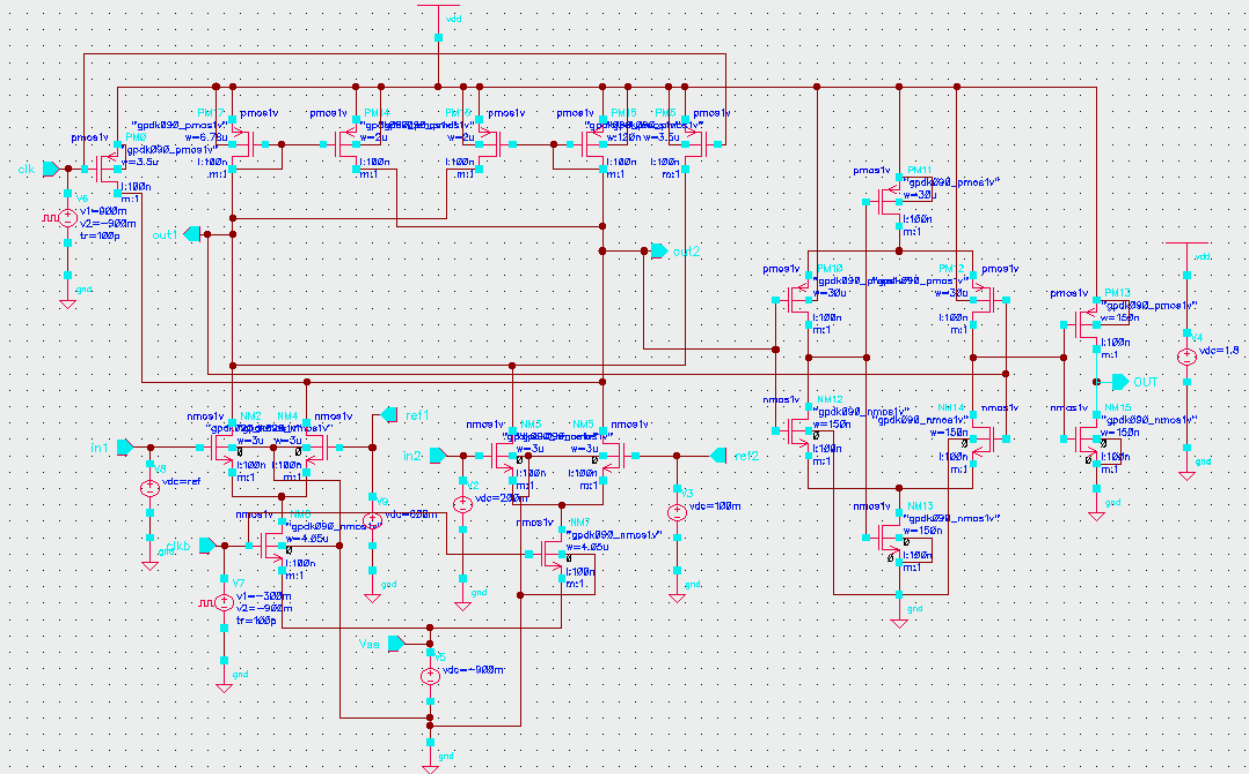


Fig. 4.7 dc circuit dynamic comparator using positive feedback

The DC response of the above circuit is shown.Here in this circuit 500mv as reference voltage.So above the reference voltage the Voltage is 1.776v as logic 1.and below the reference voltage the voltage is 15.16uv as logic 0.

Dc waveform:-

The DC wave form is shown .In this circuit the reference voltage is 500mv.so tripping should occur at the 500mv.

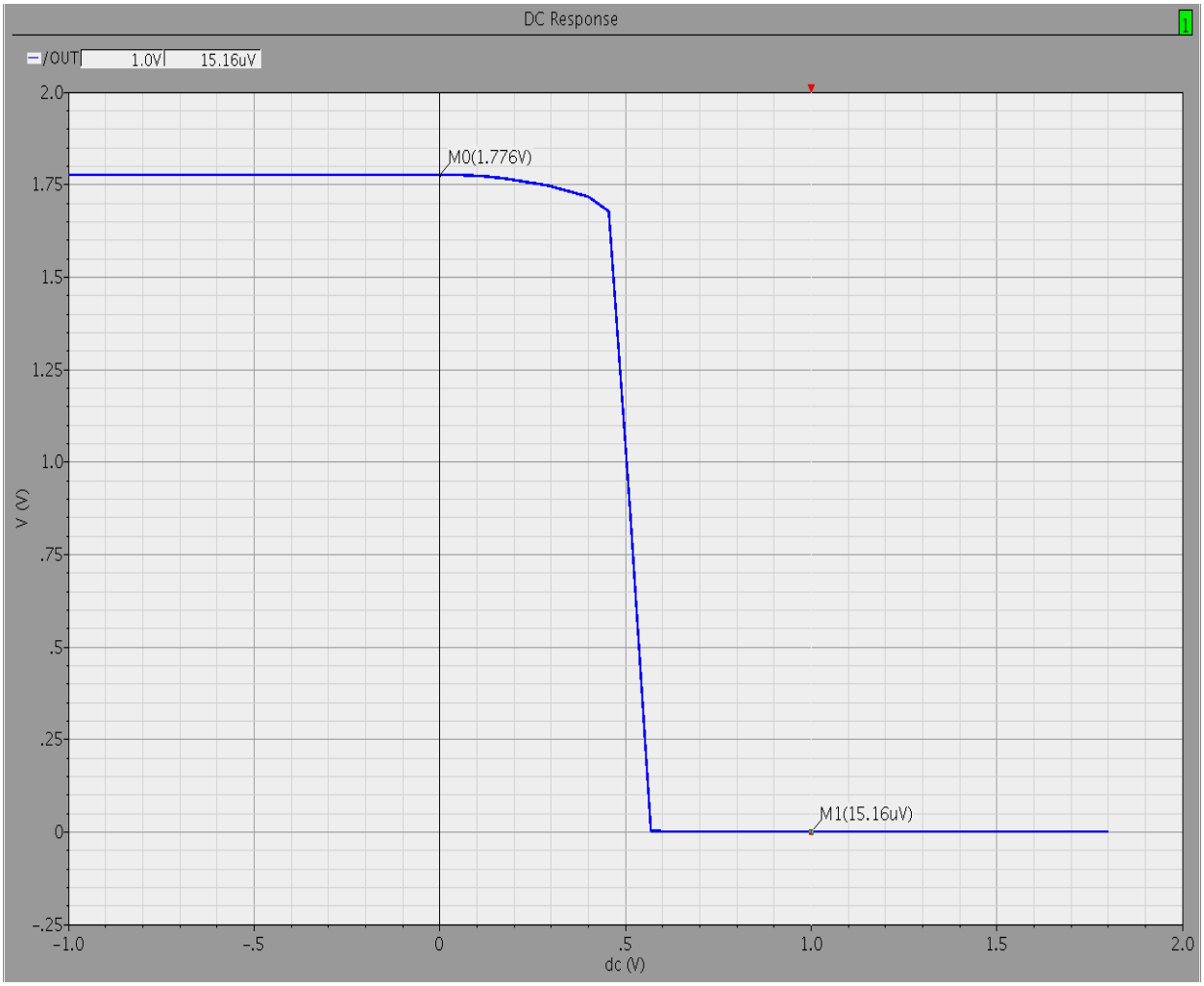


Fig. 4.8 DC Waveform for dynamic comparator using positive feedback

4.3.2 Offset circuit:

The offset Voltages are Calculated as shown in Fig4.9.and connected all the DC voltages as 0Volts.And the simulated the circuit for Zero DC voltages. The Waveform of the offset Voltage are shown.

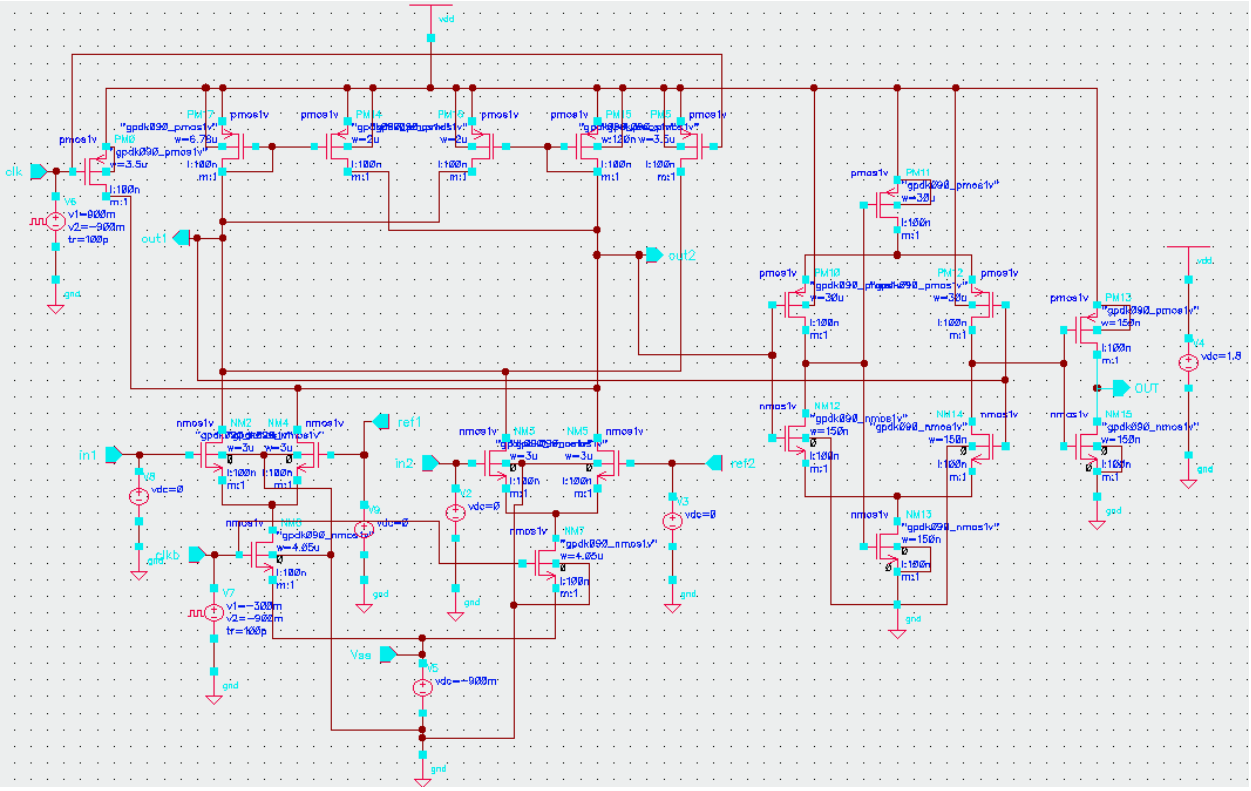


Fig. 4.9 Offset circuit for dynamic comparator using positive feedback

Offset voltage is nothing but distance between the origin and the output. Here input voltage is sweeping the from -1V to 1.8V.The waveform of the offset circuit the offset voltage is 21.41mV.The offset waveform is shown in fig.4.10

Offset waveform:-

Offset voltage is nothing but distance between the origin and the output. Here input voltage sweeping the from -1V to 1.8V.If we see the waveform of the offset circuit the offset voltage is 30.67mV.

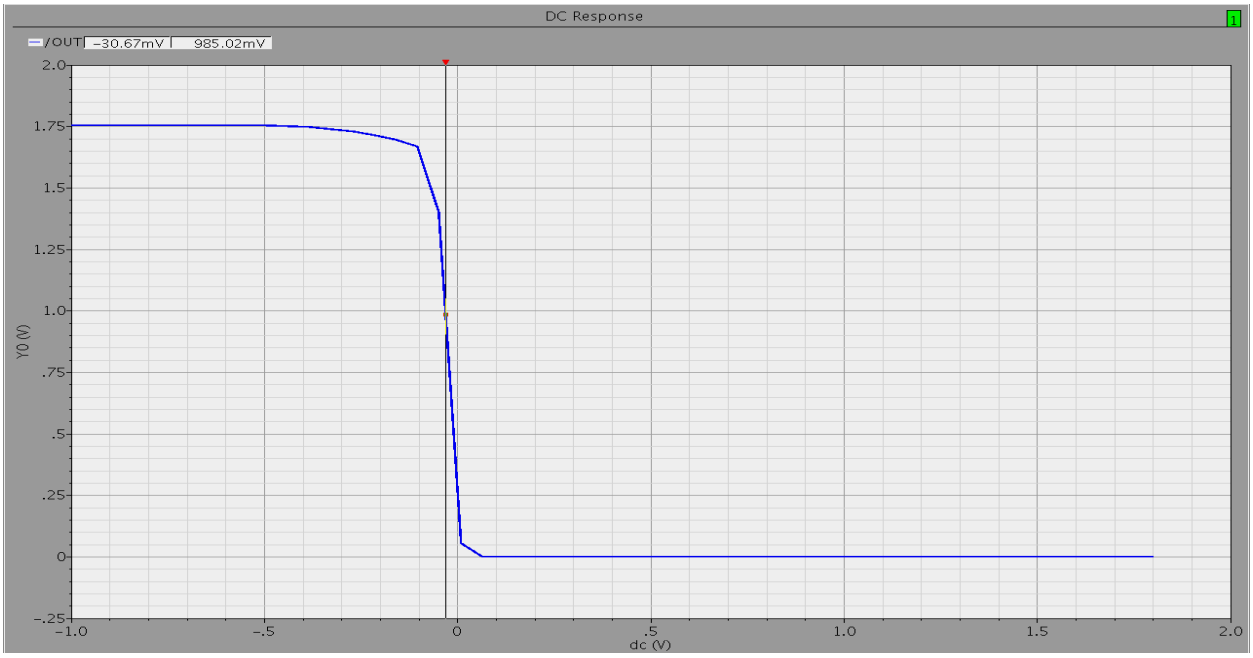


Fig. 4.10 Offset Waveform for dynamic comparator using positive feedback

4.3.3 Transient circuit

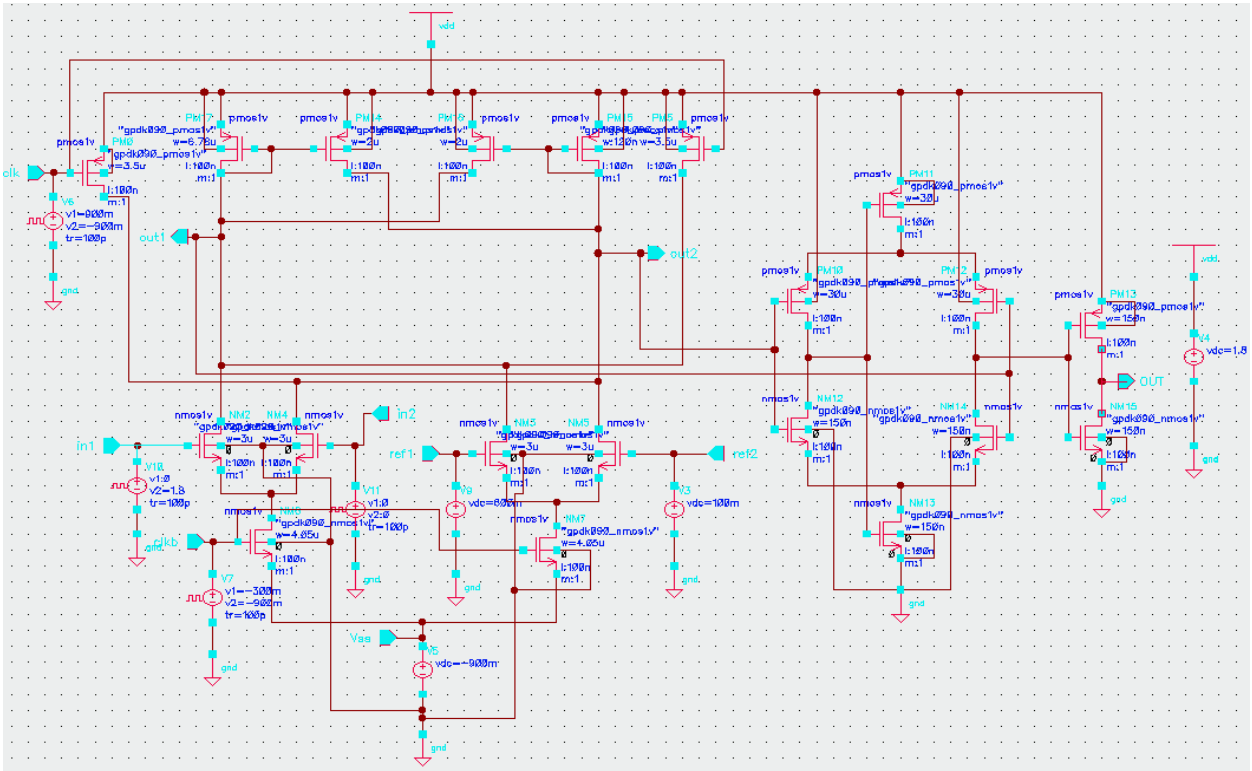


Fig. 4.11 Transient circuit for dynamic comparator using positive feedback

This is the circuit for calculating the delay of the Comparator. So for calculating the delay of the Comparator the Transient Analysis is. Here 1.8v as input pulse given to the one input of the Dynamic Comparator using positive feedback. And 500mv as reference Voltage. The output waveforms of the circuit are shown and calculated the Delay ,Speed and Power dissipation.

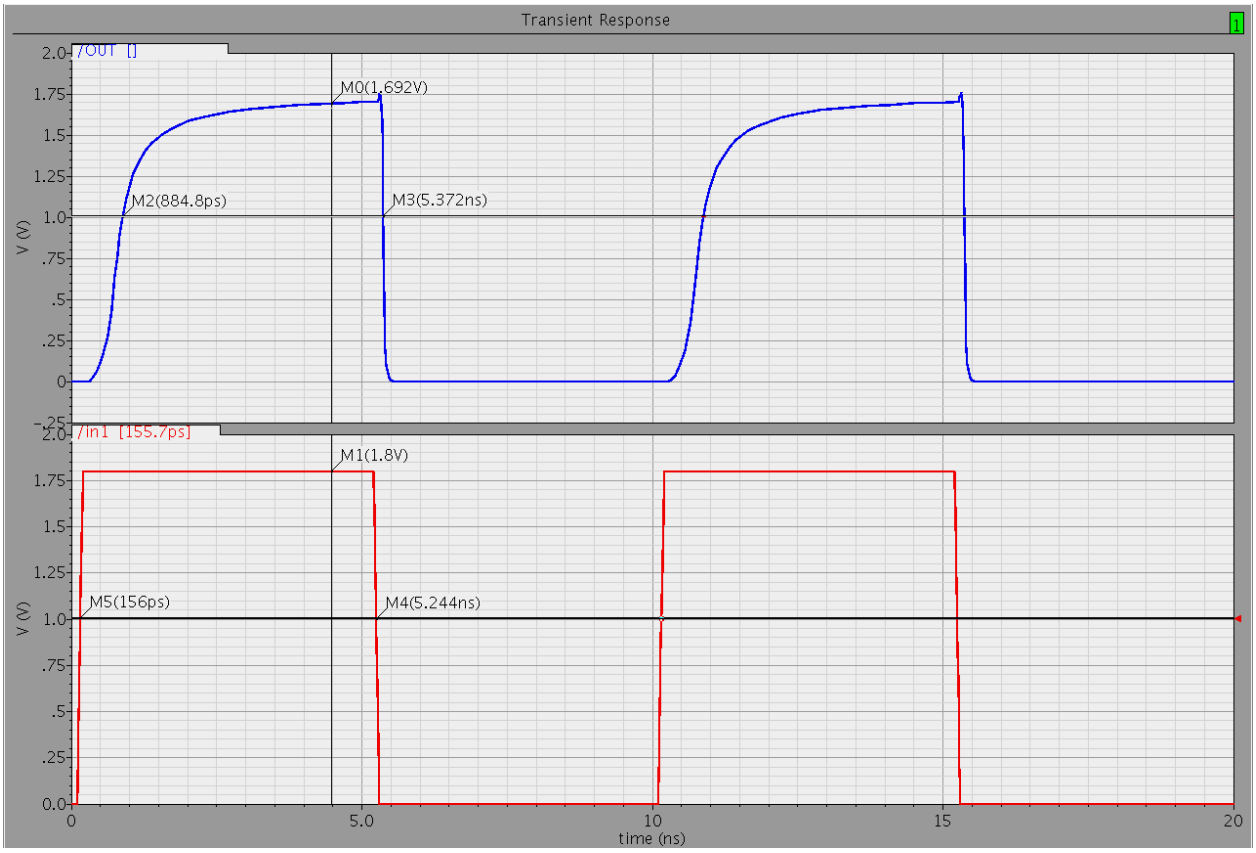


Fig. 4.12 Transient wave form for dynamic comparator using positive feedback

The rise time and fall time of input and output waveforms are are calculated for Delay and Speed.

4.4 Summary of Results

Calculation for Delay and speed for Dynamic comparator using positive feedback

Vir = 156ps Vif = 5.244ns

Vor = 884.8ps Vof = 5.372ns

Delay = 0.7288ns+ 0.128 ns /2 =0.4284ns

Speed = 2.334 GHz

Power Dissipation= 2.47mw

After post layout simulation calculation for Delay and speed for Dynamic comparator using positive feedback

Vir = 156.6s Vif = 5.244ns

Vor = 841.7ps Vof = 5.429ns

Delay = 0.6857ns+0.185ns/2 = 0.8707/2 =0.4353ns

Speed =2.28MHz

Power Dissipation = 2.297mw

4.5. DYNAMIC COMPARATOR USING POSITIVE FEEDBACK: PMOS AS A SWITCH

This is the circuit of Dynamic comparator using positive feedback. The hysteresis can also be accomplished by using internal positive feedback. Figure 4.13 shows the differential input stage of a comparator . In this circuit there are two paths of feedback. The first is current-series [15,16] feedback through the common-source node of transistors NM2 and NM5. This feedback path is negative. The second path is the voltage-shunt feedback through the gate-drain connections of transistors PM14 and PM16[6]. This path of feedback is positive. If the positive-feedback factor is less than the negative-feedback factor, then the overall feedback will be negative and no hysteresis will result. If the positive-feedback factor becomes greater, the overall feedback will be positive, which will give rise to hysteresis in the voltage-transfer curve. As long

as the ratio $\beta_{NM14}/\beta_{NM17}$ is less than one, there is no hysteresis in the transfer function. When this ratio is greater than one, hysteresis will result.

The following analysis will develop the equations for the trip points when there is hysteresis Assume that plus and minus supplies are used and that the gate of NM2 is tied to grouond.In this input and reference voltages we are giving here are differential stages.So With the input of NM5 much less than zero, NM2 is on and NM5 is off, thus turning on PM17 and PM14 and turning off PM15 and PM16. All of i_6 flows through NM2 and NM17, so V_{out2} is high. Note that NM5 is shown even though it is off. At this point. NM14 is attempting to source the following amount of current:

$$i_{PM14} = \frac{(W/L)_{PM14}}{(W/L)_{PM17}} i_{PM17} \qquad (4.5.1)$$

As Vin increases toward the threshold point (which is not yet known), some of the tail current is begins to flow through NM5. This continues until the point where the current throughNM5 equals the current in PM14. Just beyond this point the comparator switches state. To approximately calculate one of the trip points[6], the circuit must be analyzed right at the point where i_{NM5} equals $i_{PM14.}$ In this circuit two PMOS switches are connected to clk.so these two PMOS switches draws more current .So mismatches are reduced .After simulation the offset voltage is 18.07mV

Mathematically this is

$$i_{PM14} = \frac{(W/L)_{PM14}}{(W/L)_{PM17}} i_{PM17} \qquad (4.5.2)$$

$$i_{NM5} = i_{PM14} \qquad (4.5.3)$$

$$i_{NM6} = i_{NM5} + i_{NM2} \qquad (4.5.4)$$

therefore

$$\therefore i_{PM17} = \frac{i_{NM6}}{1+\left[\dfrac{(W/L)_{PM14}}{(W/L)_{PM17}}\right]} = i_{NM2} \qquad (4.5.5)$$

$$i_{NM5} = i_{NM6} - i_{NM2} \qquad (4.5.6)$$

Knowing the currents in both NM2 and NM5, it is easy to calculate their respective V_{Gs} voltages. Since the gate of NM2 is at ground, the difference in their gate-source voltages will yield the positive trip point as given below:

$$(V_{GS})_{NM2} = \sqrt{\frac{2i_{NM2}}{\beta_{NM2}}} + V_{T1}$$

$$(V_{GS)})_{NM5} = \sqrt{\frac{2i_{NM5}}{\beta_{NM5}}} + V_{T2} \qquad (4.5.7)$$

$$V_{TRP+} = (V_{GS})_{NM5} - (V_{GS})_{NM2} \qquad (4.5.8)$$

Once the threshold is reached, the comparator changes state so that the majority of the tail current now flows through NM5 and PM15. As a result, PM16 is also turned on, thus turning off PM17, PM14, and NM2. As in the previous case, as the input decreases the circuit reaches a point at which the current in NM2 increases until it equals the current in PM16. The input voltage at this point is the negative trip point V_{TRP-} To calculate the trip point, the following equations apply:

$$i_{PM16} = \frac{(W/L)_{PM16}}{(W/L)_{PM15}} i_{PM15} \qquad (4.5.9)$$

$$i_{NM2} = i_{PM16} \qquad (4.5.10)$$

$$i_{NM6} = i_{NM5} + i_{NM2} \qquad (4.5.11)$$

Therefore, $i_{PM16} = \frac{i_{NM6}}{1+[\frac{(W/L)_{PM16}}{(W/L)_{PM15}}]} = i_{NM5}$, $i_{NM2} = i_{NM6} - i_{NM5}$ (4.5.12)

to calculate V_{GS}, the trip point is

$$V_{TRP-} = (V_{GS})_{NM5} - (V_{GS})_{NM2} \qquad (4.5.13)$$

4.5.1 DC CIRCUIT

The DC response of the above circuit is shown. Here in this circuit 500mv as reference voltage. So above the reference voltage the Voltage is 1.776v as logic 1.and below the reference voltage the voltage is 14.42uv as logic 0.

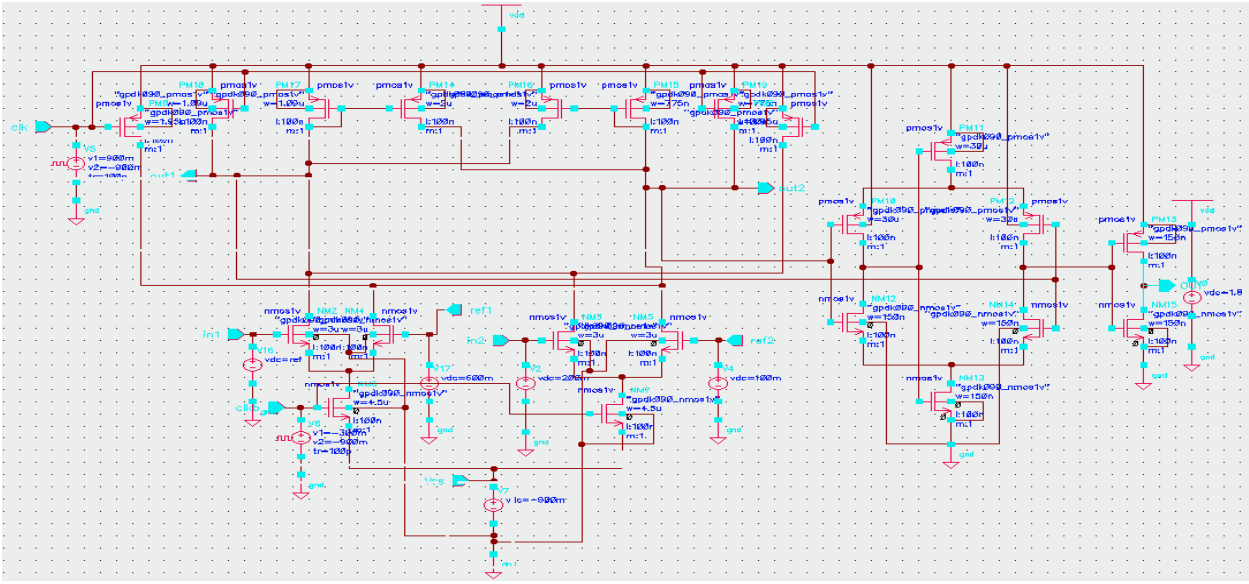


Fig. 4.13 DC Circuit for dynamic comparator PMOS as switch

DC WAVEFORM:-

The DC wave form is shown .In this circuit the reference voltage is 500mV. So tripping should occur at the 500mV.

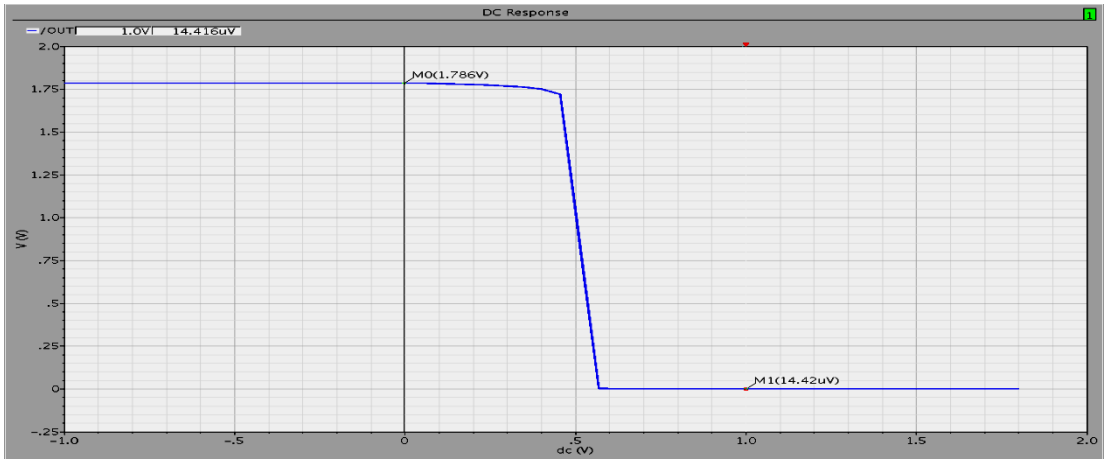


Fig. 4.14 DC Waveform for dynamic comparator PMOS as switch

4.5.2 OFFSET CIRCUIT:-

The offset Voltages are Calculated as shown in Fig.8.Here Zero DC voltages are connected to inputs .The Waveform of the offset Voltage are shown.

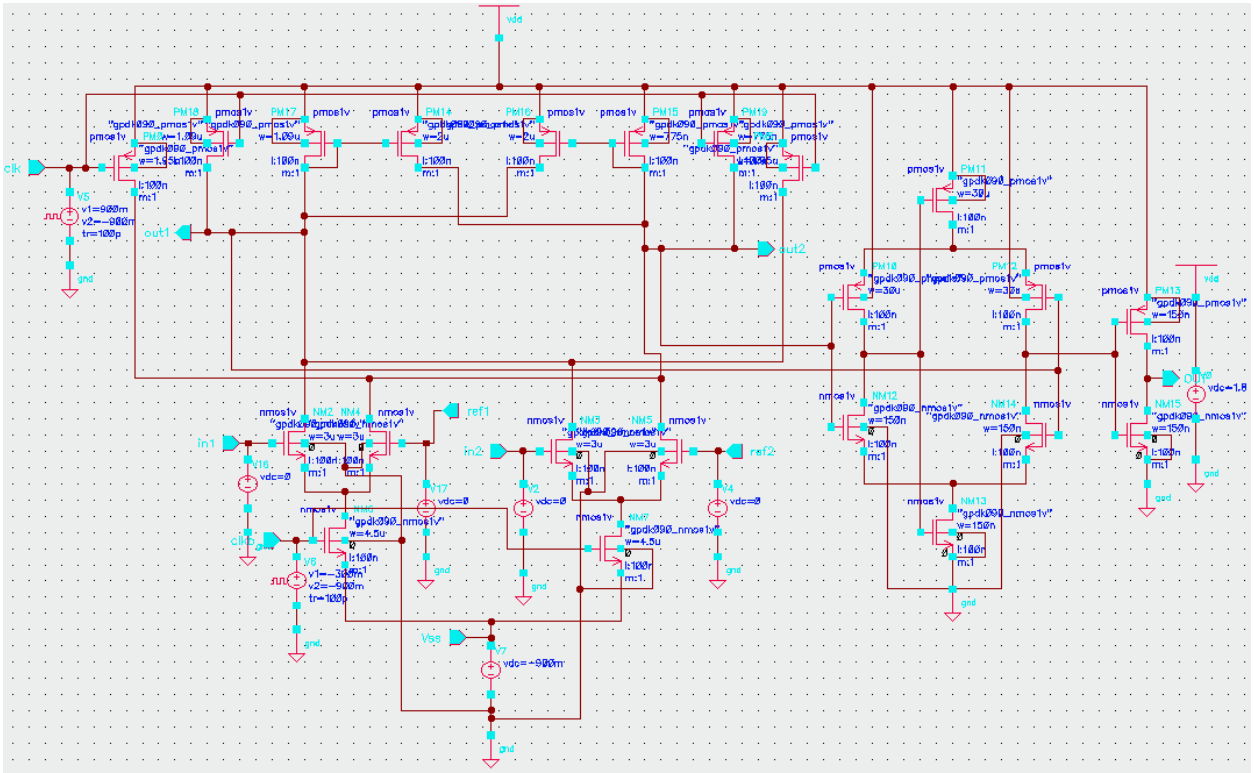


Fig. 4.15 Offset Circuit for dynamic comparator PMOS as switch

OFFSET WAVEFORM:-

Offset voltage is nothing but distance between the origin and the output. Here the input voltage is sweeping from -1V to 1.8V.The offset circuit the offset voltage is 18.07mV.

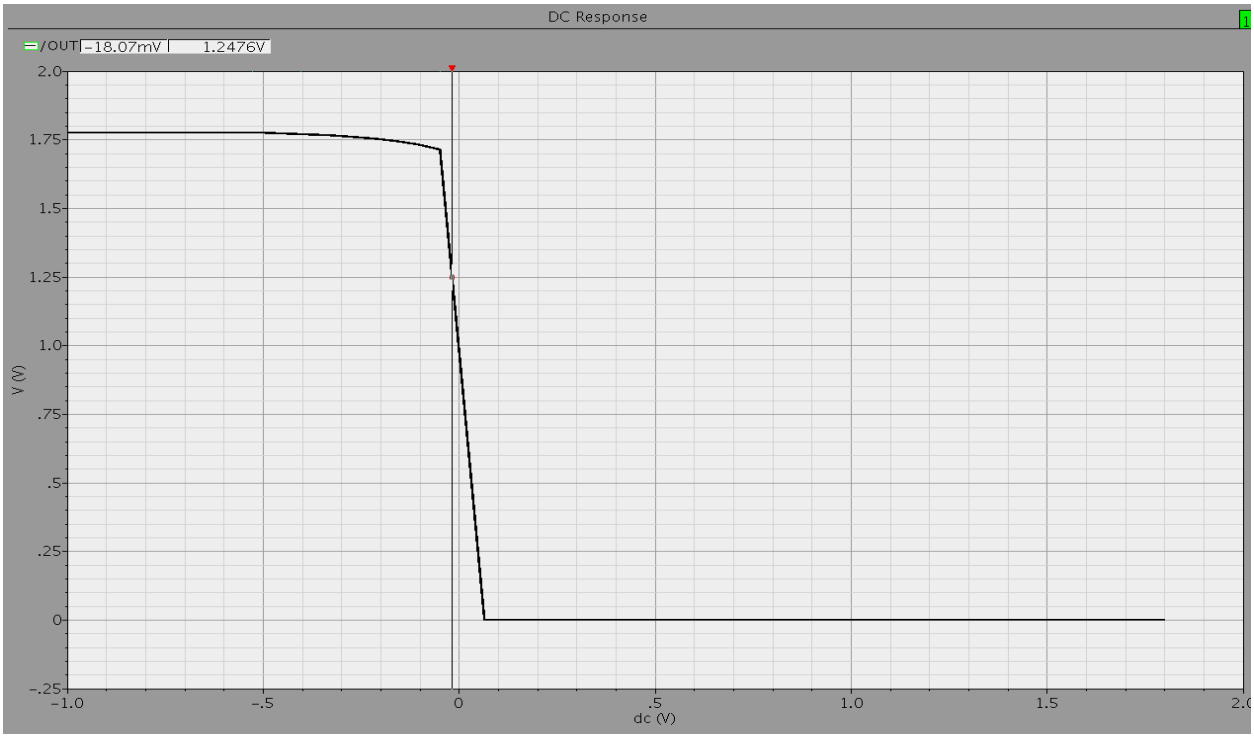


Fig. 4.16 Offset Waveform for dynamic comparator PMOS as switch

4.5.3 Transient circuit:-

This is the circuit for calculating the delay of the Comparator. So for calculating the delay of the Comparator the Transient Analysis is. Here 1.8v as input pulse given to the one input of the Dynamic Comparator using positive feedback. And 500mv as reference Voltage. The output waveforms of the circuit are shown and calculated the Delay ,Speed and Power dissipation.

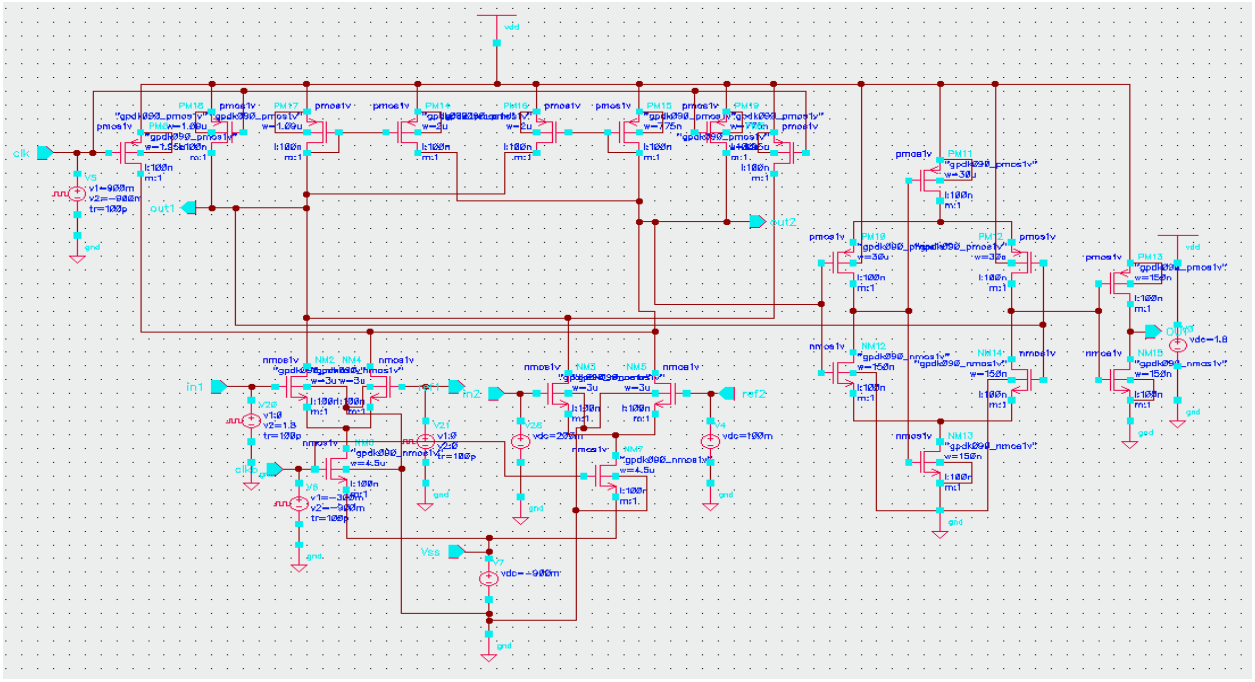


Fig. 4.17 Transient circuit for dynamic comparator PMOS as switch

Transient wave form

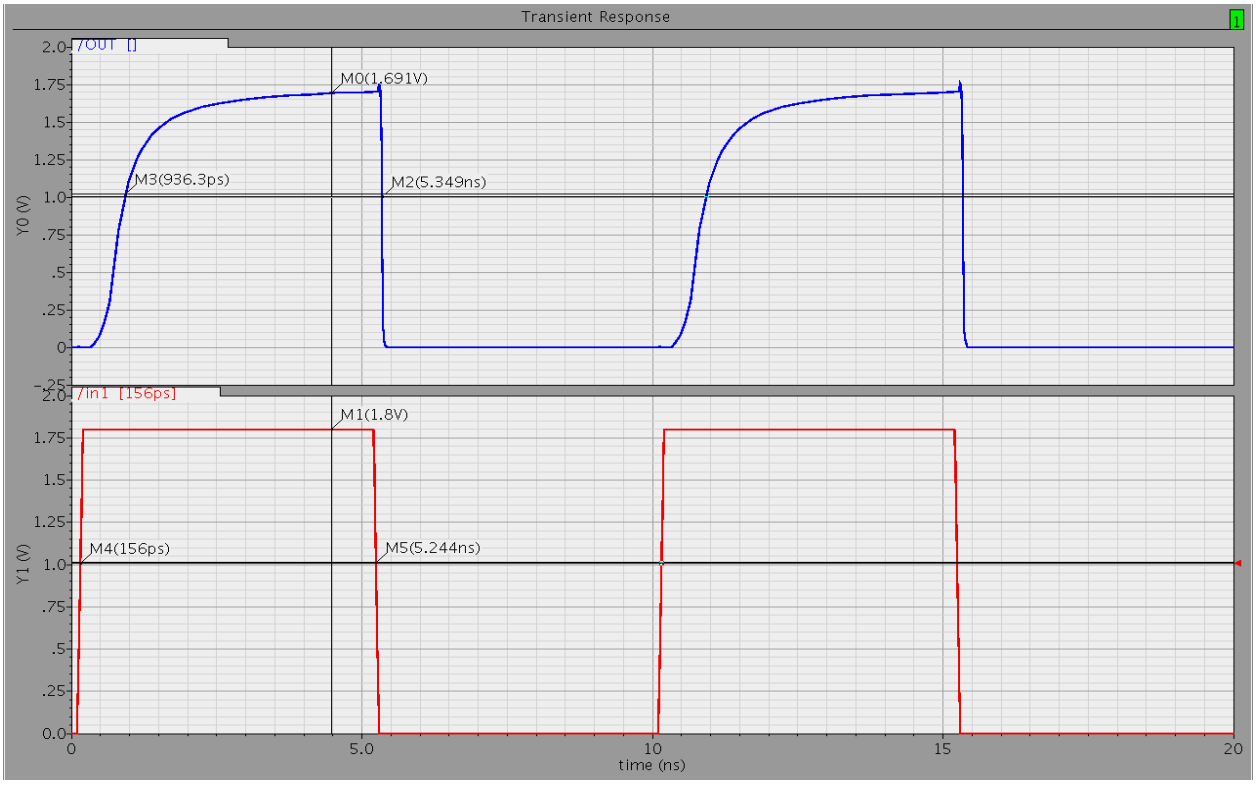


Fig. 4.18 Transient wave form for dynamic comparator PMOS as switch

The rise time and fall time of input and output waveforms are are calculated for Delay and Speed.

4.6 Summary of Results

Calculation for Delay and speed for Dynamic comparator using positive feedback

Vir = 156ps Vif = 5.244ns

Vor = 936.3ps Vof = 5.349ns

Delay = 0.78ns+ 0.105ns /2 =0.4425ns

Speed = 2.259GHz

Power Dissipation= 2.77mw

After post layout simulation calculation for Delay and speed for Dynamic comparator using positive feedback with PMOS as a switch

Vir = 156ps Vif =5.243ns

Vor = 758.3ps Vof =5.352ns

Delay = 0.6023ns+0.109ns/2 = 0.3556ns

Speed = 2.812 MHz

Power Dissipation = 2.564mw

Area = 226.134um^2

Table 4.1 Comparison of different comparators

No	**Comparator name**	**V_{OL}**	**V_{OH}**	**Offset voltage**	**Delay**	**Speed**	**Power Dissipation**
1	Pre-amplifier based Comparator	9.25mV	1.796v	186mV	0.0935ns	10.69GHz	0.0922mW
2	Differential Comparator	9.252mV	1.776v	208.8mV	0.476ns	2.1GHz	0.34mW
3	Dynamic Comparator	14.39µV	1.779v	48.32mV	0.383ns	1.83GHz	4.14mW
4	Dynamic Comparator Using Positive feedback	15.16µV	1.776v	30.67mV	0.428ns	2.33GHz	2.47mW
5	Dynamic Comparator using Positive feedback PMOS as a switch	14.426µV	1.786v	18.07mV	0.442ns	2.259GHz	2.77mW

Table 4.2 Comparison Results after post layout simulation :-

No	**Comparator Name**	**Delay**	**Speed**	**Power Dissipation**	**Area**
1	Pre-amplifier based Comparator	0.168ns	5.952GHz	0.0924mW	91.96um^2
2	Differential Comparator	0.54ns	1.09GHz	0.338mW	213.35um^2
3	Dynamic Comparator	0.46ns	2.16GHz	3.543mW	232.35um^2
4	Dynamic Comparator Using Positive feedback	0.435ns	2.28GHz	2.297mW	226.134um^2
5	Dynamic Comparator using Positive feedback PMOS as a switch	0.3556ns	2.812GHz	2.564mW	216.47um^2

Table 4.3 Hysteresis Comparison of Dynamic comparators

NO	COMPARATOR	V_{trp+}	V_{trp-}	V_{HYS}
1	Dynamic comparator	544.2mV	-533.921mV	1.077V
2	Dynamic comparator using positive feedback	280mV	-280mV	0.56mV
3	Dynamic comparator using positive feedback PMOS as a switch	357.57mV	-357.7mV	0.7145mV

4.7 Experiments and Simulation Results:

The performance of the dynamic comparator topologies was verified and compared by GPDK 90 nm–only MOS transistors is used. The Dynamic comparators occupying approximately same area .The one of the input voltage is sweeping from -1v to 1.8v.another input voltage is 200mv.and the (Vref)reference voltage is 500mv.The supply voltage is 1.8v.To reduce the offset voltage minimum length of MOSFETS are set to 100nm.

In table 1 the performance of Pre amplifier based comparator ,Differential comparator ,Dynamic comparator, Dynamic comparator using positive feedback, Dynamic comparator using positive feedback PMOS as a switch are summarized. In the preamplifier based comparator, Differential Dynamic comparator the offset voltage is more than all the comparators. And power dissipation is less and for the dynamic comparators the offset voltage is less Power dissipation is nearly in mill volts. The offset voltage of Preamplifier based comparator is 186mV.Differential comparator is 208mV.Dynamic comparator is 48.32mV.Dynamic comparator using positive feedback is 30.67mV. Dynamic comparator using positive feedback PMOS as a switch is 18.07mV.De;ay of the Preamplifier comparator is 0.0935ns. Delay of the Differential Dynamic comparator is 0.476ns. Delay of the Dynamic comparator is 0.383ns. Delay of the Dynamic comparator using positive feedback is 0.428 ns .Delay of the Dynamic comparator using positive feedback PMOS as a switch is 0.44ns.The delay of the Dynamic comparators are almost same.

And the power dissipation of the dynamic comparator is 4.14mW.and for the Dynamic comparator using positive feedback is 2.77mW which is nearly reduces to half.

In table 2, the results are after post layout simulation. The delay, speed, Area, Power dissipation are summarized. In table 3 Hysteresis band ,tripping point voltages are summarized. The advantage of the Dynamic comparator using positive feedback is the power dissipation was reduce from4.14mV.to 2.47mV.Delay of the Dynamic comparator is 0.4618ns. Delay of the Dynamic comparator using positive feedback is 0.435ns. Delay of the Dynamic comparator using positive feedback PMOS as a switch is 0.3356ns .so the Dynamic comparator using positive feedback is faster than the Dynamic comparator.

4.8 Conclusion:

Dynamic Comparators are simulated in GPDK 90 nm at 1.8 Supply Voltage. The simulation results shows that the offset voltages are reduced. The offset voltages of Dynamic comparator, Dynamic comparator using positive feedback, Dynamic comparator using positive feedback PMOS as a switch are 48.32 mV,30.67mV,18.07mV respectively. The power dissipation Dynamic comparator, Dynamic comparator using positive feedback, Dynamic comparator using positive feedback PMOS as a switch 4.14mW,3.017mW,2.77mW.

Chapter 5

Conclusion and Future Scope

5.1 Conclusion:

A new dynamic comparator using positive feedback was proposed for high speed, low offset, low power dissipation targeted for ADC application. In the new design, inputs were reconfigured from the typical structure along with a use of restricted clock for the tail current. The proposed structure shows significantly low power dissipation, high speed, low noise low offset compared to the existing typical 'Dynamic comparator'. Reset of the input transistor drain nodes and use of buffers at the output nodes can further reduce the offset. The modifications made to the typical differential pair dynamic comparator can easily reduce the overall offset to only few milli-volts as compared to hundreds of milli volts. With the positive feedback Dynamic comparator width is reduced to the mV range with the 100 MHz clock. The hysteresis band found in this positive feedback Dynamic comparator is reduced to half compared to typical Dynamic Comparators.

5.2 Scope for future work:

From simulation results shows that Dynamic comparators gives less offset voltage, low noise ,low power dissipation compared to conventional comparators. In the future by using Auto zeroing techniques one can reduce the offset voltage, power consumption, Hysteresis band, noise response. By decreasing the number of transistors one can reduce the Area, Power dissipation. And also by reducing the size of each transistor one can get less power dissipation, high speed, matching accuracy

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2. L. Sumanen, M. Waltari, K. Halonen, "A Mismatch Insensitive CMOS Dynamic Comparator for Pipeline A/D Converters" IEEE ICECS, vol.1, pp. 32-35, Dec. 2000.

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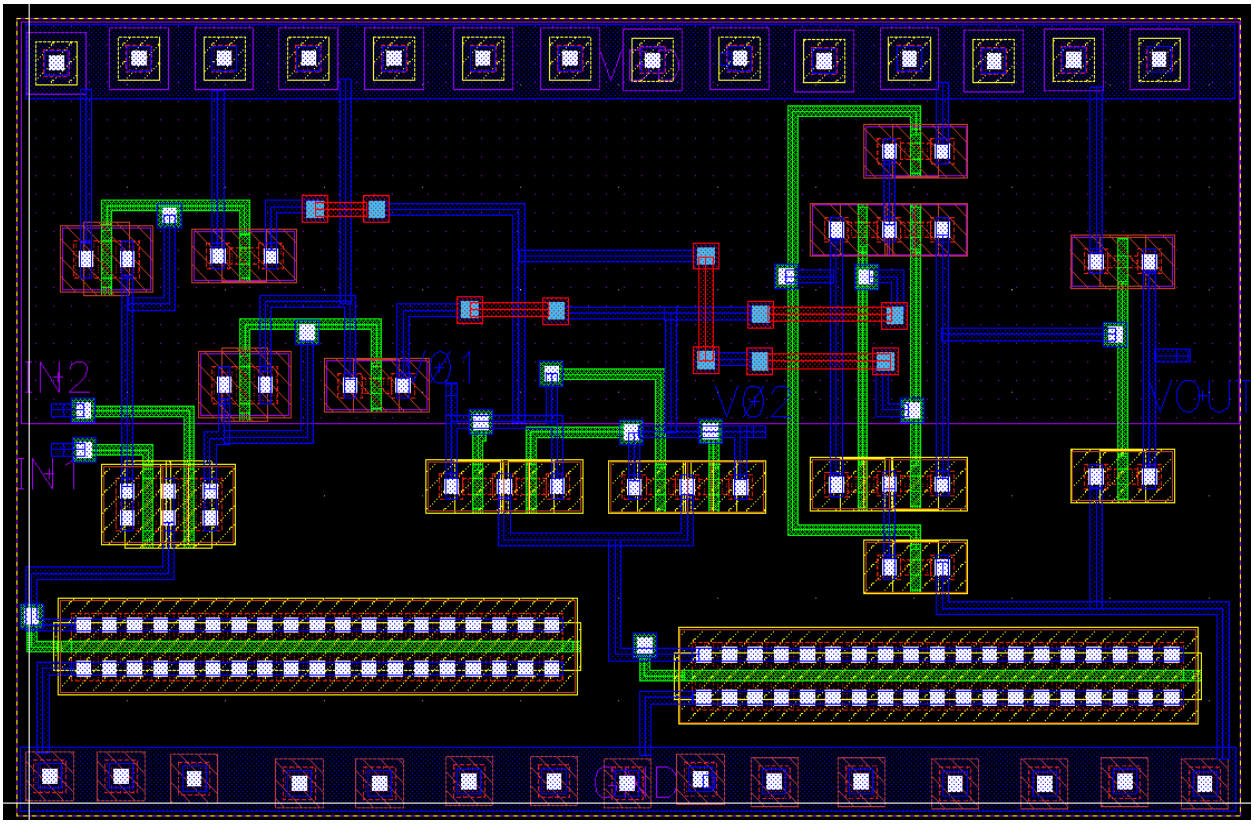
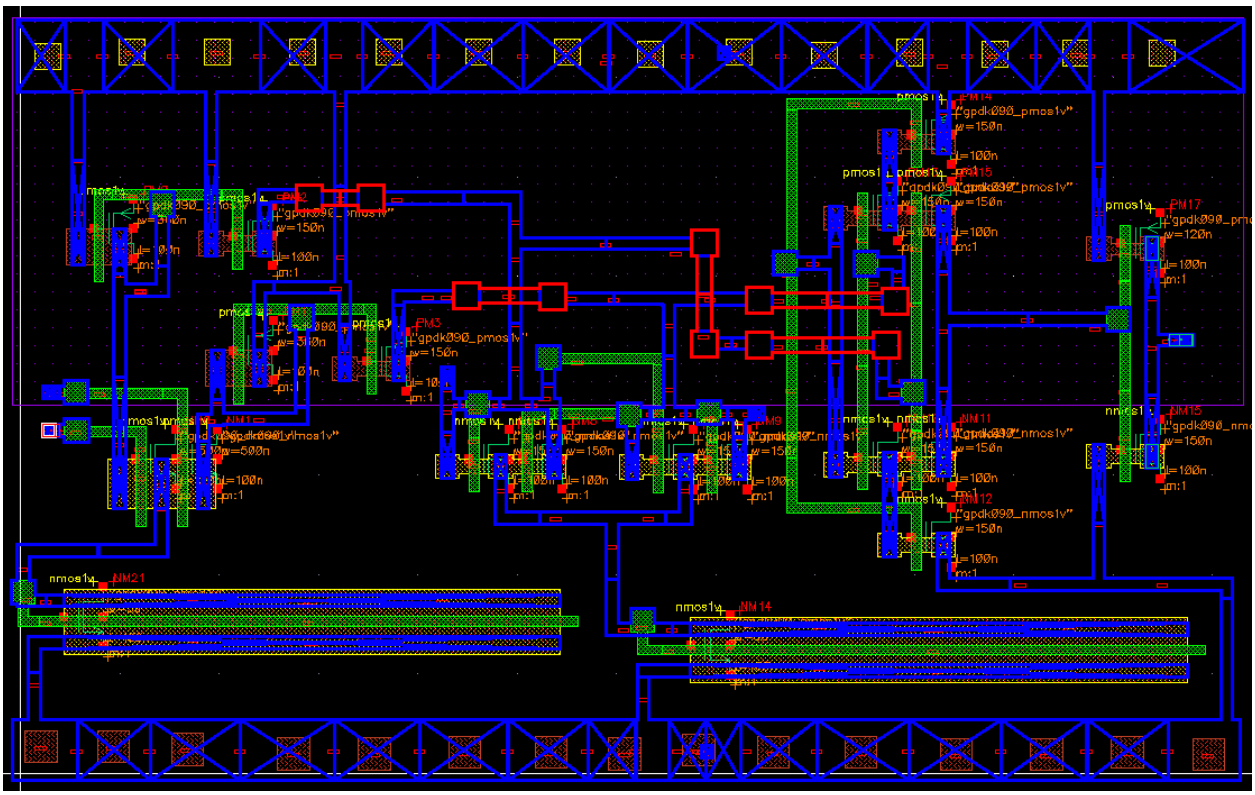
Appendix

Layout for Pre-amplifier based comparator

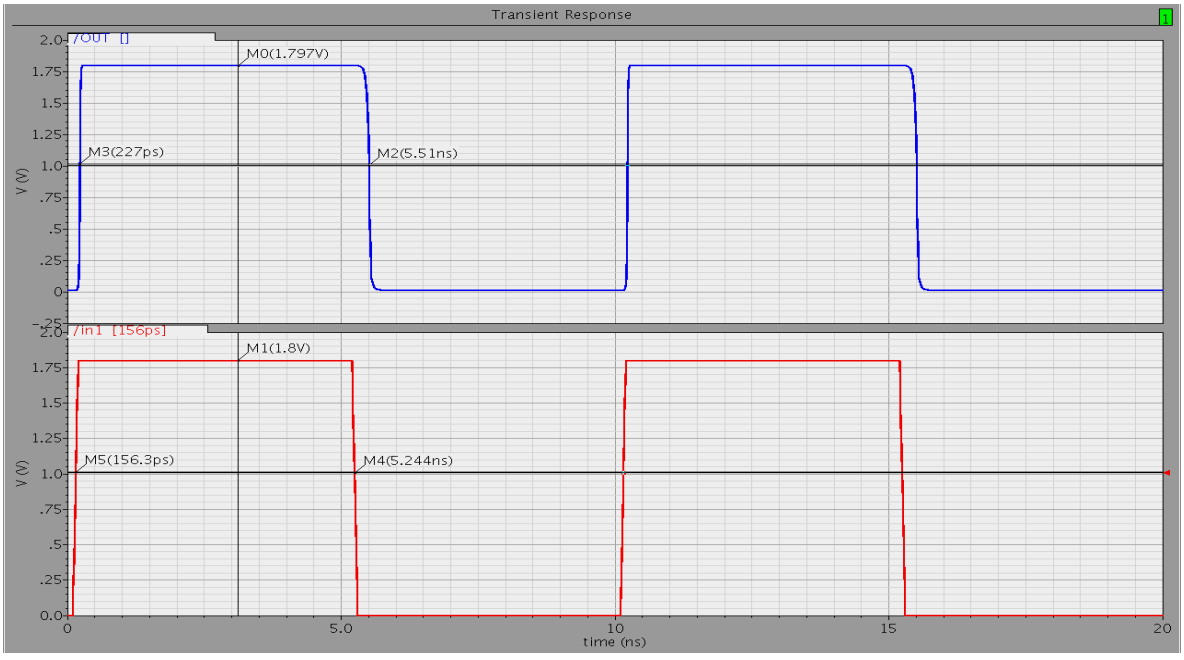


Layout vs Schematic for Pre-amplifier based comparator

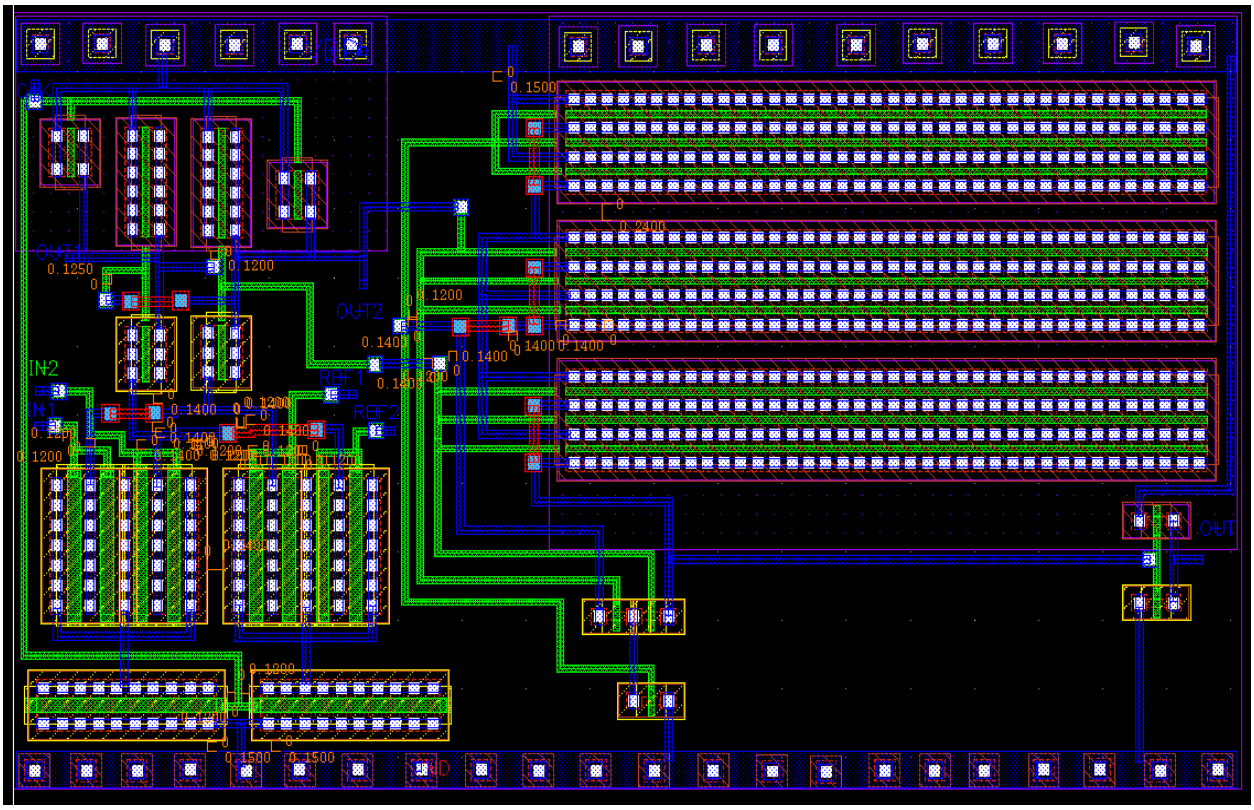
Post layout Simulation for Pre-amplifier based comparator



Transient wave form after post layout simulation:-

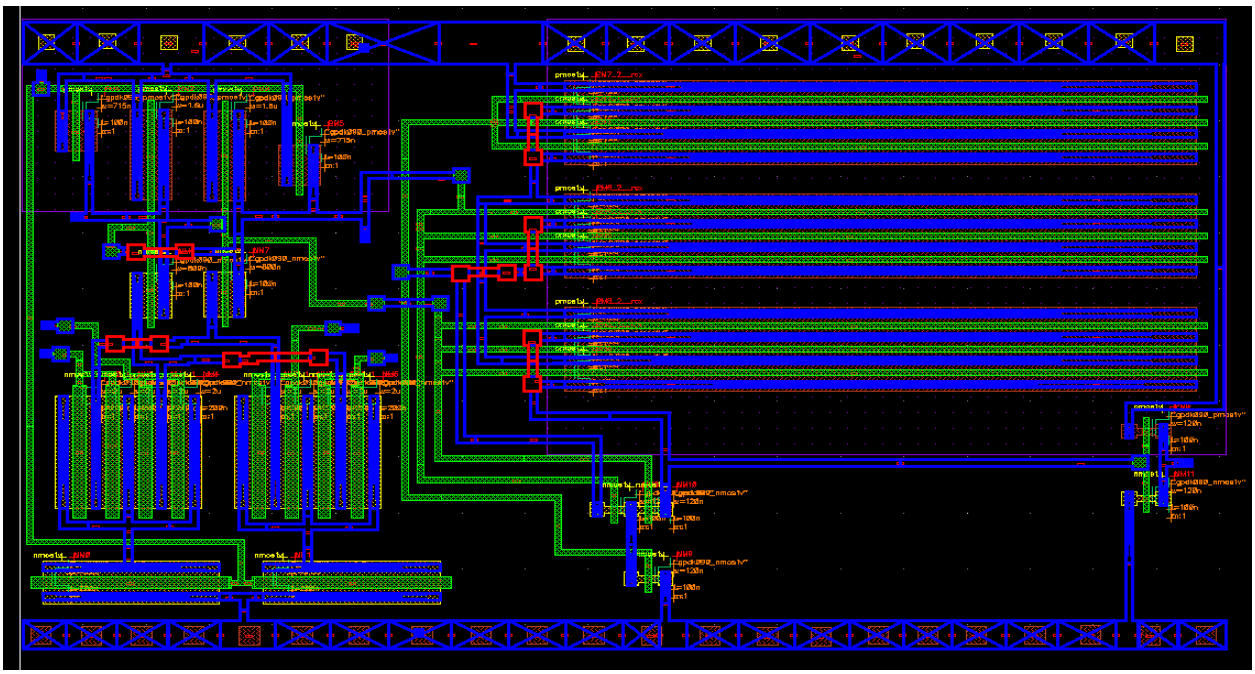


LAYOUT for Differential Dynamic Comparator

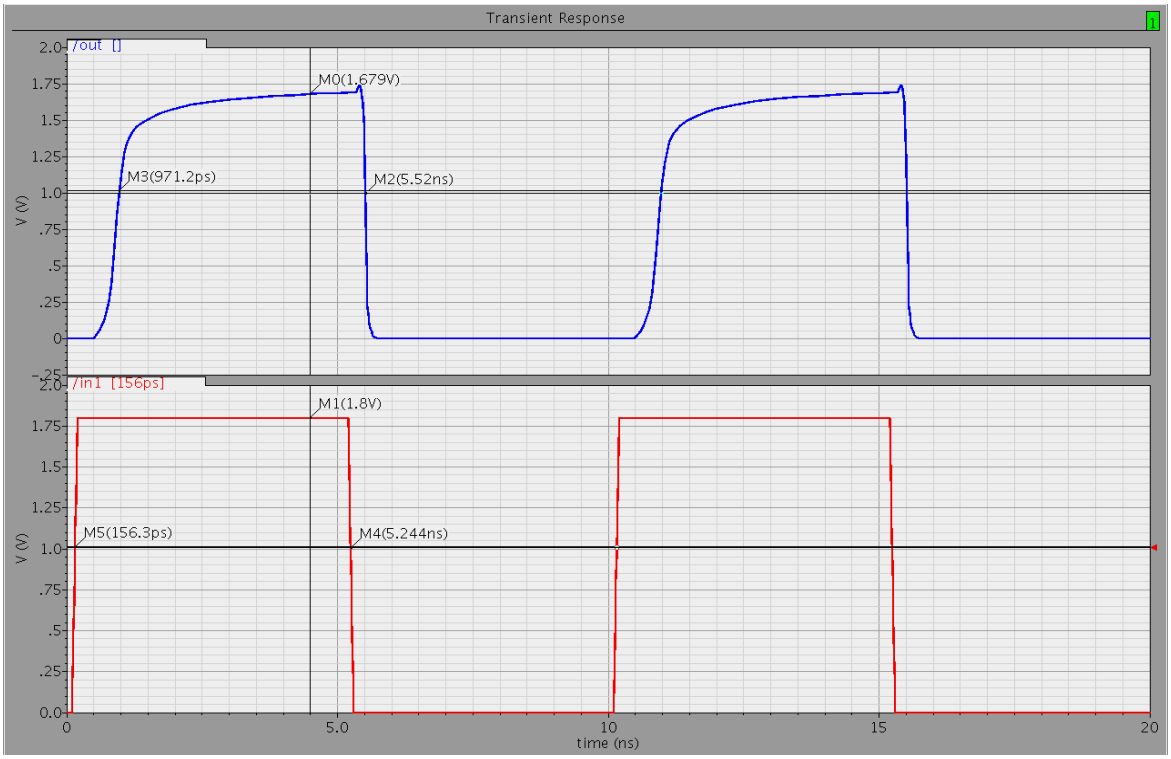


Layout vs Schematic for Differential Dynamic Comparator

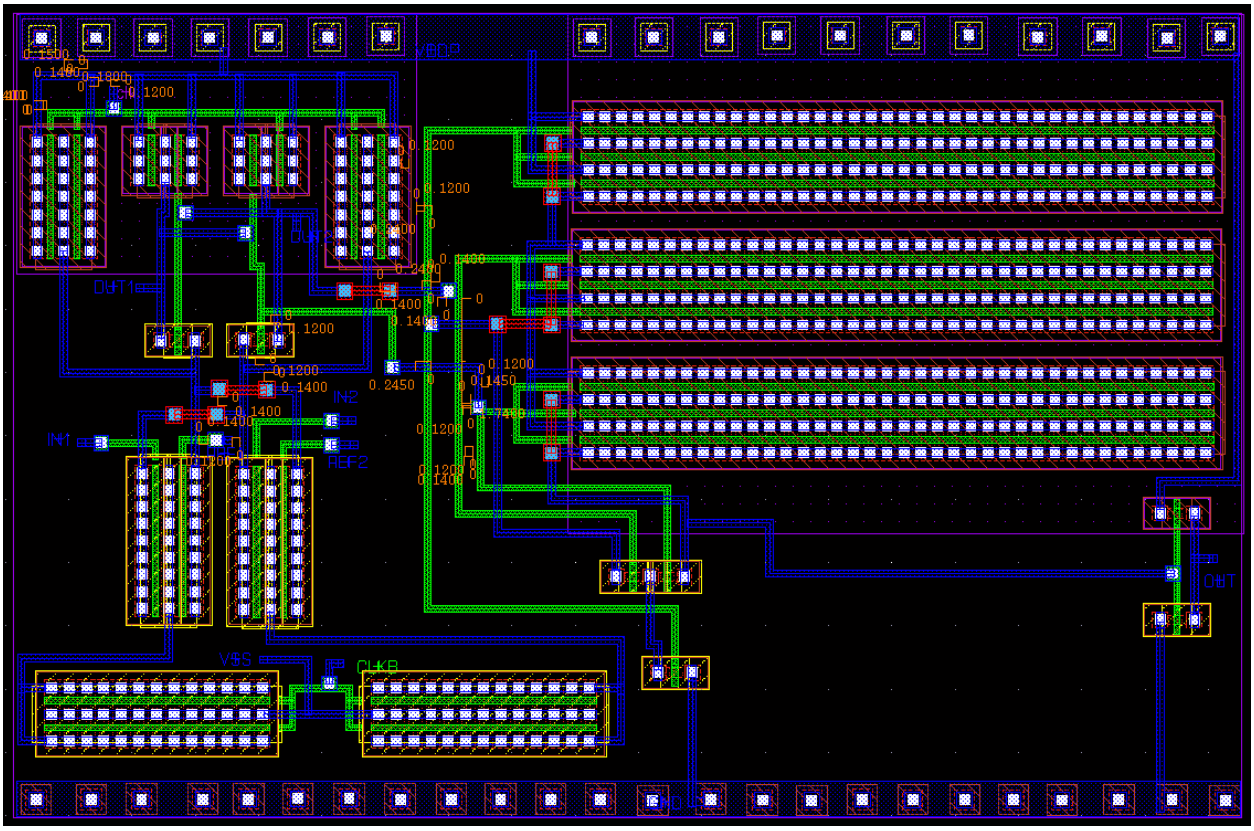
Post layout Simulation for Differential Dynamic Comparator



Transient wave form after post layout simulation:-

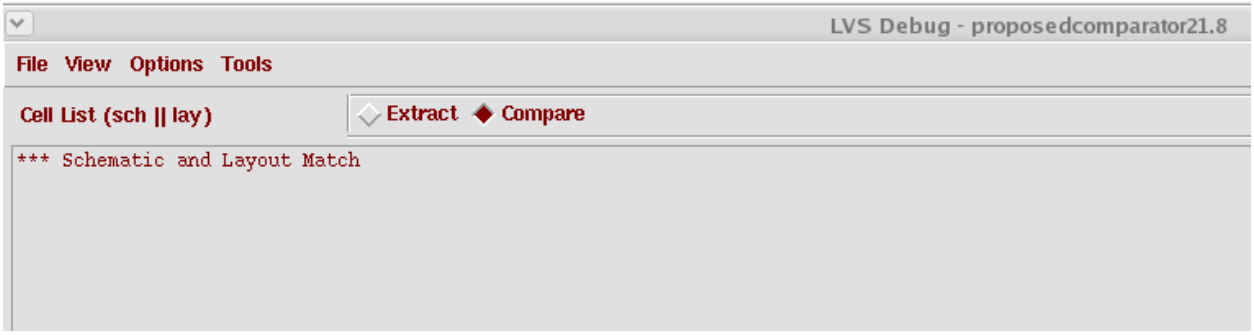


Layout for Dynamic Comparator

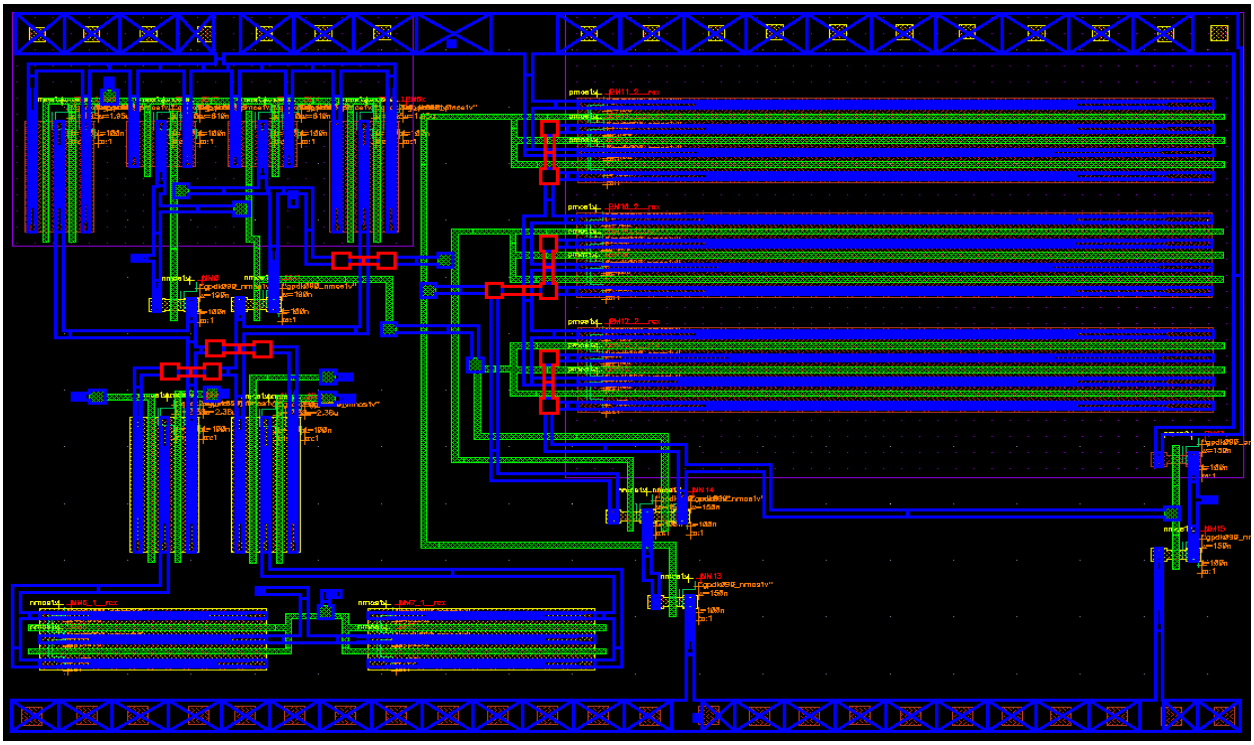


Layout vs Schematic for Dynamic Comparator

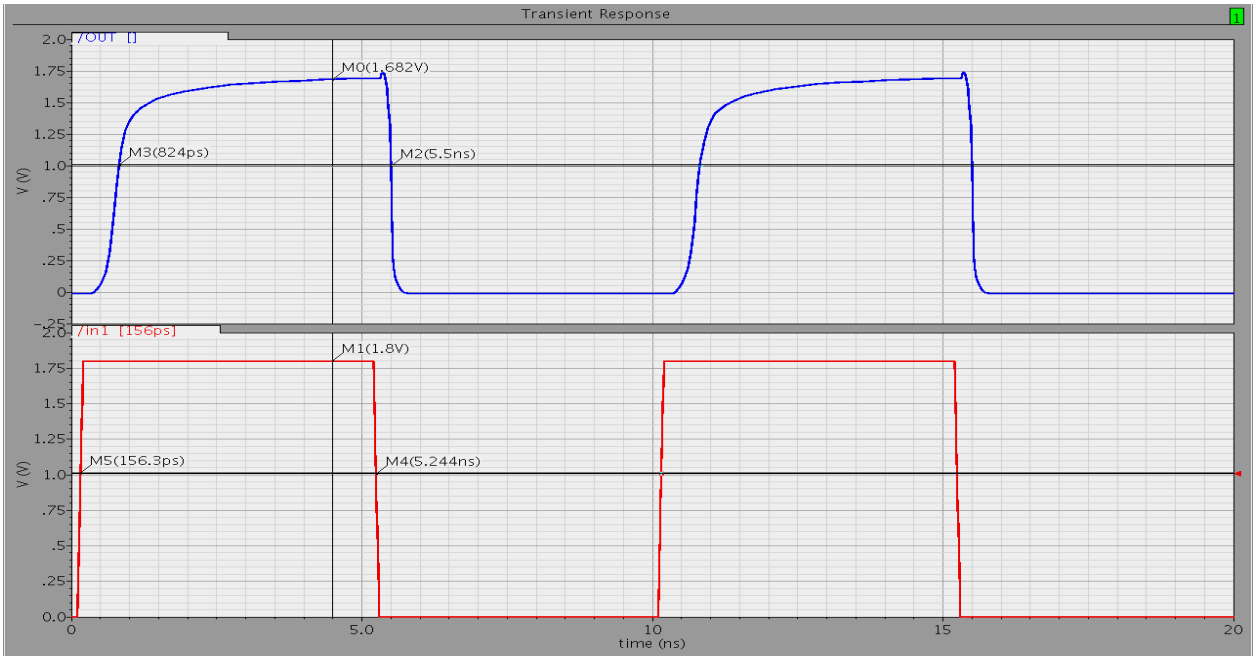
This is the output of the LVS(layout vs Schematic) that shows Schematic and Layout Match



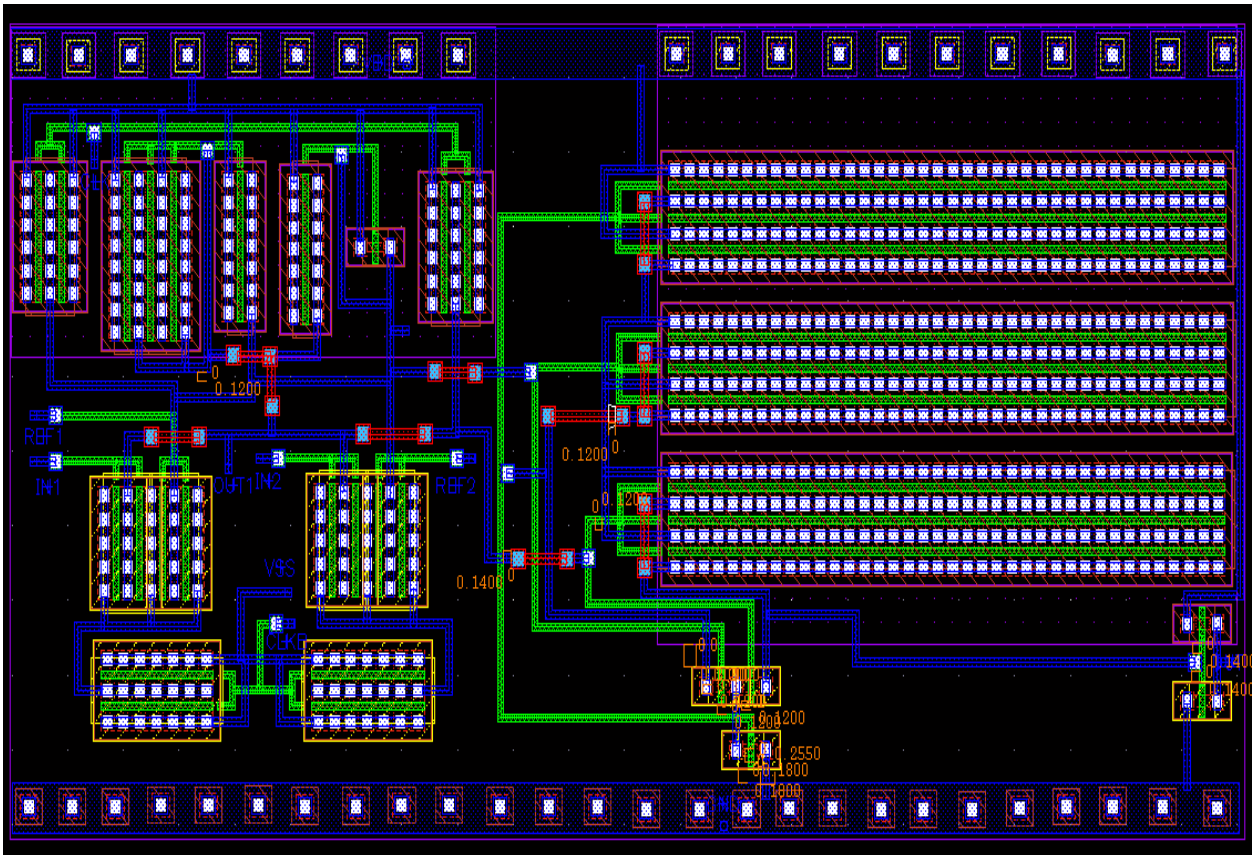
Post layout Simulation for Dynamic Comparator



Transient wave form after post layout simulation:-

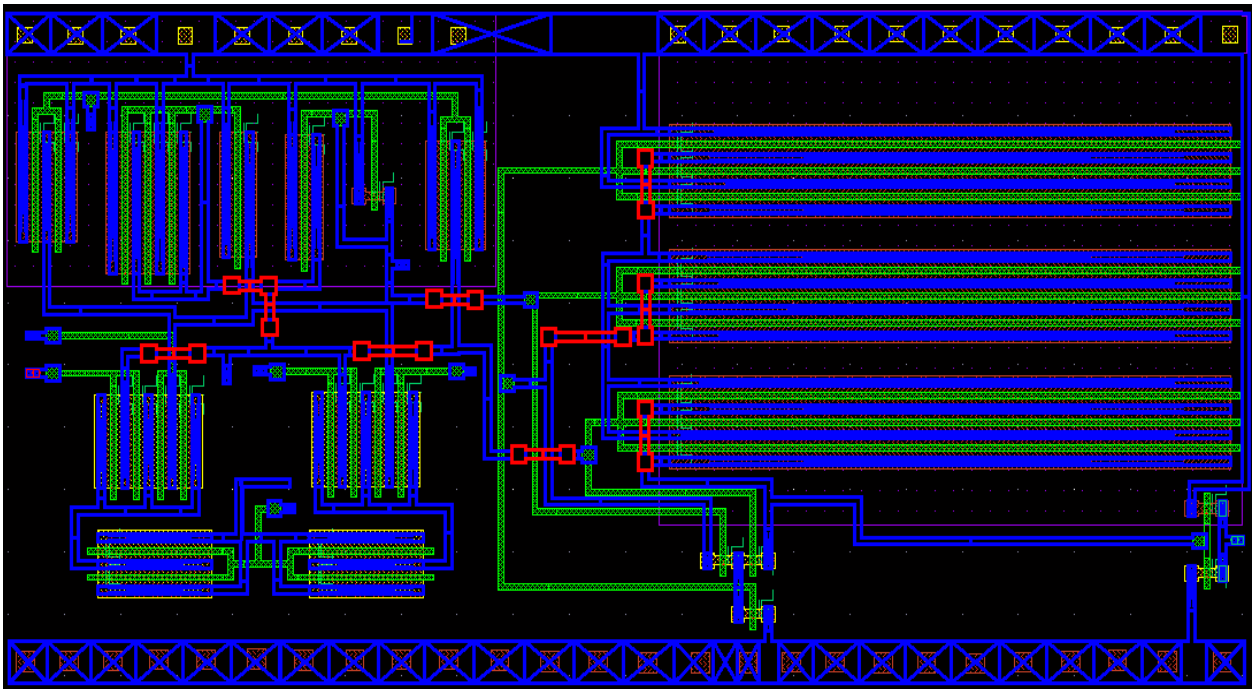


Layout for dynamic comparator using positive feedback

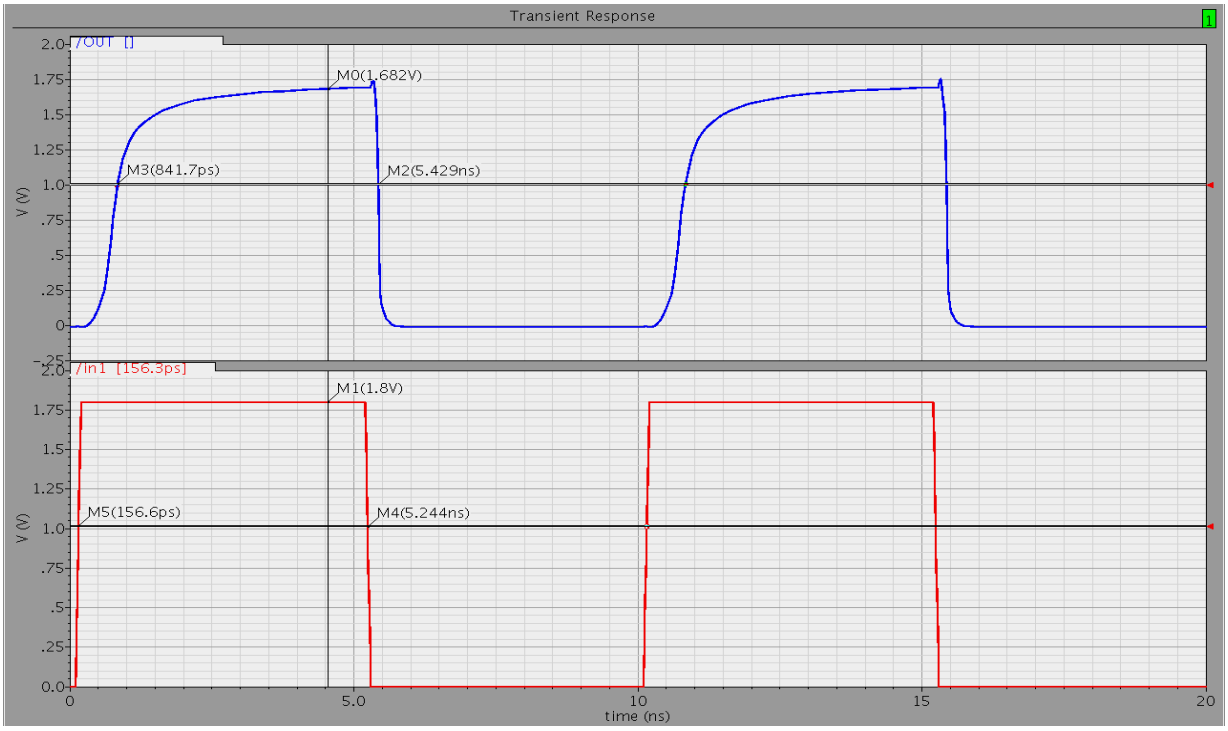


Layout vs Schematic for dynamic comparator using positive feedback

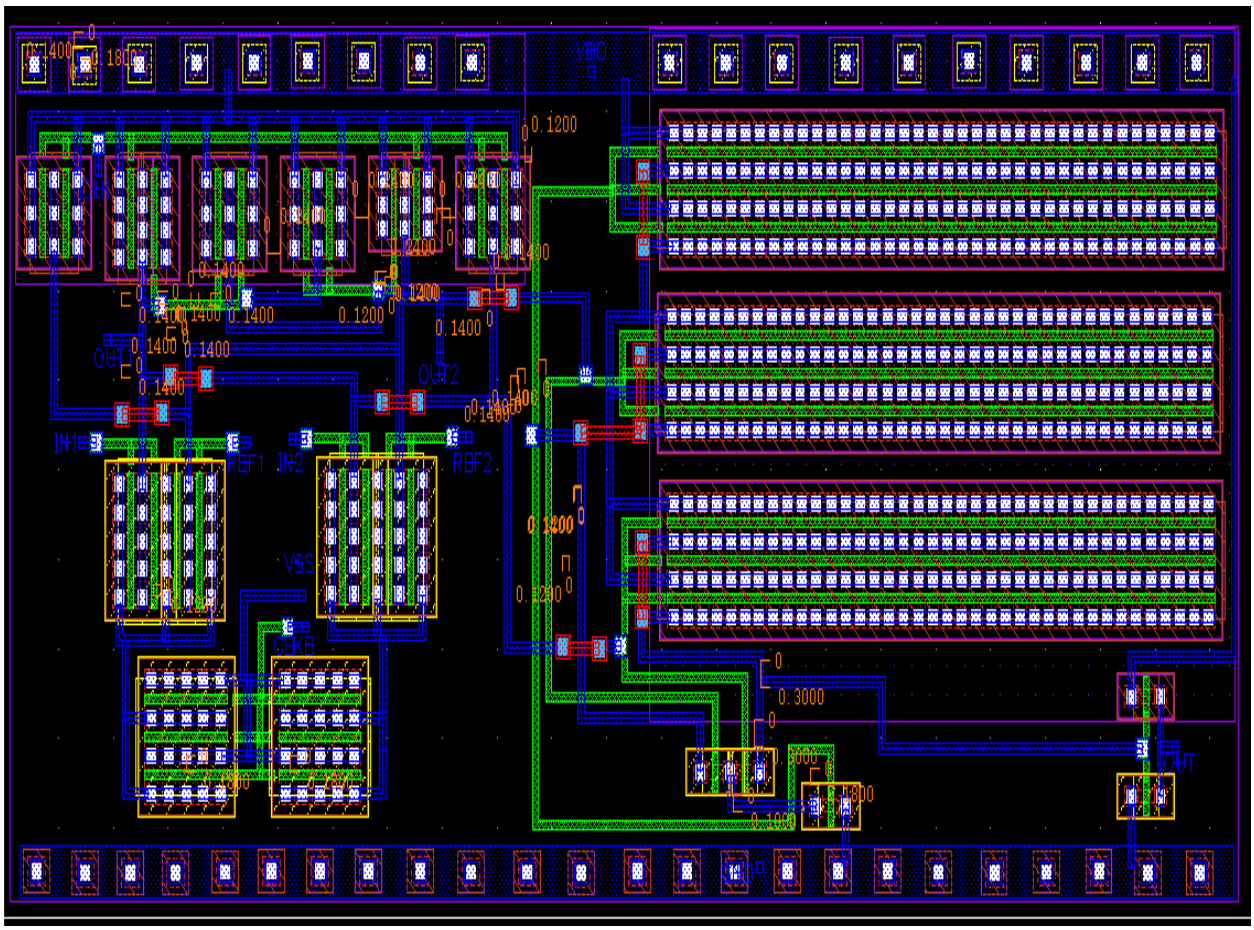
Post layout Simulation for dynamic comparator using positive feedback



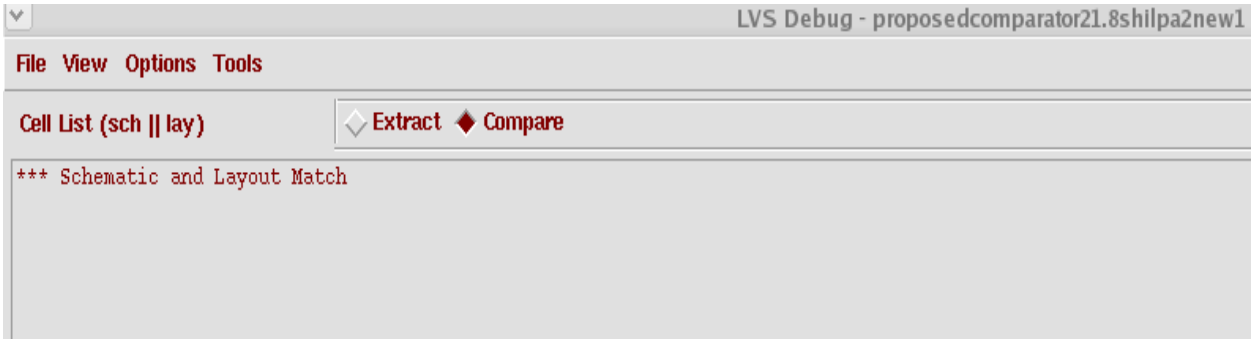
Transient wave form after post layout simulation:-



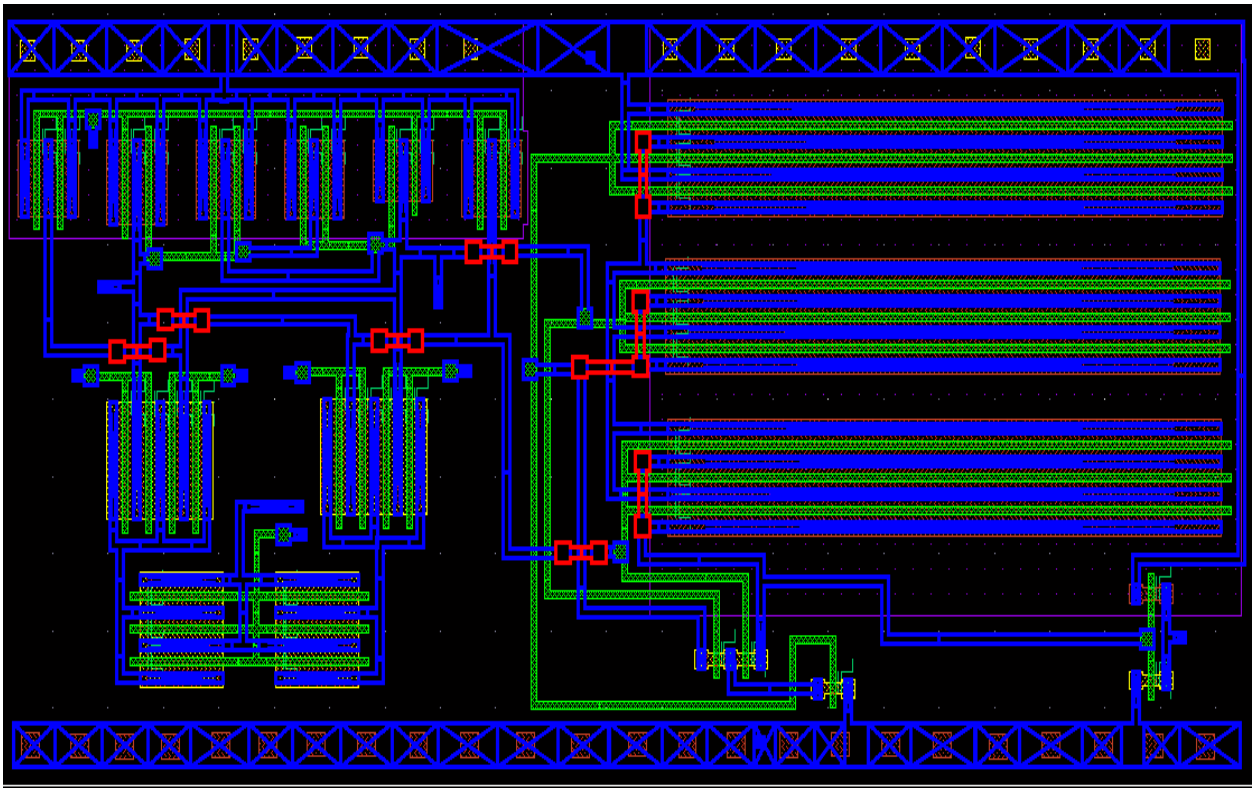
Layout for dynamic comparator PMOS as switch



Layout vs Schematic for dynamic comparator PMOS as switch



Post layout simulation for dynamic comparator PMOS as switch



Transient wave form after post layout simulation:-