DESIGN OF PHASE LOCKED LOOP

A THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF

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CERTIFICATE

This is to certify that the thesis entitled, "**Design of phase locked loop**" submitted by **Subrat Dash** and **Santanu Kumar Bahali** in partial fulfillment of the requirements for the award of Bachelor of Technology Degree in Electronics & Communication Department at the National Institute of Technology, Rourkela (Deemed University) is an authentic work carried out by them under my supervision.

And to the best of my knowledge, the matter embodied in the thesis has not been submitted to any other University/Institute for the award of any Degree or Diploma.

Prof. Debiprasad Priyabrata Acharya

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I would also like to convey my sincerest gratitude and indebtedness to all other faculty members and staff of Department of Electronics & Communication Engineering, NIT Rourkela, who bestowed their great effort and guidance at appropriate times without which it would have been very difficult on my project work.

An assemblage of this nature could never have been attempted with our reference to and inspiration from the works of others whose details are mentioned in references section. I acknowledge my indebtedness to all of them

My parents and brothers mean all to me. They left me on my way giving me great amount of freedom which has been crucial in developing an open attitude. Their love pushed me to do my best and that I think is take way I repay them.

Finally, I think the Almighty who tells me to travel a difficult road which always ends in a better me.

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Abstract

In the optical communication in a backbone infra structure, flexibility means, for example, programmable bitrates requiring a PLL with robust operation over a wide range of frequency range. A wide range PLL could be used by different protocols and applications so that we maximize the reusability and reduce time to market.

In this report we try to present an extended frequency CMOS monolithic VCO design. A negative feedback control algorithm is used to automatically adjust the VCO range according to control voltage. Based on this analog feedback control algorithm, the VCO achieves a wide range without any pre-register settings.

Here we discuss about different component of PLL (Phase Lock Loop), mainly on Phase Frequency Detectors and VCO (voltage controlled oscillator). Here we proposed different architecture of Phase frequency detectors and also of VCOs and designed many architecture in mentor graphics.

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1. Introduction

1.1 Phase locked loop

High-performance digital systems use clocks to sequence operations and synchronize between functional units and between ICs. Clock frequencies and data rates have been increasing with each generation of processing technology and processor architecture. Within these digital systems, well-timed clocks are generated with phase-locked loops (PLLs) and then distributed on-chip with clock buffers. The rapid increase of the systems' clock frequency poses challenges in generating and distributing the clock with low uncertainty and low power. This research presents innovative techniques at both system and circuit levels that minimize the clock timing uncertainty with minimum power and area overhead.

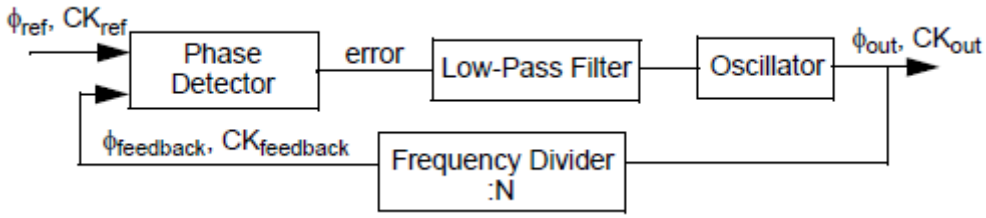
With the exponential growth of no of internet nodes, the volume of data transported by its backbone continues to rise rapidly. Among the available transmission media, optical fibers have highest bandwidth with lower cost, serving an attractive solution for internet backbone. However, the electronic interface proves to be the bottleneck in designing high speed digital system. This fact, combined with the ever-shrinking time to market, indicates that designs based on flexible modules and macro cells have great advantages. In the optical communication in a backbone infra structure, flexibility means, for example, programmable bitrates requiring a PLL with robust operation over a wide range of frequency range. A wide range PLL could be used by different protocols and applications so that we maximize the reusability and reduce time to market.

1.2 PLL Fundamentals

Phase-locked loops (PLLs) generate well-timed on-chip clocks for various applications such as clock-and-data recovery, microprocessor clock generation and frequency synthesizer. The basic concept of phase locking has remained the same since its invention in the 1930s. However, design and implementation of PLLs continue to be challenging as design requirements of a PLL such as clock timing uncertainty, power consumption and area become more stringent. A large part of this research focuses on the design of a PLL for high-performance digital systems.

1.3 PLL Definition

The basic block diagram of a PLL is shown in Figure. A PLL is a closed-loop feedback system that sets fixed phase relationship between its output clock phase and the phase of a reference clock. A PLL tracks the phase changes that are within the bandwidth of the PLL. A PLL also multiplies a low-frequency reference clock, CK_{ref}, to produce a high frequency clock, CK_{out}.

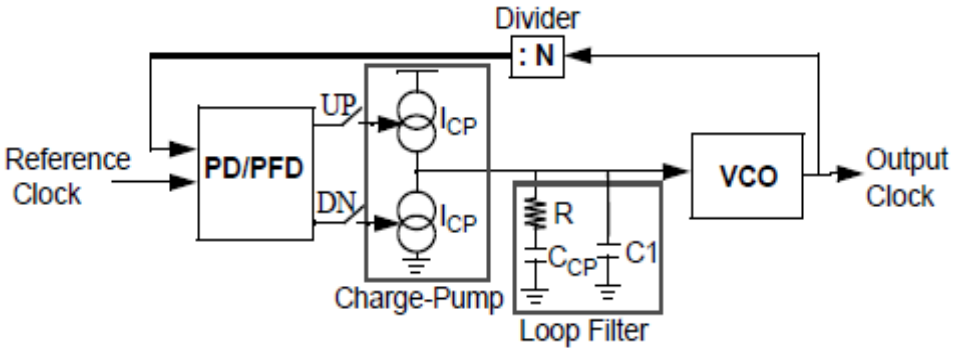


Basic PLL Block Diagram

The basic operation of a PLL is as follows. The phase detector (comparator) produces an error output signal based on the phase difference between the phase of the feedback clock and the phase of the reference clock. Over time, small frequency differences accumulate as an increasing phase error. The difference or error signal is low-pass filtered and drives the oscillator. The filtered error signal acts as a control signal (voltage or current) of the oscillator and adjusts the frequency of oscillation to align ϕ feedback with ϕ ref. The frequency of oscillation is divided down to the feedback clock by a frequency divider. The phase is locked when the feedback clock has a constant phase error and the same frequency as the reference clock. Because the feedback clock is a divided version of the oscillator's clock frequency, the frequency of oscillation is N times the reference clock.

1.4 PLL Component

The block diagram of a charge-pump PLL is shown in Figure. A PLL comprises of several components: (1) phase or phase-frequency detector, (2) charge-pump current, (3) loop filter, (4) voltage-controlled oscillator, and (5) frequency divider. The functioning of each block is briefly described below.



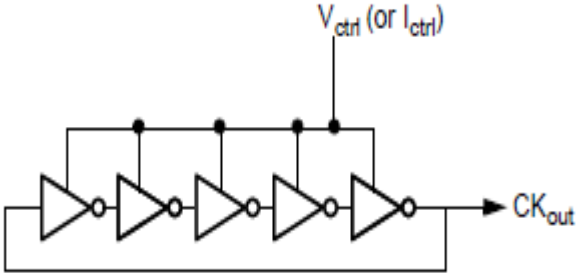
Individual Blocks in PLL Diagram

1.4.1 Voltage Controlled Oscillator

An oscillator is an autonomous system that generates a periodic output without any input. A CMOS ring oscillator shown in Figure is an example of an oscillator. So that the phase of a PLL is adjustable, the frequency of oscillation must be tunable. In the example of an inverter ring oscillator, the frequency could easily be adjusted with controlling the supply (voltage or current) of inverters. The slope of frequency versus control signal curve at the oscillation frequency is called voltage-to-frequency (current-to- frequency) conversion gain, K_{VCO}; $_{VCO}=df_{VCO}/dV_{ctrl}$ evaluated at f_{VCO}. Since phase is the integral of frequency, the output phase of the oscillator is equal to $\int \Phi_{VCO} = K_{VCO}.V_{ctrl}\, dt$. In other words, the VCO in the frequency domain (s-domain), is modeled as

$$\Phi_{VCO}/ V_{ctrl}(s) = K_{VCO}/S;$$

Ideally, for the linear analysis to apply over a large frequency range, K_{VCO}, needs to be relatively constant.



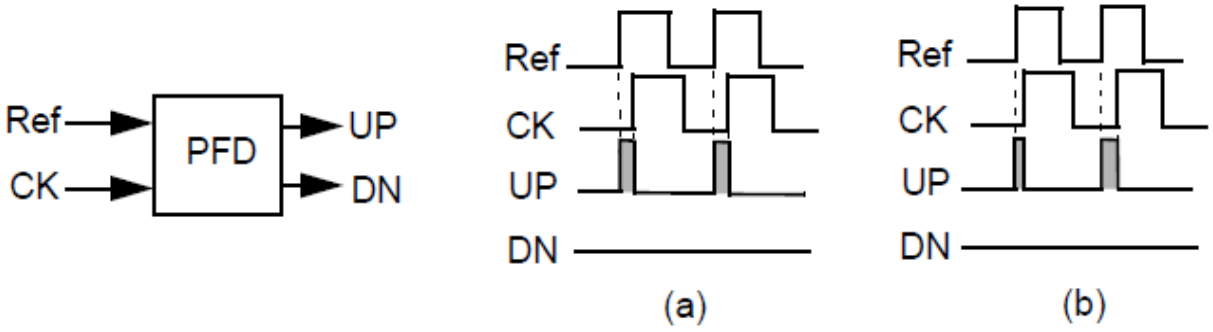
A five Stage Ring Oscillator

1.4.2 Frequency Divider

The PLL reference clock is generated from a crystal. The crystals typically operate from tens to a few hundreds of MHz's On the other hand; VCOs for clocking and parallel link applications operate at a few GHz or even ten GHz. For proper functioning of the phase detector or phase-frequency detector, discussed in the next section, a frequency divider divides down the VCO frequency to the frequency of the reference clock.

1.4.3 Phase Detector

The phase detector (PD) compares the phase difference between two input signals and produces an error signal that is proportional to the phase difference. In the presence of a large frequency difference, a pure phase detector does not always generate the correct direction of phase error. Phase error accumulates rapidly and can oscillate between phase error of $>180^{o}$ and $<180^{o}$ from cycle to cycle. The average phase detector output contains little frequency information and no valuable phase information. Since the phase detector is insensitive to frequency difference at the input, upon start-up when the oscillator's frequency divided by N_1 is far from the reference frequency, the PLL may fail to lock. The problem is known as an inadequate *acquisition range* of the PLL. To remedy the problem, a phase-frequency detector (PFD) is used that can detect both phase and frequency differences. Figure 2.4 conceptually demonstrates the operation of a PFD for two cases: (a) the two input signals have the same frequency, and (b) one input has higher frequency than another input. In both cases, the DC contents of PFD's outputs, *UP* and *DN*, provide information about phase or frequency difference



Operation of a PFD: (a) $f_{ref}=f_{CK}$, $\phi_{ref}\#\phi_{Ck}$ and (b) $f_{ref}>f_{CK}$

1.4.4 Charge pump and loop filter

The charge-pump circuit comprises of two switches that are driven with *UP* and *DN* outputs of PFD as shown in Figure 2.2. The charge-pump injects the charge into or out of the loop filter capacitor (C_{CP}). The combination of charge-pump and C_{CP} is an integrator that generates the average of *UP* (or *DN*) pulses. This average voltage adjusts the frequency of the subsequent oscillator circuit. Since the VCO introduces another integrator, the loop gain of a charge-pump PLL has two poles at origin; thus, the closed loop system is unstable. To stabilize the system, a zero, $\omega_z = 1/RC_{CP}$, is introduced in the loop gain by adding a resistor, R, in series with C_{CP}. The PFD, charge pump and filter are often modeled with a linear continuous-time model. In reality, the PFD acts as a pulse modulator system and drives the charge-pump for the duration of pulse width which is equal to PFD input phase difference, $\Delta\phi$. The actual phase response is not linear because phase is cyclical. Furthermore, the phase information is discrete, sampled at the clock reference frequency.

1.5 Noise and Power Considerations

The primary goal to design a PLL for high-performance digital systems is to generate an output clock with minimum timing uncertainty. The timing uncertainty arises from mismatches in devices and noise sources present in the system. Device mismatches causes a static phase shift (or skew) in the PLL output clock from its desired phase. Skew can be minimized with a careful layout and increasing the device size. Skew is generally less critical than jitter because, due to its static nature, the system can compensate for the static errors. Dynamic noise causes a random phase shift (or jitter) in the PLL output clock. The noise sources in a PLL are device electronic noise such as thermal noise or flicker noise and power-supply or substrate noise.

1.6 Band Width of PLL

The bandwidth of a PLL is the measure of the PLL's ability to track the input clock and jitter. The closed loop gain 3-dB frequency of the PLL determined the PLL bandwidth. The bandwidth is approximately the unity gain point for PLL open loop response.

A high bandwidth PLL provides a fast lock time and tracks jitter on the reference clock source, passing it through to the PLL output. A low bandwidth PLL filters out reference clock jitter, but increase lock time.

1.7 Phase Noise and Its Causes

Phase noise is the frequency domain representation of rapid, shot-term random fluctuation in the phase of a wave. The term phase noise is used to describe phase fluctuation due to random frequency fluctuation of a signal. Phase noise can be caused by a number of conditions, but is mostly affected by an oscillator's frequency stability.

The oscillator output is describe by

$$V(t) = V_0 \sin(2*pi*f*t+ph)$$

Where f=oscillator frequency and ph=Phase angle

Its instantaneous frequency = f+ (1/2*pi)*(d pi/d t)

If the instantaneous frequency is same as f then the tern (d ph/d t) is zero so phase noise is zero unless there is a phase noise.

Causes of Phase noise

a. The noise figure of active component such as transistors, integrated circuits, voltage regulator zeners etc.
b. Thermal noise in passive component such as resistors.
c. Flicker noise in active components.
d. Noise process in the oscillator
e. Higher Q crystal will improve lower offset frequencies of phase noise generally less than 100 Hz offset. As the crystal frequency increases the 'Q' of the crystal decreases and the phase noise at lower frequency offset will increases.
f. The crystal has a g-sensitivity that will degrade the phase noise under dynamic vibration conditions.
g. Long-term frequency stability can be affected by a long term drift caused by the crystal and component aging assuming temperature remains same.
h. Frequency Change due to temperature changes can also affect system stability.

2. Architecture of PLL

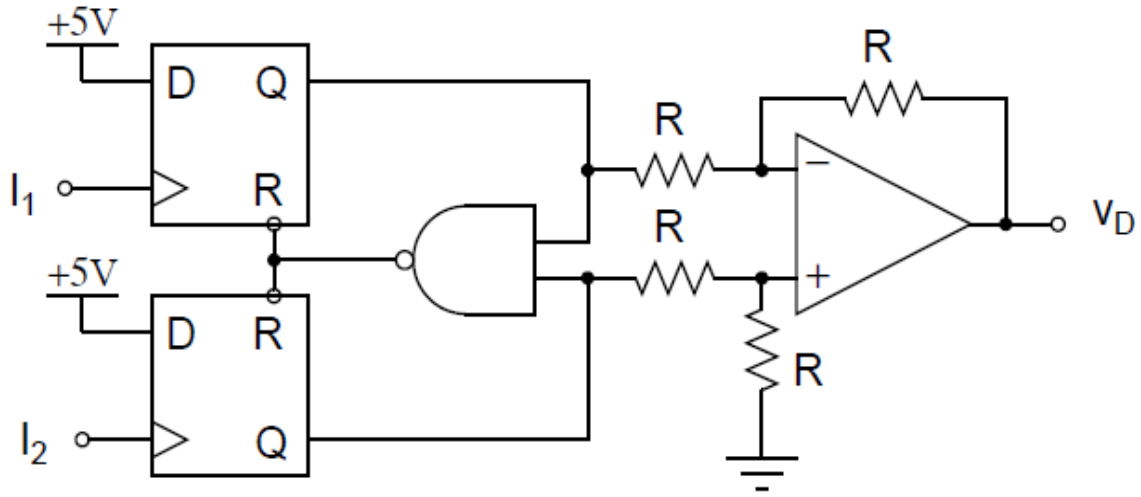
A wide range PLL requires a wider tuning range of VCO. In this paper, a fully integrated CMOS VCO with an extended frequency range is described. In section-II, following a brief overview of conventional architecture for ring type based VCO design; the proposed architecture is described to solve the problems of conventional methods. A negative feedback control algorithm automatically adjusting VCO frequency range is used to extend the frequency range. Also circuits of this wide tuning range VCO are described.

2.1 Phase frequency Detector

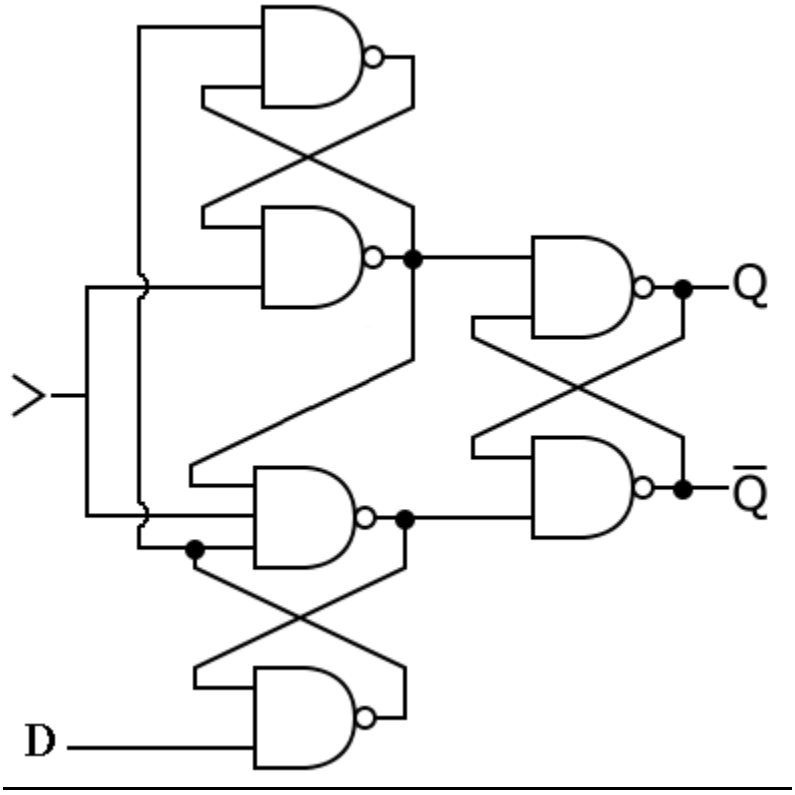
In an analogue mixer a number of different frequencies are generated within the mixer namely the sum of the frequencies and the difference frequency (otherwise known as the beat note) when both input frequencies are the same is the phase difference is zero and the beat note is DC.

Phase detectors are part of a Phase Locked Loop (PLL) and can be either analogue e.g. mixer or digital e.g. D-type flip-flop. When a mixer is used the output consists of the sum and difference frequencies.

Most PLL circuits now use digital phase detectors formed from two D-type flip-flops as shown.



2.1.1 **Edge Triggered D-Flipflop**



2.1.2 **Differentail Amplifier**

A differential amplifier is a type of electronic amplifier that multiplies the difference between two inputs by some constant factor (the differential gain). Many electronic devices use differential amplifiers internally. Given two inputs V_{in}^{+} and V_{in}^{-}, a practical differential amplifier gives an output Vout:

$$V_{\text{out}} = A_{\text{d}}(V_{\text{in}}^{+} - V_{\text{in}}^{-}) + A_{\text{c}}\left(\frac{V_{\text{in}}^{+} + V_{\text{in}}^{-}}{2}\right)$$

Where Ad is the differential-mode gain and Ac is the common-mode gain.

The common-mode rejection ratio is usually defined as the ratio between differential-mode gain and common-mode gain:

$$\mathrm{CMRR} \triangleq \frac{A_\mathrm{d}}{A_\mathrm{c}}$$

In the above equation, as Ac approaches zero, CMRR approaches infinity. Thus, for a perfectly symmetrical differential amplifier with Ac = 0, the output voltage is given by:

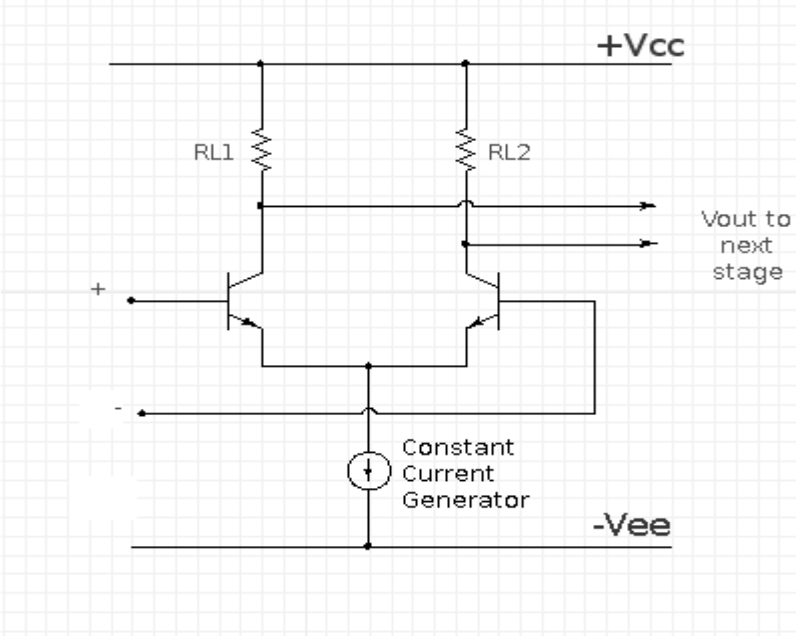
$$V_\mathrm{out} = A_\mathrm{d}(V_\mathrm{in}^+ - V_\mathrm{in}^-)$$

Note that a differential amplifier is a more general form of amplifier than one with a single input; by grounding one input of a differential amplifier, a single-ended amplifier results.

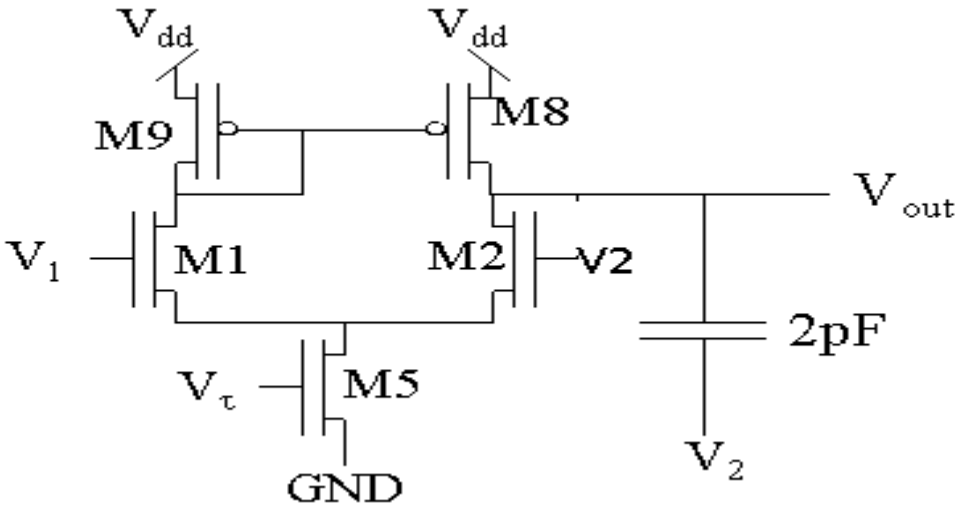
Some kinds of differential amplifier usually include several simpler differential amplifiers. For example, an instrumentation amplifier, a fully differential amplifier, a negative feedback amplifier, a instrument amplifier, or a isolation amplifier often includes several op-amps; and those op-amps usually include a long-tailed pair.

A differential amplifier is the input stage of operational amplifiers, or op-amps, and emitter coupled logic gates.

Differential amplifiers are found in many systems that utilize negative feedback, where one input is used for the input signal, the other for the feedback signal. A common application is for the control of motors or servos, as well as for signal amplification applications. In discrete electronics, a common arrangement for implementing a differential amplifier is the long-tailed pair, which is also usually found as the differential element in most op-amp integrated circuits.

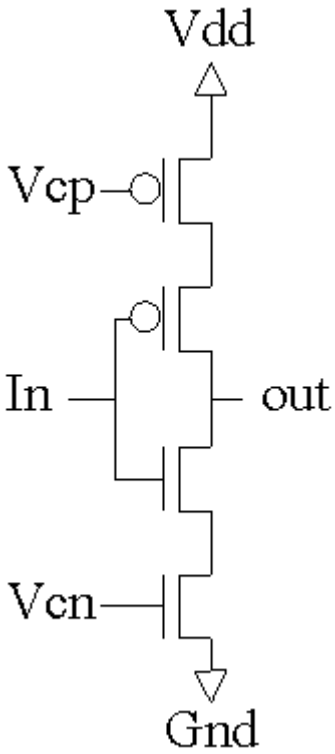


Differential Amplifier



Current source load Differential amplifier

2.1.3 **Current Starved Inverter**



2.1.4 **Current starved VCO**

VCOs are widely used in PLLs to provide a local clock signal that can be locked to the frequency and phase of a reference signal. Current-starved VCO topologies are commonly used because of their wide frequency range of operation, allowing for tunable designs that can easily accommodate the high-speed specifications in an RF application.

Description of VCO Circuit Topology

The current-starved VCO, schematically represented in Fig. 1, includes two components: the input-bias stage and a ring oscillator (RO) structure designed using an odd number (N>5) of current-starved inverters, where N is the number of RO stages. The input voltage, V_{invco}, sets the current through the input-bias stage and current mirrors, which subsequently control the current through the current-starved inverters and control the delay of each stage. The RO oscillates at a period of (Td*2N), where t_d is the delay time of an inverter stage.

Design:

$$C_{ox} = \frac{\mathcal{E}_{ox}}{t_{ox}} = \frac{\mathcal{E}_0 \mathcal{E}_r}{t_{ox}}$$

$$K_n = U_{0n} * C_{oxn}$$

$$K_p = U_{0p} * C_{oxp}$$

In Inverter we take $\frac{W_n}{L_n} = \frac{3}{2}$

Both the NMOS and PMOS are designed for equal drive

i.e. $K_n \frac{W_n}{L_n} = K_p \frac{W_p}{L_p}$

$$C_{tot} = C_{ox}(W_p L_p + W_n L_n) + \frac{3}{2} C_{ox}(W_p L_p + W_n L_n)$$

$$= \frac{5}{2} C_{ox}(W_p L_p + W_n L_n)$$

$I_{DCentre}$ =N*C_{tot}*V_{dd}*F_{centre}

Where N=total Number of inverters in series (must be odd)

F_{center} =Centre frequency

The W/L ratio for the N1 and N2 can be calculated from the following formula

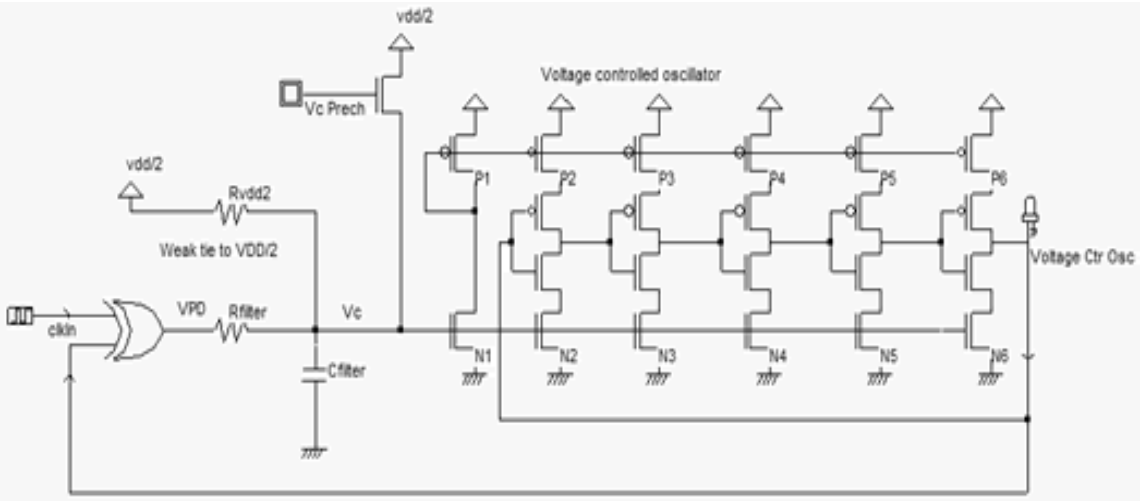
$$I_{centre} = \frac{\beta}{2}(V_{GS} - V_{TH})^2$$

$$= \frac{K_n}{2} \cdot \frac{W_n}{L_n}(V_{GS} - V_{TH})^2$$

P1 and P2 and are same β as N1 and N2

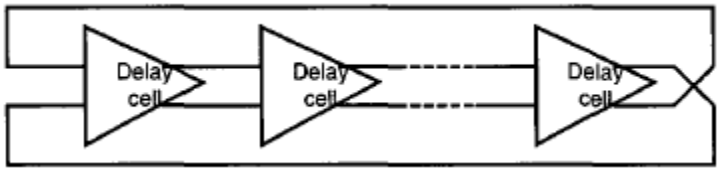
So W/L ratio for these MOS can be calculated from the following formula

$$K_n \frac{W_n}{L_n} = K_p \frac{W_p}{L_p}$$

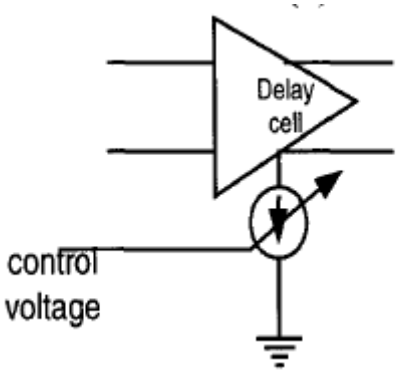


2.2 Limited Range Problem Of conventional VCO

The most common used architecture for VCO in CMOS technology is voltage controlled ring type oscillator. It consists of several delay cells forming a closed loop as shown in figure. The output clock frequency is determined by the delay of each delay cell which in turn is controlled by control voltage. A wide frequency range of oscillator means a wide tuning range of each delay cell. The delay cell is usually a differential pair with a tail current and some active loading. The delay of each cell is controlled by the tail current. There are some difficulties associated with this architecture to achieve the wide tuning range. By using a single tail current, the tuning range is limited by the control voltage range. The control voltage is usually constraint by the power supply voltage, i.e. $0 \leq V_{control} \leq V_{dd}$ .If we choose the small tail current, the tail current is still not large enough even that the control voltage reach the up limit so that the high end frequency range of VCO is small. On the other hand, if we choose the large tail current, the tail current is still large even that the control voltage reached the lower limit so that the lower end frequency range of VCO is large.



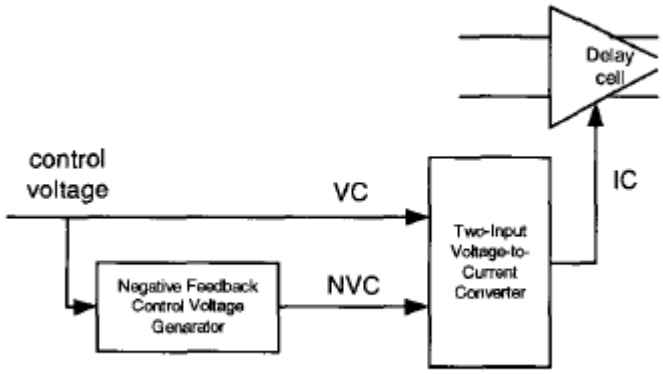
Ring type Oscillator



Voltage controlled delay cell

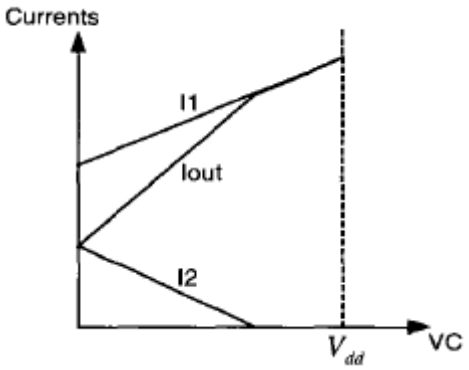
2.3 Negative feedback architecture

In order to solve the limited range of conventional VCO architecture, the negative feedback controlled architecture is proposed. Figure shows a block diagram of the proposed architecture. This architecture includes three blocks: a negative feedback control voltage generator, a two-input voltage to current converter and delay cells. The negative feedback generator converts the control voltage which will be inputted to the voltage-to-current converter block. The two input voltage-to-current converter converts the two control voltage inputs VC and NVC to current IC which is supplied to the delay cell block. And finally the delay cell block delays the input signal to the output signal whose delay is controlled by controlled current IC.

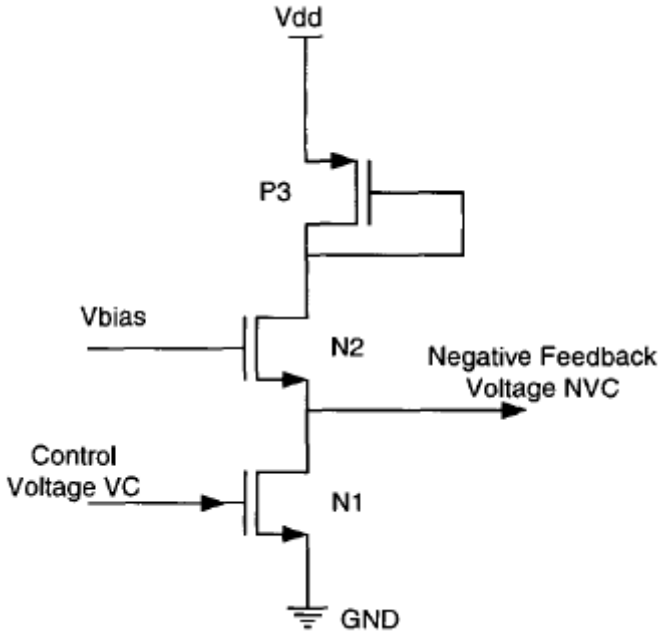


Block Diagram of proposed architecture

The negative feedback control voltage generator takes the control voltage VC (supplied by PLL) as an input and generates the negative feedback control voltage NVC. This block does not need any additional pre-settings such as register bits or reference voltages for comparators. The purpose of this block is that when the input control voltage VC is low, the output negative feedback control voltage should be high. On the other hand, when VC is high, NVC is low.



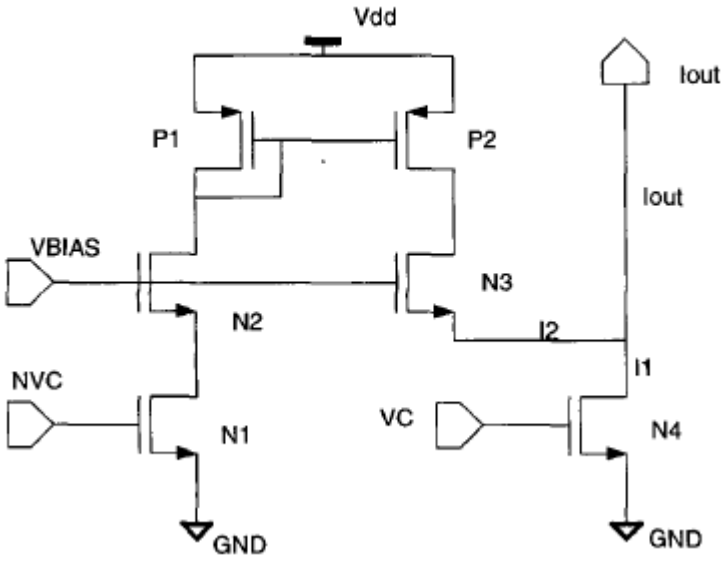
The relation between current and control voltage



Negative feedback control voltage generator

2.4 Two input voltage to current converter

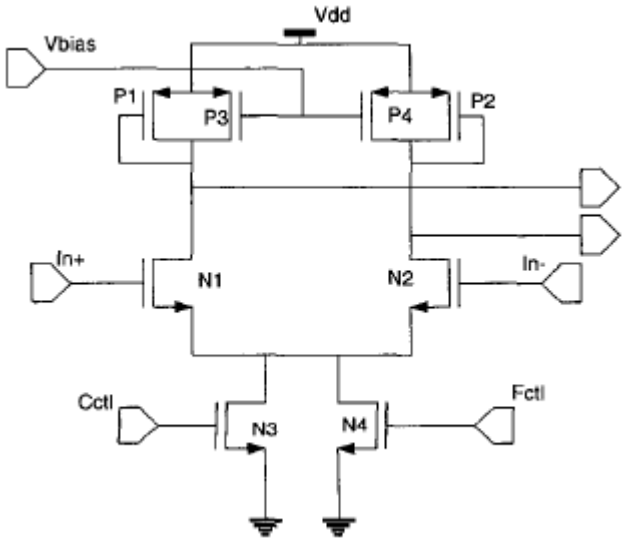
The two input voltage-to-current converter accepts the two control voltages VC and NVC as inputs and generates the control currents to each delay cell in the VCO. The purpose of this block is to generate the wide range currents with the limited range control voltage. The output is designed as the subtraction of two current sources controlled by the two input voltages. The output current is designed as the subtraction of he two current sources controlled by two input voltages: VC and NVC. The relations between I_{out},I_1 and I_2 and the control voltage are shown in the diagram.I_1 increase with increase in VC while I_2 decreases. So when the control voltage VC is small, the effective output current I_{out} is small although the current controlled by VC is large. But when VC is high, the effective output current I_{out} is equal to I_1 which is high because the current source I_2 is 0 and doesn't reduce I_{out}. So the current range is effectively expanded.



Two input voltage-to-current converter

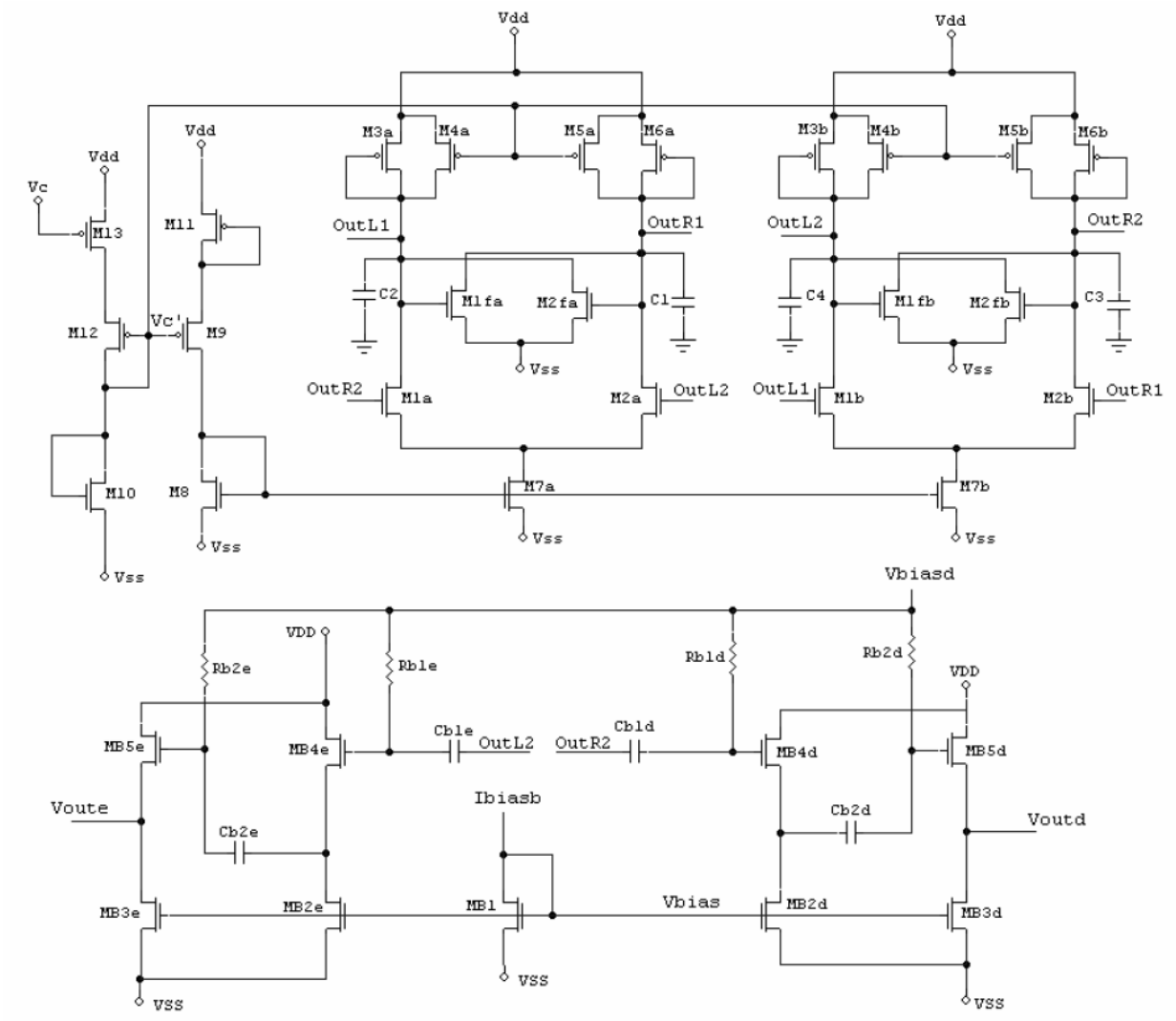
2.5 Delay cell design

The delay cell is a differential pair with loading and bias controls. The self biased techniques are used to reduce jitter and process variations. This arrangement for extended frequency range VCO results a large gain of the VCO. The above negative feedback scheme combined with advanced delay cell generates a wide frequency range and low phase noise VCO.

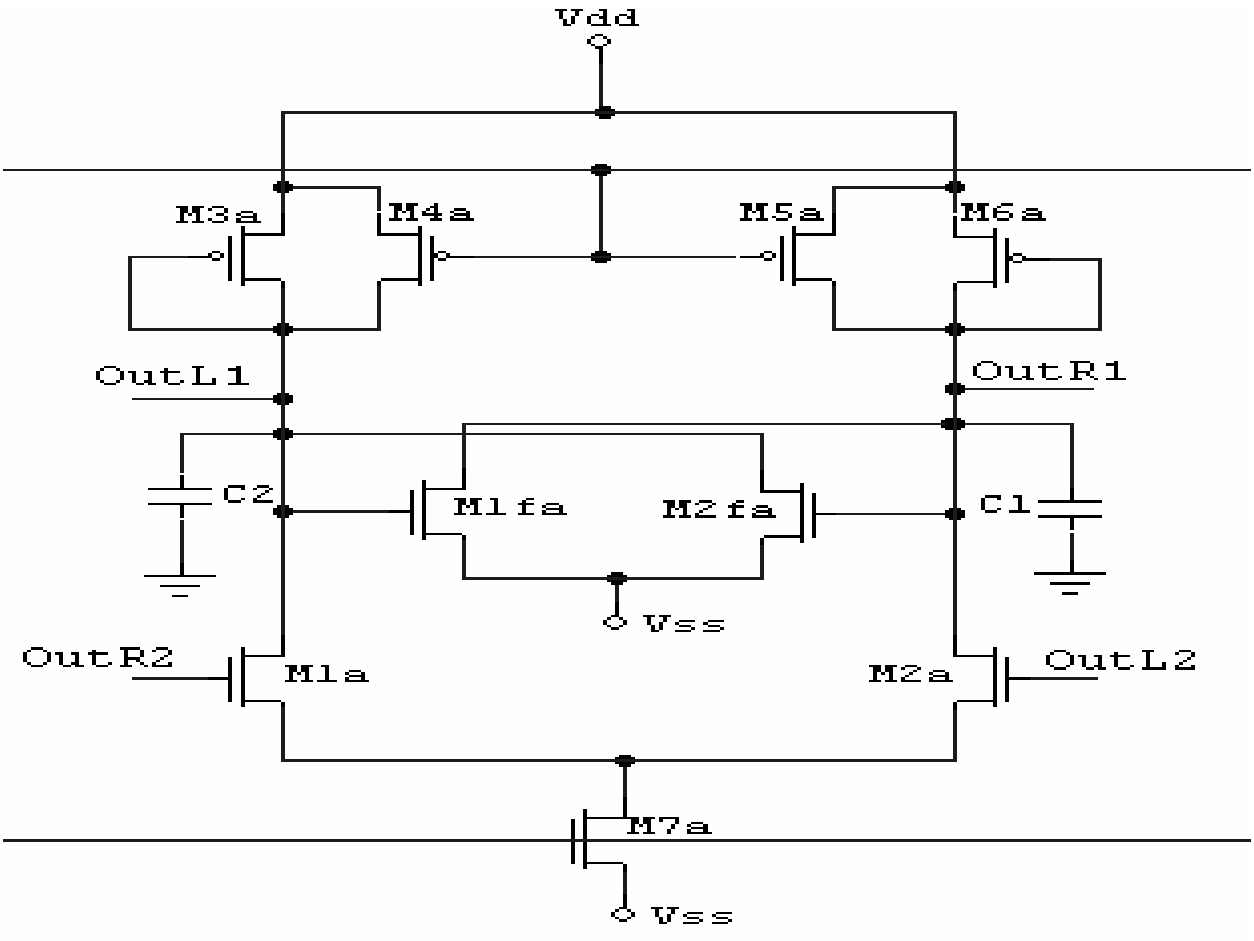


Delay Cell circuit

A High Swing Low Power CMOS Differential Voltage Controlled Ring Oscillator.



High Swing Low Power CMOS Differential Voltage-Controlled Ring Oscillator



Differential Amplifier Circuit with Positive Feedback

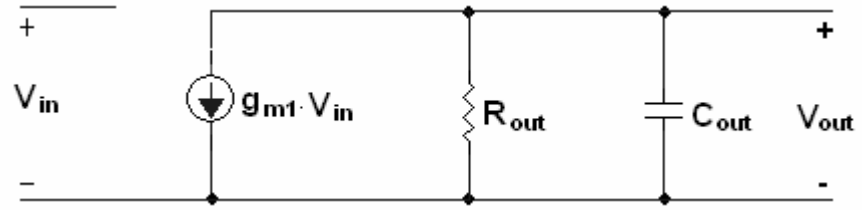
In the delay cells proposed in this work, we provide the necessary bias condition for the circuit to oscillate by means of using the positive partial feedback generated by M1f and M2f, as depicted in above figure..

In the upper portion of the circuit, we have M3 and M4 or M5 and M6, that implements a voltage controlled symmetrical load modifying the delay when the control voltage Vc is changed, together with the oscillation frequency. The use of this type of load allows diminishing the sensibility to variations in common mode and also the phase-noise of the circuit [8]. In the lower portion of the figure, a two-stage source follower buffer is implemented to drive the output load composed by pad and instrument capacitances isolating the VCO from these loads.

In the proposed VCO, the operation frequency is determined by the number of delay cells in the loop. The total capacitance and resistance associated to the output nodes depends on the operating regions of the transistors in the delay stages. The biasing scheme composed by transistors M8 to M13 provides a controlled bias current and a controlled voltage *Vc* ' in such a way that the transistors M4 and M5 stay in the saturation region for the whole control voltage range. Also this arrangement avoids the cells to loose gain maintaining a linear relation between the control voltage *Vc* and the tail current provided to the cells by M7. Transistor M10 allows

Establishing a minimum current for the delay cells even if the control voltage leaves its nominal values.

If the transistors M4 and M5 are always in the saturation region, the small signal model of the transistors can be used to analyze the circuit, as stated in figure below.

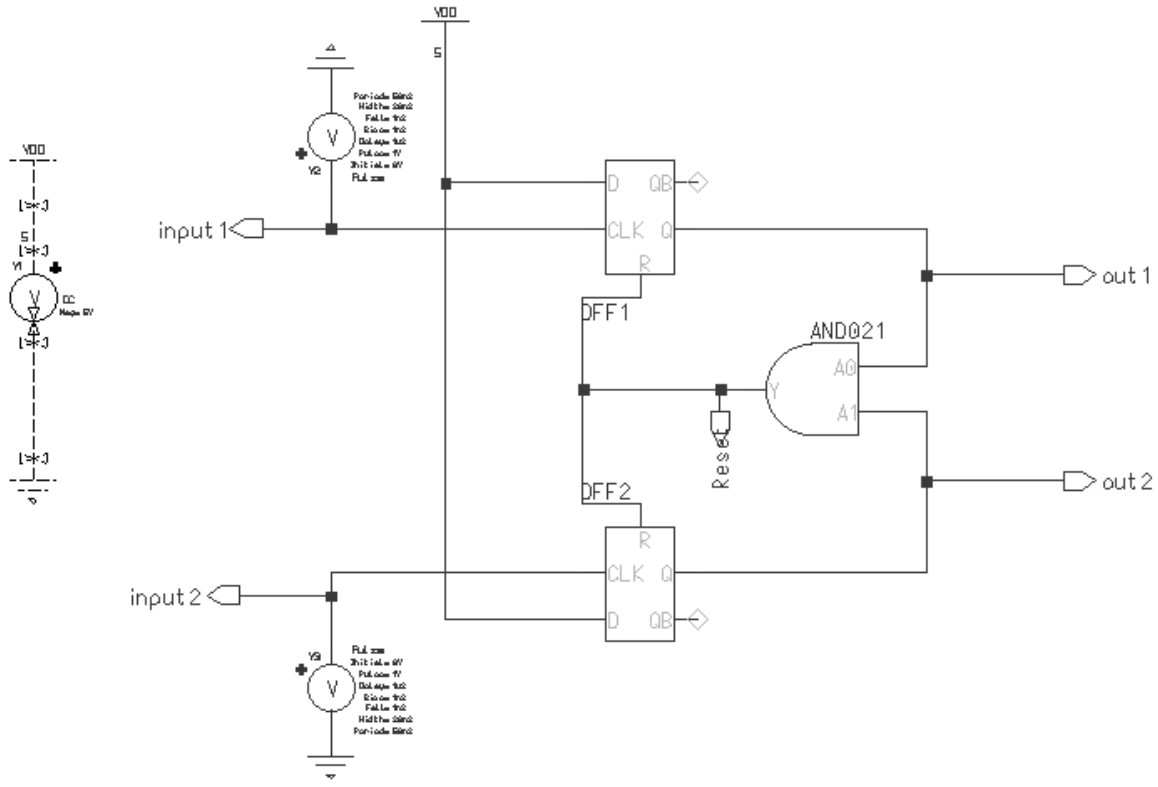


From figure one can derive the resistance and capacitance at the output node of the circuit

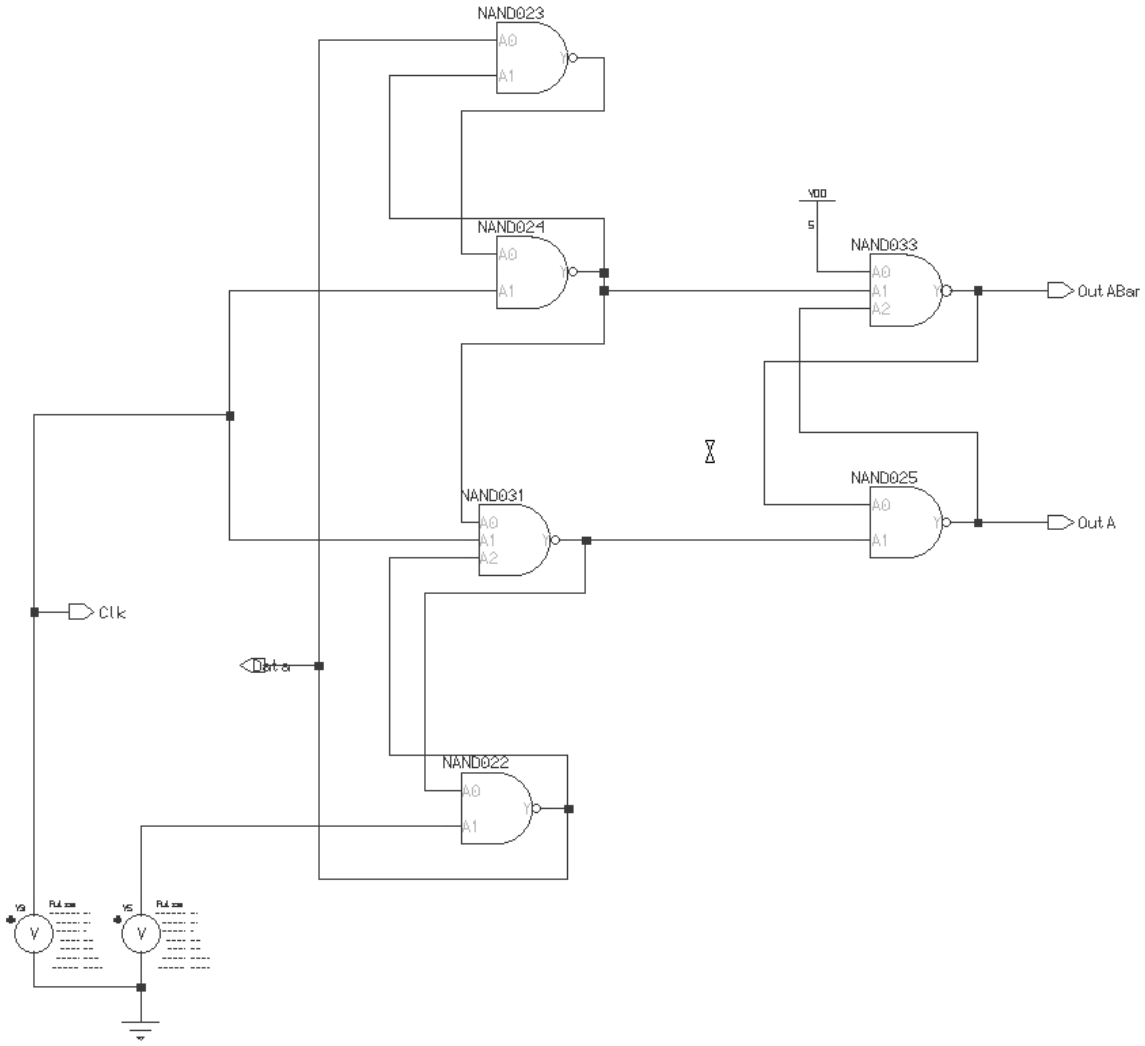
The frequency behavior of the VCO is determined by the inverse relationship to the delay of each cell, which is $\tau = R*C$. In this case, the action is taken in the R variable, modifying the output conductances of transistor M4 and M5 through the variation of voltage Vc'.

3. Circuit Design

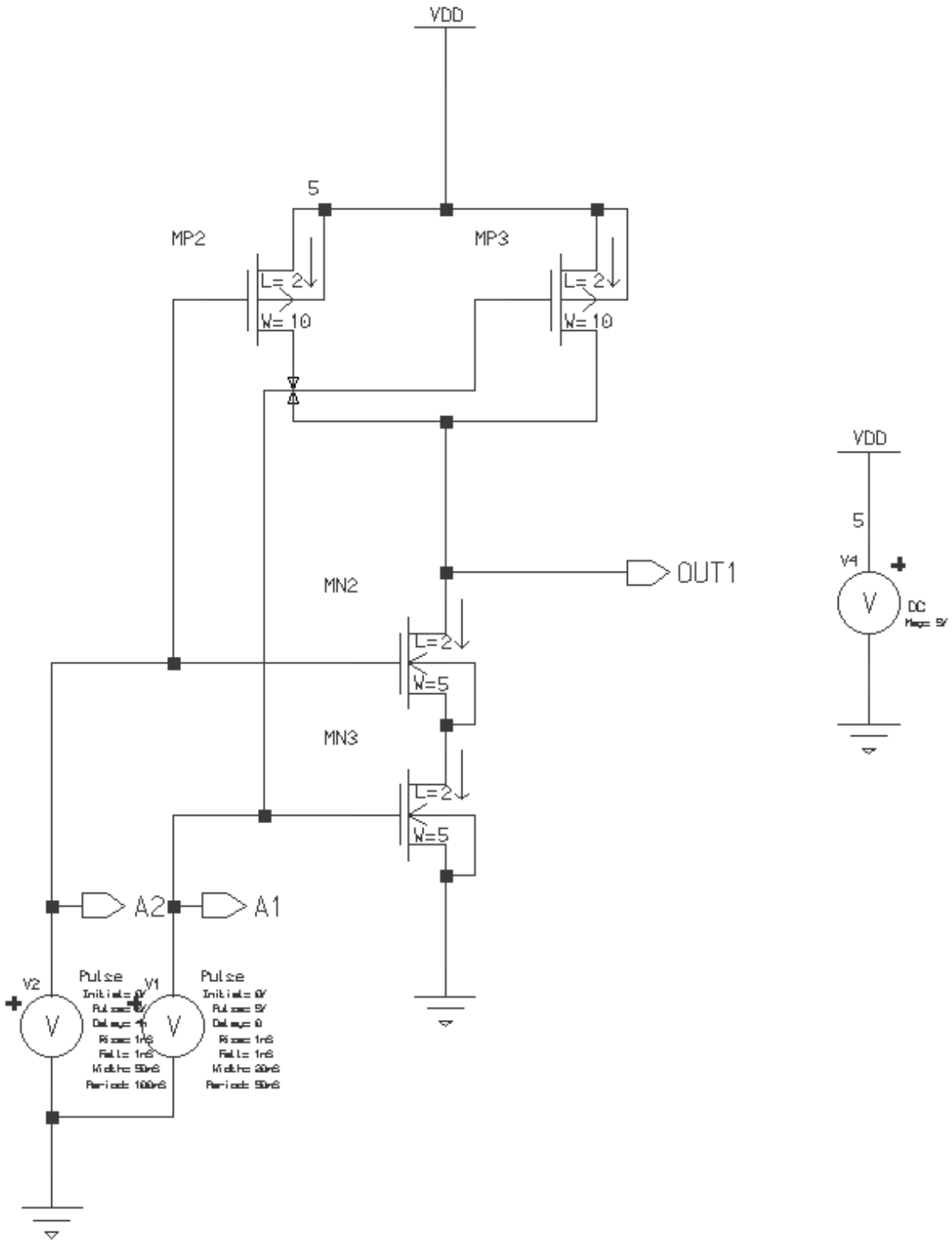
3.1 Phase frequency detector circuit



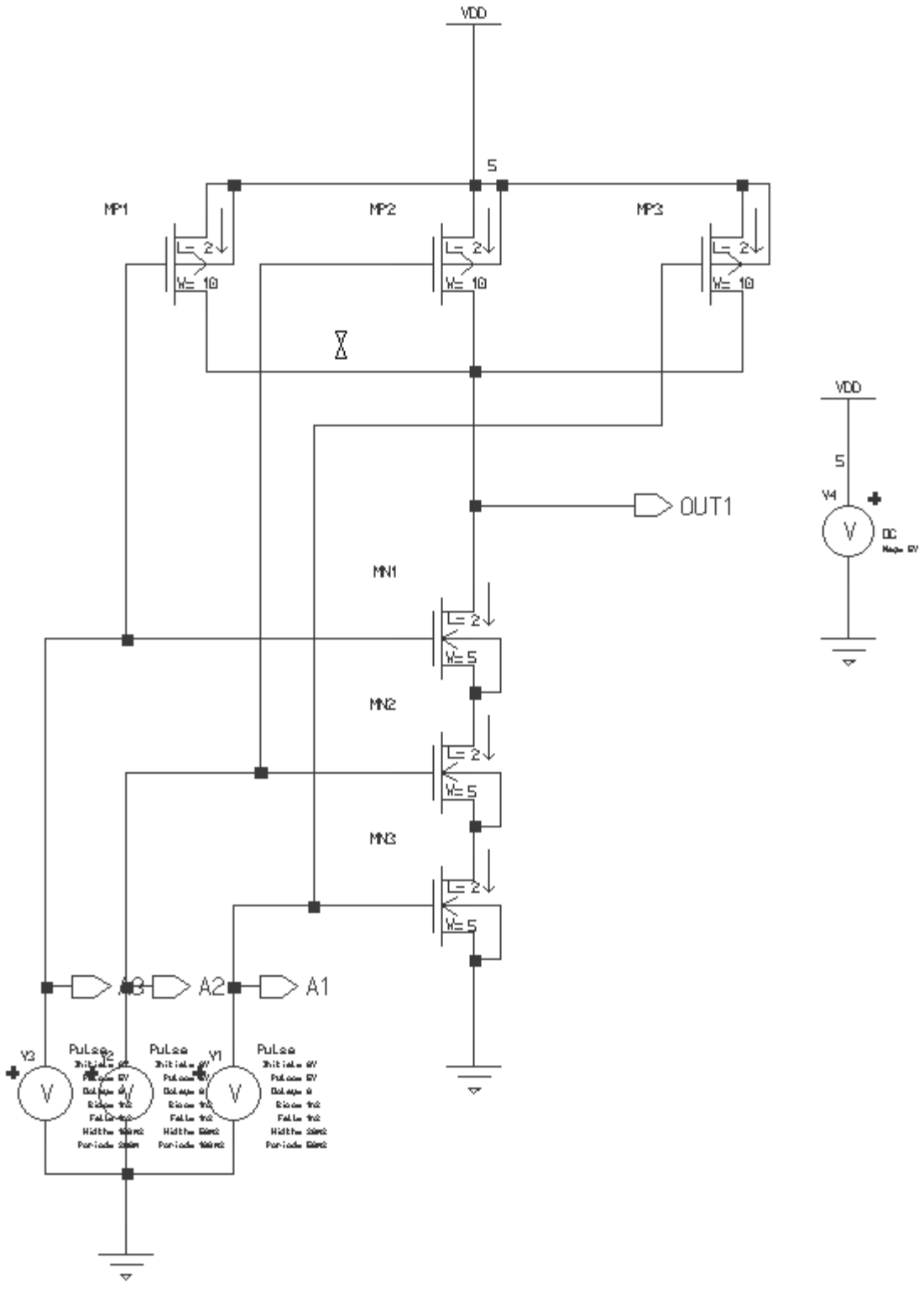
Phase Frequency Detector Circuit Using D-flip-flop



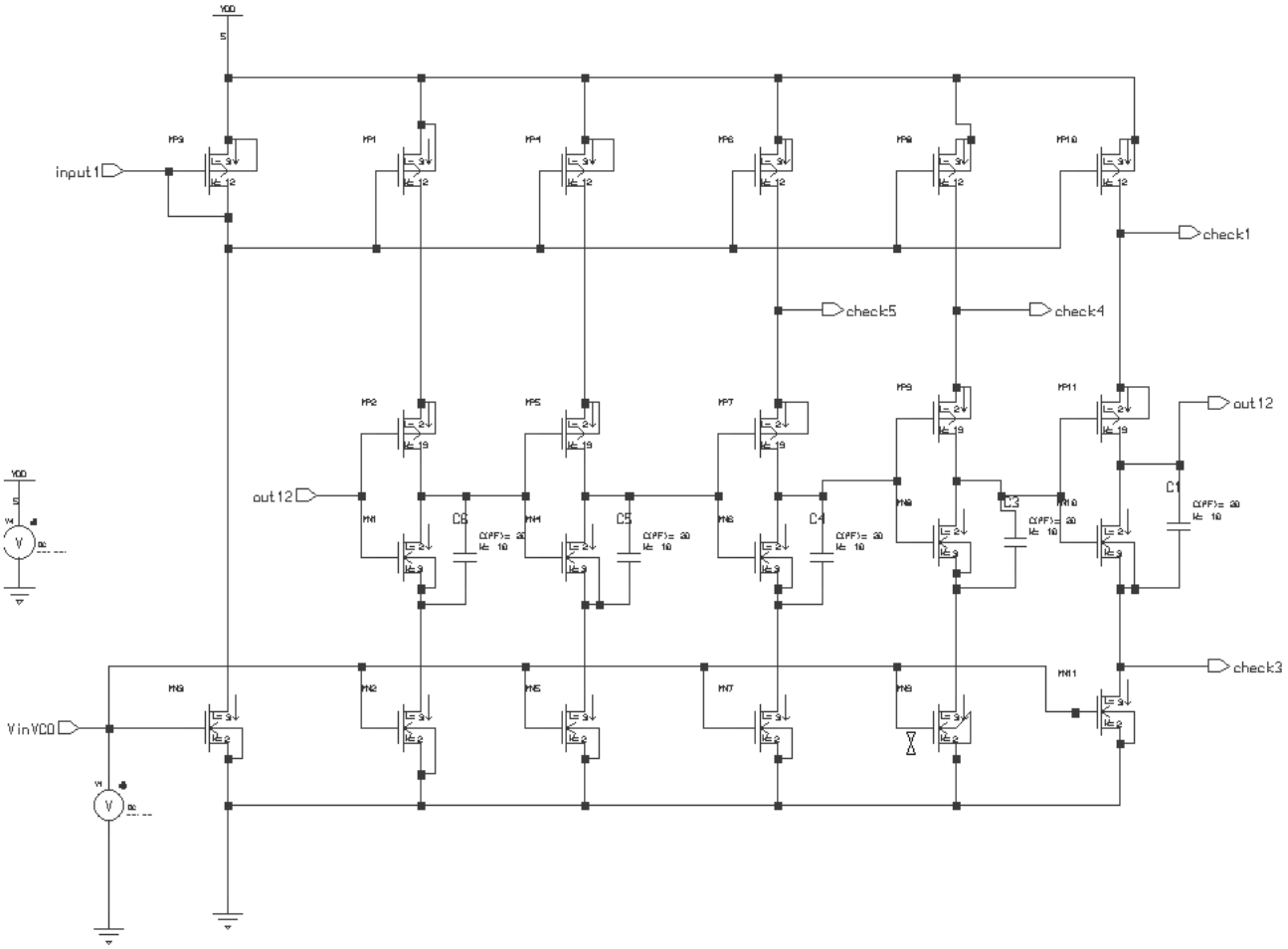
D-Flip Flop (with clock and Reset) Using Nand Gates



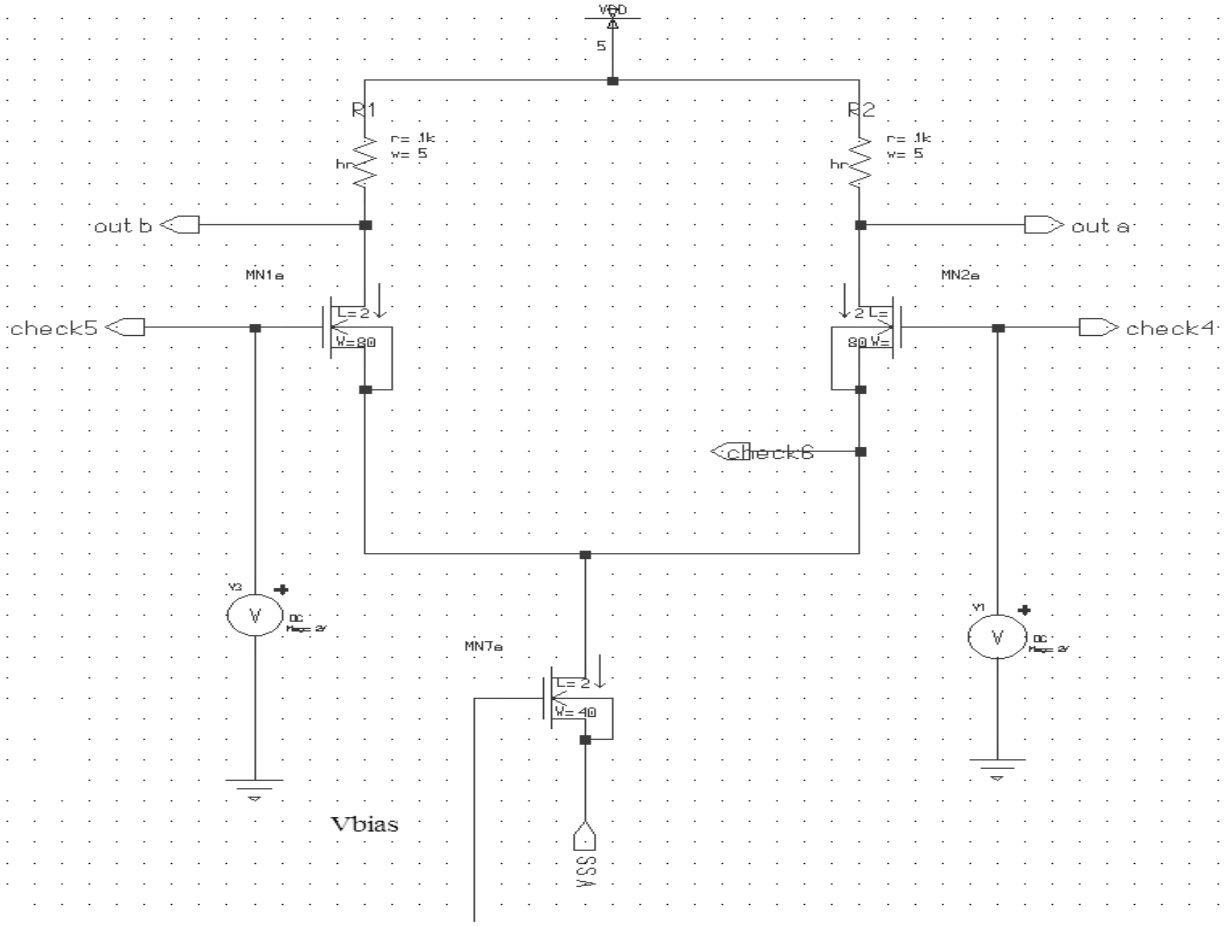
Two Input Nand Gate Using CMOS



Three Input Nand Gate Using CMOS



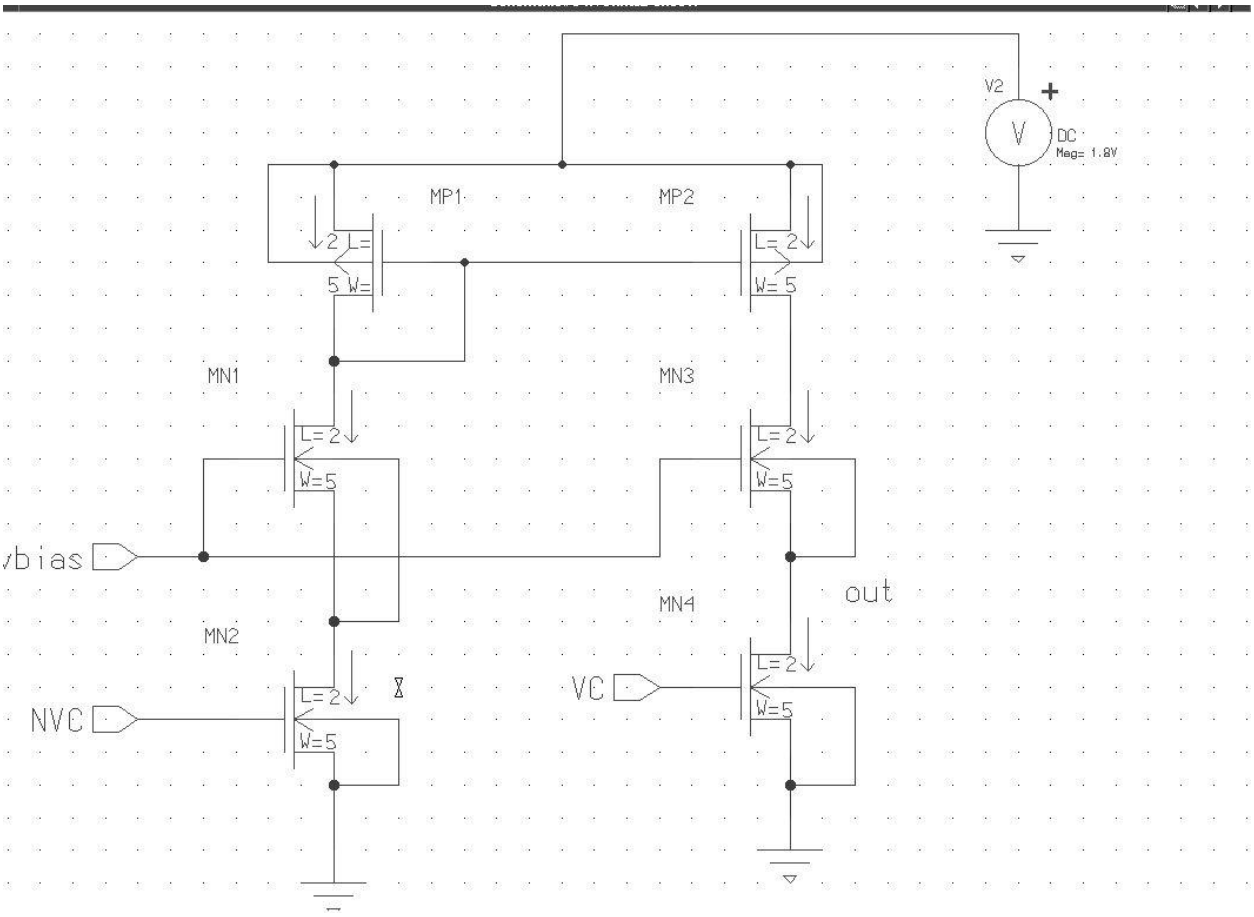
Current Starved VCO



Differential Amplifier

3.1 Negative feedback control voltage generator

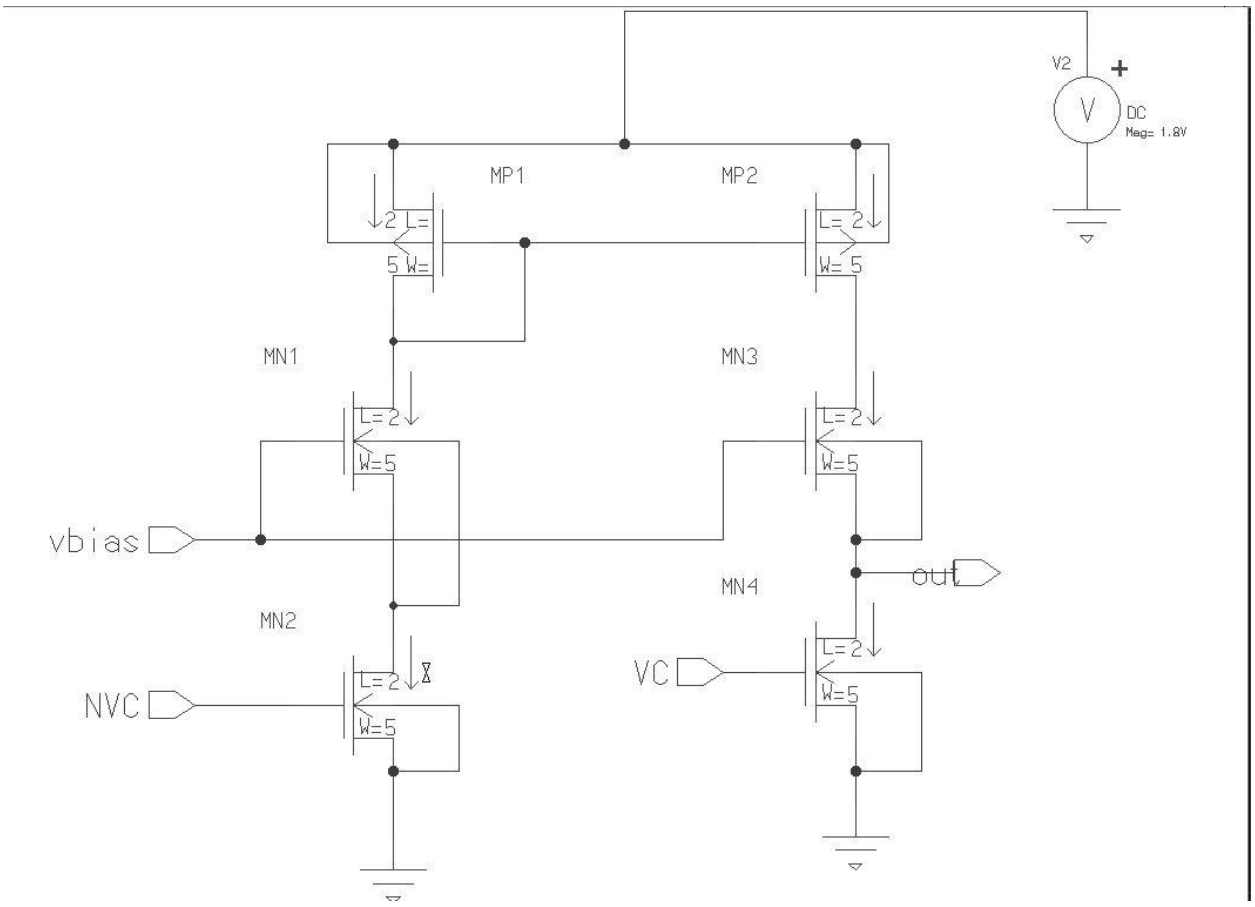
The negative feedback control voltage generator is based on a common source amplifier. The transistor diagram is shown in the figure. There are two transistors N1 and N2 and one PMOS transistor P1. The input signal is connected to gate of N1 and the gate of N2 is connected to a bias voltage. The output signal is taken from the drain of N1. So when input VC is low, NMOS transistor N1 is in cut-off region, the drain of N1 will be pulled to a high voltage. On the other hand, when the input VC is high, N1is ON and pull the drain voltage almost to ground, i.e. the output voltage NVC will be very small.



Negative feedback voltage generator

3.2 Two input voltage to current converter circuit

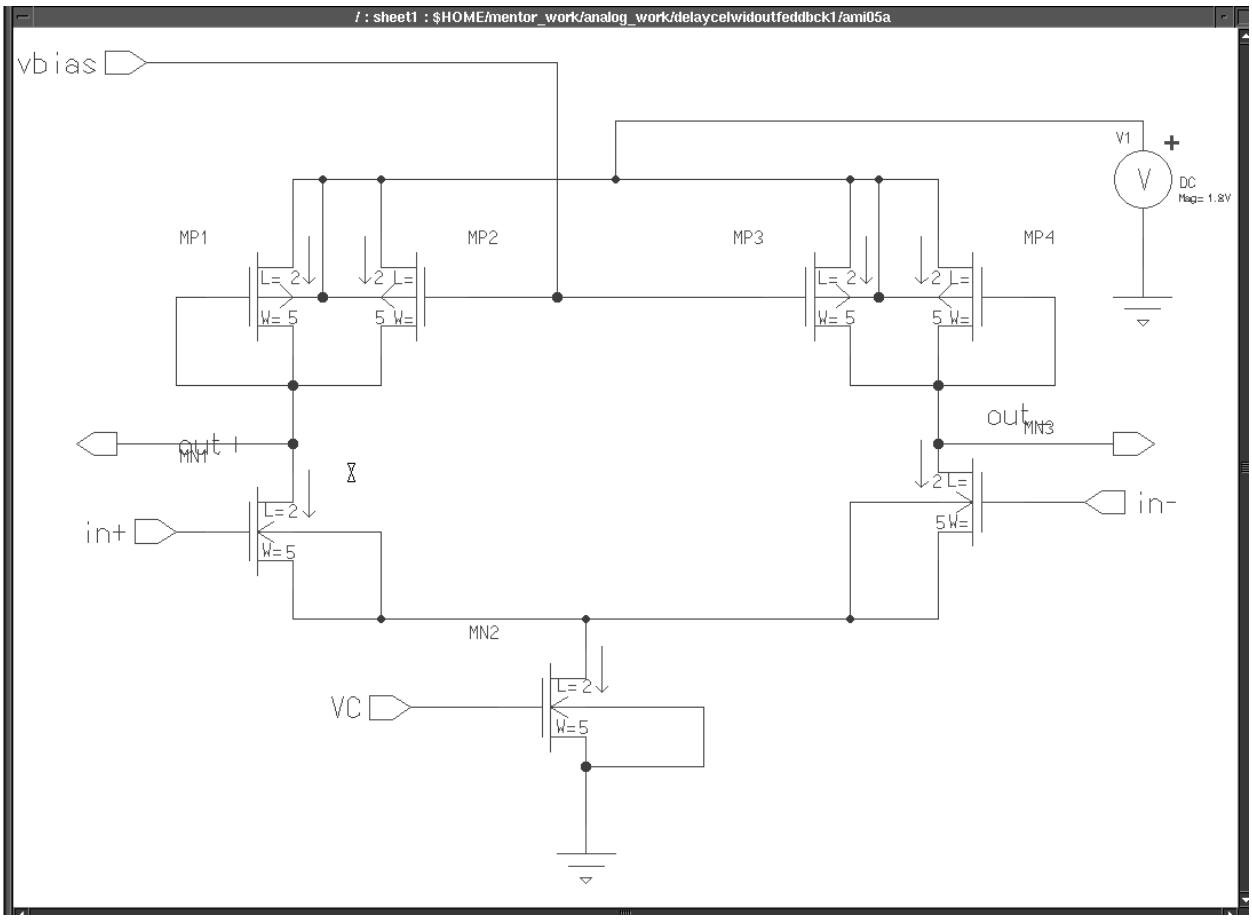
The two input voltage to current converter circuit is shown in the figure. Control voltage VC controls the current source N1 which is mirrored by transistors N2, P1, P2. The output current I_{out} equal to I2 subtracted from I1.



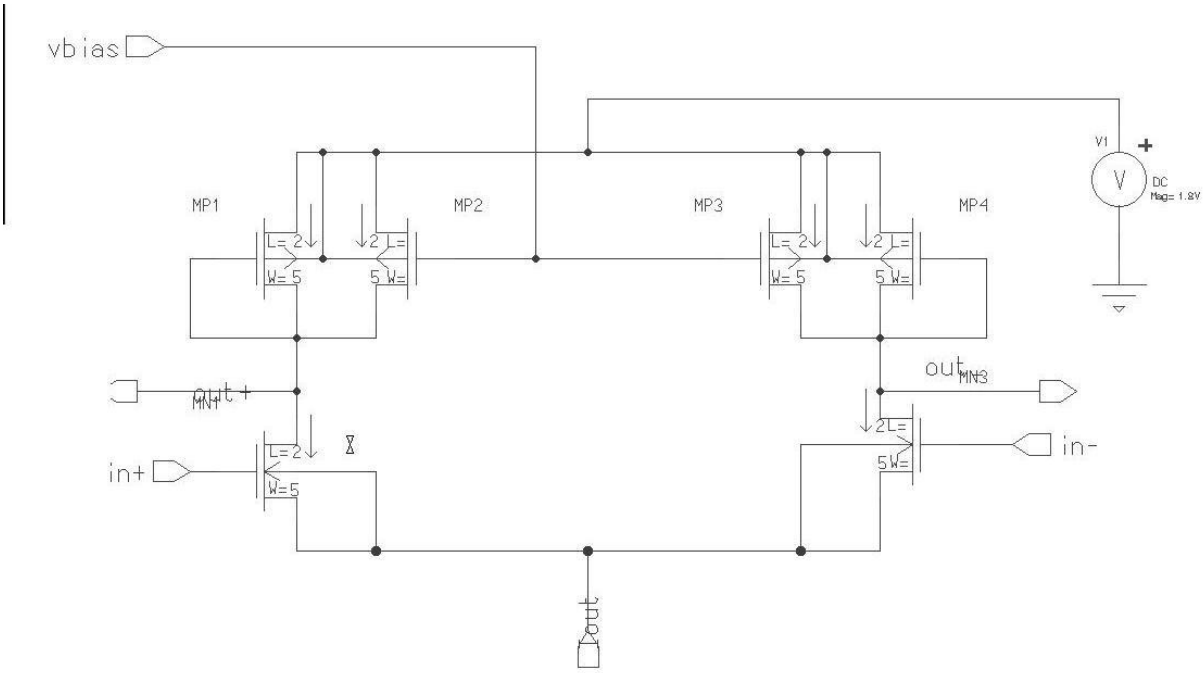
Current-to-voltage converter

3.3 Delay cell circuit

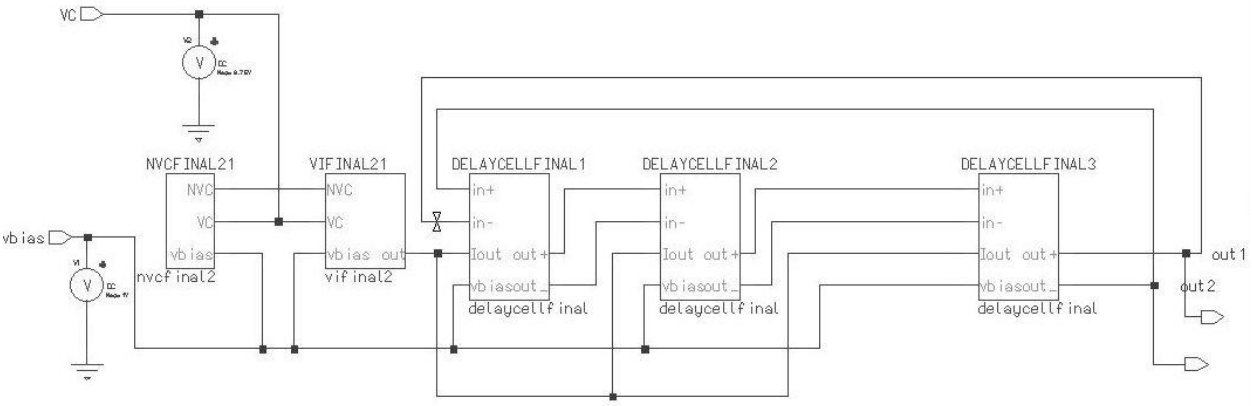
The delay cell circuit is shown in the figure. The delay cell is a differential pair with loading and bias controls. The self biased techniques are used to reduce jitter and process variations.



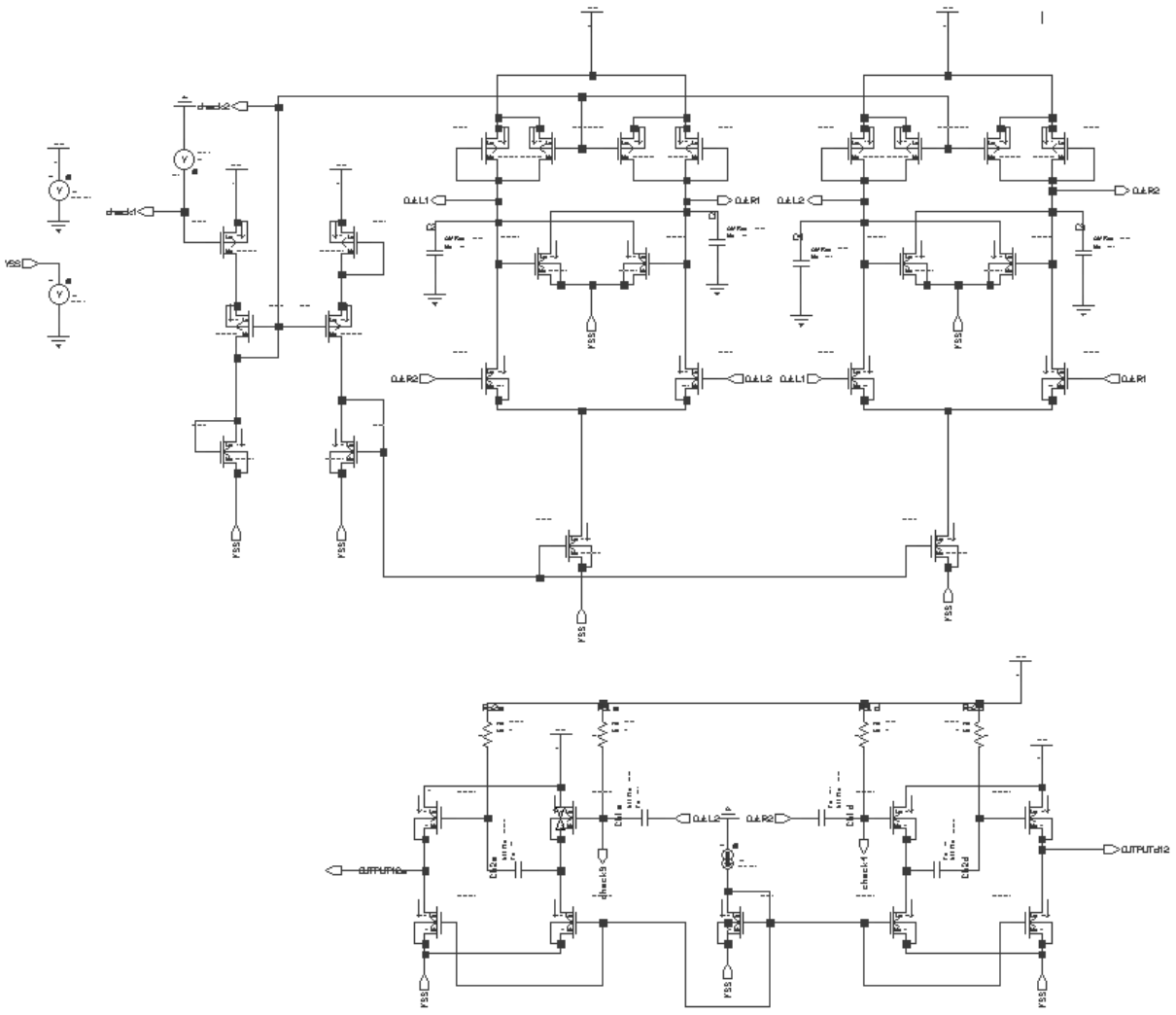
Delay cell no feedback



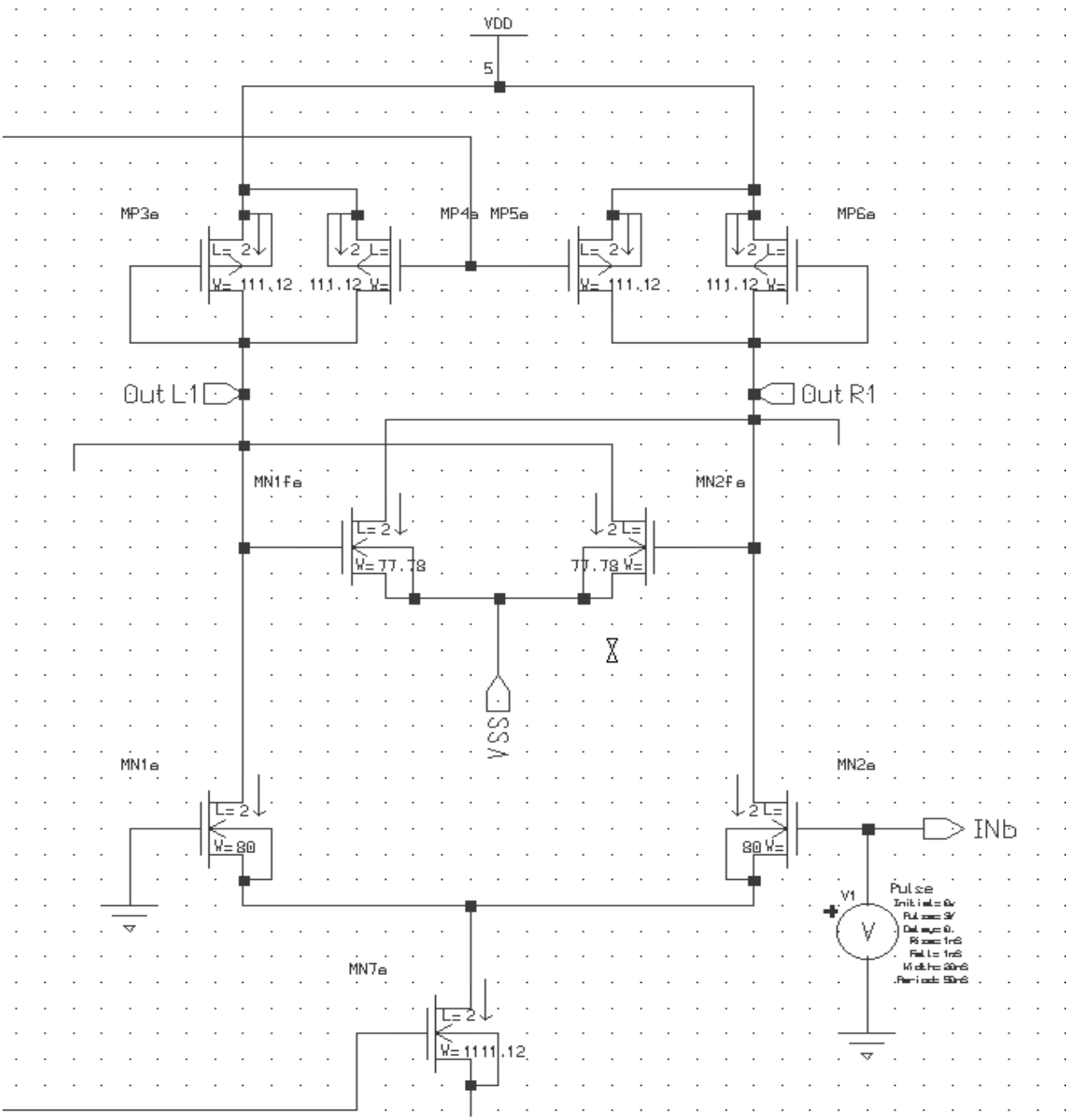
Delay cell with feedback



Proposed VCO

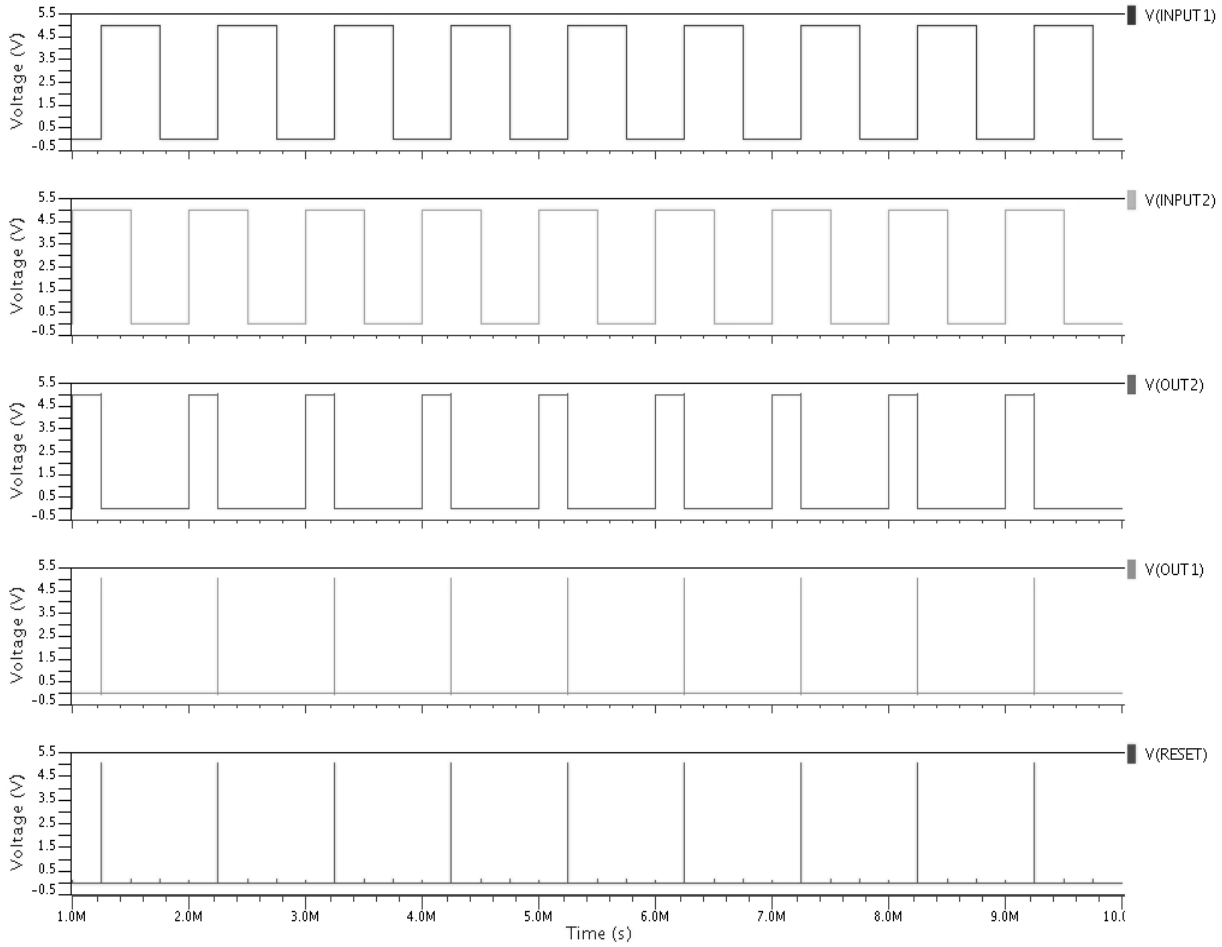


High Swing Low Power CMOS Differential
Voltage-Controlled Ring Oscillator

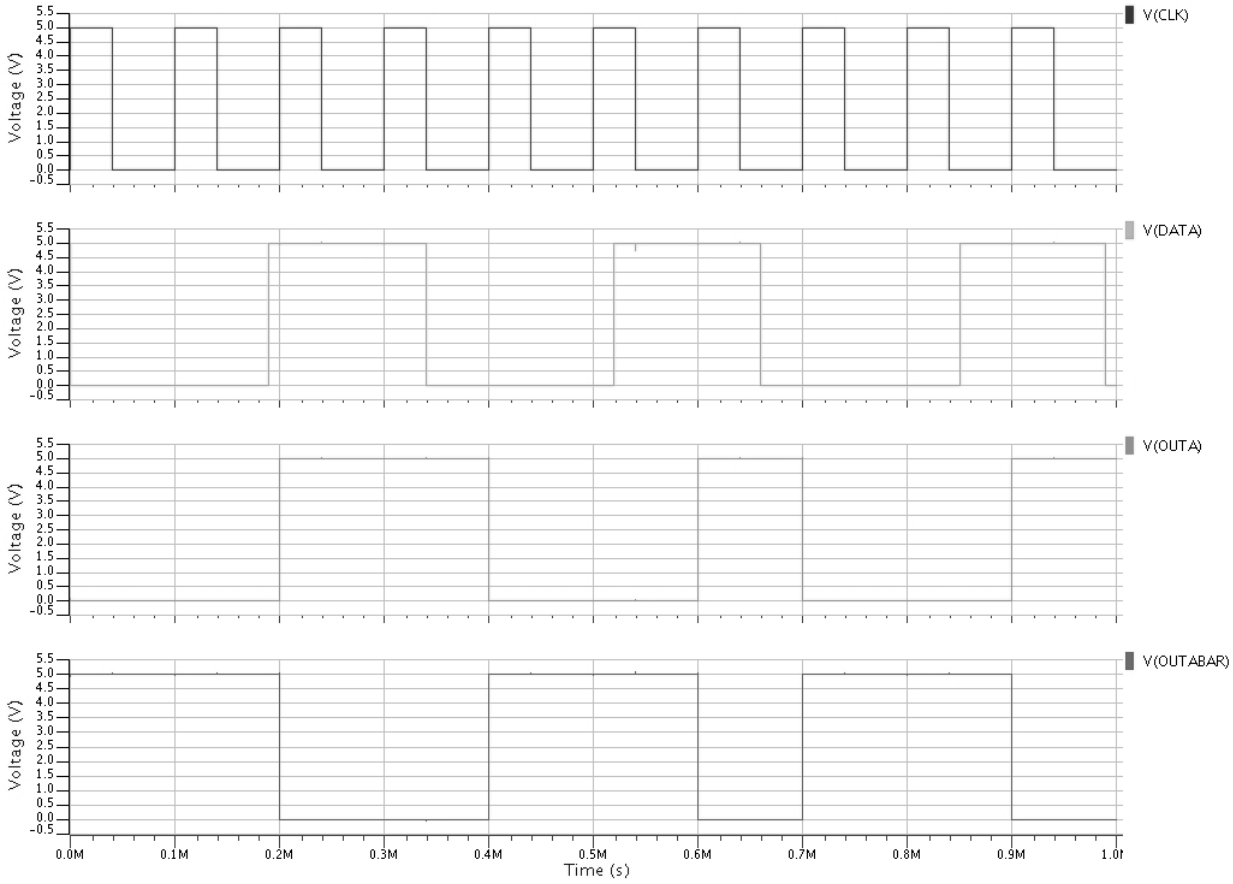


Differential Amplifier Circuit with Positive Feedback

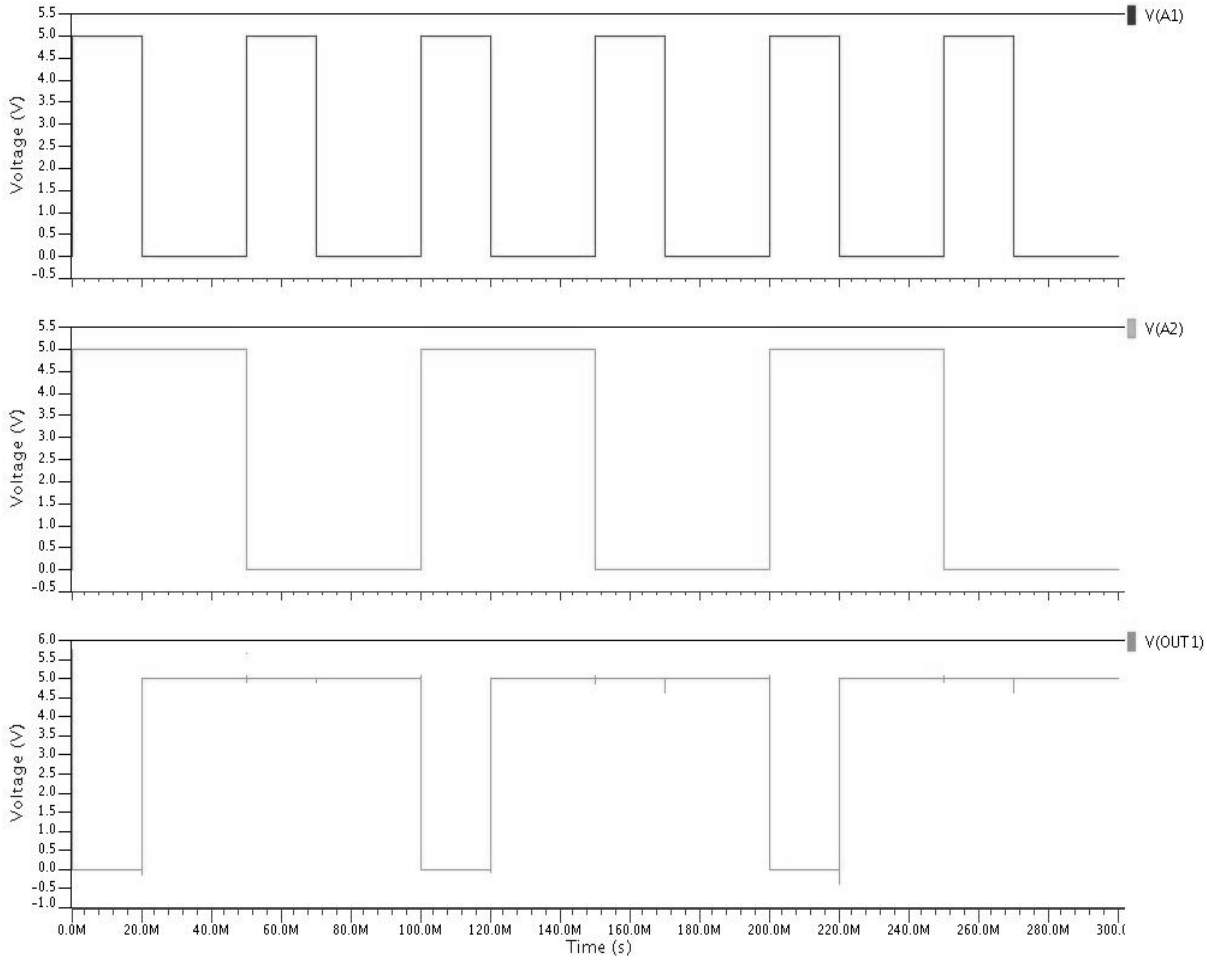
4. Results



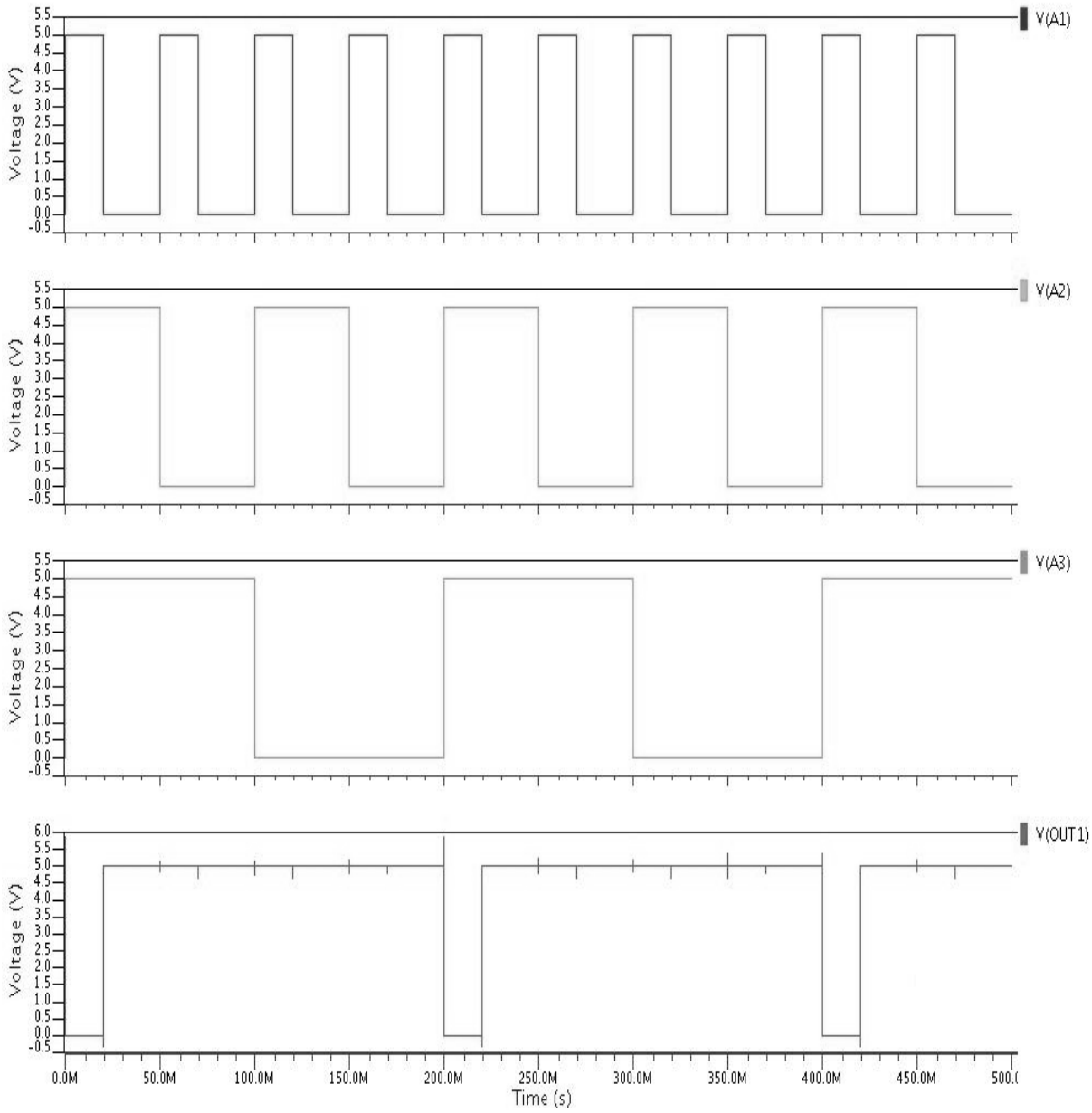
Phase detector Output



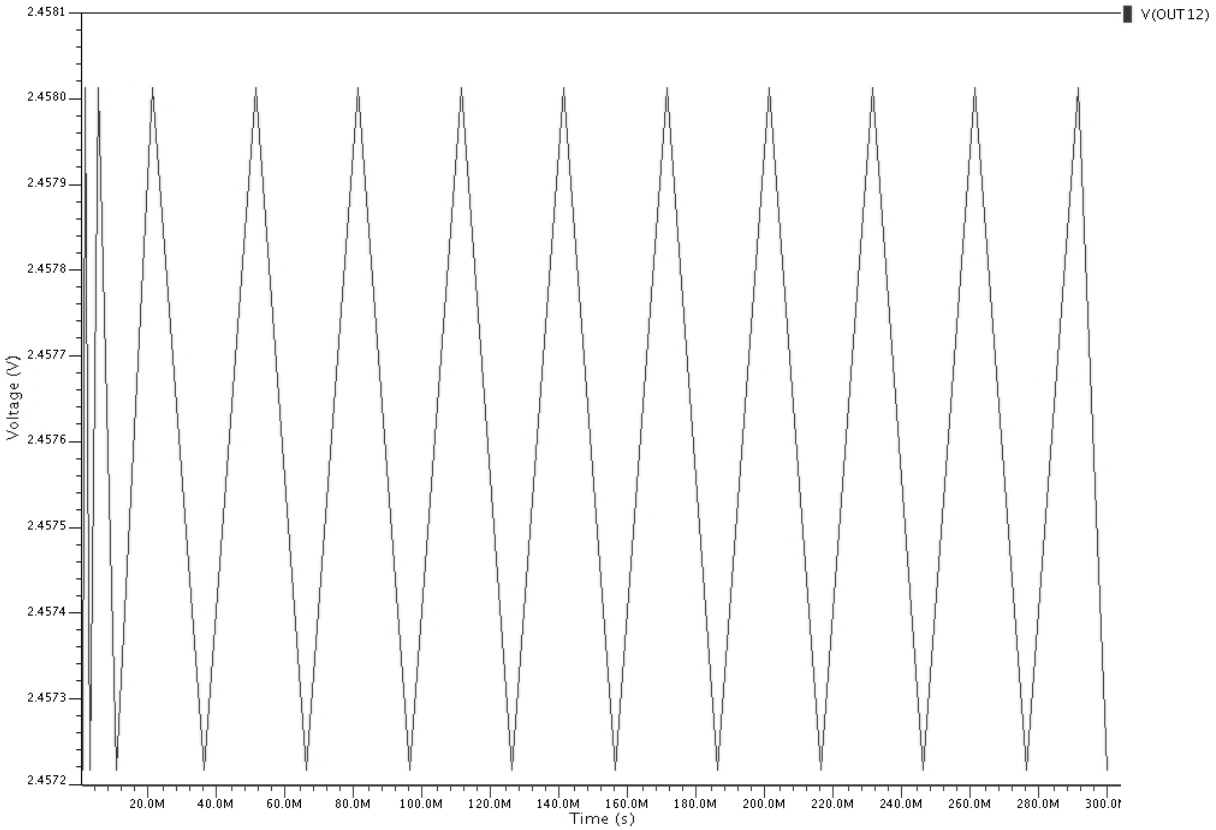
Edge Triggered D-Flip Flop Output



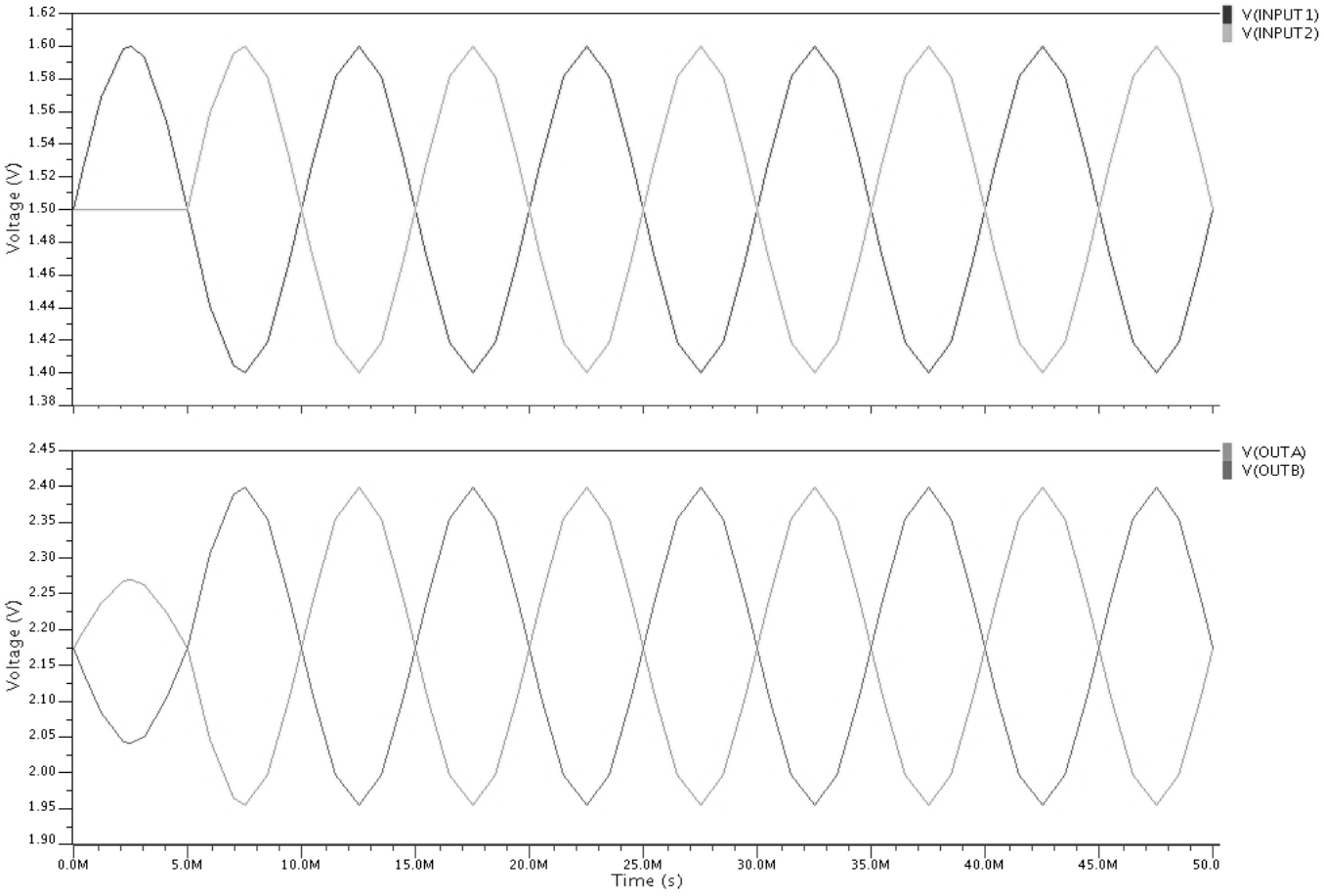
Two input Nand Gate Output



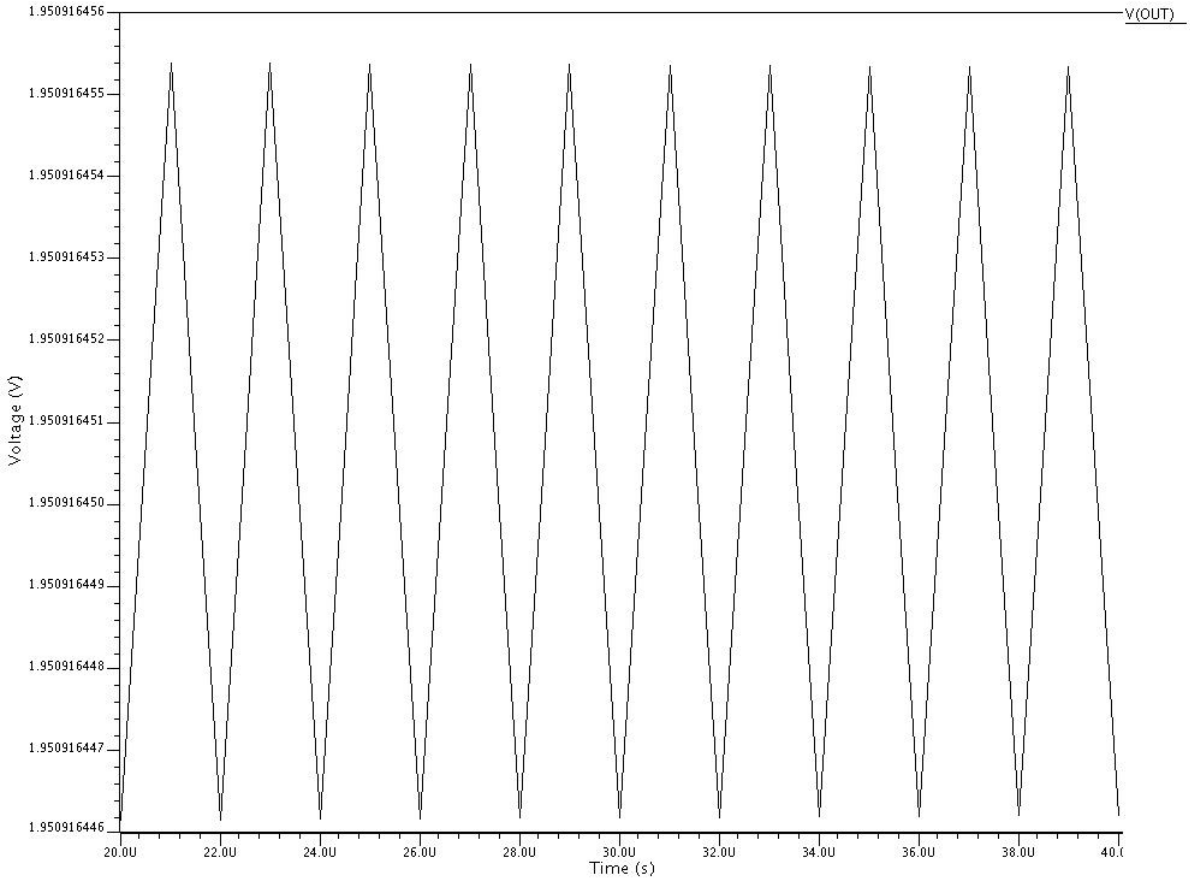
Three Input Nand Gate Output



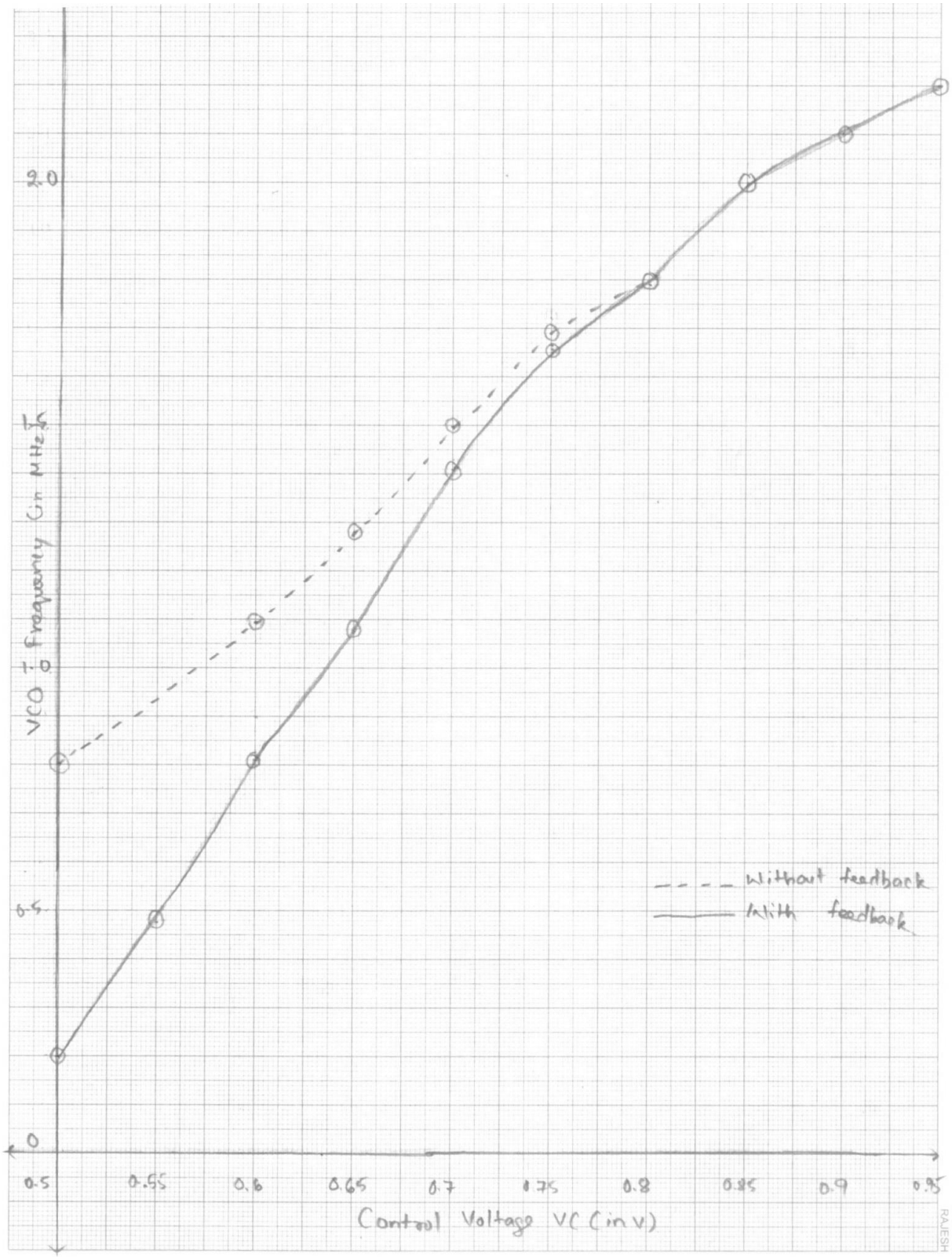
Current starved VCO output



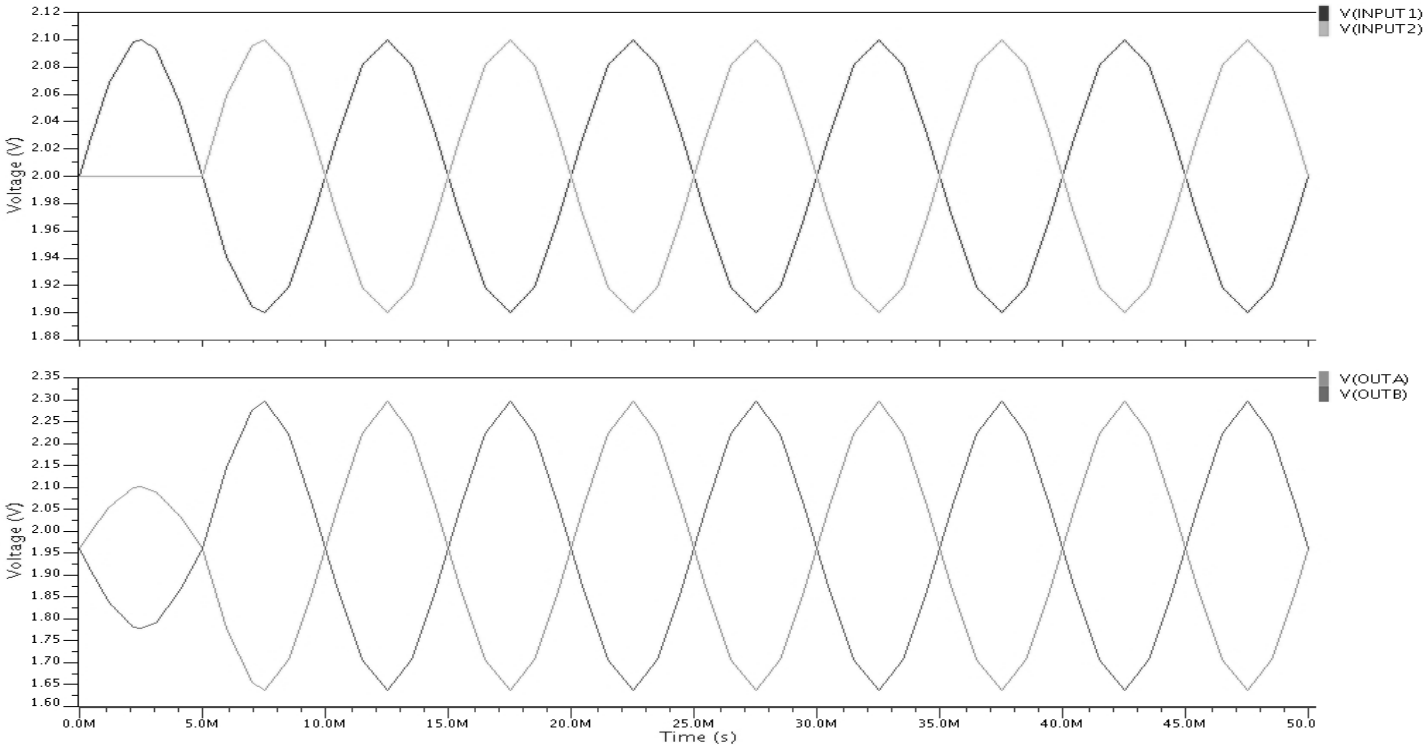
Differential Amplifier



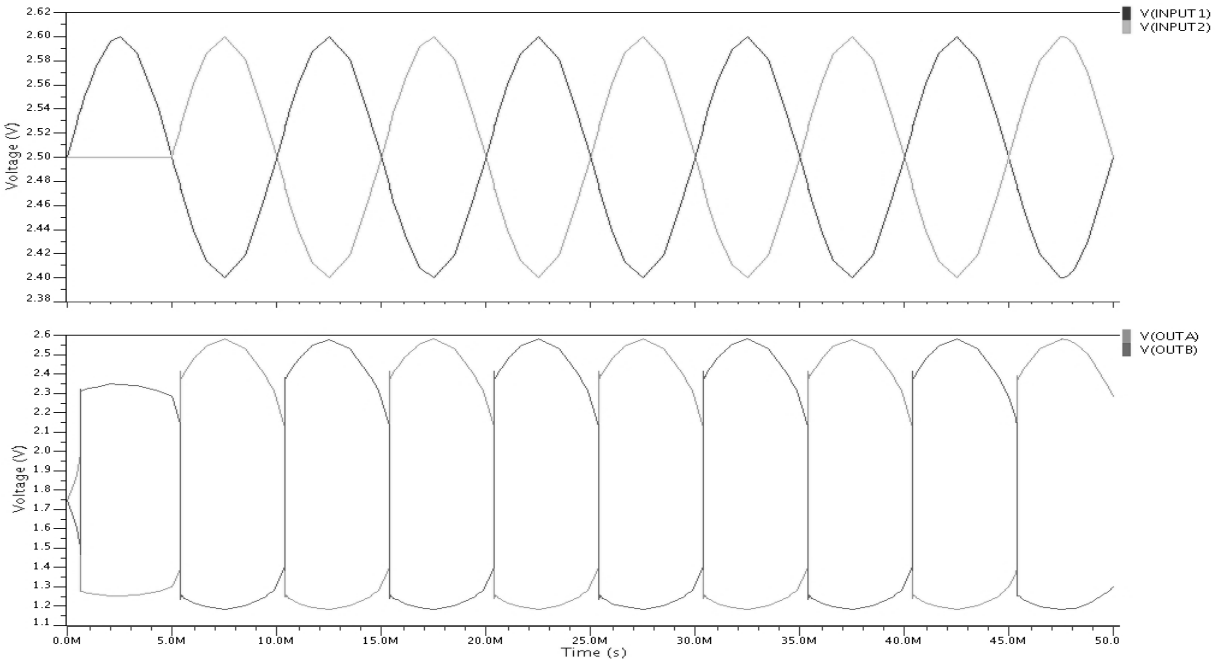
Proposed VCO output


VCO f.o frequency (in MHz)
2.0
1.0
0.5
0
0.5
0.55
0.6
0.65
0.7
0.75
0.8
0.85
0.9
0.95
Control Voltage VC (in V)
without feedback
with feedback
RAJESH

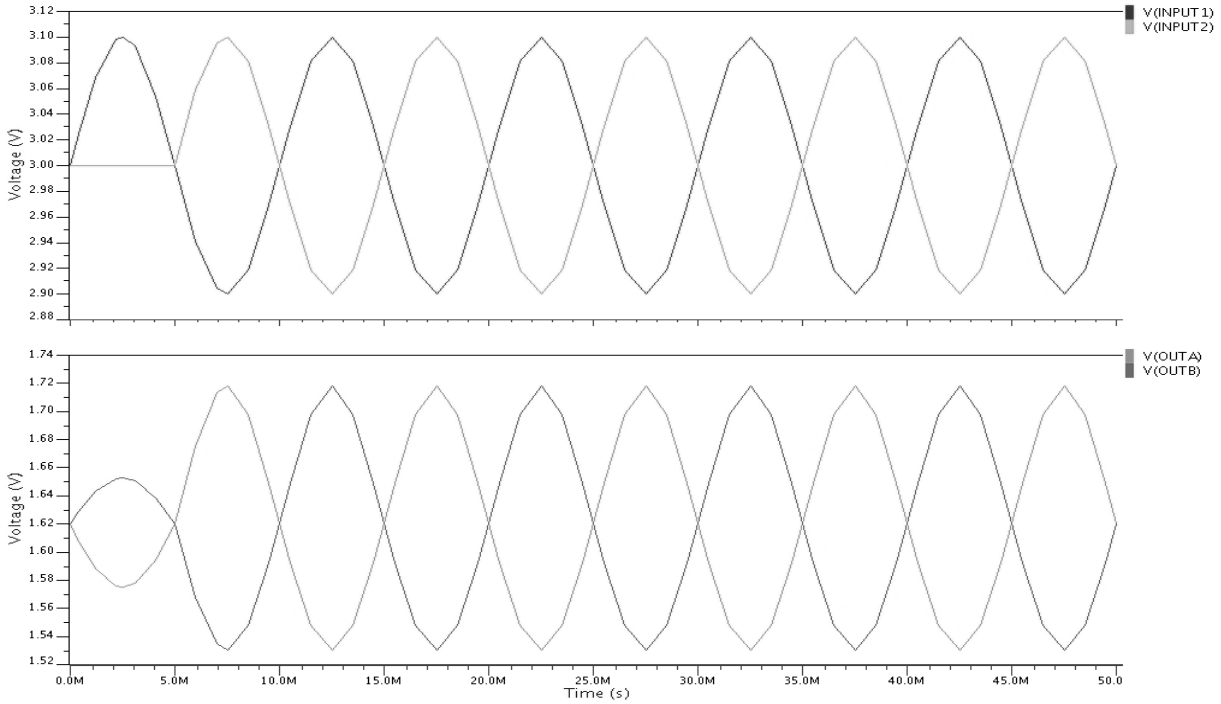
Figures for Differential amplifies used in the High Swing Low Power CMOS Differential Amplifier.



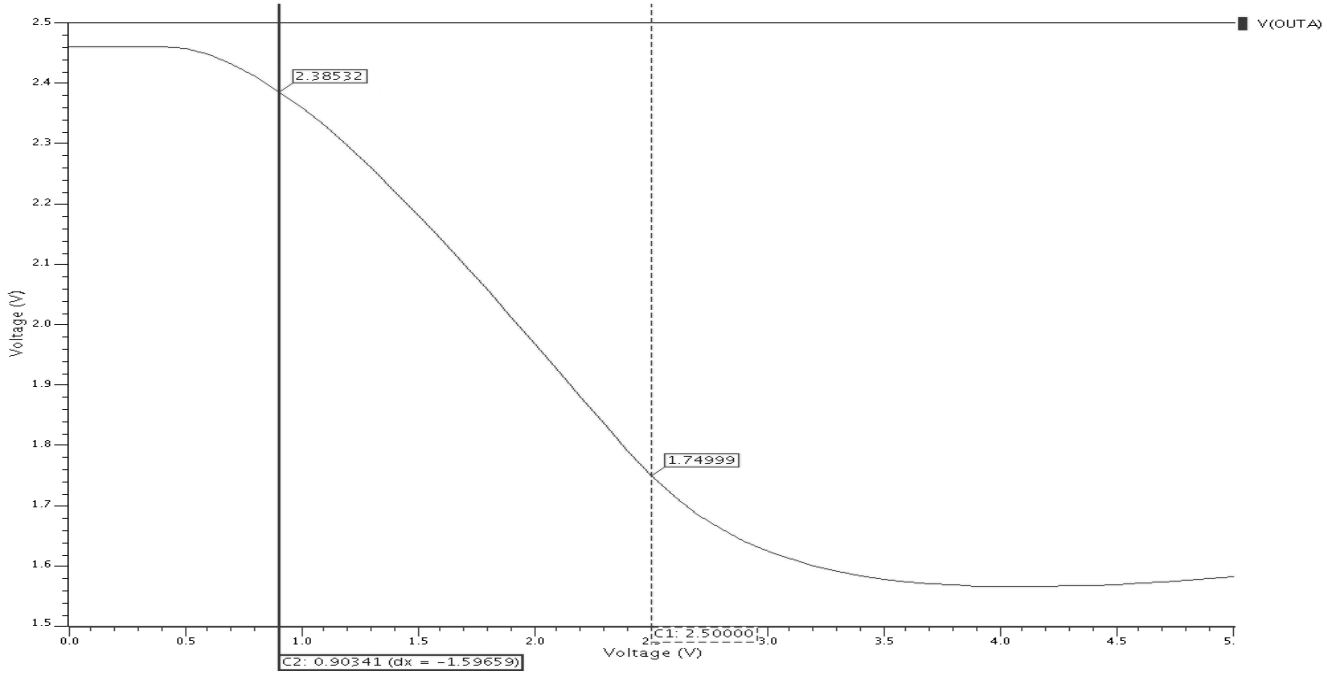
VCO input bias Voltage=2V



VCO input bias Voltage=2.5V

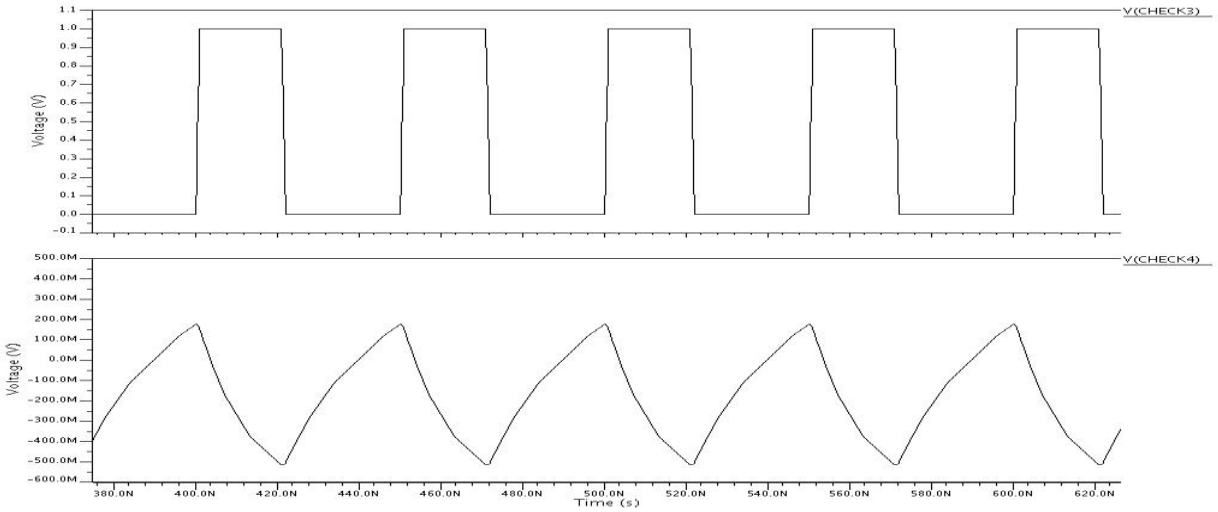


VCO input bias Voltage=3V

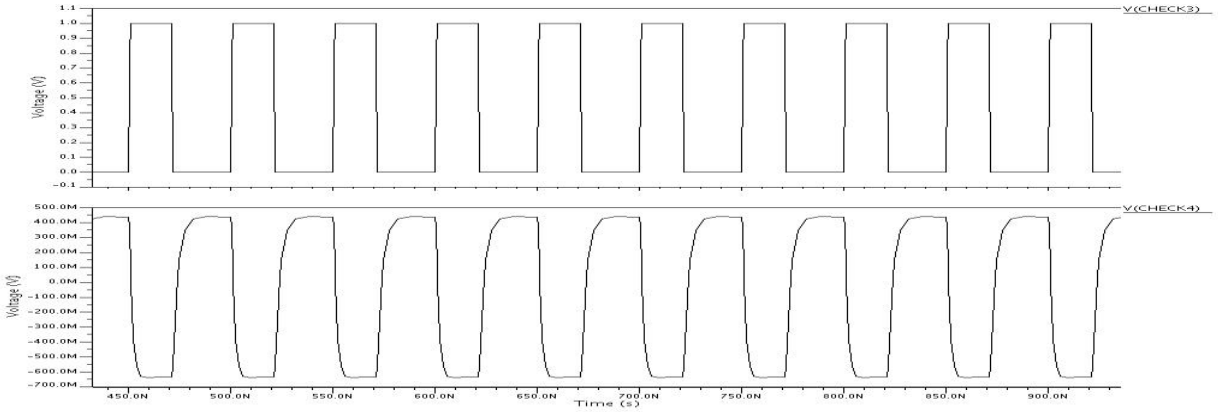


DC Analysis of Diff. Amp (one input at ground)

Results for High swing Low power CMOS differential voltage controlled oscillator



c=100pf, vc=1 M1 and M2 at VSS



c=10pf vc=1 M1 and M2 at VSS

5. Conclusion

In this report, we designed an extended frequency range CMOS monolithic voltage controlled oscillator (VCO) design. A negative feedback control algorithm is used to automatically adjust the VCO range according to the control voltage. Based on this analog feedback control algorithm, the VCO achieves a wide range without any pre-register settings. Low phase noise can be achieved by using both coarse and fine control in VCO.

The output of the current Starved VCO is in the range of mili volts. This is may be due to the improper W/L ratio of the MOSFETs. Because in the design we use very simple equations for describing the behaviors of the MOS but MOS doesn't work according to these equations.

6. Bibliography

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7. R. Jacob Baker , Harry W.Li , David E.Boyce CMOS Circuit Layout and Simulation