WATTMETER DESIGN USING DELTA MODULATION TECHNIQUES

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By

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CERTIFICATE

This is to certify that the thesis entitled, "WATTMETER DESIGN USING DELTA MODULATION TECHNIQUES" submitted by PARTH PRADHAN in partial fulfillments for the requirements for the award of Bachelor of Technology Degree in Electronics & Instrumentation Engineering at National Institute of Technology, Rourkela (Deemed University) is an authentic work carried out by them under my supervision and guidance.

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other University / Institute for the award of any Degree or Diploma.

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CONTENTS

Chapter 1

INTRODUCTION

Instantaneous power in a load is measured by multiplying the voltage across it by the current flowing through it. The multiplication is achieved in a delta sigma wattmeter by using two samplers rather than a multiplier. Sampling and multiplication are closely related. For example, double side-band suppressed carrier modulation can be produced by either multiplying an analogue signal with a sinusoidal carrier, or by sampling the analogue signal with a binary pulse train and filtering these samples. Alternatively these samples can be produced without a sampler if a multiplier is used. This is achieved by multiplying pulse train, whose binary values are arranged to be zero or unity, with the analogue signal.

The delta-sigma wattmeter is given this name because the voltage developed across the load in which the power is to be measured is encoded by a delta sigma modulator, d.s.m into a binary waveform. The d.s.m. decoder is just a low-pass filter.

Chapter 2

LINEAR DELTA MODULATION

2.1 INTRODUCTION

The main objectives of this chapter are to describe the behavior of delta modulator system and to discuss its important characteristics and limitations. It will be shown here that a delta modulator is a non-linear sampled-data closed loop control system which accepts a band limited analogue signal and encodes it into binary form for transmission through a telecommunication channel. At the receiver the binary signal is decoded into a close replica of the original signal.

Before enlarging on the principles of delta modulation it is reasonable to ask if there is any necessity to go through the processes of encoding and decoding, instead of just passing the analogue signal directly. The answer to this question lies in the imperfections of telecommunication channels and their associated terminal equipments. When band-limited continuously varying signals such as speech or television are transmitted over these channels they are degraded by the effect of noise, dispersion and non linearity.

A method of overcoming the deterioration is to encode the continuous message signal at the transmitter into signals which are quantized in both time and amplitude. Suppose that the amplitude of the encoded signal is allowed only two values, i.e. a simple binary code is used. Some error is involved in the encoding process due to quantization of the continuous signal, but under certain conditions this can be made very small. Having transformed the continuous signal into binary one and transmitted it through the channel it arrives at the destination in a distorted form. The receiver observes this distorted binary signal at each sampling instant and answers a simple question: “which binary level does this sample represent? This question is repeatedly asked at every sampling instant and the answer manifests itself as a reformed binary waveform which is then decoded into a continuous signal. If the answer to above questions are all correct this continuous signal is a close facsimile of the original signal encoded at the transmitter, where the only errors which occur are due to the encoding and decoding processes.

Linear delta modulation was first described by Deloraine , Van Miero and Derjavitch in a French patent taken out in august 1946.By the early 1950’s detailed descriptions of delta sigma modulation had been made by de Jager , Libois , van de Weg, Zetterber and others.

2.2 LINEAR D.M SYSTEM

An analogue signal is band-limited by a band-pass filter F1 having critical frequencies fc2 and fc1 , where fc2 > fc1, to form the input signal x(t). The waveform L(t) at the output of the delta modulator consists of pulses of duration τ seconds spaced T seconds apart (T>> τ) having amplitudes of either ±V volts. These pulses occur at clock times, i.e. at a rate fp= 1/T where fp is considerably greater than the Nyquist rate fc2.The delta modulator acts as an analogue to digital converter having an analogue input signal x(t) and binary output signal L(t). The relationship between x(t) and L(t) is such that L(t) is a binary representation of x(t), where the rate of occurrence of each binary pulse is directly proportional to the instantaneous slope of x(t). If the slope is positive then while this condition exists the output L(t) has more positive pulses than negative pulses. The situation is reversed when x(t) has a negative slope.

Figure 2.2 shows how the voltage waveform of a delta modulator varies with time when the input signal is a sinusoid. The pulses comprising the binary output waveform are drawn for convenience having negligible width τ. When these pulses are integrated by the integrator in the feedback network the resulting waveform y(t) consists of steps having magnitude ±γ volts and duration T seconds, which oscillate about the analogue signal x(t) . The difference between x(t) and y(t) is the error signal e(t). This error signal is quantized to limits ±V, which means that the sign and not the magnitude of the error is quantized. The output of the quantizer is sampled every T seconds to produce the L(t) pulses.

If e(t) ≥0 at a clock instant, a positive pulse will be produced at the output of the encoder. When the pulse is integrated y(t) is increased by a positive step. This increase in y(t) will be subtracted from x(t) and a change in the magnitude of the error signal occurs. If the error has not become negative by the next clock instant the output of the encoder will again be a positive pulse. As long as e(t) ≥0 at successive clock instants a sequence of positive pulse will be produced. Eventually y(t) will become greater than x(t) , at a clock instant e(t)<0 , and a negative pulse will occur at the output of the encoder resulting in the diminution in the y(t) waveform by an amount γ. Thus the encoder attempts to minimize the error waveform when an input is present by varying the polarity of the pulses at the output of the modulator at clock instants. When the slope of the sinusoid is large and negative there are more negative than positive pulses generated. The situation is reversed when the slope is large and positive. At the maxima and minima of the waveform where the slope is close to zero there are approximately equal number of positive and negative L(t) pulses. The encoder attempts to generate an L(t) pattern whose mean value approximates to the mean value of the slope of the sinusoid over a short period of time. From period t1 and t2 there are 10 clock periods and the L(t) waveform generates seven positive pulses and 3 negative pulses. The average value of L(t) over this period is 4Vτ/10T. An ideal integrator has an impulse response $h_i(t)$ which equals unity for t ≥ 0 and zero for t < 0. A solitary L(t) generates a step γ=Vτ volts at the output of the integrator. Observe that γ is in volts because the impulse response has the dimensions $(s)^{-1}$. The avergae value of L(t) can now be written as

0.4γ/T. The change in x(t) over the same time interval t1 and t2 is 3γ, and this corresponds to a mean slope of 0.3γ/T which is an approximation to the mean value of L(t). If γ is small and fp is large this approximation is improved. For a period of 10T , from time t3 to t4 , the slope x(t) = 0.1γ/T and the average value of L(t) is 0.2γ/T. However, if the average value is taken from time t5 to t6 the slope of x(t) is still 0.1γ/T but the average value of L(t) is now zero. The average value of L(t) now oscillates about the average slope of x(t). The wide deviations of the average of L(t) about the average of x(t) demonstrate the desirability of minimizing γ provided tracking can be maintained.

2.2.1 DECODER

The decoder in linear d.m. consists of an integrator and a simple filter. Assuming errorless result transmission the L(t) signal is recovered and integrated to give y(t) . This y(t) signal is identical to the feedback to the error point in the encoder. As y(t) only differs from the input signal x(t) by a relatively small error signal e(t) it follows that the signal at the output of the integrator at the decoder is a good reproduction of the error input signal. The step like nature of y(t) is removed by passing the signal through a filter whose frequency bass band is same as the message band f_{c1} to f_{c2}, i.e. filters F_i and F_o may be considered to be identical. Further simplifications may be added to the decoder by making the filter F_o a low pass rather a band-pass one. This is because the noise below f_{c1} is generally not troublesome. The simplicity of the decoder in linear d.m. is one of the attractions, particularly when the integrator can be produced with just a resistor and capacitor.

2.2.2 LOCAL DECODER

Local decoder is used to mean the system which is placed in the feedback path of the encoder. In the linear d.m. it is just an integrator, but in other encoders it can become rather complex. The decoder is a local decoder followed by a band-limiting filter whose main function is to exclude unwanted noise.

2.2.3 ZERO ORDER HOLD

A practical encoder will have a zero order hold circuit following the sampler. This circuit when in receipt of a sample causes its value to be held at a constant amplitude for one clock period. The result is that the L(t) waveform now consists of binary levels which may or may not change at clock instants , rather than narrow pulses of duration τ and amplitude ±V. The hold circuit must be used in practice because narrow pulses with their large bandwidth cannot be countenanced for transmission purposes; in addition it's easier to produce binary levels than narrow pulses. The zero-order hold circuit can be placed outside or inside the closed loop. Because a sample and zero order hold circuit can be implemented with a D-flip-flop it is usual to

place the zero order hold circuit in the feedback loop. This results in y(t) changing from a waveform with steps to one with ramps and this might intuitively lead one to expect a significant reduction in the error signal. Although the presence of sample and hold circuit does effect the shape of the spectrum of the distortion components in the signal y(t) at the output of the local decoder it only has a negligible effect on the distortion components which reside in the message band and are passed by the final filter F_o. Consequently the signal to noise ratio at the output of the decoder is, to a close approximation , is same irrespective of whether the linear d.m. codec generates narrow binary pulses or contains a sample and hold circuit. Generally, the discussion of the various delta modulation systems will be made assuming that the encoder generates narrow binary pulses or impulses, although the presence of a sample and hold circuit in the encoder will be considered occasionally, as in the case of the exponential d.m. codecs. Irrespective of whether L(t) , the output waveform from the delta modulator, consists of binary pulses or levels it will be processed by the transmitter terminal equipment to a form suitable for transmission. For example, the L(t) waveform may be filtered, amplified and perhaps then used to modulate a carrier waveform.

2.2.4 IDLING BEHAVIOUR

The linear d.m. system (codec) is in its idling state when there is no analogue input signal. In the steady state the binary output signal L(t) is composed of alternate positive and negative pulses resulting in a feedback signal y(t) which is nearly a square wave having a period $2/f_p$ and amplitudes $\pm\gamma/2$. The error waveform is equal to $-y(t)$ as there is no input signal. The result is that the waveform at the output of the quantizer is also a square waveform, having the same frequency as that of the error signal, but with amplitudes $\pm V$. The idling pattern of the linear d.m. system is 1 0 1 0 1 0….. where the logical ones and zeroes refer to the positive and negative pulses of the L(t) waveform respectively.

A feature of this idling pattern is that when an analogue signal is applied, the slope required to produce an all ones pattern has the same magnitude and opposite polarity as the slope which will produce an all zeroes pattern. The encoder is therefore symmetrical . Because the y(t) waveform when idling is as described above its frequency spectrum is composed of lines where the fundamental and therefore the lowest frequency is half the clock rate.

The final filter Fo in the decoder rejects frequencies above the highest frequencies which are expected in x(t) when the latter is applied to the encoder. As the clock rate is greatly in excess of these expected frequencies in x(t), generally by a factor of 10 or more, the waveform y(t) in the idling state is completely rejected by the filter Fo. The result is that when the coder is idling, no signal emerges from the output of the decoder.

When no input is presented to the encoder, it has an oscillatory idling pattern; this doesn't imply an unstable situation, on the contrary, it must be emphasized that the linear delta modulator is very stable. The idling feedback waveform y(t) never increases its magnitude or

changes from a square waveform. If the encoder does have some asymmetry then the waveform y(t) only changes in the prescribed limits. Similarly when an input signal is present the delta modulator always attempts to track this signal, even if the encoder is asymmetrical. This inherent stability of the linear delta modulator has been theoretically verified by Gersho. The presence of a second integrator does cause some instability.

2.2.5 SLOPE OVERLOAD

When the step size γ in the waveform y(t) is reduced , without changing the clock rate , a condition occurs where the feedback voltage y(t) is not always varying about the input signal x(t) . Figure 2.3 shows there are sequence of positive and negative steps in y(t) and the error is now excess of γ. By doubling the amplitude and at the same time halving the frequency of the input sinusoid, the relationship between x(t) and y(t) occur because the slope of the sine wave is unaltered . The slope of x(t) is simply related to the length of the sequence of similar polarity pulses in the waveform L(t), and during these sequences the mean slope of y(t) is a constant. This condition, where the feedback waveform y(t) doesn't always vary about the input signal, i.e. track it , is referred to as slope overload. Generally , slope overload starts when the slope of x(t) is greater than the maximum slope associated with y(t). However, during the condition of slope overload the slope of x(t) may be zero.

The limitations imposed on the sinusoid to prevent slope overload will now be examined. When the overload condition occurs a sequence identical polarity pulses occur at the output of the linear d.m. encoder. Let us assume the feedback waveform y(t) increases by $\gamma = V\tau$ volts per clock period. The maximum rate of increase of y(t) is

$$\xi = \gamma/T = \gamma f_p$$

For an input waveform

$$x(t) = Es \sin 2\pi fst$$

$$x'(t) = Es2\pi fs \cos 2\pi fst$$

The condition of slope overload is generally avoided if

$$Es2\pi fs \leq \gamma fp$$

The overload characteristic is a graph of the maximum value Esm of ES in decibels against $\log_{10} fs$, which avoids overloading the delta modulator. A delta modulator cannot encode high

frequency sinewaves without evoking a slope overload condition unless the amplitude is restricted. High frequency signals can of course be accommodated by increasing the product γf_p .

2.2.6 AMPLITUDE RANGE

The maximum amplitude E_{sm} of the input sinusoid which doesn't overload the encoder is given by the expression:

$$E_{sm} = \gamma f_p / 2\pi f_s$$

When idling the waveform y(t) at the output of the integrator is square with a peak to peak value of γ. In order to disturb this idling square wave the input sinusoid must have an amplitude $\geq \gamma/2$. When Es is just greater than $\gamma/2$, the encoder is virtually incapable of tracking the input signal , and the decoded output has severe distortion. The greater E_s becomes relative to $\gamma/2$ the better the tracking, the minimum value of E_s which gives an acceptable decoded signal-to-noise ratio is clearly a subjective choice. The ratio of E_{sm} to this value of E_s is referred to as the dynamic range , DR, of the input. However, an amplitude range , AR, will be defined which is the ratio of the value of E_s which overloads the encoder , i.e. E_{sm}, to the value of E_s which just disturbs the idling pattern, i.e. $\gamma/2$. Hence

$$AR = f_p / \pi f_s$$

AR is maximized by ensuring that at f_{c2}, the highest frequency to be encoded, $f_p >> f_{c2}$. This illustrates that the bit rate for a delta modulation must be in excess of the Nyquist rate for a tolerable AR.

DELTA SIGMA MODULATION

The linear delta sigma modulator is composed of a delta modulator preceded by an integrator i.e. delta modulator encodes the integral of the input signal x(t). The waveform at the output of the decoder in delta modulator tracks the integral of x(t) with some error e(t). The recovery of x(t) therefore involves the addition of a differentiation to the decoder to compensate the extra integrator placed before the input to the encoder , and a low pass filter to reduce the effects of quantization. As the integrator and differentiator in the decoder are complimentary they can be removed to produce a decoder which is simply a sharp cut-off low pass filter. The two integrators can be replaced by one integrator placed after the error signal because

$$\int x(t)dt - \int L(t)dt = \int e(t)\,dt$$

Chapter 3

EXPONENTIAL DELTA SIGMA MODULATION

3.1 INTRODUCTION

The **Delta-Sigma** (ΔΣ) modulation is a method for encoding high resolution signals into lower resolution signals using pulse-density modulation. This technique has found increasing use in a range of modern electronic components, such as analog to digital and digital to analog converters, frequency synthesizers, switched mode power supplies and motor controls. One of the earliest and most widespread uses of delta-sigma modulation is in data conversion. An ADC or DAC circuit which implements this technique can easily achieve very high resolutions while using low-cost CMOS processes, such as the processes used to produce digital integrated circuits. The principle of the ΔΣ architecture is to make rough evaluations of the signal, to measure the error, integrate it and then compensate for that error. The mean output value is then equal to the mean input value if the integral of the error is finite.

3.2 EXPONENTIAL DELTA MODULATION SYSTEMS

In the exponential delta modulation system described by Johnson perfect integrators are replaced by an RC circuit. A sample and hold circuit in the form of a D-type flip-flop is introduced after the quantizer. This means that the output consists of binary levels rather than pulses. The encoder is shown in figure 3.1. The input voltage to RC circuit shown in this figure is the voltage at the output of the sample and hold circuit, i.e. L(t), which has binary levels of ±V. These levels may or may not change at sampling instants depending on whether there has been a change of the error signal at these instants. If a perfect integrator rather than an RC is used in the encoder the y(t) waveform is composed of straight lines which have either positive or negative slopes of equal magnitude. The polarity of these slopes only change when the binary levels of L(t) change. When an RC circuit is used, the shape of y(t) becomes exponential, hence the name for this type of encoder. When a perfect integrator is used in the feedback loop of the encoder a continuous sequence of ones at its output results in a constant rise in y(t). Further, there is no limit to the rise of y(t). However, the same continuous sequence of one's applied to an RC circuit causes y(t) to rise exponentially to the voltage representing logic one , i.e. to V. Thus

when encoding, the increase or decrease in y(t) following a change in the binary level of L(t) depends on the actual value of y(t).

Consider the value of y(t) to be positive at a value close to +V just prior to a sampling instant. If L(t) becomes a logic one y(t) will increase and if L(t) becomes a logic zero it will decrease. If the changes in the values of y(t) are compared one clock period later the negative change is larger than the positive change. This is because the capacitor C has a voltage difference which is small when L(t) is a logic one but large when L(t) is a logic zero ; the change in y(t) is a function of the difference between the voltage to which the capacitor is being charged and the actual voltage on the capacitor.

It is now apparent that by replacing a perfect integrator by an RC circuit in the feedback loop the values of y(t) are more difficult to estimate. Further the amplitude range and overload characteristics are modified. The RC circuit of figure 3.1 has the transfer function

$$H(j2\pi f) = \frac{1}{1+j2\pi fCR}$$

Putting

$$f1 = \frac{1}{2\pi RC} = \frac{1}{2\pi T1}$$

$$H(j2\pi f) = \frac{f1}{f1+jf}$$

And for input frequencies f, where f >> f1

$$H(j2\pi f) \cong \frac{f1}{jf1}$$

As the transfer function for a perfect integrator is 1/(2πf) it follows that , except for a scaling factor, above eqn., is the equation of a perfect integrator. Thus if f1 is chosen to be smaller than the lowest input frequency, fc1, to be encoded then the RC circuit performs as an integrator and y(t) is composed of straight line segments. However, exponential variations in the y(t) waveform can be an advantage in the presence of transmission errors.

3.1 IDLING CHARACTERISTIC OF EXPONENTIAL D.M. CODEC

Consider the situation when the power is first switched on to the encoder and there is no input signal. The voltage at the output of the encoder will either go to +V or –V. Suppose it initially goes to –V; the capacitor C will start to change from 0 to –V and when subtracted from x(t), which is zero, will produce a large positive error signal. This will cause L(t) to switch to +V and y(t) to start to charge to this positive value. Provided y(t) is positive by the next sampling

time, thereby ensuring that the error is negative, L(t) will switch to –V . However, if y(t) is still negative at next sampling instant L(t) will maintain a voltage of +V. Eventually y(t) will go positive at a sampling instant and L(t) will have a negative level –V. After a settling down time L(t) will acquire a …1 0 1 0 1 0 1 0….idling pattern. This will occur irrespective of the initial polarity of the L(t) signal.

The RC circuit has time constant much greater than the sampling period thereby ensuring that it behaves similarly to a perfect integrator, i.e. maintaining y(t) close to zero at all times when idling . Consequently, there is negligible difference in the idling situation between the linear delta modulator and the exponential delta modulator. However, the effect of the sample and hold circuit means that L(t) is a square waveform and y(t) is a small triangular waveform.

The time constant T1, is often tens or hundreds of sampling periods. T1 is found by drawing tangent at the origin of the y(t) curve to intersect the aiming potential V; T1 is the time between the origin and this intersection. By applying the properties of similar triangles,

$$\frac{D}{T/2} = \frac{V}{T1}$$

Then, $$D = \frac{\pi V f1}{fp}$$

Effects of propagation

Practical quantizers require a minimum value of input amplitude in order to produce the voltage ±V. They are also limited in frequency response, and conventional operational amplifiers cannot operate as quantizers at bit rates above say, 10Mbits/s. At these high bit rates the comparator in D-flip-flop can be used as the quantizer. This flip-flop must not have too high a propagation delay or the establishment of the required…1 0 1 0 1 0 ….idling pattern will be prohibited. This can be demonstrated as follows.

Suppose the minimum value of D which causes the flip flop to function is $\pm d$, i.e. the error > |d| at a clock instant for L(t) to be ±V. Let the propagation time of the flip flop be τ_p , i.e. τ_p seconds after the clock has been applied the L(t) level changes. The result is that the y(t) waveform has the same shape but is moved to the right τ_p seconds. The clock samples q(t) when e(t) is less than |D| , although e(t) continues to increase in value. As the slope of e(t) is $\pm 2Df_p$ it is easy to show by similar triangles that when e(t) is sampled its magnitude is $D(1-2f_p\tau_p)$. This idling waveform e(t) is maintained until the clock is increased above $(D-d)/(2\ \tau_p\ D)$ when the output binary pattern becomes …..0 0 1 1 0 0 1 1….. and e(t) has peak to peak values of ±2D. In order to restore the …..1 0 1 0 1 0 …. Pattern a flip flop having a low τ_p should be selected and f_1 made as high as the restrictions on amplitude range permit.

3.2 OVERLOAD CHARACTERISTICS

If the slope of the input signal becomes greater than the maximum rate of increase in the feedback signal y(t) the encoder is overloaded. In the case of exponential delta modulator the maximum rate of increase in y(t) is exponential.

Suppose the input signal x(t) is a sine wave Essin2πfst. The question to be answered is for what value of Es will cause the encoder to be overloaded. Now the slope of x(t) w.r.t. is

$$x'(t) = E_s 2\pi f_s cos 2\pi f_s t = 2\pi f_s [E_s^2 - E_s^2 sin^2 2\pi f_s t]^{\frac{1}{2}}$$

$$= 2\pi f_s [E_s^2 - x^2(t)]$$

Assuming that the encoder is tracking correctly the instantaneous value of y(t) i.e. the voltage across the capacitor C, closely approximates to x(t). When x(t) is increasing monotonically with time y(t) changes exponentially and its slope is the voltage difference between the aiming potential V and the voltage x(t) on the capacitor divide by the RC time constant T1, i.e.

$$\{V - x(t)\}/T_1$$

The difference in slopes between the signals y(t) and x(t) is

$$\Delta = \frac{V - x(t)}{T_1} - 2\pi f_s [E_s^2 - x^2(t)]^{1/2}$$

When x(t) is decreasing monotonically the slope of y(t) is

$$\frac{-(V - x(t)}{T_1}$$

and the slope of x(t) is negative.

Δ is seen to be a function of x(t).Providing the sloe of y(t) remains greater than the slope of x(t) the overload condition is avoided. To find the value of x(t) which just causes slope overload we find the value of x(t) for which Δ is a minimum, i.e. the value of the instantaneous value for which the two slopes are nearly equal, and equate Δ to zero.

Differenciating above expression for Δ w.r.t. x(t)

$$\frac{d\Delta}{dx(t)} = -\frac{1}{T1} + 2\pi f_s x(t)\{E_s^2 - x^2(t)\}^{-1/2} \qquad \text{(A)}$$

Putting eqn. A equal to zero gives

$$x(t) = \frac{E_s}{\{1+(2\pi f_s)^2 T_1^2\}^{-1/2}} \qquad \text{(B)}$$

If $\frac{d^2\Delta}{dx^2(t)}>0$ for x(t) , then Δ is a minimum.

$$\frac{d^2\Delta}{dx^2(t)} = 2\pi f_s[E_s^2 - x^2(t)]^{-1/2}[1 + x^2(t)\{E_s^2 - x^2(t)\}^{-1}] \qquad \text{(C)}$$

Substituting the value of x(t) from (B) into (C) gives

$$\frac{d^2\Delta}{dx^2(t)} = \frac{\{1 + (2\pi f_s T_1)^2\}^{3/2}}{E_s(2\pi f_s)^2 T_1^3} > 0$$

Then, $\Delta_{min} = \frac{V}{T_1} - \frac{E}{T_1}\{1 + (2\pi f_s)^2 T_1^2\}^{1/2}$

Putting Δ_{min}=0, where $E_s = E_{sm}$, $E_{sm} = \frac{V}{\{1+(2\pi f_s T_1)^2\}^{1/2}}$

The overload characteristic gives the values of amplitude E_{sm} for each frequency to avoid the overload condition. Overload is avoided if value of Es for a given frequency fs is below the characteristic: it can be seen that for fs <<f1, Es can be as large as V before overload occurs. Also for these low frequencies overload is independent of frequency. At higher frequencies, f>>f1, the RC circuit behaves as a perfect integrator and the max value of E_s, i.e.E_{sm}, decreases with frequency. The value of E_{sm} has been found to be independent of clock rate, but for the delta modulator the value of E_{sm} can always be increased by increasing the clock rate fp.

3.3. AMPLITUDE RANGE

The amplitude range AR is defined as

$$AR = \frac{E_{sm}}{D}$$

Where Esm and D are as defined above.

Chapter 4

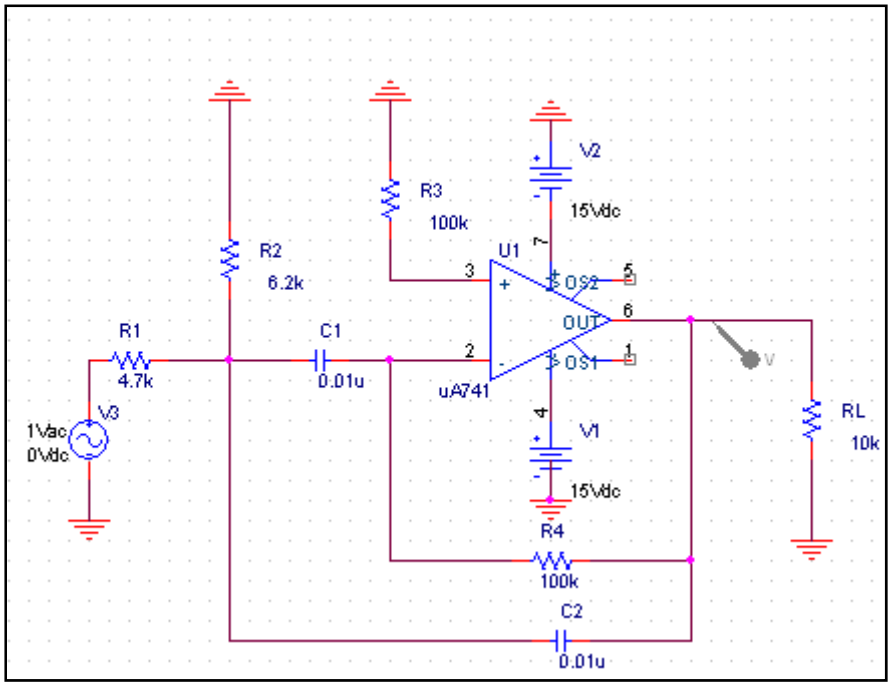
COMPONENTS DESIGN

4.1 BAND-PASS FILTER

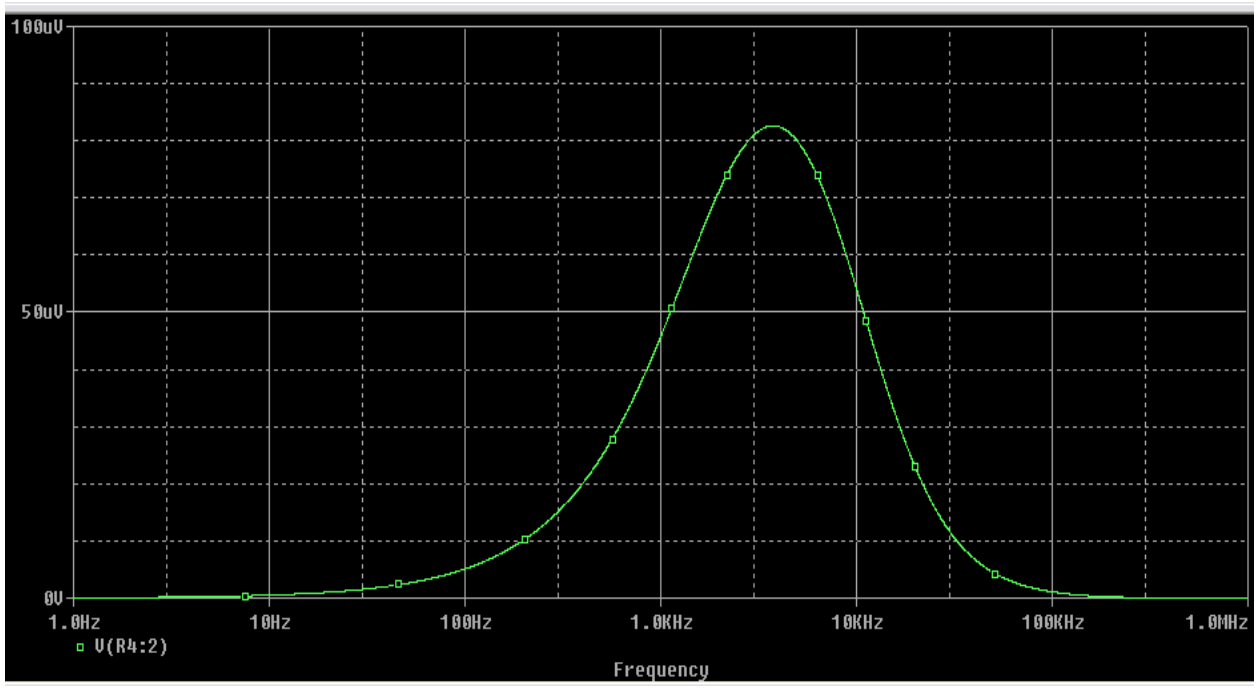
The narrow band pass filter uses only 1 op-amp.This filter is unique in the following respects:

- It has two feedback paths, hence the name multiple-feedback filter.
- The op-amp is used in the inverting mode.

An advantage of multiple feedback filter is that its center frequency fc can be changed to a new frequency fc` without changing the gain or bandwidth.



Band-pass filter with center frequency fh



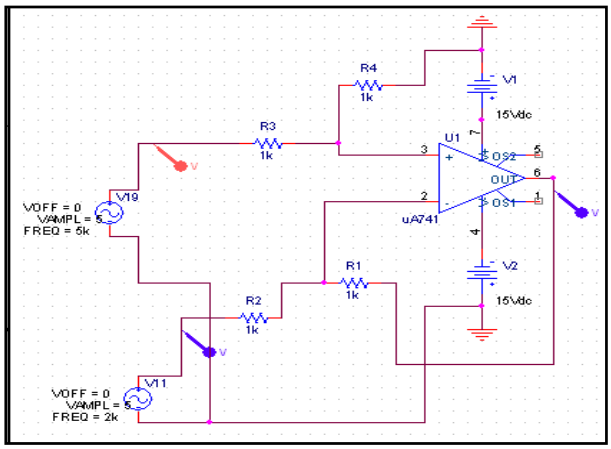
4.2 OP-AMP AS SUBTRACTOR

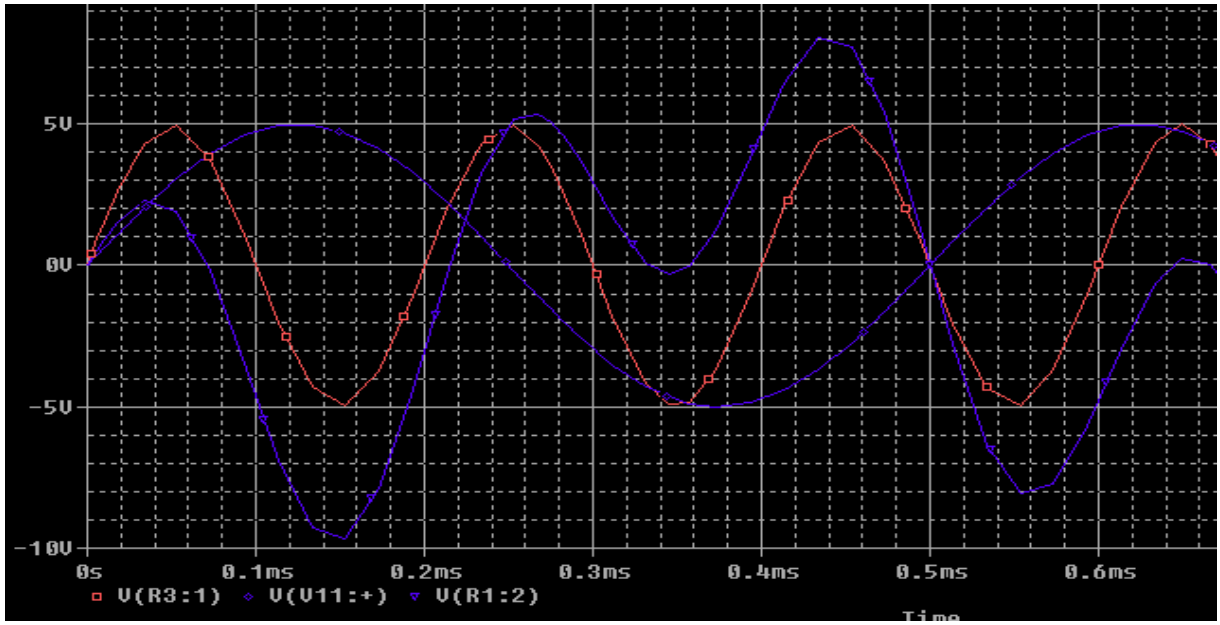
A basic differential amplifier can be used as a subtractor . In the schematic below, input signals can be scaled to the desired values by selecting appropriate values for the external resistors. When all the resistors are equal in value, the gain of the amplifier is equal to 1. From the figure , the output voltage of the differential amplifier with a gain of 1 is

$$V_o = -\frac{R}{R}(V_a - V_b)$$

That is, $V_o = V_b - V_a$

Thus, the output voltage V_o is equal to the voltage V_b applied to the non-inverting terminal minus the voltage V_a applied to the inverting terminal; hence the circuit is called a *subtractor*.





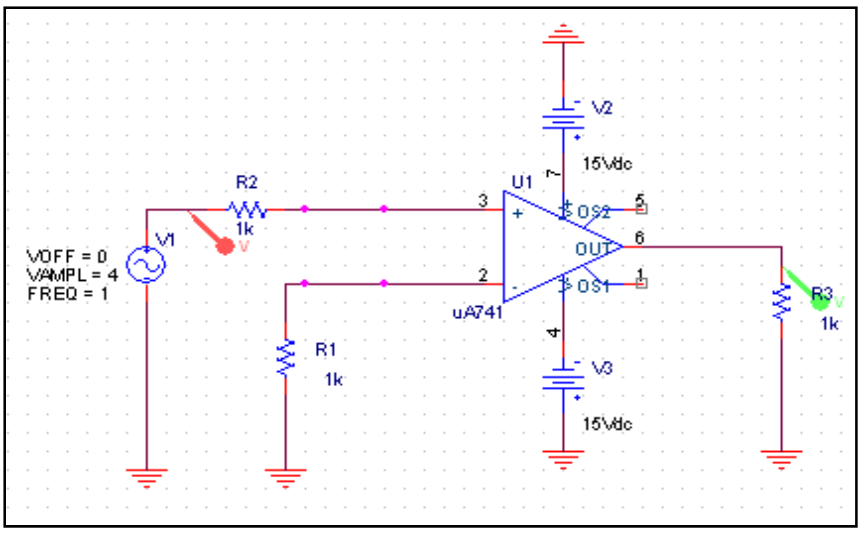
1. A subtractor circuit 2. Input and output waveforms

4.3 OP-AMP AS COMPARATOR/ 1 BIT QUANTIZER

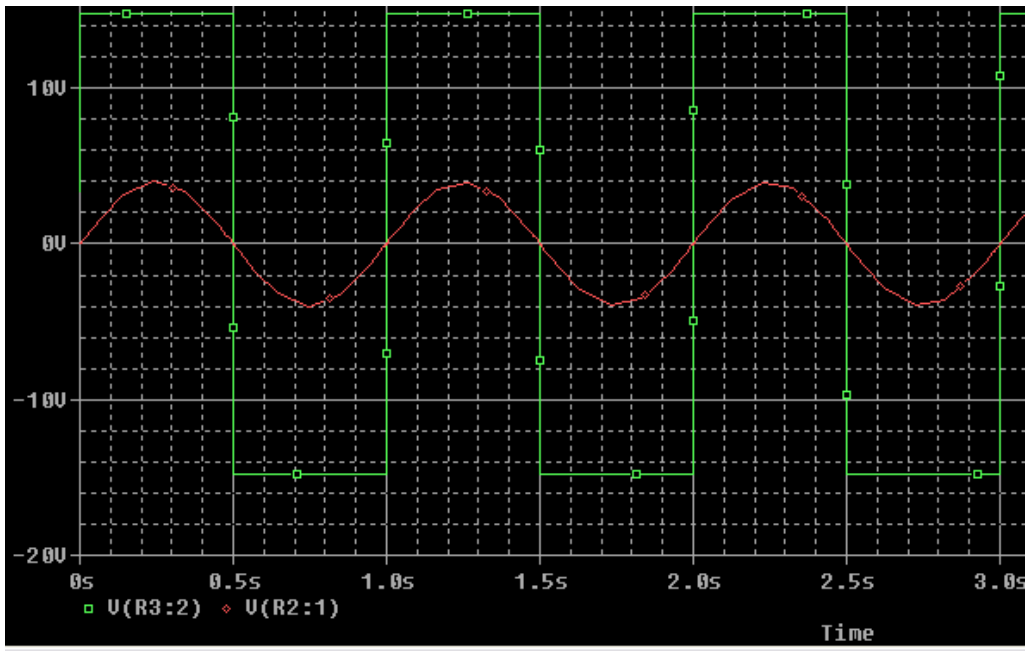
A comparator, as its name implies, compares a signal voltage on one input of an op-amp with a known voltage called the reference voltage on the other input. In its simplest form, it is nothing more than an open-loop op-amp, with two analog inputs and a digital output; the output may be (+) or (-) saturation voltage, depending on which input is the larger.

Zero crossing detector

An immediate application of the comparator is the zero-crossing detector. The basic comparator can be used as the zero-crossing detector provided that V_{ref} is set to zero (V_{ref} =0). The output V_o is driven into negative saturation when the input signal $\boldsymbol{v}_{in}$ passes through zero in the negative direction. Conversely, when $\boldsymbol{v}_{in}$ passes through zero in the positive direction, the output v_o switches and saturates positively (here V_{ref} is applied to negative terminal of the op-amp).



1.Zero crossing detector 2. Input and output waveforms



4.4 D-FLIP FLOP AS SAMPLE AND HOLD CIRCUIT

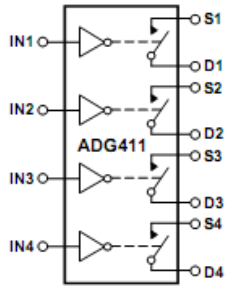
D flip-flop has only one input referred to as D-input or data input.

INPUT D_n	OUTPUT Q_{n+1}
0	0
1	1

This is equivalent to saying that the input data appears at the output at the end of the clock pulse. The output will be in the form of binary levels rather than pulses.

4.5 ADG411 as FET SWITCHES

The ADG411, ADG412 and ADG413 are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC2 MOS process which provides low power dissipation yet gives high switching speed and low on resistance. The on resistance profile is very flat over the full analog input range ensuring excellent linearity and low distortion when switching audio signals.



VDD -Most positive power supply potential.

VSS -Most negative power supply potential in dual supplies. In single supply applications, it may be connected to GND.

VL -Logic power supply (+5 V).

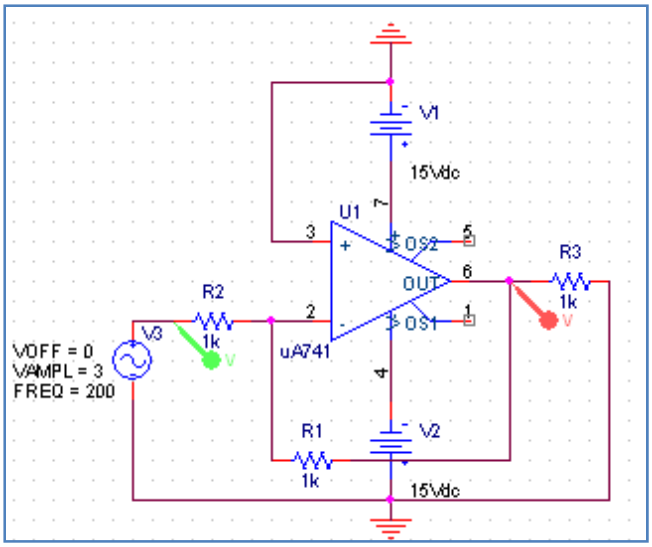
GND- Ground (0 V) reference.

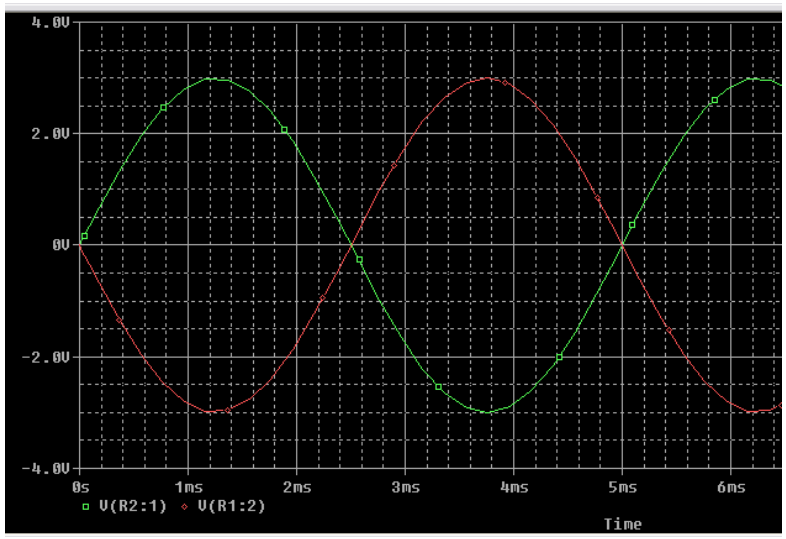
S -Source terminal. May be an input or output.

D -Drain terminal. May be an input or output.

4.6 OP-AMP AS INVERTER

If we need an output signal equal in amplitude but opposite in phase to that of the input signal , we can use the inverter. The inverting amplifier works as an inverter if R1= Rf(feedback resistor).





1. Inverter circuit 2. Input and output waveforms

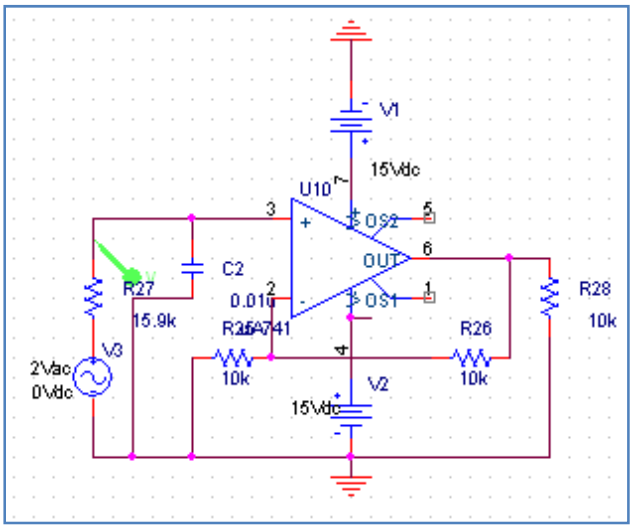
4.7 OP-AMP AS LOW PASS FILTER

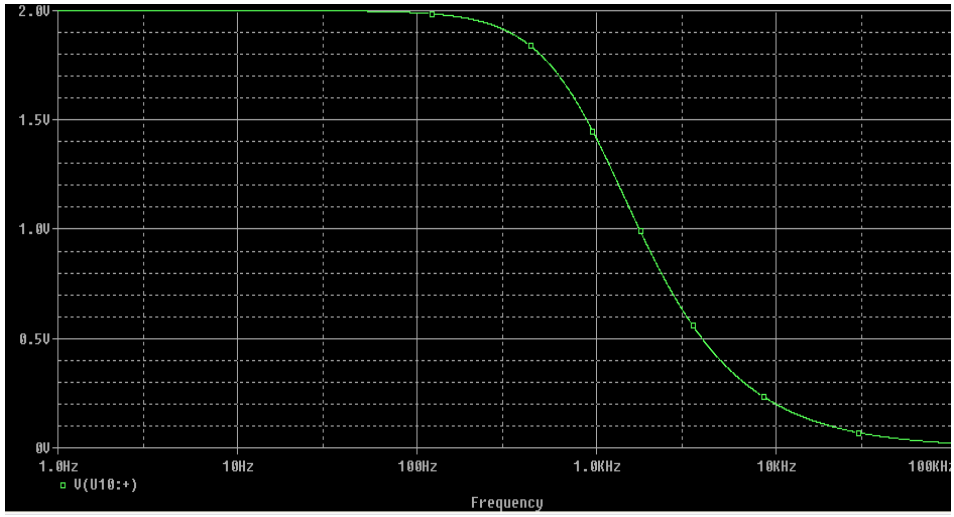
The low pass filter used in this design is a first order low-pass Butterworth filter that uses an RC network for filtering. The op-amp is used in the non-inverting configuration ; hence it does not load down the RC network. Resistors R1 and Rf determine the gain of the filter.

According to the voltage divider rule, the voltage at the non-inverting terminal is

$$V_1 = \frac{-jX_c}{R=jX_c} V_{in} \qquad \text{where } j = \sqrt{-1} \text{ and } -jX_c = 1/j2\pi fc$$

$$\frac{V_0}{V_{in}} = \left(1 + \frac{R_f}{R_1}\right)\left(\frac{1}{1+j2\pi fRC}\right)$$





Filter Design

A low pass filter can be designed by implementing the following steps:

1. Choose a value of high cut-off frequency f_H.
2. Select a value of C less than or equal to 1μF.
3. Calculate the value of R using R=$(1/2\pi f_H C)$
4. Finally, select values of R1 and Rf dependent on the desired passband gain A_f using

$$A_f \cong 1 + \frac{R_f}{R_1}$$

Chapter 5

DELTA SIGMA WATTMETER DESIGN

DESCRIPTION

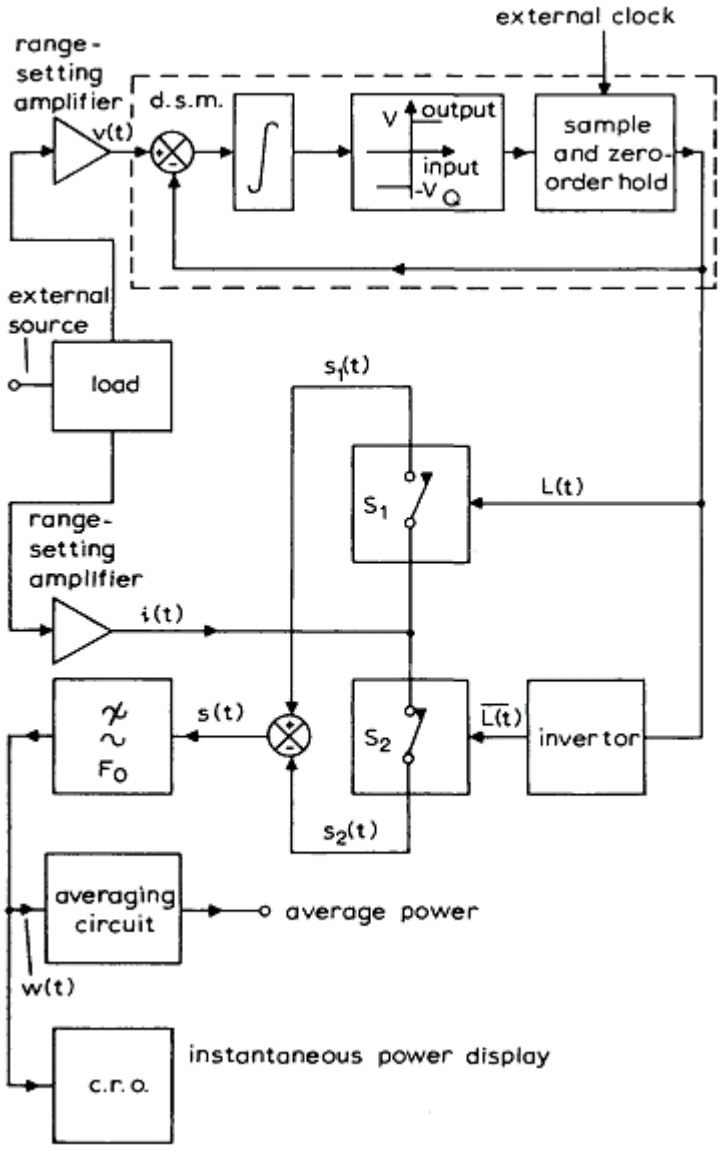
The delta-sigma wattmeter described enables both the instantaneous and mean power in a load to be measured by the utilization of a delta-sigma modulator and junction switching f.e.t.s. Before discussing the wattmeter, it is necessary to review briefly the relevant parameters of the delta-sigma modulator.

The block schematic of a d.s.m. is shown in the dotted lines below. This coder encodes an analogue signal v (t) into a binary waveform L (t) having levels ± V, where the rate of occurrence of each binary level is directly proportional to the amplitude of v (t). The system is so arranged that, when tracking the signal v(t), the input to the quantiser Q makes small variations about a zero threshold level. v(t) can be decoded from L(t) with some distortion by simply passing L{t) through a low-pass filter having a pass-band equal to the spectrum of the input signal.

The w(t) waveform in Fig. below is the product of the two signals i(t) and v(t). Considering the system as an instantaneous multiplier, it is essential that w(t) be zero if i(t) or v(t) is zero. When v(t) is zero, the d.s.m. is in its idle state, where the L(t) waveform is a square wave having a p.r.f. of 1/2 T, where T is the clock period.

The sampling of a waveform is equivalent to multiplication in the time domain. If the L(t) waveform is used to sample i(t), w(t) is proportional to i{t), as the process is essentially pulse amplitude modulation. For w(t) to be zero when v(t) is zero, irrespective of the value of i(t), two samplers S1 and S2 are used. The output of S1 is the current waveform when L{t) occupies its positive level, and S2 provides samples of i(t) when L(t) is zero. The outputs from Si and S2 are subtracted to give the signal s(t). As the sampling rate is several orders greater than the highest frequency fc in the i(t) and v(t) signals, it follows that, by passing the s(t) signal through the lowpass filter Fo, which has a critical frequency equal to 2/c, the resulting w(t) signal is zero. When i(t) is zero, then, irrespective of whether v(t) is present or not, w(t) is zero, as there is no signal for the output of the d.s.m. to sample. When v(t) is encoded by the d.s.m. and i(0 is presented to the samplers, the value of the instantaneous power in the load is proportional to the instantaneous value of the w(t) signal.

The L(t) waveform is no longer a square wave, and its binary changes reflect the instantaneous amplitude of the v(t) signal. For example, if v(t) is sinusoidal, the L{t) waveform will consist of levels + V and — V which are sinusoidally distributed in time. During that part of the cycle where v(t) and i(t) have the same polarity, the s(t) signal is positive, and, when v(t) and i(j) have opposing polarities, the s(t) signal is negative. In designing the wattmeter, the system parameters are implemented as follows.



Delta-Sigma Wattmeter

In the d.s.m., the L(t)` signal is feedback, rather than the L(t) signal, enabling the subtractor to be replaced by an adder. This adder and the integrator in the forward path of the

d.s.m. are achieved in one operational-amplifier circuit. To prevent the output voltage of this operational amplifier from reaching its saturation limit Vs, the condition is that Vs + 2V T/RC must hold, where RC is the time constant of the integrator. This condition applies to the worst case, when the maximum input which the coder can accommodate, i.e. V, is applied just after the instant when L(t) has changed to V, subsequent to the integrator output being just below zero. The sample-and-hold circuit is implemented with a D flip-flop. The D flip-flop also has a comparator associated with its D input. However, to ensure that small values of the signal at the output of the integrator will result in the flip-flop making the correct transition at clock times, it is desirable to introduce an integrated-circuit comparator between the integrator and the flip-flop.

There are two essential setting-up requirements. One is the establishment of a 10101010 . . . L(t) pattern when the input v(t) is zero, and the other is that, when v(t) is at either of its peak values + V or - V, the output pattern must be just all ones or just all zeros, respectively. Two junction-switching f.e.t.s are used as the samplers S1 and S2 because of their zero-offset characteristic. The signal is produced by applying the outputs from samplers S1 and S2 differentially to an operational amplifier. The w(t) signal is conveniently displayed on an oscilloscope subsequent to filtering the s(t) signal.

The mean power in the load can be processed from s(t) and simultaneously displayed by connecting the s(t) signal to a moving-coil micro-ammeter. Of course, this method of detection and display does degrade the accuracy of the wattmeter. The higher the clock rate, the more closely the mean of the L(t) signal follows the mean of the input signal v(t) over a period of time Tm. The difference between the two mean values will at no time exceed plus or minus one pulse of the L(t) waveform of duration T averaged over the period Tm, i.e. TV/Tm.

Expressing this error as a percentage of the maximum signal which the d.s.m. can accommodate, gives

$$e = \pm (T/Tm) * 100\%$$

If Tm is restricted to 1 % of l/fc, it can be shown that the mean value of v(t) or i(t) does not differ from its instantaneous value by more than 0067%. Since this error is relatively small, the mean value of the L(t) waveform over the period Tm is considered to represent the instantaneous value of v(t). Consequently, a clock rate fp of (10^4)*(fc/e) ensures that the 'instantaneous power' w(i) is in error by an amount less than e. The overall error will exceed the system error e, owing to circuit imperfections.

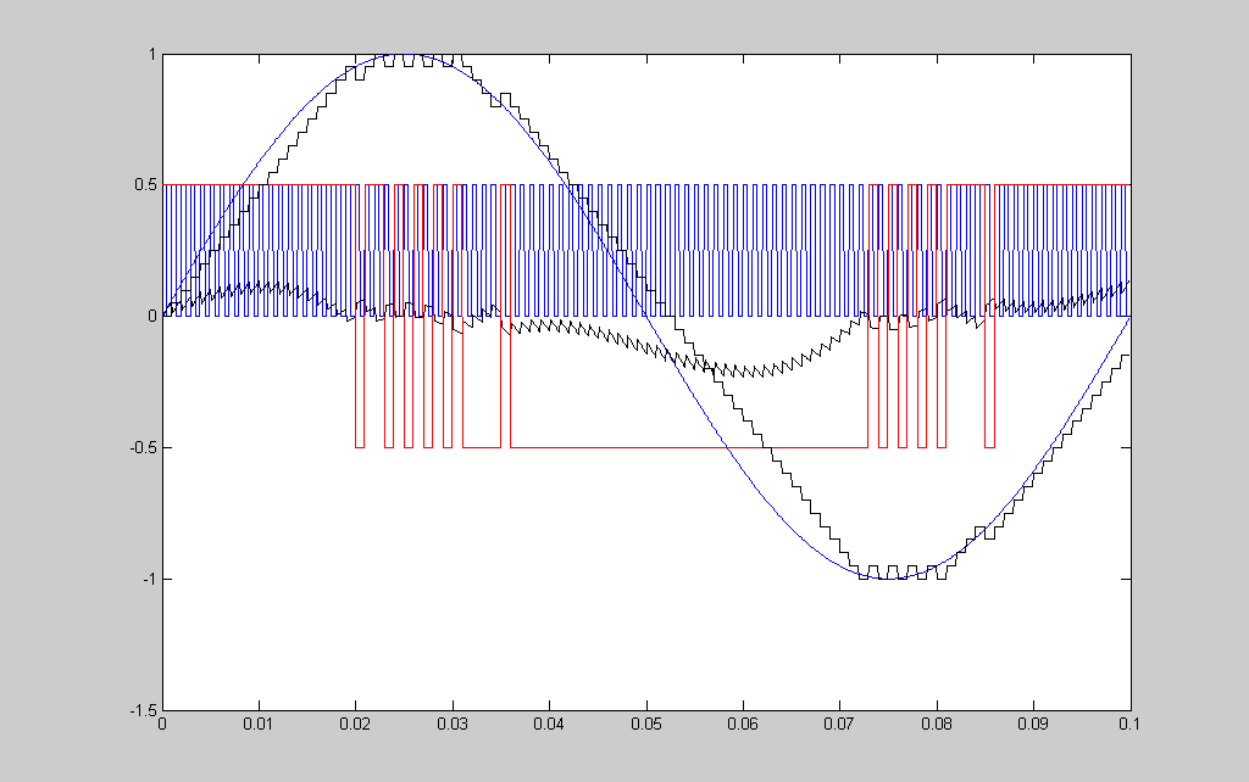
The error e applies to 'instantaneous power'. However, when measuring mean power, the error is less sensitive to clock rate. For example, the authors achieved errors of less than 2 % when measuring mean power in a 50 Hz circuit using a delta-sigma wattmeter in which the clock rate was 5 kHz and the s(t) signal was averaged by a moving-coil instrument.

Chapter 6

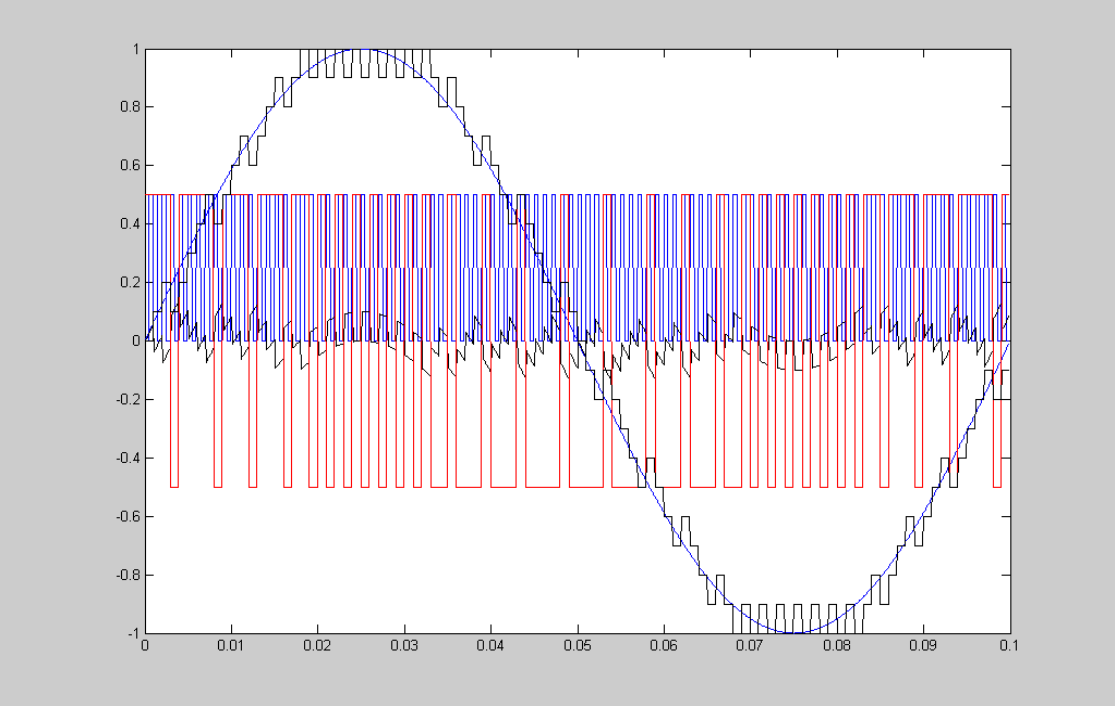
IMPLEMENTATION RESULTS

6.1 MATLAB SIMULATION RESULTS

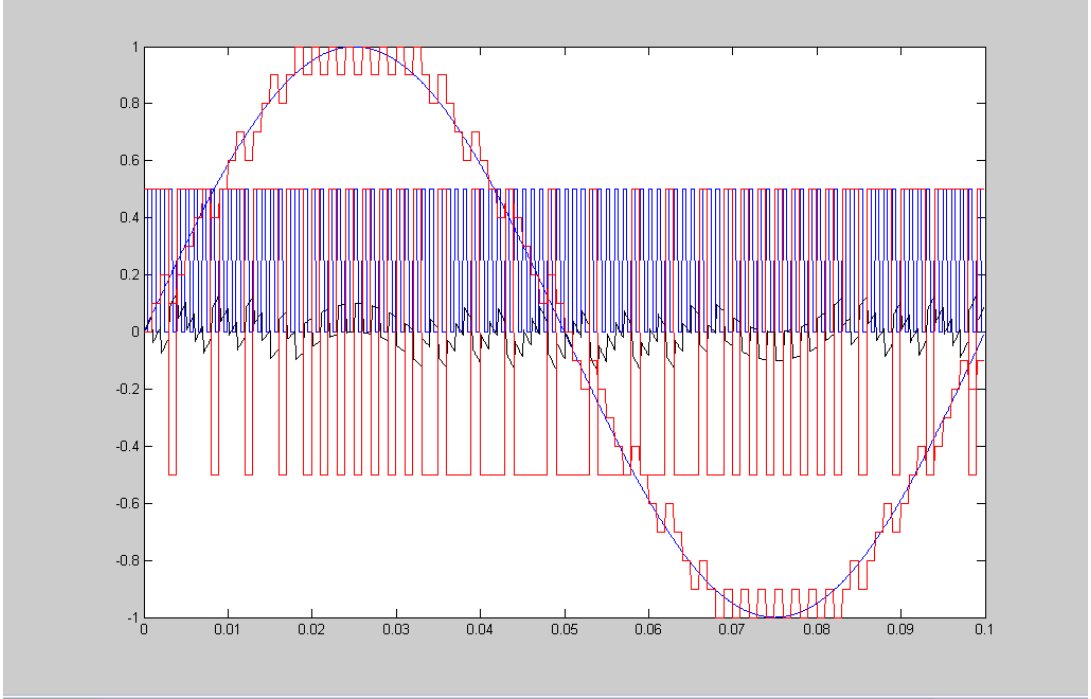
A. Slope Overload characteristic



B. Delta sigma modulator – L(t) waveform to encode input signal x(t)

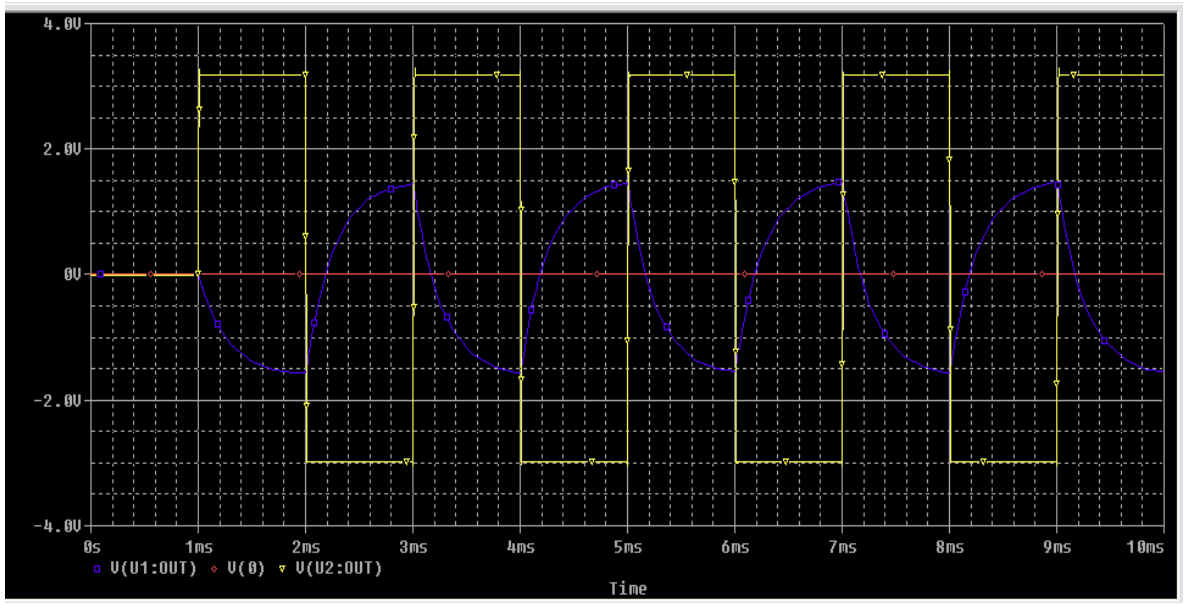


C. Decoded signal in red (reconstruction from binary levels L(t))-decoded

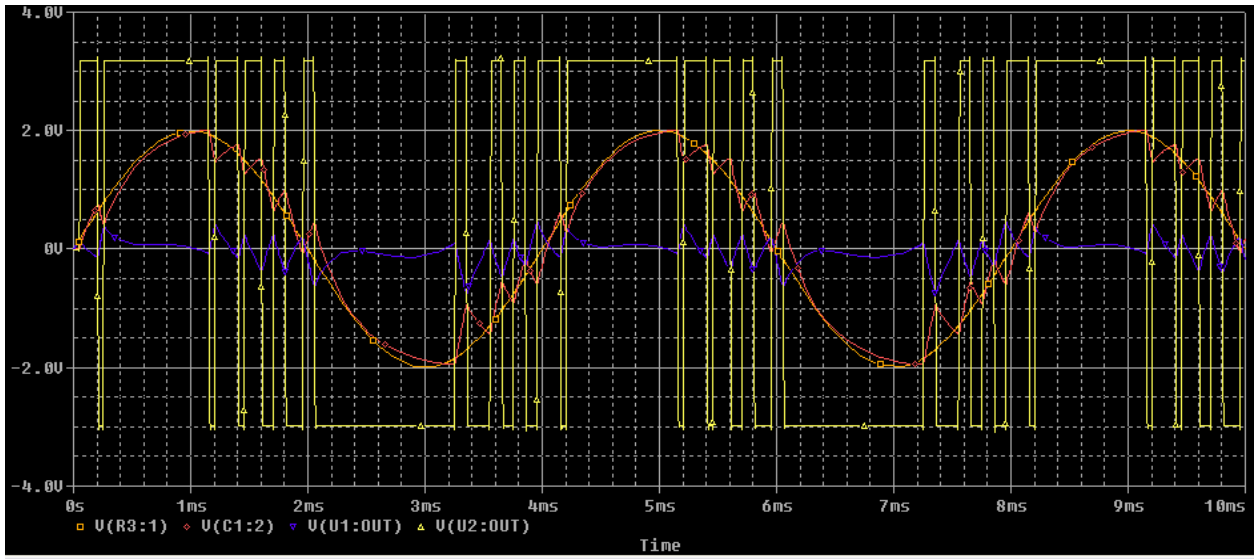


6.2 ORCAD SIMULATION RESULTS

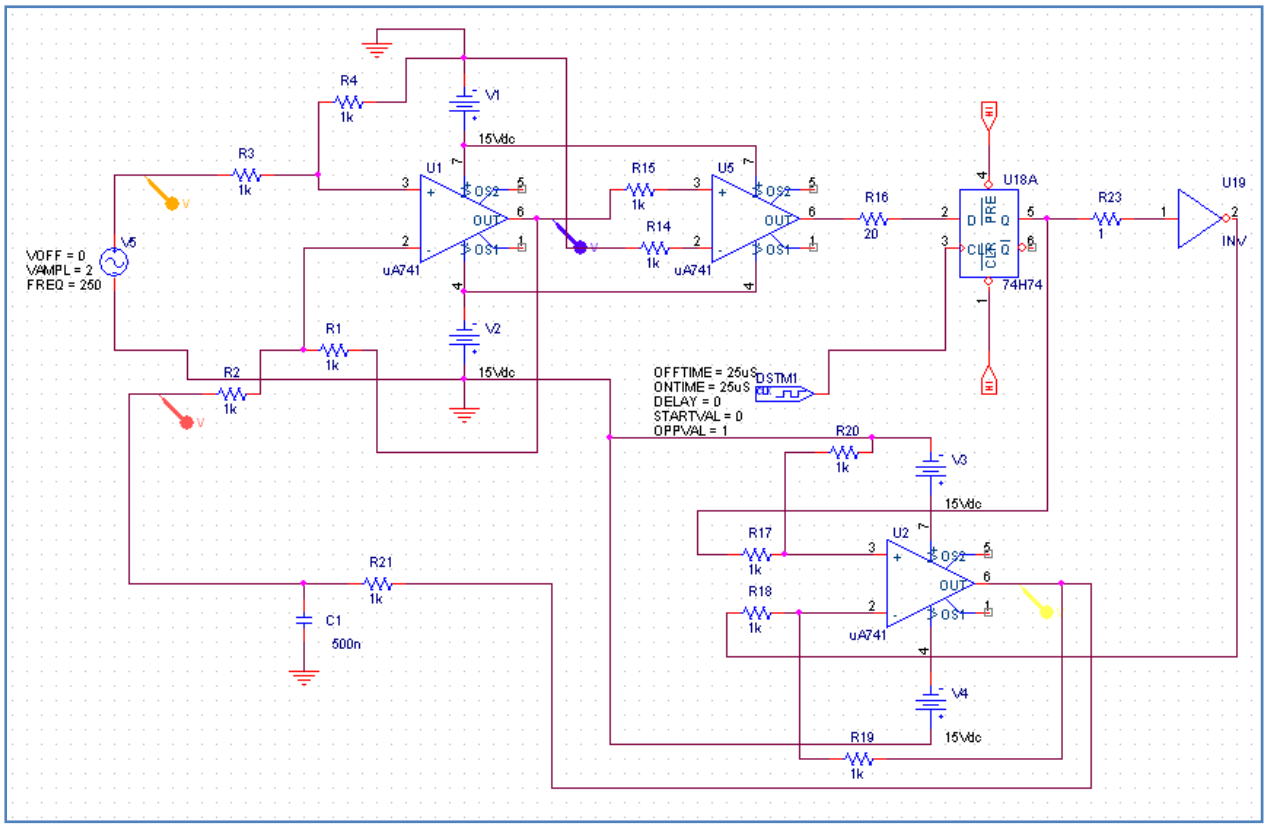
A. Idling behavior of d.s.m. When no input signal is given the binary signal L(t) is composed of alternate positive and negative voltage levels which is nearly a square wave having a period equal to clock period and amplitude ±γ/2.



B. Generation of L(t) waveform . The polarity of the slopes of input signal changes only when the binary levels of L(t) change.



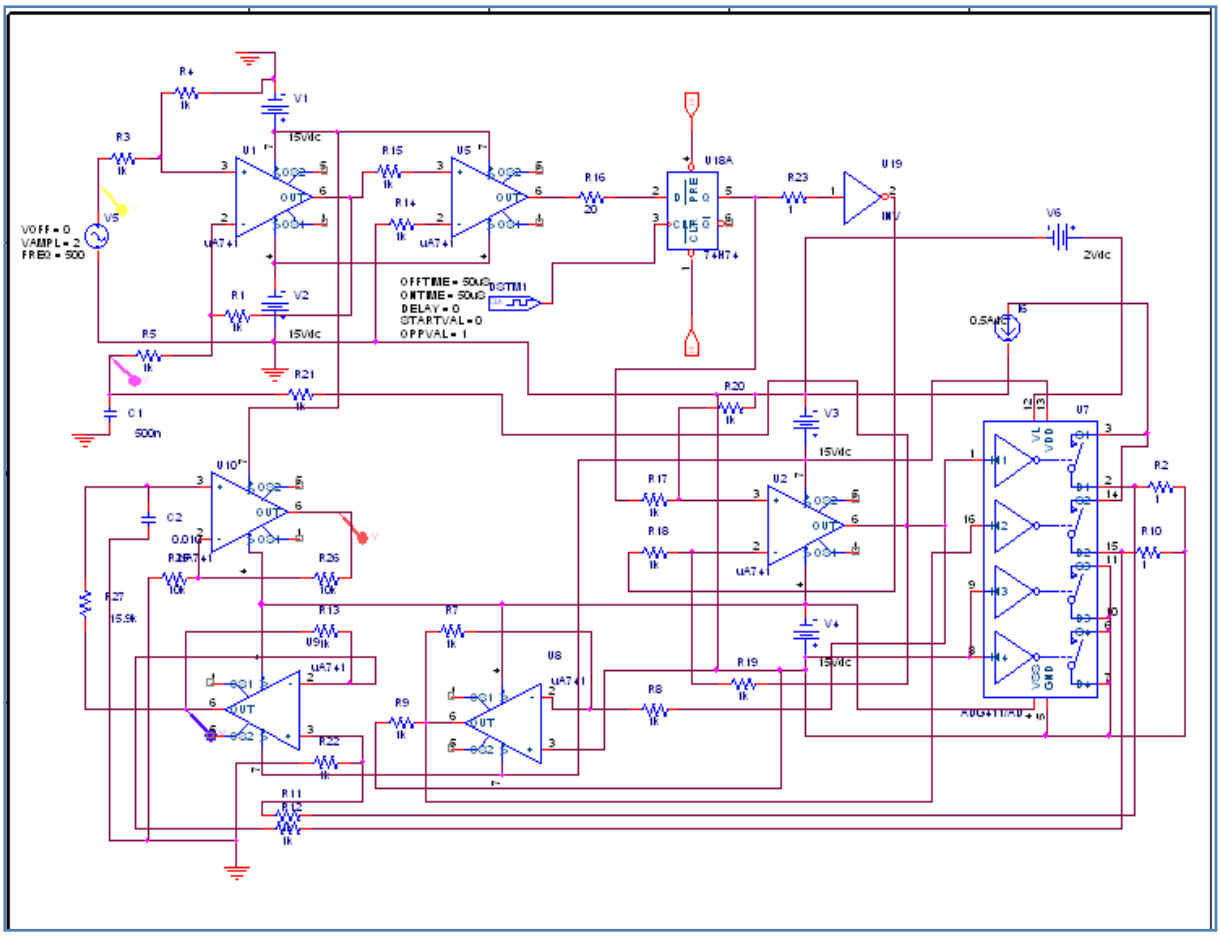
The circuit schematic of Delta sigma modulator.

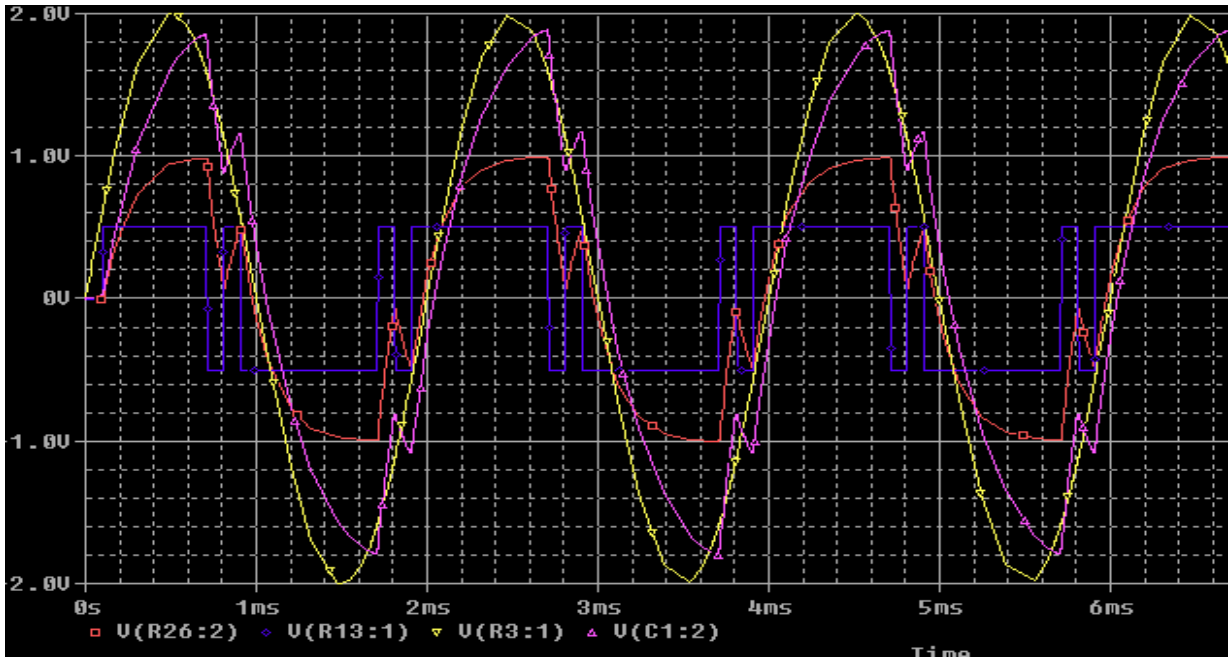


C. Wattmeter Design

- **The input signal is first band-limited by a band-pass filter having critical frequencies f_{c1} and f_{c2}. If the input signal is D.C. voltage, ther is no need of band-pass filter.**
- **A op-amp subtractor is employed to find the error signal between input signal and feedback signal.**
- **The error signal is then fed to the zero crossing detectors so that binary levels representing the sign of error signal is obtained.**
- **The binary level is given to D flip-flop to sample and hold the signal as well as maintain a synchronization of the circuit operation w.r.t. clock period.**
- **The output of the D flip-flop has only high and zero level but the desired L(t) has +V and –V binary levels. So, the D Flip-flop output is passed through a digital inverter which is then subtracted to the output of D flip-flop to get the desired L(t).**
- **The input current (scaled to VI) source is sampled by the L(t) and L(t)` using a switching IC ADG112.The L(t) is inverted by an analog op-amp inverter. The s1(t) and s2(t) are subtracted by op-amp subtractor which is then filtered using a Butterworth first order low pass filter to obtain a signal indicative of the amplitude and sign of the instantaneous power.**

Schematic of wattmeter with the waveforms showing power output.





CONCLUSION

The wattmeter design has been implemented successfully and simulation results were found to be correct. The MATLAB simulation was done to study the functioning of delta sigma modulator and then the schematic of the circuit was prepared in P-SPICE (Orcad).Critical errors were encountered during A/D conversion but it was sorted out. The hardware was also constructed which worked fine. It can measure both A.C. and D.C. signal power. The delta sigma wattmeter can be made with common electronic components and hence is cheap and reliable.

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[3] STEELE, R.: 'Pulse delta modulators—inferior performance but simpler circuitry', Electron. Eng., 1970, 42, pp. 75-79
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