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HIGH PERFORMANCE MICROPROCESSOR SYSTEM FOR EDDY CURRENT DEFECTOSCOPE MEASUREMENT SIGNAL PROCESSING

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This article shows principles of development of the eddy current defectoscope data acquisition system. It describes goals of development of this system and main requirements for its characteristics. Also on basis of these requirements possible implementation of the device was suggested.

Key words:
Eddy current defectoscope, data acquisition and processing system, multichannel measurement, digital signal processing.

A new method of eddy current testing for steel tubes and pipes was developed at the department of Information-measurement techniques. This method increases the effectiveness of inspection by using circular and lengthwise multifrequency eddy currents. To analyze the method, researchers created the experimental eddy current testing system.

The eddy current testing system consists of an eddy current transducers module; module of electronics, which purpose is to generate signals for eddy current transducers (ECT) and to provide an analog front end; data acquisition board “NI USB 6363”; a personal computer, which provides digital processing and visualization functions.

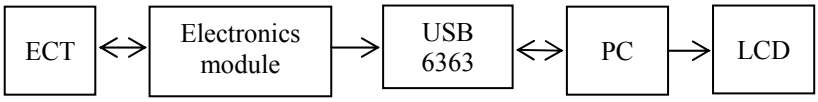

Fig.1. Block diagram of the experimental eddy current testing system

The results of an experiment were positive; therefore, it was decided to develop a completely self-sufficient device not dependent on an external data acquisition module and personal computer to process and visualize measurement data.

It will allow improving some characteristics of the eddy current testing system, which are limited mostly by the external data acquisition module «NI USB-6363», decrease overall cost of the system (USB-6363 alone costs around 2500$) and, in perspective, commercialize this device.

Electronics module used in the experimental device doesn’t require any amendments. Nevertheless it is necessary to develop a circuit, which will perform such functions like signal discretization, processing and visualization. These functions in the experimental device are performed by the data acquisition board and a PC. The circuit must provide the following characteristics:

-multichannel data acquisition (18 channels);
-complex digital processing;
-VGA/DVI video output;
-interfacing to PC through the standard high speed interfaces (either USB, Ethernet or PCI-E);
-possibility of saving test data.

Taking above into consideration it is possible to suggest a block diagram of a module responsible for data acquisition, processing, visualization and interface.

The system consists of multichannel ADC, CPU, LCD and keyboard.

ADC REQUIREMENTS AND CHOICE

Since the frequency of signals to be measured is relatively low and also there is no need for synchronous data acquisition, it is preferable to use one ADC with a multiplexer instead of multiple ADC’s or a multichannel simultaneous sampling ADC.

There is a possibility to simplify the development work by the use of a multichannel ADC in an integrated circuit form. It will allow us not only to save a space on a printed circuit board, but also to improve metrological characteristics of the circuit.

Processor choice mainly depends on a sampling rate of an ADC, processing method (sample by sample or frame by frame), DSP algorithm complexity and also visualisation complexity. Inasmuch as the algorithm allows only frame by frame processing, there is no need for very powerful DSPs. The whole signal can firstly be recorded and only then processed, so there are no strict frames for processing time. But the fact that there are no strict time frames doesn't mean that there are no frames at all. The processing time t_{pr} needs to be not more than the acquisition time t_{aq} in order to ensure continues inspection. To meet this requirement the sampling rate must not be very high. Because the higher sampling rate is, the more samples are acquired. A high number of samples leads to increase in the processing time. At the same time the sampling rate affects quantization error. For example, to reproduce a signal with the quantization error $\sigma_d = 0.2\%$ the following frequency is required:

$$f_s = (30 \div 40) f_c$$

where f_c –frequency after which begins a sharp decrease of the spectral component amplitudes;. f_s – sampling rate.

Experiments have shown that f_c is approximately equal to 200 Hz. Hence, in order to provide quantization error $\sigma_q = 0.2\%$ sampling frequency must be at least 6 KHz. In the experimental eddy current testing system sampling rate equals 15 KHz per channel. This value has proven to be well suited for this purpose, therefore it is necessary to use the self-same frequency in the new data acquisition and processing module.

For example, one of the ADCs suitable for this device is 11-channel TLV 2556-EP which is produced by Texas Instruments™. Main characteristics of TLV 2556-EP are:

-11 channels;
-12 bit resolution;
-18.1 ksps/channel;
-SPI interface.

Inasmuch as the number of channels of this ADC is only 11, it is required to use 2 ADCs in order to meet the number of channels requirement.

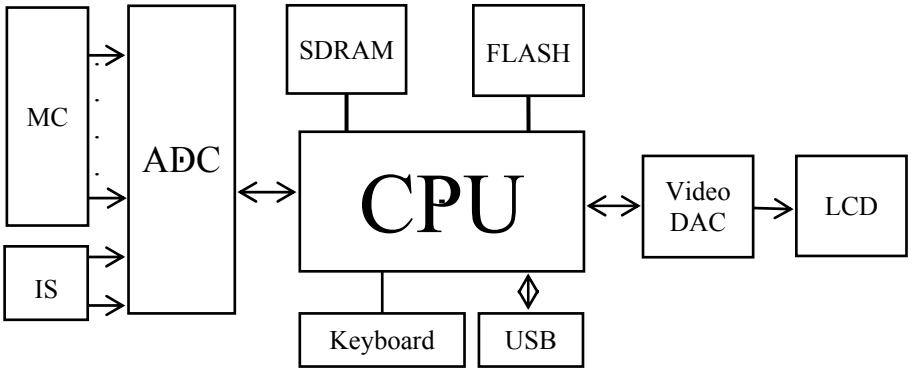

Fig.2. The block diagram of the DAQ module. IS – induction sensor; MC – measurement channels.

PROCESSOR REQUIREMENTS AND CHOICE

There are requirements for a processor as well. As it has already been said the processing time t_{pr} must be less than the acquisition time t_{aq}. Also processor must have either parallel ports or a specialized LCD interface to be able to visualize measurement data through a standard DVI/VGA display. Another important requirement for a processor is an affordable price of evaluation board. So analysis of the market was conducted at first. Analysis has shown that evaluation boards of Texas instruments™ DSPs have one of the lowest prices in the industry. Also Texas Instruments™ holds leading positions in the DSP market. Therefore it was decided to choose the processor of this manufacturer.

Texas Instruments produces a wide range of processors. One of them is OMAP L138. It has 2 cores (ARM and DSP) running at frequencies up to 456 MHz. Combination of ARM and DSP cores can considerably simplify the process of programming. For example, ARM cores are often used for

visualisation and interfacing and have ready-to-use libraries and functions for that, whereas DSP cores are optimized for math operations and high speed data flow. OMAP L138 has all the required interfaces including uPP (universal parallel port) which can be used for interfacing a video DAC.

It is important to evaluate the processing time of the key algorithms for this processor. The algorithm includes m_1=50 arithmetic operations with the processing time equal or less than the processing time of vector multiplication. The number of clock cycles required to multiply two vectors of an equal length *n*:

N=n+25 [2];

The length of the vector can be calculated by using the formula:

$$\mathrm{n} = f_s \frac{l}{v},$$

wheref_s – sampling rate,

l – length of the tube,

υ – speed of the tube.

Therefore the amount of time required to process multiplication operations equals:

$$t_1 = \left(f_д \frac{l}{v} + 25\right) \cdot \frac{m_1}{f_{clock}},$$

wherem_1- the number of multiplication operations;

f_{clock}-clock frequency;

Also there are m_2=4 division operations. One division operation takes up to 41 clock cycles [3].

Therefore the amount of time required to process division operations equals:

$$t_2 = \frac{41 \cdot (f_д \frac{l}{v}) \cdot m_2}{f_{clock}};$$

After substitution of all known values the general processing time for f_{clock}=456 MHz, f_s=18.1 KHz, m_1=50 and m_2=4 equals:

$$t_{обр} = t_1 + t_2 = \frac{8.494 \cdot 10^{-3} \cdot l}{v} + 2.7 \cdot 10^{-6};$$

The following diagram describes the dependence of the processing time on the speed of the tube for the tube speeds ranging from 0.1 to 4 m/s and the length *l* of 5 meters.

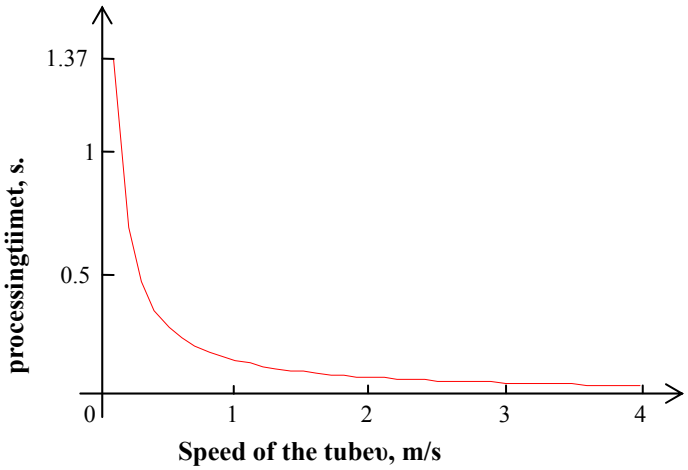

Fig.3. Dependence of the processing time on the speed of the tube

The diagram shows that at the speed of 0.1 m/s processing time equals 1.37sec.and acquisition time equals:

$$t_{aq} = \frac{5}{0.1} = 50\ sec.$$

At the speed of the tube of 5 m/s processing time equals 0.01sec. Processing time is significantly lower than the acquisition time. Therefore it is possible to continuously control tubes and pipes during the production process. After checking the performance requirements it is important to consider

the price of the evaluation module of this processor. Prices on the OMAP L138 evaluation modules start around 195$ which is affordable. The aforesaid processor meets the requirements for performance and price hence it can be used in the device.

Except for a processor and an ADC it is necessary to buy a video DAC. For example THS8200 can be used in the device. DAC THS8200 has the following characteristics:

- 3 DACs (205 ksps)
- support of VESA video formats
- programmable hsync/vsync output
- configurable master/slave mode
- I2C interface

THS8200 has the reasonable price of 9$.

CONCLUSION

A general concept of the data acquisition and processing system has been developed. According to the following table it significantly reduces the overall cost of the system:

Table 1. An approximate price of the system

OMAP L138 Evaluation board	x1	199$
TLV 2556	x2	18$
THS8200	x1	9$
PCB	x1	~70$
Total price		~296$

Undoubtedly the circuit will require a range of other components like resistors, capacitors, cables etc., but it's impossible to take them all into consideration until the circuit diagram is fully ready. Nevertheless their price is very low in comparison with the main parts of the system.

The approximate total price of the new data acquisition and processing system is 296$, whereas the system based on the USB-6363 costs 2500$+the price of PC.

REFERENCES

1. Goldshtein A., Bulgakov V., Kroening M. Eddy current testing of tubes and pipes with stimulation of multi frequency eddy currents of circular and length wise directions // Polzunov Herald - 2012.№2/1, p. 146-150.

2. Texas Instruments Website. URL: http://www.ti.com/lsds/ti/dsp/c6000_dsp/c674x/benchmarks. (Access date: 24.02.2013).

3. Texas Instruments Website. URL: http://www.ti.com/lit/an/spra707/spra707.pdf. (Access date: 24.02.2013).

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