A Dumbbell Type (D-Type) Multilevel Inverter Based on Switched Capacitor Concept

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In this paper, a new single-phase seven level inverter with reduced device count is introduced. The structure can boost the input voltage by synthesizing the capacitors' voltages in predetermined current paths. A single DC voltage source is utilized to generate the output AC staircase waveform, which is facilitated via Nearest Level Control. Self-voltage balancing ability, less number of semiconductor devices, high efficiency and control simplicity are the most significant inherent attributes of the proposed circuit. It is also noticeable that in this configuration neither bulky transformer/inductor nor filters are applied. Power loss calculation and required capacitance of the proposed inverter are investigated and theoretical efficiency of 93.31% was reached. Moreover, the proposed converter operates under various load conditions with lower Total Harmonic Distortion compared to recent topologies. Ultimately, operating principles of the proposed D-Type seven-level Inverter and simulation results in MATLAB SIMULINK environment are validated by experimental ones obtained from the laboratory prototype.

Keywords: Multilevel Inverter (MLI), Single-source, Switched-Capacitor (SC), step-up, Nearest Level Control, self-balancing.

1. Introduction

With the expansion of renewable energy application in power systems, the role of inverters are intensified which have led to augmentations of different aspects especially in cost, efficacy and quality of such systems [1]. According to S. Debnath and co-authors, high voltage and high power inverters are vitally required in bulk power controls [2].

The flourish of inverters were firstly started from three level topologies which suffered from both high voltage stress across the circuit components and Total Harmonic Distortion (THD) considering their component's low ratings [3]. Such limitations resulted in Multi-Level Inverters (MLI) origin which are widely implemented in daily used devices in residence and industries [4]. Based on the quality, type of source and

high/medium power demand of the circuit, these topologies are divided into Neutral Point Clamp (NPC) [5], Flying Capacitor (FC) [6], Cascade H-Bridge (CHB) [7] and Switched Capacitor (SC) [8] categories. Initial circuit configuration of each group has its pros and cons which requires more attention. For instance, voltage balancing in Direct Current (DC) link capacitors caused by limited switching states is an important issue for NPC and FC structures. While in CHBs, demanding several DC sources results in cost and size increment of the topology. Considering these aspects beside ease of controllability, has led to more prominent utilization of SC structures in power electronics such as: Fuel cell system [9], Fluorescent lamp [10], White Light-Emitting Diodes (WLED), Op-Amp, Liquid Crystal Display (LCD) drivers, Uninterruptible Power Supplies (UPS) [11], LASERs, Radars, X-Rays [12], Electrical Vehicles (EVs) [13], Grid integration of renewable energy systems [14], High frequency Alternative Current (AC) Microgrid [15], High frequency AC power distribution system [16], High-frequency-link DC transformer for Medium Voltage DC (MVDC) power distribution [17] and Magnetic Resonance Imaging (MRI) [18].

Although SC structures benefit from abovementioned advantages, they require some considerations in number of semiconductors, choosing appropriate capacitors and suitable output to input ratio whether they have boosting ability or not [19]. The advance of SCs is limited due to requiring so many switches and diodes which has necessitated the attention of many researchers in this criterion [20]; Therefore, several novel single-source SC-based concepts with reduced number of switches were proposed in [3, 12, 17].

Furthermore, boosting capability is an important obligation in industries, particularly in grid integration of renewable energy systems. Thus, Hinago and Koizumi proposed another SC-based MLI that steps the input voltage up to three times in the output

without using any inductors nor transformers [21]. Whereas, in [22] a new MLI topology including H-bridges and SC units is introduced.

This research aims to achieve a suitable arrangement of switches that improves Peak Inverse Voltage (PIV), Total Standing Voltage (TSV), THD, and obviously overall economic implementation cost. Consequently, the presented article reveals a novel single-source seven level inverter based on switched capacitor category. Realization feasibility by using a simple control strategy and generating negative voltage levels without any auxiliary circuit are other pros of the D-Type topology. Also, it is suitable for both medium power and voltage application. In order to achieve these goals, this study is organized as follows: Section 2 illustrates the description, principle of operation, switching patterns, Modulation strategy and expansion of the proposed topology. Moreover, a comprehensive comparison of D-type structure with other seven-level circuit configurations is performed in section 3. Then, determination of circuit capacitances with regard to power loss and efficiency calculations are discussed in Section 4. Furthermore, simulation results of the proposed topology are brought in section 5 and then the performance of the D-Type inverter is investigated through experimental tests in the laboratory environment. Ultimately, Section 6 of this paper is devoted to Conclusion.

2. Familiarization with D-Type structure

2.1. Topology Description

The structure of the proposed single-phase inverter is illustrated in Figure 1. Similar to other SCs, the operation of D-Type configuration depends on synthesizing the capacitors' voltages in a predetermined pattern to achieve the desired output waveform. This circuit configuration consists of 2 capacitors (C_1 and C_2), 8 unidirectional (S_1 to S_4 and S_6 to S_9) and one bidirectional (S_5) switches (in this case, MOSFET). Both capacitors

directly are charged up to V_{in}, via a single DC source. Then, by utilizing 9 gate driver circuits and applying Nearest Level Control (NLC), a seven level staircase AC voltage (*3Vin, 2Vin, Vin, 0, -Vin, -2Vin, -3Vin*) is generated across the load.

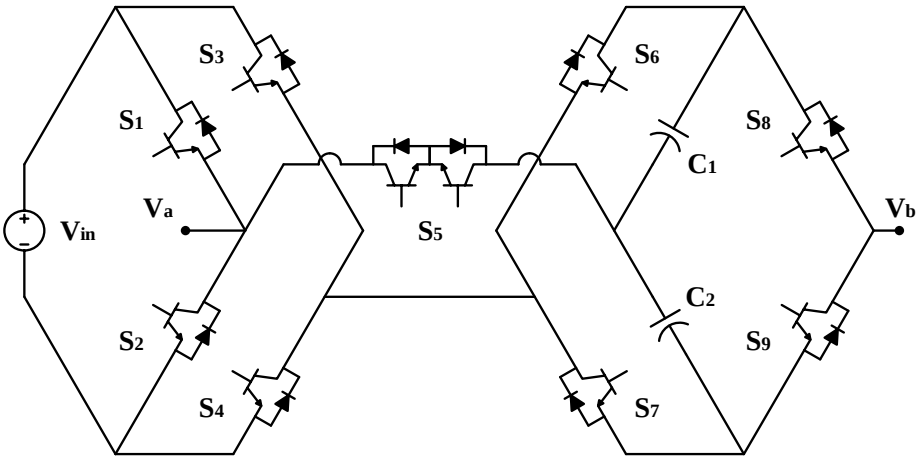
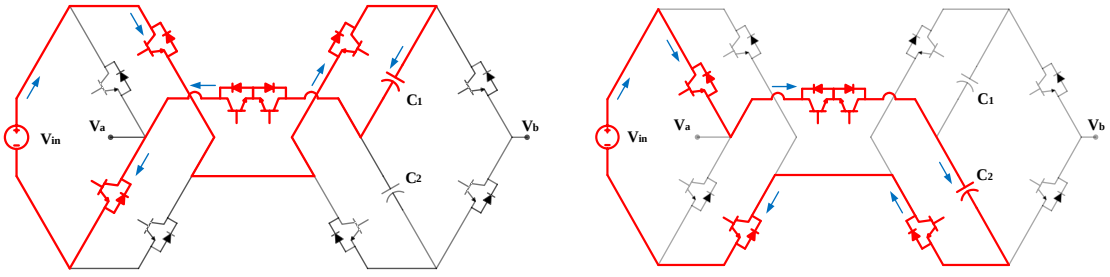


Figure 1. The structure of the proposed 7-level SCMLI (*Vout = Va - Vb*)

2.2 Operating principles

The output staircase waveform of the D-type inverter includes 3 positive, 3 negative and zero levels. Each level is achieved by synthesizing the voltages of the capacitors. Reaching the required waveform necessitates sufficient charge of the capacitors to the desired voltage through the predetermined current paths as depicted in Figure 2. According to Figure 2.a, the input source directly charges the capacitor C_1 up to V_{in} via S_2, S_3, S_5, and S_6 switches. Similarly, as shown in Figure 2.b, capacitor C_2 is charged by the source via S_1, S_4, S_5 and S_7 switches up to V_{in}.



(a) (b)

Figure 2. Predefined charging paths for capacitors (a) C_1 and (b) C_2

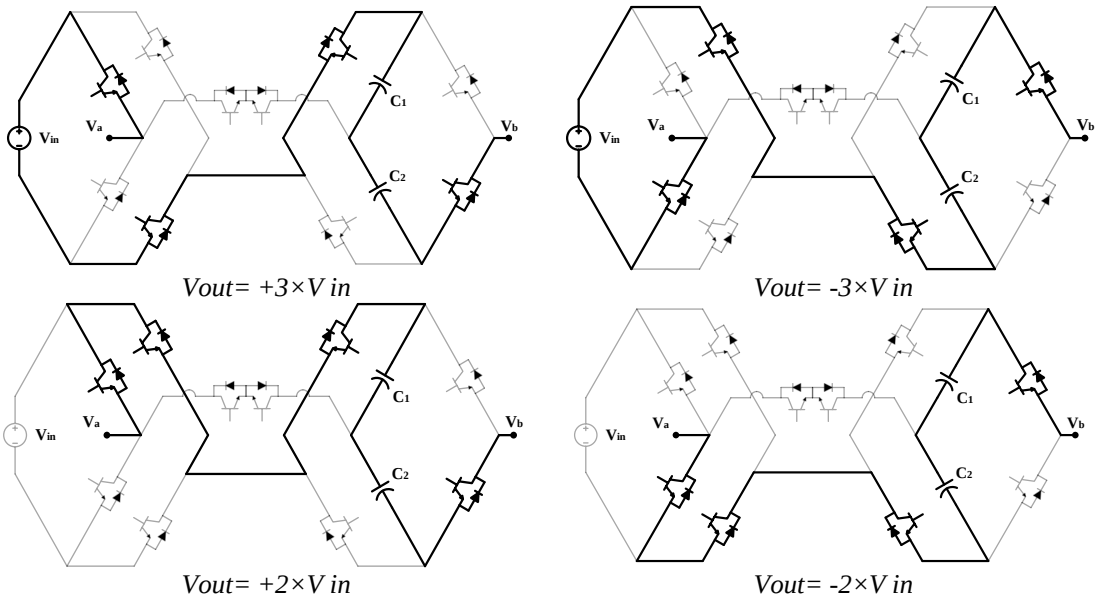
Furthermore, during charge and discharge intervals, rated voltage boundaries of the semiconductor devices should be considered. Hence, specific switching patterns for

charging and discharging of the capacitors should be defined. In this case, the switching states of the D-Type topology is brought in Table 1; Note that the state of each switch in Table 1, is shown by either 1 or 0 that represent ON or OFF, respectively.

Table 1. Selected Switching States of the D-type structure

	Active Switches									
state	**S1**	**S2**	**S3**	**S4**	**S5**	**S6**	**S7**	**S8**	**S9**	V_{ab}
1	**1**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**1**	***+3Vdc***
2	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**1**	***+2Vdc***
3	**1**	**0**	**0**	**1**	**1**	**0**	**1**	**0**	**1**	***+1Vdc***
4	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	**0**	***0***
5	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	***0***
6	**0**	**1**	**1**	**0**	**1**	**1**	**0**	**1**	**0**	***-1Vdc***
7	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**1**	**0**	***-2Vdc***
8	**0**	**1**	**1**	**0**	**0**	**0**	**1**	**1**	**0**	***-3Vdc***

The corresponding paths of eight abovementioned switching states are illustrated in Figure 3. As can be seen, the D-type topology benefits from the fact that the DC source can simultaneously supply the load and charge the capacitors C_1 and C_2 in levels $-1V_{in}$ and $+1V_{in}$, respectively. For levels $\pm 2V_{in}$, the two capacitors feed the load themselves. While in levels $\pm 3V_{in}$, the input source joins them in series.



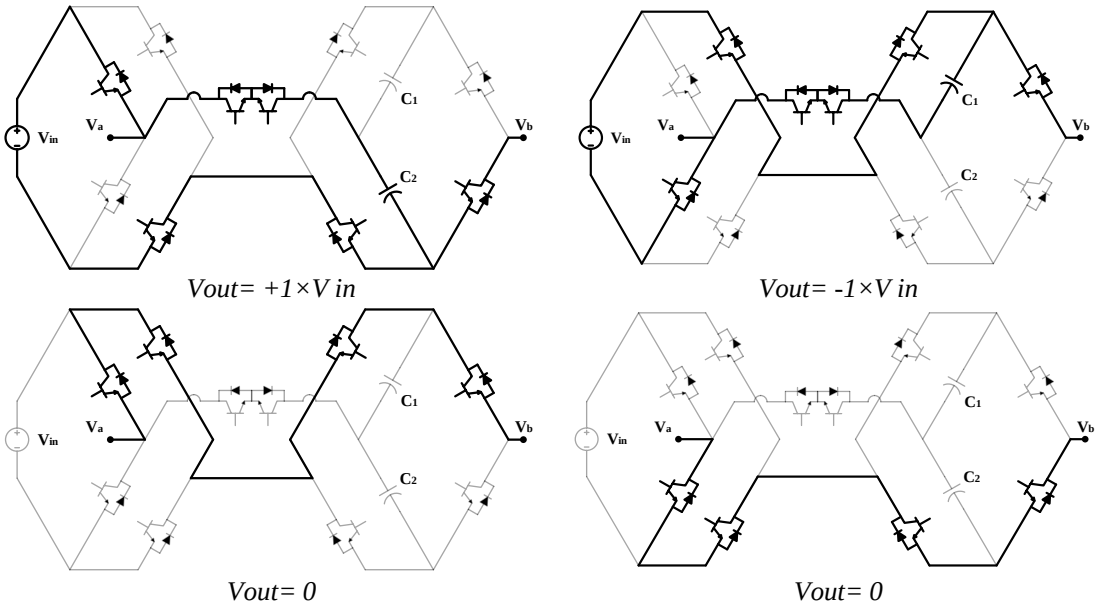


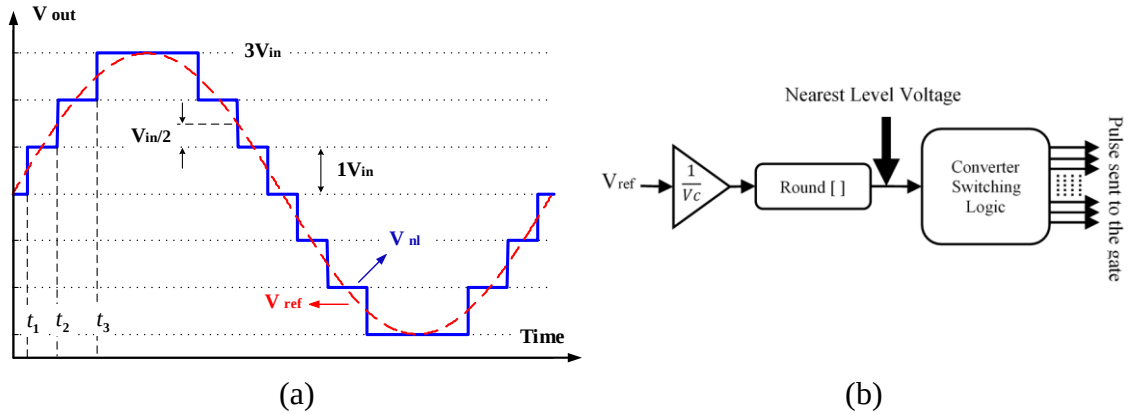
Figure 3. Predefined charging/discharging paths for D-Type inverter

2.3 Modulation Approach

The NLC technique is used for the operation of the proposed D-Type MLI to generate the desired near sinusoidal staircase output voltage with a 50Hz frequency. This strategy is an offline method to track the closest voltage level of the sample staircase waveform (V_{nl}) to the reference voltage (V_{ref}) [23]. As shown in Figure 4.a, the waveform is shaped by comparing the V_{ref} and desired output voltage (staircase) waveform. Then, the V_{nl} is determined by:

$$V_{nl} = \frac{1}{V_{in}} round(V_{ref}) \tag{1}$$

Afterward, the switching angles t_i ($i = 1, 2, 3$) and time intervals of each voltage level are determined. Finally, using the switching states of Table 1 and based on the charging and discharging modes of the capacitors, appropriate switching state for making each voltage level is selected (Figure 4.b) [20].



(a) (b)

Figure 4. NLC Method for the proposed 7-level SCMLI (a) NLC Scheme Waveform (b) Logic scheme

By applying this strategy, process speed improves and also calculations and implementation is simplified. In addition, allowing small steps of voltage levels and also low switching frequency, leads to the favourability of this strategy especially for MLIs. Hence, sufficient switching states of the D-Type topology could be adapted from Table 1 for each voltage level of the output.

2.4 Structural Comparison

An extensive study on D-Type structure and other seven-level inverters are presented in Table 2. These topologies are compared in terms of the number of switches, diodes, capacitors, drive circuits, input sources, *PIV*, *TSV* (*PIV* is the maximum voltage that each switch has to withstand when it is off and *TSV* is the sum of the *PIVs* of all switches in a prototype), boost ratio, and *THD*. It is crucial in an MLI topology design to use maximum achievable rating of switches. In some studies, the number of switches is rather low, while they operate with higher voltage stress. Thus, decreasing the number of switches by increasing the standing voltage in standard range is an important aspect which should be considered in comparison. Moreover, boosting ratio is the proportion of the output amplitude to the input source or the sum of input sources if there are more than one source.

As can be seen, topologies introduced in [29], [28] and [30] need less active switches, but it is important that they cannot boost the input voltage. Unlike the D-Type circuit, authors in [31], [32] and [30] introduced structures that require several isolated DC sources and the amplitude of the output does not exceed the sum of input voltages (they cannot boost the input voltage). One may note that [26] is a single-source topology with the ability to boost the input voltage. However, it suffers from higher *THD* than the proposed circuit.

It is noteworthy that unlike most other boost SC-MLIs, the proposed D-Type concept requires less semiconductor devices and also less gate driver circuits to generate the same output levels. In addition, having the lowest amount of the *TSV* and *THD* makes the proposed structure suitable for medium / high voltage application.

Table 2. Comparison of Different 7-Level Topologies

Reference	Switches	Diodes	Drivers	Capacitors	Source	*PIV (*Vin)*	*TSV (*Vin)*	*THD (%)*	Boost ratio
D-Type	10	10	9	2	1	2	14	12.72	3
[24]	16	16	14	2	1	1	16	-	3
[25]	10	10	10	2	1	3	18	25.4	3
[26]	7	11	7	2	1	3	21	-	3
[27]	14	14	14	2	1	1	14	15.02	3
[28]	7	9	7	3	1	1	5	-	1
[29]	8	8	8	0	2	2	12	22.47	1
[30]	8	8	8	0	2	3	18	9.31	1
[31]	10	10	7	0	3	3	19	19.05	1
[32]	12	12	12	0	3	1	12	20	1

3. Discussion

This section is devoted to an extensive discussion over the essential calculations for capacitances besides the losses and efficacy's determination. At last, possible extension forms of D-Type inverter for higher voltage levels are investigated.

3.1 Theoretical determination of the Capacitances

In order to achieve self-balancing for the voltage of the capacitors and avoid undercharging, the capacitances must be carefully specified. As a result, no external balancing circuit would be required. Therefore, two main factors should be taken into consideration: the first factor is related to the load current amplitude and its phase difference with the load voltage. The second one is discharging time of the capacitors while maintaining their voltage ripples within an acceptable boundary. The maximum charge drawn from each capacitor is calculated by [19, 21]:

$$\Delta Q_{Ci} = \int_{t_{1i}}^{t_{2i}} I_{out} \sin(2\pi f_o t - \phi)\, dt \tag{2}$$

where in this relation f_o and I_{out} represent the output frequency and the load current amplitude, respectively. Besides, the period of [t_{1i} , t_{2i}] is the longest discharging time interval for each capacitor, which demonstrates the worst possible condition. It should be noted that both capacitors C_1 and C_2 have the same capacitance values and the equivalent capacitance of the circuit (C_{eq}) while supplying the load can be determined by:

$$C_{eq} \geq \frac{\Delta Q_C}{k\, V_{eq}} \tag{3}$$

where, k is the maximum acceptable voltage ripple. Since both capacitors are directly charged by the input source (Figure 3.a and b), their voltages are equal.

$$V_{C1} = V_{C2} = V_{in} \tag{4}$$

3.2 Power Loss and Efficiency Analysis

The overall power loss of the circuit mostly originates from conduction losses and semiconductors switching. The conduction loss is caused by current flowing through circuit components which is obtained from [33]:

$$P_{con-L} = P^{sw}_{con-L} + P^{D}_{con-L} = (k_1.V^{sw}_{on} + k_2.V^{D}_{on}).I_{av-L} + (k_1.R^{sw}_{on} + k_2.R^{D}_{on}).I^2_{rms-L} \tag{5}$$

in which I_{av-L} and I_{rms-L} represent the average and Root Mean Square (RMS) current values of voltage level L ($L=0, \pm1, \pm2, \pm3$), respectively. Furthermore, Table 3 determines parameters k_1 and k_2, that are the number of switches and diodes involved in producing level L.

Table 3. Number of semiconductors involved in each level

Voltage Level	Number of Switches (*k1*)	Number of Diodes (*k2*)
+3 V in	**4**	**0**
+2 V in	**3**	**1**
+1 V in	**3**	**1**
0	**2**	**2**
-1 V in	**1**	**3**
-2 V in	**1**	**3**
-3 V in	**0**	**4**

Lastly, total conduction losses can be calculated as:

$$P_{con} = \sum_{L=-3}^{3} P_{con-L} \tag{6}$$

On the other hand, switching loss deals with inherent characteristics of switches which is mainly caused by delays of the semiconductor devices in the course of turning ON and OFF. This source of loss can be determined by the following equations [34]:

$$P_{sw-n(ON)} = f_{sw} \int_0^{t_{on}} V_{off\ state-n}(t).i(t)dt = \frac{1}{6} f_{sw} V_{off\ state-n} I_{on\ state1-n} t_{on} \tag{7}$$

$$P_{sw-n(OFF)} = f_{sw} \int_0^{t_{off}} V_{off\ state-n}(t).i(t)dt = \frac{1}{6} f_{sw} V_{off\ state-n} I_{on\ state2-n} t_{off} \tag{8}$$

Where, f_{sw} is the switching frequency, $V_{off\ state-n}$ represents the off-state voltage of nth switch, $I_{on\ state1-n}$ is the current of n^{th} switch when the switch is completely turned on, and $I_{on\ state2-n}$ shows the current of n^{th} switch before turning off. Consequently, total switching loss of the circuit is calculated by:

$$P_{sw} = \sum_{n=1}^{N-switch} \left(\sum_{j=1}^{N_{on(n)}} P_{sw-on(nj)} + \sum_{j=1}^{N_{off(n)}} P_{sw-off(nj)} \right) \tag{9}$$

Consider that $N_{on(n)}$ and $N_{off(n)}$ are the number of times which n^{th} switch turns on and off, throughout one cycle. Hence, the overall power loss is:

$$P_{loss} = P_{con} + P_{sw} \tag{10}$$

At last, efficiency (η) is obtained from:

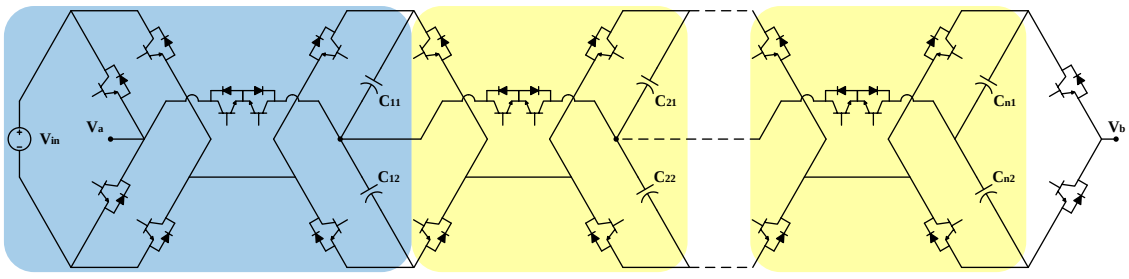
$$\eta = \left(\frac{P_{out}}{P_{out} + P_{loss}} \right) \times 100 \tag{11}$$

The theoretical efficiency of the proposed D-Type topology for $R_{load}=87.5$ ohm $V_{in} = 30V$, $V_{out-\max} = 90V$, $f_{out} = 50Hz$ and IRFP460 MOSFET switch characteristics, was reached to 93.31%.

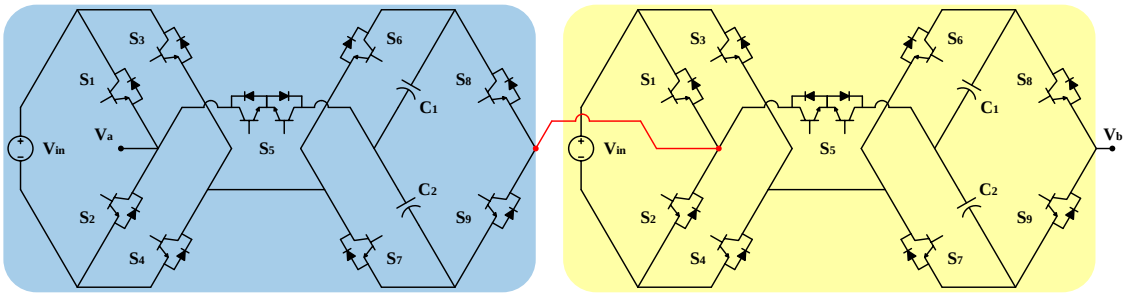
3.3 Topology Expansion

Achieving higher voltage levels (and/or output power) to increase the quality of output waveform is possible either by extending or cascading the structure as depicted in Figure 5.a and 5.b, respectively.

In some application, higher voltage levels might be required, hence the extended circuit configuration as shown in Figure 5.a is introduced. In this case, the low voltage (low /high current) DC input source is converted to a higher voltage /lower current AC output. Moreover, since all the capacitors are charged equally up to V_{in}, the output voltage is the sum of the capacitors' voltages.



(a)



(b)

Figure 5. Expansion of D-Type structure (a) extended, (b) cascaded topology

However, in some cases such as solar panels, multiple DC sources are available. In this circumstance, cascading the structure as in Figure 5.b could be a satisfactory option to collect the voltage of several panels (as V_{in}) and connect them to reach higher AC output voltages in both stand-alone and grid-connected application.

4. Results

In order to evaluate the proposed D-Type inverter, an extensive simulation and experimental investigation are accomplished. Results are exclusively described in associated sections.

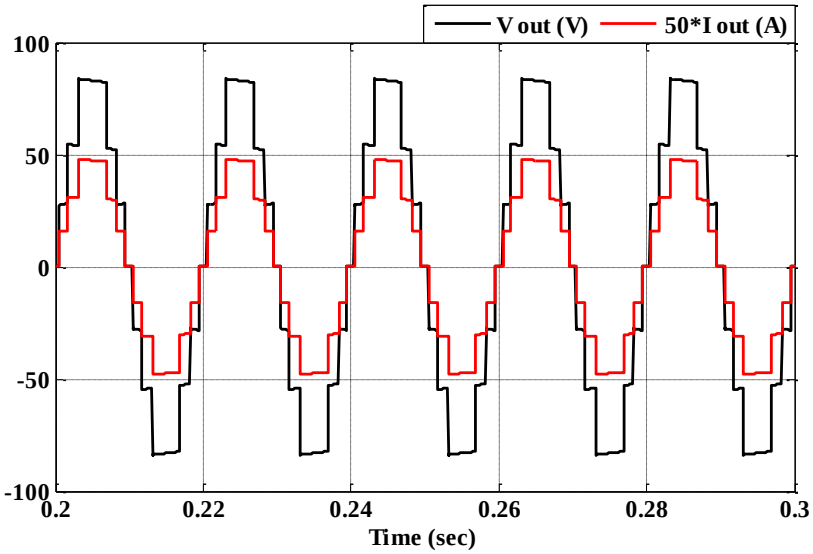
4.1 Simulation Results

Simulations of the D-Type topology were done in MATLAB Simulink software. The specifications of the simulation are brought in Table 4. The converter is studied under various loads. Next, the extended form of this converter is investigated. The NLC technique is used for operation of the inverter as discussed in section 2.3.

Table 4. Simulation parameters

Parameter	Value
Input voltage (Vin)	**30 V**
Number of voltage levels	**7**
Maximum output voltage	**90 V**
Output frequency	**50 Hz**
Switches	**MOSFET**
Capacitors	***C1=C2= 4700 µF***
Load	***R= 87.5 Ω , L= 103 mH***

Figure 6.a shows the output voltage and current waveforms for $V_{in}=30$ Volts and a pure resistive load of $R=87.5\Omega$. The corresponding capacitors voltages are brought in Figure 6.b. Note that the amplitude of the output voltage is 3 times the input and each level equals $1\times V_{in}$. Also, Figure 6.c brings the output waveforms of a resistive-inductive load of $R=87.5\Omega$ and $L=103mH$. The harmonic spectrum of the load voltage is illustrated in Figure 6.d. It reveals that the Voltage *THD* is 12.17 percent and the amplitude of all unwanted voltage harmonics is below 5 percent of the fundamental one.



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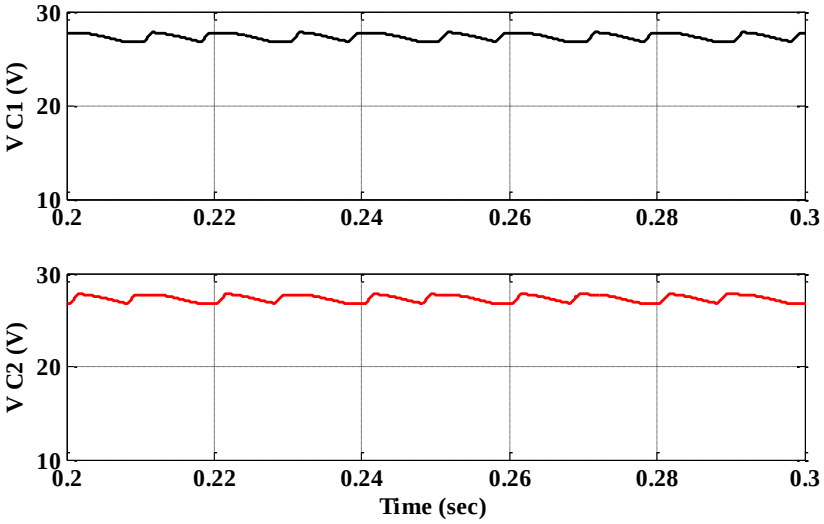

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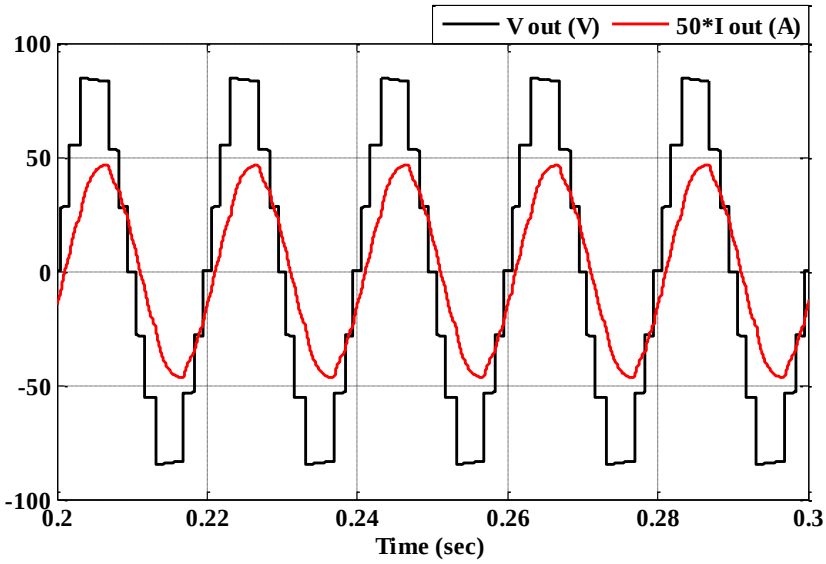

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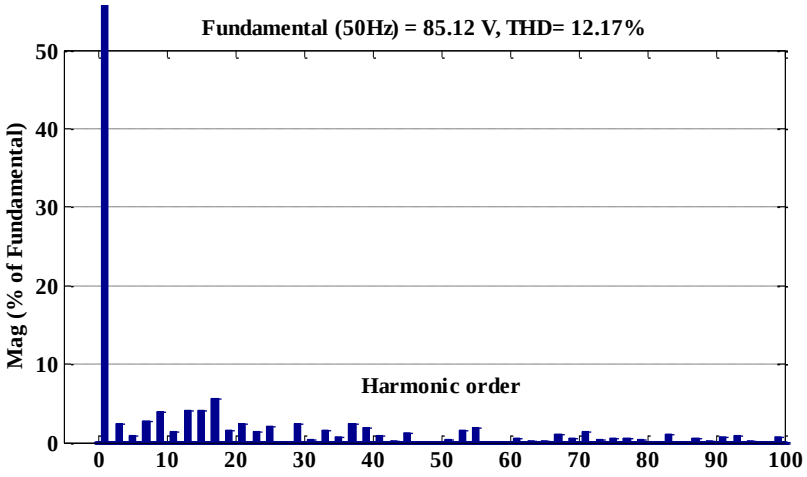
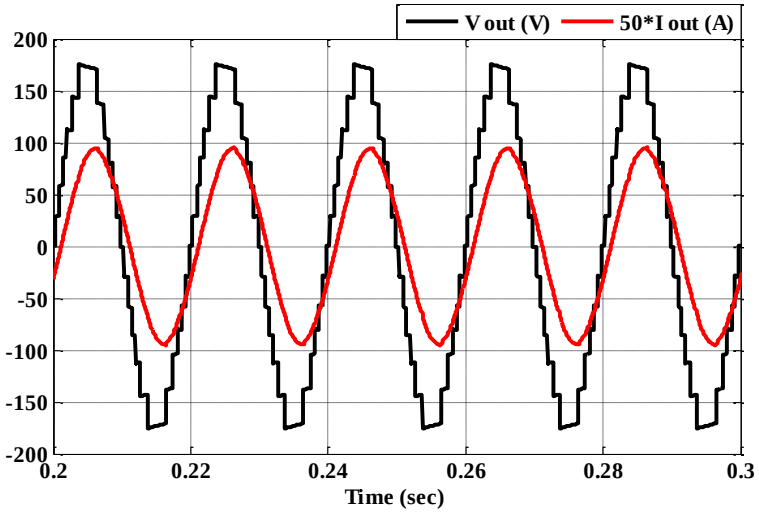


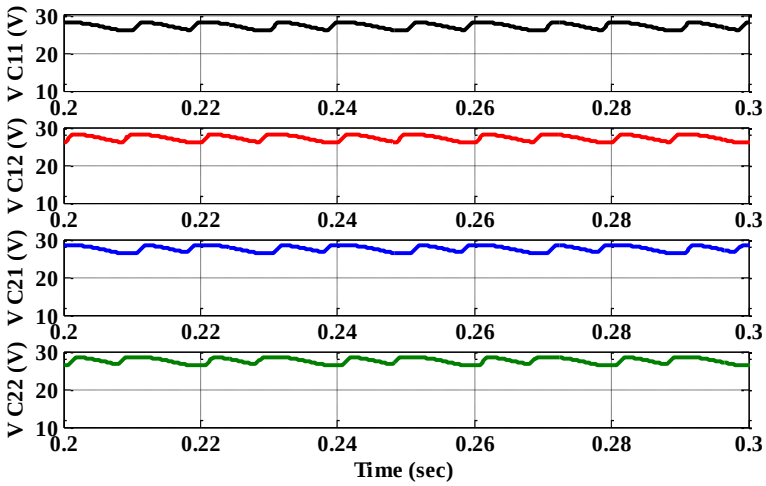
(d)

Figure 6. Simulation results of the D-Type inverter, (a) output voltage and current waveforms of a R-load (*R=87.5*Ω), (b) Capacitors voltages, (c) output waveforms of a R-L load (*R=87.5*Ω, *L=103mH*), and (d) Harmonic spectrum of the output voltage

Moreover, a 13-Level cascaded structure of Figure 5.b comprised of two identical modules was simulated. The parameters of the simulation are as described in Table 4. Using two identical power supplies resulted in generating a maximum of $6\times V_{in}$ boosting ratio, depicted in Figure 7.a. Capacitors voltages as presented in Figure 7.b show that for a desired tolerance, voltages of all four capacitors are self-balanced (without any auxiliary circuit). Furthermore, harmonic content for the 13-Level output voltage with the overall THD of 7.16 percent is illustrated in Figure 7.c.



(a)



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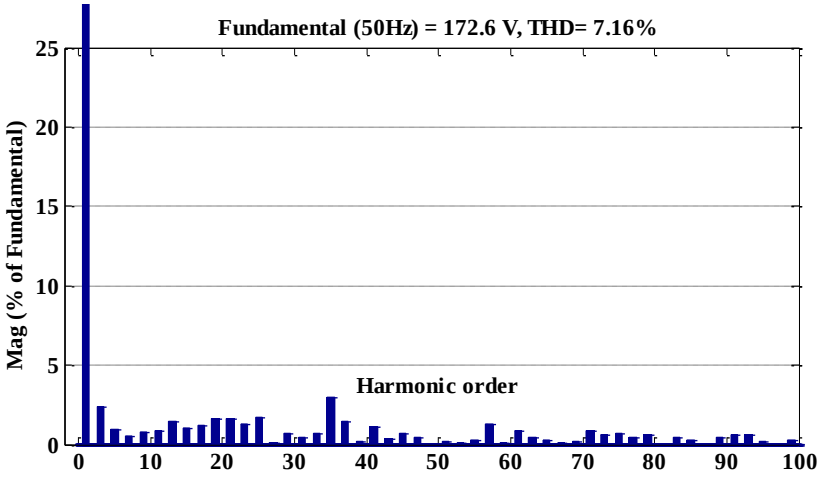
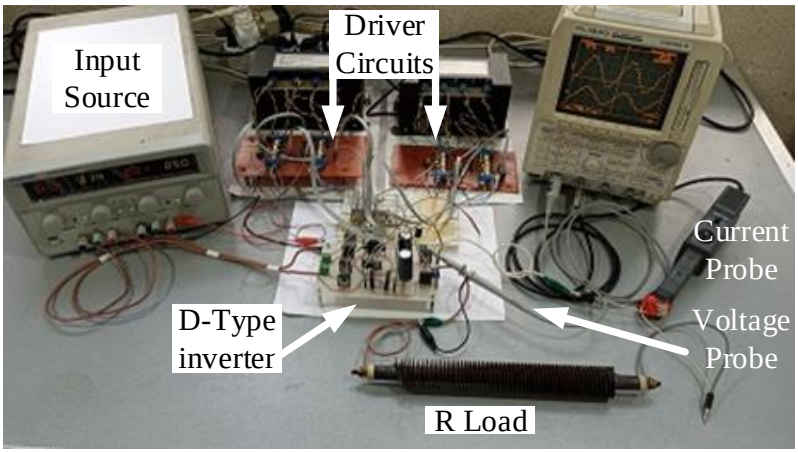


(c)

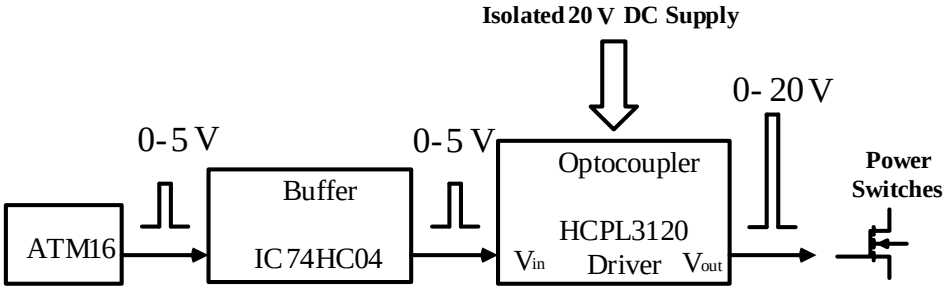
Figure 7. Simulation results of the Cascaded D-Type inverter, (a) output voltage and current waveforms of a R-L load (*R=87.5*Ω, *L=103mH*), (b) Capacitors voltages, and (c) Harmonic spectrum of the output voltage

4.2 Experimental Results

Simulation results of a single-cell seven level D-Type topology is validated by a laboratory prototype, shown in Figure 8.a. The parameters of the prototype device are given in Table 5 and the rating of the utilized MOSFETs are briefly presented in Table 6. Furthermore, Figure 8.b illustrates the control diagram of the circuit switches where gate drive pulses are made by ATMEGA16 microcontroller based on offline NLC calculations. Then, gate pulses are amplified to turn switches on and off, with the control circuit being isolated from the power circuit (using Opto-isolator, HCPL3120).



(a)



(b)

Figure 8. (a) Laboratory prototype of the proposed topology, (b) Control diagram of the circuit switches

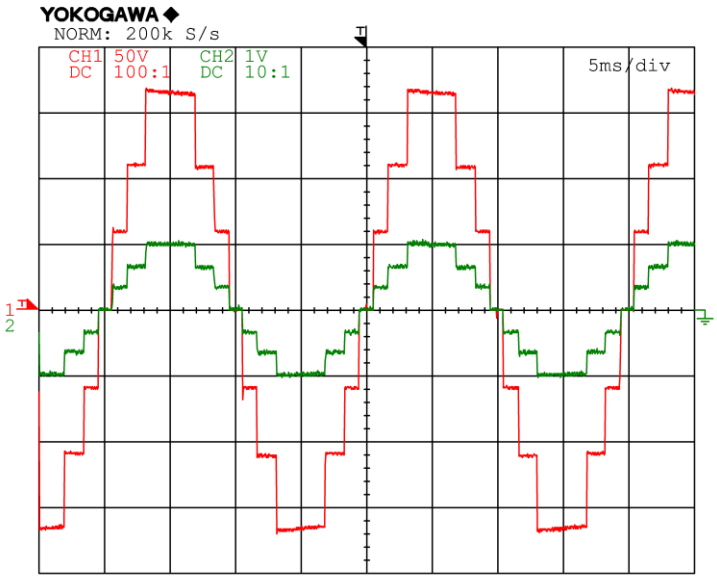
Table 5. Specification of the laboratory setup

Parameter	Value
Input voltage (Vin)	**30 V**
Number of voltage levels	**7**
Maximum output voltage	**90 V**
Output frequency	**50 Hz**
Switches	**IRFP460-MOSFET**
Capacitors	***C1=C2= 4700 µF***
Load	***R= 87.5 Ω , L= 103 mH***

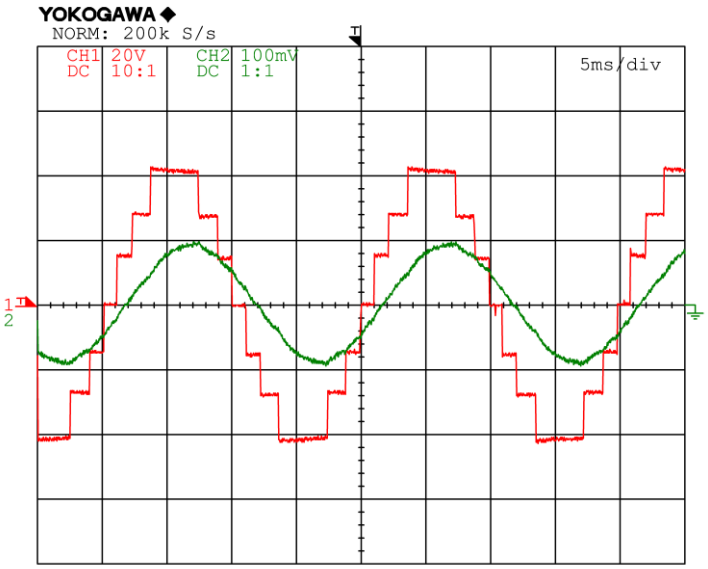
Table 6. Specification of the utilized MOSFET switches

Parameter	Value
Range of voltage	**500 V**
Range of current	**20 A**
Rise time	**15 n sec**
Fall time	**25 n sec**
On state resistance	**0.27 Ω**
On state voltage	**2 V**
On state voltage for antiparallel diode	**1.6 V**
On state resistance for antiparallel diode	**0.02 Ω**

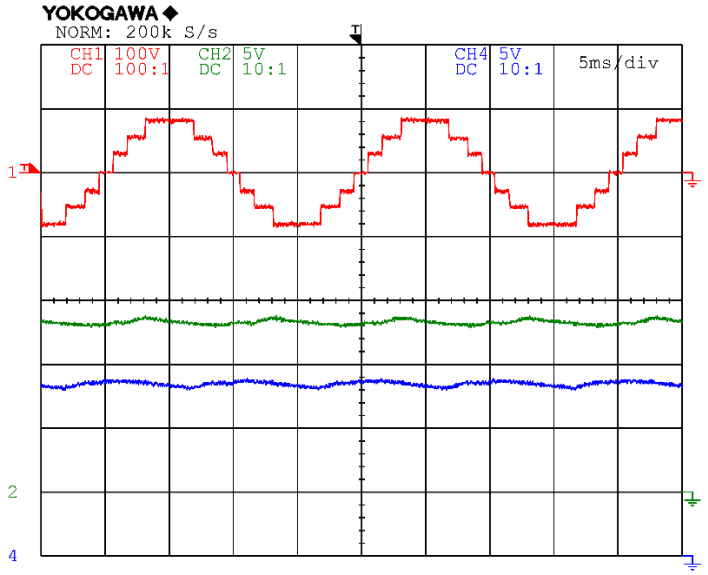
The experimental results of the test setup for different type of conditions are illustrated in Figure 9. Figure 9.a shows the output waveforms for a pure resistive load ($R=87.5\ \Omega$). The output voltage and current waveforms are comprised of seven steps peak to peak in which every voltage step is 30 V. The setting of the voltage and current probes are on 25 V and 1 A per division, respectively. Similarly, Figure 9.b depicts output waveforms for a resistive-inductive (R-L) load. Where, the setting of the voltage and current probes are on 40 V and 1 A per division, respectively. Besides, Figure 9.c shows the voltages of the capacitors. Figure 9.d represents the experimental output voltage harmonic spectrum of the proposed D-Type MLI.



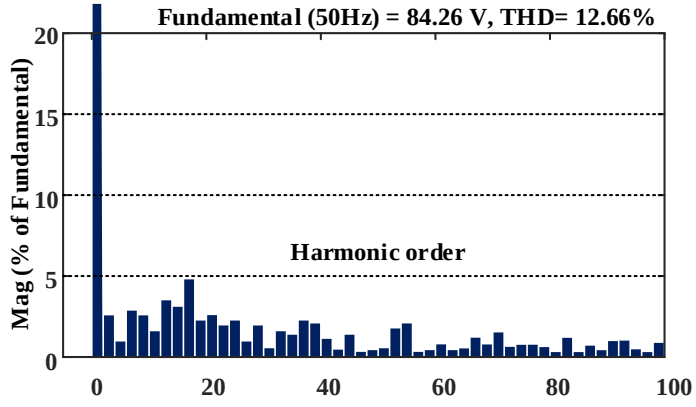
(a) CH1: 25 V/div, CH2: 1 V/div, 5 ms time/div



(b) CH1: 40 V/div, CH2: 1 V/div, 5 ms time/div



(c) CH1: 100 V/div, CH2: 10 V/div, CH4: 10 V/div, 5 ms time/div



(d)

Figure 9. Experimental results of the proposed D-type (a) R load (5 ms time/div) (b) R-L load (5 ms time/div), (c) output and capacitor voltages (5 ms time/div) and (d) Experimental harmonic spectrum of the output voltage.

Then, the performance of the inverter under sudden load change is examined. In this case, the load repeatedly changes from $Z_1 = 87.5\ \Omega$ to $Z_2 = Z_1 \,||\, (95\ \Omega + 103\ mH)$ with the frequency of 10 Hz (Figure 10). In other words, the system supplies a resistive load (87.5 Ω), at first. Then, an R-L load with amplitude of $R = 95\ \Omega$, $L = 103\ mH$ connects to the load in parallel.

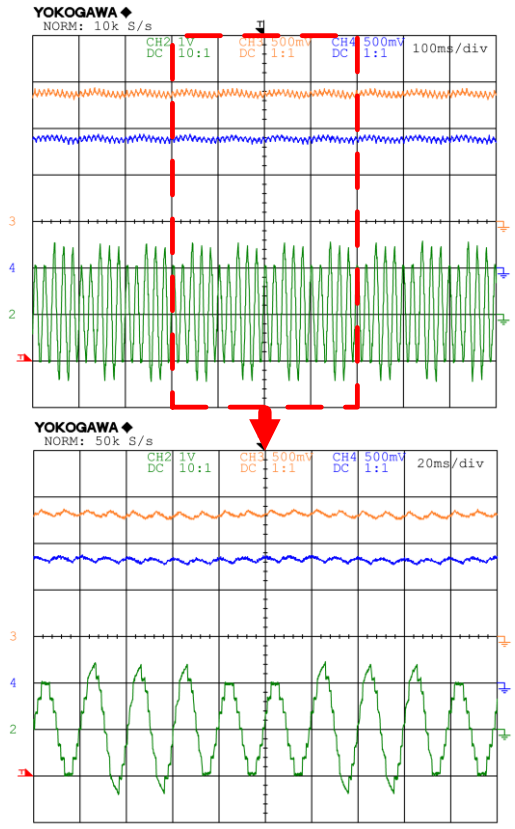


Figure 10. Capacitor voltages and load current under sudden load change (CH2: 1 V/div, CH3: 10 V/div, CH4: 10 V/div)

5. Conclusion

In this paper, a novel seven-level inverter cell based on switched-capacitor approach with self-balancing capability is introduced. The NLC strategy is applied for the operation of the proposed D-Type inverter. Moreover, a comparative study indicates that the D-Type topology performs better compared with recent topologies for the same output levels while it needs less number of circuit components. The evaluation of the D-Type structure is performed through theoretical analyses accompanied by simulation in

MATLAB Simulink software representing 93.31 percent efficiency. Also, a 13-Level cascaded structure comprised of two identical modules is presented, increasing the boosting ratio to six and further decreasing output voltage THD. Finally, the operation of the seven level D-type topology is validated by experiments applied to a laboratory prototype.

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