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Numerical simulation of low frequency noise in polysilicon thin film transistors

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Abstract- Numerical simulations of low-frequency noise are carried out in two technologies of N-channel polysilicon thin film transistors biased from weak to strong inversion, and operating in the linear mode. Noise is simulated by GR processes. The contribution of grain boundaries on the noise level is higher in the strong inversion region. The microscopic noise parameter deduced from numerical simulations is lower than the macroscopic one defined according to the Hooge empirical relationship and deduced from noise measurements. The higher macroscopic value is attributed to the drain current crowding induced by non conducting spots in the devices due to structural defects. The ratio of these two noise parameters can be considered as an indicator to qualify TFT technology.

Index terms- low frequency noise, Generation-Recombination, polysilicon TFTs, numerical simulation, impedance field method

I. INTRODUCTION

The physical origin of low-frequency (1/f) noise in TFTs due to carrier fluctuation is still controversial. It can be explained by trapping/detrapping into slow oxide traps [1-3] and/or by generation/recombination (GR) processes of carriers at defects such grain boundaries (GBs) [3] and thus the corresponding defect densities can be deduced. 1/f noise level is then strongly dependent on fabrication process. In this work we analyze by numerical simulations the 1/f noise level in N-Channel polysilicon TFTs biased in the linear mode. Noise is simulated by GR mechanisms (and the impact of the (structural) defects is pointed). Studied TFTs are issued from two (low temperature $\leq 600^\circ\text{C}$) technologies: Furnace Solid Phase Crystallized (FSPC) and Laser Solid Phase Crystallized (LSPC) TFTs. FSPC TFTs are built with one poly-Si layer: the upper part is heavily doped (source and drain regions) and the bottom part is none intentionally doped (active layer): see figure 1 (a). LSPC TFTs are fabricated with two poly-Si layers: source and drain regions are made on doped layer, whereas an underlying undoped layer constitutes the active one (see figure 1 (b)). Active layer in LSPC TFTs undergoes an additional solid phase thermal annealing by using a scan of an Ar laser beam. Details concerning TFT fabrication are given in ref [4,5].

II. SIMULATION

In both simulated TFTs (fig. 1) the doped and undoped polycrystalline films are 150nm thick. The oxide thickness t_{ox} is 60nm in FSPC TFT and 74nm in LSPC TFT. In FSPC TFT we get $W/L=50\mu\text{m}/20\mu\text{m}$, whereas in LSPC TFT $W/L=80\mu\text{m}/60\mu\text{m}$. The polysilicon is described by introducing equally spaced GBs, depicted as thin amorphous silicon layer with a width of 2 nm, perpendicular to the carrier **transit** direction. The grain size in FSPC TFT and LSPC TFT is 300 nm and 500 nm, respectively. Geometrical dimensions of each part of the structure correspond to those of processed devices (see ref [4,5]).

1/f noise simulation is based on the impedance field method (IFM) of Shockley by using the DESSIS-ISE multidimensional simulator of ISE-TCAD software [6]. A numerically efficient Green function approach to the Langevin equation-based simulation of the IFM is the basis for the implementation in ISE simulator. The complex Green functions G describe the propagation of perturbations inside the device to the contacts. The noise voltage spectral density was calculated from integration over all noise sources [6]:

$$S(\omega, r) = \sum_{\alpha=n,p} \int_{\Omega} G_{\alpha} K_{\alpha,\alpha}^{GR} G_{\alpha}^* dr + \sum_{\alpha=n,p} \int_{\Omega} G_{\alpha} K_{\alpha,\alpha}^{fGR} G_{\alpha}^* dr \quad (1)$$

where K^{GR} , K^{fGR} and Ω represent the GR and the flicker GR local noise sources and the device volume respectively. The GR noise source model that is expressed as a tensor:

$$K_{n,n}^{GR} = \frac{J_n \otimes J_n}{n} \frac{4\alpha_{gr} \tau_{gr}}{1 + \omega^2 \tau_{gr}^2} \quad (2)$$

J_n is the local current density, n the local carrier density, τ_{gr} the equivalent GR lifetime, α_{gr} a constant which represents the quasi Poissonian character of the carrier number (N) fluctuations ($\langle \Delta N^2 \rangle = \alpha_{gr} \langle N \rangle$) and $\omega = 2\pi f$ is the angular frequency. The 1/f noise source is represented as the sum of GR noises produced by sub bands of impurities or defects, with a corresponding distribution of trapping characteristic times between τ_1 and τ_2 : $g(\tau) = (\ln(\tau_2 / \tau_1) \tau)^{-1}$ [3]. The flicker GR local noise source is expressed as a tensor:

$$K_{n,n}^{fGR} = \frac{J_n \otimes J_n}{n} \frac{2\alpha_H}{\pi f \log\left(\frac{\tau_2}{\tau_1}\right)} [\arctan(\omega\tau_2) - \arctan(\omega\tau_1)] \quad (3)$$

α_H is identified to *the microscopic Hooge noise parameter* associated with the local source of noise.

The calculation of the drain current noise spectral density requires knowledge of the local noise source K . We defined the flicker GR local noise sources K^{fGR} in the whole bulk of the active layer with α_H assumed identical for all sources. In order to obtain a 1/f behaviour in the studied frequency band (1Hz-10³Hz), the relaxation times τ_1 and are fixed at 10⁻⁷s and 10⁴s, respectively. For GR mechanism at SiO₂/Sipoly interface $\tau = \tau_0 \exp(\gamma y)$ with $\tau_0 \sim 10^{-12}$ s, $\gamma \sim 10^{10} \text{m}^{-1}$, and y the tunnel path. For GR mechanism at GBs associated to thermally assisted tunnelling process (see inset of fig 1) $\tau = \tau_0 \exp(\Delta E/kT) \exp(\gamma y)$ [7]. For example if $y \approx 3 \text{nm}$ and $\Delta E \approx 0.2 \text{eV}$ it gives $\tau_2 \sim 10^4$ and this justify the high value of τ_2 . For some spectrums with a Lorentzian (figure 2), we introduced a GR local noise source K^{GR} .

III. RESULTS AND DISCUSSION

A good fit of experimental with numerical noise spectra was obtained (figure 2), and then the microscopic noise parameter α_H in (3) was deduced for FSPC and LSPC TFTs. Values of α_H versus effective voltage ($V_{GS}-V_0$), with V_0 the flatband voltage, are reported in figure 3. Plots of macroscopic apparent noise parameter α_{app} , deduced from the experimental measurements [8] according to the Hooge formula $S_{IDS}/I_{DS}^2 = \alpha_{app}/(fN)$ with N the free carrier number in the channel, is also reported. For both devices α_H and α_{app} increase from weak to moderate inversion and then it decreases from moderate to strong inversion. This singular behaviour, previously reported for α_{app} [8], suggest that α_H and α_{app} are directly related. Higher value of α_{app} could be explained by the current crowding (CC) due to structural defects inducing non conducting spots [9,10,11]. In such case CC is characterized [11] by standing 1/f noise in a relative noise level for a unit area $C_{us} = KR_{sh} = (f S_{IDS}/I_{DS}^2)WL$ with $K = \alpha_{app}q\mu$ (μ carrier mobility) and $R_{sh} = (V_{DS}/I_{DS})(W/L)$ the sheet resistance (linear mode- $V_{DS}=300mV$). Plots of C_{us} versus R_{sh} reported in the inset of the figure 3 show that $K > K_{Au} = 5 \times 10^{-21} cm^2/\Omega$ obtained for gold resistor indicating CC on a microscopic scale. For homogeneous materials $\alpha_H/\alpha_{app} \sim 1$ whereas for disordered materials $\alpha_H/\alpha_{app} \ll 1$. In our case, the maximum value of this ratio is ~ 0.17 and ~ 0.11 respectively for FSPC and LSPC TFTs. The lower value in LSPC TFT can be explained by the poorer quality of the access resistance because of the active layer/source(drain) region interface acting as an additional non conducting spot. This effect is consistent with the higher measured macroscopic parameter and the higher K-value for LSPC TFTs (figure 3). Thus α_H/α_{app} could be considered as an indicator of quality.

In the figure 4 we report the impact of the local sources of noise at the GBs on the noise level in the TFTs. The results show that the addition of sources of noise at the GBs leads to a significantly higher simulated drain current noise in the strong inversion region, and thus that the contribution of the grain boundaries on 1/f noise generation in TFTs is higher at the On-State.

IV. CONCLUSION

Numerical simulations of low frequency noise in TFTs is presented. Noise is modelled by carrier fluctuations due to GR mechanisms of carriers from defects within the active layer. The study underlines the impact of the structural defects of polysilicon and/or of those induced by the design of the devices on the 1/f noise level in polysilicon TFTs.

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Figure captions

Figure 1: Schematic cross-section structure of devices for 2D simulation, (a) FSPC TFT, (b) LSPC TFT. For simplicity, all Grain Boundaries (GBs) are not represented on the figure. Inset: schematic thermally assisted tunnelling process at grain boundaries.

Figure 2: Experimental and simulated noise current spectra at different gate voltages for (a) FSPC TFT ($W/L=50\mu\text{m}/20\mu\text{m}$) and (b) LSPC TFT ($W/L=80\mu\text{m}/60\mu\text{m}$) biased in the linear mode ($V_{DS}=300\text{mV}$). Insets: Plots of the normalized noise current spectral versus the corresponding measured drain current.

Figure 3: Noise parameters versus effective gate voltage. Flatband voltage V_0 is approximately identified to the gate voltage corresponding to the minimum of drain current. α_{app} is deduced from measurements of S_{IDS} , and α_H by fitting the calculation according to (1) and (3) of S_{IDS} with the corresponding measurements. Inset: Calculated C_{it} versus R_{sh} for FSPC and LSPC TFTs.

Figure 4: Simulated noise current spectral versus effective gate voltage in TFT: effect of local source of noise at the grain boundaries on noise level.

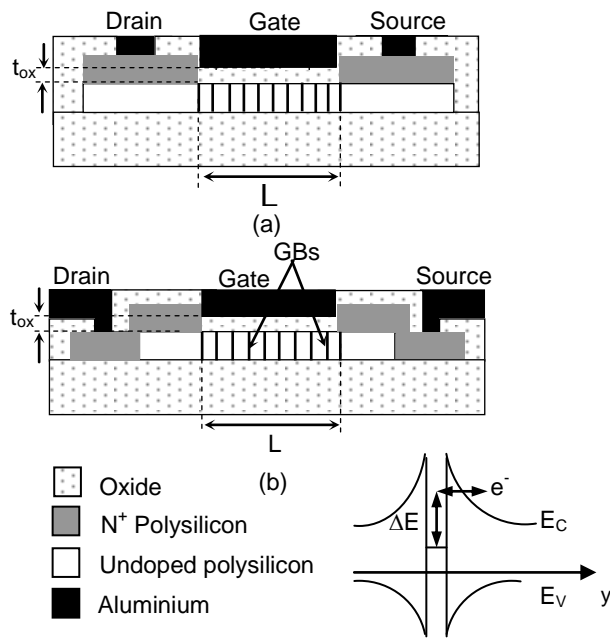
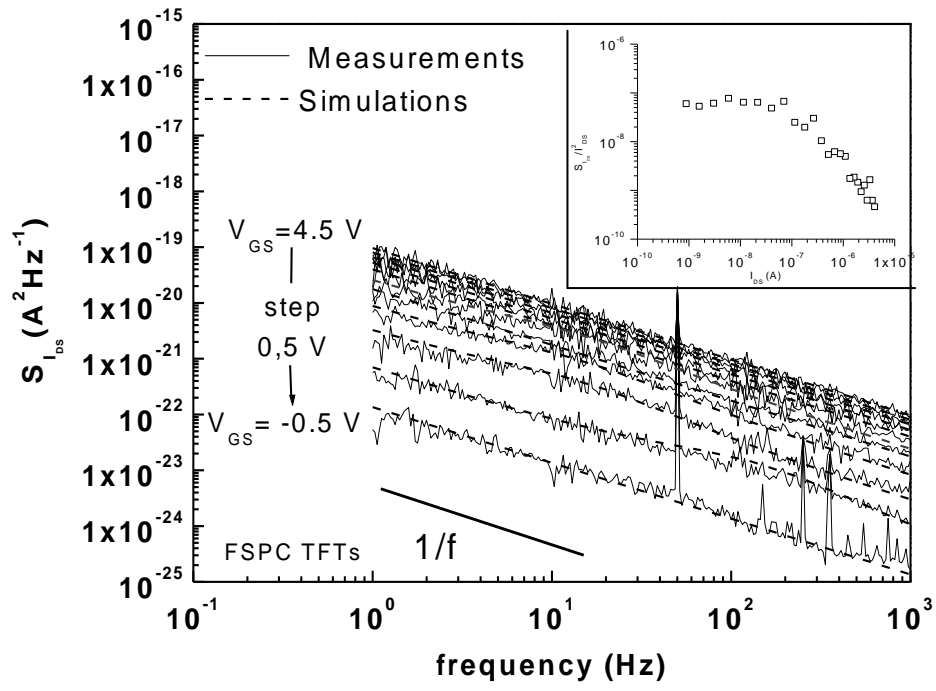
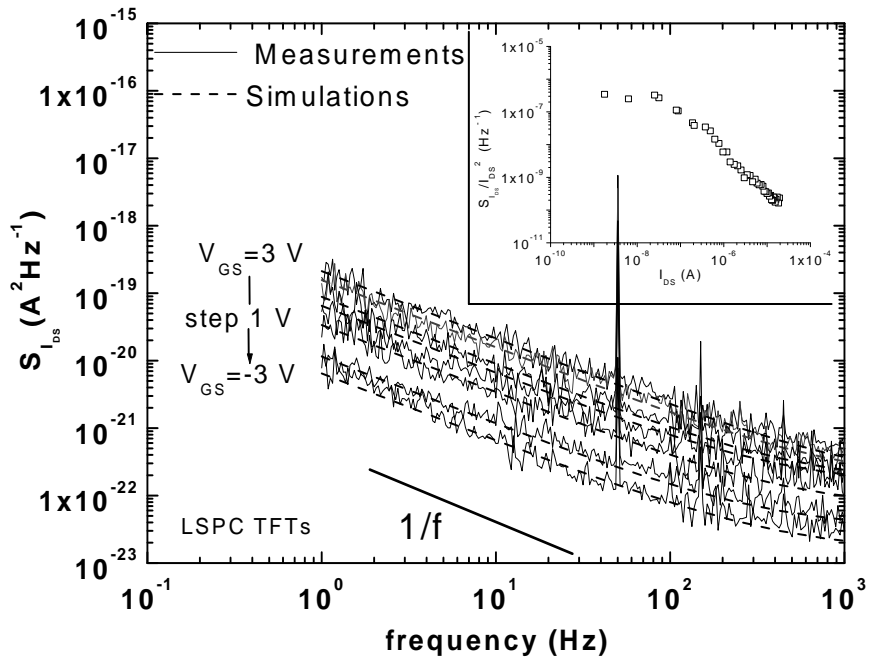


Figure 1



(a)



(b)

Figure 2

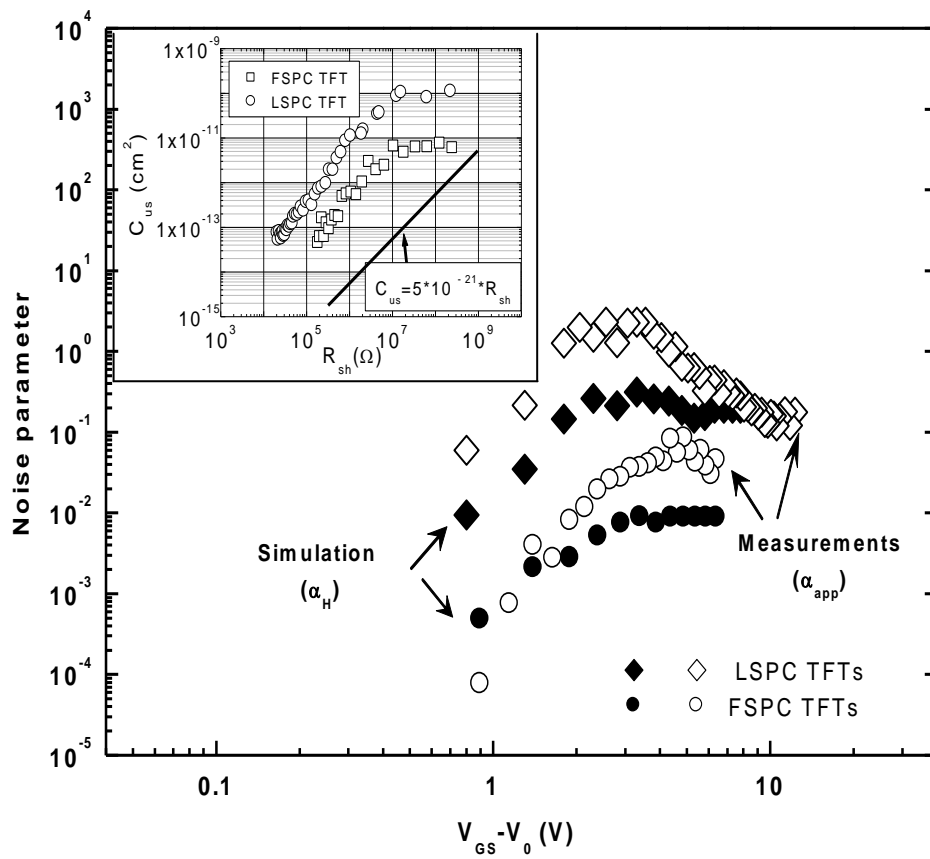


Figure 3

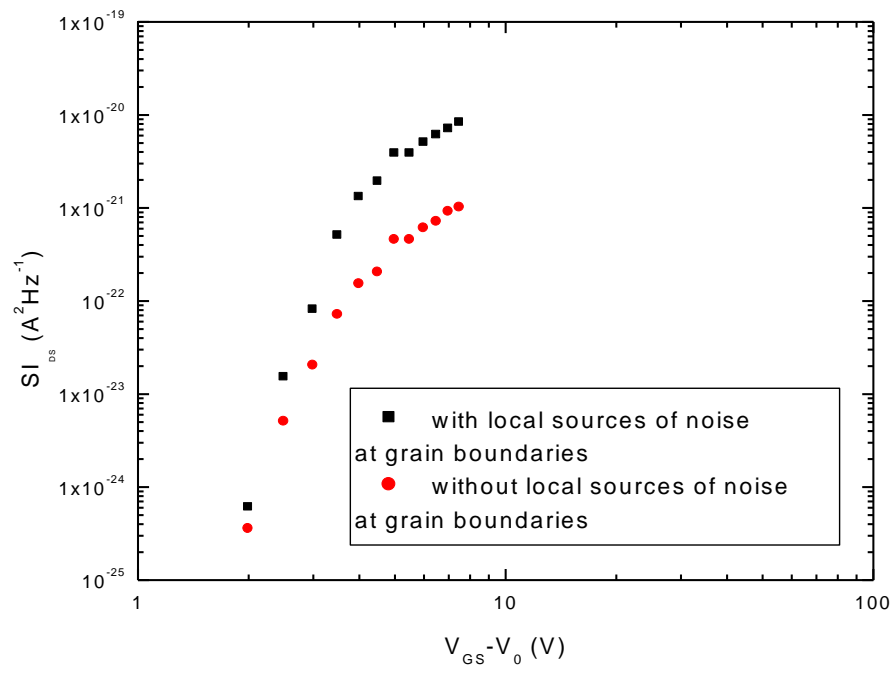


Figure 4