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Low-frequency noise is studied in N-channel polysilicon TFTs issued from two (low temperature ≤600°C) technologies: furnace solid phase crystallized (FSPC) and laser solid phase crystallized (LSPC) TFTs. The distribution of the trap states (DOS) into the polysilicon bandgap determined for devices biased in the weak inversion is one decade lower for LSPC devices.
The high range values ($10^{-4}\leq\alpha\leq1$) of the measured macroscopic noise parameter, defined according to the Hooge empirical relationship, are explained by the drain current crowding due to structural defects within the active layer. The higher values of $\alpha$ for the LSPC TFTs are attributed to a better structural quality of the active layer.



**1 Introduction** Polysilicon thin-film transistors (TFTs) are key elements for large area electronics such as flat panel displays, and flexible electronics because of their high potential usefulness in driving circuits and/or in addressing pixels. However, some improvements remain in TFT technology because the electrical properties are strongly affected by the trapping of carriers at the defects located at the grain boundaries and at the oxide/semiconductor interface. In particular, the resulting high level of low frequency (1/f) noise can be one limiting factor for using such devices [1].

The physical origin of 1/f noise in TFTs due to carrier fluctuation is still controversial. It is useful to model 1/f noise by trapping/detrapping (T/D) of carriers into slow oxide traps located close to the interface [2-3] and the corresponding distribution of states (DOS) into the band gap can be deduced [2]. In addition, T/D processes of carriers at grain boundaries (GBs) have also been previously suggested and the average defect density at GBs can be deduced from noise measurements [3]. 1/f noise level is then strongly dependent on both interface and active layer qualities, and thus on fabrication process parameters [2,4]. Therefore 1/f noise measurement can be used as diagnostic tool to qualify TFT technology.

In this paper we study 1/f noise in devices issued from two low-temperature (≤600°C) N channel polysilicon TFT technologies: furnace solid phase crystallized (FSPC) and laser solid phase crystallized (LSPC) TFTs. We report the effect of the laser annealing on the active layer on the 1/f noise level and its relation both with the interface and the active layer crystal qualities.

**2 Devices and experimental description** FSPC TFTs are elaborated with a single poly-Si layer (fig. 1. a): the upper part is heavily *in-situ* n-type doped (source and drain regions), and the bottom part is none intentionally doped and is dedicated to the active layer. LSPC TFTs are fabricated with two poly-Si layers (see fig. 1. b): an undoped polysilicon layer forms the active one, whereas an *in-situ* n-type doped layer constitutes source and drain regions. For the two types of TFTs the polysilicon layers are deposited by a LPCVD (Low Pressure-CVD) technique and are crystallized by a FSPC thermal annealing in vacuum at 600°C. Before gate insulation an additional SPC thermal annealing of the active layer is carried out on LSPC structures by using a scan of an Ar laser beam. The gate insulator is made of $SiO_2$ deposited by CVD process at atmospheric pressure (APCVD) at 390°C and annealed at 600°C in nitrogen ambient for densification.
The thickness of the gate oxide is 60nm and 76nm in SPC TFT and in LSPC TFT respectively. Electrodes are made of thermally evaporated aluminium. Finally the devices were annealed into forming gas ($N_2/H_2$=95%) at 390°C during 30 minutes. More details for fabrication are given in ref [5] and [6].

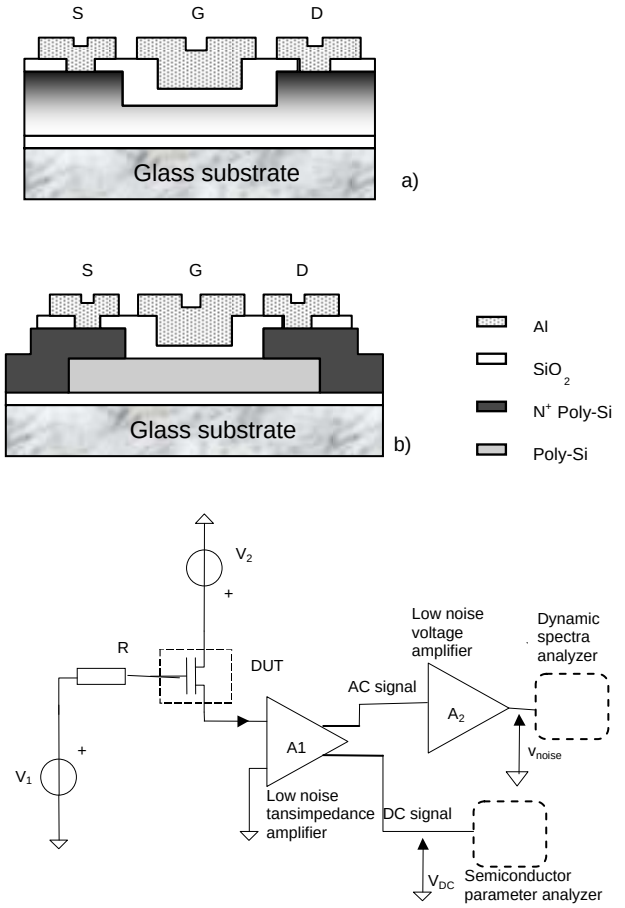


**Figure 1** Schematic cross section of the a) FSPC TFT, b) LSPC TFT, c) Experimental set-up for noise measurements in devices under test (DUT).

For LPC TFTs process laser annealing parameters (P=4.8W, v=70mm/s) were adjusted to limit contamination from the glass substrate of the active layer. In these conditions the active layer remains in solid phase and does not offer a high degree of crystal quality as usually provided by other types of laser crystallization processes. In addition, a high surface roughness and a contamination from the glass substrate are possible as reported in such laser annealed polysilicon layer [6]. In such case the average grain size in laser annealed polysilicon layer is quite the same as for FSPC annealed polysilicon layers (~ 100nm [5,6]).

Noise measurements are carried out in a shielded environment by using a low noise transimpedance amplifier (EG&G 5182, 15fA/$\sqrt{\text{Hz}}$) connected to the source electrode, followed by a low noise voltage amplifier (EG&G 5113, 4nV/$\sqrt{\text{Hz}}$) and a HP 3562A dynamic signal analyzer (see fig. 1 c). Static drain current measurements arecarried out by using a HP 4156 B semiconductor parameter analyzer. All tested devices are biased in the linear mode ($V_{DS}$=300mV) from weak to strong inversion.

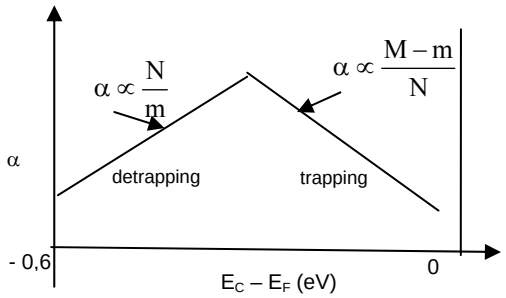


**Figure 2** Theoretical variations of noise parameter versus the Fermi level position into the bandgap (after [7]).

**3 Results and discussion** Low frequency noise in MOS transistors is described by the widely used Hooge empirical relation:

$$\frac{S_{I_{DS}}}{I_{DS}^2} = \frac{\alpha}{fN} \tag{1}$$

where $S_{IDS}/I^2_{DS}$, $\alpha$, N and f stand for the normalized drain current spectral, the noise parameter, the free carrier number and the frequency respectively. For N-channel MOS transistors the $\alpha$ measured values are dependent on the gate bias over a high range magnitude ($10^{-6}$-1). In the case of polysilicon TFTs values are higher than for single crystalline silicon transistors [7] and related to mechanisms conduction depending on both gate oxide interface and active layer qualities as discussed in the two next sections.

**3.1 Trapping/detrapping processes of carriers into the oxide**. The noise analysis is first supported by the results previously reported [8] on the theory of the sum of generation/recombination (GR) spectra to explain T/D processes following the tunnelling theory of carriers into the gate oxide traps located close to the interface.

From weak to moderate inversion (at low gate voltages):

$$\alpha \approx 4\frac{N\lambda}{mz} \tag{2}$$

with m the number of trapped carriers into the oxide close to the interface, z the effective oxide thickness (=3nm), and $\lambda$ the tunnel attenuation distance (≈0.1nm). In such case detrapping processes dominate and $\alpha$ increases versus the Fermi level ($E_F$) position into the bandgap (or with the gate voltage) following N/m ratio (see fig 2).

In the strong inversion (at high gate voltages):

$$\alpha \approx \frac{(M-m)\lambda}{Nz} \tag{3}$$

where M is the total number of traps uniformly distributed into the gate oxide. In such case trapping processes dominate and α increases versus the Fermi level into the band-gap following (M-m)/N ratio (see fig. 2), with M-m as the trapping centre number. M and m are associated with trap states around the Fermi level (fixed by the gate voltage).

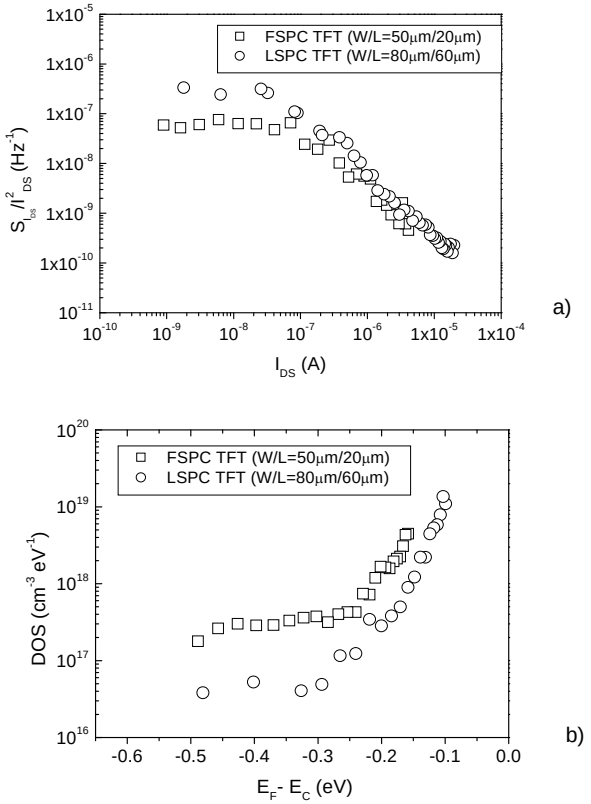


**Figure 3** a) Normalized drain current spectra versus drain current for FSPC and LSPC TFTs, b) DOS into the band gap for the FSPC and the LSPC TFTs versus the position of the Fermi level into the band gap. After [2].

Validity of these theoretical predictions has been previously experimentally demonstrated [2,7].

The number of trapped carriers into the oxide is strongly controlled by the distribution of interface states. Therefore, considering traps located around the Fermi level, the density of deep states (DOS) into the polysilicon band-gap at the interface can be deduced from the normalized drain current spectral according to (1) and (2) by standing [2]:

$$N_{OX_{DOS}}(V_{GS}) \approx N_{OX_{DOS}}(E_F) \propto \frac{m}{WLzkT} \approx \frac{4\lambda}{WLz^2kTf}\frac{I_D^2}{S_{I_D}} \quad (4)$$

Plots of the DOS for the FSPC and the LSPC TFTs are reported in the figure 3. The lower value of the DOS (one order of magnitude) for LSPC devices suggests a lower number of trapped carriers due to a lower density of deep states associated to dangling bonds close to the interface. This result is related to a better crystal quality of the active layer because of the laser annealing. Furthermore, M-m values were deduced in the strong inversion for the two types of devices: M-m~$10^7$ (ie M≥$10^7$) for FSPC TFT and M-m~$10^8$ (ie M≥$10^8$). The higher value for LSPC structures is related to a higher total density of oxide traps M attributed to a possible contamination of the oxide from the glass substrate and to a lowering of the density of defects at the interface during the laser annealing.

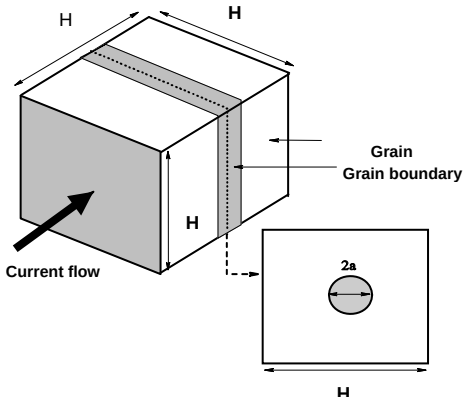


**Figure 4** Schematic conducting region at GB in circular grey area.

These results show the effect of the laser annealing on the 1/f noise level depending on the gate oxide interface quality related to the crystal quality of the layer.

**3.2 Current crowding**. In this section the noise analysis is supported by the theory of the current crowding (CC) due to structural defects inducing non conducting cavities. CC leads to an overestimation of the measured noise parameter in relation to the quality of the interface and/or of the active layer described as follow.

Trapping carriers at defects induce energy barrier modelled by non conducting cavities. In this case [9]:

$$\alpha = \alpha_H \frac{\Omega}{\Omega_{eff}} \quad (5)$$

with Ω and $\Omega_{eff}$ standing for the volume of the full conducting region and of the restricted conducting one respectively, and $\alpha_H$ the noise parameter in homogeneous materials. In this model a constant noise parameter $\alpha_H$ is considered in the whole semiconductor, but a few cavities do not participate to the conductivity due to high energy barriers. The current density is higher near the non conducting cavities than in homogeneous situation, leading to a higher noise parameter. The number of the non conducting cavities remains constant but their dimension decrease (higher $\Omega_{eff}$) with the gate bias. If we consider a circular restricted conducting region at grain boundary (see figure 4) then (5) becomes [9]:

$$\alpha = \alpha_H \frac{H^3}{20\pi a^3} \qquad (6)$$

where H is the grain size and a the radius of the restricted conducting contact region at GB.

At low gate voltages (from weak to moderate inversion) energy barriers are maximum, the current flows preferentially the lowest barriers in restricted contacts regions and then $\alpha>\alpha_H$. At high gate voltages (from weak to strong inversion) the energy barriers decrease, the current density becomes uniform and $\alpha\sim\alpha_H$. Then, for homogeneous materials $\alpha_H/\alpha\sim1$ whereas for disordered materials $\alpha_H/\alpha<<1$ and this ratio can be considered as a quality factor of the polycrystalline silicon and thus as an indicator on the reliability of the TFTs. Next, CC is experimentally demonstrated.

For TFTs operating in the linear mode, it is commonly admitted that the drain current is strongly controlled by (intergranular) energy barriers ($E_B$) accordingly:

$$I_{DS} \approx \frac{W}{L}\mu_{fe0} exp\left(-\frac{E_B(V_{GS})}{kT}\right) C_{ox}(V_{GS}-V_0)V_{DS} \qquad (7)$$

with $\mu_{fe0}$ the optimum carrier field effect mobility at high gate voltages ($E_B<kT$), $C_{ox}$ the gate oxide capacitance per unit area, L(W) the length(width) of the channel, and $V_0$ the gate voltage defined as the gate voltage corresponding to the minimum of drain current of the transfer characteristic $I_{DS}=f(V_{GS})$. Thus, defining the sheet resistance as $R_{sh}=(V_{DS}/I_{DS})(W/L)$, in this case CC is characterized by standing 1/f noise in a relative noise level for a unit area [10]:

$$C_{us} = f\frac{S_{I\,DS}}{I_{DS}^2}WL = KR_{sh} \qquad (8)$$

where $K=\alpha q\mu$ (q elementary charge) with a value of $5\times10^{-21}cm^2/\Omega$ ($=K_{Au}$) obtained for gold resistor, and that can be used as a figure of merit [10]. Plots of $C_{us}$ versus $R_{sh}$ reported in the figure 5 a) for the two types of TFTs show that $K\geq K_{Au}$ and indicate CC on a microscopic scale. Furthermore, we report in the figure 5 b) the plots of $\alpha$ and $\mu_{fe}$ versus $R_{sh}$. $\alpha$ values were previously deduced in function of $V_{GS}$ according to a protocol described in ref [7], and $\mu$ is calculated from the transconductance $g_m=dI_{DS}/dV_{GS}$ measured in the linear mode. The reported values of $\alpha$ are higher than in crystalline silicon (c-Si) MOS transistors (in ref [7] $10^{-6}<\alpha<10^{-2}$), because of a higher defect density in polysilicon TFTs corresponding to $\Omega/\Omega_{eff}>1$ in (5). In addition, plots of the figure 5 a) show that K value is higher for LSPC TFTs than in FSPC TFTs. This is both explained by higher noise parameter and field effect mobility in LSPC devices (figure 5 b). According to (6), higher values of $\alpha$ for LSPC TFTs are related to a higher V/a ratio explained by a higher grain size and/or a lower defect density at the grain boundary, also confirmed by a higher field effect mobility in the laser annealed polysilicon layer.

These results are consistent with those previously observed by analysis of 1/f noise following the theory of T/D

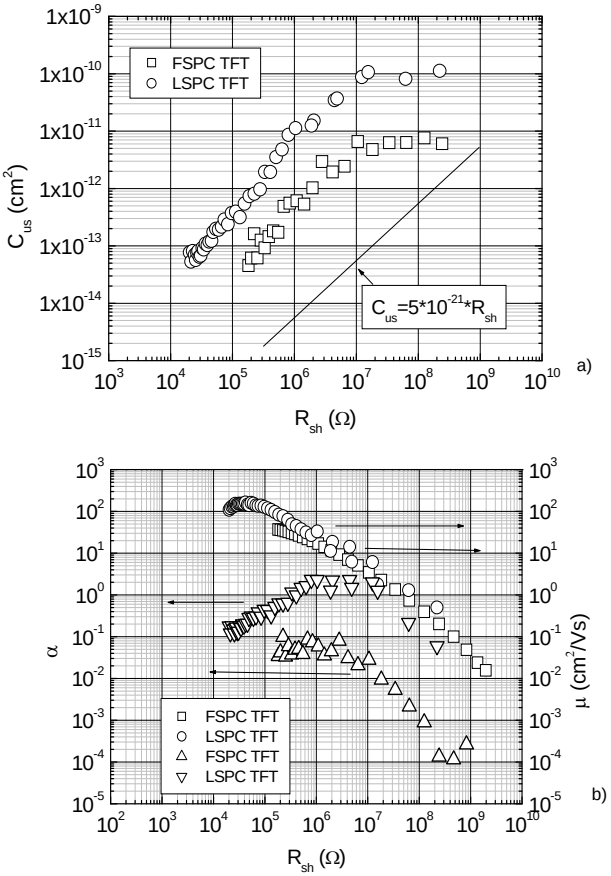


**Figure 5** a) $C_{us}$ versus $R_{sh}$ for FSPC and LSPC TFTs, b) Field effect mobility and noise parameter versus sheet resistance for FSPC and LSPC TFTs.

processes of carriers at oxide traps close to the interface. Therefore, analysis of the 1/f noise following the theory of the CC is also a good diagnostic tool to qualify the active layer.

**4 Concluding remarks** Laser annealing effect of the polysilicon active layer is pointed out on the low frequency noise level in TFTs. Measurements show that noise level is strongly dependent on the gate oxide interface and polysilicon active layer qualities. Analysis shows that noise level can be reduced by improvement of the active layer crystal quality. Therefore, 1/f noise measurement is a good criterion of quality on the microscopic scale of the polysilicon layer, and thus it is a hyperfine diagnostic tool to qualify and to improve TFT technology.

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## References

[1] M. Aoki, T. Hashimoto, T. Yamanaka, T. Nagano, Jap. J. Appl. Phys. **35**, 838 (1196)
[2] L. Pichon, A. Boukhenoufa, C. Cordier, B. Cretu, J. Appl. Phys. **100**, 54504 (2006)
[3] C.A. Dimitriadis, G. Kamarinos, J. Brini, IEEE Elect. Dev. Lett. **22**, 381 (2001)
[4] A. Mercha, L. Pichon, R. Carin, K. Mourgues, O. Bonnaud, Thin Solid Films **383**, 303 (2001)
[5] L.Pichon, K. Mourgues, F.Raoult, T. Mohammed-Brahim, K. Kis-Sion, D. Briand, O. Bonnaud, Semicond. Sci. Technol. 16, 918 (2001)
[6] J. F. Michaud, Ph.D Dissertation, University of Rennes 1, France (2004)
[7] A.Boukhenoufa, L.Pichon, C.Cordier, B.Cretu, L.Ding, R.Carin, J. F. Michaud, T. Mohammed-Brahim, Proceedings of: Noise and Fluctuations: 18th International Conference on Noise and Fluctuations-ICNF 2005, edited by T. Gonzalez, J. Mateos, and D. Pardo, pp 319-322
[8] F. N. Hooge, Physica B **336**, 236 (2003)
[9] A. Mercha, L. K. J. Vandamme, L. Pichon, R. Carin, J. Appl. Phys. 90(8), 4019 (2001)
[10] L.K.J.Vandamme, H.J.Casier, Proceedings of 34th ESSDERC, editors R.P.Mertens and C.L.Claeys, pp 365-368