A Direct Power Injection Model for Immunity Prediction in Integrated Circuits

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***Abstract*— This paper introduces a complete simulation model of a Direct Power Injection (DPI) setup, used to measure the immunity of integrated circuits to conducted continuous-wave interference. This model encompasses the whole measurement setup itself as well as the integrated circuit under test and its environment (printed circuit board, power supply). Furthermore, power losses are theoretically computed, and the most significant ones are included in the model. Therefore, the injected power level causing a malfunction of an integrated circuit, according to a given criterion, can be identified and predicted at any frequency up to 1 GHz. In addition to that, the relationship between immunity and impedance is illustrated. Simulation results obtained from the model are compared to measurement results and demonstrate the validity of this approach.**

***Index Terms*— EMC, IC, DPI, immunity, modeling, simulation**

I. Introduction

NOwadays, the steep growth of mass-market electronic communication systems is the source of numerous electromagnetic disturbances, to which an increasing number of integrated circuits (IC) are becoming more and more susceptible. Indeed, the decrease in geometry length induces a reduction in power supply voltage and, consequently, noise margin. In order to characterize the behavior of these ICs to electromagnetic interference, several measurement methods are currently under standardization process, under the supervision of the International Electrotechnical Commission (IEC), one of which is Direct Power Injection (DPI) [1]. However, these methods rely only on measurements, and thus can not be used for immunity prediction. Therefore, this article introduces a complete electrical model of a DPI setup, making it possible to predict the immunity of an IC (i.e. its ability to withstand electromagnetic interference without exhibiting any malfunction) on a given printed circuit board (PCB) within the design phase.

An example of DPI setup is displayed in Fig. 1. Continuous sine-wave RF power (from 10 MHz to 1 GHz) delivered by a generator is fed into an amplifier and then injected into a pin of the IC under test (either a power pin or a signal input pin) through a capacitor blocking the DC voltage coming from the power supply (hence the name of the test). A directional coupler allows the measurement of incident and reflected powers by the means of two power meters. The IC under test works under normal operating conditions; since the one used in this study is a digital synchronous circuit, it is fed by a clock signal and a data signal, as explained in Sect. IV-D.3.

First of all, a preliminary study of the power transmitted is introduced in Sect. II. Then, Sect. III points out the need for estimating and modeling of power losses in DPI experiments. The electrical model of the DPI setup itself is presented in Sect. IV, each part of the system being analyzed separately. Sect. V deals with the immunity criterion and the simulation algorithm chosen for this study. Finally, simulation results as well as comparisons between measurements and simulations are given in Sect. VI and demonstrate how this electrical model allows the prediction of the immunity of an IC during a DPI experiment.

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II. Theoretical study of transmitted power

The purpose of the DPI experiment is the characterization of the immunity of an integrated circuit as a function of the effective power transmitted to the circuit. However, due to impedance mismatch, most of the RF power delivered by the generator is reflected towards the source, and only a small amount enters the PCB and IC under test. Consequently, the computation of this effective transmitted power is necessary. It relies on the knowledge of the impedance Z_{DUT} of the whole circuit under test, which is extracted from the S_{11} parameter of the circuit obtained from a vector network analyzer (VNA):

$$Z_{DUT} = Z_0 \frac{1 - S_{11}}{1 + S_{11}} \tag{1}$$

in which Z_0 = 50 Ω is the nominal impedance of the analyzer. Then, the incident power can be computed from this impedance and the incident voltage V_{Inc}:

$$P_{Inc} = I_{Z_0}\ V_{Inc} = \frac{{V_{Inc}}^2}{Re(Z_{DUT})} \tag{2}$$

The transmitted power P_{Trans} can then be expressed from the incident power:

$$P_{Trans} = (1 - |S_{11}|^2)\ P_{Inc} \tag{3}$$

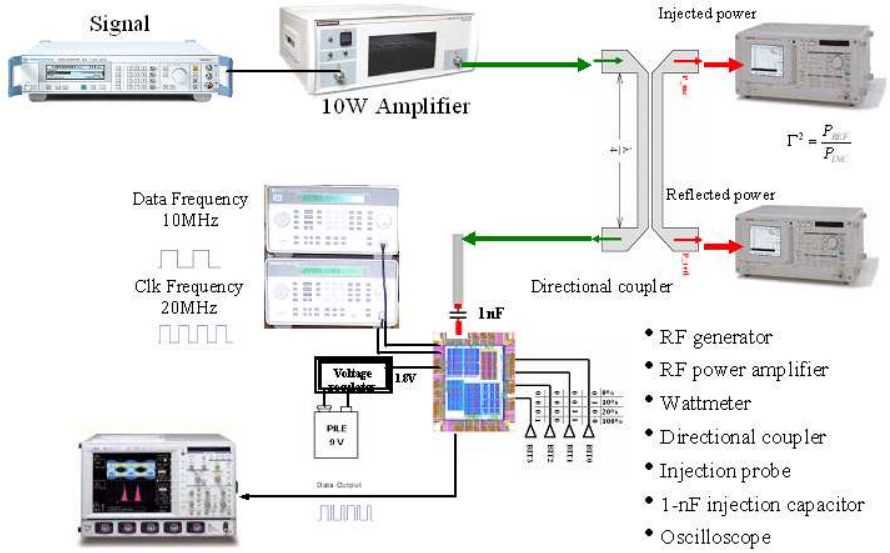

Fig. 1. **DPI injection system**

By replacing the reflection factor by its expression, Eq. 4 is obtained:

$$P_{Trans} = \left(1 - \left|\frac{Z_{DUT} - Z_0}{Z_{DUT} + Z_0}\right|^2\right) \; P_{Inc} \tag{4}$$

By separating the real and imaginary parts of Z_{DUT}, the exact expression of transmitted power can be obtained:

$$P_{Trans} = \frac{4 \; Z_0 \; Re(Z_{DUT})}{|Z_{DUT} + Z_0|^2} \; P_{Inc} \tag{5}$$

The expression in Eq. 5 is well suited to the calculation of P_{Trans} from measurements, owing to the use of power meters in DPI experiments. However, it is unusable for DPI electrical modeling and simulation, since power generators are not available in common circuit simulators. A convenient solution consists in using a RF voltage source, and expressing the transmitted power as a function of source voltage instead of injected power. This can be achieved by combining Eq. 2 and Eq. 5:

$$P_{Trans} = \frac{4 \; Z_0}{|Z_{DUT} + Z_0|^2} \; {V_{Inc}}^2 \tag{6}$$

These expressions will be used in Sect. VI-A in order to build up immunity plots (in dBm) from electrical simulation results (in V).

III. Power losses in Direct Power Injection

A. Theoretical estimation of power losses by the Q-factor method

During a DPI experiment, considerable RF power may be injected into the populated PCB. However, only a small amount of this power actually enters the IC under test, the remainder being either dissipated in other discrete components or lost. From 10 MHz to 1 GHz, these power losses are due to many different phenomena: conductive losses, dielectric losses, radiation, surface waves. A convenient approach to estimate the relative contributions of these losses is the use of the quality factor [2].

1) Conductive losses: An approximated formula for the quality factor due to conductive losses in a PCB track is given in [3]:

$$Q_c \approx \frac{h}{\delta_s} \approx h\sqrt{\frac{\pi \; \mu_0 \; \mu_r}{\rho}} \; \sqrt{f} \tag{7}$$

in which h is the thickness of the cavity represented by the whole PCB, and δ_s is the skin depth. $\rho \; = 1.72 \cdot 10^{-8} \; \Omega \cdot m$ is the resistivity of copper, $\mu_0 \; = 4\pi \cdot 10^{-7} \; H \cdot m^{-1}$ the permeability of vacuum and μ_r = 1 the relative permeability of copper. As expected, Q_c is proportional to the square root of f, the injection frequency. Its values are shown for different frequencies in table I.

2) Dielectric losses: The quality factor of dielectric losses in a FR4 board is given in [3]:

$$Q_d = \frac{1}{\tan\delta} \tag{8}$$

in which $\tan\delta \approx 0.02$ [4] is the loss tangent of the PCB material. Its value depends on the injection frequency [5], but remains approximately constant in high frequency for FR4 material.

3) Radiated losses: Radiated losses can be computed from the cavity model of a PCB [6]. Their quality factor, for the dominant TM_{10} mode on rectangular PCBs, can be expressed by:

$$Q_{rad} \approx \frac{3 \; \varepsilon_r \; L_e \; \lambda_0}{16 \; p \; c_1 \; W_e \; h} \approx \frac{3 \; c \; L_e}{16 \; p \; c_1 \; h \; W_e}\sqrt{\frac{\mu_r}{\varepsilon_r}} \; \frac{1}{f} \tag{9}$$

in which h = 1.6 mm is the thickness of the cavity represented by the whole PCB, ε_r = 4.4 the relative permittivity of the dielectric (FR4), μ_r = 1 the relative permeability of the PCB, L_e and W_e the effective dimensions of the PCB (10.3 cm

square). λ_0 is the wavelength of the electromagnetic wave in the PCB:

$$\lambda_0 = \frac{c}{n_1\ f} = \frac{c}{\sqrt{\varepsilon_r\ \mu_r}\ f} \tag{10}$$

Dimensionless values p = 0.82 and c_1 = 0.25 are computed using Eq. 11 given in [6]:

$$p = 1 + \frac{a_2}{10}\ (k_0\ W_e)^2 + \frac{3}{560}\ ({a_2}^2 + 2a_4)\ (k_0\ W_e)^4 + \frac{1}{5}\ c_2\ (k_0\ L_e)^2 + \frac{1}{70}\ a_2\ c_2\ (k_0\ W_e)^2 (k_0\ L_e)^2 \tag{11}$$

with a_2 = -0.16605, a_4 = 0.00761, c_2 = -0.0914153, and

$$c_1 = \frac{1}{{n_1}^2} + \frac{2}{5\ {n_1}^4} = \frac{1}{\varepsilon_r\ \mu_r} + \frac{2}{5\ (\varepsilon_r\ \mu_r)^2} \tag{12}$$

It can be seen that Q_{rad} is inversely proportional to frequency.

4) Summary of losses: The overall quality factor for the PCB and the integrated circuit is given by:

$$\frac{1}{Q_f} = \frac{1}{Q_c} + \frac{1}{Q_d} + \frac{1}{Q_{rad}} \tag{13}$$

Table I illustrates the values of conductive, dielectric, radiated and overall quality factors at various frequencies, which are valid for the TM_{10} cavity mode.

$f_{inj}[MHz]$	Q_c	Q_d	Q_{rad}	Q_f
410	490.7	50	4693	44.94
500	542	50	3847	45.24
530	558	50	3630	45.31
650	618	50	2960	45.54
850	706.6	50	2263	45.75

TABLE I

Q-FACTORS FOR POWER LOSSES

It can be seen that the lowest quality factors, corresponding to the highest losses, are Q_d and Q_c. Therefore, only dielectric and conductive losses will be modeled, since the DPI experiment is valid up to 1 GHz.

B. Modeling of conductive and dielectric power losses

The objective of this study is to develop an electrical simulation model for a complete DPI setup, making it possible to use conventional SPICE-based simulators. This electrical simulation thus requires equivalent electrical models for power losses, which must be expressed as equivalent impedances. The following section deals with the buildup of these equivalent loss models.

In the DPI experiment, RF power is injected into a pin of the IC by a feed port, which is modeled as a 0.2215 mil-sided square [7]. Since the IC is located precisely at the center of the PCB, and the dimensions of the IC package are relatively small compared with the ones of the PCB, the injection point can be considered to be located at the center of the PCB by first approximation. Moreover, the spacing between both planes of the PCB under test (1.6 mm) is much smaller than the dimensions of the board (103 mm). Therefore, it can be considered that the electromagnetic field propagates in a radial direction outward from the source [4]. As a result, a circular parallel plane structure made of imperfect conductors is used (Fig.2).

Furthermore, a rectangular microstrip patch structure with an electrically small w-wide current strip can be replaced by a cylindrical current source with a radius equal to one-fourth of w [6]. Then, the radius r_0 of this cylindrical current source is equal to 0.02756 mils.

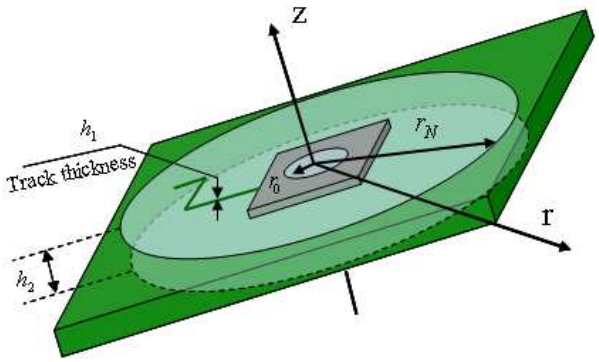

Fig. 2. **Discretization of power losses**

This structure is discretized into an array of circular rings with the same width Δr, each circular ring representing one segment of the proposed model. The equivalent impedance per unit length $Z_c(r)$ of a ring is given in Eq. 14 ([7], [8]):

$$Z_c(r) = \frac{1+j}{\pi\ \sigma\ \delta_s\ r} \tag{14}$$

in which r represents the radial distance from the injection point, $\sigma = 5.96 \cdot 10^7\ S \cdot m^{-1}$ the conductivity of copper and δ_s the skin depth according to Eq. 7.

$Z_c(r)$ can be splitted into two equivalent devices $R_c(r)$ (resistance) and $L_c(r)$ (inductance) in series given by Eq. 15 and 16:

$$R_c(r) = \frac{1}{\pi\ \sigma\ \delta_s\ r} = \frac{1}{r}\sqrt{\frac{\mu_0\ \mu_r}{\pi\ \sigma}}\ \sqrt{f} \tag{15}$$

$$L_c(r) = \frac{1}{2\pi^2\ f\ \sigma\ \delta_s\ r} = \frac{1}{2\pi\ r}\sqrt{\frac{\mu_0\ \mu_r}{\pi\ \sigma}}\ \frac{1}{\sqrt{f}} \tag{16}$$

Then, the values of $R_c(r)$ and $L_c(r)$ are multiplied by Δr in order to obtain the whole model used for conductive losses. This model is shown in Fig. 3.

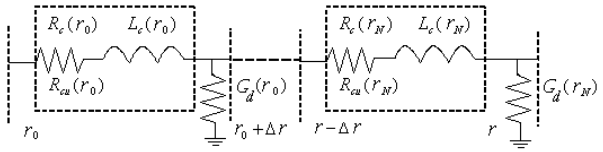

Fig. 3. **Equivalent electrical model of conductive and dielectric power losses**

Dielectric losses can be modeled by a conductance shown in Fig.3 and given by Eq. 17:

$$G_d(r) = \frac{2\pi\ \varepsilon_0\ \varepsilon_r\ r\ \tan\delta}{h}\ \omega = \frac{4\pi^2\ \varepsilon_0\ \varepsilon_r\ r\ \tan\delta}{h}\ f \tag{17}$$

As expected, it can be seen that dielectric losses are proportional to frequency, even if the associated quality factor is a constant. Above a given frequency, these dielectric losses can prevail over conductive losses. It can be noted that the values of these equivalent elements are frequency-dependent and thus can not be modeled as plain resistors and inductors. Therefore, behavioral electrical models (coded in VHDL-AMS) will be used later in the simulation process.

IV. Electrical model of the DPI setup

Since the evaluation of the immunity of the integrated circuit under test requires an exact knowledge of the power actually injected into the circuit, it is necessary to model the whole DPI setup very accurately. Therefore, each part of the setup (injection probe, injection capacitor, PCB, IC and directional coupler) must be modeled separately as equivalent passive elements; these individual models must then be combined in order to obtain the whole equivalent model.

A. Modeling of the injection probe

The injection probe of a DPI setup is essentially a coaxial cable with a copper core, but its impedance is not 50 Ω in this case. Each part of the injection system (injection probe, connection between the probe and the PCB ground) was measured and modeled separately from measurements obtained with the help of a vector network analyzer (VNA). The model of the injection probe is inductive, with a low series resistance. This probe is attached to the IC under test through a capacitor which will be modeled later, but its outer connector is soldered on the ground plane of the PCB. Consequently, the inner wire of the probe is coupled with the ground plane through a capacitance and a resistance, representing the dielectric of the coaxial cable. Moreover, the equivalent inductance of the small wire connecting the core of the cable with the IC pin is included in the model. Fig. 4 depicts a schematic of the injection probe as well as its equivalent electrical model, while Tab. II summarizes the actual values of its equivalent elements.

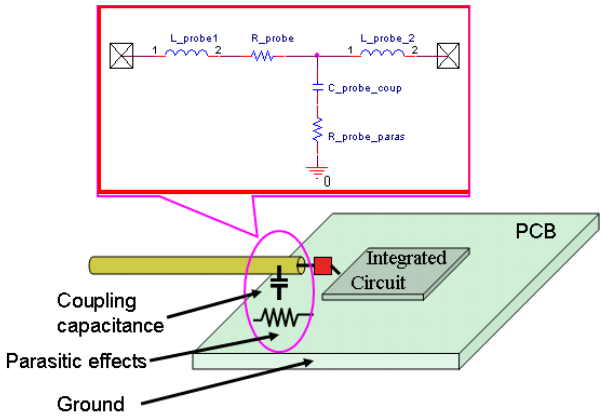

Fig. 4. **Schematic and equivalent model of the injection probe**

Elements	Values	Elements	Values
L-probe-1	2.05 nH	L-probe-2	3.4 nH
R-probe	1.06 Ω	C-probe-coupl	0.85 pF
R-probe-paras	300 Ω		

TABLE II
EQUIVALENT ELEMENTS OF THE INJECTION PROBE

B. Modeling of injection and decoupling capacitors

The DPI setup includes two discrete capacitors: a 1 nF injection capacitor, used to prevent the reinjection of the DC voltage supplied by the board into the RF power amplifier, and a 47 nF decoupling capacitor located on the PCB. An accurate impedance measurement of these capacitors can be achieved thanks to an Agilent® N1020A probe connected to a VNA. These ceramic SMD capacitors can be modeled by a series RLC network. Fig. 5 plots the simulated, fitted impedance profile of the injection capacitor, along with its equivalent model.

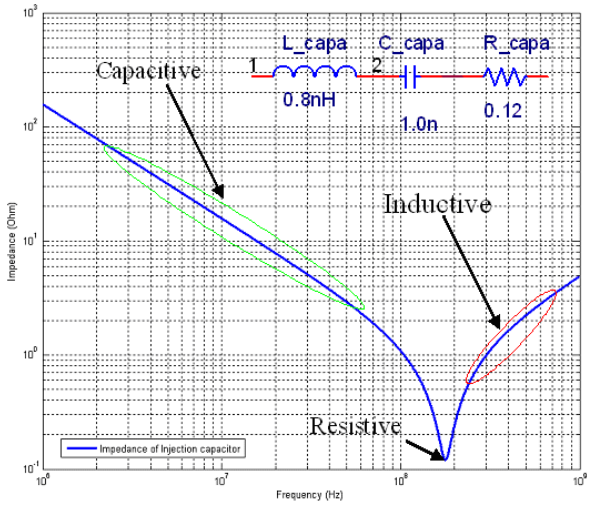

Fig. 5. **Impedance profile and equivalent model of the injection capacitor**

The equivalent inductance can be computed from Eq. 18:

$$L = \frac{1}{4\pi^2 \ {f_{res}}^2 \ C} \tag{18}$$

in which f_{res} is the resonant frequency of the capacitor. The same operation can be reiterated for the decoupling capacitor. The equivalent elements of both capacitors are shown in Tab. III.

Elements	Value	Elements	Value
C-capa	1.0 nF	C-decoup	47 nF
R-capa	0.12 Ω	R-decoup	0.2 Ω
L-capa	0.8 nH	L-decoup	1.88 nH

TABLE III
EQUIVALENT ELEMENTS OF THE INJECTION AND DECOUPLING CAPACITORS

Since the injection capacitor is soldered directly on the pin of

the IC and the injection probe, no track length has to be taken into account. Likewise, the decoupling capacitor is located under the V_{dd}/V_{ss} power pin pair of the IC, with less than 1 mm track length. This is included in the capacitor model.

C. Modeling of the PCB under test

In this study, the DPI setup does not follow the standard proposal [1]. The custom-designed PCB (called ALI) (Fig. 6) includes its own power supply, composed of a 9 V battery and several regulators, including a 1.8 V regulator for the digital core and IOs of the IC, the only one to be modeled in this case. Conversely, the standard proposal requires the use of an external power supply, with a choke inductor in series preventing the reinjection of RF power into the supply. Since most industrial boards include their own power supplies, this case study may be closer to industrial requirements than the typical DPI setup of the proposal. The key issue of the study is that it can be supposed that a non-negligible amount of the incident RF power is in fact injected into the power supply of the board, and not in the IC or even in the decoupling capacitor. This assertion will be demonstrated in Sect. VI-A. The regulator, the battery and the PCB tracks (including vias) were modeled by series RLC networks. In particular, the

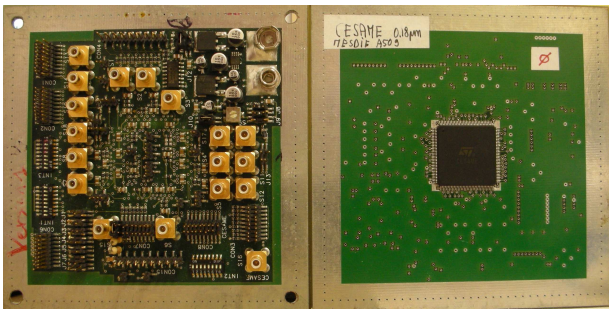

Fig. 6. **ALI board (left: connector side, right: IC side)**

inductances of the V_{dd} and V_{ss} tracks, both located over a ground plane, were established thanks to Eq. 19 [9]:

$$L_{V_{dd}} = L_{V_{ss}} = \frac{\mu_0\ \mu_r\ l}{2\ \pi} \ln\left(\frac{8h}{w} + \frac{w}{4h}\right) \qquad (19)$$

in which l and w are respectively the length and the width of the track, h the distance between the track and the ground plane. On this PCB, w = 300 μm and h varies between 0.5 mm and 1.5 mm depending on the routing layer. Fig. 7 depicts the whole model of the PCB, including the decoupling capacitor modeled previously, while Tab. IV outputs the values of all passive elements of the model.

It can be seen that the series inductance of the V_{dd} track (including the regulator) is quite high. Therefore, the amount of RF power injected into the power supply of the board should decrease in high frequency. Likewise, the series inductance of the decoupling capacitor should reduce the absorption of RF power in high frequency. Consequently, more RF power is supposed to be injected into the IC itself as frequency increases.

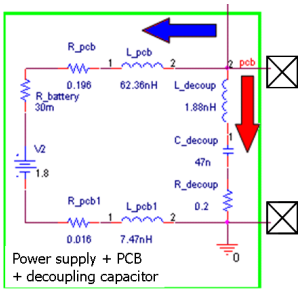

Fig. 7. **Model of the whole PCB and power supply, including the decoupling capacitor**

Elements	Values	Elements	Values
C-decoup	47 nF	R-pcb-vdd	0.196 Ω
R-decoup	0.2 Ω	R-pcb-vss	0.016 Ω
L-decoup	1.88 nH	L-pcb-vdd	62.35 nH
R-battery	30 mΩ	L-pcb-vss	7.47 nH

TABLE IV
EQUIVALENT ELEMENTS OF THE WHOLE PCB AND POWER SUPPLY

D. Modeling of the integrated circuit

1) Introduction: The CESAME integrated circuit [10] was designed at INSA Toulouse (France) and fabricated by ST Microelectronics® in 0.18 μm technology. It is composed of six logic cores, with a total of 610000 transistors. All cores are identical from a functional point of view, however, they differ in the design of their power supply architectures (plain, RC decoupling, substrate isolation, meshed power supply rails).

2) Package model: CESAME is encapsulated in a TQFP144 package. The electrical model of this package was obtained from a 3D electromagnetic simulation with HFSS® (Ansoft®) [11] and verified at INSA Toulouse with ASERIS-EMC2000® (EADS-CCR®) [12]. Fig. 8 displays the whole model. The leftmost part of the model represents the lead-frame, and the rightmost part represents the bonding and the pads.

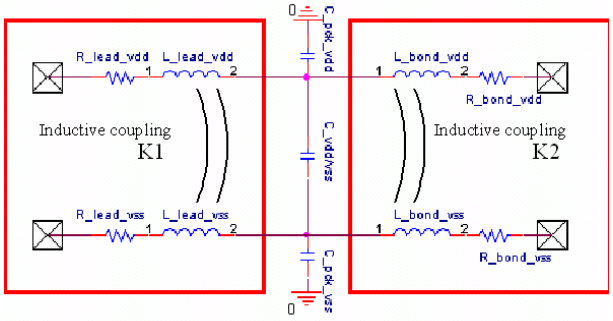

Fig. 8. **Package model**

In order to compute the inductances of the leadframe and the bonding, it can be noted that the V_{dd} and V_{ss} pins are adjacent on the package, which implies that the current return path can be easily determined. Therefore, their equivalent inductances

can be computed from Eq. 20 [9]:

$$L_{V_{dd}} = L_{V_{ss}} = \frac{\mu_0\ \mu_r\ l}{2\ \pi} \ln\left(\frac{4h}{d}\right) \tag{20}$$

in which l and d are respectively the length and the diameter of the leadframe or the bondwire, and h its distance to the ground plane.
Then, the C-vdd/vss coupling capacitance between both power supply rails (C_{12} on Fig. 9) can be computed from Eq. 21 [13]:

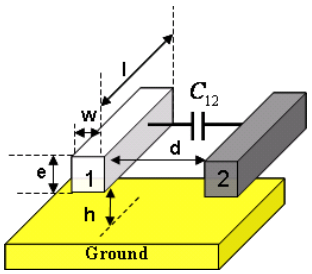

Fig. 9. **Capacitive coupling between supply rails**

$$C_{12} = \varepsilon_0\ \varepsilon_r\ l \left[\frac{e}{d} + 1.21\left(\frac{e}{h}\right)^{0.1} \left(\frac{d}{h} + 1.15\right)^{-2.22} + 0.25\ \ln\left(1 + 7.17\frac{w}{d}\right) \left(\frac{d}{h} + 0.54\right)^{-0.64}\right] \tag{21}$$

Tab. V summarizes the values of the package model.

Elements	Value	Elements	Value
R-lead-vdd	56 mΩ	R-lead-vss	56 mΩ
L-lead-vdd	5 nH	L-lead-vss	5 nH
L-bond-vdd	6 nH	L-bond-vss	6 nH
R-bond-vdd	56 mΩ	R-bond-vss	56 mΩ
C-pck-vdd	0.45 pF	C-pck-vss	0.45 pF
C-vdd/vss	0.67 pF		

TABLE V
EQUIVALENT ELEMENTS OF THE PACKAGE AND BONDING

In addition to that, intra-IC inductive coupling between V_{dd} and V_{ss} (Fig. 8) is an important factor which widely influences the amount of RF power actually injected into the die [14]. The mutual inductance between both rails is given by Eq. 22, and the coupling factor by Eq. 23:

$$M_{V_{dd}/V_{ss}} = \frac{\mu_0\ \mu_r\ l}{2\pi} \ln\left[\frac{(d+4w)^2 + (1.5w+2h)^2}{(d+w)^2 + (1.5w)^2}\right] \tag{22}$$

$$K_M = \frac{M_{V_{dd}/V_{ss}}}{\sqrt{L_{V_{dd}}\ L_{V_{ss}}}} \tag{23}$$

in which d, w and h are shown in Fig. 9. In Tab. VI, K_1 represents the coupling factor between both leadframes, K_2 the inductive coupling between both bondwires.

K_1	K_2
0.65	0.66

TABLE VI
V_{dd} TO V_{ss} INDUCTIVE COUPLING

3) Modeling of CESAME cores: The transistor netlist of the NORM core in the CESAME chip (chosen for this paper) includes 240 identical base cells, each one containing about 400 transistors. In order to speed up time-domain simulation, only one base cell (reference cell) is included in the whole netlist. The remaining cells are replaced by an equivalent parallel RC model representing the impedance of all CMOS transistors. This model is itself in parallel with the reference cell (Fig. 10).

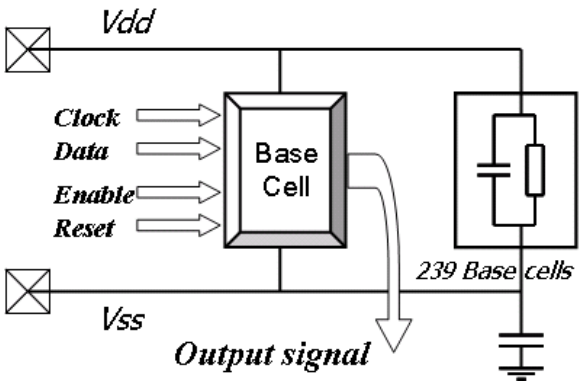

Fig. 10. **Model of the CESAME core for immunity simulation**

The reference cell is fed with a 20 MHz clock signal and a square 10 MHz data signal, and the output of the cell can be directly observed on an output pin of the chip.
The parasitic elements of the pads and the on-die power supply rails are then modeled using the same methodology as the one used for the package. The inductance of the V_{dd} and V_{ss} supply rails can be computed from Eq. 24 [9]:

$$L_{V_{dd}} = L_{V_{ss}} = \frac{\mu_0\ \mu_r\ l}{2\pi} \ln\left(\frac{4h}{w} + 1\right) \tag{24}$$

Moreover, the surface of the CESAME die is 10 mm^2, it is located about 1 mm above the ground plane, thus leading to an additional C_core/pcb = 500 fF coupling capacitance between the substrate and the ground.
Two on-chip current sensors [10] are located on the supply rails and are represented by 1.7 Ω resistors.

E. Modeling of the directional coupler

The directional coupler used for power measurements can be identified as a 50 Ω lossless transmission line. Its propagation time T_d is computed using Eq. 25:

$$T_d = Z_0\ C_0 = 2538\ \text{ps} \tag{25}$$

in which C_0 is measured with a VNA in Smith chart mode.
The coupler has a very strong influence on the global

impedance profile of the setup. Unfortunately, it is integrated in the power amplifier and can not be removed for DPI measurement purposes (only for impedance measurement). Therefore, simulations and measurements will always take this coupler into account.

F. Complete electrical model of the DPI setup

By assembling all the models computed previously, a complete electrical SPICE model of the DPI setup can be established, which is depicted in Fig. 11.
As demonstrated in section III-B, conductive losses are represented by additional RL networks in series with the injection capacitor. These are behavioral models which can be coded in VHDL-AMS [15] for transient and AC simulations, which makes it easier to include frequency-dependent behaviors.
Moreover, P1 represents the power injected into the PCB, P2 the power injected into the decoupling capacitor and P3 the power injected into the IC. P-net is the power delivered to the core of the IC.
An AC simulation allows the extraction of the global impedance plot, with and without the directional coupler (Fig. 12).
As can be seen, the directional coupler shifts the impedance plot to the left and adds parasitic resonances, which demonstrates the importance of its proper modeling. Fig. 13 plots a comparison between the simulated impedance profile and the measurement performed on the experimental setup, which shows a very good correlation.

V. Methodology for immunity simulation

A. Definition of an immunity criterion

The definition of immunity criteria for integrated circuits is still a prominent issue, due to the very wide range of IC functionalities. In this study, a common criterion for the immunity of digital circuits, suggested in the DPI and the WBFC (WorkBench Faraday Cage) standard proposals, was chosen [1] [16]; the circuit is considered as perturbed if:

- either the ripple voltage of the data output of the reference cell crosses the $\pm 20\%$ boundary when established at a given logic level,
- or a jitter greater than $\pm 10\%$ is observed on the edges of the data output with respect to the original signal

B. Simulation algorithm

The DPI simulation algorithm is based on the standard DPI measurement procedure (Fig. 14). For each injection frequency (from 10 MHz to 1 GHz in 10 MHz steps, as suggested in the standard proposal), a time-domain simulation is performed. During this simulation, the injected power is increased continuously, until either the immunity criterion is met or the maximum injection power (40 dBm) is reached. The exact power level is then recorded, and the whole data set is plotted versus frequency. Simulations are performed with ADVance-MS Mach® (Mentor Graphics®) [17]. The transistor netlist of a base cell is used along with the model of the whole power supply network, with approximated transistor models for confidentiality reasons. The whole simulation diagram is displayed in Fig. 15.

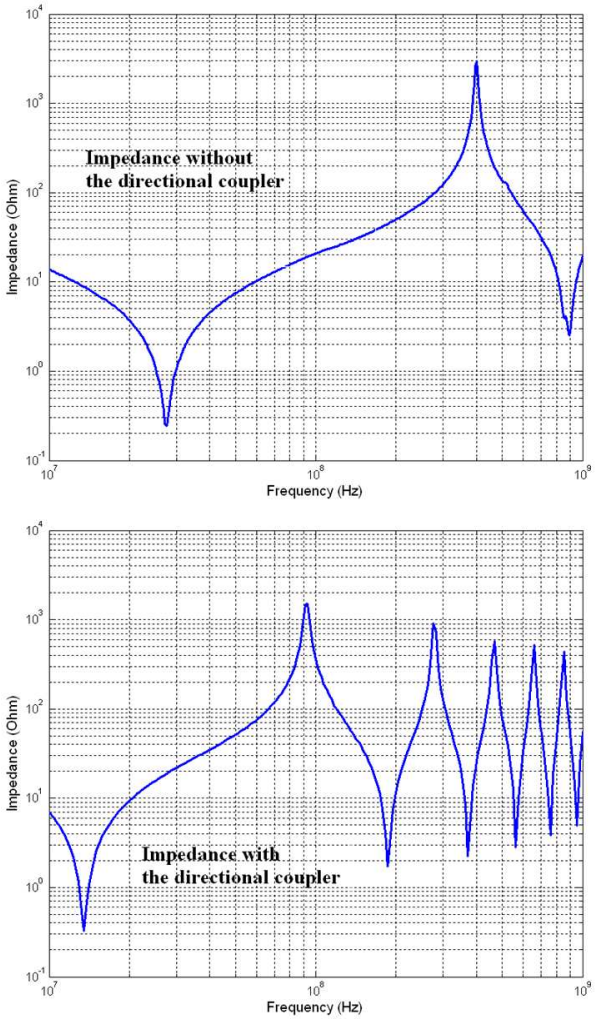

Fig. 12. **Simulated impedance profile of the whole DPI setup, without (top) and with (bottom) the directional coupler**

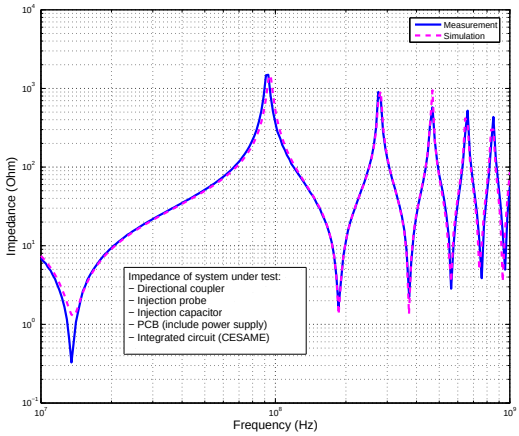

Fig. 13. **Simulated (dashed line) and measured (solid line) impedance profiles of the DPI setup**

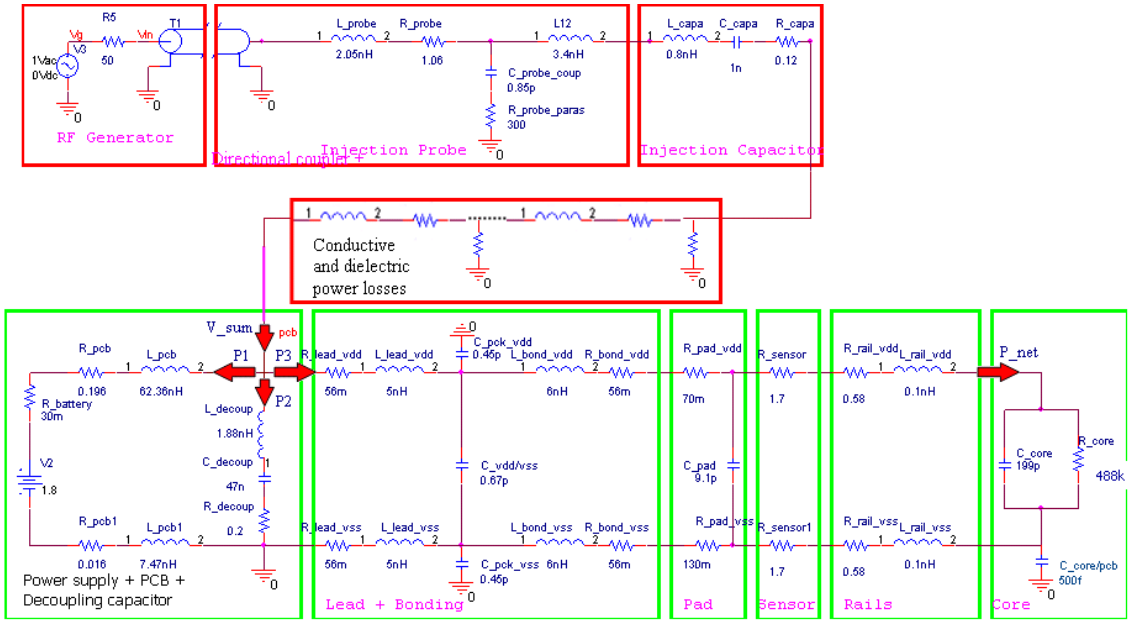

Fig. 11. **Complete electrical model of the DPI setup**

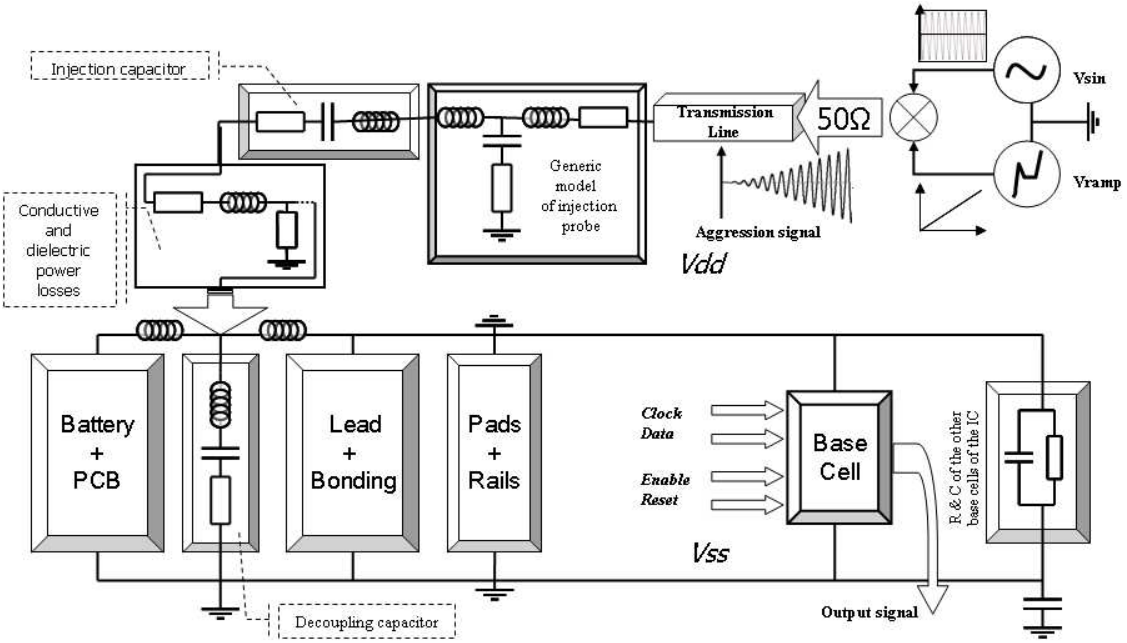

Fig. 15. **Complete DPI diagram for time-domain simulation**

As can be seen, the power generator used in measurement is replaced by a sine-wave voltage generator, the amplitude of which is multiplied by a slower ramp (1 μs rise time). The amplitude of the resulting signal thus increases from 0 to 22.36 V (corresponding to 40 dBm on a 50 Ω load). The effective transmitted power can then be computed from Eq. 26 and the reflected power from Eq. 27:

$$P_{inj} = I_{inj}\ U_{inj} \tag{26}$$

$$P_{ref} = P_{inj} - P_{tran} \tag{27}$$

VI. Results

A. Immunity simulation

A first immunity simulation, as described in the previous section, was performed from 10 MHz to 1 GHz. In order to speed up simulation, the frequency-dependent loss models described in Sect. III-B were not included. Fig. 16 plots the simulation results obtained without the coupler, in order to eliminate the parasitic role of the latter. It represents the power necessary to cause a malfunction of the integrated circuit as a function of frequency. Of course, no comparison with

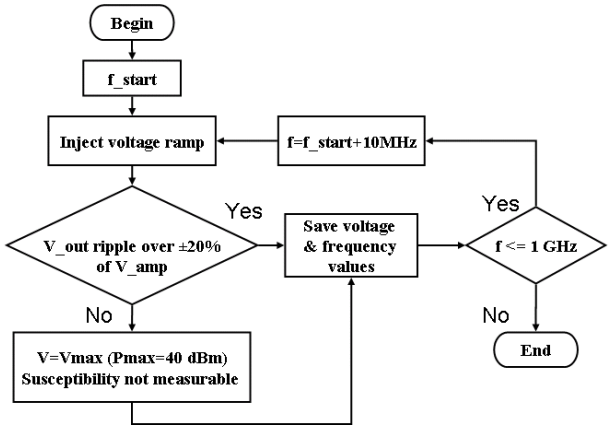

Fig. 14. **DPI simulation algorithm**

measurements is possible at this stage.

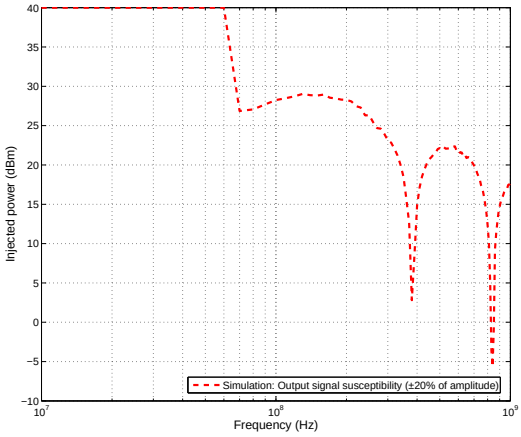

Fig. 16. **Immunity simulation without the directional coupler**

It can be noted that:

- below 70 MHz, the maximum available power level (40 dBm) is even too low to measure the immunity of the board,
- above this frequency, the high-susceptibility frequencies match the resonances and antiresonances of the impedance profile of the board (Fig. 12, top).

This can be explained by plotting the simulated power injected into the power supply for a constant 1 W power delivered by the generator (Fig. 17). Below 70 MHz, a substantial amount of injected power flows through the power supply, and thus does not enter the integrated circuit, which of course can not be perturbed.

B. Comparison between simulations and measurements for the lossless model

Fig. 18 shows a comparison between experimental measurements and simulations (with the directional coupler, but still without any loss models). A very good frequency matching of strong and weak immunity points can be observed, which

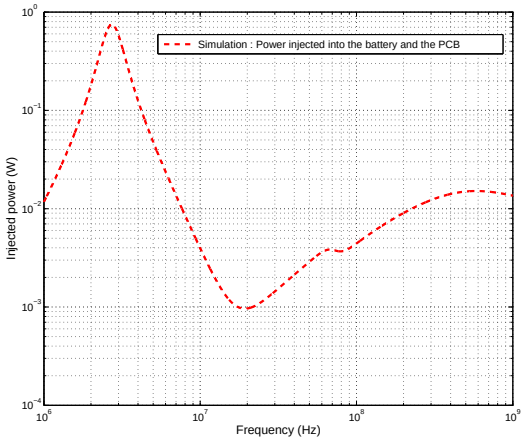

Fig. 17. **Power injected into the power supply for a 1 W incident power (simulation)**

clearly demonstrates the relationship between the impedance profile and the immunity profile.

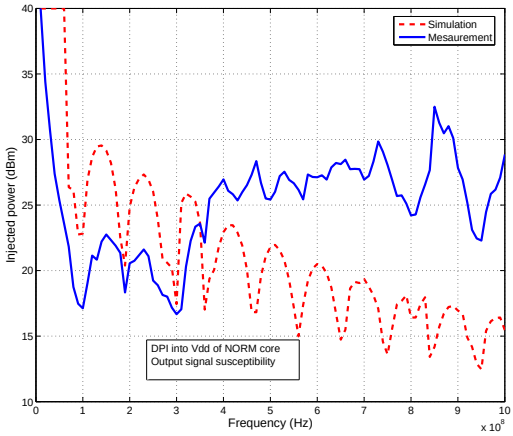

Fig. 18. **Immunity simulation (dashed line) and measurement (solid line) for the lossless DPI model**

However, it is also clear that, the simulation being about 20 dBm below the measurement above 360 MHz, it is necessary to take into account power losses within the setup.

C. Measurement of radiated losses

In order to validate the absence of radiated losses, another measurement was performed by introducing the whole PCB (with the injection probe and capacitor) into a GTEM cell while performing the DPI experiment (Fig. 19).

The GTEM cell is used essentially to measure the energy coupled into a given mode of the cell. In order to separate the resonances of the GTEM cell from those of the DUT, the S_{21} transmission parameter of the GTEM cell was measured, and its results did not show up any interference between both resonance categories.

Measurement results, plotted in Fig. 20, demonstrate that:

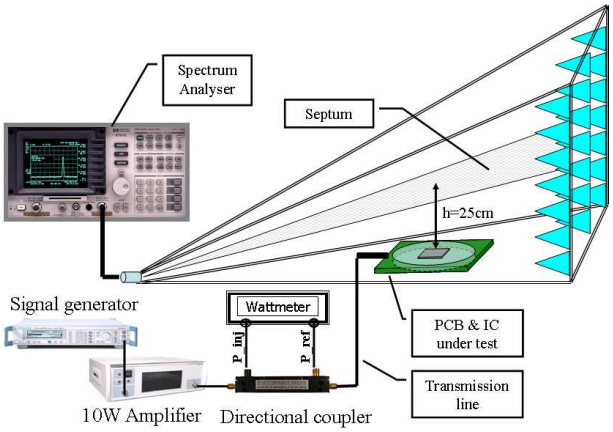

Fig. 19. **Measurement setup for radiated losses in GTEM cell during DPI experiment**

- the amount of radiated power is negligible, as demonstrated before,
- the radiated power varies as the inverse of the impedance profile of the board, which is an expected result since high impedance points correspond to low current flows (for a constant voltage), and vice versa.

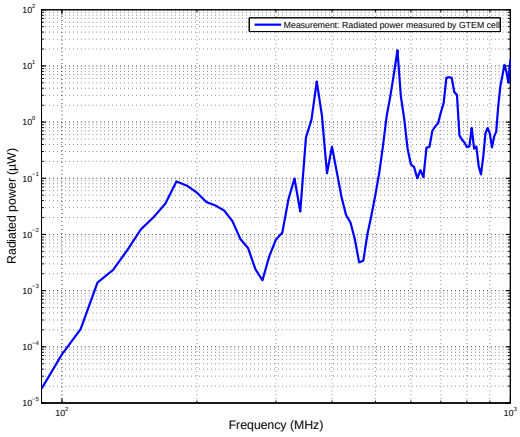

Fig. 20. **Radiated power measured in the GTEM cell during DPI experiment**

D. Comparison between simulations and measurements for the lossy model

The second simulation set includes the whole DPI model, with conductive and dielectric loss models. Fig. 21 depicts the comparison between experimental measurements (same as in Fig. 18) and new simulation results.

The correlation between both results is better than 8 dBm below 360 MHz, and almost perfect in amplitude above. However, small frequency shifts can be observed; they are mainly due to little differences between simulated and measured impedance profiles (Fig. 12) which are easier to read on a linear frequency axis.

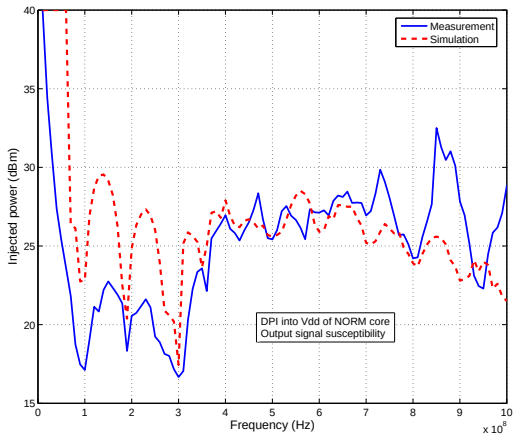

Fig. 21. **Immunity simulation (dashed line) and measurement (solid line) for the lossy DPI model**

This comparison clearly demonstrates the relationship between the high- and low-immunity frequencies of a system under DPI test and its impedance profile.

VII. Conclusion

In this article, a complete electrical model of a Direct Power Injection (DPI) setup was presented. Each part of the system (directional coupler, injection probe, injection capacitor, power supply, PCB, IC) was characterized and modeled, with a special attention given to power distribution. Then, a theoretical study of electrical losses clearly demonstrated that only conductive and dielectric losses must be taken into account in the frequency range of the DPI standard, and a behavioral electrical model of these losses was added to the DPI model. Immunity simulations were performed using the complete electrical model, and compared with experimental results. They demonstrate that there is a strong relationship between the impedance profile and the immunity profile of the system under test, and that an accurate prediction of immunity levels can be achieved by simulation, provided that losses are taken into account.

In a near future, other immunity tests such as near-field injection and very fast transmission-line pulse (VF-TLP) will be performed on the same PCB and IC, and their results will be compared with those obtained in this article. Equivalent electrical models of these experiments are expected to be implemented.

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REFERENCES

[1] IEC EMC Task Force. IEC62132-3 : Direct RF power injection to measure the immunity against conducted RF-disturbances of integrated circuits up to 1 GHz. Draft technical report, IEC, August 2001.

[2] M. Xu and T.H. Hubing. Estimating the power bus impedance of printed circuit boards with embedded capacitance. *IEEE Transactions on Advanced Packaging*, 25(5):424–432, November 2002.

[3] C.A. Balanis. *Antenna Theory : Analysis and Design*. Wiley, third edition, 2005.

[4] H.W. Shim and T.H. Hubing. A closed-form expression for estimating radiated emissions from the power planes in a populated printed circuit board. *IEEE Transactions on Electromagnetic Compatibility*, 48(1):74–81, February 2006.

[5] J.H. Jang, N. Ishitobi, B.C. Kim, and G.J. Seung. Effects of microstructural defects in multilayer LTCC stripline. *IEEE Transactions on Advanced Packaging*, 29(2):314–319, May 2006.

[6] K.F. Lee and W. Chen. *Advances in Microstrip and Printed Antennas*. Wiley, first edition, 1997.

[7] M. Xu and T.H. Hubing. Application of the cavity model to lossy power-return plane structures in printed circuit boards. *IEEE Transactions on Advanced Packaging*, 26(1):73–80, February 2003.

[8] J.C. Parker. Via coupling within parallel rectangular planes. *IEEE Transactions on Electromagnetic Compatibility*, 39(1):17–23, February 1997.

[9] E. Sicard. *Le Couplage Diaphonique dans les Circuits CMOS Submicroniques*. Habilitation à diriger des recherches (in French), INSA de Toulouse, 1998.

[10] B. Vrignon, S. Ben Dhia, E. Lamoureux, and E. Sicard. Characterization and modeling of parasitic emission in deep submicron CMOS. *IEEE Transactions on Electromagnetic Compatibility*, 47(2):382–387, May 2005.

[11] Ansoft Corporation. HFSS. http://www.ansoft.com/.

[12] EADS-CCR. ASERIS-EMC2000. http://www.aseris-emc2000.com/.

[13] N. Delorme, M. Belleville, and J. Chilo. Inductance and capacitance analytic formulas for VLSI interconnects. *IEE Electronics Letters*, 32(11):996–997, May 1996.

[14] H.B. Bakoglu. *Circuits, Interconnects and Packaging for VLSI*. Addison-Wesley, first edition, 1990.

[15] R. Perdriau, M. Ramdani, J.L. Levant, and A.M. Trullemans. EMC evaluation in integrated circuits using VHDL-AMS. In *IEEE International Symposium on Industrial Electronics (ISIE)*, May 2004.

[16] IEC EMC Task Force. IEC62132-4 : Measurement of electromagnetic immunity of integrated circuits in the range 150 MHz to 1 GHz : Workbench faraday cage. Draft technical report, IEC, September 1998.

[17] Mentor Graphics Corporation. ADVance-MS. http://www.mentor.com/.

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