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# THERMAL DEPENDENCE OF LOW-FREQUENCY NOISE IN POLYSILICON THIN FILM TRANSISTORS

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## Abstract

Thermal dependence of low frequency noise in low temperature ( $\leq 600^\circ\text{C}$ ) polysilicon thin film transistors is studied in devices biased from weak to moderate inversion and operating in the linear mode. Drain current noise spectral density, measured in the temperature range from 260K to 310K, is thermally activated following the Meyer Neldel rule. Analysis of the thermal activation of noise, supported by the theory of trapping/detrapping processes of carriers into oxide traps located close to the interface, leads to the calculation of the deep state interface distribution in function of the Meyer Neldel characteristic energy.

## 1. Introduction

Polysilicon thin-film transistors (TFTs) are key elements for flat panel displays and flexible electronics because of their high potential usefulness in driving circuits and/or in addressing pixels. However, some improvements remain in TFT technology because the electrical properties are strongly affected by the trapping of carriers at the defects located at the grain boundaries and at the oxide/semiconductor interface. In particular, the resulting high level of low frequency ( $1/f$ ) noise can be one limiting factor for using such devices. For polysilicon TFTs it is useful to model  $1/f$  noise by trapping/detrapping (T/D) of carriers into slow oxide traps located close to the interface [1,2] as depicted in the figure 1, and the corresponding distribution of states into the band gap can be deduced [1]. In addition, T/D processes of carriers at grain boundaries (GBs) have also been

previously suggested and the average defect density at GBs can be deduced [2].  $1/f$  noise level is then strongly dependent on both interface and active layer qualities, and thus on fabrication process parameters [1,3], and its measurement can be used as diagnostic tool to qualify TFT technology. In this paper the effect of the temperature on the  $1/f$  noise level in polysilicon TFTs is studied in relation to the carrier transport and to the interface state density.

## 2. Devices technology and experimental details

TFTs are elaborated with a single poly-Si layer (fig. 2): the upper part is heavily *in-situ* n-type doped (source and drain regions), and the bottom part is none intentionally doped and is dedicated to the active layer. Polysilicon layer is deposited by a LPCVD (Low Pressure-Chemical Vapor Deposition) technique and is crystallized by a solid phase crystallization thermal annealing at 600°C. A 60 nm thick SiO<sub>2</sub> gate insulator is deposited by CVD process at atmospheric pressure (APCVD) at 390°C and annealed at 600°C in nitrogen ambient for densification. Electrodes are made of thermally evaporated aluminium. Finally the devices were annealed into forming gas (N<sub>2</sub>/H<sub>2</sub>=95%) at 390°C. More details for fabrication are given in ref [4].

Noise measurements are carried out in a shielded environment by using a low noise transimpedance amplifier (EG&G 5182, 15fA/ $\sqrt{\text{Hz}}$ ) connected to the source electrode, followed by a low noise voltage amplifier (EG&G 5113, 4nV/ $\sqrt{\text{Hz}}$ ) and a HP 3562A dynamic signal analyzer [6]. Static drain current measurements are carried out by using a HP 4156 B semiconductor parameter analyzer. All tested devices are biased in the linear mode ( $V_{\text{DS}}=300\text{mV}$ ) from weak to strong inversion. A temperature controlled wafer system, operating in vacuum ( $10^{-6}$ - $10^{-5}$  Pa), allows temperature measurements from 260K to 310K.

## 3. Results and discussion

Transfer characteristics of the studied devices are plotted for various temperatures in figure 3. The Arrhenius plots of the drain current have been previously reported [6] and showed that the drain current follows the Meyer-Neldel (MN) rule [7] according the relationship:

$$\begin{cases} I_{DS} = I_{DS0} \exp\left(\frac{E_A}{E_{MN}}\right) \exp\left(-\frac{E_A}{kT}\right) \\ I_{DS0} = \beta_0(V_{DS})(V_{GS} - V_0) \end{cases} \quad (1)$$

with  $E_A$  the activation energy associated with multiple-trapping transport of carriers [8] and decreasing with the gate voltage,  $E_{MN}$  the MN characteristic energy ( $\approx 0.1\text{eV}$  in our case),  $V_0$  the gate voltage corresponding to the minimum of the drain current, and  $\beta_0(V_{DS})$  the transconductance. Previous works reported that MN effect is related to process fabrication parameters and to interface trap state distribution [1,6]. In addition, study of numerical simulation of static drain current showed that MN effect is strongly controlled by the trap distribution associated with defects located at the gate insulator/active layer interface rather than defects located at grain boundaries [9]. Such thermal activation is assumed to be common to 1/f noise and it is explained by trapping processes of carriers at the interface along the channel.

Temperature dependence of the 1/f noise in TFTs was then studied and the plots of the normalized drain current spectral density ( $S_{IDS}/I_{DS}^2$ ) versus the drain current are reported for different temperatures in the figure 4 (a). The Arrhenius plots of the measured drain current noise spectral density ( $S_{IDS}$ ) are displayed in the figure 4 (b). The decreasing linear plots of  $S_{IDS}$  versus  $1/kT$  and the common intersect at  $1/kT \neq 0$  show that  $S_{IDS}$  is thermally activated and follows the MN rule especially from weak to moderate inversion ( $-3\text{V} \leq V_{GS} \leq 1\text{V}$ ). The corresponding values of the thermal activation energy of the measured  $S_{IDS}$  versus  $V_{GS}$  were deduced and plotted in the figure 4 (c). Maximum value of  $E_A$ , corresponding to the minimum value of  $I_{DS}$  (close to desertion of carriers in the channel region  $V_{GS} \sim -5\text{V}$ ), was not measured because noise measurements for devices biased at low level of the drain current (*ie* below  $\sim 10^{-9}\text{A}$ ) was difficult. Such thermal dependence of the measured drain current noise spectral density is first observed. Furthermore,

these results suggest that 1/f noise in polysilicon TFTs is related to T/D processes of carriers from defects located close the interface explained as follow.

Our noise analysis is supported by the theory of the sum of generation/recombination spectra to explain T/D processes following the tunnelling theory of carriers into the gate oxide traps located close to the interface (Mc Worther model) [10] (see fig 1). In such case 1/f noise can be described by the widely used Hooge empirical relation:

$$\frac{S_{I_{DS}}}{I_{DS}^2} = \frac{\alpha}{fN} \quad (2)$$

where  $\alpha$ ,  $N$  and  $f$  stand for the noise parameter, the free carrier number and the frequency respectively. Previous theoretical study [11] on the relevance of the Mc Worther model showed that theoretical values of  $\alpha$  do not correspond to those usually measured for crystalline MOS transistors. However, in the case of polysilicon TFTs, a previous experimental study [12] showed that results are in accordance with theoretical predictions of  $\alpha$  reported in ref [11], and thus this model was assumed to be convenient in our study. In such case, it was reported that from weak to moderate inversion (at low gate voltages):

$$\alpha \approx 4 \frac{N\lambda}{my} \quad (3)$$

with  $m$  the number of trapped carriers into the oxide close to the interface,  $y$  the effective oxide thickness, and  $\lambda$  the tunnel attenuation distance ( $\approx 0.1\text{nm}$ ). The number  $m$  is both controlled by the number of trap at the interface  $n_t$ , the depth of the oxide  $y$ , and the inversion free carrier number  $N$ . Then it can be expressed as  $m(E, y) = \exp(-y/\lambda)f_t(1-f_t)n_tN$ , with  $f_t=1/(1+\exp((E-E_F)/kT))$  the Fermi factor,  $E$  and  $E_F$  trap and Fermi energies respectively [13]. Assuming that close to the interface,  $N \approx N_C W L t_{si} \exp((E_F - E_C)/kT)$  with  $N_C$  ( $\sim 10^{19}\text{cm}^{-3}$ ) the effective density of states in the conduction band,  $W$  ( $=L=40\mu\text{m}$ ) the width(length) of the channel and  $t_{si}$  ( $=150\text{nm}$ ) the thickness of the active layer, therefore the average number of trapped carriers into the oxide is:

$$m(E) \approx f_t(1-f_t)n_t(E)N \left( \int_0^{t_{ox}} \exp(-y/\lambda)dy \right) / t_{ox} \approx n_t(E)Nf_t(1-f_t)\lambda / t_{ox} \quad (4)$$

with  $t_{ox}(=60\text{nm})$  the thickness of the gate oxide. Considering that trapping occurs when  $E \leq E_F$  then  $E_C - E_F \approx E_A - (E_F - E)$  (see fig 1), that  $Nf_t(1-f_t) = (N_C W L t_{si}) \exp(-E_A/kT) (1 + \exp((E - E_F)/kT))^{-2}$ , and that  $1 + \exp((E - E_F)/kT) \approx 1$ , therefore according (1), (2), (3) and (4):

$$S_{IDS} = \frac{4\lambda}{m t_{ox} f} I_{DS}^2 \approx \frac{4}{n_t N f_t (1-f_t) f} I_{DS}^2 \approx S'_{IDS0} \exp\left(\frac{E_A}{E'_{MN}}\right) \exp\left(-\frac{E_A}{kT}\right) \quad (5)$$

with  $S'_{IDS0} = 4I_{DS0}^2 / (n_t N_C f W L t_{si})$ ,  $E'_{MN} = E_{MN}/2$ , and  $E_A$  and  $n_t$  both depending of the gate voltage related to  $E_F$  and  $E$  levels into the polysilicon band gap respectively.

The slope of the linear plot of the  $S_{IDS} = f(E_A)$  curve (see inset of fig. 4 (c)), with  $S_{IDS}$  deduced from Arrhenius plots at  $1/kT=0$ , gives a MN characteristic energy  $\approx 0.1\text{eV}(=E_{MN})$ . This implies that:

$$S_{IDS} \approx S_{IDS0} \exp\left(\frac{E_A}{E_{MN}}\right) \exp\left(-\frac{E_A}{kT}\right) \quad (6)$$

with according (5)  $S'_{IDS0} \approx S_{IDS0} \exp(-E_A/E_{MN})$ , and thus it gives:

$$n_t \approx \frac{4}{f N_C W L t_{si}} \frac{I_{DS}^2}{S_{IDS}} \exp\left(\frac{E_A}{kT}\right) = \frac{4}{f N_C W L t_{si}} \frac{I_{DS0}^2}{S_{IDS0}} \exp\left(\frac{E_A}{E_{MN}}\right) \quad (7)$$

The thermal activation following the MN rule of  $S_{IDS}$  depicted in the figure 4 (b) is then explained by the  $1/f$  noise model used in this study. In addition, (7) shows that  $n_t$  follows the MN rule and allows the calculation of  $n_t$  from  $E_A$  and  $S_{IDS}/I_{DS}^2$  measured from weak to moderate inversion. The corresponding interface trap states distribution  $N_t$  ( $\text{cm}^{-2} \text{eV}^{-1}$ ) can be deduced considering traps within an energy band  $kT$  around the Fermi level by standing:

$$N_T(E) \approx \frac{n_t(E)}{W L k T} \approx \frac{4}{f N_C (W L)^2 t_{si} k T} \frac{I_{DS}^2}{S_{IDS}} \exp\left(\frac{E_A}{kT}\right) \approx N_{t0} \exp\left(\frac{E_C - E}{E_{MN}}\right) \quad (8)$$

with  $N_{t0} = 4I_{DS0}^2 / (f N_C (W L)^2 t_{si} k T S_{IDS0}) \sim 10^9 \text{ cm}^{-2} \text{ eV}^{-1}$  and  $E_A = E_C - E$ . Plots of  $N_T$  versus  $E_C - E$  are displayed in the figure 5 for various temperature measurements. As predicted by (8) no significant dependence on the temperature is observed and  $N_T$  increases as the energy trap state level is

deeper. These results are in contrast with the MN effect related to the distribution of defects exponentially decreasing as it becomes deeper in the gap [8]. In fact, two types of distributions have to be considered: i) Gaussian distribution associated with deep level related to dangling bond (DB) type defects and, ii) high level decreasing exponential band tailing rather related to strained bond type defects. In our study noise measurements, made for devices biased from weak to strong inversion, are controlled by deep trap states. Therefore, the interface state distribution plotted in the figure 5 is associated with a deep level corresponding to DBs with significant values close to the maximum for the resulting interface trap state distribution (see inset of fig. 5). However, the expected maximum of  $N_T$  ( $N_{Tmax}$ ) close the midgap, corresponding to the maximum value of  $E_A$  usually measured at the minimum value of  $I_{DS}$ , is not observed and should be extrapolated because of the limitations of the  $1/f$  noise measurements previously mentioned.  $N_{Tmax}$  estimated according (8) with  $E_C-E \approx 0.56$  eV is higher than  $10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ , thus with a channel thickness  $\sim 10^{-5}$  cm it gives  $N_{Tmax} \geq 10^{17} \text{ cm}^{-3} \text{ eV}^{-1}$ . This value is convenient with previous published results [14]. Furthermore, this experimental study validates result of numerical simulation of  $I_{DS}$  reporting that MN effect is strongly controlled by trap state distribution associated with DBs located at the interface [9].

#### **4. Conclusion**

Study of thermal dependence of low-frequency noise in polysilicon TFTs is first presented. Experimental results are explained by the theory of trapping/detrapping process of carriers following the tunnel theory into slow oxide traps located close to the interface. It is shown that the Meyer-Neldel effect is directly associated with the trapping/detrapping process of carriers from defects such as dangling bonds located at the interface and responsible of the resulting low frequency noise level in the polysilicon TFTs biased from weak to moderate inversion. Moreover, a further investigation of  $1/f$  noise level in TFTs biased from moderate to strong inversion is needed to verify the relation of the MN effect with tail state distribution.

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