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Electrical properties of polysilicon nanowires for devices applications

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Polysilicon nanowires are synthesized using the well known and low cost technique commonly used in microelectronic industry: the sidewall spacer formation technique. Polysilicon layer is deposited by Low Pressure Chemical Vapour Deposition technique on SiO_2 wall patterned by conventional UV lithography technique. Polysilicon film is then plasma etched. Accurate control of the etching rate leads to the formation of nanometric size sidewall spacers with a curvature radius as low as 100nm used as polysilicon nanowires. These polysilicon nanowires are first integrated into the fabrication of electrical devices as resistors and electrical properties are studied in function of *in situ* phosphorus doping levels. I(T) measurements show that polysilicon nanowires dark conductivity is thermally activated according to the Seto's theory. In addition, field effect transistors made with such polysilicon nanowires used as channel region highlight promising field effect behaviour.

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1 Introduction

Owing to their physical and electrical properties, SiNWs (silicon nanowires) represent a promising material with strong potential for a large variety of applications. They are currently attracting much attention as components for future nanoelectronic devices such as nanowire field effect transistors [1], photonic and optoelectronic devices [2], and as chemical or biological sensors [3, 4]. SiNWs present large advantages with respect to bulk silicon: high surface to volume ratio, possibility of surface functionalization, synthesis compatible with large area technology, leading to the development of innovative electronic devices. SiNWs development could significantly impact areas of electronics, genomics, biomedical diagnosis, drug discovery.... They can be prepared by the top-down approach, using various advanced methods such as e-beam [5], AFM [6] or deep UV [7] lithography. The main disadvantage of these advanced lithographic tools with nanometer size resolution rests on their high cost. The bottom-up approach usually consists in a metal catalytic growth [8]. Thus, VLS (Vapour-Liquid-Solid) growth technique uses metallic nanoparticles as aluminium, nickel, gold… This approach suffers from both metal contamination and the difficulty in precisely positioning the device location.

In this work, SiNWs are synthesized using a low cost technique commonly used in microelectronic industry: the sidewall spacer formation technique. Previous works reported the feasibility of undoped silicon NWs and their potential applications for fabrication of field effect transistors [9] as biological sensors [10]. In this case, SiNWs present a polycrystalline structure, and their electrical behaviour is expected to be different from crystalline SiNWs due to higher defect density and carriers confinement at nanometric scale. In addition, thanks to their higher surface to volume ratio compared to thin films, these polysilicon NWs are promising for charged (bio)chemical species detection.

Polysilicon NWs based devices performances are strongly correlated with NWs electrical properties. However, polysilicon NWs electrical behaviour has not been yet studied. Thus, prior to develop polysilicon NWs based devices for high efficient (bio)chemical sensing applications, a well understanding of electronic polysilicon NWs properties is required. Here, we present a study of the polysilicon NWs electrical behaviour as a function of the N-type doping level, and their potential applications in devices (resistors, TFTs) fabrication are demonstrated.

2 Experimental details

The key nanowire fabrication steps are illustrated in figure 1 (a). At first, a dielectric film A is deposited and patterned into islands by conventional UV lithography. Then, a polysilicon layer is deposited by LPCVD

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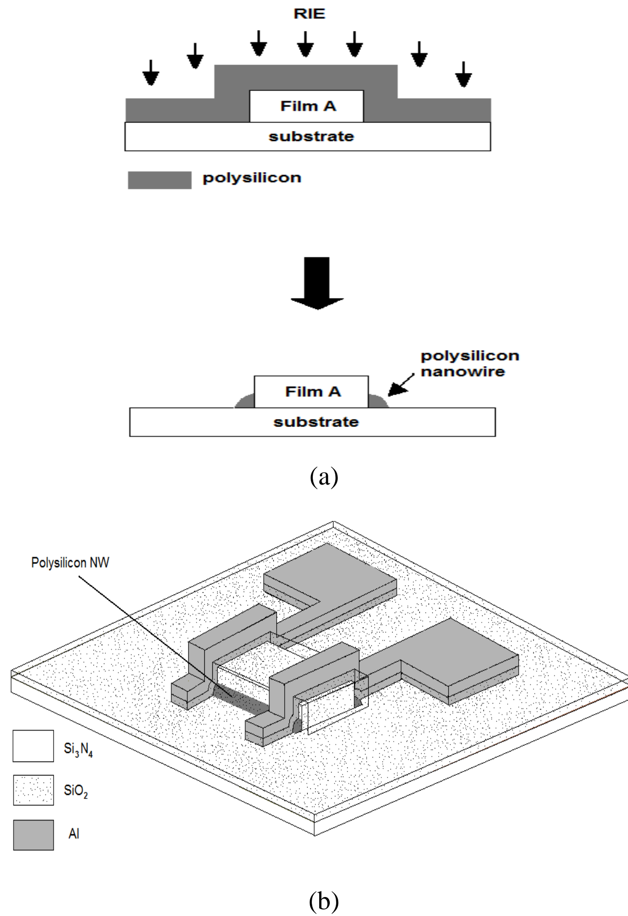

(a)

(b)

Figure 1 (a) Fabrication of polysilicon NWs by the sidewall spacer formation technique, (b) polysilicon NWs based resistors.

(Low Pressure Chemical Vapour Deposition) technique. Accurate control of the polysilicon layer Reactive Ion Etching (RIE) rate leads to the formation of nanometric size sidewall spacers that can be used as nanowires. The feasibility of this technological step was previously demonstrated [11].

Phosphorus doped polysilicon films used for nanowires are deposited by thermal decomposition of a mixture of pure silane (SiH_4) and phosphine (PH_3) diluted in helium. The *in-situ* doping level is controlled by adjusting the PH_3/SiH_4 mole ratio varying from 0 (undoped film) to 1.2×10^{-3} (heavily doped film). The corresponding incorporated phosphorus atoms concentration C_p, previously determined from SIMS (Secondary Ions Mass Spectroscopy) analysis, varies from 2×10^{16} cm^{-3} to 2×10^{20} cm^{-3} [12]. Silicon films are deposited in an amorphous state at 550°C and 90 Pa, and then crystallized by a thermal annealing in vacuum at 600°C during 12 hours.

The *in-situ* doped polysilicon NWs are integrated into resistors (fig. 1 (b)) for electrical characterization. The nanowires are capped by a SiO_2 layer deposited by Atmospheric Pressure Chemical Vapour Deposition (APCVD) technique at 390°C and contact openings are wet etched. Aluminium is then thermally evaporated and electrodes defined by wet etching.

Static electrical characteristics I(V) are collected at room temperature using a HP 4155 B semiconductor parameter analyzer. For current-temperature measurements, in the range 200K to 530K, samples are placed in a cryostat in vacuum (10^{-3} - 10^{-4} Pa) and dark current is measured using a Keithley 617 electrometer.

3 Results and discussion

Electrical properties of 10 µm length and 100 nm curvature radius polysilicon NWs are investigated in function of the *in-situ* doping level. Such polysilicon NWs were previously investigated by scanning electronic microscopy [11].

I(V) characteristics of the polysilicon NWs based resistors are plotted in the figure 2 for 2×10^{16} $cm^{-3} \le C_P \le 2 \times 10^{20}$ cm^{-3}. The *in-situ* doping effect is studied through the dependence of the polysilicon NW resistivity with doping concentration as shown in the figure 3. The resistivity

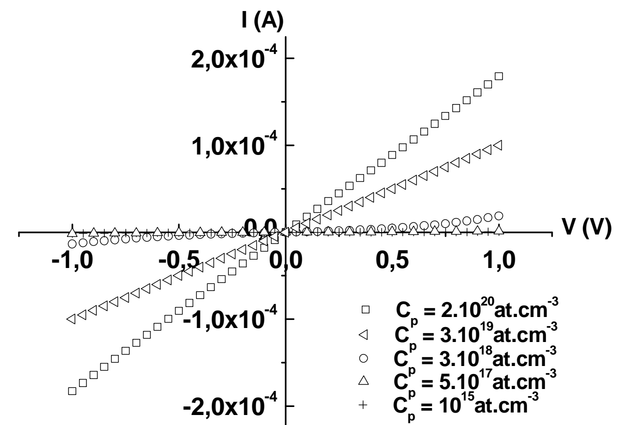

Figure 2 I(V) characteristics of the polysilicon NWs based resistors at different phosphorus atoms concentration levels (10 µm length NWs).

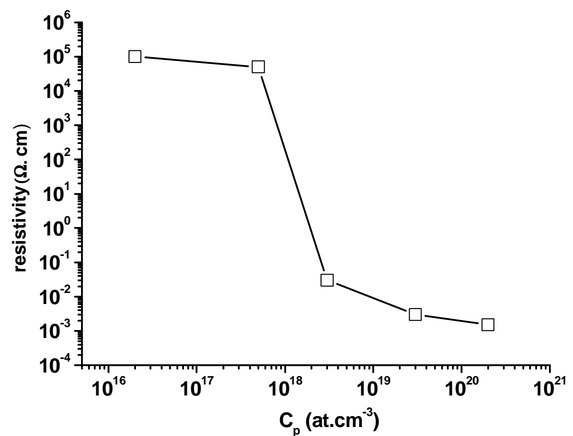

Figure 3 Variations of the resistivity of the polysilicon NWs versus the phosphorus atoms concentration.

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reaches 10^5 Ω.cm for the lightly doped polysilicon NWs. Increasing the doping level from about 1×10^{18} cm^{-3} results in an abrupt resistivity drop of about 6 orders of magnitude for only a factor of 10 further increase in doping concentration. Beyond that range resistivity decreases following the same doping effect as in crystalline silicon. The shape of the curve, quite similar to previously observed results for *in-situ* doped polysilicon layers [12-13], indicates that polysilicon NWs doping effect is in accordance with the Seto's theory [14]. In this model, the conduction is thermally activated.

Figure 4 (a) presents the temperature dependence of the electrical conductivity, σ, for different C_p values. The activation energy, E_a, is deduced from the slope of the decreasing linear curve at high temperatures. The variations of E_a with C_p plotted in figure 4 (b) highlight an evolution in accordance with the Seto's theory. Indeed, for low doping levels, it means below a critical concentration, N*, E_a slightly decreases with C_p. In this case, generation of

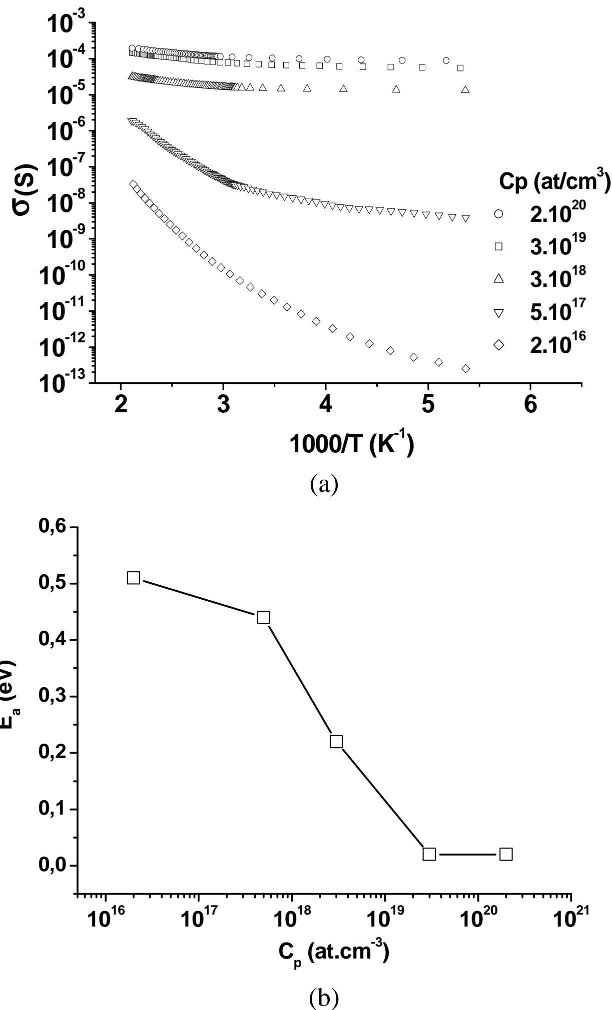

Figure 4 (a) Arrhenius diagrams of polysilicon NWs conductivity for various phosphorus atoms concentrations. (b) Variations of the corresponding activation energy of the conductivity versus the phosphorus atoms concentration.

trapped carriers dominates. So, the corresponding activation energy is related to the energy barrier needed for emission of carriers into the conduction band from deep levels located into the bad gap associated with residual and/or structural defects. For high doping levels (>N*), free carriers diffusion over the intergranular barrier E_b (induced by trapped carriers at grain boundaries) dominates. In this case, $E_a = E_b$ and it decreases with the doping level. In this model, N* is related to the quality of the polysilicon layer both through the defects density at the grain boundaries and the lateral grain size. In our case N* ~ 10^{18} cm^{-3}, corresponding to the value obtained for previous studies [12-14]. These results show that this electrical conduction model can be applied for polysilicon NWs at high temperatures.

For lower temperatures, the slight dependence of σ with 1000/T is commonly described by the conduction in localized states [15]. These states are associated with a high defect density uniformly distributed along the NWs. Two types of defects can be involved either located i) at the surface of the wire and/or ii) in the core of the polysilicon layer. Indeed, in this last case, because the amorphous silicon crystallization process begins at the Si_3N_4/amorphous silicon interface, the defects density (including grain boundaries) is higher in the inferior part of the polysilicon layer (few nanometers thick) constituting the nanowire. For the lowest temperatures range σ does not depend on temperature, indicating tunnel conduction through these defects.

Our results highlight the good control of the doping level on the 100 mn long curvature radius polysilicon NWs over a wide range, with a doping effect similar to polysilicon layer [12-14]. This study shows that despite the high defects density within these polysilicon NWs, there is no significant doping species segregation at grain boundaries affecting doping efficiency. In addition, thanks to their high surface to volume ratio, such doped NWs are promising candidates for optimized devices devoted to charged (biological and/or chemical) species detection.

Thin Film Transistors (TFTs) are fabricated (see figure 5 (a)) using undoped polysilicon NWs following the synthesis method described in section II. In our case, the substrate is heavily N-type doped crystalline silicon wafer acting as gate electrode. The film A is a 100 nm thick Si_3N_4 layer deposited by LPCVD technique at 600°C. Source and drain regions are made of heavily *in-situ* N-type doped polysilicon layer deposited by LPCVD technique. This layer is patterned by reactive ion etching with SF_6 plasma before thermal evaporation of aluminium used for source and drain electrodes.

Field effect behaviour displayed on the figure 5 (b) shows a switching ratio ~ 10^4 and good ohmic contacts (see inset of fig. 5 (b)). Threshold voltage, V_T, and optimum field effect mobility, μ, are determined according to the classical conduction electrical model used for the MOSFET (Metal Oxide Semiconductor Field Effect Tran

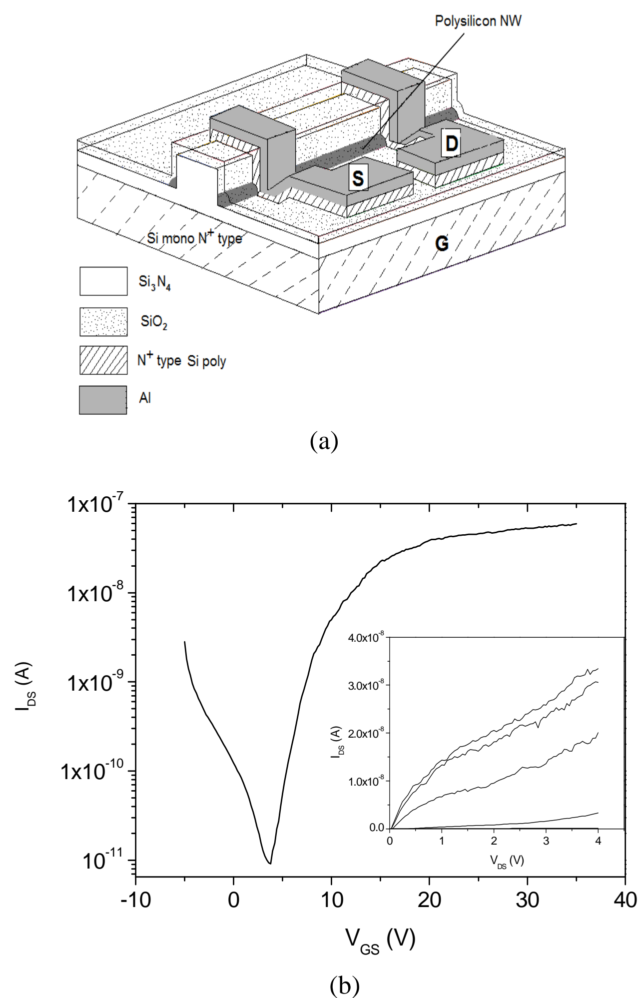

Figure 5 (a) Schematic illustration of the polysilicon NWs based TFT. (b) Transfer characteristics (W/L = 0.1µm/10µm, V_{DS} = 4 V). Inset: output characteristics (V_{DS} = 1 V to 4V, step 1 V).

sistor) [16]. µ is deduced from the maximum slope of the $I_{DS}(V_{GS})$ curve (transconductance) plotted in the saturation mode and V_T is determined by the intercept of the $I_{DS}^{1/2}(V_{GS})$ curve with the gate axis voltage. The low field effect mobility (~ 3 cm^2/Vs) and the high threshold voltage ($V_T \approx 8$ V) values are related to the poor gate insulator (Si_3N_4)/active layer (polysilicon NWs) interface quality. The electrical properties of our polysilicon NWs based TFTs, as well as technology, have to be improved for high efficient chemical and/or biological sensing applications.

4 Conclusion

The sidewall spacer formation technique allows the feasibility of arrays of parallel horizontal polysilicon NWs using conventional UV lithography. This low cost and compatible with silicon thin film technology patterning method represents an attractive process for polysilicon nanowires fabrication. *In-situ* doping control of these 100 nm curvature radius polysilicon NWs is demonstrated, and thus it makes them good candidates for the fabrication of electrically controlled thin film devices, particularly for integrated chemical and/or biological sensors.

The next step of this study will consist in the fabrication of lower curvature radius polysilicon NWs (< 50 nm) and to study their specific electrical properties at nanometric scale and their ability for fabrication of optimized high sensitive and low detection level chemical and/or biological sensors.

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