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Growth-in-place deployment of in-plane silicon nanowires

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Up-scaling silicon nanowire (SiNW)-based functionalities requires a reliable strategy to *precisely* position and integrate individual nanowires. We here propose an *all-in-situ* approach to fabricate self-positioned/aligned SiNW, via an in-plane solid-liquid-solid growth mode. Prototype field effect transistors, fabricated out of in-plane SiNWs using a simple bottom-gate configuration, demonstrate a hole mobility of 228 cm^2/V s and on/off ratio $>10^3$. Further insight into the intrinsic doping and structural properties of these structures was obtained by laser-assisted 3 dimensional atom probe tomography and high resolution transmission electron microscopy characterizations. The results could provide a solid basis to deploy the SiNW functionalities in a cost-effective way. © *2011 American Institute of Physics.* [doi:10.1063/1.3659895]

Silicon nanowires (SiNWs) are basic building blocks to construct a new generation of transistors and sensor applications.[1,2] Though SiNWs can be readily grown via several cost-effective bottom-up approaches, most notably via the well established vapor-liquid-solid (VLS) mechanism,[2,3] the challenge for large-area electronic applications remains to arrange SiNWs into ordered 2 dimensional (2D) arrays as active components or interconnections. The ability to grow SiNWs at desired locations could lead to industrial scaling of the promising SiNWs functionalities. For instance, it could advantageously replace amorphous and microcrystalline Si thin films used in flat panel displays. SiNWs grown by the VLS process are usually perpendicular to the substrate surface and need to be positioned selectively in a "pick-and-place" manner[4] or via solution-based techniques.[3,5] Though the VLS growth of SiNWs can be constrained by nanoscale channels/pores,[3,6] the template fabrication steps introduce extra complexity and are mostly incompatible with planar Si technology.

We have proposed recently an in-plane solid-liquid-solid (IPSLS) SiNW growth mode[7,8] to address this challenge by fabricating in-plane SiNWs *all-in-situ* in a plasma chemical vapor deposition (PECVD) system. In contrast to the VLS process[9] that takes place in a gas precursor environment, a thin layer of hydrogenated amorphous Si (a-Si:H) is absorbed by indium catalyst drops, moving on a substrate surface, to produce crystalline in-plane SiNWs.[7,8,10] The driving force, as depicted in Fig. 1(a), arises from the difference in Gibbs energy between hydrogenated amorphous Si (a-Si:H) and crystalline Si.[11] A unique feature of the in-plane growth lies in that the movement of catalyst drops can be guided by simple surface features, like a single edge step. This allows to determine the position and the growth

path of the SiNWs[7,8,10,12] and offers an exciting opportunity to position the in-plane SiNWs during their growth without interrupting the vacuum. Here, we explore this feature to deploy self-positioned SiNWs in a process compatible with large area substrates and demonstrate prototype SiNWs-FETs devices. Further insights of the structural properties, as well as the catalyst doping effect in the SiNWs, were obtained by using transmission electron microscopy (TEM) and laser-assisted 3D atom probe tomography (APT) characterizations.[13]

The SiNWs were fabricated on top of an n$^+$-Si wafer coated with a thick SiO$_2$ layer. First, as shown in Figs. 1(c) and 1(d), indium-tin-oxide (ITO) stripes were deposited and patterned on the substrate followed by a SiN$_x$ layer coverage ($\sim$180 nm in thickness). Guiding channels were formed by etching into the SiN$_x$ layer. Then, the substrates were loaded into a PECVD system and treated with a H$_2$ plasma at 300 °C to precipitate metal indium droplets at the surface of the exposed ITO pads [Fig. 1(e)]. The substrate was then cooled to 100 °C and covered with a thin layer of a-Si:H [Fig. 1(f)]. The samples were annealed *in-situ*, under vacuum, at 300–450 °C, to activate the indium droplets which moved around and produced well-defined in-plane SiNWs. After the growth of SiNWs, the remnant a-Si:H matrix was selectively removed by an *in-situ* H$_2$ plasma etching at 100 °C. More details on the fabrication process are available in the supplementary material.[17]

During the growth of in-plane SiNWs, the front a-Si:H/catalyst interface, from which Si atoms are constantly absorbed, always lead the in-plane motion of catalyst drop. After the initial random growth on the ITO pad, seen in the inset of Fig. 2(b), the catalyst drop eventually runs into the step sidewall provided by the SiN$_x$ guiding edge, which is also coated with a layer of a-Si:H. In doing so, it forms a new absorption front as illustrated by the green line in Fig. 1(b). Depending on the growth balance condition,[7] this extra

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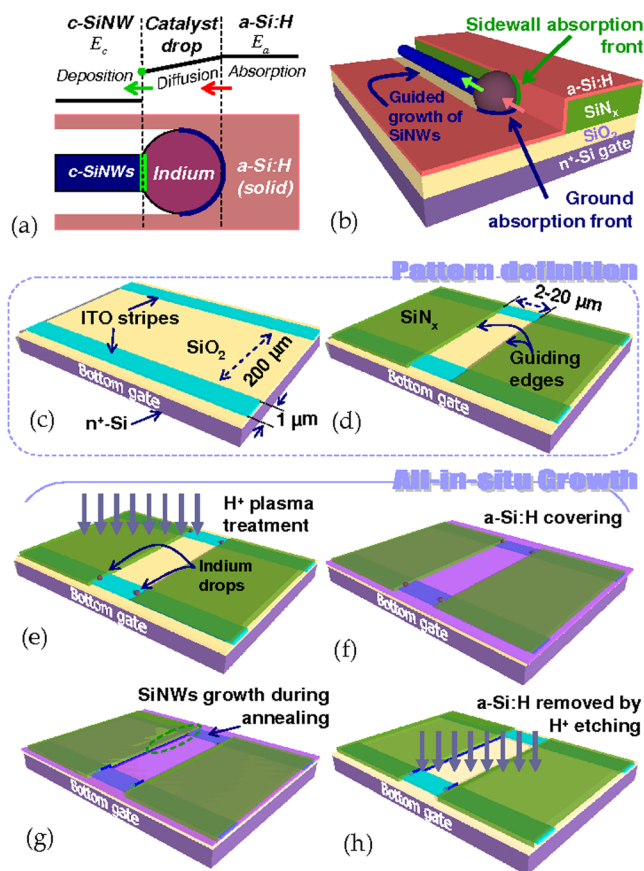
FIG. 1. (Color online) (a) Schematic illustration of the in-plane growth of SiNWs via IPSLS mode; (b) the formation of a new absorption front (green line) on the step sidewall and the guided growth of in-plane SiNWs. (c)-(h) the ITO stripes and guiding edge patterning processes, and the *all-in-situ* plasma treatment/deposition steps in a PECVD system.

sidewall absorption front can exert a lateral attraction force which *guides* the motion of a catalyst drop to produce aligned SiNW along the sidewall edge. In Figs. 2(a) and 2(b), we show the scanning electron microscopy (SEM) pictures of a guiding edge matrix, with a spacing of 200 μm and channel width of 2–20 μm. At each guiding edge, on both sides of the channel, we found one and only one precisely aligned SiNW. It is important to note that precise control over the number of in-plane SiNWs is also a critical factor to building robust device applications. Meanwhile,

based on this in-plane guided growth strategy, the diameter of the SiNWs can also be effectively controlled by the size of the catalyst drops, which in our case is achieved by tuning the initial H_2 plasma treatment condition. To give an example, SEM images of the thinner guided SiNWs with diameters down to 40 nm, 28 nm, and 14 nm are provided in the supplementary material Figs. S1(a)–S1(c), respectively.[17]

Based on the self-aligned SiNWs, shown in Fig. 2, we continue to explore their structural properties by using high resolution TEM (HR-TEM), as well as the electronic transport properties and device performance in a bottom-gate SiNWs FETs configuration. The SiNWs in these arrays have an average diameter of ∼170 nm and span a channel length of 200 μm. A typical HR-TEM image of a SiNW in Fig. 2(c) shows that the growth direction of this specific SiNW is ⟨211⟩. The high crystallinity of the in-plane SiNWs is confirmed by an enlarged view of the lattice in the right inset of Fig. 2(c). Twin planes, parallel or oblique to the growth direction, can be found in the in-plane SiNWs. A simple bottom-gate SiNW FET structure was realized by connecting selected SiNW channels with Al electrode contacts and using the n^+ c-Si wafer as bottom-gate. The transfer characteristics of a typical single SiNW (of ∼170 nm in diameter and 200 μm in length) are presented in Fig. 3(a). The channel current I_{ds} can be modulated by V_g and pinched off by applying a positive gate voltage, indicating a p-type SiNW channel, with an on-off current ratio $>10^3$ and a subthreshold slope S = 690 mV/dec. The carrier mobility in the SiNW channel is estimated according to a simple bottom-gate model as depicted by the inset of Fig. 3(a), $\mu = S \cdot V_{sd} \cdot l_w^2 / C$, where $S \equiv dI_{ds}/dV_g$ and $C = \varepsilon_0 \varepsilon_{SiO_2} l_w d_w / t_{SiO_2}$ are the transconductance and the capacitance between the SiNW channel and the bottom-gate, respectively, with l_w, d_w, and t_{SiO_2} being the length and width of the SiNW channel and the thickness of the bottom SiO_2 dielectric layer, ε_{SiO_2} and ε_0 the relative dielectric constant and the vacuum permittivity. The field effect hole mobility in this specific guided SiNW channel is thus deduced to be 228 cm^2/Vs.

Though no dopant sources were intentionally introduced, indium incorporation in Si is known to introduce acceptor states in the crystalline Si, with dopant levels at 0.16 eV above the valence band.[14] Further insight on the indium concentration was obtained by probing a single SiNW
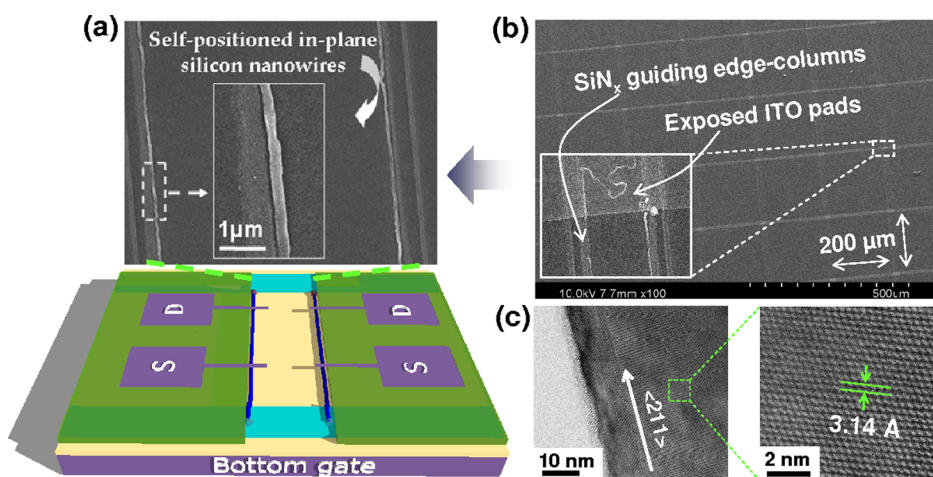

FIG. 2. (Color online) (a) SEM images and illustration of the self-positioned growth of aligned SiNWs along the guiding edges, as well as the configuration of the bottom-gated SiNWs FET; (b) the matrix of ITO rows and SiN$_x$ guiding columns. (c) HR-TEM image of an in-plane SiNW grown in ⟨211⟩ direction, with an enlarged view of the Si lattice on the right inset.
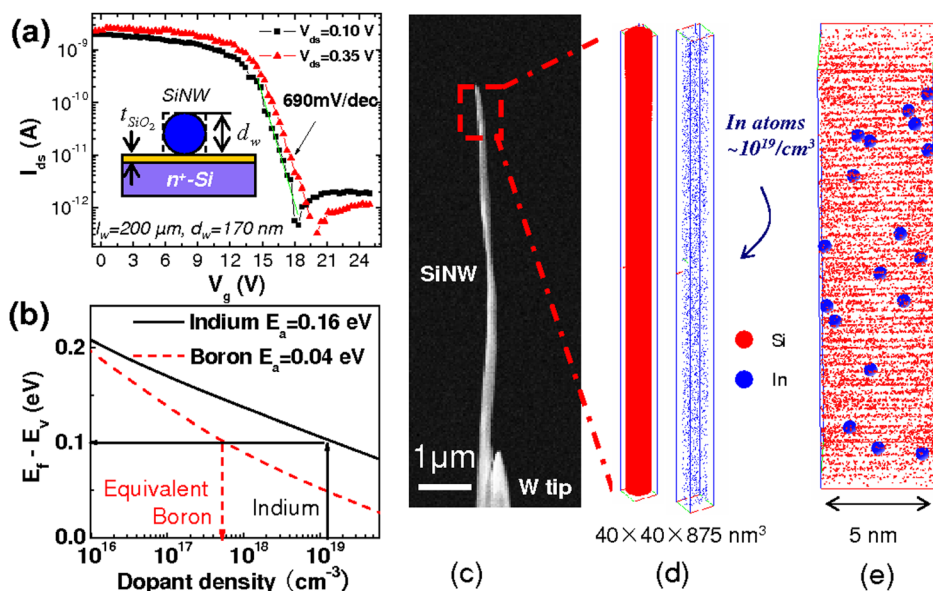
FIG. 3. (Color online) (a) The transfer properties of the SiNW FET, with an illustration of the bottom-gate structure in the inset; (b) the calculated Fermi level position as a function of the dopants concentration of indium (solid) or boron (dashed) dopants; (c) SEM image of a single SiNW mounted on a W tip. (d) 3D reconstruction of the distribution profile of silicon atoms (red) and indium atoms (blue) in a selected volume of $40 \times 40 \times 875$ nm^3 and (e) an enlarged view of the discrete distribution of indium and silicon atoms in a 5 nm wide slab region.

with APT. A SiNW segment was chosen and mounted on a tungsten tip by focus ion beam cutting and soldering manipulations, as shown in Fig. 3(c). A 3D reconstruction of the distribution profile of indium atoms in the SiNW is shown in Fig. 3(d), with analyzed volume of $40 \times 40 \times 875$ nm.^{3} A magnified view of an extracted slab in Fig. 3(e) reveals the discrete distribution of indium atoms among the clearly resolved Si-$\langle 111 \rangle$ planes. By taking an inter-plane distance of 0.31 ± 0.01 nm as a calculation parameter for the reconstruction, the indium concentration in this SiNW segment is determined to be $\sim 10^{19}$ cm^{-3}.

Compared to boron doping in c-Si, which features a shallow acceptor level with an activation energy of $E_a = 0.045$ eV above the valence band, indium dopants are known to introduce a deeper level at $E_a = 0.160$ eV. According to the neutrality condition in c-Si,[14] the Fermi level position can be determined as a function of the boron or indium dopant concentrations, as depicted in Fig. 3(b). Since indium atoms have an ionization energy that is four times larger than boron, assuming that the concentration of active indium dopants is the same as that of indium atoms $\sim 10^{19}$/cm^3, the hole carriers given off by the indium atoms are estimated to be $\sim 3.7 \times 10^{17}$/cm^3. As only ionized dopants provide the kind of scattering centers that limit the carrier mobility,[15] an ionized dopants concentration of $\sim 3.7 \times 10^{17}$/cm^3 leads to a hole mobility in boron doped c-Si in the range of ~ 220 cm^2/Vs.[15] This is consistent with our best mobility of 228 cm^2/Vs that was measured in the in-plane SiNWs channels, indicating that the hole mobility is mainly limited by the ionized indium dopants. Interestingly, the hole mobility in the self-positioned SiNWs channels is comparable or even higher than that achieved in the best p-channel polycrystalline Si transistors (~ 200 cm^2/Vs),[16] and much higher than that in the amorphous silicon and metal oxide materials adopted in active matrix flat panel displays.

In summary, we have demonstrated an *all-in-situ* approach to deploy self-positioned SiNW channels in an up-scalable and cost-effective process. Prototype field effect transistors fabricated in a simple bottom-gate configuration have been realized and demonstrate an on/off ratio $>10^3$ and hole mobility of 228 cm^2/Vs. These results lay an important basis for direct integration of in-plane SiNW FETs for high performance planar display and flexible electronics.

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[17]See supplementary material at http://dx.doi.org/10.1063/1.3659895 for details on the fabrication and characterization process and SEM images of the thinner guided SiNWs.