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# Fabrication and electrical characterization of silicon nanowires based resistors.

L Ni, F Demami, R Rogel, A C Salaün, L Pichon

Institut d'Electronique et des Télécommunications de Rennes, Groupe  
Microélectronique, UMR CNRS 6164, Université de Rennes 1, campus de Beaulieu,  
263 avenue du général Leclerc, 35042 Rennes cedex, France

fdemami@univ-rennes1.fr

**Abstract.** Silicon nanowires (SiNWs) are synthesized via the Vapor-Liquid-Solid (VLS) mechanism using gold (Au) as metal catalyst and silane ( $\text{SiH}_4$ ) as precursor gas. Au nanoparticles are employed as liquid droplets catalysis during the SiNWs growth performed in a hot wall LPCVD reactor at  $480^\circ\text{C}$  and 40 Pa. SiNWs local synthesis at micron scale is demonstrated using classical optical photolithography process. SiNWs grow with high density anchored at the dedicated catalyst islands. This resulting network is used to interconnect two heavily doped polysilicon interdigitated electrodes leading to the formation of electrical resistors in a coplanar structure. Current-voltage (I-V) characteristics highlight a symmetric shape. The temperature dependence of the electrical resistance is activated, with activation energy of 0.47 eV at temperatures greater than 300K.

## 1. Introduction

Owing to their physical and electrical properties, silicon nanowires (SiNWs) are currently attracting much attention as promising components for future nanoelectronic devices such as nanowire field effect transistors [1], photonic and optoelectronic devices [2]. SiNWs can be prepared by the top-down approach, using various advanced methods such as e-beam [3], AFM [4] or deep UV [5] lithography. The main disadvantage of these advanced lithographic tools with nanometer size resolution rests on the high cost generated. The bottom-up approach usually employs metal catalytic growth for preparation of SiNWs. Thus, VLS (Vapour-Liquid-Solid) growth technique uses metallic nanoparticles. The metal catalyst used is usually gold although other metals are also employed [6,7]. However, this approach suffers from the difficulty in precisely positioning the device.

In this work, we present a technological process based on localized metal deposition to activate vapour deposition synthesis of SiNWs by the VLS technique. The silicon nanowire network resulting is used to interconnect electrodes to achieve an electrical resistor in a coplanar structure.

## 2. Experiment details

The fabrication process of the SiNWs based resistors includes 2 photolithographic steps and process stages are represented on Figure 1. First, substrate (silicon wafer or glass substrate) is capped with a  $\text{SiO}_2$  layer deposited by Atmospheric Pressure Chemical Vapor Deposition (APCVD) and acts as a buffer film. Then, a heavily phosphorous *in-situ* doped amorphous silicon layer is deposited by Low Pressure Chemical Vapor Deposition (LPCVD) at  $550^\circ\text{C}$  and 90 Pa. Subsequent solid phase crystallization is performed at  $600^\circ\text{C}$  under vacuum to get a highly doped polysilicon film. This film is then patterned and dry etched to define the geometry of the comb shape electrodes (interdigitated structure shown in Figure 1-a). Au thin film ( $\leq 5$  nm) is then deposited by thermal evaporation and

locally removed using a lift off technique in order to define precise location for silicon nanowires synthesis (Figure 1-b). Finally, SiNWs are grown in a hot wall LPCVD reactor using silane as precursor gas in order to link together the two electrodes. Deposition temperatures and pressure are respectively 480°C and 40 Pa. This synthesis results in a tangled growth of SiNWs insuring electrical contact between the two doped electrodes (Figure 1-c). LPCVD parameters are chosen in order to avoid silicon deposition on areas uncovered with Au thin film. Different interdigitated structures can be achieved, varying number of teeth and local deposition of gold (on each tooth or half teeth). This fabrication process can be achieved either on silicon wafer or on other substrate compatible with the maximum process temperature (600°C).

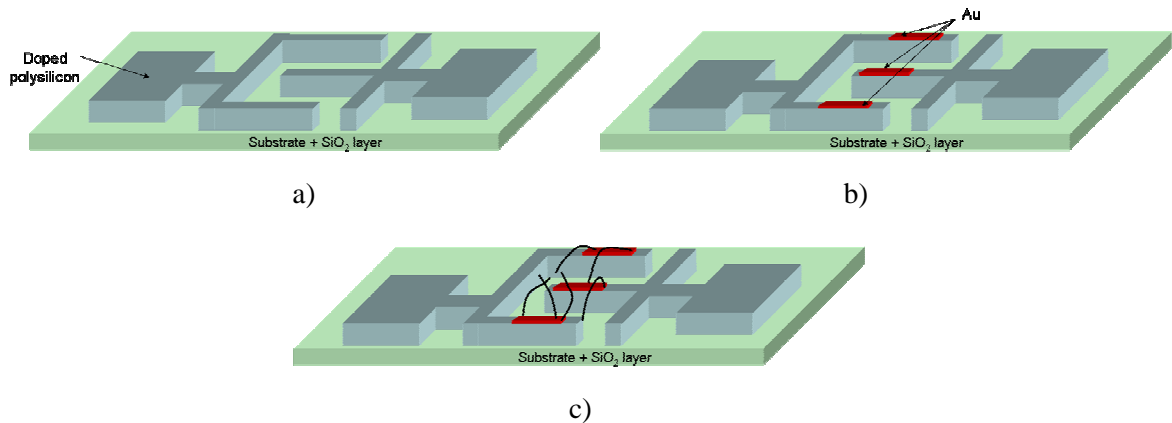


Figure 1: Key device fabrication steps of the SiNWs based resistors. a) definition of the comb shape electrodes geometry on a SiO<sub>2</sub> capped substrate. b) Thin film Au local deposition after lift off technique. c) Growth of SiNWs by LPCVD.

I-V characteristics were performed by using a HP 4155 B semiconductor parameter analyzer. Dark current versus temperature was performed by using a Keithley 617 electrometer. Samples were placed in a cryostat under vacuum and temperature varied from 100 K to 580 K. SEM observations were also performed to show SiNWs shape and length.

### 3. Results and discussion

Figure 2-a) shows high density SiNWs network synthesized by LPCVD at 480°C and 40 Pa. SiNWs exhibit a diameter around 100 nm (not shown here) and a length that can reach at least 10 μm. Since spacing between teeth does not exceed 10 μm, SiNWs can insure interconnexion between electrodes as shown in Figure 2-b). Most SiNWs interconnect themselves during their synthesis insuring this way the electrical conduction between the two electrodes.

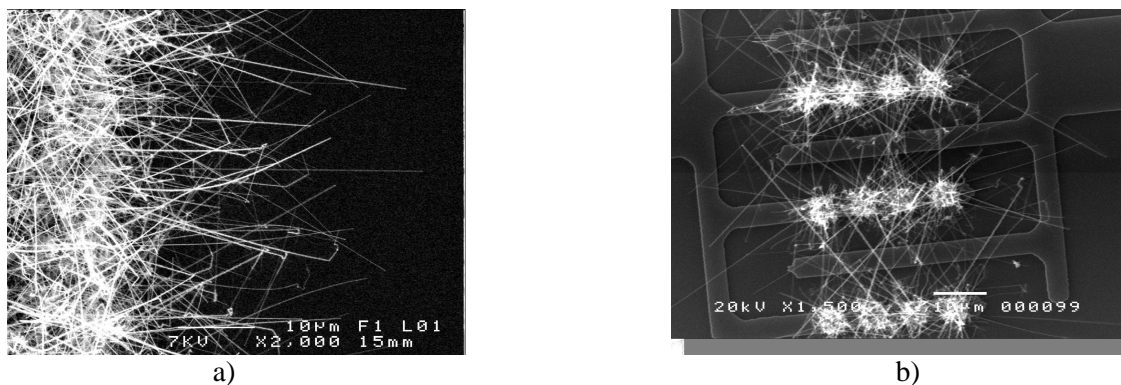


Figure 2: a) SEM observation of SiNWs synthesized. Length can exceed 10 μm. b) SEM observation of SiNWs based resistor (Au was deposited on local areas on half teeth).

Figure 3 shows the I-V characteristics of the SiNWs comb shape resistors after localized SiNWs synthesis. As a reference, I-V characteristic before SiNWs growth was also plotted (curve  $\times$ ) in order to insure initial electrical insulation between the two electrodes. This set of measurements highlight a good qualitative correlation between current levels measured and parameters as space between teeth ( $w$ ) and the number of teeth of the comb resistor ( $n$ ). Indeed, current increases as space between teeth ( $w$ ) decreases and number of teeth increases. On the other hand it is difficult to make a fair performance comparison between comb shapes because the number of participating nanowires can be vastly different.

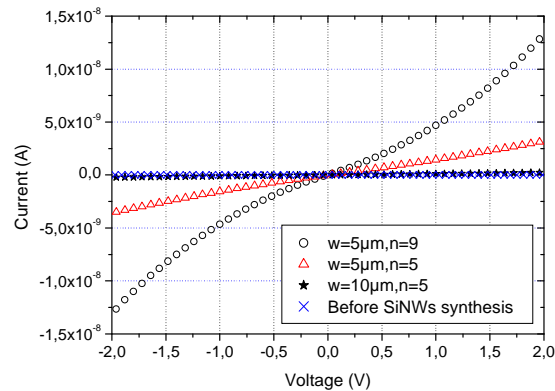


Figure 3: I-V characteristics of SiNWs comb shape resistors depending on the space between teeth ( $w$ ) and the number of teeth ( $n$ ).

Figure 4 shows the temperature dependence of the current under obscurity and the electrical resistance of the interdigitated structures. At temperatures above 300K, a well defined activation energy of 0.47 eV can be determined by fit. At temperatures below 200K, the resistance tends to saturate indicating a different conduction mechanism coming from carriers hopping between localized states. Such states can be associated to defects located either in the bulk or at the surface of the wires.

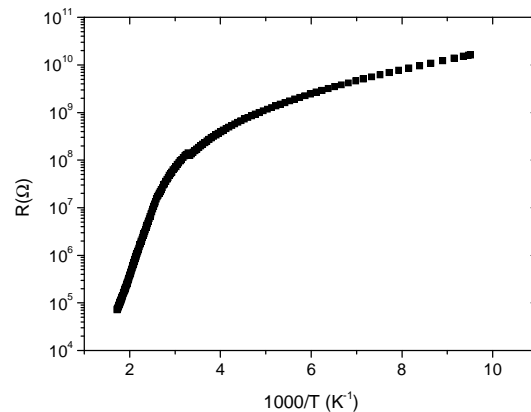


Figure 4: Resistance-Temperature dependence of SiNWs based devices.

Main interest of SiNWs rests on their high surface that can be sensitive to charges. Figure 5 shows results of a simple test that consists in exposing SiNWs to smoke in a cryostat. Upon exposure to smoke, current is found to dramatically increase and this phenomenon exhibits a reversibility aspect when air is re-introduced. This first demonstration serves only as a proof-of-concept for a new kind of sensor based on silicon nanowires. Indeed, SiNWs are of special interest because they are expected to play an important role as their surface can be modified with functional group.

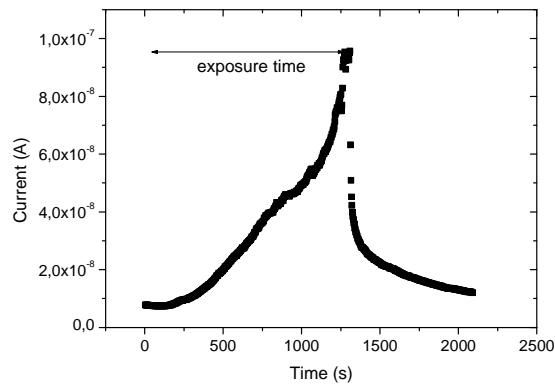


Figure 5: Current response of the device as a function of time upon exposure to smoke.

#### 4. Conclusion

A random network of silicon nanowires was synthesized via the VLS mechanism in a LPCVD reactor using Au as metal catalyst and silane as precursor gas in order to achieve SiNWs comb shape resistors between two electrodes. Temperature dependence of the electrical resistance of the structure is of activated type, with a well defined activation energy of 0.47 eV in the high temperature range. At temperatures below 100K, a hopping conduction mechanism is observed. SiNWs are expected to be used as highly sensitive sensors for a wide range of functional applications.

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