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Variable range hopping conduction in N- and P-type *in situ* doped polycrystalline silicon nanowires

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Abstract
Temperature dependence of electrical properties in N- and P-type *in situ* doped polycrystalline silicon nanowires synthesized by the sidewall spacer formation technique has been studied. Experimental analysis has been carried out for a temperature range from 200 K to 530 K on *in situ* doped polycrystalline silicon nanowires with doping level varying from 2×10^{16} to 9×10^{18} cm^{-3}. Results show that for N- and P-type doped samples the temperature dependence of the conductivity follows the 3D variable range hopping model due to hopping between localized electronic states near the Fermi level. The corresponding densities of states are determined following exponential (tail states) distributions associated to the statistical shift of the Fermi level.

(Some figures may appear in colour only in the online journal)

1. Introduction

Quasi-one dimensional semiconductor nanowires feature a high surface-to-volume ratio and special electronic and optical properties, arising from the size confinement in the nano-sized channel region [1–4]. These unique aspects, especially in silicon nanowires (SiNWs), stimulate enormous research efforts to design and develop a new generation of high performance FET transistors and sensors by incorporating the SiNWs as the functional channels. The SiNWs technologies highlighting intrinsic compatibility to classical silicon technology have the potential to enable the development of innovative, high-performance and low-cost sensors applications, and bring significant impact in areas of electronics, mechanics, genomics and biomedical diagnosis.

SiNWs can be synthesized by the top-down approach, using various advanced methods such as e-beam [5], AFM [6] or deep UV [7] lithographies. The main disadvantage of these advanced lithographic tools with nanometer size resolution rests on their high cost. An alternative way is the bottom-up approach that usually employs metal catalytic growth. The most commonly used growth technique is the VLS (vapor–liquid–solid) method using metallic nanoparticles. The metal catalyst used is usually gold although other metals are also employed [8]. However, this approach suffers from the difficulty in precise positioning and self-orientation of the nanowires in a planar configuration.

In this work, SiNWs are synthesized without requiring costly lithographic tools, following the sidewall spacer formation technique (top down approach), commonly used in submicron scale device silicon technology to insulate device active area. The spacer at nanometric scale made of silicon constitutes the nanowire. This method is an alternative way to synthesize SiNWs in a 2D configuration [9, 10] compatible with planar Si technology. In this case, SiNWs present a polycrystalline structure, and their electrical behavior is expected to be different from crystalline SiNWs due to higher defect density. In this kind of disordered material, the electronic transport is strongly affected by the carriers trapping effects at these defects. The corresponding energy distribution of the states (DOS) is representative of the crystal quality of the material, and many studies have been devoted to the determination of the DOS.

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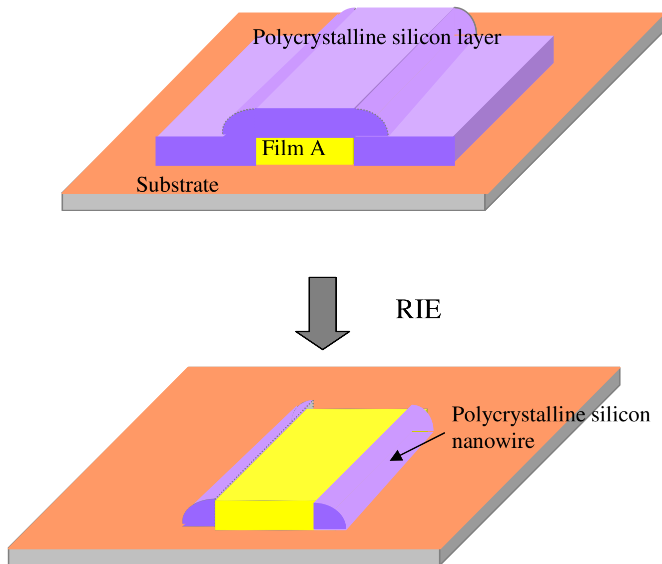


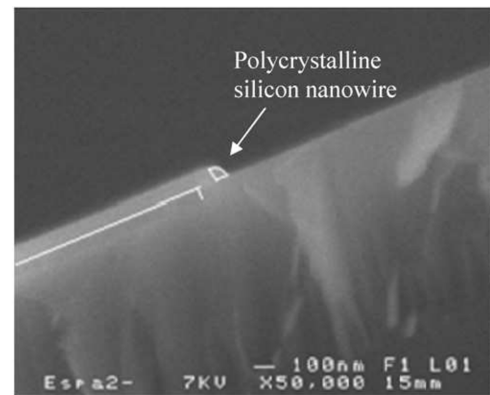
Figure 1. Fabrication of polycrystalline silicon NWs by the sidewall spacer formation technique.

Few studies about electrical behavior in polycrystalline silicon NWs have been reported. Thus, prior to developing polycrystalline silicon NWs based devices, in particular for high-performance electronics applications, a good understanding of electronic polycrystalline silicon NWs properties is required. In this paper, carrier transport in polycrystalline silicon NWs is analyzed as a function of temperature and doping level. Analysis is based on the hopping process between localized states related to the nanowire size-dependent defect density within the polycrystalline silicon nanowire. An experimental approach to extract exponential localized tail states distributions is presented.

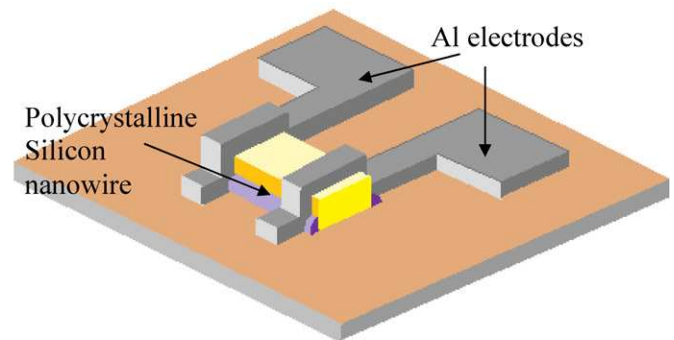
2. Experimental details

The key fabrication steps of polycrystalline silicon NWs are illustrated in figure 1. First, a dielectric film A is deposited on an oxidized silicon substrate and patterned into islands by conventional UV lithography. Then, a polycrystalline silicon layer is deposited by the LPCVD technique. Accurate control of the polycrystalline silicon layer reactive ion etching (RIE) rate leads to the formation of nanometric size sidewall spacers that can be used as nanowires. The feasibility of this technological step was previously reported [10]. Thus, polycrystalline silicon NWs with a 50 nm curvature radius were synthesized (see figure 2(*a*)). This method allows the fabrication of the parallel SiNWs network.

Phosphorus (or Boron) *in situ* doped polycrystalline silicon films used for nanowires were deposited by thermal decomposition of a mixture of pure silane and phosphine (or diborane) diluted in helium. The *in situ* doping level is controlled by adjusting the PH_3/SiH_4 (or B_2H_6/SiH_4) mole ratio varying from 0 for undoped films to 6×10^{-5} (or 10^{-4}) for heavily doped films. The corresponding incorporated phosphorus (boron) atoms' concentrations, C_P (C_B), previously determined from SIMS (secondary ions mass spectroscopy) analysis, varies from 2×10^{16} to 9×10^{18} cm^{-3} (or 2×10^{16} to 6×10^{18} cm^{-3}) [11]. Silicon films were deposited in an amorphous state at 550 °C and 90 Pa, and then crystallized by a thermal annealing in vacuum at 600 °C for 12 h.



(*a*)



(*b*)

Figure 2. (*a*) SEM picture of the 50 nm radius curvature polycrystalline silicon NW cross section view. (*b*) Polycrystalline silicon NWs-based resistor used for electrical measurements.

The *in situ* doped polycrystalline silicon NWs were integrated into resistors devices in coplanar structure (figure 2(*b*)) for electrical characterization. In this way, the nanowires were capped by a SiO_2 layer deposited by the atmospheric pressure chemical vapor deposition (APCVD) technique at 420 °C and contact openings wet etched. Contact electrodes were made of thermally evaporated aluminum and defined by wet etching. Finally a thermal annealing in the forming gas (N_2/H_2:0.9) was carried out at 390 °C to ensure good electrical contacts. Resistors were fabricated with 10 μm length parallel SiNWs.

Electrical dark conductivity of the polysilicon nanowires, σ, was deduced from $I(V)$ measurements collected at room temperature using a HP 4155 B semiconductor parameter analyzer. For current-temperature measurements, in the range 200 K to 530 K, samples were placed in a cryostat in vacuum (10^{-3}–10^{-4} Pa) and dark current was measured using a Keithley 617 electrometer.

3. Results and discussion

The polycrystalline silicon NWs structural quality is quite different from the polycrystalline silicon layer. Indeed, because the crystallization process of the amorphous silicon layer from

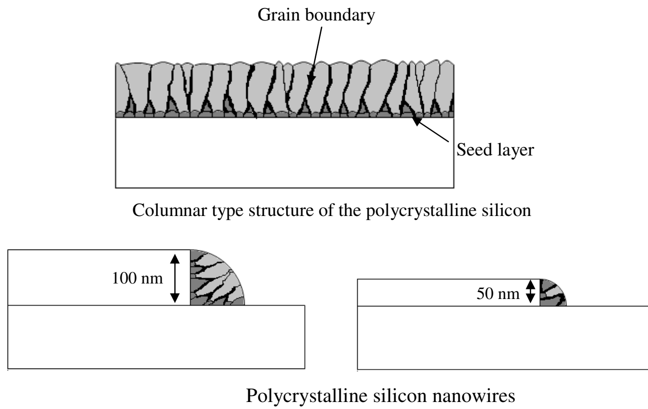


Figure 3. Schematic illustration of structural defects in the core of the polycrystalline silicon NWs.

which NWs are processed starts from seeds located at the bottom interface (seed layer in figure 3), the polycrystalline silicon layer is usually considered to be made of large size (>100 nm) monocrystalline grains with a columnar-type structure. In this case, according to Seto's theory [12] carriers transport is strongly affected by intergranular barriers induced by the carriers trapping effect at defects located at these grain boundaries. Such electrical behavior was previously reported by our group for 100 nm radius curvature polycrystalline silicon nanowires [13]. Indeed, as illustrated in figure 3, the structural defect density involved (including grain boundaries) is higher in the inferior part of the layer (few nanometers thick) constituting the nanowires. Thus, the structural quality of the 50 nm radius curvature NWs is likely quite similar to micro- or nano-crystalline silicon material embedding quasi uniformly distributed high defect density (strongly affecting carriers transport). Therefore, a different transport mechanism is expected in these NWs. The most convenient model describing electrical properties in such disordered N- or P-type semiconductor material is the carrier hopping between localized states close to the conduction band (E_C) or valence band (E_V) edges, respectively, firstly proposed by Mott [14]. In this case, the carrier transport mechanism is thermally activated. The activation energy was deduced from the slope of the linear decrease of the electrical conductivity in an Arrhenius representation. For N- and P-doped polycrystalline silicon nanowires, the corresponding measured activation energy (E_A) decreases with the doping concentration, and is significantly lower than the expected values for polycrystalline silicon layers [12] (figure 4(*a*). In particular, measured activation energy for undoped silicon nanowires is significantly lower than the expected midgap value for undoped silicon (∼0.55 eV). Such values of E_A highlight that thermoelectronic conduction is not predominant and validate the contribution of localized states for carrier transport. In addition, the decrease of E_A is related to the increase of the carrier number in the silicon nanowires and thus also to the statistical shift of the Fermi level into the bandgap energy.

Electrical properties of polycrystalline silicon NWs were investigated as a function of temperature and *in situ* doping level. For all studied polycrystalline NWs, dark conductivity

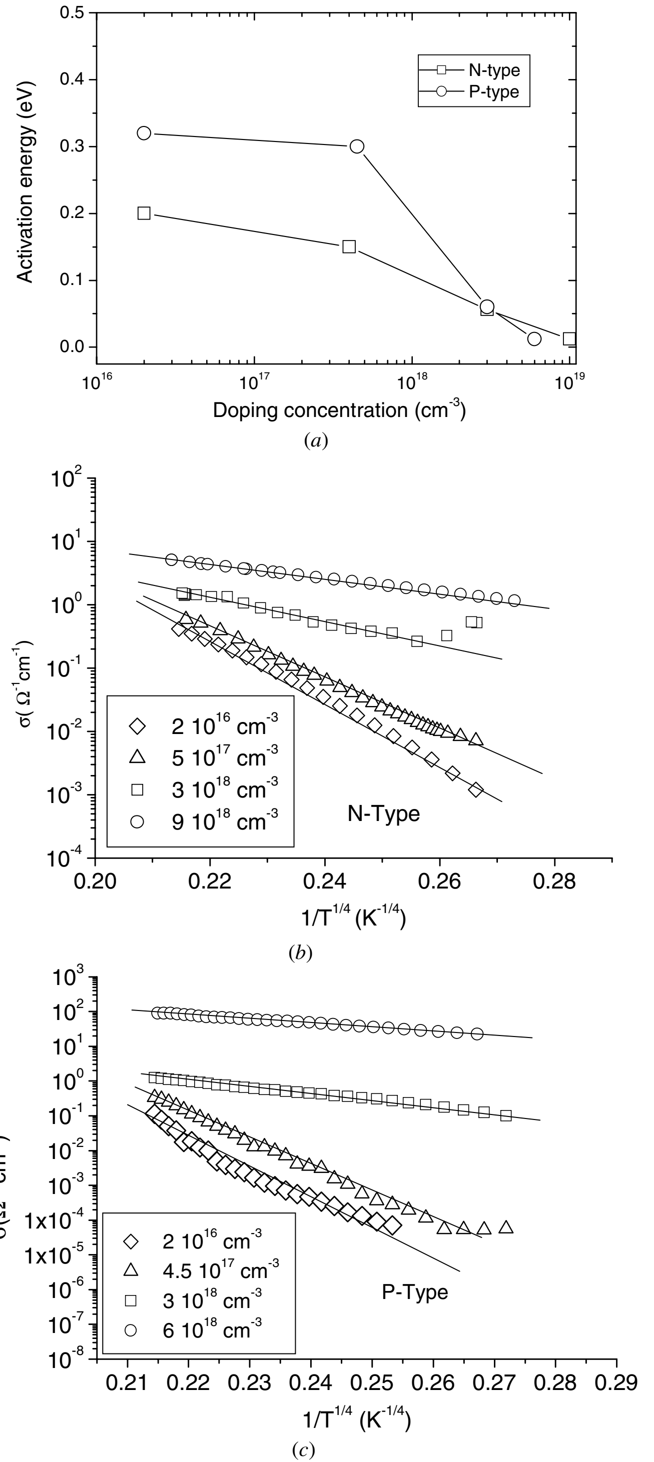


Figure 4. (*a*) Plots of the N- and P-doped polycrystalline silicon nanowires electrical conductivity activation energies versus doping concentrations. (*b*) Dark conductivity as a function of $T^{-1/4}$ for N-type (*a*) and P-type (*c*) polycrystalline silicon NWs.

is thermally activated, and the temperature dependence, displayed in figures 4(*b*) and (*c*), follows the 3D variable range hopping (VRH) mechanism described by Mott's law [14]:

$$\sigma = \sigma_0 \exp\left[-\left(\frac{T_0}{T}\right)^{1/4}\right] \quad (1)$$

where in our case σ_0 and T_0 are both dependent on the doping level, and [15–19]:

$$T_0 = \frac{\gamma^3 c^4}{kN(E_F)} \tag{2}$$

with k being the Boltzmann constant, $N(E_F)$ being the density of localized states near the Fermi level calculated by adjusting the parameter electronic wave decay length γ^{-1} for localized states (0.3 nm $\leqslant \gamma^{-1} \leqslant$ 3 nm) and c being a constant in the range of 2.06–4.2 depending on the $N(E_F)$ feature [16]. In this model, hopping refers to carrier tunneling transitions from occupied to unoccupied localized states, the state energy difference being bridged by emission of absorption of one or several phonons. The hopping between states close in energy level (even if they are wider spaced) becomes preferable to those between the nearest neighbors whose energies differ substantially. In addition, according to Mott [14], $N(E_F)$ is assumed as an energy-independent distribution, and a large number of previous studies on carrier transport [15–19], in particular in amorphous, micro- or nano-crystalline silicon layers, reported the average value depending on the quality of the material.

The conductivity prefactor, σ_0, deduced from linear fits in figures 4(*b*) and (*c*), follows (figure 5)

$$\sigma_0 = \sigma_{0m} \exp\left[\left(\frac{T_0}{T_m}\right)^{1/4}\right] \tag{3}$$

where T_m and σ_{0m} are independent of doping level, with $T_m \approx 755$ K, $\sigma_{0m} \approx 3.4\ \Omega^{-1}\ \mathrm{cm}^{-1}$ for N-type NWs, and $T_m \approx 830$ K, $\sigma_{0m} \approx 15.5\ \Omega^{-1}\ \mathrm{cm}^{-1}$ for P-type NWs. According to previous study based on numerical modeling of single-phonon hopping transport [16], such positive correlation between these two parameters predicts an exponential distribution of the localized electronic states $N(E_F)$ related to strained bond-type defects (tail states) in the core of the disordered semiconductor. Such a state distribution feature acts as a quality factor of the polycrystalline silicon NWs.

The localized states densities were deduced from relation (2) for each doping level for N- and P-type samples, respectively. Calculations were carried out for $c = 4.2$ corresponding to an exponential state distribution [16]. The variations of $N(E_F)$ with doping level are reported in figure 6 for 0.3 nm $\leqslant \gamma^{-1} \leqslant$ 3 nm (gray area). Previous works [20, 21] reported that the doping species mainly affect the deep state defect distribution (dangling bonds) feature, in particular for hydrogenated amorphous silicon layer, but few changes for shallow tail states distributions. In this case, one can consider that the variations of $N(E_F)$ with the doping level should give an insight into the corresponding exponential states distributions for one adjusted γ^{-1} value. However, representation of such DOS versus the statistical shift of the Fermi level into the bandgap energy is commonly used. In this way, one can assume that the average free electron (n) and hole (p) concentrations for N-type and P-type samples, respectively, are given by $n = N_C \exp(-(E_C\text{-}E_F)kT) = \eta_N C_P$ and $p = N_V \exp(-(E_F\text{-}E_V)kT) = \eta_P C_B$, where η_N and η_P ($\leqslant$1) are the doping efficiencies, N_C and N_V the effective conduction and valence band state densities ($N_C \approx N_V \approx 3 \times 10^{19}$ cm^{-3}). Thus, the plots in figure 6 are directly related to the usual representations of the DOS. Previous work [11] reported that for polycrystalline silicon layers deposited under the same conditions as for the nanowires, doping efficiency is high (~100%) for high doping levels. For such a doping efficiency for our polycrystalline silicon NWs, and such that it does not significantly influence the calculation of the Fermi level from the bandgap edges, $E_F\text{–}E_C \approx \mathrm{kT} \times \ln(C_P/N_C)$ and $E_V\text{-}E_F \approx \mathrm{kT} \times \ln(C_B/N_V)$ for *N*- and *P*-doped NWs, respectively. In this case, the corresponding DOS versus E_F were replotted in figure 7 for highest γ^{-1} values to be consistent with $N(E_F)$ values obtained by others experimental methods for highly disordered silicon films [17, 20, 22].

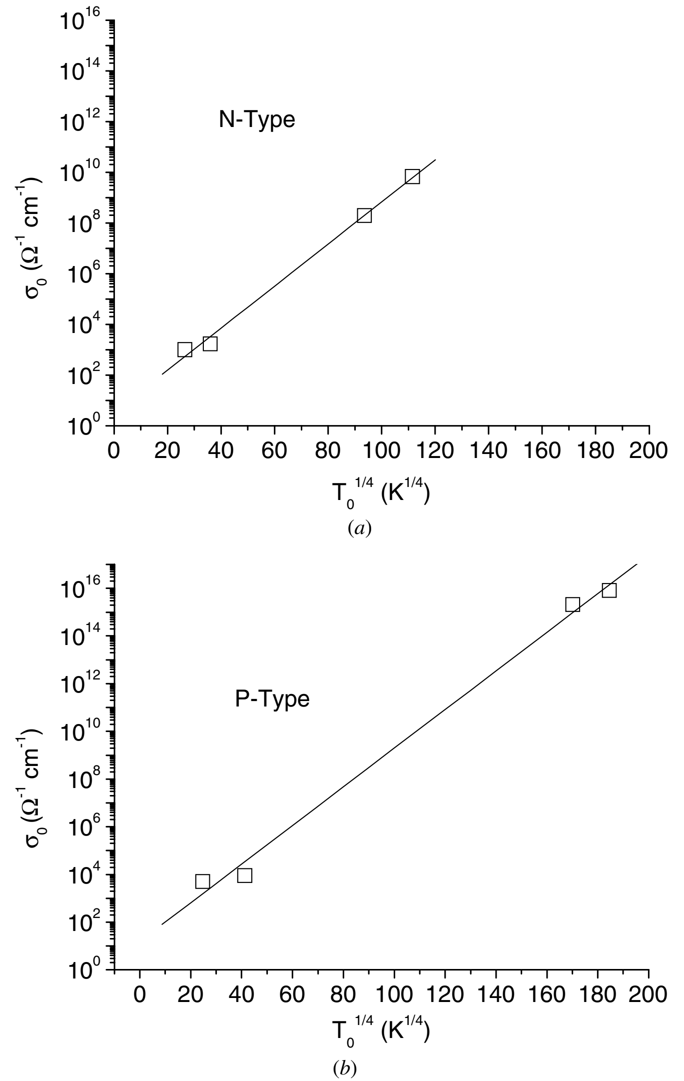


Figure 5. Dark conductivity prefactor as a function of $T_0^{1/4}$ for N-type (*a*) and P-type (*b*) polycrystalline silicon NWs.

According to these results, $N(E_F)$ related to shallow tail states distributions (close to the band gap edges) can be modeled as

$$N(E_F) = N_{0C} \exp\left(\frac{E_F - E_C}{E_{0C}}\right) \tag{4}$$

and

$$N(E_F) = N_{0V} \exp\left(\frac{E_V - E_F}{E_{0V}}\right). \tag{5}$$

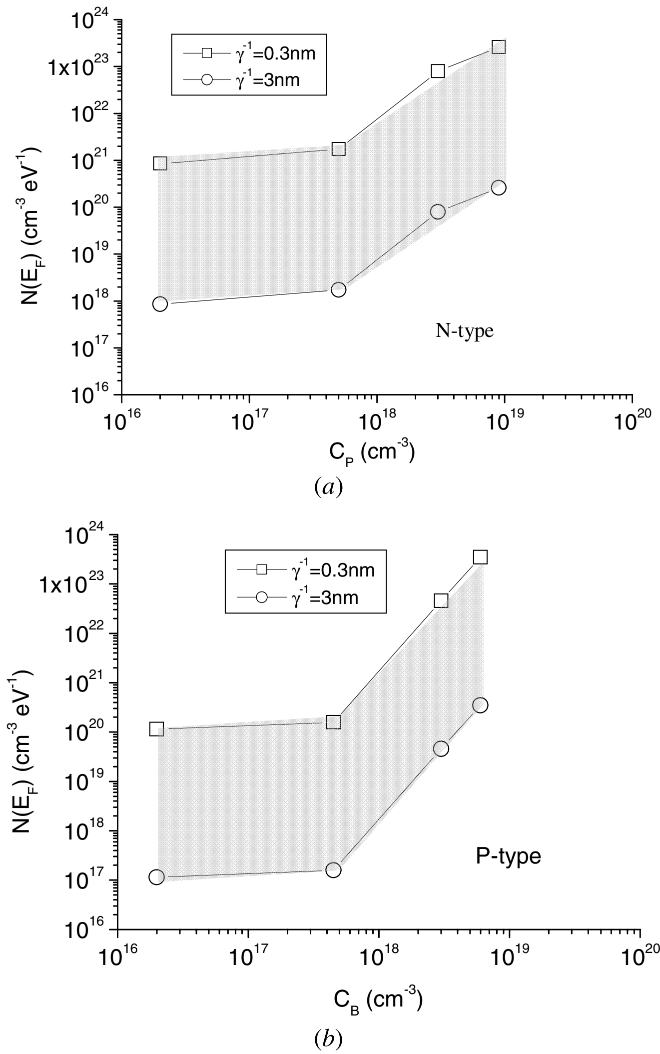


Figure 6. Distribution of localized states as a function of the doping level calculated with $c = 4.2$, and for $0.3\ \text{nm} \leqslant \gamma^{-1} \leqslant 3\ \text{nm}$ (gray area), for N-type (*a*) and P-type (*b*) polycrystalline silicon NWs.

Here $N_{0C} = 3 \times 10^{21}\ \text{cm}^{-3}\ \text{eV}^{-1}$, $E_{0C} = 15$ meV, $N_{0V} = 4 \times 10^{22}\ \text{cm}^{-3}\ \text{eV}^{-1}$, and $E_{0V} = 9$ meV deduced from the linear fit of the plots in figure 7 corresponding to $N(E_F)$ values calculated for highly doped N- and P-type samples, respectively. Even if the γ^{-1} value is not obvious, these results of our proposed bandgap shallow tail state model mean that $\gamma^{-1} \sim 3$ nm is an appropriate value for the studied polycrystalline silicon NWs. Moreover, such a value has been recently reported for such $N(E_F)$ behavior deduced from analysis of the field effect conductance of low-temperature ($\leqslant$600 °C) N-channel polycrystalline silicon TFTs reporting experimental determination of shallow tail state distribution close to the conduction band [23]. In addition, these exponential states distributions are consistent with theoretical studies previously reported in the case of hydrogenated amorphous silicon [20, 21]. However, for lightly doped samples the doping efficiency is significantly lower than for highly doped ones. Therefore, the plots of $N(E_F)$ are not representative of the tail state distributions following (4) and (5). In this case, due to the high defect density

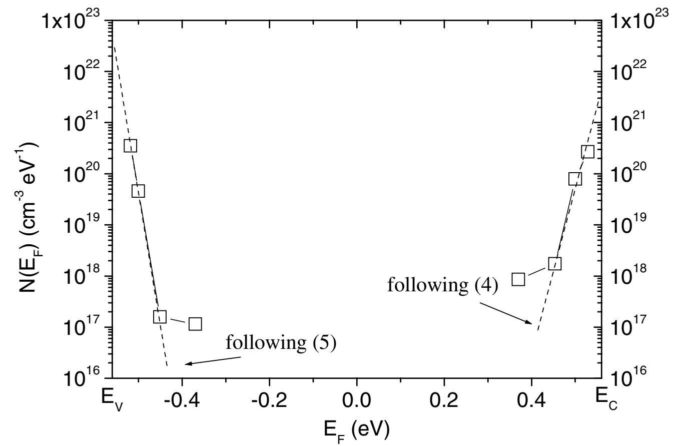


Figure 7. Distributions of localized states calculated with $\gamma^{-1} = 3$ nm as a function of the position of the Fermi level. The energy bandgap value is $E_G = 1.12$ eV. Dotted plots: calculated exponential shallow tails states distributions (close the bandgap edges) following (4) and (5) with a linear regression coefficient $R = 0.97\,683$ or $0.99\,999$, respectively.

within the polycrystalline silicon NWs one can consider that the Fermi level is pinned and thus a quasi constant value of $N(E_F)$ is measured. This result could be related to the energy-independent $N(E_F)$ assumed in Mott's model, usually reported in many previous experimental analysis of the 3D VRH mechanism in undoped disordered semiconductors [15, 17–19, 24]. Only theoretical or numerical models proposed an exponential distribution of localized states for hopping process [16, 25]. Therefore, our experimental analysis gives an approach to determine the DOS to qualify disordered semiconductors and validates the model of exponential states distribution for the VRH model.

4. Conclusion

Analysis of the dark conductivity of 50 nm curvature radius P- and N- type *in situ* doped polycrystalline silicon nanowires shows that carrier transport is described by a 3D variable range hopping mechanism between defect states near the Fermi level. In this experimental study, we emphasized the influence of the structural defect densities on specific description of carriers transport. Analysis shows that the localized state distributions are related to the statistical shift of the Fermi level. In addition, our study allows the determinations from the VRH model of the corresponding exponential shallow tail state distributions close to the valence and conduction bands' edges to qualify the polycrystalline silicon nanowires.

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