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P-type and N-type multi-gate polycrystalline silicon vertical thin film transistors based on low-temperature technology

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ABSTRACT

P-type and N-type multi-gate vertical thin film transistors (vertical TFTs) have been fabricated, adopting the low-temperature (T ≤ 600°C) polycrystalline silicon (polysilicon) technology. Stacked heavily-doped polysilicon source and drain are electrically isolated by an insulating barrier. Multi-teeth configuration is defined by reactive ion etching leading to sidewalls formation on which undoped polysilicon active layer is deposited. All the polysilicon layers are deposited from low pressure chemical vapor deposition (LPCVD) technique. Vertical TFTs are designed with multi gates, in order to have a higher equivalent channel width. Different active layer thicknesses have been attempted, and an I_{ON}/I_{OFF} ratio slightly higher than 10^5 is obtained. P-type and N-type vertical TFTs have shown symmetric electrical characteristics. Different geometrical parameters have been chosen. I_{OFF} is proportional to the single channel width, and to the tooth number. I_{ON} is only proportional to the tooth number. These devices open the way of a CMOS-like technology.

Keywords: 3D structure, Thin film transistor (TFT), Plasma etching, Polycrystalline silicon.

1. INTRODUCTION

Polycrystalline silicon thin film transistor (polysilicon TFT) has shown its interest in various applications, such as the solar cells [1], random access memories (RAMs) [2], flat panels for imaging [3], and especially in the display domains as AMLCD [4] or AMOLED [5]. For these applications, a higher integration density and thus a higher current density are looked for. Thus, the primary motivation of this work is this target that could be obtained by adopting a short channel length for the transistors. The vertical thin film transistor (vertical TFT) enables fabricating transistors with ultra-short channel length that is determined by the deposited film thickness instead of the lithographic limitation as in its planar counterpart. Indeed, this limitation is rather high due to large area process and, a better control of the channel length seems a very exciting issue. Much research has been carried out on polysilicon VTFTs.

The James D. Flammer's group has fabricated polysilicon VTFTs adopting Arsenic implanted source and drain, which degrades after annealing [6]. The Tan Fulei's group has used a bottom gate vertical TFT structure with a self-aligned offset [7], and excimer laser annealing methods [8] to crystallize the active layer. However, this self-aligned offset structure requires high temperature, and the high cost and homogeneity are the technological drawbacks of the laser crystallization. In our work, the VTFTs are fabricated with low-temperature polysilicon technology, which is compatible with glass substrates, while a homogeneous crystallization as well as an *in-situ* doping can be obtained. In previous work

[9], polysilicon VTFTs were fabricated with an undoped polysilicon active layer between two heavily-doped polysilicon layers (source and drain). However, the large overlapping area between source and drain has led to a strong off-current, I_{OFF} [9]. In this paper, a novel polysilicon VTFT structure has been proposed, which eliminates the large overlapping area by the introduction of an insulating barrier between source and drain. In addition, different geometrical parameters have been chosen, i.e., different tooth widths, Wt (10 µm and 20 µm), different numbers of teeth, Nt (1, 2 and 4), and different single channel widths, Wc (10 µm, 20 µm and 30 µm). The key point of the fabrication process lies in the formation of the continuous sidewalls due to the difference of the etching selectivity between the polysilicon and the insulating barrier. In this paper, the detailed fabrication process is introduced and electrical characterizations of the devices are presented, analyzed and discussed, more especially, the comparison between electrical behaviors of the P-type and N-type VTFTs.

2. DEVICE STRUCTURE AND DESIGN

For the polysilicon VTFTs, the schematic three-dimensional (3D) view is shown in figure 1 (a). The 3D structure enables several gates positioned in parallel, with the gate electrode passing over all the teeth. Source and drain are discriminated by a partial etching until reaching the bottom heavily-doped polysilicon layer. The RIE endpoint control is obtained from a laser interferometer measurement. Fig. 1 (b) shows clearly the cross-sectional view of a basic tooth structure including two channels. Source and drain contacts are located in front and behind the cross-sectional plan, and they are electrically isolated by an insulator barrier. Active layer is deposited after the formation of the tooth sidewalls, the distance between the two sidewalls being as small as the design rule, defined by lithography, allows. The channel

length, L, is defined by the barrier thickness located in-between the both heavily doped polysilicon layers.

3. FABRICATION PROCESS

Thin film technology is adopted to fabricate the devices, and the polysilicon thin films are the determinant factor for the fabrication of the vertical TFTs. The polysilicon layers are deposited from LPCVD technique at 550°C and 90 Pa using silane (SiH_4) as precursor gas. At these conditions, the films are still in amorphous state [10]; therefore a solid phase crystallization step (SPC) is carried out at 600°C for 12 hours to crystallize the amorphous silicon into polysilicon. The combined techniques of LPCVD and SPC have been adopted in the lateral TFTs fabrication, combination that was proved to be a way to obtain a high field effect mobility of carriers higher than 100 $cm^2/V\cdot s$ with an I_{ON}/I_{OFF} of more than 10^6 [11]. Therefore, this technology will also be used in our vertical TFTs fabrication. In addition, *in-situ* doping can be obtained by adding dopant gases to the precursor gas, SiH_4: Phosphine, PH_3, for N-type doping or diborane B_2H_6 for the P-type. Therefore, P-type and N-type VTFTs could be easily fabricated in the same run, just by adopting different doping gases for source and drain regions. In the whole fabrication process, the maximum temperature doesn't exceed 600°C.

As mentioned above, due to the dependence of active layer properties on the sidewall profile, the sidewall formation is a critical step during the fabrication process. Prior to the fabrication process, much work has been devoted to form continuous sidewalls by reactive ion etching (RIE) in order to better control the quality of the deposited active layer. Indeed, as crystallization process occurs at substrate (i.e. sidewall)-layer interface, a recess as well as a

high sidewall roughness (due to reactive ion etching) would lead to the formation of a high density of seed sites, which would induce a serious decrease of the crystalline quality of the layer.

A SiO_2 layer was involved as the insulating barrier layer in the first run. In order to reduce the recess in the sidewalls due to the difference of etching selectivity between poly-Si and the SiO_2 barrier, the SiO_2 layer should be very thin (figure 2). The thicker SiO_2 layer is, the larger the recess. Thus, to ensure a sufficient channel length, L, another undoped polysilicon layer is deposited on the insulator film. For the fabrication process, the adopted SiO_2 thickness is 100 nm, considering that the breakdown voltage, V_{BD}, is about 0.5 V/nm, while the undoped polysilicon thickness is 1 µm, in this case. Figure 2 shows that an etching processed at a high RF power, with a reduced etchant gas pressure, leads to appropriate sidewalls. The channel length, L, is approximated to the barrier thickness, i.e., L = 1.1 µm, knowing that a little extra-length is due to the tilt angle of the sidewalls, about 70° (1/cos70° = 1.06).

After adjusting the sidewall profiles, a five-mask process is carried out to fabricate the vertical TFTs. After the classical cleaning of the substrates, a 500 nm thick SiO_2 layer, playing the role of a buffer, is deposited by APCVD at 420°C. Afterwards, the deposition of the first heavily-doped polysilicon layer is followed by the deposition of a 100 nm thick SiO_2 layer by APCVD. Then, a 1 µm thick undoped polysilicon layer is deposited by LPCVD. Finally, a heavily-doped polysilicon layer is also deposited by LPCVD. The silicon oxide and the undoped polysilicon layer define the insulating layer of figure 1(a), in between the two heavily-doped layers. After each silicon layer's deposition by LPCVD, a SPC step is carried out.

After the deposition steps, two RIE steps are implemented. Indeed, first photolithography and RIE steps are performed to define the multi-gate configuration, while the second photolithography and partial RIE steps are performed to form source and drain regions. This partial etching is achieved when reaching the bottom heavily-doped layer, and the precise control of the etching endpoint is achieved with the help of a laser interferometer. Afterwards, an undoped polysilicon active layer is deposited by LPCVD technique under the same conditions, and thus patterned by the third RIE process that enables to form a channel on each sidewall, i.e., two channels for one tooth.

An essential RCA cleaning step must be performed before gate oxide deposition, in order to eliminate the defects at the surface of the active layer. After the deposition of a 70 nm thick gate oxide layer by APCVD at 420°C, a densification step at 600°C for 12 hours is carried out to eliminate most defects in the gate oxide. After that, the contact openings for source and drain are defined by the fourth mask. After a 400 nm thick Aluminum layer deposited by Joule effect evaporation, the electrodes are defined by a wet etching step. The SEM top view and the schematic side view of the final fabricated VTFT are presented in figure 3 (a) and figure 3 (b), respectively. The top view clearly shows that the gate electrode passes above all the teeth at the same time that defines a multi-gate structure.

4. ELECTRICAL CHARACTERISTICS AND DISCUSSION

For the vertical TFTs, the active layer is deposited after the formation of the sidewall. Thus, different active layers can be obtained with the nearly same sidewall profile in the same run. Because a preliminary physical simulation predicted a role of the active layer thickness, T_{AC}, on both on-current and off-current, several values were selected: 225 nm, 150 nm, 100

nm. Figure 4 shows the transfer characteristics for these different thicknesses. We may observe nearly the same I_{ON}/I_{OFF} ratio of more than 10^5, for a drain-source voltage, V_{DS} = 100 mV. This indicates relative compensated effects on the two currents.

Table 1 shows the electrical parameters deduced from the transfer characteristics and on the classical model of a TFT. When increasing the active layer thickness, T_{AC}, the smallest threshold voltage, V_{TH}, and the highest field effect mobility, μ_{FE}, are obtained. This indicates a better crystalline quality of the active layer on the sidewall, when increasing T_{AC}, which is consistent with the polysilicon growth kinetics on the planar surface [12]. The rather low mobility μ_{FE} and high threshold slope S are more likely to be due to the high roughness of the sidewalls caused by the long-time of the RIE process. In fact, even though the sidewall profile has been optimized, there is still a recess of the sidewall at the interface between the polysilicon and the SiO_2 insulating layers. In addition, the morphology of the active layer crystallized on the sidewalls is still unknown, which may also affect the electrical parameters. Even if the mobilities are in the order of 10 $cm^2/V \cdot S$, these values are suitable for many applications.

Figure 5 (a) - (c) show the relationships of on-current, I_{ON}, off-current, I_{OFF}, and on/off-current ratio, I_{ON}/I_{OFF}, with different active layer thicknesses. I_{ON} and I_{OFF} show the same trend, that is: I_{ON} and I_{OFF} both increase with the active layer thickness, T_{AC}. The I_{ON} increases with T_{AC} due to the better crystalline quality. In addition, I_{OFF} increases with the active layer thickness T_{AC}; indeed, when increasing T_{AC}, a greater part of the active layer is not under gate control and thus results in a higher leakage. Figure 5 (c) shows that reducing the active layer thickness results in an I_{ON}/I_{OFF} increase; this means that there is a balance

between I_{ON} and I_{OFF} variations with different active layer thicknesses T_{AC}.

Due to the *in-situ* doping during the LPCVD process, P-type and N-type VTFTs could be easily fabricated in the same run, just by adopting different dopant gases (PH_3 or B_2H_6) for source and drain regions. For such VTFTs, the 150 nm thick active layer is chosen, corresponding to a good compromise between the I_{ON}/I_{OFF} ratio and the mobility μ_{FE}.

The typical transfer characteristics of the P-type and N-type VTFTs are shown in figure 6 (a), with the same W/L = 80 µm/1.1 µm. I_{ON}/I_{OFF} ratios slightly higher than 10^5 are obtained for both P and N-type VTFTs. For V_{DS} = 100 mV, the deduced electrical parameters are listed in table 2. The same subthreshold slope S of 1.9 V/dec is obtained for both P and N-type VTFTs. For P-type VTFT, the field effect mobility μ_{FE} is 4.2 cm^2/V·s, while the threshold voltage V_{TH} equals to -15 V. In contrast, for N-type VTFT, μ_{FE} is 7.5 cm^2/V·s, while V_{TH} equals to 9.8 V. The difference of threshold voltage V_{TH} between P-type and N-type VTFTs is consistent with the polycrystalline silicon lateral counterparts [13]. Nevertheless, the two types of VTFTs have shown symmetric I_{ON} and I_{OFF}, which demonstrates the feasibility for CMOS-like VTFT circuit applications as inverters or oscillators.

Figure 6 (b) shows the similar transfer characteristics of the source-on-top (SOT) and the drain-on-top (DOT), which indicates that the source and drain electrodes could be permuted. Figure 6 (c) shows the output characteristics of the fabricated VTFTs, the kink effect prevents the saturation of the drain current, which could be suppressed by increasing the channel length and thus undoped polycrystalline silicon thickness [14], and by improving the crystalline quality of the active layer on the sidewalls.

For P-type and N-type vertical TFTs, the electrical characteristics are analyzed in function

of different dimensions. The same relationships have been obtained for the two types of vertical TFTs, therefore, the relationships for P-type vertical TFTs are shown as an example. For I_{ON}, its relationships with different geometrical parameters are shown in figure 7. From figure 7, I_{ON} shows a linear relationship with the tooth number, N_t, as I_{ON} is directly related with the channel numbers (there are two channels for each tooth). In the first analyses, I_{ON} appears independent of the gate width, W_C. This behavior should means that a dependence of I_{ON} with W_C could be observed by decreasing the size, but a specific study must be made in this case, especially by improving the design rule.

Figure 8 gives the relationships between the off-current I_{OFF} and the geometrical parameters. From figure 8 (a) and 8 (b), I_{OFF} shows strictly linear relationships with the tooth number N_t as well as the single channel width W_c, which confirm that the off-current I_{OFF} is directly related with the active layer region. From figure 8 (c), I_{OFF} is independent of the tooth width W_t, which highlights that I_{OFF} is just brought by the active layer part between source and drain, while the active layer on top of the tooth doesn't have any effect on I_{OFF}.

By combining the analysis of on-current I_{ON} and off-current I_{OFF}, we can conclude that, for a fixed tooth width W_t, the I_{ON}/I_{OFF} ratio follows the equation:

$$\frac{I_{ON}}{I_{OFF}} \propto \frac{N_t}{N_t W_c} \propto \frac{1}{W_c} \qquad (eq.1)$$

Which means that for the vertical TFTs, the I_{ON}/I_{OFF} ratio can be increased by reducing the single channel width W_c, thus a narrow single channel width W_c is required, which is approximate to the design rule. This also indicates a reduction of tooth length, which is fixed at 60 μm for the current mask definitions in the first runs performed in the frame of this work.

In contrast, the tooth number, N_t, doesn't affect the final I_{ON}/I_{OFF} ratio, as expected, even though the higher tooth number, N_t, enables to provide a higher I_{ON}, which is the major advantage of our vertical TFTs. In addition, the I_{ON}/I_{OFF} ratio is not affected by the tooth width, W_t.

Dynamic characterizations of vertical TFTs were not performed, at this level of the study. It is clear that in the first designs, the frequency parameters were not optimized; indeed, the relatively large area of the source and drain coverage could lead to a high parasitic capacitance and decrease the frequency performances. However, this source to drain parasitic capacitance effect is lowered since we used a 1 µm thick undoped polysilicon layer deposited on the SiO_2 thin film, which increases the channel length as well as the equivalent insulating film thickness; thus it decreases this parasitic capacitance. In addition, for the tooth width, a stabilized industrial process should adopt the smallest distance compatible with the design rule. The area of the capacitance should be minimized in this case.

5. CONCLUSION

This paper presents a vertical TFT structure fabricated by a low-temperature process ($T \leq 600$°C) polysilicon technology. By adopting the multi-gate structure, the total channel width can be enlarged while the channel length can be very short for a vertical structure. The electrical results show an I_{ON}/I_{OFF} ratio of more than 10^5 with a field effect mobility μ_{FE} around 10 $cm^2/V{\cdot}s$ for different active layer thicknesses. P-type and N-type VTFTs have been fabricated, the symmetric electrical characteristics have been obtained, which enable

CMOS-like applications. The relationships of the electrical characteristics and the geometric parameters have also been analyzed, the off-current I_{OFF} is proportional to the tooth number, N_t, and the single channel width, W_c, while the on-current, I_{ON} is only proportional to N_t. This indicates that I_{ON}/I_{OFF} ratio could be enlarged by adopting a smaller W_C that approximates to the design rule, which needs a modification of the masks. In addition, the field effect mobility μ_{FE} could be increased by reducing the sidewall roughness and improving the crystalline quality of the active layer.

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Figure captions

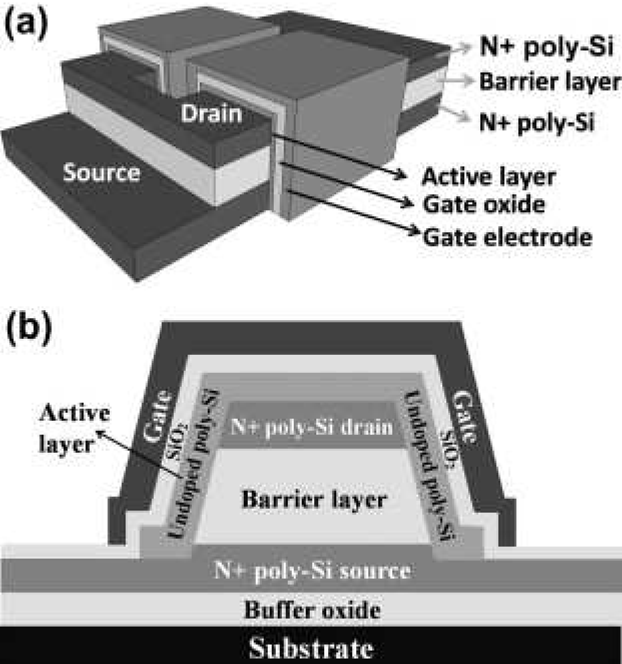

Figure 1: (a) 3D schematic of the VTFT structure, and (b) cross-sectional view of a tooth structure. The 3D view shows multi gates. The tooth structure shows that the source and drain electrical path is blocked by an insulating barrier, while the active layer is deposited after the formation of the teeth (sidewalls).

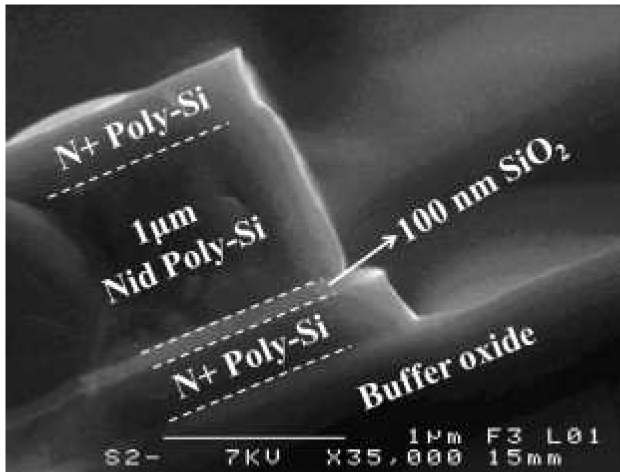

Figure 2: SEM of the optimized sidewall profile, which enables the active layer, the gate oxide layer, and the Al layer depositions on it. It remains, however, a small recess at the level of the SiO_2 insulating layer due to the etching selectivity difference.

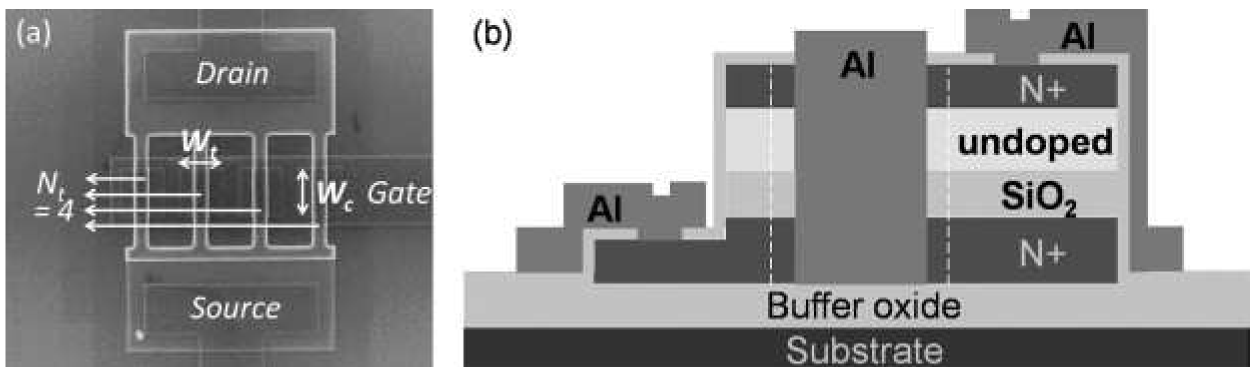

Figure 3: (a) SEM top view and (b) schematic side view of the fabricated vertical TFT. The geometrical parameters, including the tooth number, N_t, the single channel width, W_c, and the tooth width, W_t, are marked on the top view.

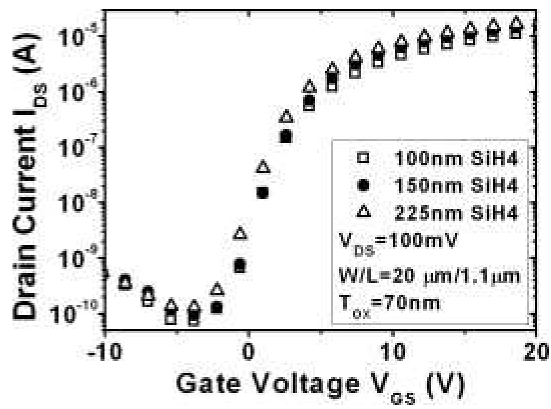

Figure 4: Transfer characteristics for different active layer thicknesses T_{AC} (225 nm, 150 nm, and 100 nm), I_{ON}/I_{OFF} ratios higher than 10^5 are obtained.

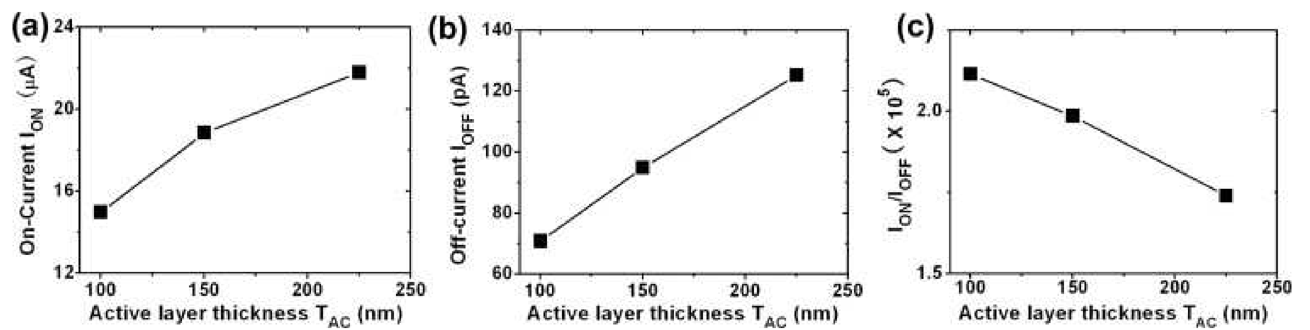

Figure 5: (a) On-current I_{ON}, (b) off-current I_{OFF}, and (c) I_{ON}/I_{OFF} relationships with different active layer thicknesses T_{AC}. I_{ON} and I_{OFF} increases with T_{AC}, while I_{ON}/I_{OFF} reduces when increasing T_{AC}.

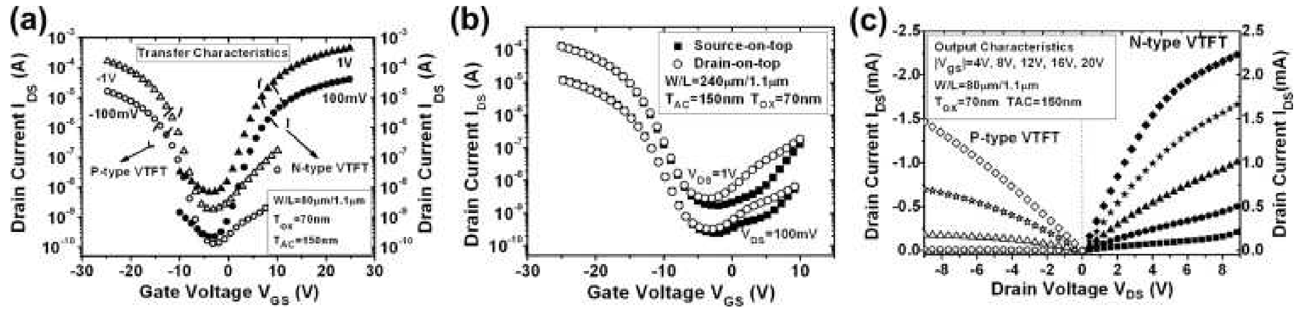

Figure 6: (a) Transfer characteristics of the P-type and N-type VTFTs, (b) transfer characteristics for source-on-top (SOT) and drain-on-top (DOT) structure, and (c) output characteristics of the P and N-type vertical TFTs. For the two types of VTFTs, the transfer characteristics are symmetric. Source and drain can be permuted. Output characteristics are affected by kink effect, which is due to the short channel length *L*.

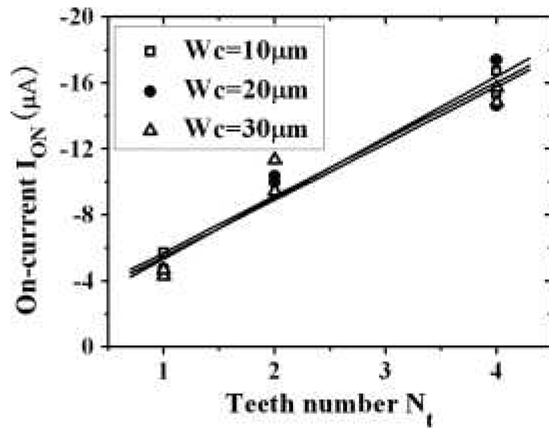

Figure 7: Variation of I_{ON} with the tooth number: I_{ON} is proportional to the tooth number, N_t.

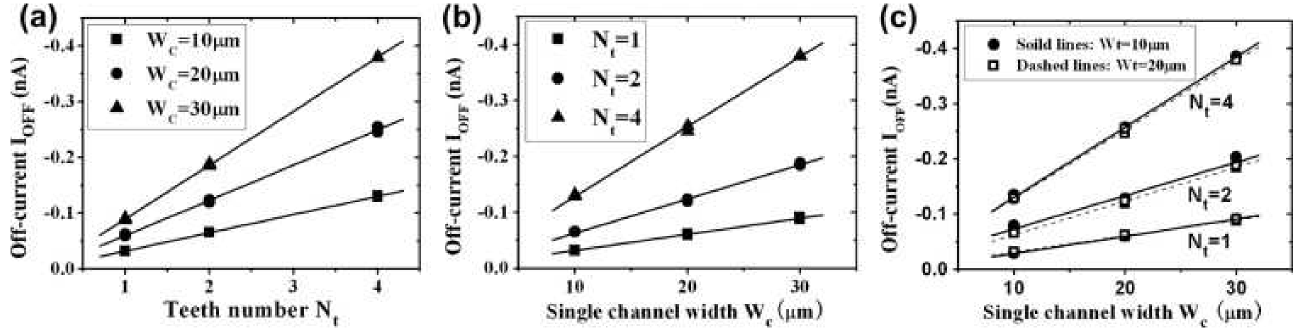

Figure 8: The relationships of I_{OFF} with different geometrical parameters: (a) I_{OFF} is proportional to the tooth number, N_t, (b) I_{OFF} is proportional to the single channel width, W_c, and (c) I_{OFF} is independent of the tooth width, W_t.

Active layer thickness (nm)	***S* (V/dec)**	**g_m (μS)**	**V_{TH} (V)**	**μ_{FE} (cm^2/V s)**	**I_{ON}/I_{OFF}**
225	1.3	1.2	3.9	13.2	1.74×10^5
150	1.3	1.0	4.4	11.5	1.98×10^5
100	1.2	0.8	5	9.2	2.11×10^5

Table 1: Electrical parameters of VTFTs with different active layer thicknesses T_{AC}. When increasing T_{AC}, threshold voltage V_{TH} reduces and field effect mobility μ_{FE} increases, while I_{ON}/I_{OFF} ratio reduces.

VTFT type	***S* (V/dec)**	**V_{TH} (V)**	**g_m (μS)**	**μ_{FE} (cm^2/V s)**
P-type	1.9	−15	1.5	4.2
N-type	1.9	9.8	2.7	7.5

Table 2: Electrical parameters of P-type and N-type VTFTs.