Behavior of the parameters of microcrystalline silicon TFTs under mechanical strain

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Abstract

N-type and P-type microcrystalline silicon top-gate TFTs, processed directly on PEN plastic substrate at maximum temperature of 180°C, were mechanically stressed.

These TFTs were bent by different curvature radii varying between infinite (flat) and 0.5 cm. The tensile stress increases the electron mobility and the compressive stress decreases it. The tensile stress decreases the threshold voltage of N-type TFTs while the compressive stress increases it. These trends are inversed if the type of stress changes OR the type of TFTs changes.

The total behavior under mechanical stress is exactly similar to that of single crystalline silicon MOSFETs in nano-scale technologies (90, 65, 45, 32 nm), where nano-scale stress is introduced in the goal to engineer the electrical parameters. The similarity originates from the microcrystalline silicon active layer that behaves like single crystalline silicon even if the stress effects are softened by the grain boundaries and the multiple crystalline orientations of the grains

Keywords: ***µc-Si TFT, PEN, Mechanical Stress***

1 Introduction

Several research studies are launched now to develop electronic devices on flexible substrate. The main targets of this electronics are the flexible displays, the intelligent textile, RFID tags and others. Some of these applications require the transparency of substrate. That's why the most used substrates are transparent plastics. However, most of transparent plastics cannot support a temperature higher than 120°C. The heat stabilised PEN (Polyethylene naphthalate) produced by DuPont Teijin Films can reach 180°C with 0.2% shrinkage during 30 minutes. Therefore, the maximum temperature that can be reached during the process is 180°C.

A number of methods and materials can be used to develop electronics on flexible substrates that cannot support a temperature highest than 180°C. One way is to fabricate the devices as usual on silicon wafers or on glass (large area electronics) and then transfer it on flexible substrate. Of course the performance of these devices is typical but the cost of the transfer will be prohibitive. The flexibility of such devices is also limited.

The other option is to fabricate the devices directly on the flexible substrate at the maximum temperature of 180°C. At such low temperature, the performance will be limited but the cost is low. So depending on the required performance and then on the targeted application, one of these two alternatives can be used. For example, electronics accompanying the sensors that sense human activities has not to work at very high frequency. In this case, direct fabrication of devices on flexible substrate can be developed.

When choosing this direct fabrication, different materials can be used. Organic materials are intensively used in many works in order to develop an organic electronics. Indeed, organic materials can hold a very low radius of curvature. However, a very long development is still needed to reach commercial electronic devices with needed reproducibility and reliability.

In this paper, N-type and P-type transistors based on inorganic materials are shown to hold a low radius of curvature without breaking. This result is interesting knowing the superior reproducibility and reliability of inorganic based devices.

Previously, we succeeded in depositing microcrystalline silicon (µc-Si:H) on glass at 165°C with sufficient electrical quality, leading to stable TFTs. [1-2]. This result was obtained thanks to the use of a mixture of silane, hydrogen and argon for the deposition [1-2] and of a very thin active layer [3-4]. The choice of µc-Si:H material is mainly due to being

more stable than most of similar materials deposited at low temperature [amorphous silicon,…]. It offers in addition the possibility to produce both N-type and P-type transistors [5-6] and therefore to develop CMOS devices.

Within this study, the optimized process of TFTs on glass is transferred on PEN substrate producing then N-type and P-type µc-Si TFTs on plastics. The success of the process led us to study the electrical behaviours of these TFTs under mechanical stress. These behaviours are explained tentatively using the numerous works on the strain on single crystalline silicon MOSFETs.

2 Experiment

2.1 Process

µc-Si:H Top-Gate TFTs are fabricated on 5 x 5 cm2 sheets of PEN (Polyethylene naphthalate). The thickness of the sheets of PEN is e = 125 µm. The sheet can reach 180°C with 0.2% shrinkage during 30 minutes. This feature limits the temperature of the process at 180°C.

The sheet of PEN is encapsulated on both sides with 250 nm thick silicon nitride. This layer protects the device from organic contamination during the process. A 100 nm thick layer undoped µc-Si:H is deposited in a PECVD reactor at 13.56 MHz using a gas mixture of silane, argon and hydrogen. Flows used for deposition are respectively 1.5, 75 and 75 sccm. The pressure is adjusted at 0.9 mbar and the RF power is fixed at 15 watts. The deposited film was optimized at 165°C [2]. After that, a layer 70 nm thick doped µc-Si:H is deposited in the same manner as the undoped µc-Si:H using a mixture of silane, hydrogen and doping gas. The doping gas is arsenic for N-type TFTs and diborane for P-type TFTs. A first photolithography step is used to define drain, source and channel regions. The µc-Si:H doped layer is etched by SF6 plasma in a Reactive Ion Etch (RIE) reactor to define source and drain regions. Then, a second photolithography step is necessary in the purpose to insulate transistors one from each other. The undoped µc-Si:H is etched by SF6 plasma. This step is followed by an RCA cleaning. After that, 300 nm thick silicon nitride film acting as gate insulator is deposited by PECVD at 150°C using mixture of silane, nitrogen and ammonia. The gas flows used for the Si3N4 deposition are respectively 2, 80 and 40 sccm. The pressure is adjusted at 0.6 mbar and the RF power is fixed at 30 watts. A third photolithography step is used to open windows for drain and source contacts. The silicon nitride film is etched by SF6 plasma. A layer of aluminum is deposited by thermal evaporation, and a fourth photolithography step is used to

define the drain, source and gate electrodes. Aluminum is etched by wet way. The final structure is presented in Fig. 1.

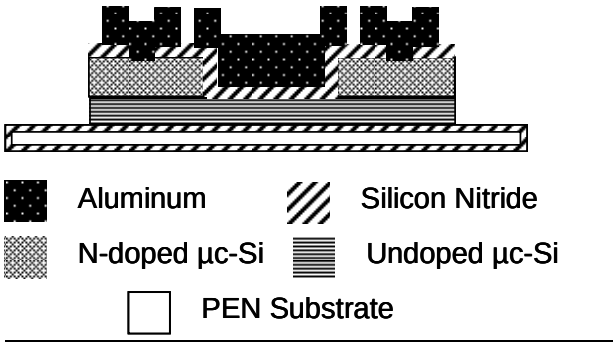

Fig. 1. Structure of µc-Si:H Top-Gate TFT.

Finally, an annealing at 180°C is performed under nitrogen. Note that the maximum temperature reached during the process is 165°C in order to avoid shrinking of the substrate between 2 photolithography steps. We maintain then the temperature of the process at much lower values than the needed maximum (180°C).

After processing, the TFTs are electrically characterized to extract the main parameters. The mobility value is deduced from the transconductance gm in the linear mode using the usual MOSFET equation. gm is the maximum slope of the linear plot of the transfer characteristics. The threshold voltage is determined in the linear mode by a linear extrapolation of the drain current versus gate voltage curve. The ratio Ion/Ioff is the maximum value of the ratio between the on-current and the off-current. The subthreshold swing S is the minimum reverse slope of the transfer characteristic (∂VGS/∂logIDS) measured in the switching region.

2.2 Mechanical behavior

The mechanical behaviors of the previous electrical parameters (mobility, threshold voltage, subthreshold swing) were studied by bending the flexible substrate at different radii of curvature. For this, the TFTs are electrically characterized under bending in the direction of their channel, using homemade tools (Fig. 2 and 3) allowing the bending of the substrate in tensile or compressive stress.

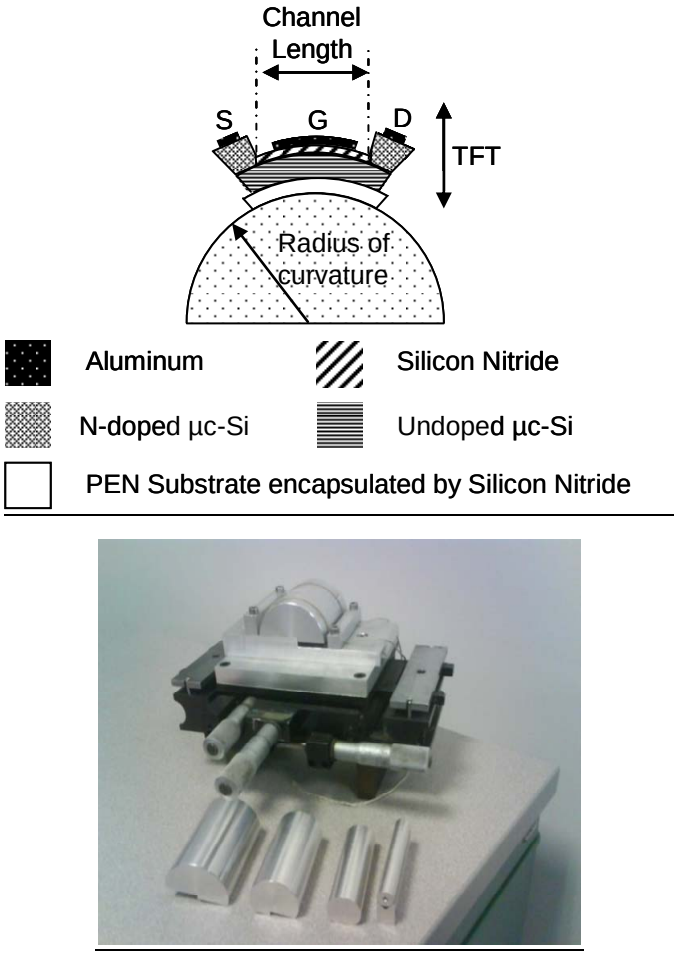

Fig. 2. Tool allowing the application of a tensile strain. The TFTs are bended outward and in parallel to the length L of the channel.

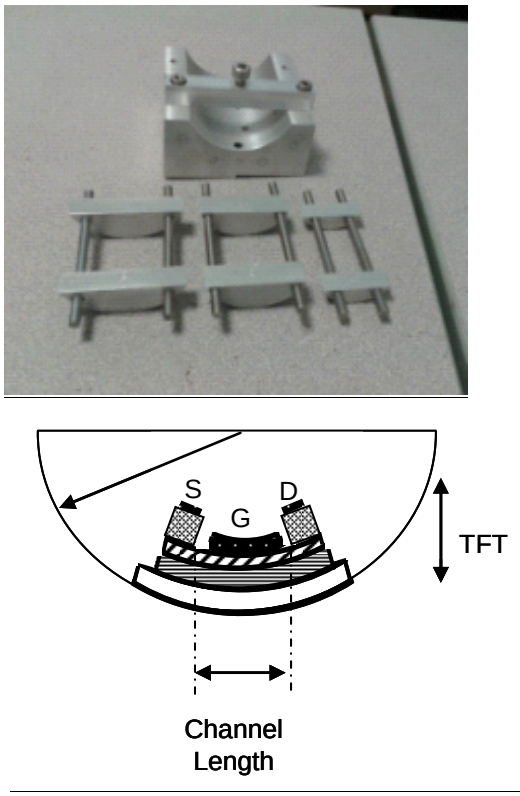

Fig.3. Tool allowing the application of a compressive strain. The TFTs are bended inward and in parallel to the length L of the channel.

To quantify the deformation of the channel induced by the bending, the multilayered structure of the TFTs was first simplified considering the different thicknesses and Young Modulus of the layers. The PEN sheet has a thickness of 125 µm and a Young Modulus of 6.45 GPa. It is covered by two 250nm thick silicon nitride layers on each face. The Young modulus of silicon nitride is 270 GPa. The structure of the TFT is located on the top layer of silicon nitride. It is constituted by a stack of the100 nm thick microcrystalline silicon layer with Y=160 GPa, the 300 nm thick silicon nitride layer used as gate insulator and the 300 nm thick aluminum layer with Y=70 GPa used as gate contact. The total thickness of silicon nitride on the top face of the PEN sheet is then 550nm. Considering this thickness and the high value of the Young modulus of silicon nitride, it can be assumed that the mechanical behavior of the stack of layers on the top face of the PEN sheet is mainly defined by the behavior of the 550nm thick silicon nitride. From the mechanical point of view, the total bended structure is considered constituted by 3 layers only, a 250 nm thick silicon nitride, the 125µm PEN sheet and a 550 nm thick silicon nitride (Fig. 4).

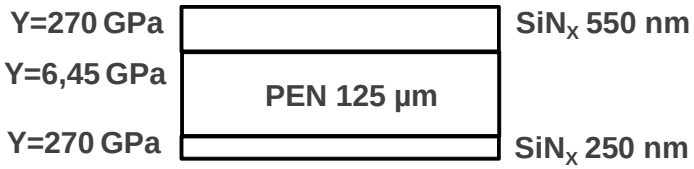

Fig. 4: Mechanical model of the total structure composed by the PEN sheet, the double silicon nitride film and the TFT.

Starting from this modeled structure, the strain $\varepsilon_{surface}$ created at the surface of the TFT by a bending at a radius of curvature R is calculated using the following equation [7]

$$\varepsilon_{surface} = \left(\frac{1}{R} \pm \frac{1}{R_0}\right) \frac{d_S + d_{f1} + d_{f2}}{2} \frac{\chi\left(\eta_1^2 + \eta_2^2\right) + 2\left(\chi\eta_1 + \chi\eta_1\eta_2 + \eta_2\right) + 1}{\chi\left(\eta_1 + \eta_2\right)^2 + \left(\eta_1 + \eta_2\right)\left(1 + \chi\right) + 1}$$

with: $\chi = \frac{Y_f}{Y_S}$; $\eta_1 = \frac{d_{f1}}{d_S}$; $\eta_2 = \frac{d_{f2}}{d_S}$.

Y_f and Y_s are the Young modulus of silicon nitride and of PEN respectively. d_{f1}, d_{f2} and d_s are the thicknesses of the bottom silicon nitride layer, of the top one and of the PEN sheet. R is the curvature radius and R_0 the initial curvature radius (infinite here in our case where we start from a flat sheet).

Fig. 5 shows the behavior of the strain $\varepsilon_{surface}$ as a function of the radius of curvature R when the stress is tensile or compressive. This curve will be used in the following to determine the behavior of the different parameters of the TFTs as a function of the strain.

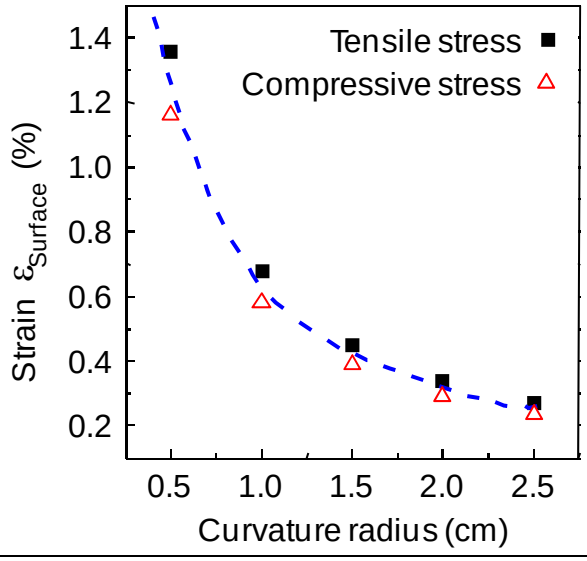

Fig.5: Evolution of the strain at the surface of the TFTs as a function of the radius of curvature of the substrate when the stress is tensile or compressive.

3. Results

3.1 Electrical Characterization

The TFTs are electrically characterized before starting the mechanical study. Fig. 6 shows the transfer characteristics of N-type and P-type TFTs in the linear regime (V_{DS}=+1V for N-type and -1V for P-type). Both TFTs have the same size with a channel width W= 100µm and a channel length L=20 µm. The characteristics are symmetric with the same absolute value of the threshold voltage VTH and the same Subthreshold swing S. The on-current of the N-type TFT is of course higher due to the higher value of the electron mobility than that of the hole mobility.

TABLE I summarizes the values of these parameters for both types of TFTs.

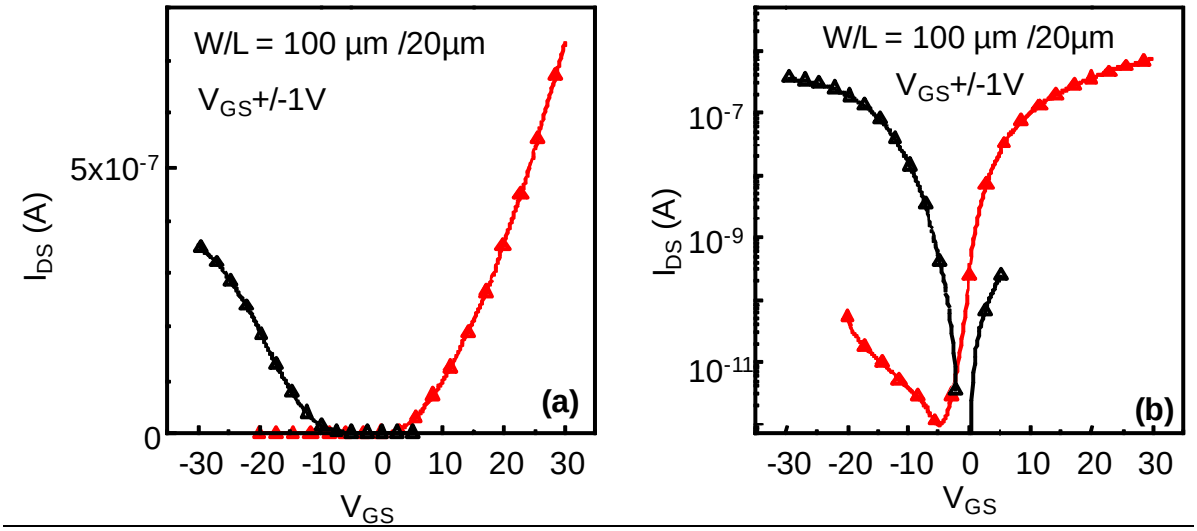

Fig 6. Transfer characteristics of N-type TFT (filled red triangle) and P-type TFT (open dark triangle) under a drain-source voltage of +1V (N-type) and -1V (P-type). The TFTs have the same size (W=100 µm, L=20µm). The characteristic is presented in linear scale (a) and in log scale (b).

	Mobility (cm^2/V.s)	Threshold voltage (V)	Subthreshold slope (V/dec)
N-type TFTs	0.43	11.5	1.3
P-type TFTs	0.24	-11.4	1.2

TABLE I: Parameters of the N-type TFTs and of the P-type TFTs fabricated on PEN

The low mobility value is usual when using silicon nitride as gate insulator in microcrystalline silicon TFTs even on glass substrate [3]. Despite this low mobility, TFTs are very stable under gate bias stress [3-4]. Finally and most importantly, the present TFTs show the possibility to fabricate symmetric N-type and P-type TFTs directly on a PEN sheet at a maximum temperature of 180°C. This temperature is reached only during the last annealing step. CMOS electronics fabricated directly on PEN is in way.

3.2 Mechanical Characterization

The demonstrated possibility of CMOS electronics fabricated directly on flexible PEN sheets needs its behavior to be checked under mechanical tensile stress and compressive stress.

3.2.1 N-type TFT

Differently sized N-type TFTs are submitted first to tensile stress induced by different radii of curvature. The behaviors of their threshold voltage and their mobility, through the ratio between their value at a curvature radius R and their initial value when the TFT is flat, are shown in Figs. 7 and 8. The figures show a decrease of the threshold voltage V_{TH} and an increase of the mobility µ when the tensile strain increases.

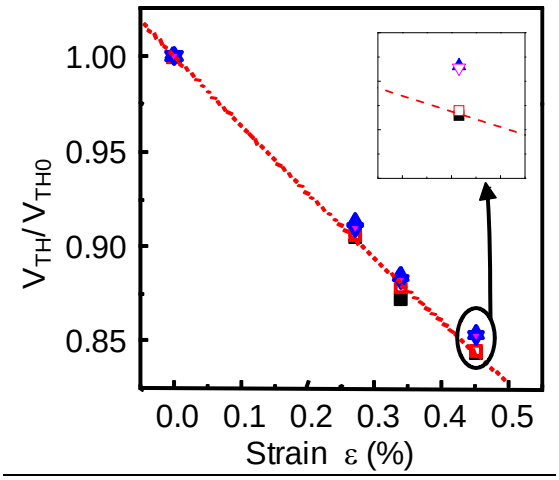

Fig.7 : Ratio between the threshold voltage at a tensile curvature radius R and its initial value when the TFT is flat for 4 different sizes (W/L=100µm/20µm: full squares, W/L=80µm/20µm: open squares, W/L=100µm/40µm: full triangles, W/L=80µm/40µm: open triangles) of N-type TFTs as a function of the strain.

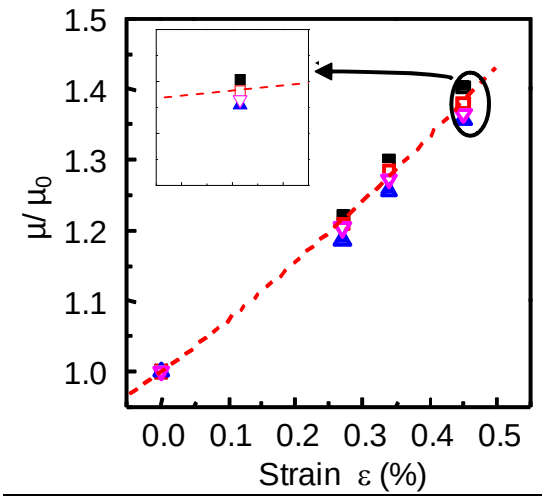

Fig.8: Ratio between the electron mobility at a tensile curvature radius R and its initial value when the TFT is flat for 4 different sizes (W/L=100µm/20µm: full squares, W/L=80µm/20µm: open squares, W/L=100µm/40µm: full triangles, W/L=80µm/40µm: open triangles) of N-type TFTs as a function of the strain.

Both, the decrease of the threshold voltage and the increase of the mobility appear to be independent of the size of the transistor. However, a deep analysis of the behavior (particularly for the highest strain shown by the insets in Figs. 7 and 8) shows that the threshold voltage and the mobility depend much more on the channel length than on its width. The variation becomes more important when the channel length decreases. This remark is not surprising if we consider that the tensile stress is applied in the direction of the channel length.

Similarly to this previous tensile stress, a compressive stress is applied to TFTs with the same size. The behaviors of their threshold voltage and of their mobility, through the ratio between their value at a curvature radius R and their initial value when the TFT is flat, are shown in Figs. 9 and 10. On the contrary of the effect of the tensile stress, these figures show an increase of the threshold voltage V_{TH} and a decrease of the mobility µ when the compressive strain increases.

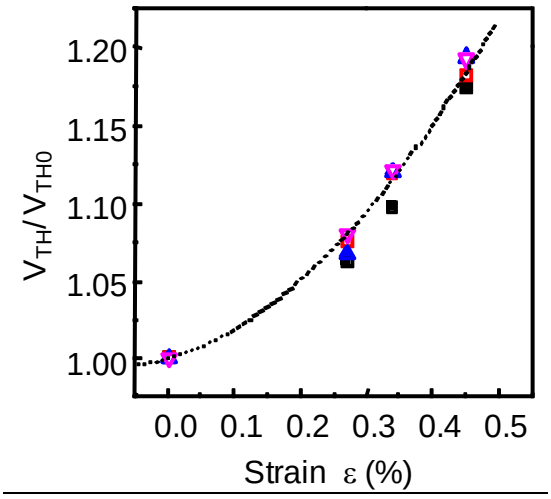

Fig.9: Ratio between the threshold voltage at a compressive curvature radius R and its initial value when the TFT is flat for 4 different sizes (W/L=100µm/20µm: full squares, W/L=80µm/20µm: open squares, W/L=100µm/40µm: full triangles, W/L=80µm/40µm: open triangles) of N-type TFTs as a function of the strain

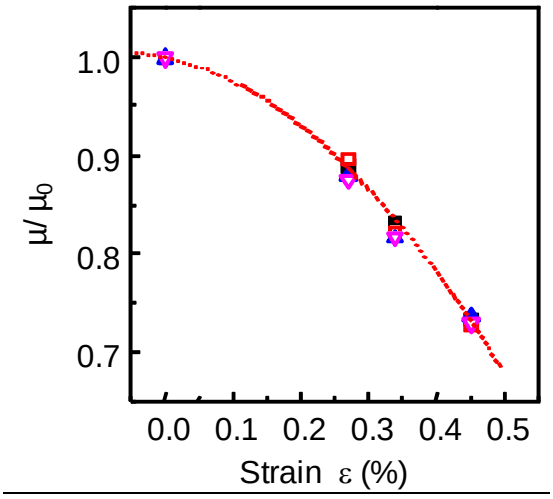

Fig.10: Ratio between the electron mobility at a compressive curvature radius R and its initial value when the TFT is flat for 4 different sizes (W/L=100µm/20µm: full squares, W/L=80µm/20µm: open squares, W/L=100µm/40µm: full triangles, W/L=80µm/40µm: open triangles) of N-type TFTs as a function of the strain

Here again, the variations of the threshold voltage and of the mobility are more important for transistors which have a shorter channel

3.2.2. P-type TFT

The previous study of the variation of the TFT parameters under mechanical stress is done now on P-type TFTs. P-type TFT with channel length 20 µm and channel width 100µm is submitted to tensile stress induced by different radii of curvature. The behaviors of its

threshold voltage and of its mobility, through the ratio between their value at a curvature radius R and their initial value when the TFT is flat, are shown in Figs. 11 and 12. The 2 figures show an increase of the threshold voltage V_{TH} and a decrease of the mobility μ when the tensile strain increases.

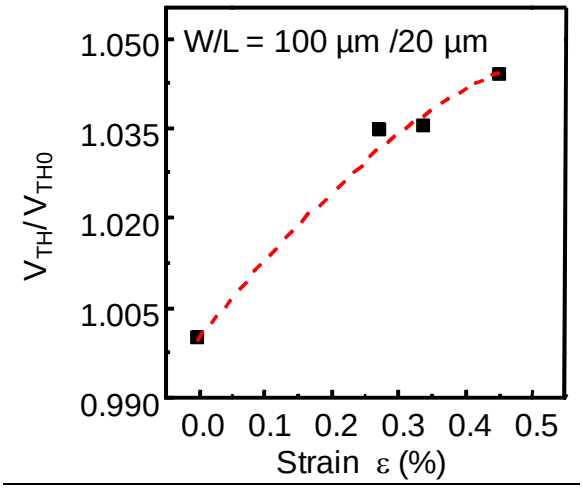

Fig.11: Ratio between the threshold voltage at a tensile curvature radius R and its initial value when the TFT is flat for W/L=100µm/20µm P-type TFT as a function of the strain.

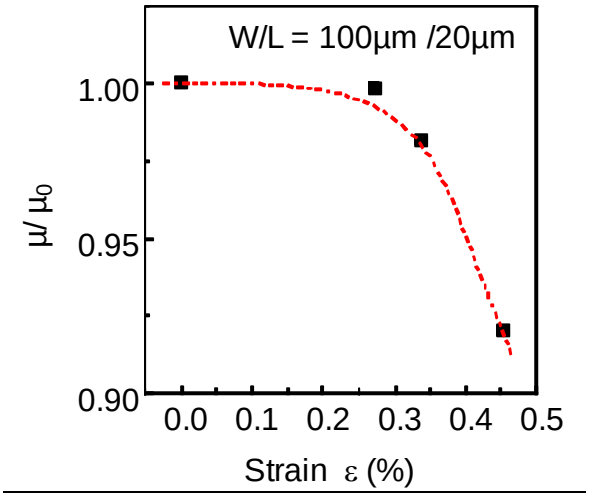

Fig.12: Ratio between the electron mobility at a tensile curvature radius R and its initial value when the TFT is flat for W/L=100µm/20µm P-type TFT as a function of the strain.

Under tensile stress, the behaviors of the threshold voltage and of the mobility show opposite trends for N-type and P-type TFTs..

Finally the same W/L=100µm/20µm P-type TFT is submitted to a compressive stress. The behaviors of its threshold voltage and of its mobility, through the ratio between their value at a curvature radius R and their initial value when the TFT is flat are shown in Figs. 13 and

14. On the contrary of the tensile stress, these figures show a decrease of the threshold voltage V_{TH} and an increase of the mobility μ when the compressive strain increases.

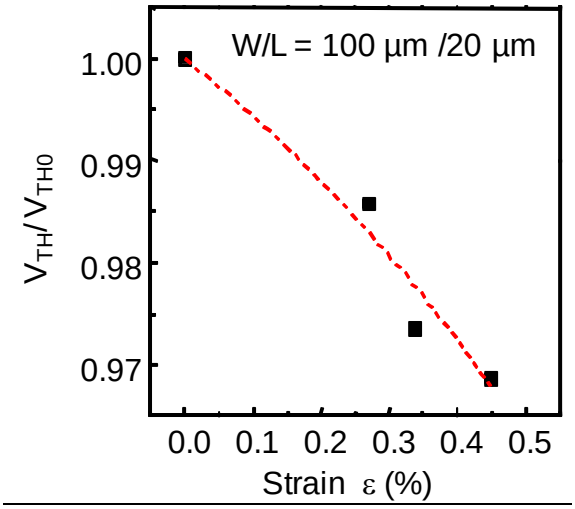

Fig.13: Ratio between the threshold voltage at a compressive curvature radius R and its initial value when the TFT is flat for W/L=100µm/20µm P-type TFT as a function of the strain

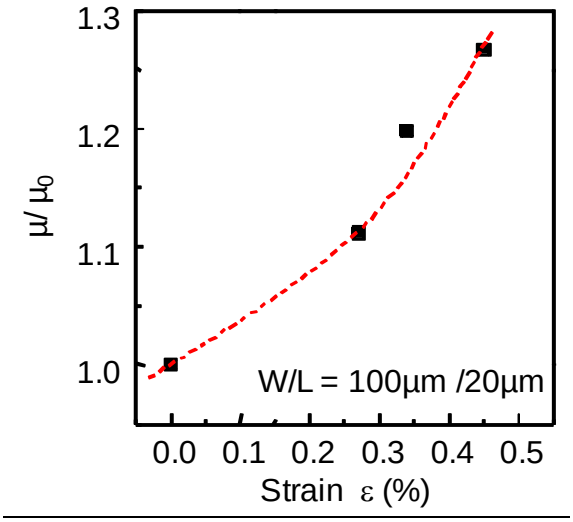

Fig.14: Ratio between the electron mobility at a compressive curvature radius R and its initial value when the TFT is flat for W/L=100µm/20µm P-type TFT as a function of the strain

4. Discussion

Before starting the discussion on previous mechanical behaviors, it is necessary to summarize the different trends of the threshold voltage and of the mobility in a table (TABLE II).

Stress	TFT	V_{TH} trend	μ trend
Tensile	N	Decrease	Increase
	P	Increase	Decrease
Compressive	N	Increase	Decrease
	P	Decrease	Increase

TABLE II: Trend of the threshold voltage and of the mobility μ for N-type and P-type microcrystalline silicon TFTs fabricated on PEN sheets under tensile and compressive stress.

The trends of both parameters change if the type of TFT changes OR the type of stress changes. To understand these trends, it may be useful to check first the literature on the mechanical behavior of silicon TFTs. Unfortunately there are very few works on silicon TFTs. Most of them are done on amorphous silicon based TFTs, mainly by the Princeton Group [7-9]. It is possible to find also some papers on the mechanical behavior of crystallized silicon TFTs mainly on LTPS TFTs fabricated on metal foils [10-12]. The electron mobility of a-Si:H TFTs was found to increase with tensile stress and to decrease with compressive stress. The electron mobility increases with tensile stress [10] and the hole mobility decreases under the same tensile stress [10, 11] for LTPS TFTs. These results are limited particularly when it comes to crystallized silicon TFTs. However, they are not inconsistent with our results.

On the other hand, a lot of complete studies on the mechanical behavior of single crystalline silicon MOSFETs are available. These intensive studies were done in nano-scale technologies (90, 65, 45, 32 nm) where nano-scale stress is introduced in the aim to increase the mobility of the electrons or of the holes. Some of the methods are given in a review [13]. These numerous works focus on the attribution of the increase of the mobility to the change in the energy bands due to the uniaxial stress, decreasing mainly the conductivity effective mass. For example, the threshold voltage decreases and the electron mobility increases for N-MOSFETs submitted to uniaxial tensile stress [13]. The decrease of the threshold voltage is attributed to a decrease of the energy band-gap and to the variation of the valence band density of states.

The same group [14] gives a 1.55 (μ/μ0) increase of the electron mobility under a tensile uniaxial strain of 0,0045% and under a vertical field of 0.7 MV/cm . The increase of the hole mobility is 3.8 (μ/μ0) under 0.005% compressive strain and under the same vertical field. In the present microcrystalline silicon TFTs, the increase of the mobility is 1.4 for electrons and 1.27 for holes, under the same order of vertical field but under a much higher tensile strain or a much higher compressive strain (0.45%).The need of a much higher strain to get the same increase of the mobility is probably due to the microcrystalline structure with grains boundaries that soften the effect of the stress and also to the different crystalline orientations of the grains even if the (220) orientation dominates.

Even if the magnitude of the mobility variations is lower with microcrystalline silicon TFTs, the most important is that the trends of the transistor parameters observed in the present study are exactly similar to that of the same parameters for MOSFETs. It may be then interesting to check what happens in microcrystalline silicon films under stress.

First, an undoped microcrystalline silicon film was deposited on a PEN sheet covered with silicon nitride, in the same conditions as for the active layer of TFTs. Its electrical conductivity was measured as a function of the tensile strain. The conductivity value increases with the strain with a little bit lower slope than that of the electron mobility of TFTs (Fig. 15). It means that the increase of the mobility of TFTs under tensile stress is due to a change in the electronic transport properties of the microcrystalline silicon active layer.

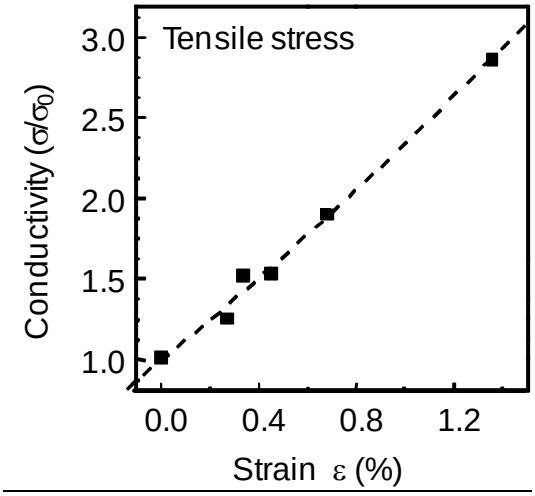

Fig. 15: Ratio between the electrical conductivity of an undoped microcrystalline silicon film deposited on PEN sheet covered with silicon nitride at a tensile curvature radius R and its initial value when the film is flat, as a function of the strain.

The second check concerns the behavior of the energy band gap of undoped microcrystalline silicon material. The UV-VIS-IR optical transmission of previous microcrystalline silicon film is measured when the film is submitted to tensile stress induced by different curvature radii. Fig. 16 gives the variation of the value of the light energy that gives a transmission value of 4% as a function of the strain. When the strain increases, this energy moves towards the low values, indicating a decrease of the energy band-gap of microcrystalline silicon. This is similar to what happens for threshold voltage of N-MOSFETs under tensile strain, the decrease of the threshold voltage of N-type TFTs under tensile strain can be attributed partially to a decrease of the band-gap of the microcrystalline silicon active layer.

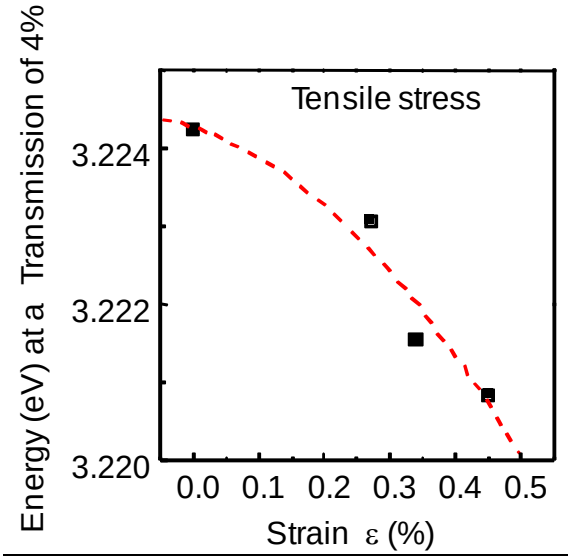

Fig. 16: Light energy at fixed low value (4%) of the transmission by undoped microcrystalline silicon film as a function of the strain

Finally, it can be interesting to check the effect of the strain on the crystalline grains of microcrystalline silicon when the stress is applied to the total structure that is constituted by crystalline grains and grain boundaries. This check can be done by using Raman spectroscopy. Indeed, amorphous and crystalline regions in the material contribute differently to the Raman spectrum. For example the transverse optic (TO) mode presents a band located at 480 cm-1 for amorphous silicon and at 520 cm-1 for single crystalline silicon. Moreover, another band located at 494–510 cm-1 is attributed to bond dilation at grain boundaries [15]. Fig. 17 gives an example of the TO band of microcrystalline silicon that is constituted by 3 sub-bands.

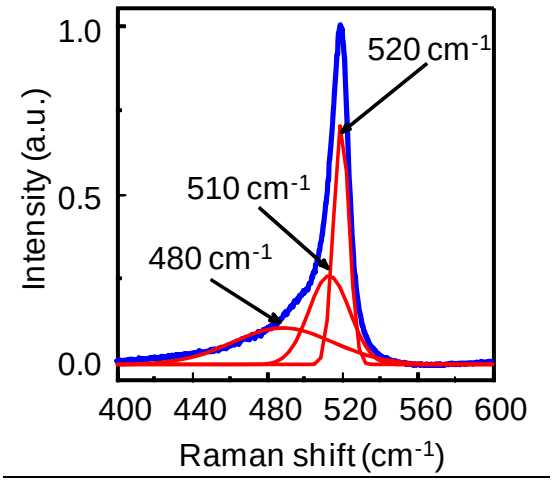

Fig: 17: Typical Raman transverse optic band of microcrystalline silicon

The Raman spectrum of previous microcrystalline silicon film submitted to different tensile stresses is measured at an excitation wavelength of 325nm. The position of the band attributed to single crystalline grains moves towards lower values of the Raman shift when the tensile strain increases (Fig. 18). The lower position of this band can be attributed to tensile strained crystalline grains as usual [16]. Here, this lower position of the band is not surprising as a macroscopic tensile stress is applied. However it means that the macroscopic stress affects directly the crystalline grain and then its electrical properties as for single crystalline silicon of MOSFETs.

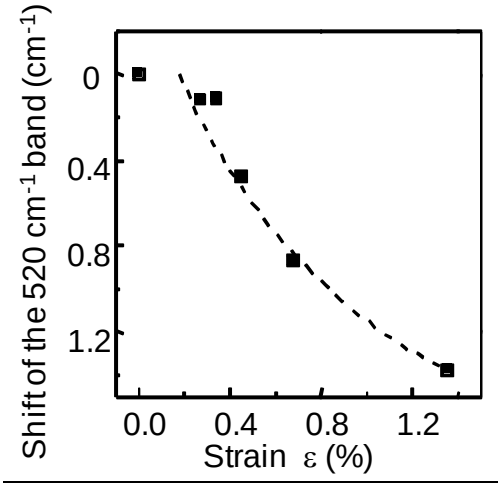

Fig. 18: Shift of the single crystalline silicon band of an undoped microcrystalline silicon film deposited on PEN sheet covered with silicon nitride as a function of the tensile strain.

All these previous experiments lead to attribute the different effects of the tensile and compressive stresses on the parameters of microcrystalline silicon TFTs to the same origins already given for single crystalline silicon MOSFETs. Only the magnitude of the effects is softened by the presence of disordered boundaries between the crystalline grains and by the different crystalline orientations of the grains.

5. Conclusion

N-type and P-type microcrystalline silicon TFTs were directly fabricated on PEN sheets at a maximum temperature of 180°C. For the first time, systematic study of the behavior of such TFTs under tensile and compressive stresses is presented here. The total behavior is exactly similar to that of single crystalline silicon MOSFETs in nano-scale technologies (90, 65, 45, 32 nm) where nano-scale stress is introduced in the aim to engineer the electrical parameters. Complementary studies show that this similarity is due to the microcrystalline silicon active layer that behaves like single crystalline silicon material even if the stress effects are softened by the grain boundaries and the multiple crystalline orientations of the grains.

This study shows also that microcrystalline silicon films can hold high strain at a level of 1.35% corresponding to a curvature radius of 5 mm. Flexible electronics based on silicon can be the future in many applications considering the present mechanical behavior and the known stability of microcrystalline silicon.

Acknnowlegments

This work was done in the frame work of the e-FlexSi project ANR -09-BLAN-0163 France.

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Figure Captions

Fig. 1. Structure of µc-Si:H Top-Gate TFT.

Fig. 2. Tool for tensile strain. TFTs are bended outward and in parallel to the channel L.

Fig.3. Tool for compressive strain. TFTs are bended inward and in parallel to the channel L.

Fig. 4: Mechanical model of the total structure composed by the PEN sheet, the double silicon nitride film and the TFT.

Fig.5: Evolution of the strain at the surface of the TFTs as a function of the curvature ratio of the substrate for tensile or compressive stress.

Fig 6. Transfer characteristics of N-type TFT (filled triangle) and P-type TFT (open triangle) under a drain-source voltage of +1V (N-type) and -1V (P-type). The TFTs have the same size (W=100 µm, L=20µm). The characteristic is presented in linear scale (a) and in log scale (b).

Fig.7 : Ratio between the threshold voltage at a tensile curvature radius R and its initial value when the TFT is flat for 4 different sizes (W/L=100µm/20µm: full squares, W/L=80µm/20µm: open squares, W/L=100µm/40µm: full triangles, W/L=80µm/40µm: open triangles) of N-type TFTs as a function of the strain.

Fig.8: Ratio between the electron mobility at a tensile curvature radius R and its initial value when the TFT is flat for 4 different sizes (W/L=100µm/20µm: full squares, W/L=80µm/20µm: open squares, W/L=100µm/40µm: full triangles, W/L=80µm/40µm: open triangles) of N-type TFTs as a function of the strain.

Fig.9: Ratio between the threshold voltage at a compressive curvature radius R and its initial value when the TFT is flat for 4 different sizes (W/L=100µm/20µm: full squares, W/L=80µm/20µm: open squares, W/L=100µm/40µm: full triangles, W/L=80µm/40µm: open triangles) of N-type TFTs as a function of the strain

Fig.10: Ratio between the electron mobility at a compressive curvature radius R and its initial value when the TFT is flat for 4 different sizes (W/L=100µm/20µm: full squares, W/L=80µm/20µm: open squares, W/L=100µm/40µm: full triangles, W/L=80µm/40µm: open triangles) of N-type TFTs as a function of the strain

Fig.11: Ratio between the threshold voltage at a tensile curvature radius R and its initial value when the TFT is flat for W/L=100µm/20µm P-type TFT as a function of the strain.

Fig.12: Ratio between the electron mobility at a tensile curvature radius R and its initial value when the TFT is flat for W/L=100µm/20µm P-type TFT as a function of the strain.

Fig.13: Ratio between the threshold voltage at a compressive curvature radius R and its initial value when the TFT is flat for W/L=100µm/20µm P-type TFT as a function of the strain

Fig.14: Ratio between the electron mobility at a compressive curvature radius R and its initial value when the TFT is flat for W/L=100µm/20µm P-type TFT as a function of the strain

Fig. 15: Ratio between the electrical conductivity of an undoped microcrystalline silicon film deposited on PEN sheet covered with silicon nitride at a tensile curvature radius R and its initial value when the film is flat as a function of the strain.

Fig. 16: Light energy at fixed low value (4%) of the transmission by undoped microcrystalline silicon film as a function of the strain

Fig: 17: Typical Raman transverse optic band of microcrystalline silicon

Fig. 18: Shift of the single crystalline silicon band of an undoped microcrystalline silicon film deposited on PEN sheet covered with silicon nitride as a function of the tensile strain.

Table Captions

TABLE I: Parameters of the N-type TFTs fabricated on PEN

TABLE II: Trend of the threshold voltage and the mobility μ for N-type and P-type microcrystalline silicon TFTs fabricated on PEN sheets under tensile and compressive stress.

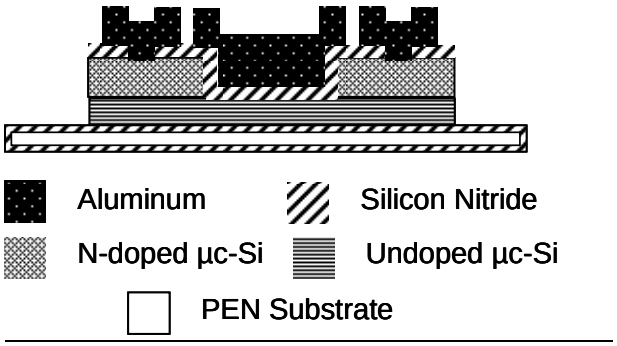
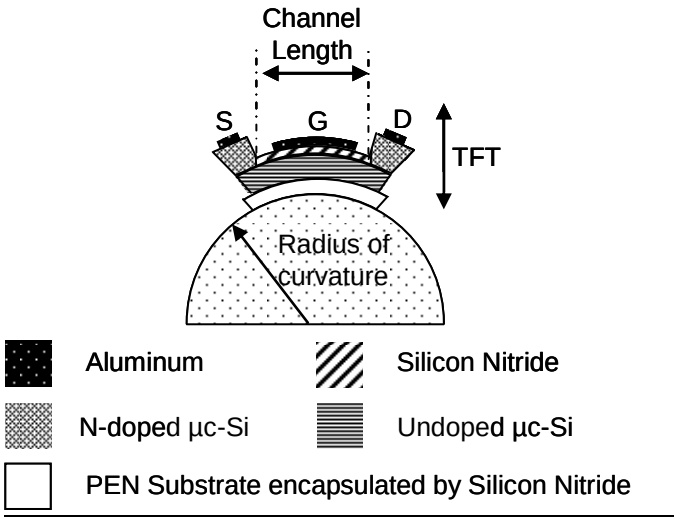

Aluminum
Silicon Nitride
N-doped µc-Si
Undoped µc-Si
PEN Substrate

Fig. 1


Channel
Length
S
G
D
TFT
Radius of
curvature
Aluminum
Silicon Nitride
N-doped µc-Si
Undoped µc-Si
PEN Substrate encapsulated by Silicon Nitride

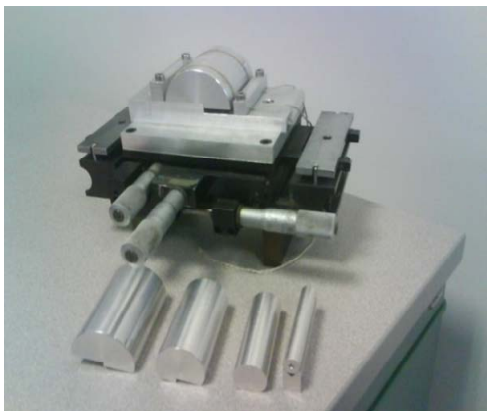
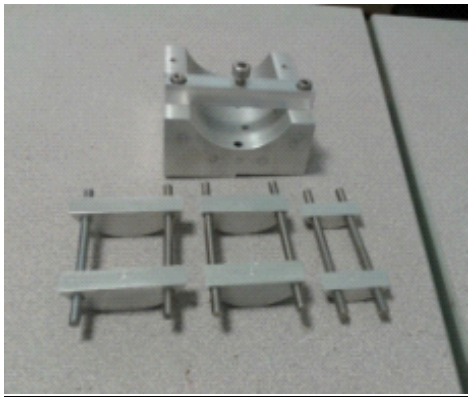


Fig. 2



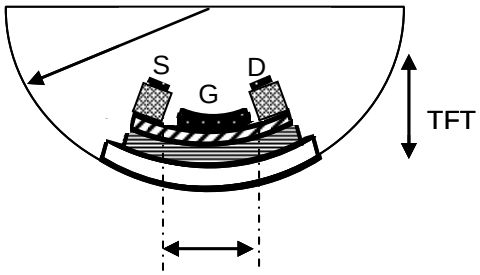


Fig.3

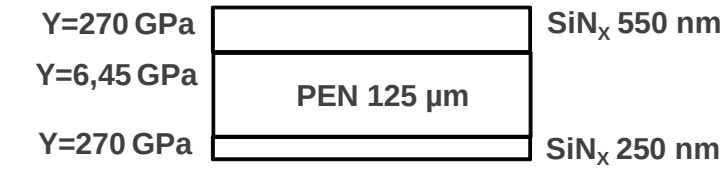


Fig.4

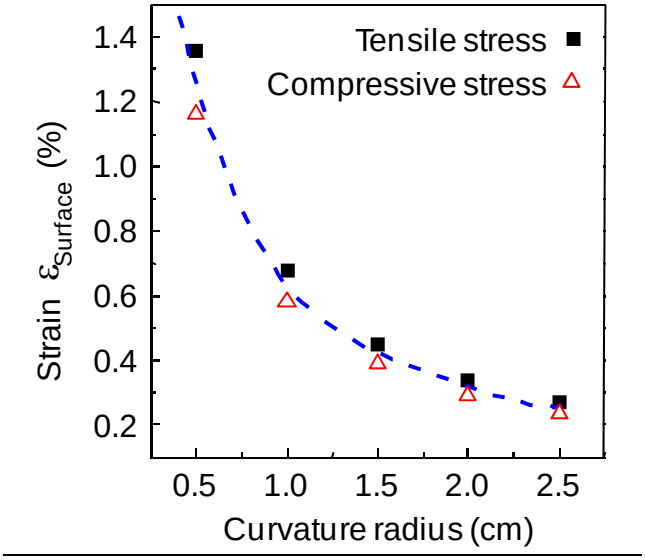

Tensile stress
Compressive stress
Strain $\varepsilon_{Surface}$ (%)
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.5
1.0
1.5
2.0
2.5
Curvature radius (cm)

Fig.5

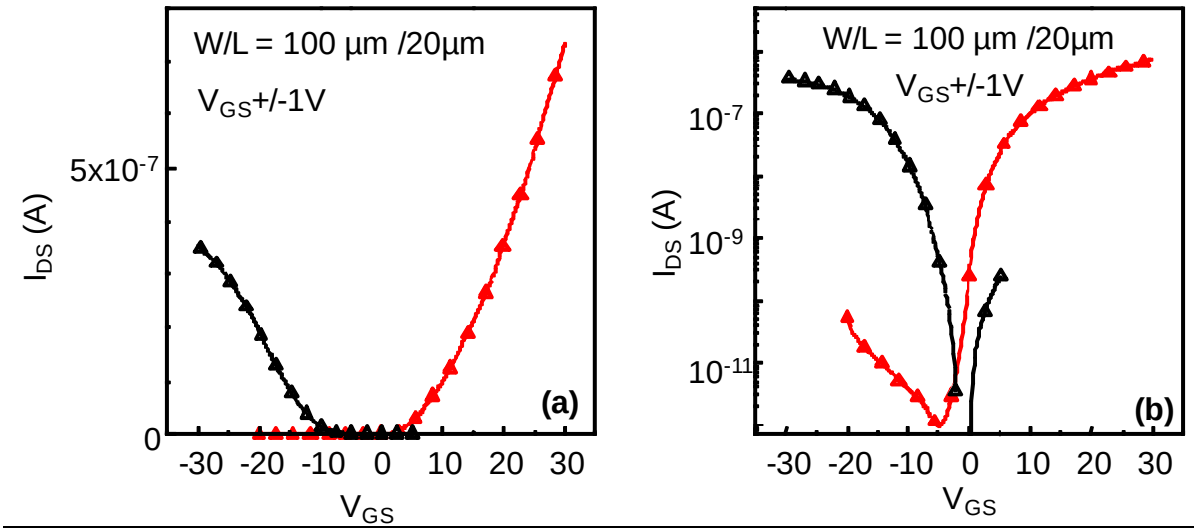

W/L = 100 µm /20µm
V_{GS}+/-1V
5x10^{-7}
0
I_{DS} (A)
-30 -20 -10 0 10 20 30
V_{GS}
(a)
W/L = 100 µm /20µm
V_{GS}+/-1V
10^{-7}
10^{-9}
10^{-11}
I_{DS} (A)
-30 -20 -10 0 10 20 30
V_{GS}
(b)

Fig.6

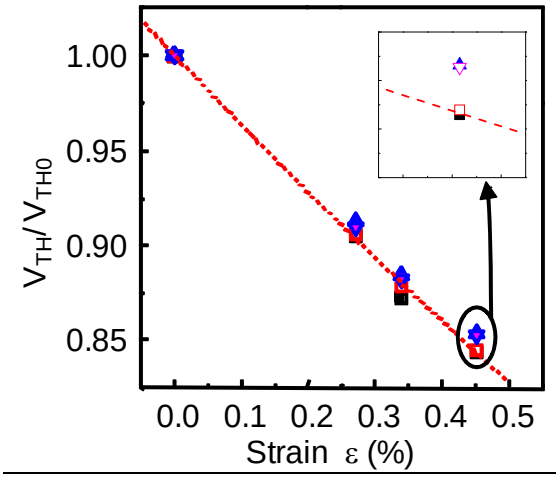


Fig.7

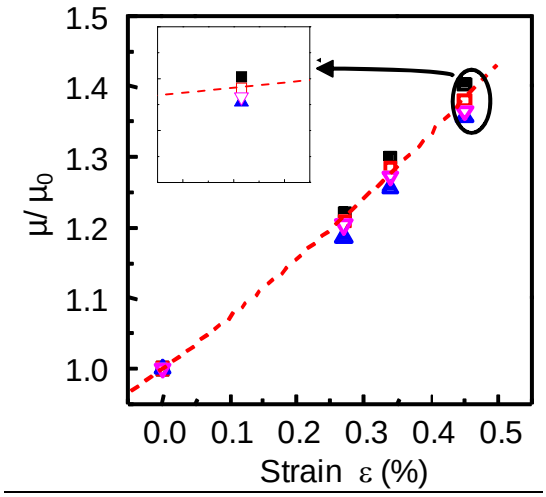


Fig.8

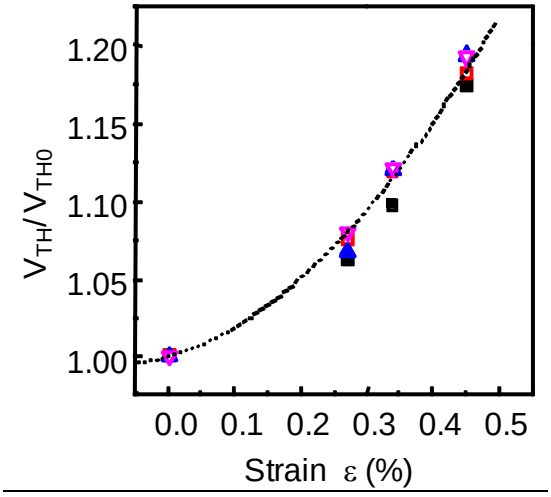


Fig.9

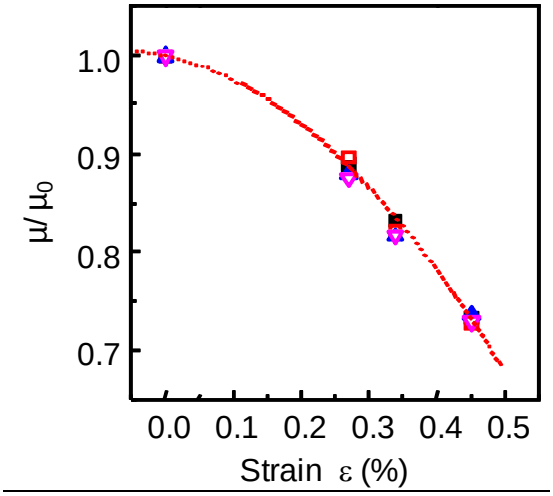


Fig.10

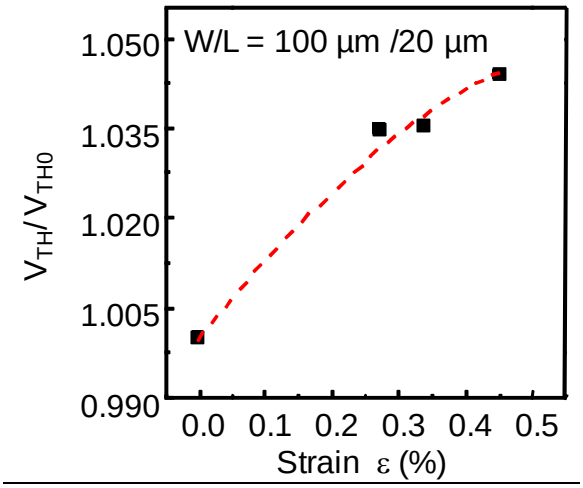

W/L = 100 µm /20 µm
1.050
1.035
1.020
1.005
0.990
V_{TH}/V_{TH0}
0.0
0.1
0.2
0.3
0.4
0.5
Strain ε (%)

Fig.11

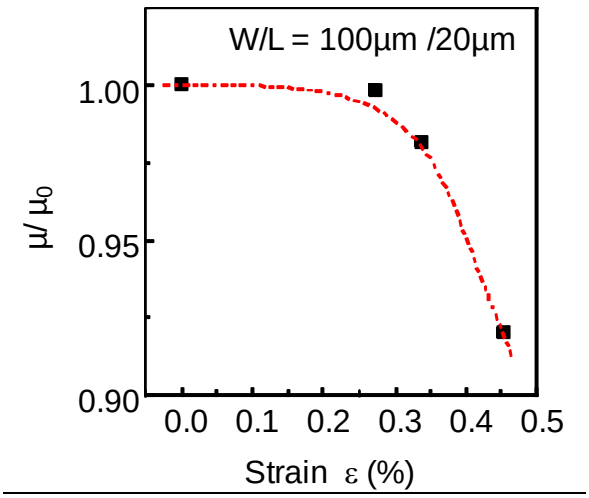


Fig.12

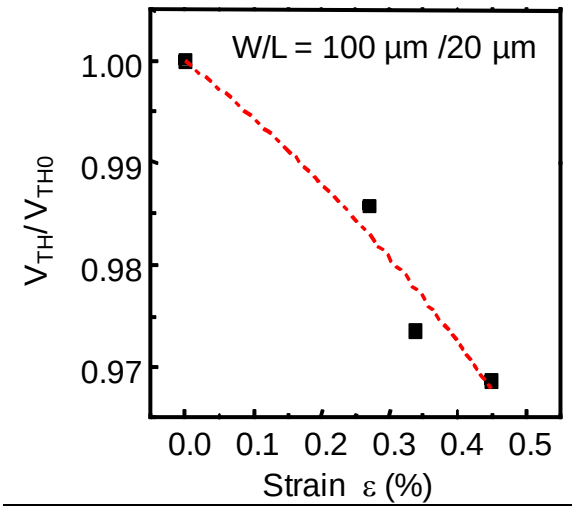


Fig.13

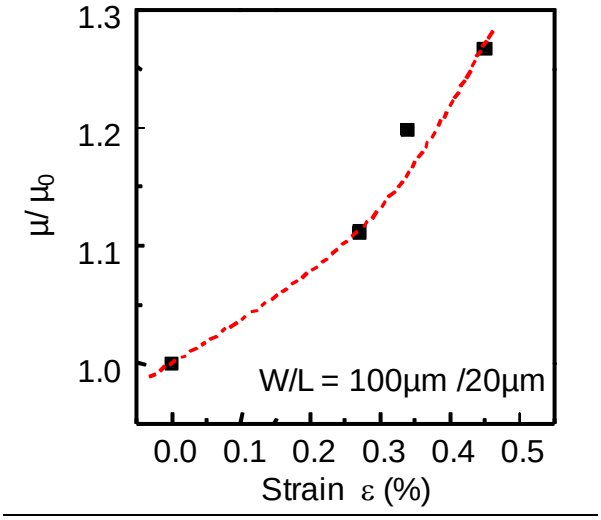


Fig.14

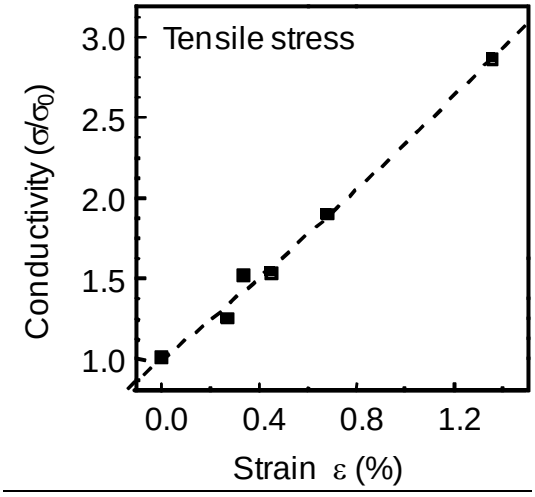

Tensile stress
Conductivity (σ/σ0)
3.0
2.5
2.0
1.5
1.0
0.0
0.4
0.8
1.2
Strain ε (%)

Fig.15

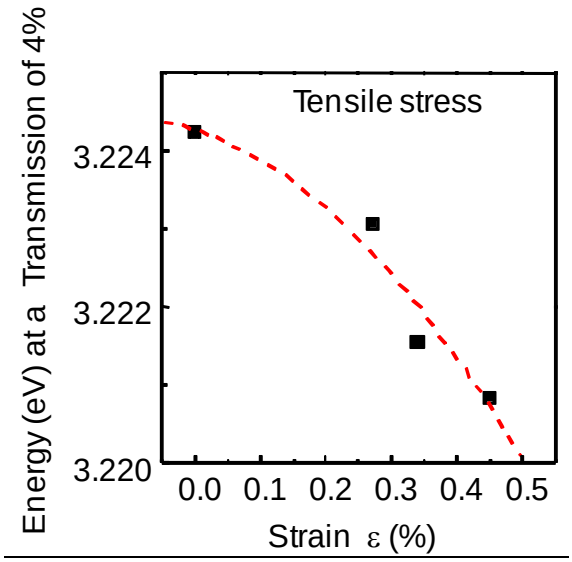

Energy (eV) at a Transmission of 4%
Tensile stress
3.224
3.222
3.220
0.0
0.1
0.2
0.3
0.4
0.5
Strain ε (%)

Fig.16

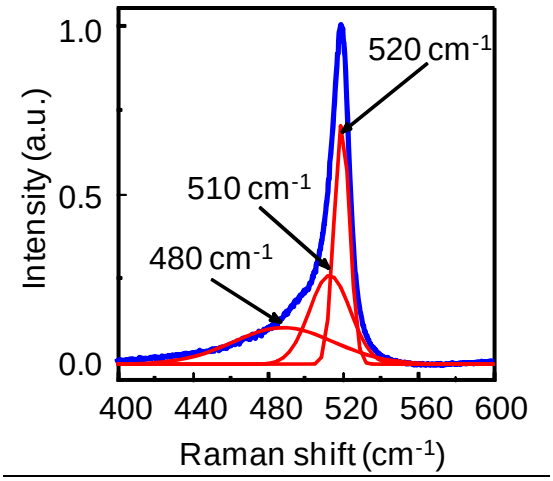

1.0
0.5
0.0
Intensity (a.u.)
520 cm-1
510 cm-1
480 cm-1
400 440 480 520 560 600
Raman shift (cm-1)

Fig.17

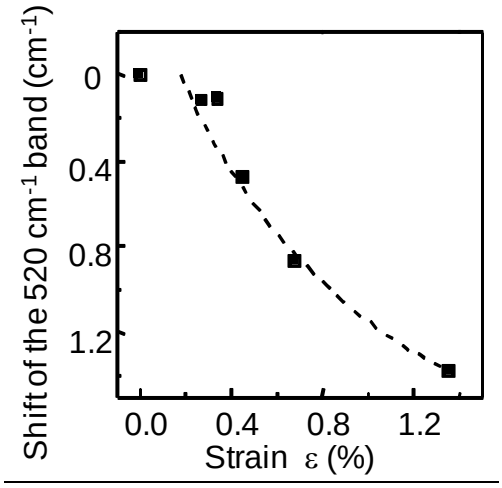


Fig.18