High efficiency low power rectifier design using zero bias schottky diodes

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***Abstract*—In this paper we present the design of high efficiency low power rectifier for microwave energy harvesting. The proposed circuit is based on a voltage booster formed by a voltage doubler type Latour structure. The circuit topology including parasitic elements and microstrip lines has been studied and optimized for high efficiency energy conversion dedicated to low input power operations (below -10dBm). Measurement results show 21% and 38% RF-DC conversion efficiencies for, respectively, -20dBm and -10dBm input power for 10KΩ resistor load at 850MHz. Experimental performances of the rectifier are in good agreement with the simulated ones.**

Keywords—Schottky, rectenna, energy harvesting

I. INTRODUCTION

The widespread diffusion of remotely powered devices has led to a growing interest in wireless energy harvesting techniques. This concept can be used to supply low power electronic devices like sensors or RFID tags over distances of several meters [1]. One approach of wireless power transmission uses the electromagnetic (EM) waves and energy transfer process can be described by three main stages. First, the power signal is generated and sent by an emitting antenna. Then, it is transported under the form of a free propogating EM wave towards the receiver where it is collected by the rectenna (rectifying antenna) to be transformed into a DC power. Rectenna efficiency optimization is still a hard task for RF designers when the incident power levels are very low [1][2].

Several rectification structures have been proposed to improve the RF-DC power conversion efficiency. In [3], [4], and [5] harmonic terminations, employed in RF power amplifier (PA) designs, have been used to improve the efficiency of a single stage shunt diode rectifier. However, optimized results are obtained only for input power beyond 0dBm. Other research works, [6][7][8], deal with the improvement of the DC output filter of the rectenna to boost the DC voltage and the conversion efficiency but they still not very efficient for low power detection. The conventional rectifying structures that have been widely studied, measured, and discussed are mainly single shunt and series mounted diode, voltage doubler and bridge rectifiers. In this work, we propose a voltage doubler structure type Latour, which to the author knowledge, has not been previously used in rectenna design. The paper is organised as follows: First, we review the different rectifying topologies. Then, we present the proposed circuit and its characteristics. In section III, we give the design guidelines and the simulated results. Finally, the measurement results are shown and discussed in section IV.

II. RECTENNA CONFIGURATIONS

A. Conventional rectifier structures

Rectifier circuits are built around diodes or diodes mounted transistors. In Fig. 1 we present three conventional rectifying structures the most used in litterature [8] [9]. The circuit is generally composed of 4 blocks: The input filter to preserve the antenna re-irradiating the high order harmonics generated by the rectifier, the input matching network (not presented in Fig. 1), the rectifying diode, and the output DC filter to filter harmonics in order to reduce voltage and current overlap. Diodes threshold voltage is a key factor when designing the rectenna. In fact, under high power levels, diode threshold is not important since it is very low compared to incident high frequency voltage amplitude. However, it becomes critical for low incident power levels due to losses. In this work, we use a zero bias shottky diode HSMS2852 with low threshold voltage of 150mV and a low junction capacitance C_{j0} of 0.18pF.

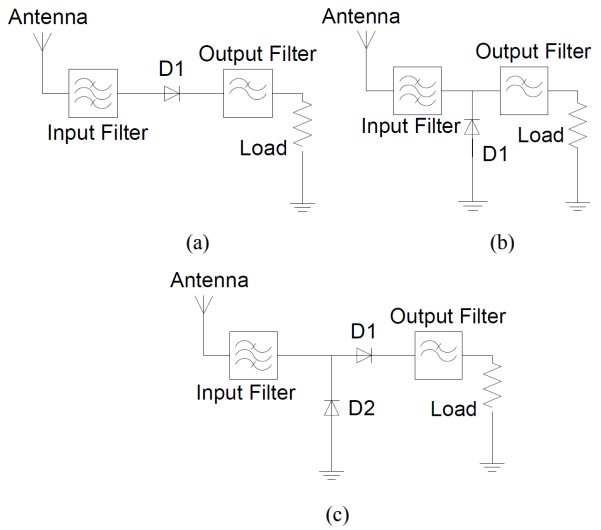


Fig. 1. Conventional rectenna topologies: (a) series; (b) shunt; (c) single stage voltage doubler

The main characteristics that should be optimized when designing rectennas are the DC output voltage V_{out} and the RF-DC power conversion efficiency defined as [10]:

$$\eta = \frac{P_{DCout}}{P_{RFin}} = \frac{V_{out}^{\ 2}}{R_L} \cdot \frac{4\pi . Z_{air}}{|E|^2 . G . \lambda^2} \quad (1)$$

Where R_L is the load resistance, Z_{air} is air characteristic impedance (120π ohms), E is electric field RMS value at receiver position, G is the receiving antenna gain, and λ is the wavelength.

RF designers should find a trade-off between a high output voltage and good power conversion efficiency when choosing the rectifier structure. A comparison between the performance of conventional rectifier topologies shown in Fig. 1, as a function of input power, has been widely discussed in several works. [10] used a Rectenna Figure of Merit (RFoM), described in (2), to compare the different rectifying topologies performances.

$$RFoM(P_{in}) = V_{DCopencircuit} . \eta_{optimalLoad} \quad (2)$$

It reported that series mounted diode rectifier seems to have the highest RFoM for low input power (below -5dBm) and offers a best compromise between DC output level and power conversion efficiency.

B. *The Proposed rectifier topology*

The rectifier topology we propose in this work is depicted in Fig. 2 (a). It is based on a voltage booster formed by a voltage doubler type « Latour ». The circuit includes two capacitors C_1 and C_2 and two rectifier diodes D_1 and D_2. The voltage source supplies two separate branches in parallel. A first branch is constituted by the series connection of the diode D_1 and the capacitor C_1, and the second branch is constituted by the diode D2 and the capacitor C_2 in series, one terminal of the capacitor C_1 being connected to one terminal of the capacitor C_2. One capacitor is charged at the positive half wave and the other at the negative half wave. The output voltage U_{out} is collected at the terminals of the circuit formed by the two capacitors C_1 and C_2.

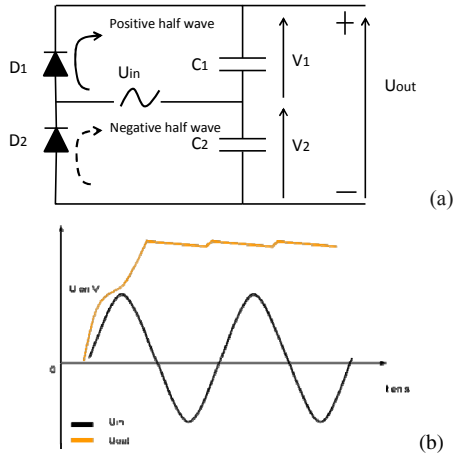


Fig. 2. (a) The proposed rectifier topology: "Latour" doubler; (b) the corresponding input and output waveforms

For open circuit case, the output voltage is twice the input peak voltage. The input and output waveforms of the circuit are illustrated in Fig. 2(b). This structure will be studied and optimized to design a high efficiency low power rectifier at 915MHz.

III. DESIGN GUIDELINES AND SIMULATION RESULTS

The global circuit optimization technique should take into account several factors such as passive components dimension including Q factor and tolerance, mircostrip lines added for matching and the non-linear behavior of the diode. These opimizations were made using the software ADS (Momentum EM simulations) from Agilent Technologies.

A. *Circuit Design*

The circuit architecture including passive components and microstrip lines is described in Fig. 3. An input inductance and a shunt capacitor of 3 pF have been added to improve the input matching. Special attention should be given to the choice of passive component in order to reduce the effect of dispersion on the sensitivity of the circuit. The input inductance has a value of 39nH and a Q factor of 35 at 800MHz. The output capacitors C_1 and C_2 are equals to 100pF. The proposed structure is designed on 1.6mm thickness FR4 substrate (εr=4.5 and tanδ=0.025).

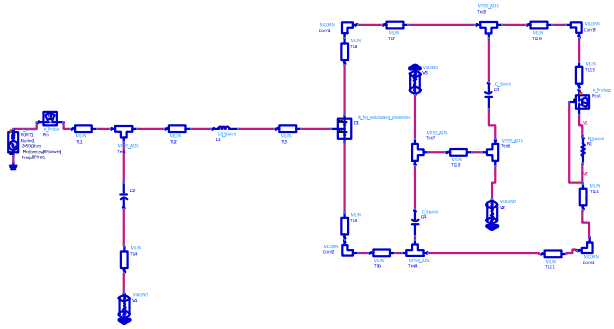


Fig. 3. Global circuit topology

B. *Simulation results*

The circuit has been simulated under Harmonic balance (HB) routine from Agilent ADS. S-paramter simulations have been caried out to optimize the matching network of the rectifier to a 50Ω input impedance at 915MHz (for input power below -10dBm). The simulated input return loss is illustrated in Fig. 4 and -19dB S11 is obtained at 915MHz.

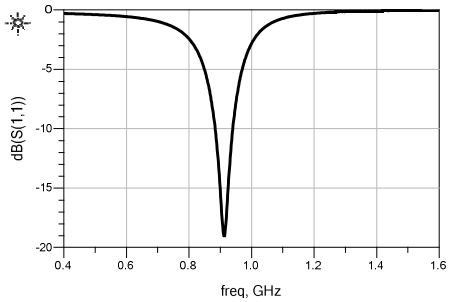
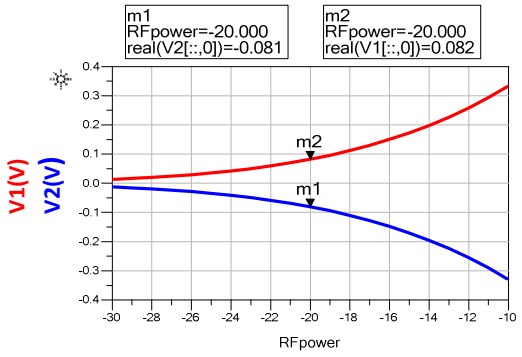
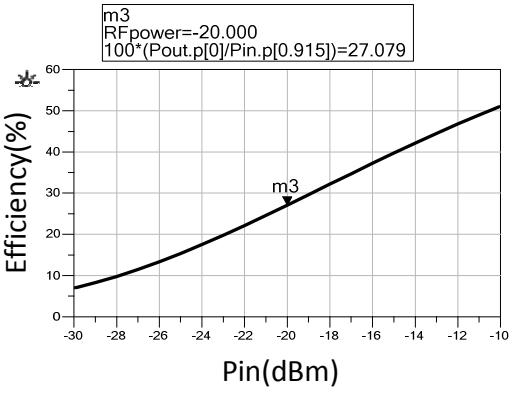


Fig. 4. Simulated S11

Harmonic balance sweep simulations have been carried out to determine the best compromise between high output DC voltage and high power conversion efficiency. Different load resistors have been tested to determine the optimal load. The output voltage achieved for a DC optimal load of 10KΩ for different input power and the corresponding RF-DC conversion efficiency are plotted respectively in Fig. 5(a) and (b) at 915MHz.



(a)



(b)

Fig. 5. (a) Output DC voltage; (b) RF-DC conversion efficiency

As can be seen, 0.163 V and 27% RF-DC conversion efficiency are obtained at -20dBm input power. At -10dBm almost 50% efficiency can be achieved.

IV. Rectifier Measurement Results

The rectifier has been designed and printed on a FR4 substrate. A photograph of the circuit is given in Fig. 6. The circuit occupies a total area of 5cm² which still very small in comparison with the area of rectifier structures using microstrip stub lines either in output or input filters [6] [9].

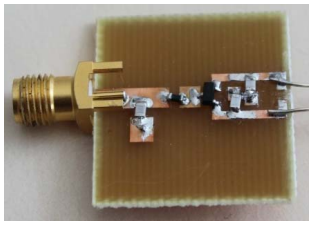


Fig. 6. Photograph of the rectifier

The measured input return loss S11 is shown in Fig. 7. The rectifier is slightly shifted but it is well matched with -13dB S11 at 850MHz for 10KΩ resistor load.

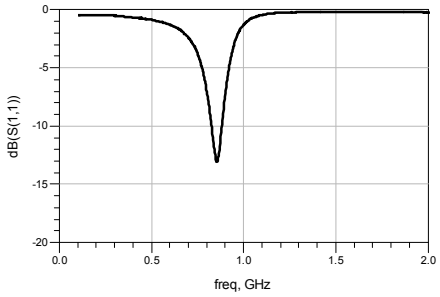


Fig. 7. Measured S11

The measurement setup, used to characterize the circuit, is described in Fig. 8. The directional coupler monitors the second harmonic power level. The power meter is used to measure the reflected power. The DC output voltage V_{out} is obtained by subtracting the voltage V_- from voltage V_+ .

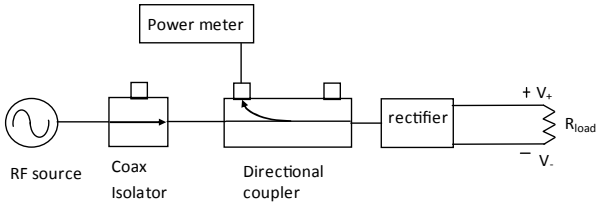


Fig. 8. Measurement setup of the rectifier

We measured the output DC voltage at three different input power levels (-20dBm, -15dBm, -10dBm) for 10 KΩ resistor load and we plotted it as a function of frequency in Fig. 9. Maximum DC voltages of 144mV and 610mV are obtained at 850MHz for -20dBm and -10dBm respectively. Good correlation with simulation results is observed at -20dBm and -15dBm input powers.

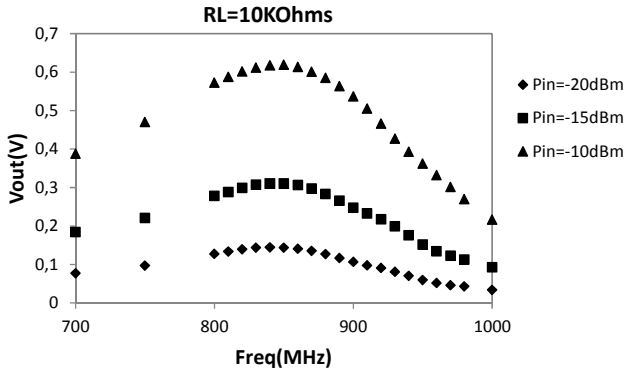


Fig. 9. Measured DC output voltage as a function of frequency

The power conversion efficiency has been computed according to (3) and plotted as a function of frequency in Fig. 10. A 21% maximum power conversion efficiency is measured at 850MHz for -20dBm input power and 10KΩ resistor load. The circuit performances are in good agreement with the predicted simulted results for input power below -15dBm. At -10dBm input power, measured power conversion

efficiency is reduced of 13% in comparison with the simulated one due to ohmic losses of the diodes.

$$\eta_{rec} = \frac{P_{outDC}}{P_{inc}} = \frac{V_{out}^2}{R_L * P_{inc}} \quad (3)$$

Where P_{inc} is the incident RF power, R_L is the DC load and V_{out} is the output DC voltage.

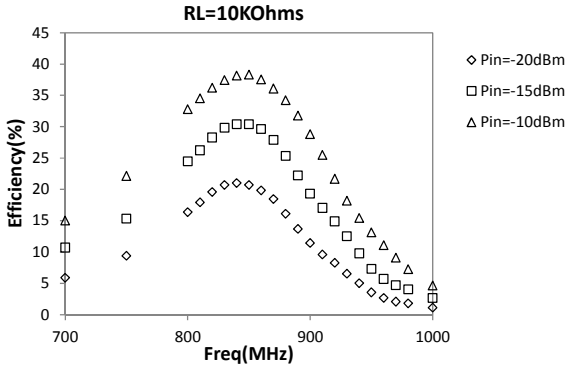


Fig. 10. Measured efficiency as a function of frequency

Measurement of the rectifier performances as a function of input power have been also carried out and plotted in Fig. 11 and Fig.12. 610mV and 1.17V DC output voltages are measured respectively at -10dBm and -5dBm input powers and 46% maximum RF-DC conversion efficiency is achieved at 0dBm input power.

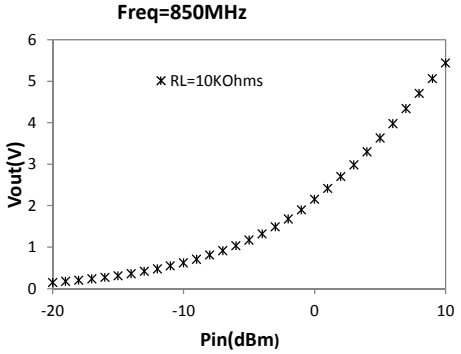


Fig. 11. Measured DC output voltage as a function of input power

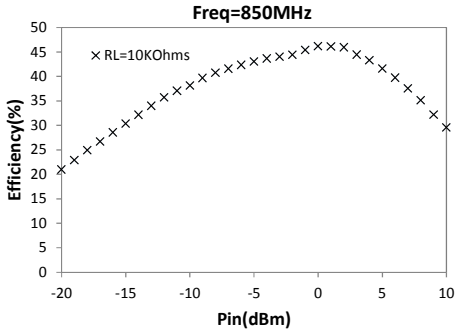


Fig. 12. Measured conversion efficiency as a function of input power

The proposed rectifier presents good performances for low power detection in comparison with the state of the art [10]. Most of the reported researches in rectifier designs operate at 2.4GHz. In [10], 300mV DC output voltage is obtained at 2.45GHz for -15dBm input power and 6KΩ resistor load.

V. CONCLUSION

A voltage doubler rectifier, type Latour, has been proposed and measured. The circuit is dedicated to low power detection applications at 850MHz. The experimental results validated the circuit high efficiency operation at low input power (below -10dBm). 21% RF-DC conversion efficiency is achieved at 850 MHz for -20dBm input power and 10KΩ resistor load. Future works involve the increase of the voltage doubler stages to boost the output DC voltage and improve the power conversion efficiency.

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