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Electrical properties of self-aligned gate-all-around polycrystalline silicon nanowires field effect transistors

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Abstract

Low temperature (≤ 600°C) polycrystalline silicon nanowires field effect transistors have been developed following a top down approach and classical photolithography techniques. N channel transistors have been tested with a single top-gate, bottom-gate and gate-all-around architecture in order to compare their electrical performances in relation to the interface state density. Analysis shows that surrounding gate enables control of parameters such as on-current, subthreshold slope and threshold voltage and offer potential further applications.

Keywords : gate-all-around, MOSFET, polycrystalline silicon, Si-nanowires, CMOS technology.

1. Introduction

As integrating smaller sized high performance electronic devices has become a key point over the past decades, innovative transistor designs have emerged. Chip-to-wafer density has to remain high to be competitive so size reduction is still a burning issue and non-planar devices are part of these brand new products. As a consequence, multigate field effect transistors (FET) have been developed [1]. Dual Gate (DG) [2], tri-gate [3], FinFET [4] and Gate-All-Around (GAA) FET [5-7] are the main structures, based on various materials, described in literature and available on the market. In such new gate architecture passing from 2D to 3D, silicon nanowires (SiNWs) FETs seem to be one of the most attractive choices. They enable to avoid problems due to short channel effect such as threshold voltage (V_{TH}) “roll-off” [8] or drain induced barrier lowering (DIBL) [9].

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More precisely, surrounding-gate transistors where the gate circles the nanowire channel allow a better electrostatic gate control. SiNWs can be prepared by a bottom-up method like layer by layer self-assembly [10], vapor-liquid-solid growth techniques [11], plasma-enhanced chemical vapor deposition (PECVD) [12] or using matrix template [13]. Nevertheless, the silicon nanowire growth process for device integration remains difficult as their size and positioning cannot always be perfectly controlled. In addition, SiNWs need to be selectively collected and handled in a planar layout. Most recent methods such as roll-to-roll technique enable SiNWs printing in order to obtain desired shapes and structures [14].

Top-down approach favors patterning architectures in a planar layout, most of the SiNWs are patterned on silicon-on-insulator substrates (SOI) by etching the first silicon layer down to buried oxide [15] because it provides best electrical performances for SiNW based FETs but the main drawback remains the high cost of these substrates. Several nano patterning techniques such as e-beam [16], atomic force microscopy [17] or deep-UV [18] were developed to achieve SiNWs. These high cost fabrication methods are not compatible with mass production. However, polycrystalline silicon SiNWs (poly-SiNWs) synthesis using sidewall spacer top down method [19-21] seems to be a lower cost alternative, fully compatible with planar complementary metal oxide semiconductor (CMOS) silicon technology.

Moreover, SiNWs FETs have nowadays attracted a lot of attention for the development of mechanical [22], biological [23] or chemical [24] sensors. In the latter two cases, SiNWs are used as sensitive units to detect charged chemical species, responsible for variation of the channel conductance. In particular, top-gate and back-gate transistors based on poly-SiNWs made by the spacer method showed to be good candidates to gas (ammonia) detection [25], pH sensing [26] and DNA hybridization [27].

GAA FETs are mainly known for enabling full channel depletion [6] so as to improve subthreshold slope (SS) and having low threshold voltage for identical subthreshold leakage current [28]. In addition, using double-gate devices proved interesting in relation to circuit drift compensation [29] because it allows dynamically fixing the threshold voltage as the second gate is able to control electrostatic effects (e.g. drift problems in organic light emitting diode (OLED) displays [30] or sensors [31]).

In this paper, we develop a low temperature (≤ 600°C) fabrication process of top-gate, bottom-gate and GAA FETs. SiNWs are made using the spacer method which is an original technique for GAA transistors fabrication. Independent biasing of each gate allows a possible threshold voltage control of these bottom gate (BGT) and top gate transistors (TGT). In addition, electrical connection of both bottom and top gate electrodes allows the formation of a gate that surrounds the channel, creating GAA architecture. Electrical performances are analyzed

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as a function of the density of state highlighting oxide/semiconducting nanowire interfaces difference in top and bottom gate configurations.

2. Experimental details

Poly-SiNWs FETs are fabricated using a 4 masks and a CMOS compatible fabrication process. N-type transistors with parallel poly-SiNWs channels are fabricated using the sidewall spacer method described below, where the spacer at nano scale made of poly-Si constitutes the nanowire. The key nanowire fabrication steps are illustrated in Fig. 1 (not to scale). Substrate is firstly covered with a 1.2 µm thick silicon dioxide (SiO_2) insulating layer deposited by Atmospheric Pressure Chemical Vapor Deposition (APCVD) technique at 420°C (not shown). Then, a 750nm thick highly N-type *in-situ* doped amorphous silicon (a-Si) layer is deposited by Low Pressure Chemical Vapor Deposition (LPCVD) technique at 550°C with a silane/phosphine mixture at 900 µbar and crystallized by thermal annealing under vacuum at 600°C. This layer is then patterned to form step used as bottom gate using classical UV photolithography and etched by reactive ion etching. A 70 nm thick SiO_2 gate insulator layer is then deposited by APCVD and densified by a thermal annealing at 600°C. Fig. 1(a) shows the obtained stepped bottom gate and the gate insulator layer. Then, a 750 nm thick LPCVD amorphous silicon layer, with two differently doped stacked regions is deposited and crystallized under the same conditions as bottom gate material. The 450 nm thick lower half layer is undoped and the 300 nm thick upper half layer is heavily N-type *in-situ* doped. This poly-Si layer is then patterned by plasma etching of this poly-Si layer to both create spacers (undoped) and source-drain electrodes (highly doped) of the transistor, as shown in Fig. 1(b). The channel length L is 5 µm and its widths (W_{TOP} and W_{BOT}) are 425 nm and 600 nm for top-gate and bottom-gate configurations respectively. In this case, using the spacer method to form SiNWs avoid using another photomasking step as it is not necessary to form source and drain regions. This technique enables self-alignment of gate. This key fabrication step enables formation of several nanowires and cost reduction of the process. Thanks to the 500 patterned steps in the bottom gate, 1.000 nanowires are formed to allow a high current level in the transistor.

A second 70 nm thick SiO_2 gate insulator is then deposited by the APCVD technique and densified. Then, a 300 nm thick N-type heavily *in-situ* doped silicon layer is deposited and crystallized. This layer is then etched to form the transistor's top-gate as shown in Fig. 1(c). Fig. 1(d) presents a schematic and a SEM image of a cross section of the whole device in its final version.

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Polycrystalline SiNWs used as channel region are common for top and bottom gates transistors. In addition, both gates can be electrically tied to form a single surrounding gate, called Gate-All-Around (GAA) transistors. Using spacer method to fabricate these transistors was not done before. Fig. 2 presents a SEM view of the device after this final stage of the fabrication process. Static electrical characteristics of the devices are collected at room temperature using an Agilent B1500A semiconductor parameter analyzer.

3. Results and Discussions

3.1. Electrical measurement of bottom and top-gate SiNWFETs

Fig. 3 presents the device performance of a single bottom or top-gate transistor. The plotted characteristics are all drawn from the same transistor based on 1.000 SiNWs by biasing either top or bottom gates of the device. The average width of SiNWs is 300 nm. The BGT and TGT show an N-type field effect transistor enhancement. TGT exhibits higher electrical performances: a higher I_{ON}/I_{OFF} ratio and SS, and a lower V_{TH} as previously reported [24]. These results are explained because quality of insulator/poly-SiNWs interface is better on the upper part of the nanowires than in the lower part. Indeed, for the BGT, channel region takes place in the seed layer of the poly-Si used to form nanowire with a higher defects density than the upper crystalline silicon nanowire surface. Thus, because the amorphous crystallization process begins at the SiO_2/a-Si interface, the defect density (including grain boundaries) is higher in the lower part of the poly-Si layer (a few nanometers thick) constituting the nanowires (see Fig. 4). These grain morphology and defect densities of Si-poly layers deposited in the same conditions were previously revealed by Haji et al [32] using transmission electron microscopy (TEM) analysis. These observations will be confirmed by electrical measurements of the interface state density in the section 3.2. Consequently, such defects lead to a poor electrode/channel interface quality because of the parasitic contact resistances. It could be due to the non-linear behavior of drain current at low source-drain voltages output characteristics for BGT compared to TGT (Fig. 5).

3.2. Electrical measurement of dual gate SiNWFETs

Fig. 6 presents the transfer characteristics of the TGT devices at different negative (a) and positive (b) bottom-

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gate voltages. Both measurements present N-type field-effect transistor enhancement with changes for off-state current values, threshold voltage and subthreshold slope. Values of V_{TH} and SS are summed up in Fig. 7. We note that for negative bottom-gate biasing, V_{GBot}, (Fig. 5(a)), V_{TH}, SS and on-current (I_{ON}) are quite similar, about 12.6 V, 4.0 V/decade and 1.4×10^{-4} A respectively, which indicates a good stability of the transistor for on-state mode. However off-current (I_{OFF}) is bottom-gate dependent and increases as negative V_{GBot} decreases. Indeed, in usual off state mode the inversion (holes) canal is responsible for the low leakage current through the reverse biased PN^+ junction at the drain. However, in our case, the negative bottom gate bias prevents the inversion (holes) top channel formation due to a likely drive back of electrons in the top region for negative bottom gate bias, which promotes electrical conduction in the core of the active layer resulting in an I_{OFF} increasing. In contrast, Fig. 6(b) highlights a dependency of SS parameter, V_{TH} and I_{OFF} for high V_{GBot} positive values (>10V). In this case, V_{TH} decreases (from 12.4 V to 3 V) and SS increases (from 3.3 V/dec to 8.7 V/dec) as V_{GBot} increases, resulting in a degradation of the on/off states switching of the TGT's transfer characteristics. For positive V_{GBot} values, the electric field may be high enough to attract electrons in the lower part of the nanowire. A channel is then formed in this region as V_{GTop} increases, responsible for a "parasitic" conduction at the back side of the SiNWs. Consequently, the TGT's apparent V_{TH} decreases as V_{GBot} increases. In the meantime, subthreshold slope increases with V_{GTop}. These hypotheses are confirmed by numerical calculation of carriers distribution within the poly-Si nanowires reported in the following section.

The numerical modeling of the dual-gate MOS structure (Top gate/Top oxide/Silicon Nanowires/Bottom oxide/Bottom gate) which is the basic vertical structure of the transistor (Fig. 8) is performed to highlight these effects of the voltage gates and of defects through the response of carrier concentration in the channel. This modelling solves the Poisson equation in order to calculate the electrostatic potential variation induced by an applied voltage. The finite element method is used to solve the Poisson equation in an iterative scheme in order to calculate the electrostatic potential, calculated at all the mesh points.

Our calculation illustrates tendencies of the conduction behaviors at $V_{TH} = 0$ V. The polycrystalline silicon is formed by crystallites composed of grains (considered as single crystal silicon), separated by grain boundaries, highly disordered and very narrow areas, of the order of several nanometers thick. This separation between two grains is considered as an amorphous silicon layer, and we use a model distribution of traps [34], taking into account the dangling bonds, tails bands and discrete traps. The mesh is very tight near the grain boundaries because of strong potential variations near grain boundaries. Moreover, modelling takes into account all the physical parameters characterizing the structure: thickness of the various layers, permittivity, work output,

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silicon doping. Results are reported in Fig. 9. From these simulation's results, one can suggest that at positive constant top-gate biasing, as long as bottom-gate biasing remains at negative or low positive values, the lower part of the nanowire is depleted. When a high positive value is reached, simulation results highlight an increase of the electrons concentration in the lower part of the nanowires, suggesting the formation of electron channel conduction in its lower part. In this case, one can consider that conduction in the lower part of the nanowire is not negligible anymore. Similarly, Fig. 9(b) points out that high negative bias values generate a channel of holes in the lower part of the poly-SiNW.

Our measurements show a relative stability of the transistor for $V_{GBot} < 10$ V. For higher V_{GBOT} values the TGT's threshold voltage can be modulated (Fig. 7). This V_{TH} control can offer many potential applications for circuit drift compensation such as OLED displays or sensors. The counterpart of this dual-gate poly-SiNWs FET main advantage is degradation of SS parameters and I_{ON}/I_{OFF} ratio. Nevertheless, for a drift compensation for the previously mentioned applications, high electrical performances in terms of high subthreshold switching are not necessarily desired.

3.3. Electrical measurement of GAA SiNWFET

Fig. 10 presents poly-SiNWs GAA FET electrical performances. Transfer characteristic at $V_{DS} = 3$ V (Fig. 10(a)) shows an N-type enhancement and main electrical parameters are $V_{TH} = 13.4$ V, SS = 2.3 V/dec and on-state current value similar to previous gate bias configuration of the device. We note that no rectifying behavior in the linear mode is observed as for BGT working mode (Fig. 10(b)). This means that bottom channel conduction does not dominate when bias is applied on the surrounding gate. The I_{ON}/I_{OFF} ratio is significantly higher than TGT's which may be due to a likely full depletion of charge carriers in the core of the poly-SiNWs in the GAA working mode (for $4V < V_G < 7V$). The surrounding gate improves TGT's performances in terms of switching ratio.

3.4. Density of states calculation

As mentioned previously, electrical properties of TGT, BGT and GAA transistor are strongly dependent on the interface and active layer qualities. In this way, we calculated density of states (DOS) in the poly- SiNWs based

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TGT and BGT. Such evaluations give information about quality of the material at the upper and the lower parts of the nanowires. As poly-Si is the active material, DOS estimation was done using the field-effect based Suzuki's incremental method [34]. Fig. 11 shows DOS values for these two transistors architectures. One can notice that BGT has a higher DOS than TGT. In particular, DOS is significantly higher (more than one decade) for high levels into the bandgap (related to tail states). One can consider that DOS is closely linked to oxide/polycrystalline silicon interface state because the conduction channel is mainly formed at this interface, in first few nanometers of the nanowire. It confirms the lower interface quality at the bottom part of SiNWs compared to its upper part. In other words, the upper part of the nanowires is better quality than lower part, which was supposed in a previous study [35]. In addition, these results confirm that in the GAA configuration, channel could be formed preferably in the upper region of SiNWs and leading to similar electrical characteristics for TGT configuration.

4. Conclusion

Polycrystalline silicon nanowire based field effect transistor has been fabricated by low-cost classical CMOS techniques. This transistor enabled top-gate, bottom-gate, dual-gate or gate-all-around configurations testing. The threshold voltage and subthreshold slope of top-gate transistor showed stability whereas the bottom-gate one was unsettled by contact resistances. In dual-gate configuration, properties show electrical stability for low positive bottom-gate biasing. Positive bottom-gate biasing induces formation of a bottom channel as defects participate to electrical conduction under some conditions which has been confirmed by simulation results. These transistors require very high operating voltages due to poor interface and crystalline quality of the material. Density of states calculations seem to confirm this hypothesis. Such a study can be a method to analyse nanowires based devices. Nevertheless, low operating voltage is not a key requirement for sensing applications. Further study on crystallization process of the polycrystalline silicon nanowire to reduce the crystal defect density could offer potential applications for low voltages electronic functions based on such transistors. In dual-gate mode, transistor enables a V_{TH} control thanks to the bottom-gate. Such a control can find application for sensors and OLED displays drift compensation. Gate-all-around architecture present characteristics related to top-gate configuration with better switching properties. In addition, as reported in previous works, poly-SiNWs based devices can be used for species detection, therefore the feasibility of such GAA structures and the

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potential effects of charged species on the SiNWs conductance in this configuration could benefit for the fabrication of high performance biochemical sensors.

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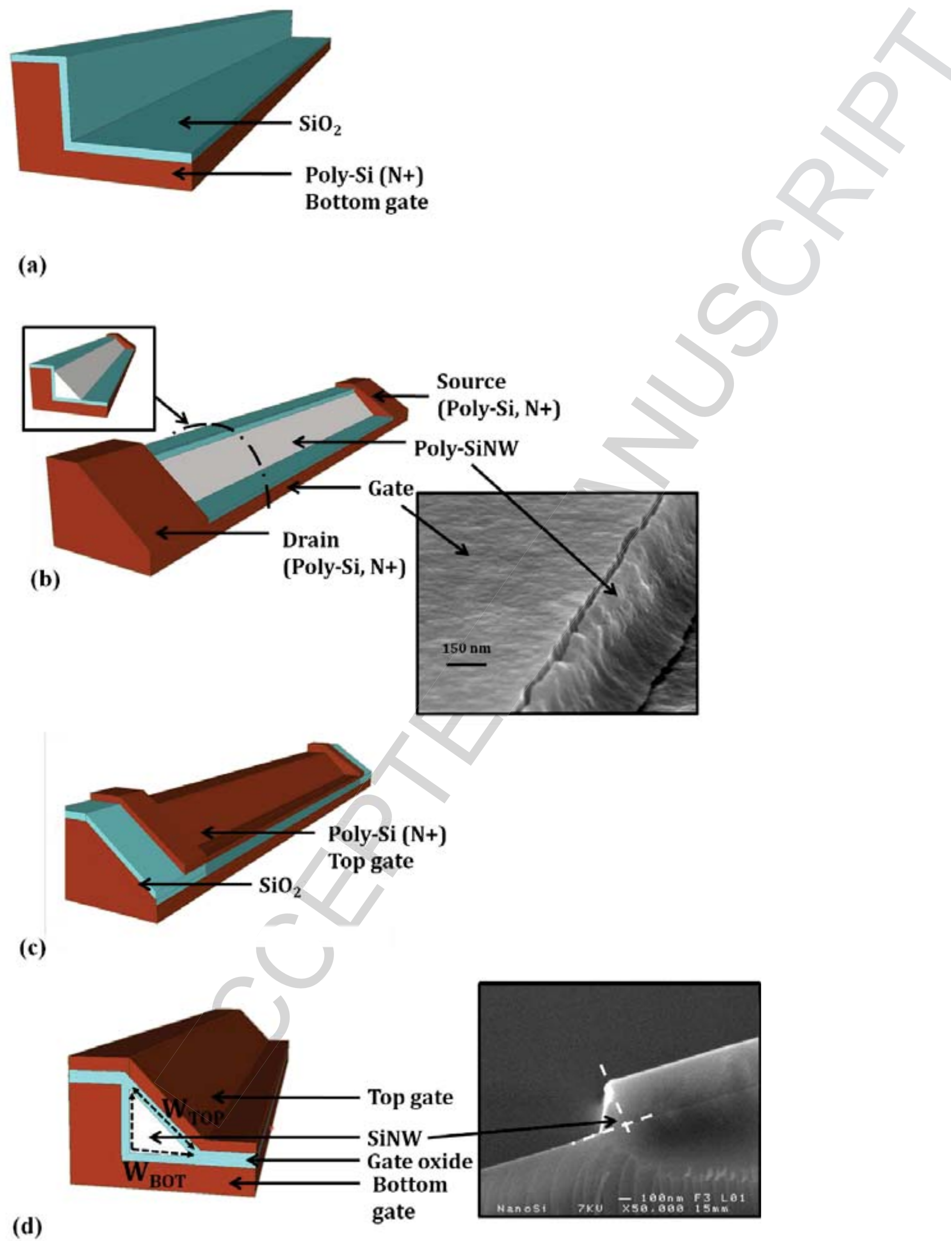

Fig. 1. Gate-All-Around Field-Effect Transistor fabrication steps: (a) stepped bottom-gate patterning and bottom oxide layer deposition, (b) polycrystalline silicon nanowire channel and drain-source zone formation and SEM image, (c) top-gate formation and (d) cross section of the final device with main dimensions : L = 5 µm, W_{TOP} = 420 nm, W_{BOT} = 600 nm per nanowire and SEM cross-section view of a silicon nanowire.

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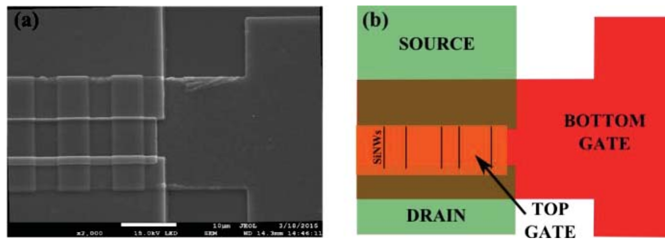

Fig. 2. (a) SEM imaging of the device with drain-source zone, multiple parallel polycrystalline silicon nanowires channels, bottom-and top-gate main regions and (b) schematic detailed view of this SEM image.

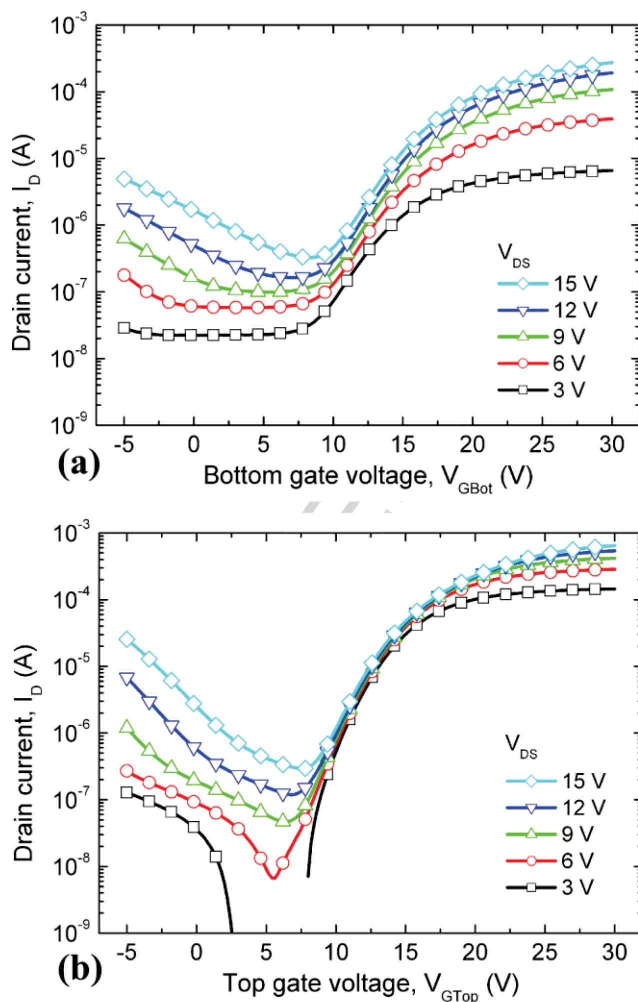

Fig. 3. Transfer characteristics of poly-Si NWFET I_{DS}–V_{GS}: (a) bottom-gate and (b) top-gate transistors (1000 nanowires, L=5 µm), showing an N-type enhancement and different off-current behavior.

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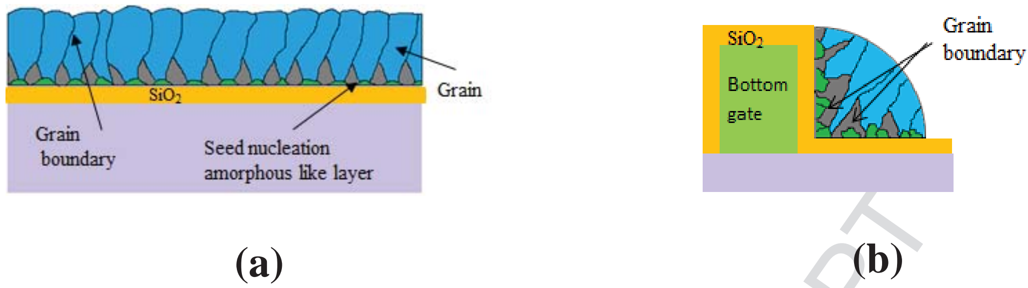
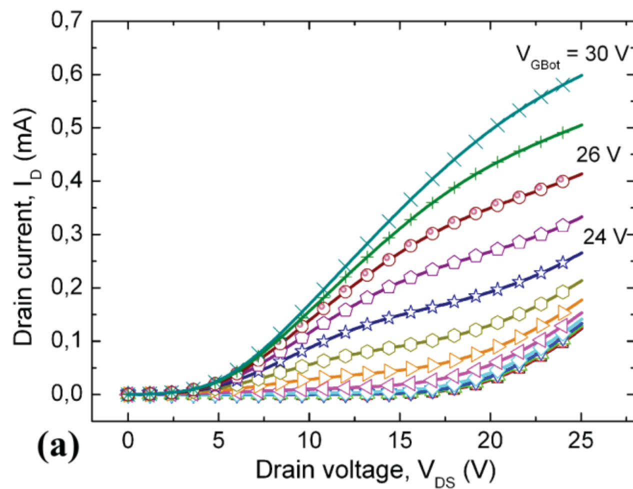


Fig. 4. Schematic cross section view illustrating the columnar type structure of a polycristalline silicon layer (a). Size lowering leads to a higher defects density within the polycristalline SiNWs close to the Si nanostructure/SiO_2 interface (b)



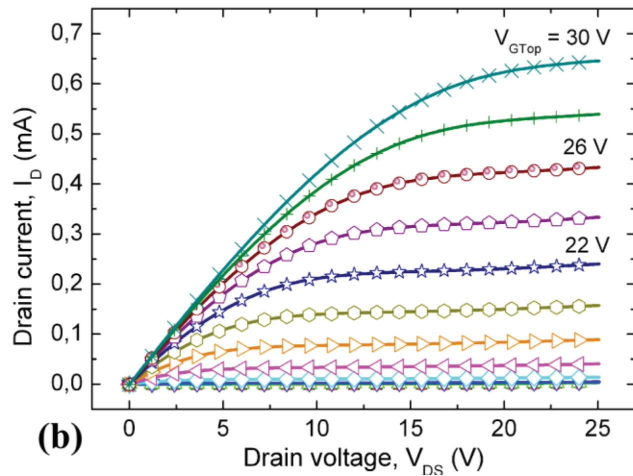


Fig. 5. Output characteristics of poly-Si NWFET I_D–V_{DS}: (a) bottom-gate and (b) top-gate transistors (1000 nanowires, L=5 µm). Measurement step is 2V. Saturation mode is easily reached for TGT and is not reached for BGT.

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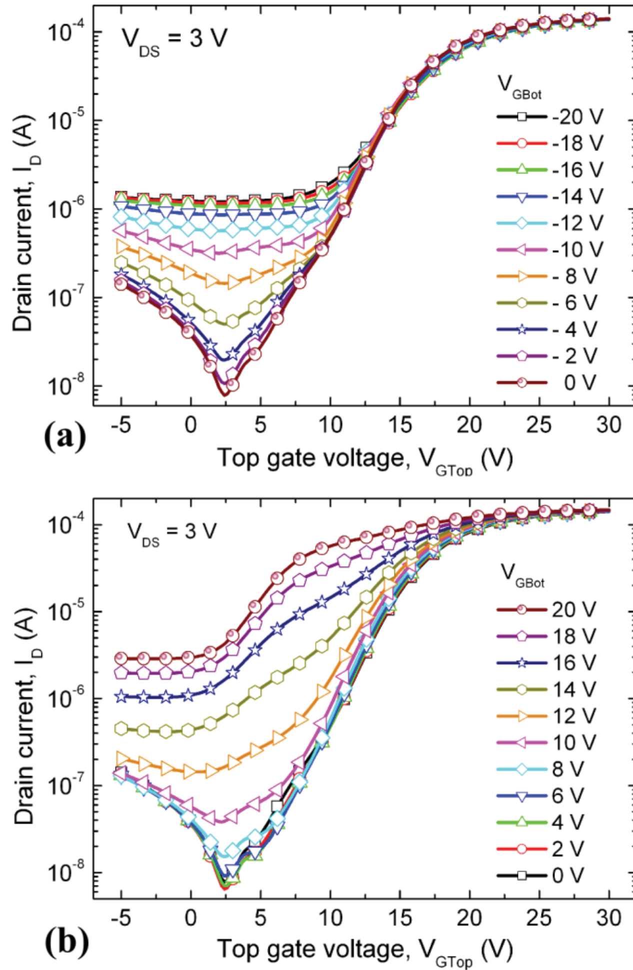

Fig. 6. Transfer characteristics of the top gate poly-Si NWFET I_D–V_{GTop}: (a) bottom-gate negative biasing and (b) positive biasing (V_{DS} = 3 V). These plots show a V_{GBot} sign dependence behavior, due to formation of a bottom channel.

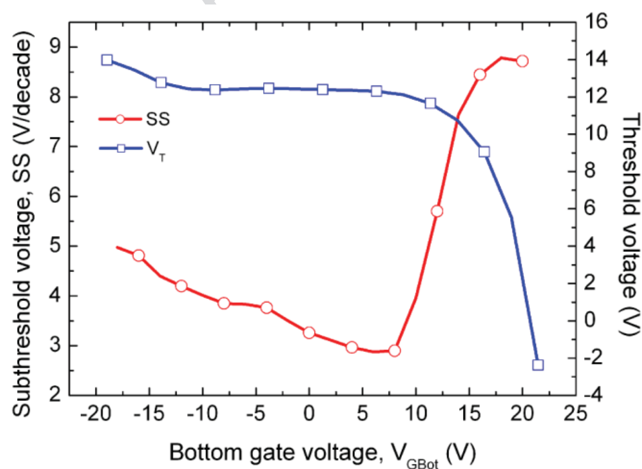

Fig. 7. Bottom-gate bias effect on subthreshold slope and threshold voltage on poly-SiNWs FET with separated top and bottom-gate electrodes (V_{DS} = 3 V). A relative stability of device is observed for V_{GBot} < 10 V.

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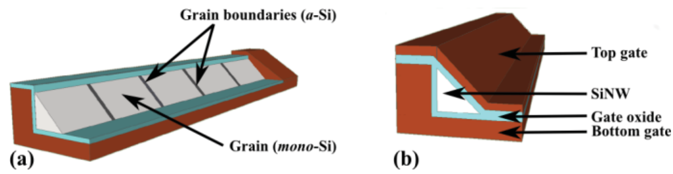

Fig. 8. Schematic structure of nanowires composed of 5 monocrystalline grains (width 80nm) and 4 amorphous grain boundary (a) (2.5 nm thickness), with a 80nm gate oxide thickness and cross section of final GAA structure (b).

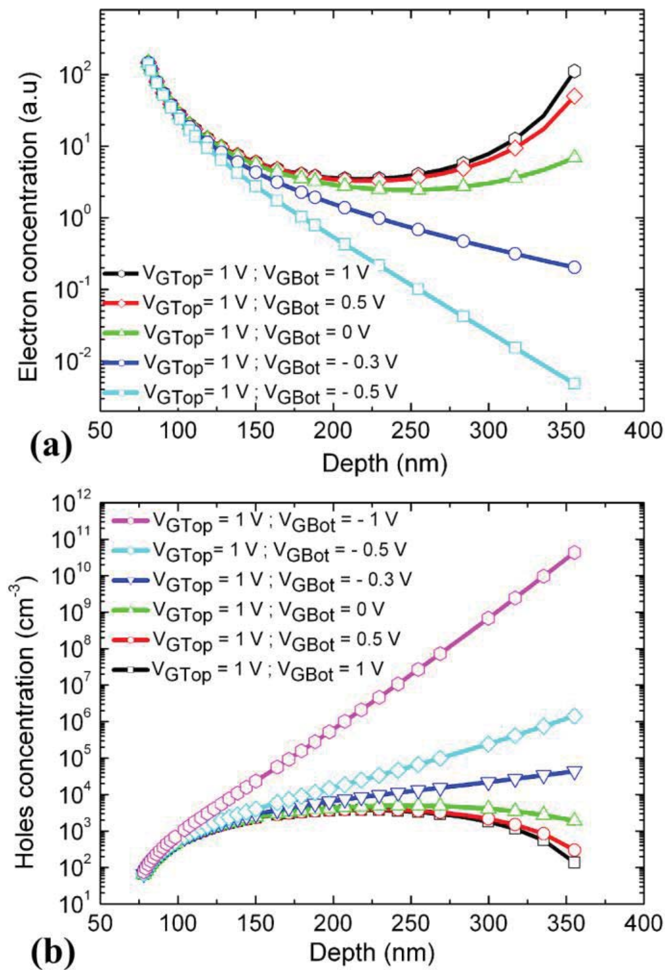

Fig. 9. Simulated distribution of electrons (a) at V_{Top}=1V (V_{GBot} =-0.5 to 1V) and holes (b) through a 300 nm width nanowire. Bottom channel conduction is as important as top channel's for positive bottom gate biasing.

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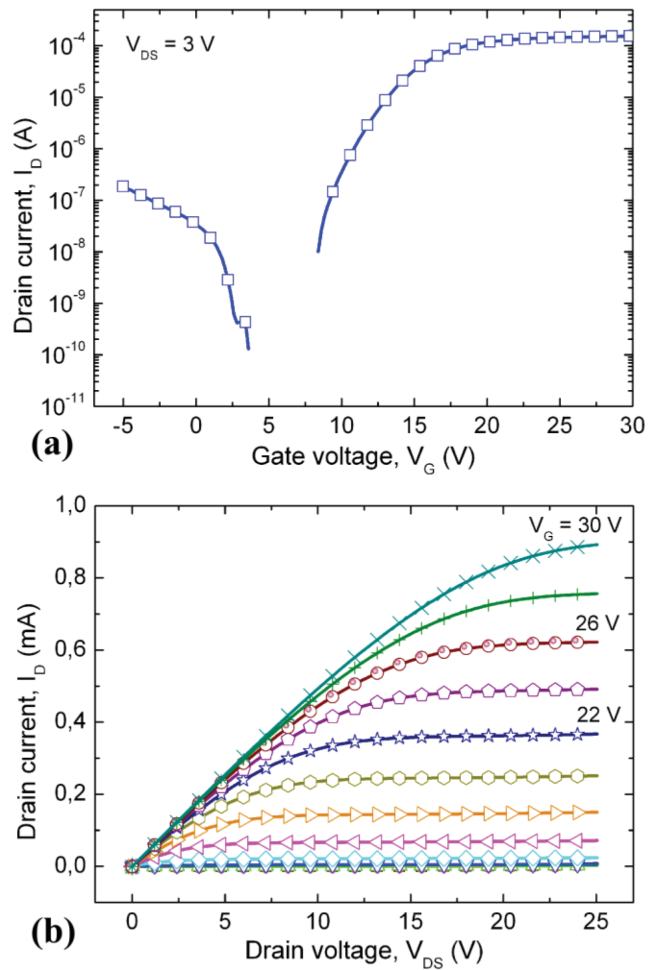

Fig. 10. Gate-All-Around poly-Si NWFET transfer I_D-V_G (a) and output I_D-V_{DS} (b) characteristics, showing a typical N-type FET behavior.

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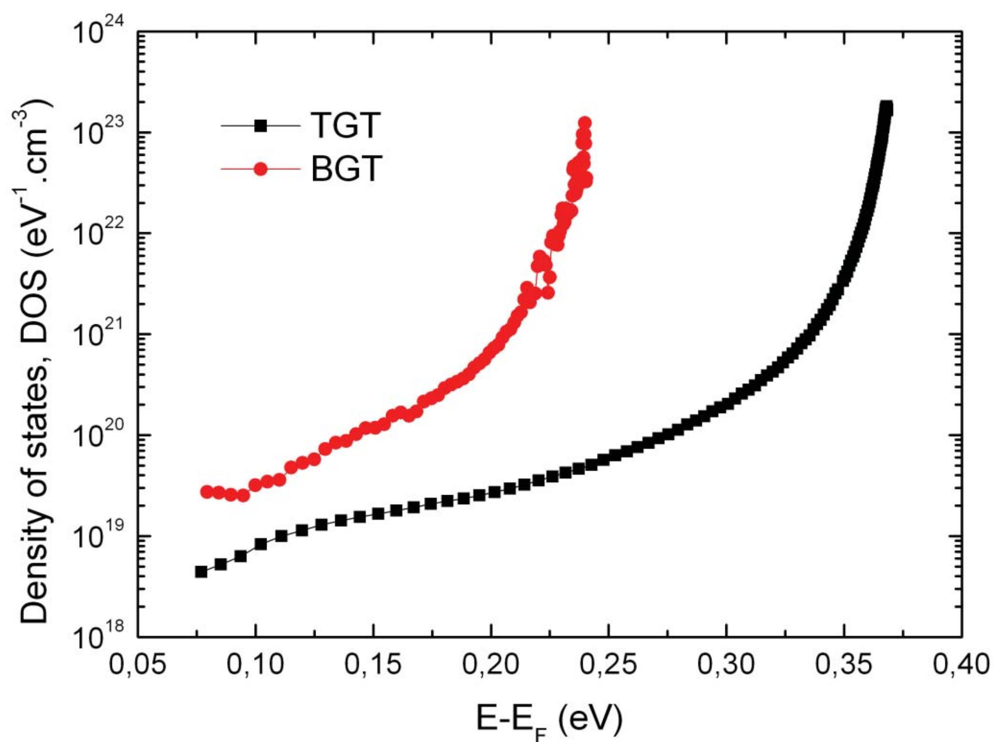

Fig. 11. Density of states for top, and bottom transistors configurations determined by Suzuki's method. Bottom-gate transistor shows higher DOS values than other two architectures.

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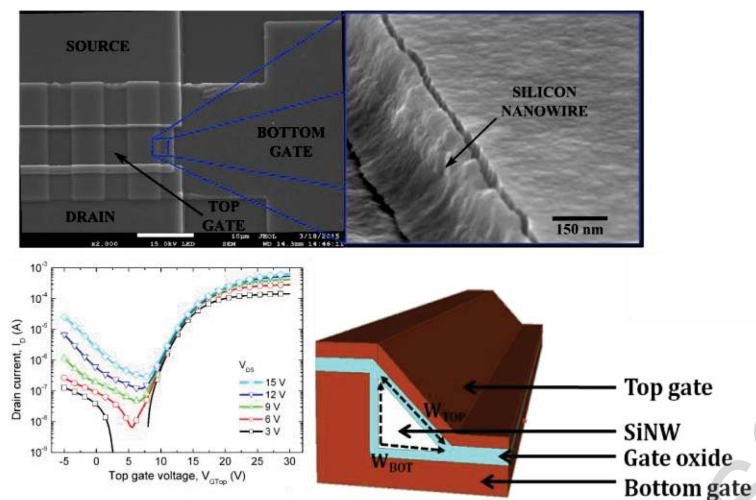

Graphical abstract

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