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Design And Characterization Of Optical Fiber-To-Chip Edge Couplers And On-Chip Mode Division Multiplexing Devices

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DESIGN AND CHARACTERIZATION OF OPTICAL FIBER-TO-CHIP EDGE COUPLERS AND ON-CHIP MODE DIVISION MULTIPLEXING DEVICES

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For my family and people who spent life together

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AWG	arrayed waveguide grating
ADC	asymmetric directional coupler
BOX	buried oxide
BPM	beam propagation method
(DE)MUX	(de)multiplexer
EDFA	erbium-doped fiber amplifier
Eskid	extreme skin-depth
EME	eigenmode expansion method
ER	extinction ratio
FDTD	finite difference time domain method
FEM	finite element method
FWHM	full width half maximum
FSR	full spectral range
HOM	high order mode
LiDAR	light for detection and ranging
LPCVD	low pressure chemical vapor deposition
MMI	multi-mode interferometer
MMF	multi-mode fiber
MDM	mode division multiplexing
MEMS	microelectromechanical systems
MFD	mode field diameter
NA	numerical aperture
OPA	optical phase array
PR	polarization rotator
PSR	polarization splitter and rotator
PBS	polarization beam splitter
PDL	phase delay line (or polarization dependent loss)
PDM	polarization division multiplexing
PDK	process design kit

RMS	root mean square
SOI	silicon on insulator
SMF	single mode fiber
SSC	spot size converter
SWG	subwavelength grating waveguide
SOA	semiconductor amplifier
SEM	scanning electron microscope
TE mode	transverse electric mode
TM mode	transverse magnetic mode
UHNA	ultra-high numerical aperture
WDM	wavelength division multiplexing

ABSTRACT

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Integrated silicon photonics has recently emerged as a promising solution to data interconnection in large data centers, which are characterized by short-range (0.5 – 2 km) and high bandwidth, *i.e.* 400 Giga-bit-per-second. Light from an external laser is first coupled to a silicon photonic chip, splits and modulated to carry data, and then multiplexed and coupled out to one or more optical fibers to take advantage of their large data bandwidth over their electric counterparts. However, short-range optical communication is still faced with several technical challenges. First, the difficulty to couple light between optical fibers and chips leads directly to significant power loss which reduces the transmission range. Therefore, a reliable scheme for fiber-to-chip coupling with high efficiency becomes imperative. Here we experimentally demonstrated various types of fiber-to-chip edge couplers and the best design yielded 0.56 dB/facet coupling loss for transverse-electric (TE) mode and 0.88 dB/facet for transverse magnetic (TM) modes, over a 100 nm bandwidth using lensed fiber. Additional challenges include (but not limit to) various on-chip optical multiplexing techniques. This thesis focuses on an emerging technique called mode division multiplexing (MDM), and presents designs, and in some cases experimental characterizations, for mode filtering, sharp bends, mode conversion as well as 3dB splitters.
Polarization handling and wavelength selective routing are also vital parts of photonic transceivers. Some theoretical solutions for better polarization and wavelength handling will be presented. Recently, integrated photonics has also shown potential in emission and ranging applications for autonomous driving, robots, and intelligent production lines. I will present the far-field emission and beam steering based on integrated optical phase arrays. Several important aspects of optical phase array are investigated, including beam forming and channel crosstalk suppression.

CHAPTER 1. INTRODUCTION

1.1 Integrated Photonics

In the past decade photonic integrated circuit (PIC) has become a promising solution for inter-chip and intra-chip optical communication. Integrated silicon photonics has emerged as one of the most prominent technology platforms, where silicon layer that guides light typically lies on top of a layer of silica which is known as silicon on insulator (SOI). SOI is favored for two prominent features: high refractive index contrast and CMOS-compatibility [1]. The high index contrast (between a silicon waveguide core and a silicon oxide cladding) leads to good confinement, which enables small device footprint with reasonably high integration density. Additionally, some photonic devices based on structure discontinuity prefer higher index contrast for better performance, such as photonic crystal structures and high-efficiency grating couplers etc. [1] The CMOS-compatibility on the other hand ensures major manufacturing companies don't need to replace their assembly line. The state-of-art CMOS fabrication process also ensures fabrication quality and reliability, which is a key driver for the growth of the field. This allows photonic products to be manufactured at high volume and being compatible to electronics IC on the same chip.

Today mainstream silicon photonics products are built on silicon-on-insulator (SOI) wafers, in which a crystalline silicon layer (200 – 250 nm thick) is stacked on top of a silicon oxide buffer layer (1-3 μm thick) followed by Si substrate. Photonic devices are pattern at thin crystalline silicon layer followed by top oxide cladding for protection while buried oxide layer (BOX) serves as barrier to prevent guided beam leaking into Si substrate.

There have been various photonic devices demonstrated on SOI platform, such as splitters, filters, (de)multiplexers, polarization-handling components, interferometers, resonators and coupling structures to optical fibers. In addition, with CMOS compatibility, electronic components such as micro-heaters and modulator driver circuits have been widely implemented on the same photonic chip. Although Si is the most widely used for passive photonics, the active part of the chip cannot be demonstrated with Si only due to its indirect bandgap. Therefore, other material based on Ge or III/V are usually chosen for light source and photodetector components. Fig 1.1 [2] shows various vital aspects for photonics industry, including generation, manipulation, and detection of light.

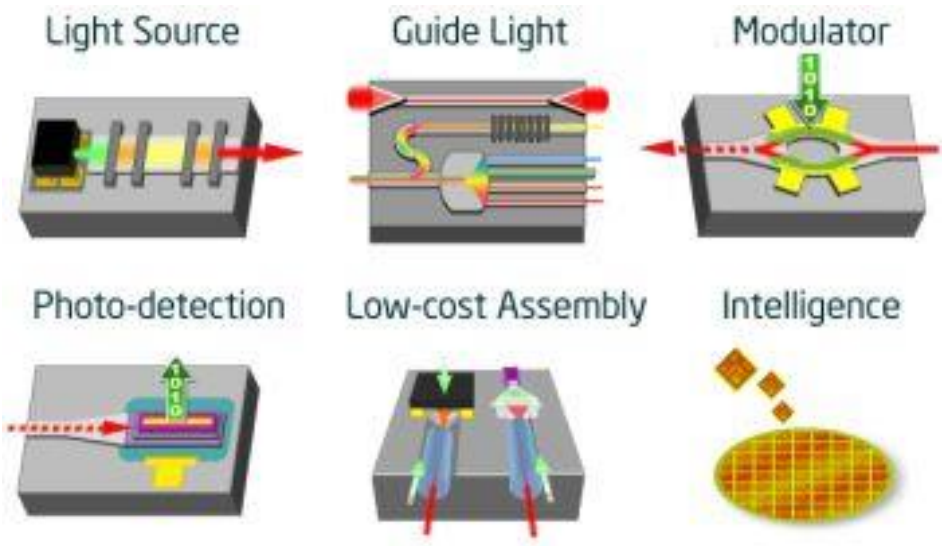


Figure 1.1 Various passive and active photonic components [2]

Although Si is widely used for passive components, its high index contrast does not always lead to design benefit. High index contrast is both a blessing and a curse: it allows one to implement unique functionalities on a very compact footprint but at the same time it makes the waveguide prone to scattering losses due to nm-scale roughness of the sidewalls of the waveguide. [1] Sensitivity to sidewall perturbation puts limit on some essential devices requiring ultralow propagation loss (such as ultra-high Q resonator) or extreme phase control (such as AWG). Hence there is an increasing interest in exploring alternative material with reasonable index contrast and CMOS-compatibility.

Recently Silicon nitride (SiN or Si_3N_4) has attracted lots of attentions with refractive index ~ 2 at 1550 nm wavelength. Silicon nitride is a common material in CMOS fabs and is typically deposited by either Low Pressure Chemical Vapour Deposition (LPCVD) at high temperature or by Plasma Enhanced Chemical Vapor Deposition (PECVD) at low temperature. [1] Due to high stress of nitride film, only nitride thickness within 300 nm can be CMOS-compatible yet there have also been rapid publication updates for photonic structure based on thick nitride. For example, Purdue researchers have reported a ultra-high Q ring resonator for optical comb generation at 600 nm thickness. [3]

Another difference between Si and SiN is optical nonlinearity. Two-photon-absorption (TPA) is a big problem for Si, which results in additional loss at high power. Therefore, Si becomes limited

at high power applications, even though Kerr nonlinearity is strong. Si_3N_4 has weaker Kerr nonlinearity but the TPA is virtually zero in view of the material's large bandgap. This enables nitride devices to work at strong power for some nonlinearity applications such as frequency comb generation [2] as well as supercontinuum generation [4].

In this thesis passive photonics components based on both Si and SiN as well as Si/SiN hybrid platform are designed and discussed. The strengths of two material platform can be even utilized together for some specific photonic applications.

1.2 Optical interconnect

Over recent years, optical interconnect based on integrated photonics has been vastly developed as alterative to electric copper interconnect to meet the ever-increasing data bandwidth demand. Conventional copper electronic interconnect faces some fundamental obstacles such as loss, crosstalk, latency, especially at high frequency regime. As a comparison, optical interconnect shows superiority in terms of high bandwidth and energy efficiency (Joule/bit) to its electric counterparts. For these reasons integrated photonics is introduced to develop optical interconnect as the preferred solution for short-range communication link (rack-to-rack, backplane, inter-board, and even inter-chip).

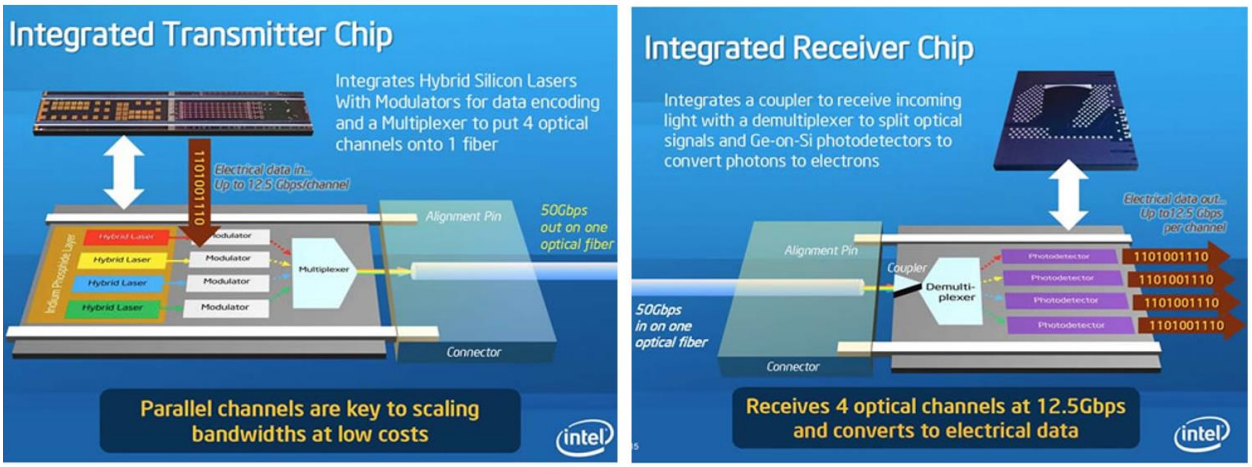


Figure 1.2 Schematic of optical transmitter chip and receiver chip developed by Intel for 50 Gbps transmission link [5]

The fundamental principle of optical interconnect is to encode and decode electric data by using optical carriers. Fig.1.2 shows a basic schematic for optical interconnect link, where a transmitter chip is used to modulate data on laser beams and receiver chip is designed to receive modulated laser beams and convert back to electric signals. Four integrated III-V lasers at different wavelengths are modulated as on-off-keying (OOK) by electric driver signals. Modulator on silicon [6] normally relies on free-plasma dispersion effect, which requires rigorous doping profile definition on silicon ridge waveguide. Then four parallel channels are multiplexed together (WDM) and couple out of chip through an optical fiber. The multiplexed beam in fiber is butt-coupled to the receiver chip, demultiplexed and converted back to four parallel electric signals (same as modulator driver signals). On receiver chip, polarization handling devices are usually required since beam after fiber transmission does not maintain polarizations. The wavelength multiplexed signal is first demultiplexed then separated channels are recovered by integrated photodetectors. Integration of passive and active devices on photonic chips enables a 50 Gbps transmission link that outperform its electric counterparts regarding bandwidth, energy efficiency and signal quality.

Recently there has been attempts to integrate both transmitter and receiver sides together on one photonic chip, named optical transceiver. Transceiver can act in a bidirectional way that allow sending and receiving optical data at the same time. Fig.1.3 illustrates a transceiver chip which integrates various active and passive components (driver circuit, waveguides, modulators, photodetector, and edge couplers etc.) together. It’s worth noticing that there is no integrated lase sources on this transceiver chip and this occurs since direct integration of III-V lasers on photonic chip is too expensive. A more favorable solution is to build a separate III-V light source chip and bond with transceiver chip to by wafer bonding.

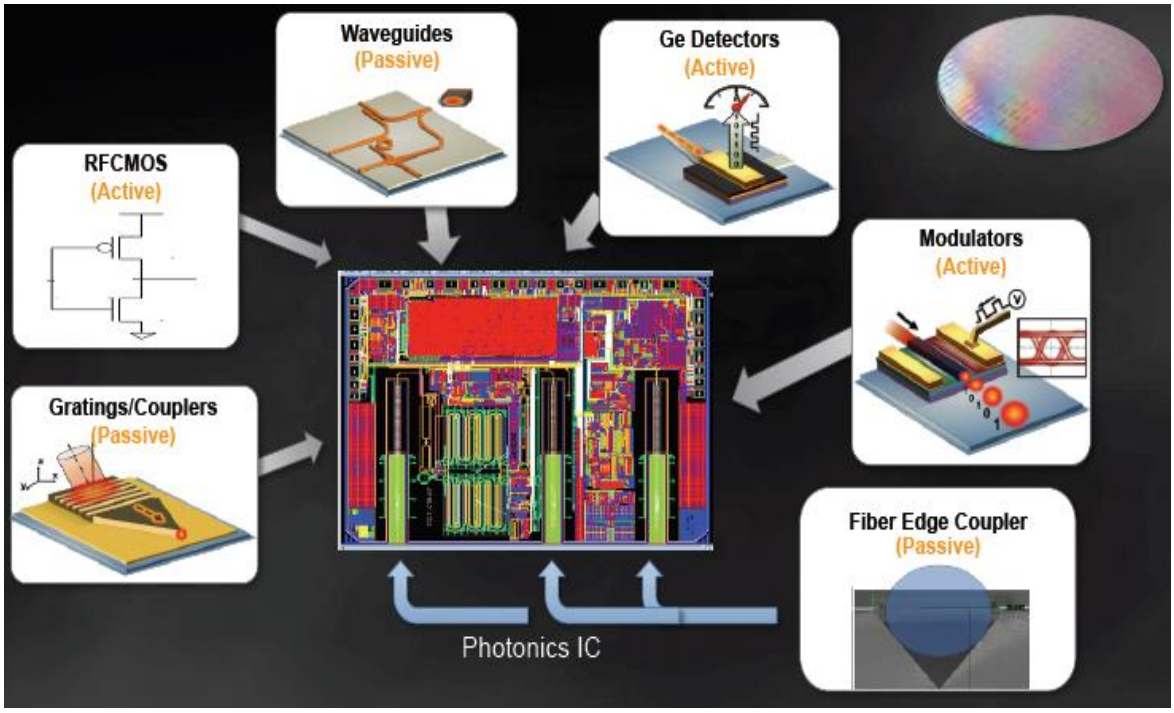


Figure 1.3 Photonic integrated circuit (PIC) for transceiver module [7]

Practically multiple optical transceiver modules are deployed with switching network. Fig.1.4 illustrates a photonic router network schematic developed by J. Bower's group [8] which comprises 8 transceivers. On each optical transceiver, 8 wavelength channels are multiplexed together for intra-chip fiber transmission. The multiplexed signals out of transceiver is sent to an optical switch network, that determines the destination of optical data packages. Switch network can allow data to be passed to any individual transceiver chip (node-to-node mode) or to all transceiver chips (broadcast mode). Multiple transceivers with shared switch network form the prototype of optical router, which is widely used at datacenters.

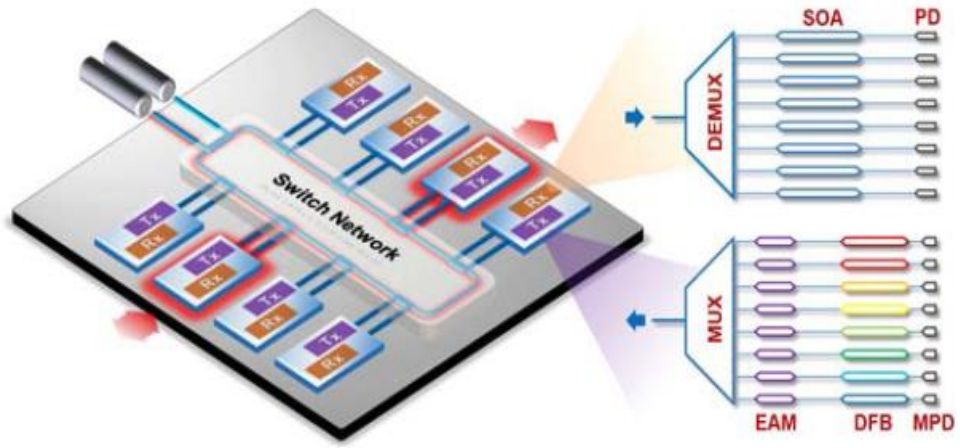


Figure 1.4 Architecture of 8 × 8 × 40 Gbps fully integrated silicon photonic network on chip [8]

Although being commercialized products, photonic transceiver chips still faces several practical challenges. Primarily, fiber-to-chip coupling efficiency remains undesirable, which limits the power budget for the entire photonic chip. In addition, most transceiver chip uses on-chip multiplexing technologies for further enhance channel capacity, while on-chip multiplexing remains far from perfect. The most widely used wavelength division multiplexing (WDM) is powerful but also expensive both in terms of multiple laser sources and massive footprint. Alternative multiplexing such as using orthogonal polarizations can be used it can at most double the data capacity but meanwhile it suffers polarization drift in optical fibers.

Another multiplexing technique based on orthogonal waveguide modes has attracted researchers' attention over recent years since it theoretically allows more than two channels to be used concurrently. Nevertheless on-chip mode division multiplexing (MDM) is still far from commercialization for its incompatibility with fiber as well as various passive design challenges (bend, split and cross…). Therefore, photonic transceiver chip and its various passive components (especially for coupling and multiplexing) are still valuable topics for scientific research.

1.3 Integrated Photonics for imaging

Recently integrated photonics has also attracted industry and academic attention for its potential application on imaging. Light Detection and Ranging (LiDAR) has been the main driving force

for photonic imaging, which can be widely used for autonomous driving, robots, and intelligent production lines. Fig.1.5 shows various detection and ranging equipped for a driverless vehicle, including conventional camera, Radar, and emerging LiDAR sensing. Comparing with camera, both Radar and LiDAR show superiority of sensing in darkness. Although Radar is robust to severe weather conditions, the long microwave wavelength of sensing dictates its low sensing resolution. LiDAR on the other hand uses much shorter wavelength at optical frequency, which allow detection of small objects under high resolution as shown in Fig.1.6.

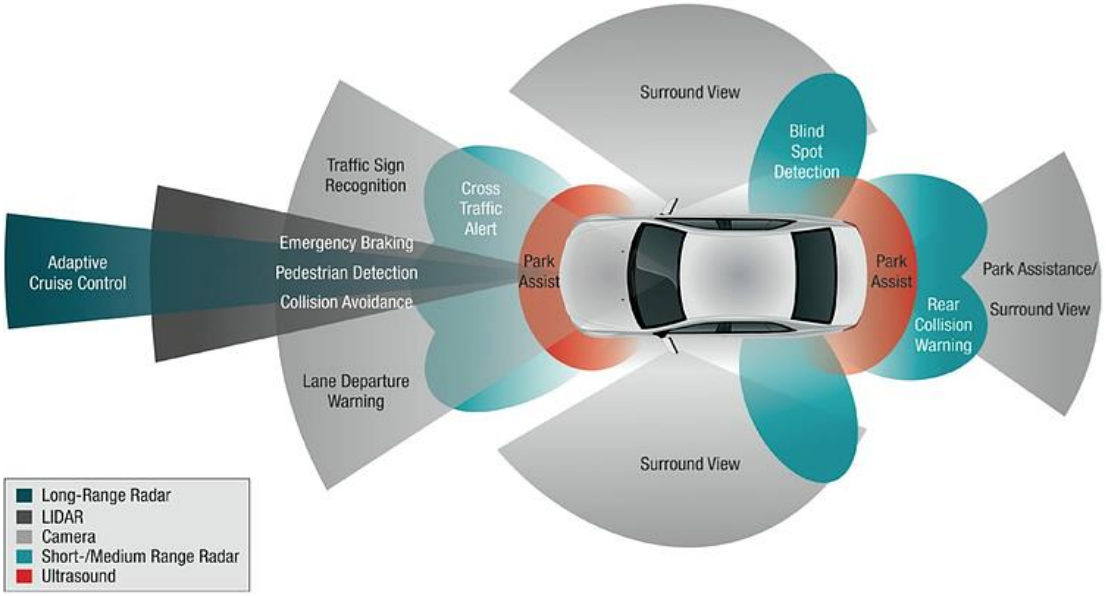


Figure 1.5 Various detection and ranging technologies for autonomous driving [9]

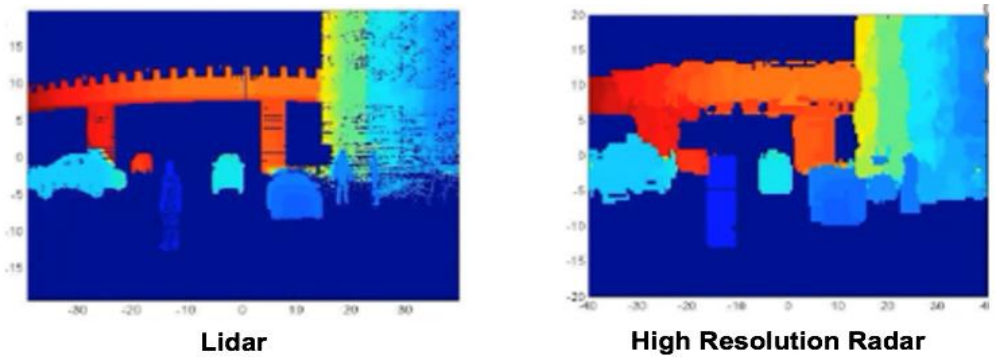


Figure 1.6 Image sensed by Lidar and high-resolution Radar [10]

Fig.1.7 show a conventional LiDAR placed on the roof of a vehicle based on sophisticated and bulky combination of laser, lenses, and mechanical rotation (spinning) parts. Due to complicated assembly and calibration as well as difficulty of mass production, conventional LiDAR shows incredibly high unit costs.

Figure 1.7 Conventional LiDAR spinning on the roof of a vehicle [11]

Alternatively, solid-state LiDAR solutions are also heavily investigated over recent years, including LiDAR based on Flash, Microelectromechanical systems (MEMS) and optical phase array. It's widely believed that miniaturized LiDAR system can be smaller, lighter, and more importantly allow faster beam steering. Those solid-state LiDAR technologies are still in the stage of laboratory research but they offer great potentials for miniaturized LiDAR. Fig.1.8 illustrates a MEMS based LiDAR, which steers the beam direction by a MEMS mirror. Nonetheless, many people believe MEMS based LiDAR is not a reliable option for vehicle due to vibration during driving and its ~ KHz steering speed is not that fast enough.

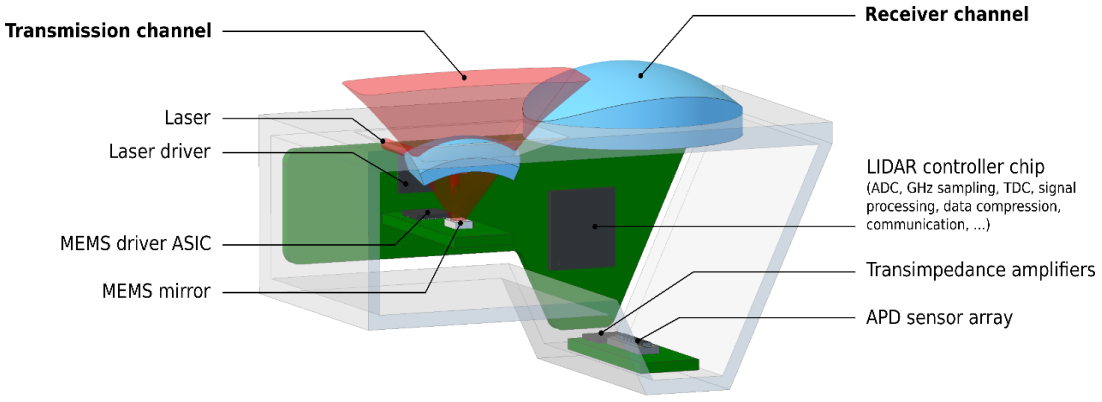


Figure 1.8 LiDAR based on MEMS mirror [12]

Another popular research direction is to use integrate optical phase array (OPA), which steers the beam by externally controlled phase front. Phase is usually controlled by thermal tuning (~ hundred KHz scan rate) or more lossy electrical tuning (~ GHz scan rate). Chip-scale LiDAR based on optical phase array can theoretically be a low-cost solution due to massive volume chip production through CMOS process. Fig. 1.9 shows a OPA reported by Intel Lab [13], allowing 80-degree beam steering angle in φ direction.

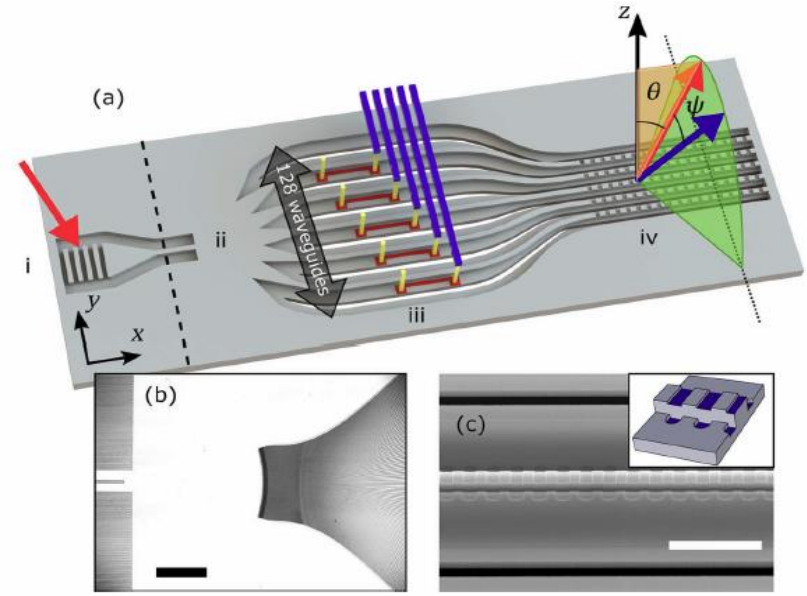


Figure 1.9 Intel's OPA solution with ultra-wide steering angle [13]

In terms of OPA, there has been no perfect solution for LiDAR yet. OPA's performance is primarily limited by several factors, including restricted steering angle (limited by grating sidelobes), beam propagation distance (limited by mainlobe emission efficiency and waveguide power handling capabilities) and efficient beam steering solution. Large adjacent grating emitter spacing is the limiting factor for grating sidelobes while if grating spacing is too small, channel crosstalk becomes inevitable. In addition to effectively steer the beam, precise phase control is needed among large number of emitter channels. Intel Lab's solution with 128 channels are individually tuned by thermal heaters and sophisticated algorithm is developed for IC circuit to tune 128 heaters concurrently. Still Intel's solution is not perfect as during sidelobe suppression, mainlobe power is also significantly attenuated. Currently OPA based LiDAR is a good opportunity for photonic. If photonic OPA chip proves to be the final candidate low-cost solid-state LiDAR, the field of integrated photonics will acquire massive consumer electronics market.

1.4 Thesis outline

This thesis mainly discusses the design of several essential devices for optical transceiver modules, including edge coupler, on-chip optical multiplexing. The emerging mode division multiplexing technique is explored in depths to offer more versatile and practical functionalities Conventional multiplexing techniques based on polarization and wavelength are numerically explored and reported in this thesis. Eventually optical phase array (OPA) based on integrated photonics is also covered in this thesis, with emphasis on OPA's passive designs. Chapter 1 will briefly overview the photonics industry and introduce those research topics.

Chapter 2 shows the fiber-to-chip edge coupler project that is sponsored by Furturewei Technologies Inc. Upon Furturewei request, various types of edge couplers are designed, fabricated, and measured. Two patent applications are filed based on edge coupler research and Futurewei Technologies took the exclusive license of the patent.

Chapter 3 concludes my research work for on-chip MDM applications where various essential MDM components (spot size converter, filter, bend, splitter, and mode converter) are designed and many of which are characterized. Chapter 3 explores the phase sensitivity phenomena which fails to be discovered by previously reported works. Three solutions to solve phase sensitivity issue have been proposed based on filter, bend, and splitter respectively.

Chapter 4 demonstrates my design work on polarization and wavelength division multiplexing. Unique design of polarization beam splitter (PBS) and polarization splitter and rotator (PSR) are numerically demonstrated to improve extinction over broad bandwidth. Arrayed waveguide grating (AWG) which is known as the industrial standard (de)multiplexers for wavelength division multiplexing is also numerically investigated. With Phoenix Optodesigner software evaluation, an AWG design toolbox is developed for automatic generation and simulation of AWG under user's specification. Various design and simulation challenges are also discussed with suggested solutions.

Chapter 5 shows some results of on-going research project on optical phase array (OPA). OPA has huge potential to work as chip-scale LiDAR emitter but its high order grating sidelobe severely limits its power efficiency and beam steering angle. This chapter shows some experimental results for conventional passive OPA and then numerically explore potential solutions for high order sidelobes suppressions.

CHAPTER 2. FIBER TO CHIP EDGE COUPLER

2.1 Introduction

Coupling of light to and from integrated optical circuits has been recognized as a major practical challenge since the early years of photonics. The coupling is particularly difficult for high index contrast waveguides such as silicon-on-insulator (SOI) due to enormous mode size mismatch. As shown in Fig.2.1, standard single mode fiber has mode field diameter ~ 10 μm which far exceed the dimension of a single mode SOI waveguide (450 nm by 200 nm). There are two main categories of fiber-to-chip coupling approaches, in-plane coupling via edge coupler and out-of-plane coupling via grating coupler. Both types of coupling scheme have been widely used for academic research and industry whereas edge coupler has become favorable by the community for some practical considerations.

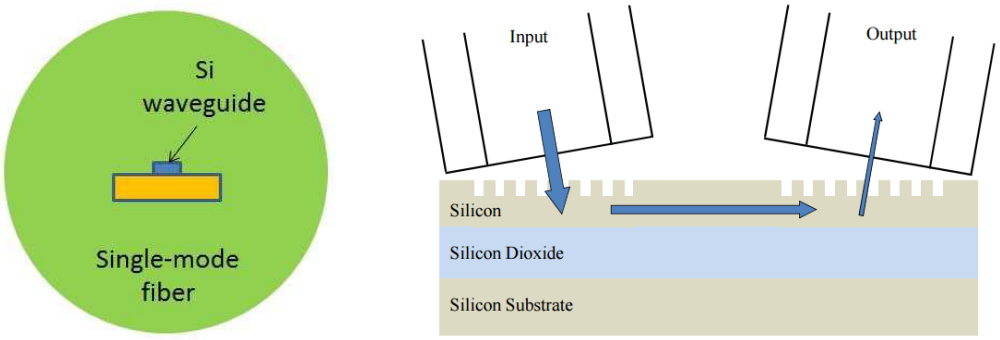


Figure 2.1 Cross-sectional of SMF-28 fiber and SOI waveguide [14] (b) Side view of grating coupler [14]

Grating couplers were invented in the 1970's as a method of coupling free space laser light into glass films. The grating coupler is essentially a Bragg grating optimized to diffract light from a free space source into a dielectric waveguide [14]. Fig.2.1 (a) shows a 2D side view illustrating the input beam from SMF-28 fiber is diffracted by grating and subsequently coupled into to the SOI chip and then gets coupled to the output fiber via another grating coupler.

Over the past few years, grating coupler has been widely used as misalignment tolerant fiber-to-chip coupler for large fiber mode size (MFD ~ 10μm). Nonetheless grating coupler has several intrinsic limitations that hindering it from industrial implementation. The grating coupler works with famous grating equation as shown in Eq.1, where n_{eff} is the effective refractive index of the

grating, n_{top} is the refractive index of the top cladding material, θ_c is the diffraction angle (coupling angle perpendicular to the chip) associated with diffraction order m. Normally designer specify a center wavelength (typically ~ 1550 nm) and diffraction order (usually m = 1) as well as diffraction angle, then grating pitch $\underline{\Lambda}$ is derived. [15]

$$n_{eff} = n_{top} \sin(\theta_c) + m \frac{\lambda}{\Lambda} \quad [15]$$

However, the grating equation is a function of wavelength $\underline{\lambda}$ and diffraction angle is also affected by beam wavelength given fixed grating pitch. Therefore, grating coupler has always been limited by its bandwidth [15] ,which prohibit its application towards wavelength division multiplexing (WDM). In addition, problem of polarization sensitivity also rises since n_{eff} term is different for (quasi)TE and (quasi)TM mode. Typically, a conventional grating coupler can achieve 20 dB polarization extinction [14] and for this reason it has been widely used at university and labs to distinguish polarizations. However, in commercial applications fiber polarization cannot be easily controlled due to fiber's circular symmetry and working for a specific polarization make grating coupler problematic at packaging.

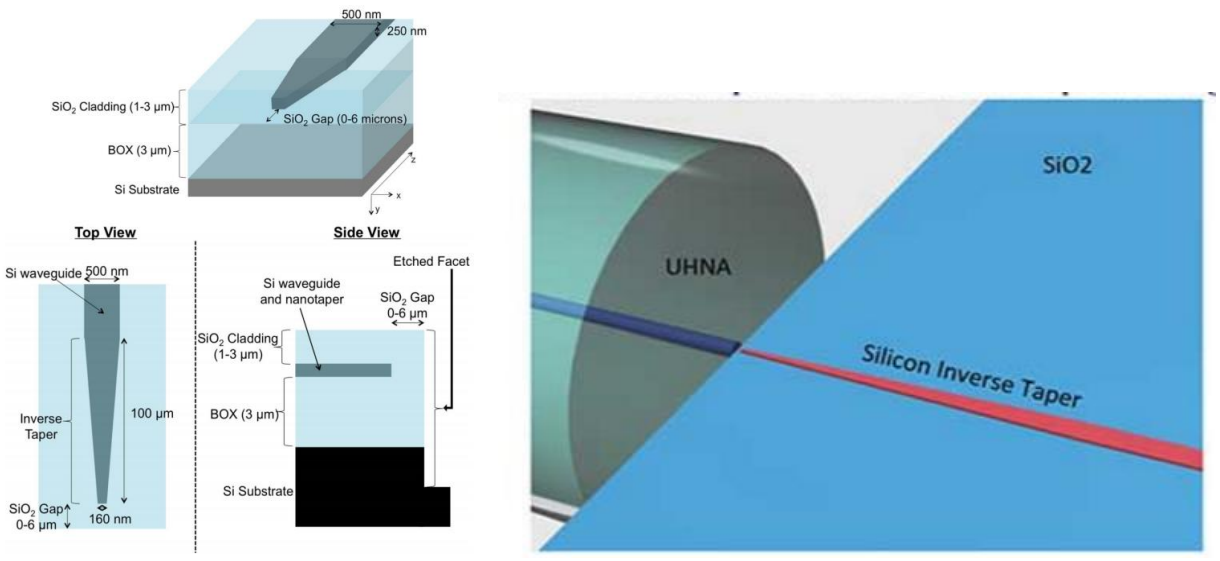


Figure 2.2 (a) Example of conventional SOI inverse taper based edge coupler schematic [16] (b) UHNA (Ultra-high NA) fiber end-fire coupled to inverse taper [17]

As an alternative, edge coupler based on inverse taper has been purposed in 2003 [18] and heavily developed over the past decade. Inverse taper relies on mode evolution where waveguide is gradually tapering down to expand the (weakly guided) mode profile to match with certain fiber mode size. Edge coupler shows polarization insensitivity as well as broadband transmission even though coming at costs of weak misalignment tolerance. However traditional SMF-28 fiber has the MFD even larger top and bottom oxide cladding, meaning mode size must be reduced before end-fire coupled to the edge coupler tip. During research most widely used approaches are splicing SMF-28 with lensed fiber [19] or high NA flat fiber [20] and splicing losses are characterized for power normalizations. Fig.2.2 shows an example configuration that couple light from high NA flat to inverse taper.

Instead of using single Si tip to obtain decent mode overlap, edge coupler with multiple tips are also designed such that supermode of multiple tips can overlap well with input fiber mode. Fig.2.3 illustrates a trident shape edge coupler developed by N. Hatori in 2014 [21]. Fiber mode initially couple to the supermode supported by tips, followed by the introduction of central Si taper. As Central taper expands wider to suck the modal field in, two outer waveguides taper away to release confined mode. Eventually when entire power is transferred from dual arms into central Si waveguide, dual outer arms are terminated. This design has been improved by a number of researchers with better initial overlap design [22] and alterative way for combining power [23]. In addition, some researchers do claim edge coupler with multiple tips show better misalignment tolerance compared with single tip inverse taper. [24]

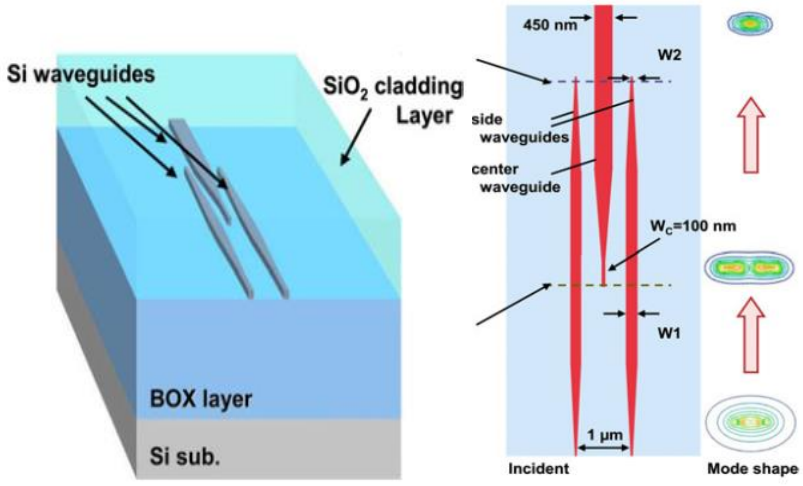


Figure 2.3 Trident edge coupler schematic and top view developed by N. Hatori in 2014 [21]

An alternative realization of edge coupling is to deploy an intermediate cladded waveguide to collect input beam first, followed by inverse taper within it to complete mode transformation [25][26]. Typically, polymer material (SU8 for instance) is used for cladded waveguide and input beam is aligned with cladded waveguide center rather than Si tip. Such edge coupler can theoretically allow direct SMF-28 fiber input given large polymer waveguide, nonetheless degradation of polymer as well as material absorption prohibit it as mainstream of edge coupler for commercial designs.

Inverse taper with and without polymer cladded waveguide has completely different operation principles. For SOI taper without cladded waveguide, tip width should be carefully chosen to match the size of input beam and typically a short taper (~ 50 μm) can ensure high mode conversion efficiency. For inverse taper with cladded waveguide, the polymer waveguide dimension must be designed to match with input beam size whereas Si tip width should remain as narrow as possible to avoid introducing mode mismatch loss.

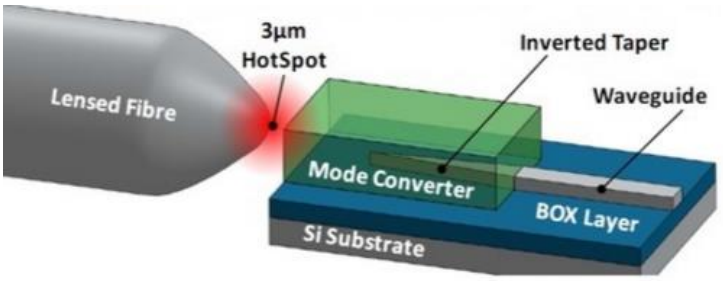


Figure 2.4 Lensed fiber end-fire coupled to inverse taper with intermediate cladded waveguide [27]

For inverse taper based mode converter, there is several rules of thumb for mode (size) conversion. Firstly, tapered waveguide must be long enough to ensure low transition loss (adiabatic transition). Secondly large the mode size mismatch between input tip and output waveguide, longer the taper length is required to suppress transition loss. Lastly larger the misalignment between input and output beam propagation axis, longer taper length is also mandatory to achieve low transition loss. Following the last rule, taper with cladded polymer waveguide usually require much longer taper length than conventional SOI taper. Substantially longer device together with accumulated polymer absorption render this coupling scheme (Fig.2.4) less favorable.

2.2 Conventional SOI edge coupler based on inverse taper

Conventional SOI edge couple based on inverse taper has been initially purposed by Michal Lipson's group in 2003 [18], since when inverse taper has been heavily developed by both academic research and industry. Although showing considerable alignment sensitivity, inverse taper shows flat-band low insertion loss as well as polarization independence. Nevertheless, inverse taper is still not an ideal edge coupling solution for industry (prefer SMF-28 fiber) for several reasons.

First and foremost, SMF-28 fiber with huge spot size leads to challenge of Si tip design during mode overlap optimization. Ideally as Si taper tip width reduce, the mode size would expand with weaker confinement. However, to design polarization independent mode overlap, a square tip is needed [28], which give too small mode profile to match with SMF-28. Another problem when using SMF-28 fiber is the power leakage into Si substrate since standard SOI wafer only has 2-3 μm thick buried oxide (BOX) layer. In order to use SMF-28 with mode radius ~ 5 μm without substantial leakage loss, IBM researches [29] purposed to etch away the Si substrate and filled with index matching gel. Nonetheless replacing Si substrate with index matching material is not a standard CMOS process and even with that complicated recipe an inverse taper with ~ 1mm length is required for low loss mode conversion. For the reasons listed above, even industry starts to accept the idea to reduce spot size (lensed fiber or high NA fiber) before coupling to inverse taper. Yet due to packaging concern, lensed fiber is not a good option which can be sensitive to misalignment and damage. High NA fiber has become a favorable candidate that active alignment is initially done followed by UV curable gel to fix the positions for packaging.

Over the past decade, several inverse-taper-based edge couplers has been reported. However, those design still rely on those rule of thumb which claim longer the taper length give better efficiency [30]. Here we further scrutinize this argument and demonstrate that when sidewall roughness is considered there should always exist an optimized taper length. Our discovery has been published in OFC conference in 2015 [19].

Here we investigate the traditional SOI inverse taper (with linear taper shape) designed for lensed fiber. Schematic of edge facet in simulation is shown in Fig.2.5 (a) where 1 μm top cladding and 3 μm BOX is chosen. Input mode is assumed to be Gaussian profile (MFD = 2.5 μm) with polarization aligned with horizontal axis (TE polarized). TE mode overlap with Gaussian mode is

firstly calculated Lumerical Mode solution based on following equation [31], which TE optimized overlap of 85% at 180 nm tip width. Similarly, optimized TM overlap around the same value can be obtained at 160 nm tip width assuming input Gaussian beam is vertically polarized.

$$overlap = |Re\left[\frac{(\int \overrightarrow{E_1} \times \overrightarrow{H_2}^{*} \cdot d\vec{s})(\int \overrightarrow{E_2} \times \overrightarrow{H_1}^{*} \cdot d\vec{s})}{(\int \overrightarrow{E_1} \times \overrightarrow{H_1}^{*} \cdot d\vec{s})}\right] \times \frac{1}{Re(\int \overrightarrow{E_2} \times \overrightarrow{H_2}^{*} \cdot d\vec{s})}| \qquad [31]$$

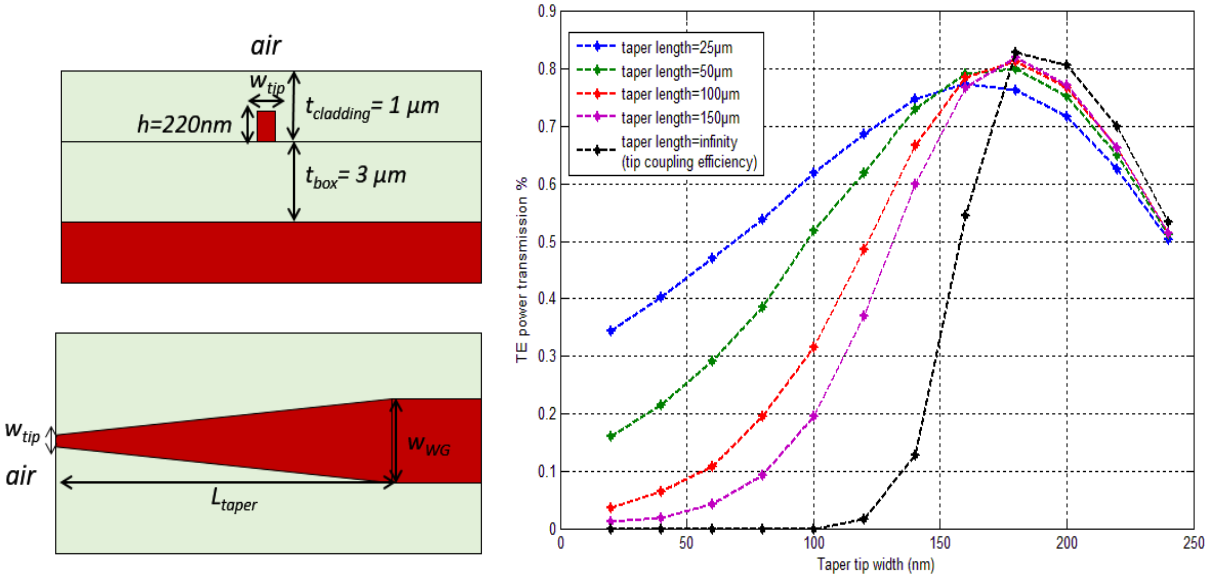


Figure 2.5 (a) front view of edge facet and top view of inverse taper (b) TE mode overlap to Gaussian mode (MFD = 2.5 µm) at 1550 nm wavelength and various tip width [19]

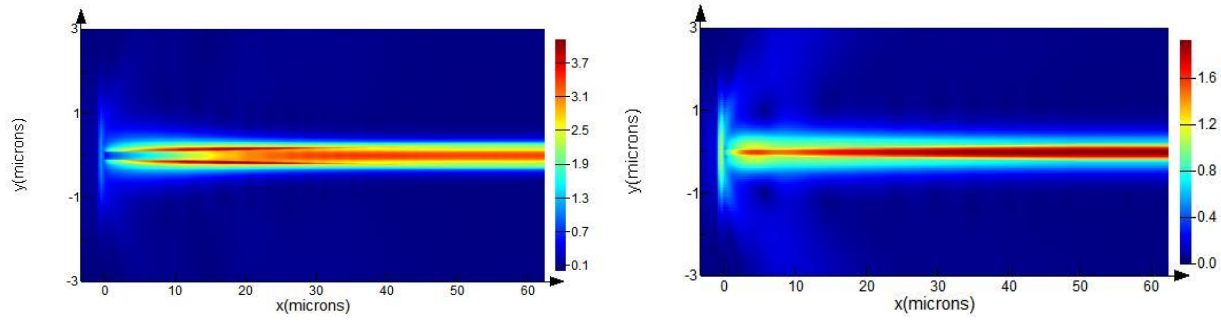


Figure 2.6 (a) |E| top view for TE input and (b) |E| top view for TM input at 1550 nm wavelength with smooth sidewall

Fig. 2.6 shows the field evolution along a 50 μm long inverse taper for both polarizations. Input beam is initially trapped by the taper tip then gradually suck into Si waveguide core. Nonetheless, story becomes different when sidewall roughness is introduced. Sidewall roughness is an inevitable fabrication imperfection mainly caused by the limited resolution of Ebeam spot size and grid discretization [32][33].

As shown in Fig.2.7, the SEM image shows Si tip has some sidewall surface fluctuation which is the sidewall roughness we are trying to evaluate. SOI is renowned for high index contrast, which leads to smaller footprint as well as high sensitivity to sidewall perturbation [1]. Sidewall roughness will not only contribute to high propagation loss but also phase error which can be detrimental for some phase sensitive applications (like arrayed waveguide grating). For edge coupler, phase error is not important but scattering loss can be even more serve than SOI strip waveguide. For standard SOI waveguide mode is relatively well confined hence very limited power resides on rough wide sidewalls, leading to ~ 3 dB/cm propagation loss. For SOI inverse taper however, during width expansion there is always a regime where mode power is strongly located at vertical sidewalls [33], leading to considerable scattering loss that cannot be ignored.

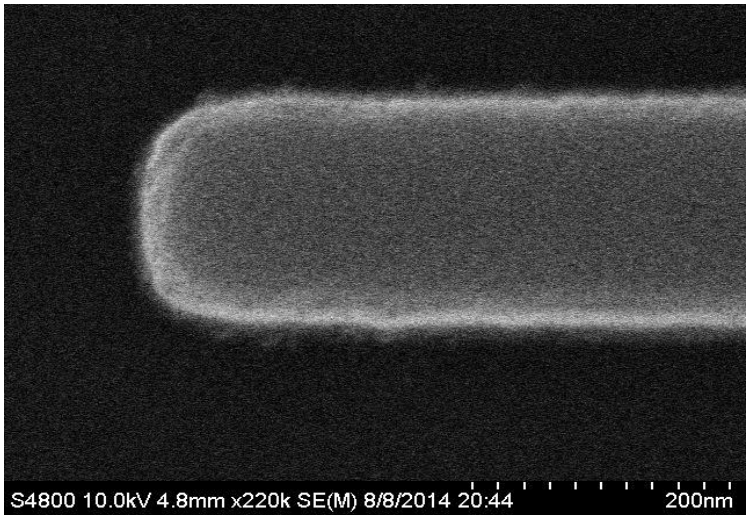


Figure 2.7 SEM image of Si tip with sidewall roughness

In Lumerical FDTD, sidewall roughness can be generated with script. Roughness is created by first generating random matrix in K space, followed by Gaussian filtering the matrix with correlation length and eventually Fourier transform back to real space and normalize with σ (sigma

RMS amplitude) [34]. By convention correlation length (Lc) depicts statistically on average the width of each "bump" (spatial frequency) and σ_{rms} dictates the rms value of surface fluctuation. From Lee's experiment [35] Lc = 50 nm for SOI waveguide and σ_{rms} is less than 10 nm (statically peak fluctuation is three times higher than σ_{rms}). Fig.2.8 shows the Lumerical structure of taper with roughness on both vertical sidewalls and under mesh refinement region with 10 nm mesh size, refractive index of such sidewall perturbation can be captured relatively well. Then the roughness is added upon a 50 μm long taper and Fig.2.9 shows TE mode propagation suffer more attenuation than TM does. This can be explained by the fact that TE mode has larger power distribution on vertical sidewalls than TM mode.

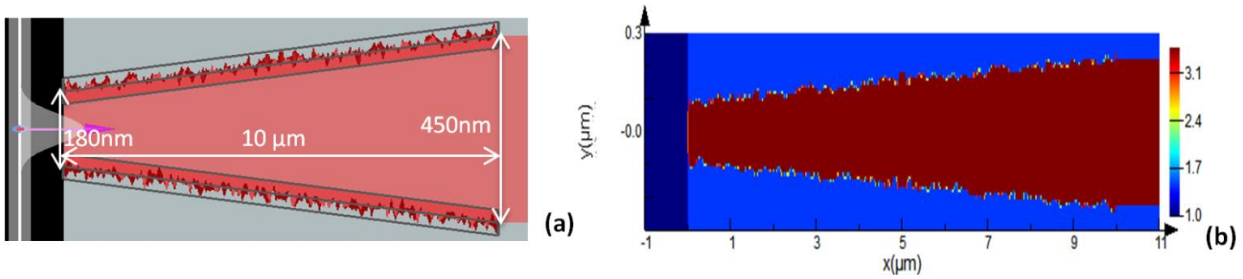


Figure 2.8 (a) Lumerical structure of a 10 μm long taper with 50 nm correlation length and 10 nm σ_{rms} (b) Refractive index monitor top view given 10 nm mesh size [19]

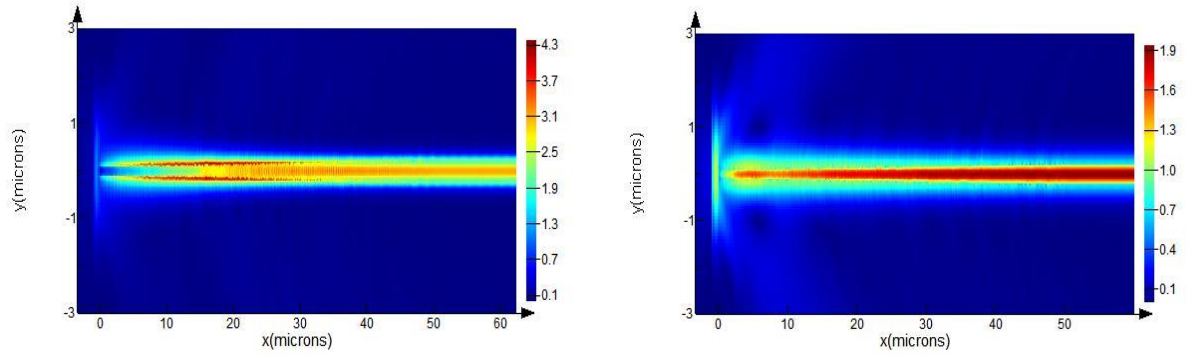


Figure 2.9 (a) |E| top view for TE input and (b) for TM input at 1550 nm wavelength with 10 nm σ_{rms} roughness and 50 nm correlation length

To characterize scattering loss caused by roughness upon an inverse taper, a measurement is done by using lensed fiber where the setup is shown in Fig.2.10 The chip is in the middle with edge couplers on both edges. Lensed fiber is spliced with SMF-28 and became located at stage for a

fiber-to-fiber test in air. The power after fiber-to-fiber test is taken as benchmark value for power normalization. Then power is measured through the chip (device) and the difference between two scenarios (with and without the chip) is treated as loss of the chip, which includes two edge coupler loss as well as some bending and waveguide propagation loss. The Si waveguide bending and prorogation loss can be characterized (more details in section 2.5) and edge coupler loss per facet can be subsequently extracted.

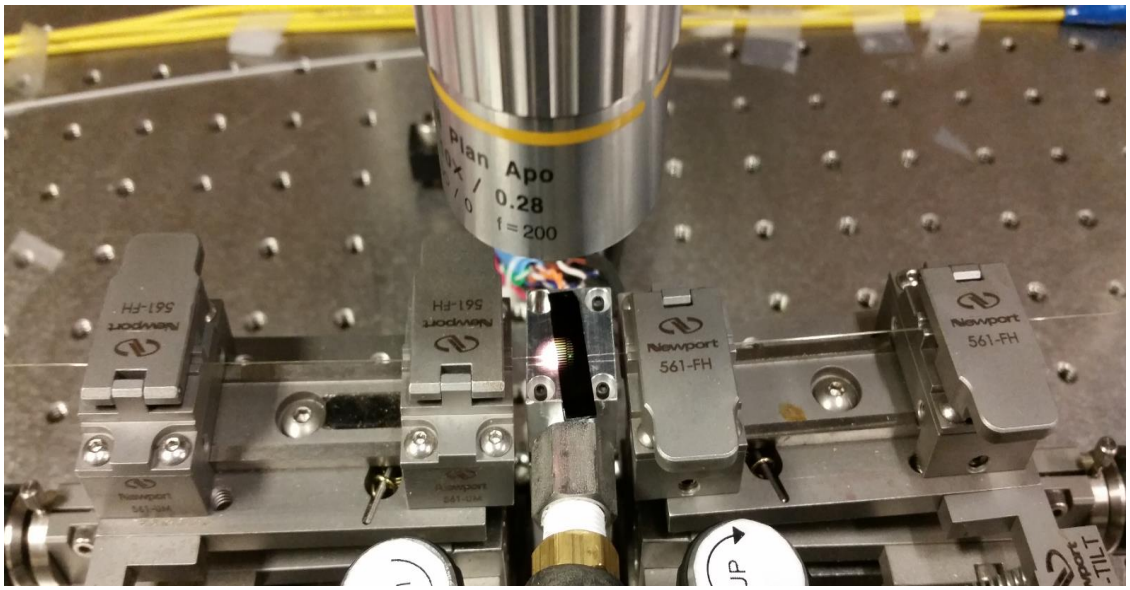


Figure 2.10 Measurement setup for edge coupler chip

During measurement, polarization of input beam can be adjusted by tuning the polarization rotator and output power is record by power meter at 1550 nm wavelength. Normally speaking by tuning the polarizations a maximum and minimum coupling loss obtained and one of the extreme value is for pure TE and another for TM. With some testing devices (cascaded sharp bend with 5 μm radius), TM shall suffer much higher bending loss compared with TE hence at maximum coupling loss polarization is treated as TM. When pure TE or TM polarization is found, fiber is laterally shifted to the neighboring device (without cascaded S bend) for measurement. This may not be a quite rigorous method to distinguish polarizations because it assumes minor lateral movement of fiber does not alter polarization. An alternative method based on ring resonator is used at other edge coupler chips (more details in section 2.5).

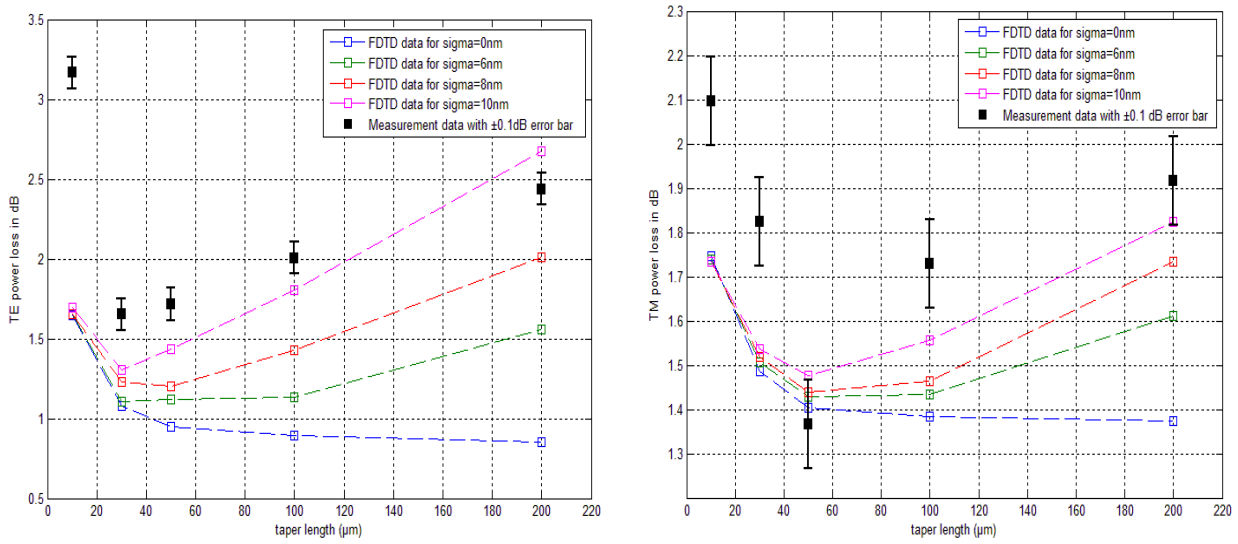


Figure 2.11 (a) TE and (b)TM coupling loss of linear inverse taper from 3D FDTD and measurement for 180 nm tip width and various taper length at 1550 nm wavelength [19]

Fig.2.11 shows the simulation as well as measurement results for both polarizations. Simulation shows at 1550 nm wavelength, when no roughness is involved, coupling loss at both polarizations decreases as taper length increases. As σ_{rms} gradually increases, the trend will be reversed at certain taper length and the turning point can be regarded as optimized taper length. At optimized taper length, mode transition loss and scattering loss from rough sidewalls reach the best tradeoff. Experimental result demonstrated such similar trend and best TE loss of 1.6 dB occurred at 30 μm long taper whereas best TM of 1.4 dB is found at 50 μm long taper. Simulation also reveals that TE mode suffers high scattering loss compared with TM. This can be explained by the fact that TE mode has higher power concentration on vertical sidewalls than that of TM. Since TE is more sensitive to sidewall roughness, taper optimizes at shorter length for TE compared with TM (in which case scattering loss take longer length to dominate).

Instead of the most traditional SOI inverse taper, inverse tapered with cantilever structure is also investigated as requested by Furturewei Technologies Inc. Cantilever structure is initially reported in 2009 [36] and 2012 [37], which aims to improve tip coupling efficiency and reduce leakage towards Si substrate. The schematic of cantilever structure is shown in Fig.2.12 where fiber is first coupled to a square cross-section SiO_2 waveguide cantilever, followed by Si taper to transform power into strip waveguide. Cantilever is formed by etching away the Si substrate, which not only

reduce leakage but also allow SiO_2 to trap beam by total internal reflection. In such design cross-section of cantilever should optimize mode overlap with input mode profile while Si tip width should be kept narrow.

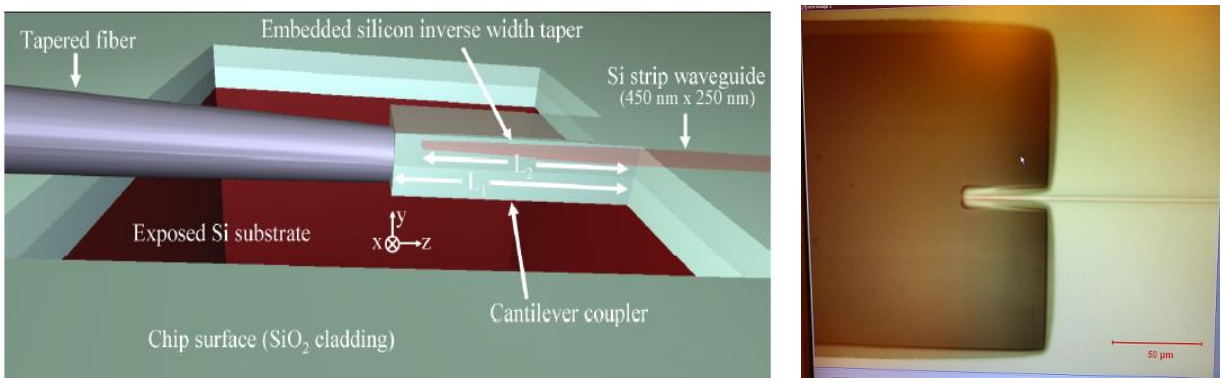


Figure 2.12 (a) schematic of inverse taper with cantilever [37] (b) optical microscope top view of cantilever structure fabricated in our group

Our group has fabricated several chips of cantilever structure and measured the coupling loss using lensed fiber. Since there's no polarization detection device on this chip, we only tune the polarizations to find the maximum and minimum coupling loss.

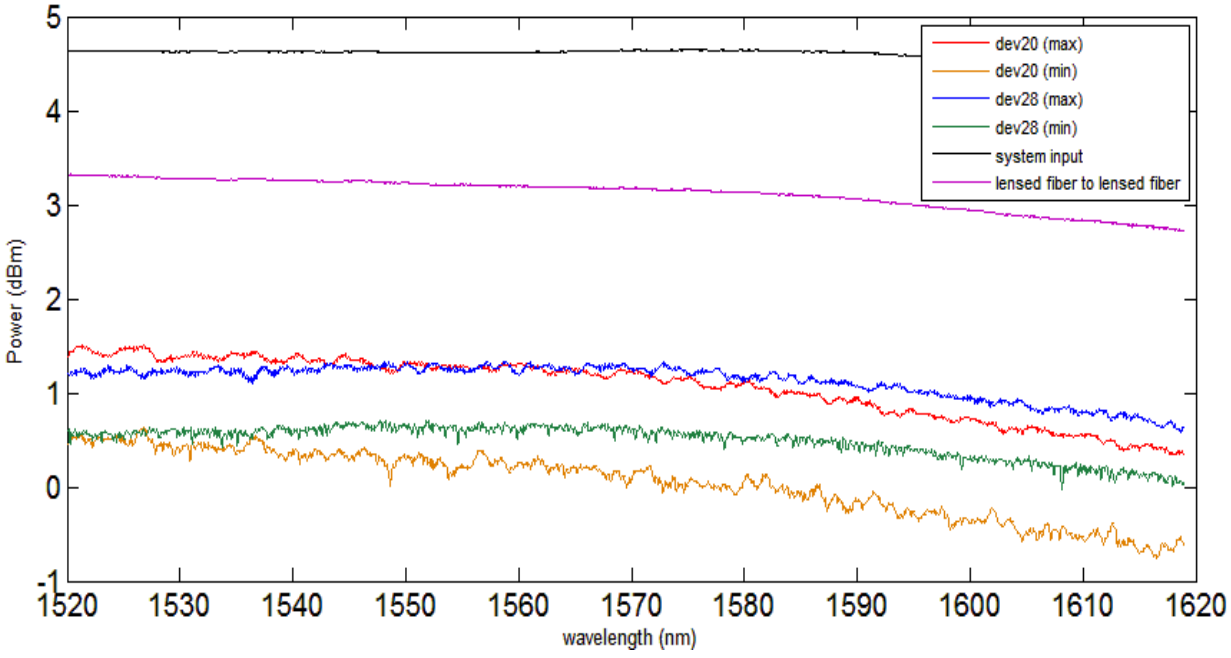


Figure 2.13 Power spectrum measurement with lensed fiber

As shown in Fig.2.13 (lensed) fiber-to-fiber loss is first characterized as reference. Then measurement spectrum through the chip is taken and difference between them is regarded as twice the coupling loss plus some bending propagation loss (relatively small for SOI waveguide). After further characterization and calculation, coupling loss spectrum in dB/facet is shown in Fig.2.14. In experiment we have demonstrated a cantilever coupling with 1-1.4 dB coupling loss over 100 nm bandwidth. With sidewall roughness considerations, we may predict that 1 dB loss is for TM and 1.4 dB loss is for TE.

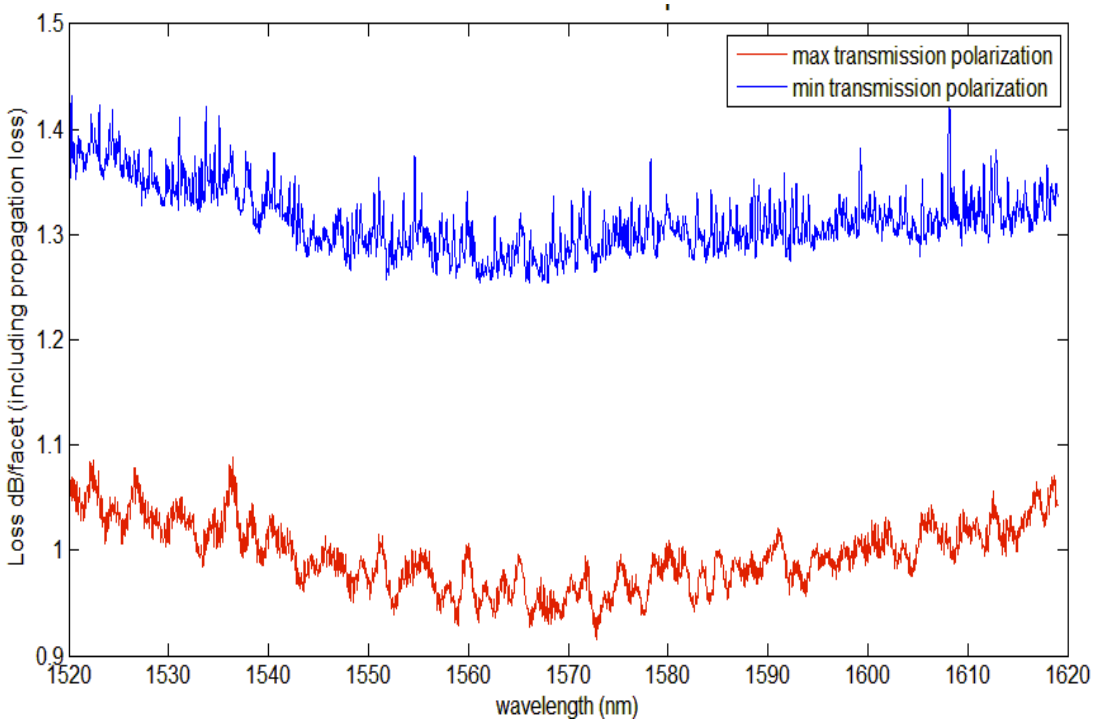


Figure 2.14 Best performing device loss measured with lensed fiber

Although cantilever edge coupler shows good coupling performance, it's worth mentioning that industry does not prefer the suspended cantilever structure due to weak mechanical reliability. The advantage of cantilever structure is to eliminate power leakage towards Si substrate while this is not the only option. Usage of intermediate cladded waveguide or thicker BOX wafer could also reduce leakage, although those solutions also have their only drawbacks. With intermediate cladded waveguide unfavorable high order mode can be easily excited while thicker BOX SOI wafer is difficult to dissipate heat. More detailed analysis about those techniques will be disused in the following sections.

2.3 Inverse taper cladded with polymer waveguide

Another traditional edge coupler is to deploy polymer as intermediate cladded waveguide within which Si taper is embedded. Although not quite preferred by industry, such design allows large input MFD to be used without necessity to remove Si substrate. As requested by Futurewei Technologies Inc, SU8 cladded edge coupler has been investigated by our group. To start with, polymer waveguide is designed for input MFD = 8 μm, which requires a 10 μm side length SU8 waveguide.

As Si taper width expands, mode will be gradually transformed into Si waveguide. It has been reported that a nonlinear taper shape can improve mode conversion efficiency [16] and our group is trying to follow such guideline for further explorations. As illustrated in Fig.2.15 (b), there exists a "window" of width expansion where mode area change is the steepest. From mode solver we can tell that 90 nm – 150 nm can be treated as TM window and 150 nm – 200 nm as TE window.

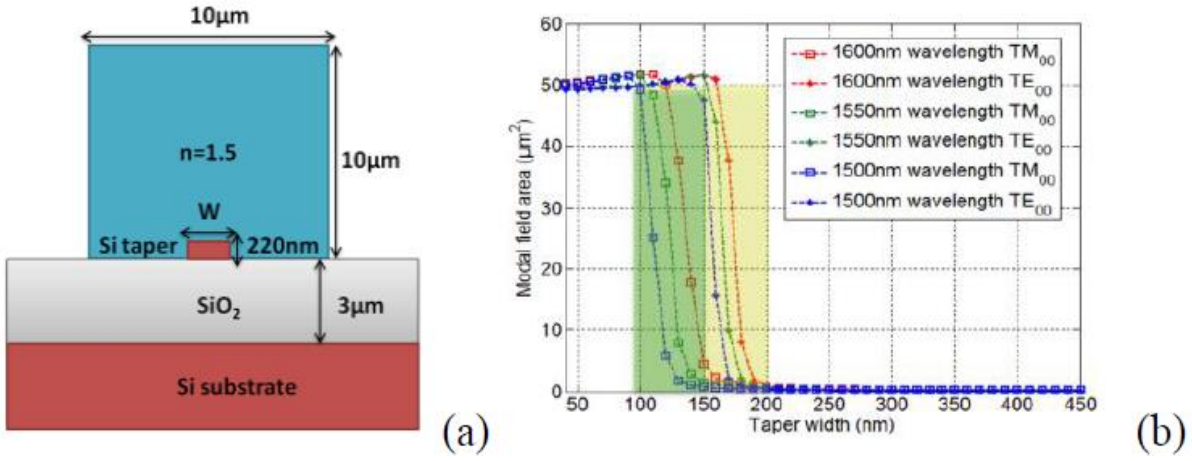


Figure 2.15 (a) cross-section of SU8 cladded edge coupler (b) Mode transition window for TE_{00} and TM_{00} (yellow and green shaped region) at 1500 nm, 1550 nm and 1600 nm wavelength

The physics behind mode transition window is at certain geometry polymer waveguide mode and Si waveguide mode becomes hybridized (mode crossing due to effective index proximity). Hence as beam propagating along such SU8 cladded taper, TM mode will couple into Si layer before TE does and TM theoretically suffer lower mode transition loss for wider transition window. Since majority of mode transformation is accomplished in such narrow window (90 nm - 200 nm), it's reasonable to design the taper such that majority of taper length is assigned to where mode transition is most dramatic.

Therefore, a 3 stage piecewise-linear taper is designed where both stage 1 (width 50 nm – 90 nm) and stage 3 (width 200 nm – 450 nm) are set to be 50 µm long and stage 2 (width 90 nm – 200 nm) is scanned. To calculate the edge coupler loss for such huge device, Eigen-Mode Expansion (EME) method is used to calculate the mode transition loss at single wavelength. EME scanning of L2 indicates L2 beyond 1.5 mm can ensure less than 0.2 dB mode transition loss. Nevertheless, for such long taper scattering loss due to sidewall roughness cannot be ignored. However, there is no possibility for direction FDTD simulation at high mesh accuracy for such long device with rough sidewalls. Here we propose a staircase approximation method to estimate accumulated scattering loss due to sidewall roughness without brute-force calculating entire device using FDTD.

To develop staircase approximation model, FDTD simulation of SU8 cladded Si taper with 10 nm σ_{rms} is done. To save computation domain, a linear inverse taper cladded by 2 µm by 2 µm SU8 waveguide is used as shown in Fig.2.16. By direct calculation of tapers at various taper length, scattering loss in dB can be extracted at 1550 nm wavelength. Fig.2.17 (a) shows the minimum TE loss of 0.4 dB can be obtain at 50 µm long taper when roughness is included. It's noticeable that scattering loss in dB almost scales up linearly with taper length.

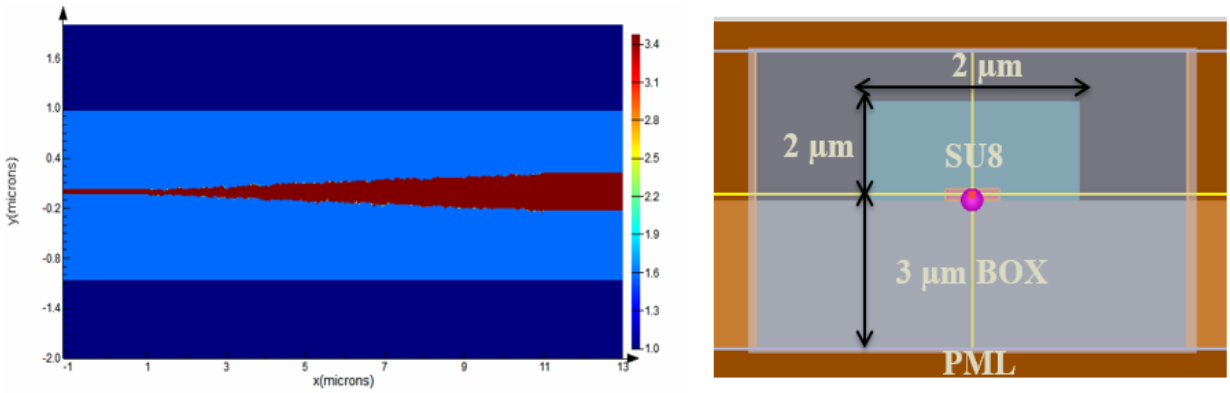


Figure 2.16 (a) FDTD refractive index monitor (b) device cross-section

The staircasing approximation starts by assuming the structure can be treated as several uniform cross-sections. When scattering loss of each cross-section is obtained, total scattering loss accumulation is just the sum of all discretized steps. Hence in FDTD, scattering loss of cross-section with various taper width (100 nm, 150 nm, 200 nm …) are calculated (as dB loss per µm) first. Then tapered structure is interpolated at constant step (1 µm for example) to extract the corresponding taper width. Eventually use the interpolated taper width per step is used to sample

the spline fitted curve in Fig.2.17 (b) and integration of all loss samples gives the accumulated scattering loss. The loss estimated from staircasing approximation agrees quite well with direct FDTD simulation. Hence for massive structure which cannot be simulated by FDTD, scattering loss can still be determined by such technique.

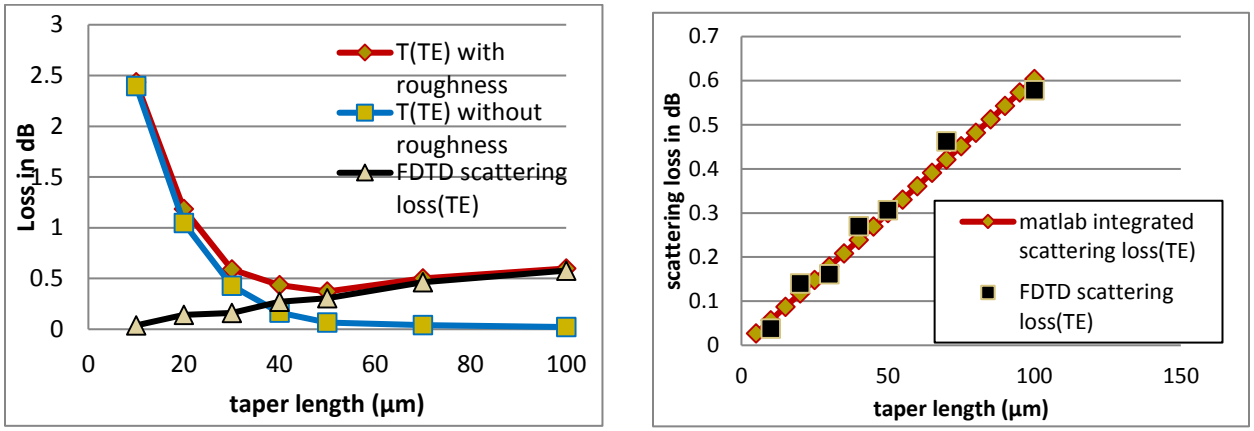


Figure 2.17 (a) 3D FDTD calculated power loss at 1550 nm wavelength for various taper length (b) Loss comparison between direct FDTD calculation and staircasing approximation on a linear taper

Staircase approximation is also applied to nonlinear Si taper with 10 μm by 10 μm SU8 cladded waveguide. Scattering loss of various cross-sections is firstly calculated then sampled by constant step. From Fig.2.18 (a) we can conclude that there is always a scattering loss peak regime and TE suffers much higher scattering loss compared with TM. The calculated scattering loss trend agrees reasonably well with T. Barwicz's analytic model [38].

The location of scattering loss spike appears after TE mode transition window, meaning scattering loss start to rise only after the mode transformation is almost complete. Once mode is sucked into Si core, there is a window of Si width that power concentration on vertical sidewall reaches peak, which causes the spike of scattering loss. This means a nonlinear taper with long L2 but short L3 can strong suppress scattering loss by passing through the high scattering regime quickly. Although nonlinear taper shape has already been proposed by Q. Xu [26] to reduce mode transition loss, here we brought new insight to such design as it can further suppress roughness-induced scattering loss. In Fig.2.18 (b), TE loss at 1550 nm is scanned with L2 given L1 and L3 both at 50 μm. Result shows that roughly at 1000 μm L2 (1.1 mm total device length), optimized TE loss ~

1.4 dB can be obtained. If a 1.1 mm long linear taper is used, TE loss can rise to more than 10 dB due to increased mode transition loss as well as scattering loss.

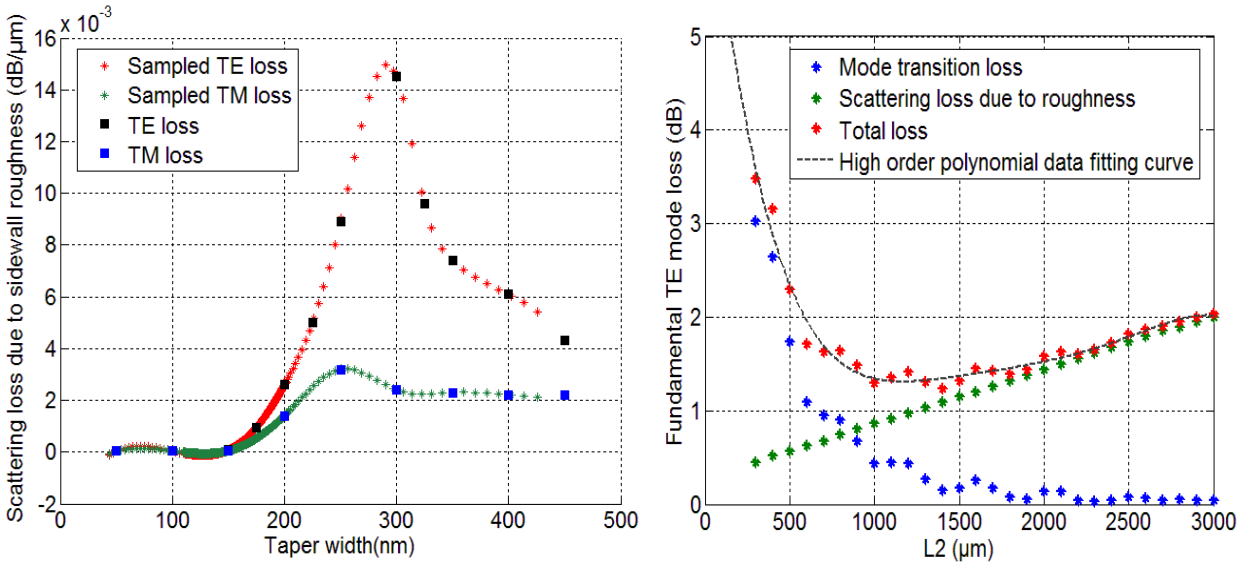


Figure 2.18 (a) Staircasing approximation of scattering loss of piecewise-linear taper with 10 μm by 10 μm SU8 cladded waveguide (b) Calculated TE loss as function of L2

Our group tried to fabricate such design for validation with 6 μm MFD high NA Nufern fibers, hence SU8 cross-section was adjusted as 8.5 μm by 8.5 μm. An example of layout used for Ebeam is shown in Fig.2.19 where substantially longer SU8 waveguide is defined for convenience edge definition (manual cleavage).

On the same layout, both linear and nonlinear inverse tapers are included and the Si taper length is designed within 1.3 mm (size of one Ebeam writing field) to avoid stitching error on Si taper structure. As shown in Fig.2.19 the main structure in the middle is restricted within one row of square cells (field) to avoid stagnation error on Si structure. Long SU8 waveguides extend beyond several fields but due to large mode size stitching error is not going to severely increase propagation loss. Fig.2.20 shows the chip fabricated by our group as well as its SEM cross-section image. Without upper cladding protection, SU8 waveguide is quite fragile even after annealing and during measurement some SU8 waveguides are indeed damaged. This also explains why polymer cladded inverse taper is an unfavorable option to industry.

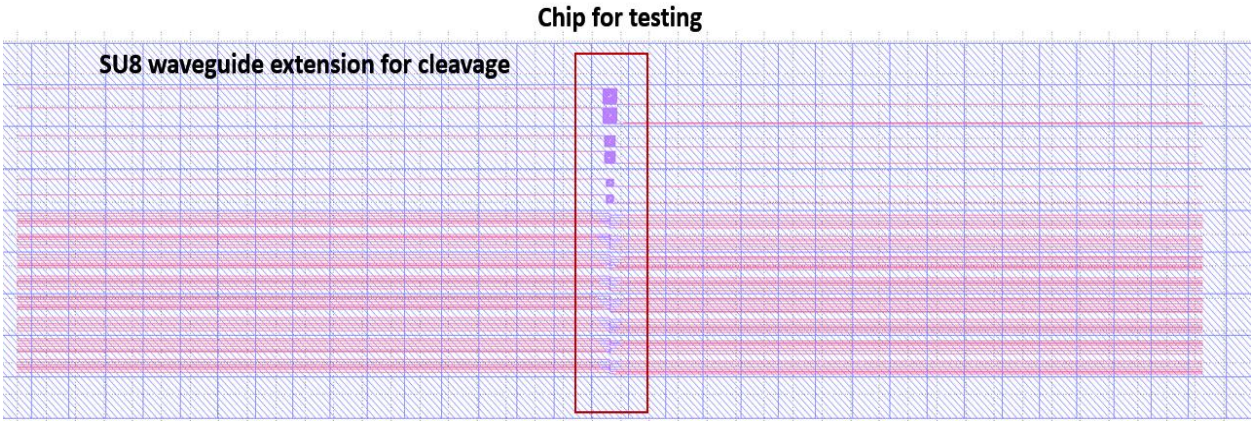


Figure 2.19 Layout for SU8 cladded inverse taper (compiled by layout editor)

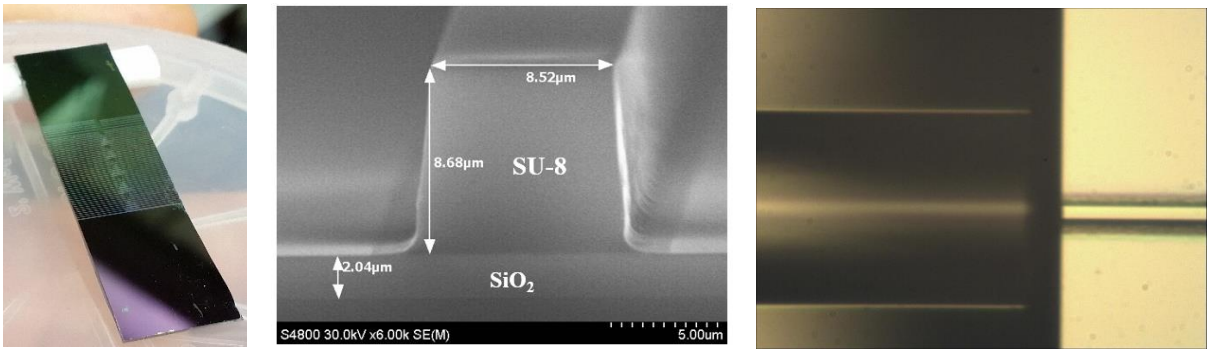


Figure 2.20 (left) photo of SU8 cladded inverse taper chip (middle) SEM image of cross-section of SU8 waveguide (right) measurement setup using 6 μm MFD high NA fiber (courtesy of Dr. Kyunghun Han and Dr. Ben Niu)

Measurement is done with the same procedure that starting with fiber-to-fiber test in air then measure the power through chip. Since SU8 (~ 1 cm long) absorption must be considered, a reference value of 2 dB/cm loss [39][40] is taken. From measurement linear shape taper leads to tremendous loss as predicted whereas nonlinear taper has achieved a narrowband low loss spectrum. With measured the spectrum in Fig.2.21 and Fig.2.22, we extracted the minimum coupling loss as 1.87 dB/facet. The polarization dependent loss is quite small but low coupling is only obtained over a narrow spectrum.

The reason for such narrow bandwidth is still unknown but it's suspected that non-vertical SU8 cleavage has caused some high order modes excitation in SU8 waveguide and in theory high order mode power coupling to Si taper is very inefficient. Another speculation is that due to fabrication

or layout fracturing error the middle long taper may become close to a uniform width centered at mode crossing. If that is the case, the mode conversion appears in the form of mode beating where certain wavelength gives strongest beat (see section 3.4). For now, we have not confirmed the underlying cause for such narrowband transmission, but we may in future keep investigate this problem to improve spectral bandwidth.

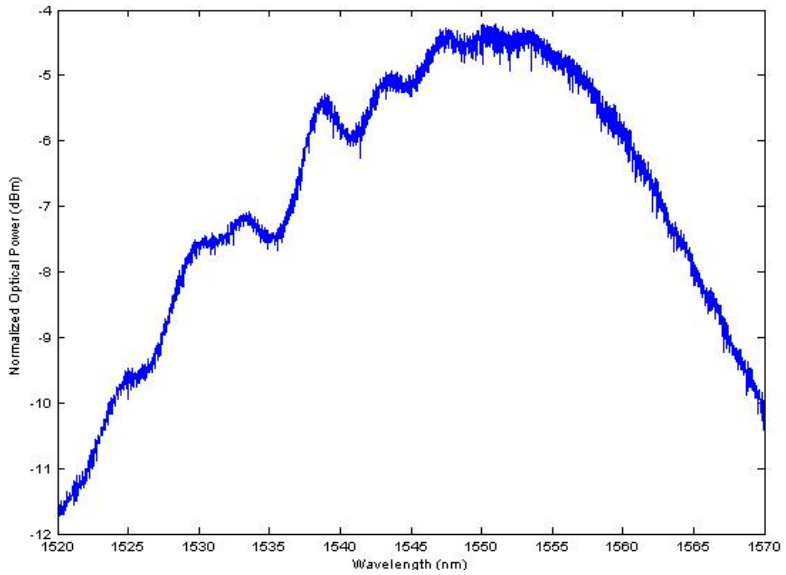


Figure 2.21 Measured power spectrum at polarization with min transmission at 1550 nm (assume TE)

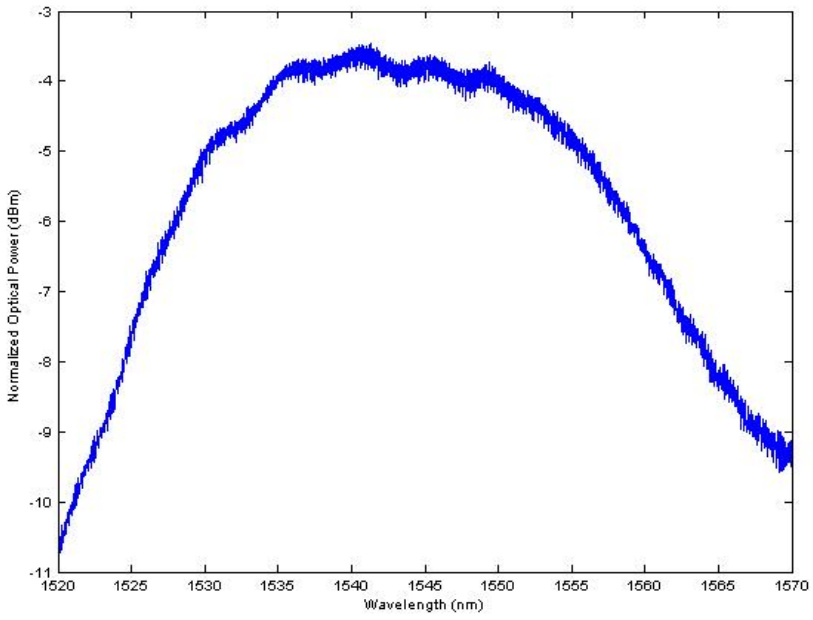


Figure 2.22 Measured power spectrum at polarization with min transmission at 1550 nm (assume TM)

2.4 Multilayer Si/SiN hybrid edge coupler with intermediate coupling steps

Although lensed fiber or high NA fiber has been widely used among researchers for efficient edge coupling, industry is still eager to see a CMOS compatible solution that allow efficient coupling from SMF-28 fiber. Polymer waveguide cladded can theoretically become one solution because polymer waveguide guidance will prevent power leakage towards Si substrate. However, our experimental demonstration does not give quite broadband high coupling efficiency and previously reported designs based on polymer waveguides are not targeted at large mode-size input. In addition, polymer waveguide supports multiple modes hence initial coupling into high-order modes cannot be efficiently harvested. More importantly polymer is not a reliable material favored by industry due to its optical absorption, insufficient mechanical strength as well as CMOS incompatibility.

Alternatively, IBM researchers developed metamaterial edge coupler for SMF-28 fiber at O band. [29] To reduce power leakage from large-size input mode, Si substrate is etched away and replaced with index matching material. Metamaterial converter is used to reduce polarization dependent coupling loss and converter is suspended over the V-groove. Nonetheless, this is not a CMOS-compatible solution, even though measurement at O band from SMF-28 gives 1.5 dB loss/facet.

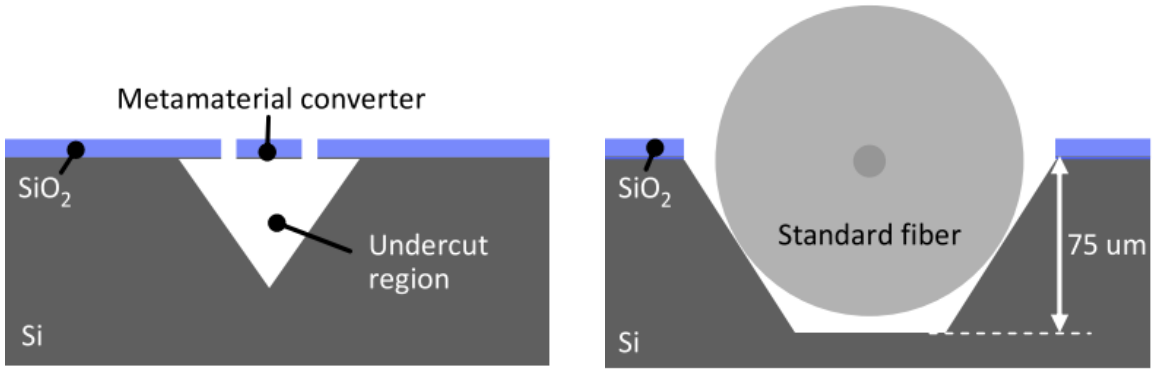


Figure 2.23 IBM's edge coupler solution for SMF-28 fiber at O band

Here we purpose a multilayer Si/Si_3N_4 structure that follows standard CMOS process and allow high efficiency power coupling from SMF-28 fiber over broad bandwidth. Fig.2.24 shows the one of such design that with multilayers of nitride (300 nm thickness for CMOS compatibility) on top of Si layer. The basic idea is input beam can be trapped (by top layer nitride tips) at height above Si layer first to avoid immediate leakage towards substrate, then followed by remaining structure

to couple power down to Si layer. Mode can be vertically dragged down by tapering out the existing confinement structure meanwhile the bottom taper becomes wider to suck the radiating power from top layer.

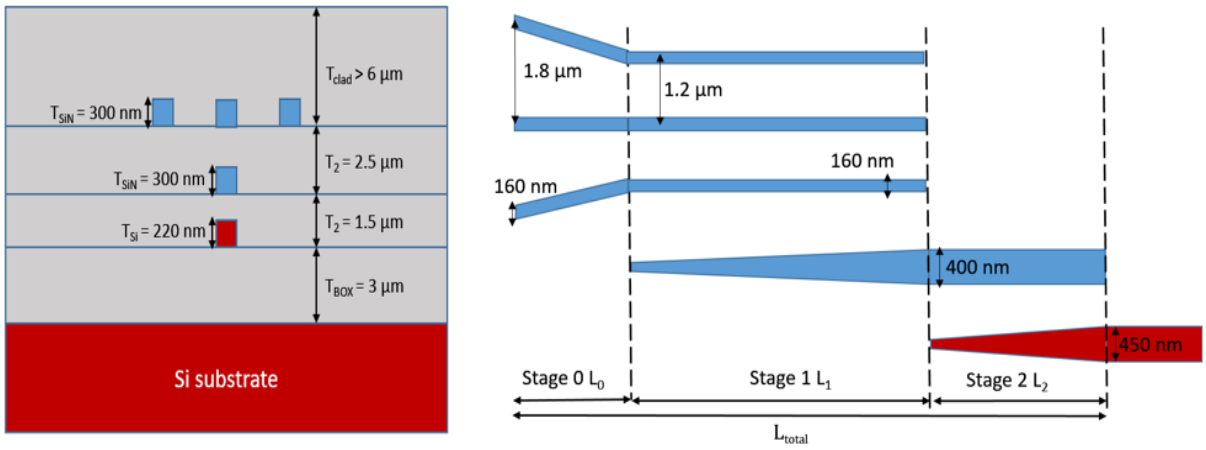


Figure 2.24 Cross-section view and top view of multilayer Si/Si_3N_4 edge coupler

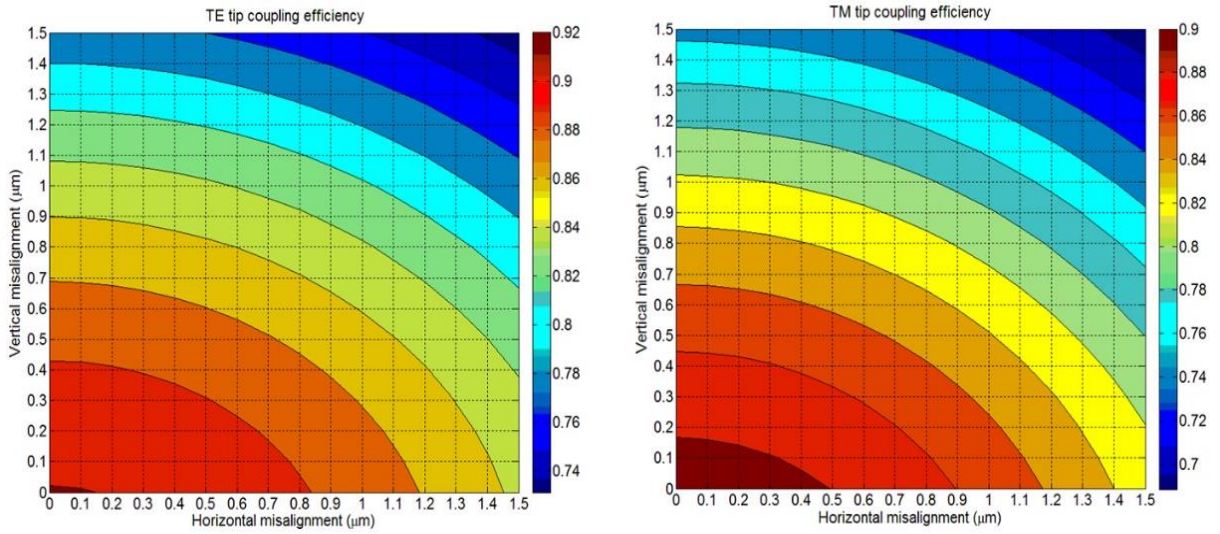


Figure 2.25 Tip coupling efficiency at 1550 nm wavelength under misalignment

The triple Si_3N_4 tip is the interface that fiber mode first couples to hence it's critical to minimize the mode mismatch loss. With similar ide to trident edge coupler [21], supermode supported by multiple tips can match well with input fiber mode if properly designed. Assuming all three tapers share the same height (300 nm) and tip width, mode overlap between fundamental mode at triple

tips with fiber mode (Gaussian mode with MFD = 10 μm and Neff = 1.44) is calculated. With sweeping tip width and center-to-center spacing between adjacent tips, 160 nm tip width and 1.8 μm spacing is chosen. Such optimized geometry can achieve 92.3% tip coupling for TE and 90.5%. As shown in Fig.2.25, even with 1.5 μm misalignment in both x and y directions over 70% tip coupling efficiency can be maintained.

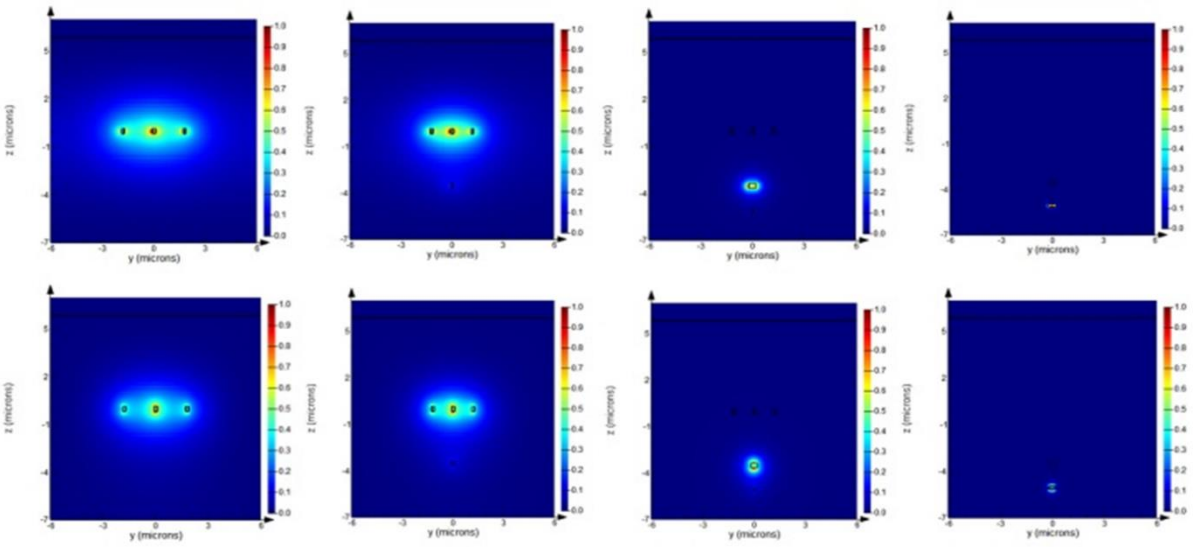


Figure 2.26 (top row) TE and (bottom row) TM mode |E| profile along propagation directions

Fig.2.24 briefly demonstrate our designed structure. Immediately after beam coupling to three parallel nitride tips, with a short L_0 (~ 20 μm), adjacent tip spacing is reduced from 1.8 μm to 1.2 μm to enhance confinement but almost negligible transition loss. Then beam trapped at top nitride layer is coupled down to intermediate nitride layer, after which Si taper starts to suck the power from intermediate layer. Mode evaluation profile of our final structure can be briefly illustrated in Fig.2.26. The input beam first couple to three parallel nitride tips followed by a short section to reduce tip spacing for better confinement. After that intermediate nitride taper starts to appear which expands wider to take the power vertically down to its layer. Ultimately Si taper appears to take power down to Si layer.

The intermediate nitride layer is deployed as a stepping stone for mode coupling from top to bottom. Intermediate nitride layer introduces two interfaces: L_0/L_1 and L_1/L_2. Hence taper tip width and ending width should be carefully designed to reduce mode mismatch losses at both interfaces. To reduce mode mismatch loss at L_1/L_2 interface, solution can be either widening the Si_3N_4 waveguide

width on top of Si taper or placing intermediate layer further away from Si layer. First solution unavoidably increases mode transition loss for intermediate layer while the later one makes evanescent coupling into Si taper even more challenging. As TM mode is less well confined, it obtains better coupling efficiency as well as higher leakage and mode mismatch loss at interfaces.

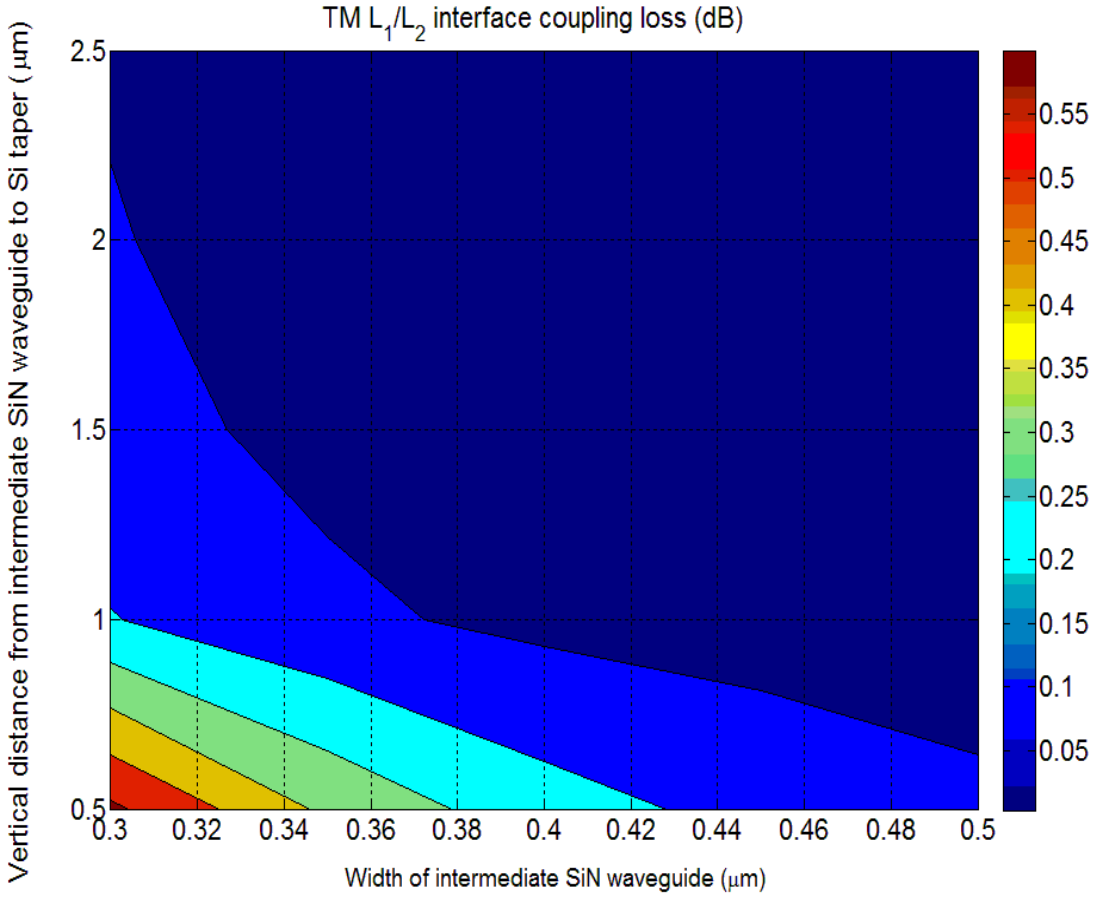


Figure 2.27 TM mode mismatch loss at L_1/L_2 interface

In Fig.2.27, TM mode mismatch loss at L_1/L_2 is calculated for various nitride waveguide width and vertical position. Vertical position of Si_3N_4 layer plays an important role such that if close to the top layer, coupling efficiency for stage 1 is boosted at costs of stage 2 and vice versa. Design guidelines prefer that silicon taper should be made short to reduce scattering loss while a long nitride taper does not incur considerable scattering due to low index contrast [35]. As a result, 400 nm wide waveguide at 1.5 μm distance on top of Si taper is a decent choice to ensure less than 0.05 dB TM mode mismatch loss at L_1/L_2 interface, which is shown in Fig.2.27. With similar

process, 100 nm is chosen as intermediate Si_3N_4 taper tip width which leads to 0.06 dB TM mode mismatch loss.

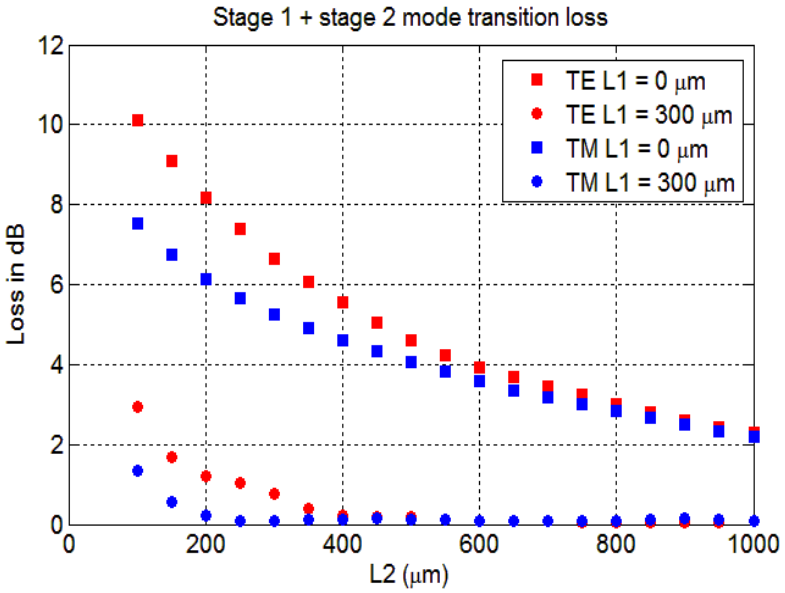


Figure 2.28 Mode conversion efficiency for stage 1 Si_3N_4 taper

Fig.2.28 shows the mode conversion (transition) loss vs. L_2 from EME calculation at 1550 nm wavelength, assuming Si taper is linear. Simulation shows without intermediate coupling step (L_1 = 0 μm), even 1 mm long Si taper cannot suppress mode transition loss within 2 dB. As a comparison, with 300 μm long intermediate nitride taper, merely 400 μm Si taper is needed to achieve < 0.2 dB coupling loss for both polarizations.

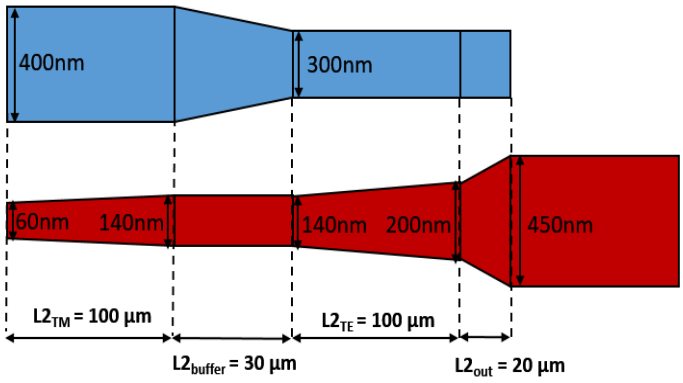


Figure 2.29 Top view of a piecewise linear Si taper with tapered intermediate nitride waveguide

To further shorten Si taper length, piecewise linear Si taper (Fig.2.29) can be designed with similar procedure in section 2.3. Here two polarization requires different treatments because TM suffers higher leakage while TE suffer higher scattering. In our design, the mode transition window is further divided into TM (80 nm -140 nm) and TE (140 nm – 200 nm) windows. As beam propagate along the intermediate nitride waveguide, TM mode couples to Si taper first with high efficiency then followed by the inefficient TE coupling once Si width enters the TE window. As a result, to balance two polarizations, the suspended nitride waveguide is tapered such that wider at TM window to reduce leakage while narrower at TE window to boost coupling efficiency (at cost of higher leakage).

With given parameters in Fig.2.29 and 60 nm Si tip width, over 98% mode conversion efficiency can be obtained for both polarizations according to EME calculation. With semi-vectorial BPM simulation from Rsoft, 94% stage 2 efficiency can be obtained for both polarizations while the 4% deviation can be explained by difference between full and semi-vectorial calculation. As shown in Fig.2.30, majority of mode coupling for TM mode is coupled down to Si layer earlier than TE since TM mode transition window appears before TE window.

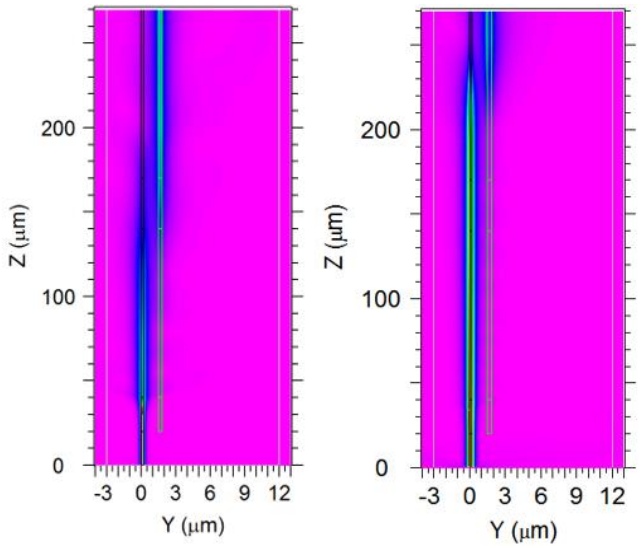


Figure 2.30 TE (left) and TM (right) major E field component amplitude along propagation in BPM simulation (source injected from Si waveguide Z = 0 μm)

While nitride stage leads to negligible scattering loss, Si stage scattering must be considered due to high index contrast. The total accumulated scattering loss can be approximated by FDTD

simulations, which is sampled along the structure at step of 20 μm. Then the total loss can be sampled and interpolated to 1 sample per μm and summation of all sampled loss gives the accumulated scattering loss. Assuming σ_{rms} = 5 nm and L_c = 50 nm as roughness parameters, estimated scattering loss is around 0.1 dB for TE and 0.02 dB for TM. Low scattering loss is incurred because the most lossy regime is quickly passed through.

Leakage loss can also be estimated using staircase approximation, with propagation loss calculated at each step along the entire structure as shown in Fig.2.31. From very beginning triple tips with 160 nm width gives weaker TE confinement than TM hence initial TE leakage is higher. However, stage 0 and stage 1, TE mode becomes even better confined than TM hence leakage loss quickly falls below TM curve. Without special treatment at stage 2, TM leakage becomes comparable to TE and early appearance of leakage TM spike than TE indeed proves TM window is passed before TE window. Assuming mode power is tracked at the fundamental mode along the structure, leakage loss is estimated as 0.13 dB for TM and 0.15 dB for TE.

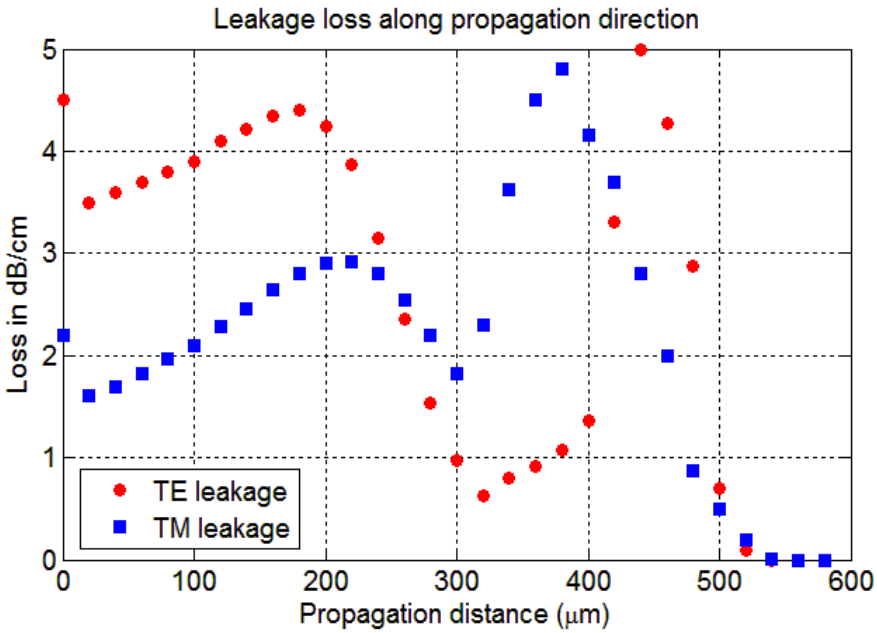


Figure 2.31 Leakage towards Si substrate along propagation distance

The mode transition loss of the entire structure is shown in Fig.2.32, showing less than 0.35 dB TE and 0.25 dB TM loss over 100 nm bandwidth. Assuming leakage and scattering loss is constant within 100 nm bandwidth, total loss no more than 1 dB for TE and 0.8 dB for TM can be obtained

with 570 μm total device length (L_0 = 20 μm, L_1 = 300 μm and L_2 = 250 μm), including input mode mismatch.

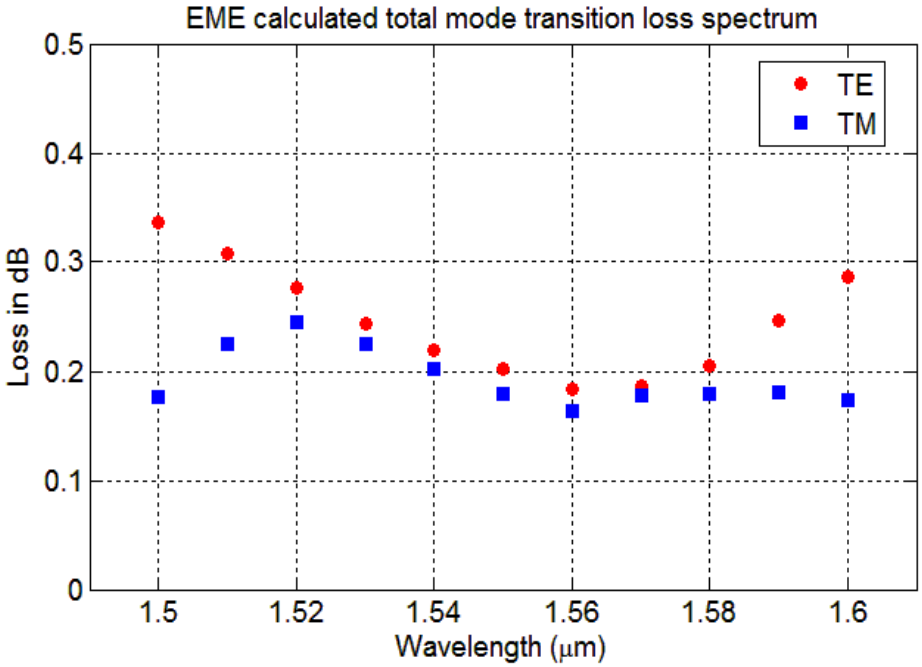


Figure 2.32 EME calculated mode transition loss spectrum for the device

Due to fabrication challenge, this multilayer Si/SiN edge coupler is not fabricated in university cleanroom. With CMOS capability, in future our group may try a fabrication through foundry process. Si/SiN hybrid edge coupler design contributes to the first patent application with exclusive license taken by Futurewei Technologies Inc.

2.5 SOI meta-material edge coupler

Conventional SOI inverse taper is designed with a proper tip width which then gradually expands to single-mode waveguide width (450 nm for example). The tip width is designed to support the fundamental mode with optimal mode overlap to the input beam. The conventional design requires that the proper tip width is chosen but this can be restricted by specific SOI wafer. For instance, on SOI wafer with 220 nm Si thickness, the best overlap to a Gaussian mode with 2.5 μm MFD occurs at 180 nm for TE and 160 nm for TM [18][19]. An edge mode without polarization dependence can only be supported by a square tip [28] (width = thickness = 220 nm) which shows

however poor overlap for both polarizations because mode is too well confined (mode area too small to match 2.5 μm MFD). The birefringence effect of Si waveguide (TE and TM mode area difference) becomes even more significant when trying to match large input MFD beam.

As a solution to eliminate birefringence is by using a square tip at the chip edge. A bilayer SOI inverse taper [41] has been reported to use a square tip with weak confinement in the very beginning, which is eventually merged with top layer as 220 nm thick conventional waveguide. Although this idea is neat, double layer Si definition is somehow challenging during fabrication.

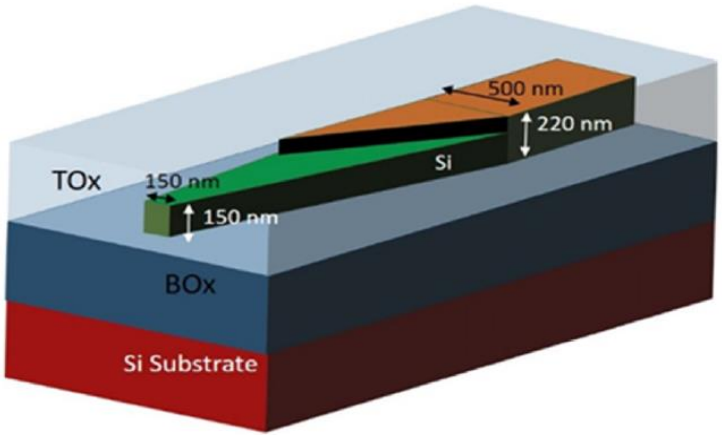


Figure 2.33 SOI bilayer inverse taper [41]

Another interesting solution to reduce polarization dependent loss is meta-material edge coupler, which is firstly reported by IBM researcher at O band [29] followed by P. Cheben at C band [22]. As shown in Fig.2.34, the meta-material edge coupler starts with a tapered subwavelngth grating waveguide (SWG) using a square tip from very beginning. SWG is eventually overwritten by a solid taper on the same layer to ultimately form a conventional strip waveguide. Mode sizes of both polarizations can be equally adjusted by changing the duty cycle of the subwavelength grating waveguide (SWG). Input beam (especially with large MFD) can nicely couple to Bloch mode of SWG without polarization dependence. The Bloch mode however needs to be converted to strip waveguide mode as output. There has been published work [28][29] using a hybrid taper to convert the mode, although it leads to some inevitable mode mismatch loss and fabrication challenge of high resolution Ebeam lithography. As requested by Futurewei Technologies Inc, our group starts to investigate meta-material edge coupler by duplicating the existing results first.

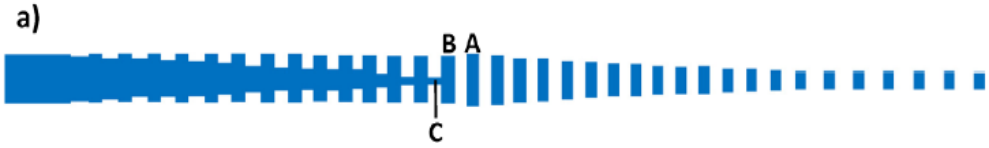


Figure 2.34 Schematic of SOI dielectric meta-material edge coupler reported by P. Cheben [28]

Design phase starts as the SWG design at the edge cross-section, which is shown in Fig.2.35. The device is fabricated on 220 nm Si thickness SOI wafer with 3 μm BOX and top cladding. Tip is designed to support fundamental mode that overlaps nicely to Gaussian mode with 4 μm MFD (from high NA flat fiber). According to convention the tip is designed as "square" while the refractive index is scanned, which yields 2.5 as an optimal index. Assuming input mode is a Gaussian mode with 4 μm MFD in the air, mode overlap including the Fresnel's reflection can reach 92% for TM and 94% for TE. n = 2.5 can be realized at duty cycle X = 53% (Equivalent n = 2.5 = 1.444×(1-X) + 3.44×X hence X = 0.53 = 53%).

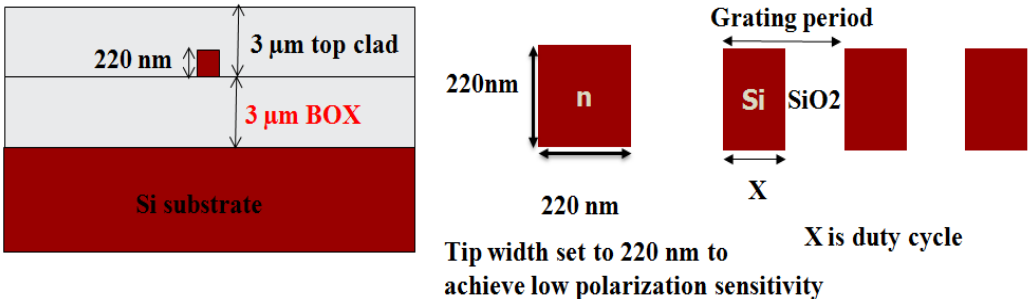


Figure 2.35 SWG design at edge facet

Selection of grating period (Λ) is also critical since SWG allows beam propagation only if the period is small enough. As shown in Fig.2.36 the SWG should safely operates in the rightmost regime for Bloch mode propagation. This requires the Bragg wavelength ($\lambda_{Bragg} = 2 \times n_{eff} \times \Lambda$) far away from operation wavelength. In other words, (1500~1600) / Λ >> 2 × n_{eff} where n_{eff} is the max Block mode index. For example, if the Bloch mode can finally reach the n_{eff} = 2, no more than 375 nm grating period should be used. With reference from P. Chenben, 300 nm grating period is chosen to ensure operation regime to be far away from Bragg reflection zone. This

argument gives several predictions for meta-material edge couplers. Firstly, TE mode will eventually suffer more disruption along propagation than TM as TE will reach higher n_{eff}. Secondly, shorter operation wavelength will be more closely located near Bragg reflection regime hence even smaller grating period may be required (especially for O band application).

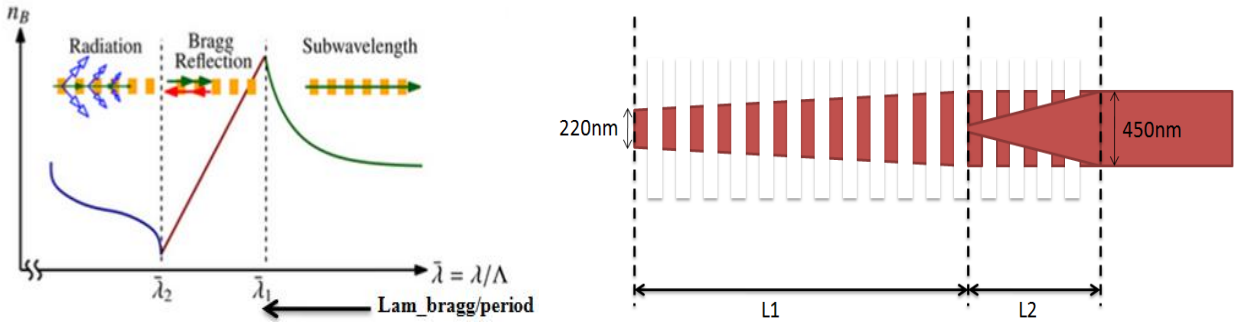


Figure 2.36 (a) Various operation regimes for SWG [43] (b) Simulated real structure top view

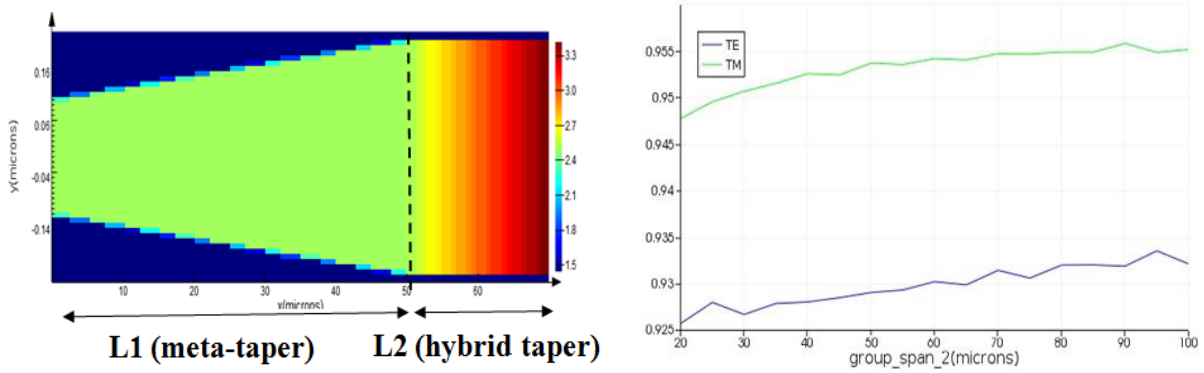


Figure 2.37 (a) EME equivalent structure refractive index top view (b) mode conversion efficiency at 1550 nm wavelength under L1=50 μm and scan L2

Numerical simulation of the physical structure can be calculated with 3D FDTD which is the most reliable but also computation consuming. EME method although being much more efficient, cannot directly be used on SWG since no eigen-mode can be found at "void trenches". Nonetheless an equivalent structure can be calculated where the stage 1 SWG assumes n = 2.5 uniformly. The stage 2 is the hybrid taper that SWG taper is overlapped with an inverse taper to gradually the index to Si. Fig.2.37 shows the structure and its equivalent EME model.

EME calculation shows the upper limit of the mode conversion efficiency (mode transition loss only). Without considering the tip coupling loss as well as sidewall scattering and leakage, EME

can still give an intuitive measure of the taper length required for decent performance. The figure above shows while L1 = 50 μm, scanning L2 is not going to significantly improve the performance. In FDTD simulation, L1 = 50 μm & L2 = 20 μm is chosen given EME performance about 0.6 dB loss as 92% tip coupling efficiency is considered.

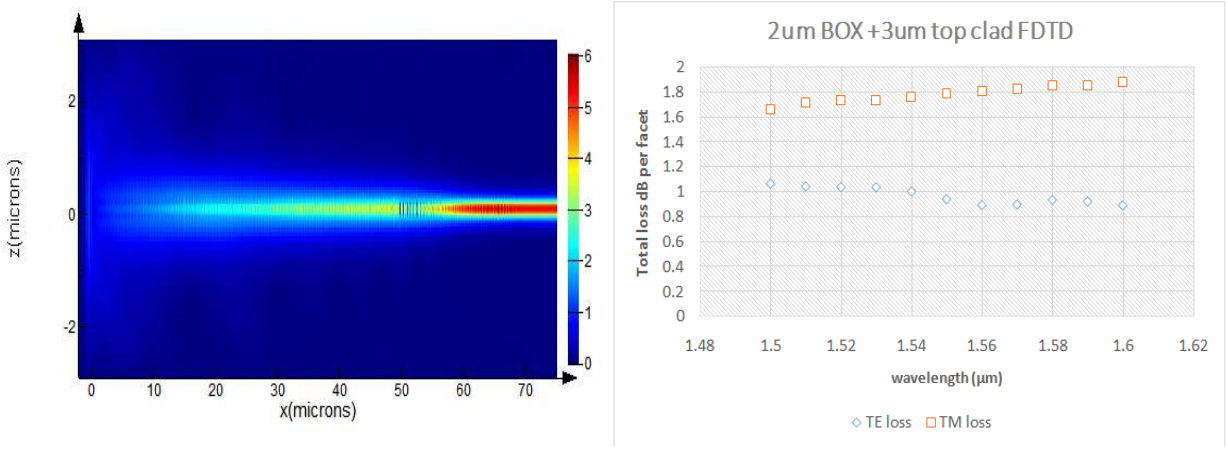


Figure 2.38 (a) 3D FDTD TE simulation |E| profile cut view (b) FDTD calculated transmission spectrum

The realistic structure of metamaterial taper (50nm hybrid taper tip width) is simulated in 3D FDTD, assuming input mode is Gaussian profile with 4 μm and perfectly focused at the Si tip. To include effect of leakage, Si substrate with both 2 μm BOX is used here. Fig.2.38 shows the FDTD results that TM shows 1 dB additional loss compared with TE. The polarization independent loss is caused by the power leakage through 2 μm BOX where TM is leakier due to weaker confinement. Theoretically if 3 μm BOX wafer is used to reduce leakage, TM loss can be brought down to similar level of TE.

Several layouts for are developed by Layout Editor and Fig.2.39 shows the basic overview of an selected layout. On the top of entire layout, sets of spiraled waveguides with 50 μm bending radius and 20 μm waveguide spacing are deployed. All spiral waveguides assume using the same linear SOI inverse taper for coupling. With cut-back method, bending loss at 50 μm bending radius, propagation loss together with inverse taper coupling loss can be characterized.

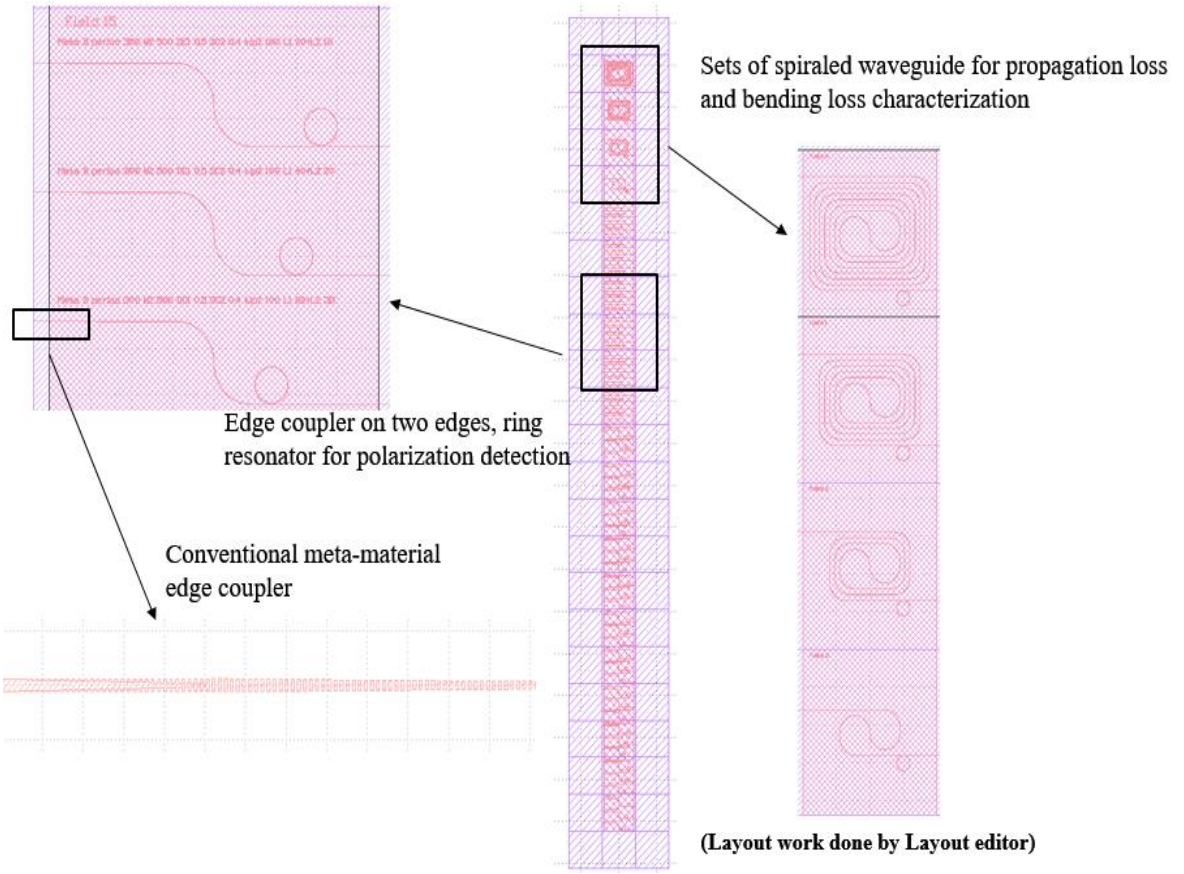


Figure 2.39 Layout for SOI metamaterial edge coupler

The remaining parts of layout are edge coupler with S bend at 50 μm bending radius connected by waveguides and polarization detection (PD) ring. The PD ring will resonate for both TE and TM mode but with different Q factor and extinction ratio. In experiment input beam polarization can be adjusted by polarization rotator to find pure TE or TM polarization by maximizing high Q (TE) or low Q (TM) resonance. On the same layout both SOI linear inverse tapers and meta-material taper exist to compare the efficiency. Due to fabrication concern from industrial point of view, 100 nm hybrid taper width instead of 50 nm (in simulation) is used.

As a discussion about the hybrid taper dimension, larger tip width will intuitively increase mode mismatch loss and increase reflection. Hybrid taper tip dimension can strongly influence its performance because most of power is trapped along the tapered structure.

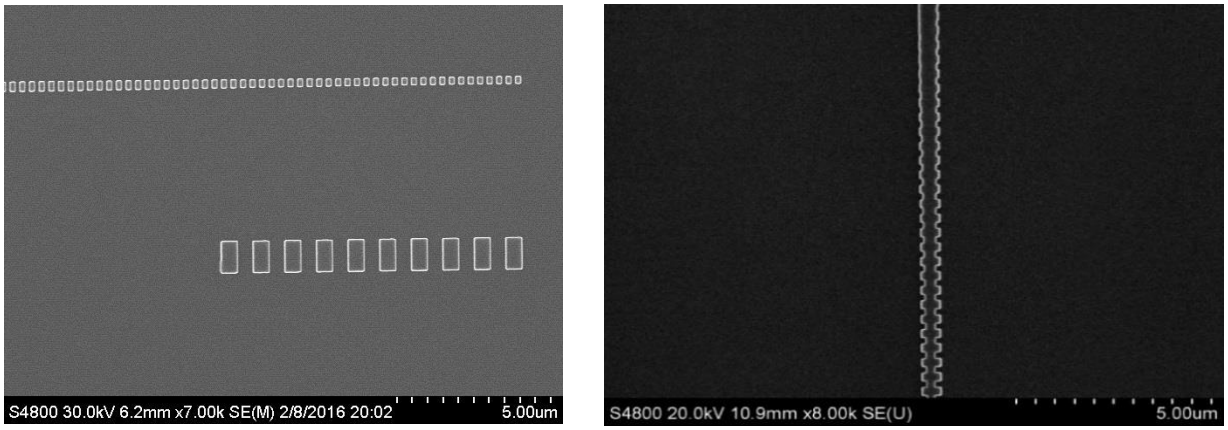


Figure 2.40 SEM image at (left) meta-material edge and junction of hybrid taper (courtesy of Dr. Kyunghun Han)

Our group fabricated the layout with several dose levels in order to compensate inaccuracy of Ebeam exposure. Fig.2.40 shows the SEM image taken before growing top dioxide cladding (LTO). Image shows sharp periodic square shapes after proximity effect correction (PEC) is applied. However, at junction of hybrid taper, image shows ~ 20 nm horizontal offset between solid taper and gratings, which might come from fracturing error.

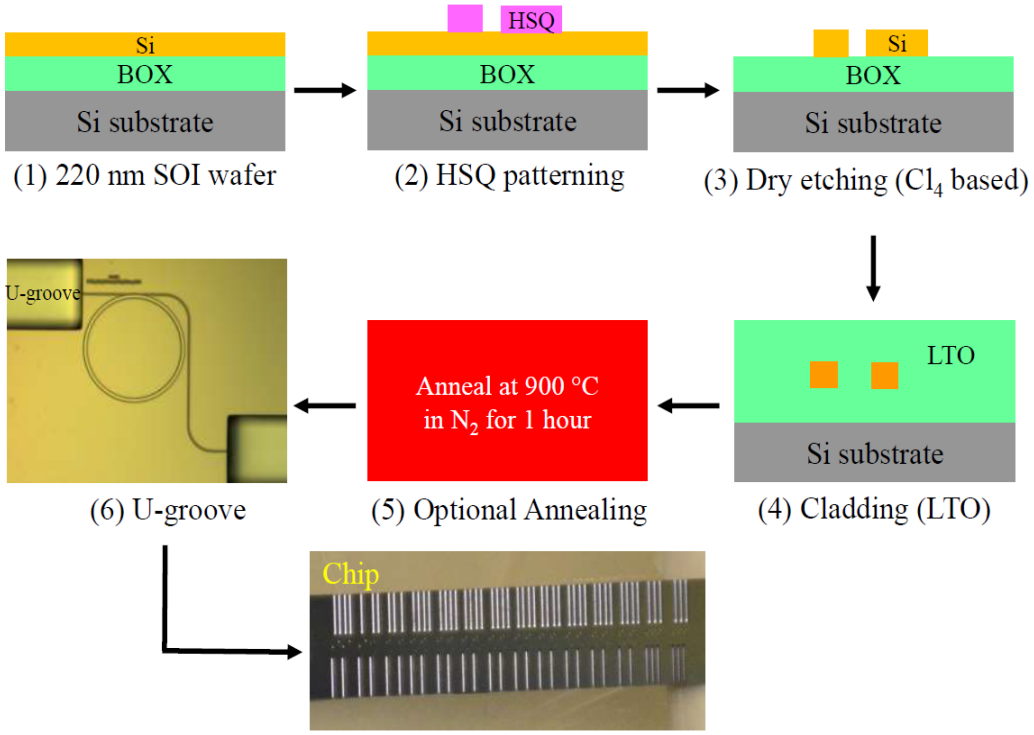


Figure 2.41 Fabrication process flow (with U-groove) on SOI platform (courtesy of Prof. Minghao Qi)

Edge coupler on SOI platform is mostly fabricated via the process flow in Fig.2.41. Initially with Ebeam writing and Panasonic etching, Si structure is defined. Then the chip is oxidized by LTO all the way towards the top cladding thickness. If the chip is going to have U-groove (optional), then optical lithography and etching is taken to define the groove region.

The chip measurement starts from characterizing the input power from high NA flat fiber. UHNA4 from Nufern Inc. is used which yields 4 μm MFD at C band and 3.3 μm MFD at O band [44]. As shown in Fig. 2.42 (a), Nufern claimed 0.2 dB/splicing can be obtained when UHNA4 sliced to SMF28 given specific splicing machine is used. With our splicer in the lab, measured splicing loss turns out to be much higher. As shown in Fig.2.42 (c) splicing machine gives an estimate of 0. 67 dB loss / splicing however this loss estimation is normally used for SMF28 fiber splicing which cannot be trusted. Fig.2.42 (b) briefly shows how we prepare the high NA fiber for optical measurement as well as how to characterize the splicing loss.

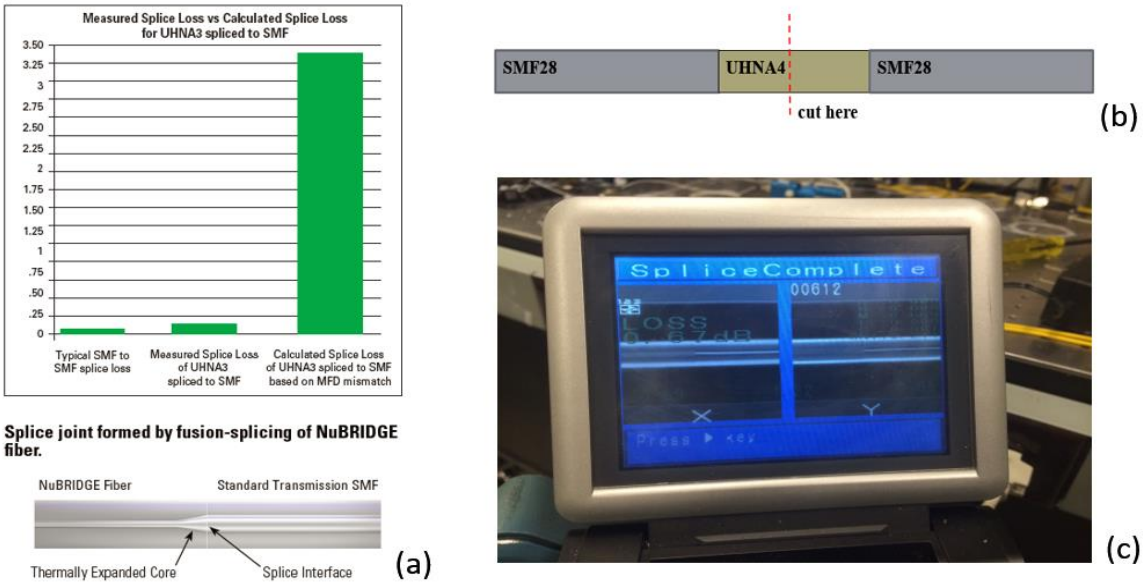


Figure 2.42 (a) Nufern advertised ultra-low loss splicing between SMF28 and high NA fiber [44] (b) SMF-28 and high NA fiber splicing configuration for optical measurement (c) fiber splicing machine with estimated loss in optics lab

First, a power test through standard SMF-28 fiber is done. Then a section of UHNA4 fiber (ultra-high NA with 4 μm MFD) is cut and spliced with SMF-28 fiber on both ends. The total insertion loss of SMF28/UHNA4/SMF28 can be measured and the additional loss (compared with original SMF28) is 2 times the splicing loss. Without Nufern fiber, system input is measured at 3.61 dBm

while with SMF28-Nufern-SMF28, power transmission dropped to 0.76 dBm. This gives on average 1.42 dB per splicing. The splicing loss characterized is noticeably higher than what Nufern company claimed and this is because our splicing machine cannot adiabatically taper the fiber core very well. Splicing loss is not a constant hence each time when using new Nufern fibers, splicing loss is characterized (mostly below 2 dB).

Then the Nufern fiber is cleaved from middle into two pieces and two pieces are used as input and output fiber. Before cutting the Nufern fiber, 0.76 dBm power is measured through SMF28/UHNA4/SMF28. After Nufern fiber is cleaved from middle, a fiber-to-fiber power measurement is done as shown in Fig.2.43 (a). Due to imperfect cleavage (non-vertical cut as shown in the microscope image), Around - 0.2 dBm power is obtained as shown in Fig.2.44 (a) with very little spectral fluctuation. This means Nufern fiber cleavage causes ~ 1 dB extra total power loss (0.5 dB/facet). The cleavage loss can be potentially reduced by better fiber cut with near vertical cleavage.

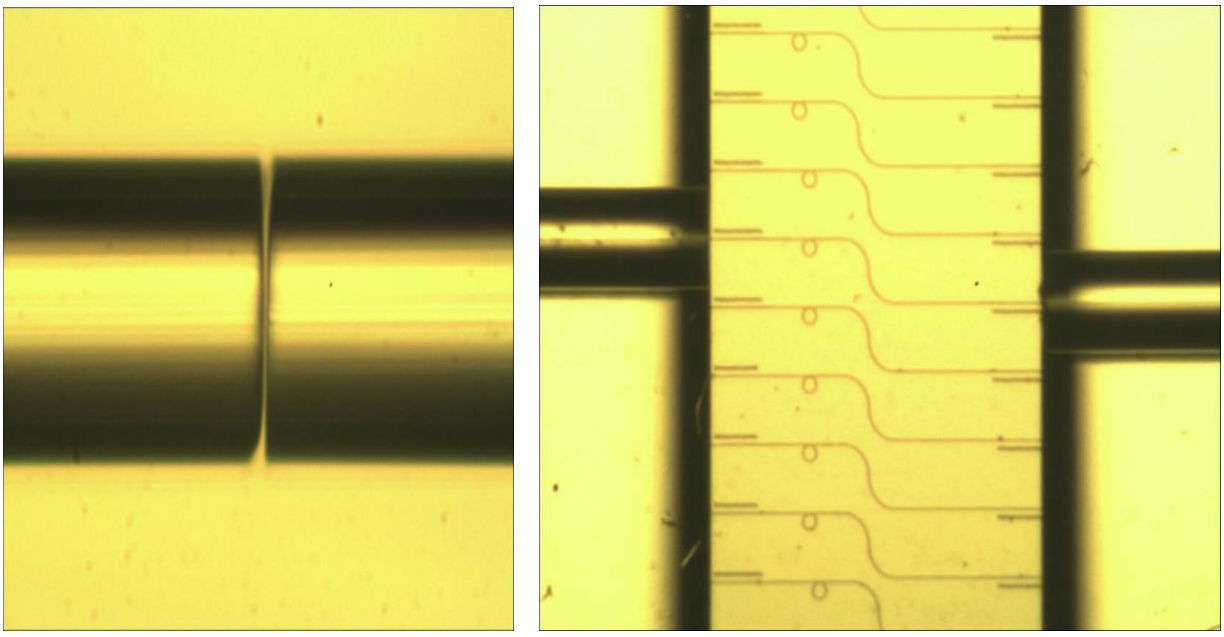


Figure 2.43 (a) fiber-to-fiber measurement setup after cutting the Nufern fiber and (b) transmission measurement setup through the chip

There has been a debate on whether the power before or after Nufern fiber cleavage should be used as input power reference. P. Cheben's paper used lensed fiber for measurement and there is no such concern (no fiber cleavage is demanded). However, for high NA fiber with non-ideal cleavage,

power before cleavage is used as input reference, which is a more conservative approach that gives higher coupling loss (0.5 dB/facet additional cleavage loss included).

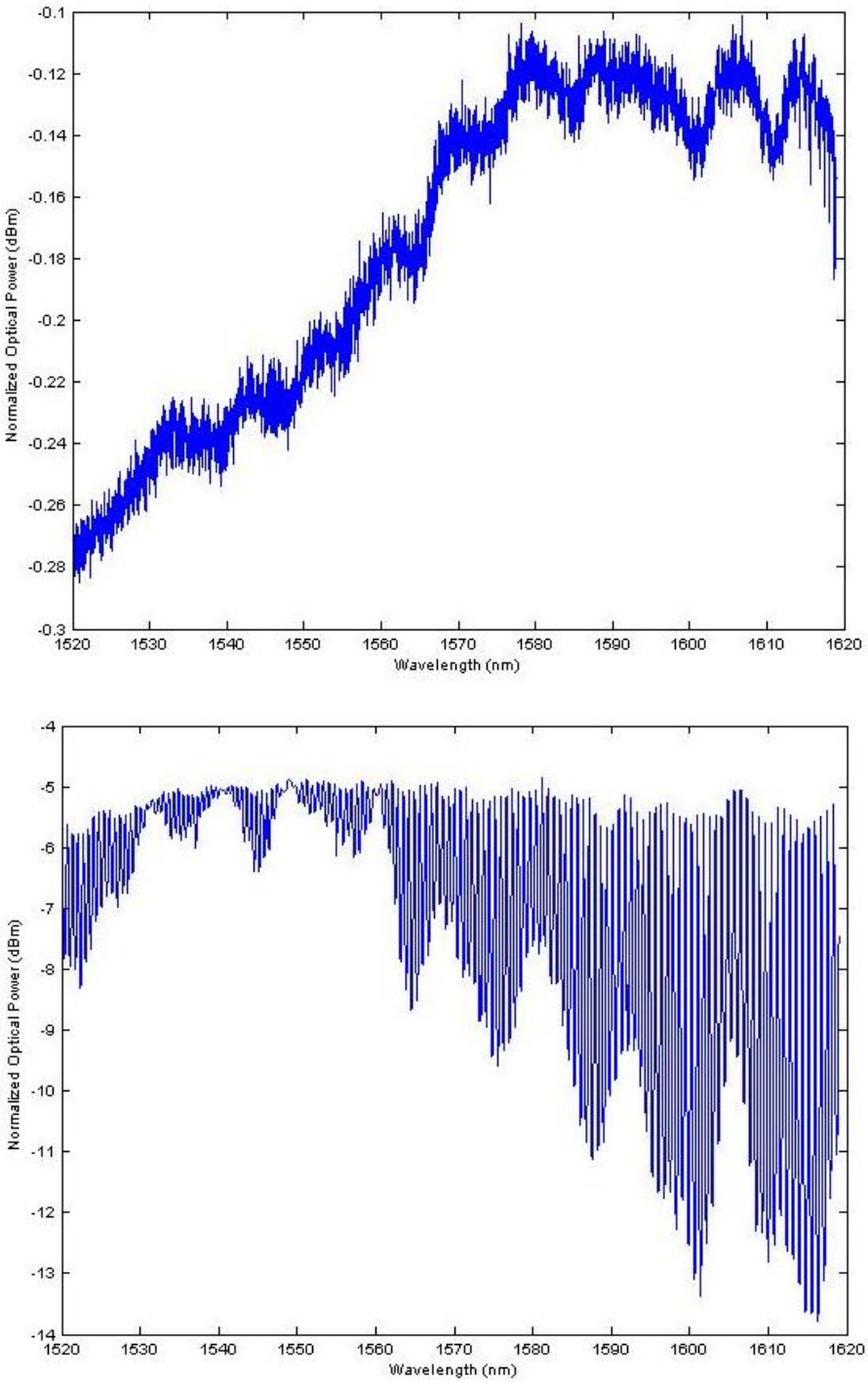


Figure 2.44 (a) Measured of fiber-to-fiber test (b) Measured TE transmission spectrum (with rapid spectral oscillation) through the chip

The chip under test is shown in Fig.2.43 (b). The chip is designed with two edge couplers on both edges, connected with strip waveguides and one S bend are in the middle. The chip is designed without U-groove such that during fiber coupling the correct height is found, only translational movement is required to find the coupling of the next device. The chip from the first batch (the process flow described above) does not yield satisfies results. As shown in Fig.2.44 (b), TE polarization beam shows strong (up to 8 dB swing) and rapid power oscillation while TM shows slightly weaker oscillation though.

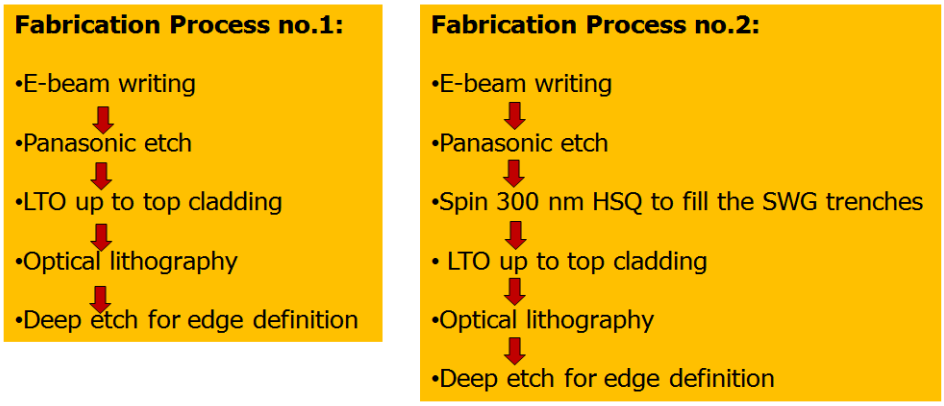


Figure 2.45 (a) Conventional process flow and (b) Modified process flow

After several trials of fabrication and measurement, the problem is identified as non-ideal fabrication process. With conventional process flow, the LTO process may not cover all small trenches of SWG, leading to random air bubbles in the gaps. Those random air voids can strongly scatter the forward propagating beam, leading to weird transmission spectrums. To fix the problem the process flow is modified such that before LTO, thin layer HSQ spinning and annealing is done to fully cover the air gaps at Si layer. As shown in Fig.2.45, both conventional and modified process flow are illustrated.

The chip fabricated via modified process flow is tested with the same setup again. As shown in Fig.2.46, rapid power oscillation is gone for both polarizations and flatband transmission is obtained. The dips and spikes are ring resonances for polarization detections. The ring has 20 μm radius and 400 nm gap that will resonate at both TE (high Q) and TM (low Q) polarizations. By

tuning the polarization rotator on the measurement stage, pure polarization can be found by maximizing one resonance and minimizing the other.

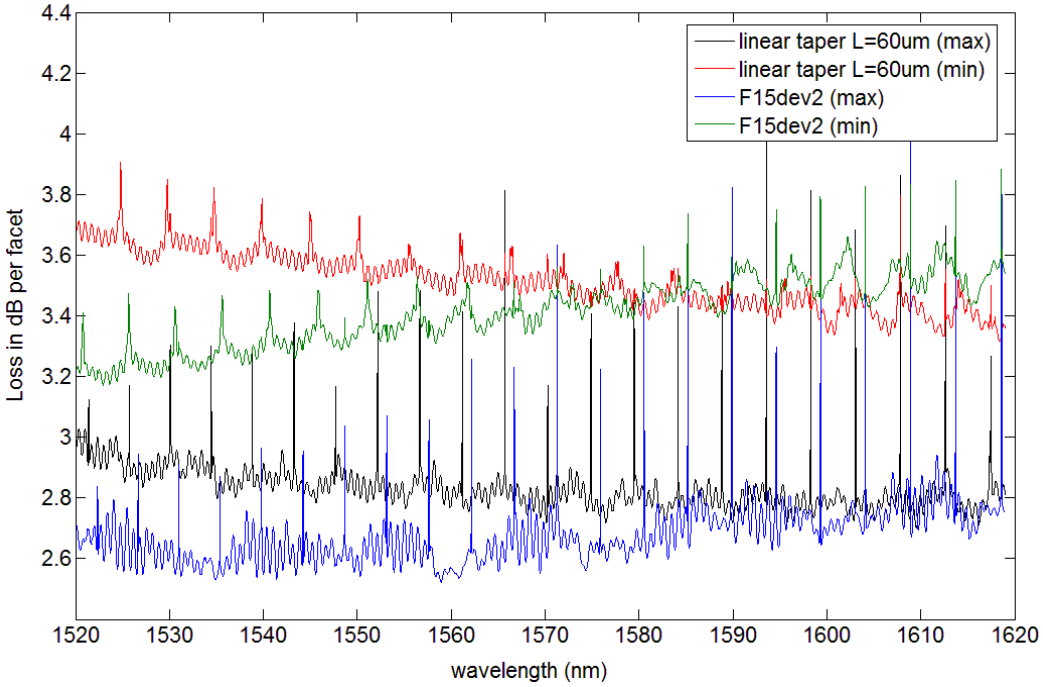


Figure 2.46. Coupler loss comparison between best-performing linear inverse taper and meta-material edge coupler (including propagation and bending loss)

With 2 μm BOX simulation predicts about 1 dB higher TM loss than TE due to leakage, which explains the ~ 1 dB/facet polarization dependent loss (PDL). Measurement shows roughly minimum 2.6 dB/facet loss for one polarization (TE assumed) and maximum 3.5 dB /facet loss for the other polarization (TM assumed). Comparing with the best-performed linear inverse taper, meta-material taper shows < 0.5 dB coupling loss improvement, which is not a surprising bonus.

Conventional meta-material edge coupler indeed shows slightly improved performance (< 0.5 dB) to linear inverse taper. Nonetheless power loss at junction between SWG and hybrid taper becomes inevitable. Better way of Bloch-to-strip mode conversion remains to be discovered. The trident edge coupler idea can be incorporated in to SWG here to solve the problem. Conventional trident edge coupler uses two tips that trap the input beam in a form of strip supermode then converted into strip mode at the inverse taper in the middle.

Similar idea can still apply as shown in Fig.2.47, where dual SWG trap the mode in the form of Bloch supermode then couple to strip mode at inverse taper by evanescent coupling. If the tip width of inverse taper between dual SWG is narrow enough, no mode mismatch loss will be incurred. Meta-trident design not only reduces the mode mismatch loss at hybrid taper junction, but also removes the necessity to fabricate high resolution hybrid taper. Compared with conventional trident edge coupler, meta-trident coupler also provides the same advantage that input mode size of both TE and TM can be equally scaled by adjusting SWG duty cycle.

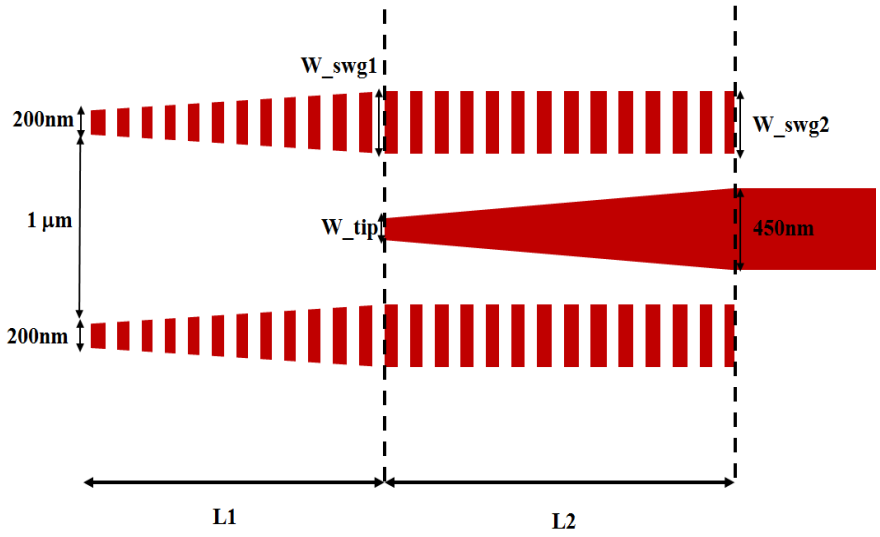


Figure 2.47 Design prototype for meta-trident edge coupler for high NA fiber

The design prototype is shown in Fig.2.47. The first stage of meta-trident coupler is dual SWG tapers that trap input beam in the form of Bloch supermode. Dual taper tips are also designed with shape close to square to ensure equal mode area for both polarizations. The width expansion of SWG at stage 1 is for purpose of increased mode confinement (to suppress leakage). At the end of stage 1, an inverse taper starts to appear and gradually suck Bloch mode power on dual SWG into the middle strip waveguide.

The design phase starts at the dual SWG at edges. With tip width near 220 nm and various gap sizes, polarization independent mode area can be easily found. As shown in Fig.2.48, the TE and TM MFD curves almost overlap, indicating no birefringence for the Bloch supermode. Although it seems n =2.3 is matches better with 4 µm MFD input, the supermode power distribution makes the optimized overlap to occur at slightly smaller MFD. Here n = 2.457 is found with overlaps 95%

to Gaussian mode with 4 μm MFD, which is exactly 50% duty cycle. As an example, in Fig.2.49, 200 nm wide dual SWG spaced by 1 μm shows equal mode area of TE_{00} and TM_{00}. As comparison when Si index is used, polarization independence can no longer be obtained given various tip width and gap sizes.

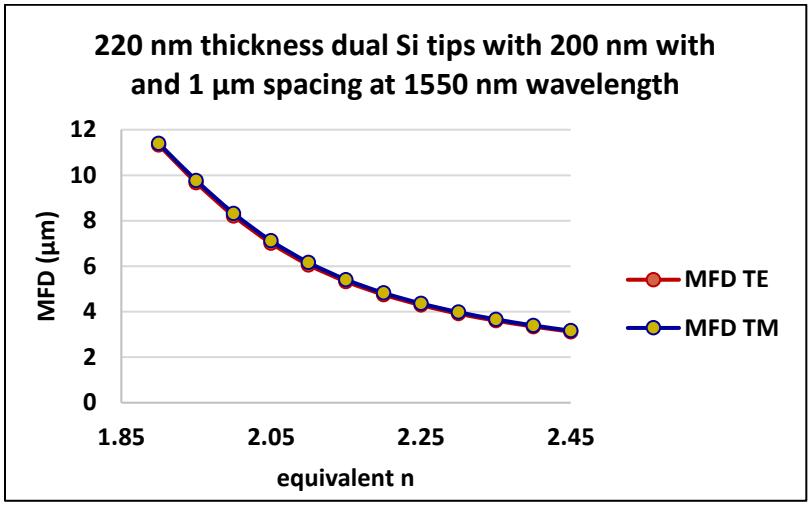


Figure 2.48 Fundamental mode MFD as function of equivalent refractive index

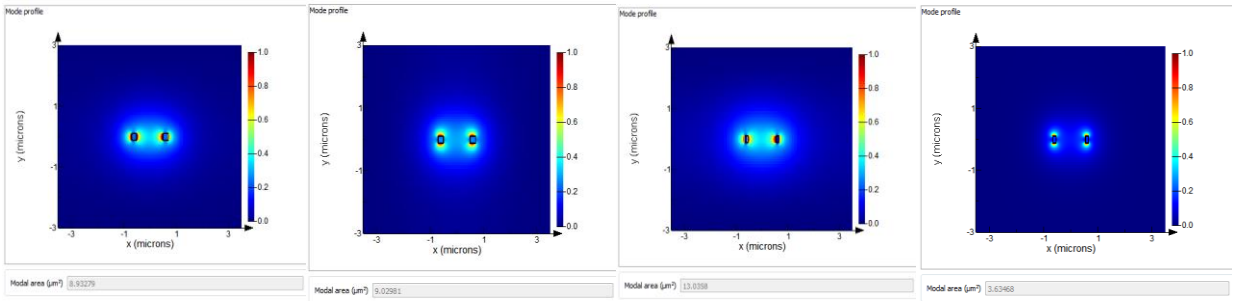


Figure 2.49 | E | of (a) TE_{00} with n_{strip} = 2.457 (b) TM_{00} with n_{strip} = 2.457 (c) TE_{00} with n_{strip}= n_{si} (d)TM_{00} with n_{strip}= n_s

To get a rough estimate of the required taper length, EME simulation is applied on the equivalent structure where dual SWGs are replaced by strip waveguides with n_{strip} = 2.457. As shown in Fig.2.5.50, input mode is set as supermode of dual waveguide and EME results is canned for various L1 and L2. Simulation shows L1 and L2 beyond is not going to give any further improvement at 1550 nm wavelength and meanwhile TM is more efficient than TE during evanescent coupling.

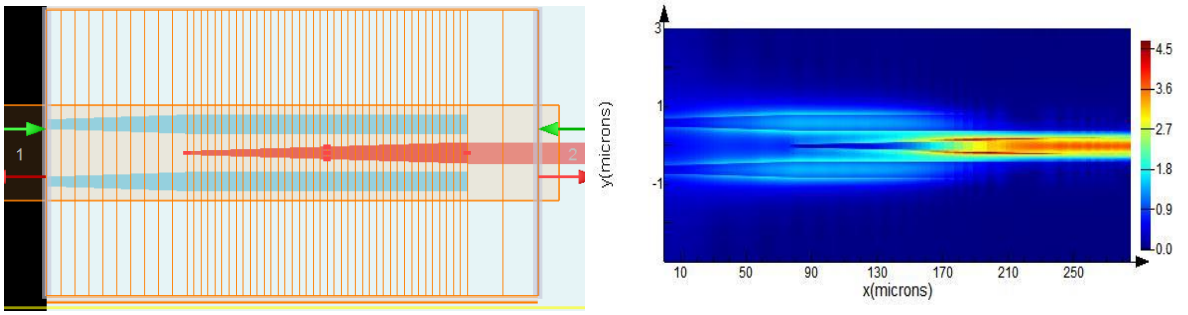


Figure 2.50 (a) Top view of equivalent structure in Lumerical EME solver (b) |E| top view in EME

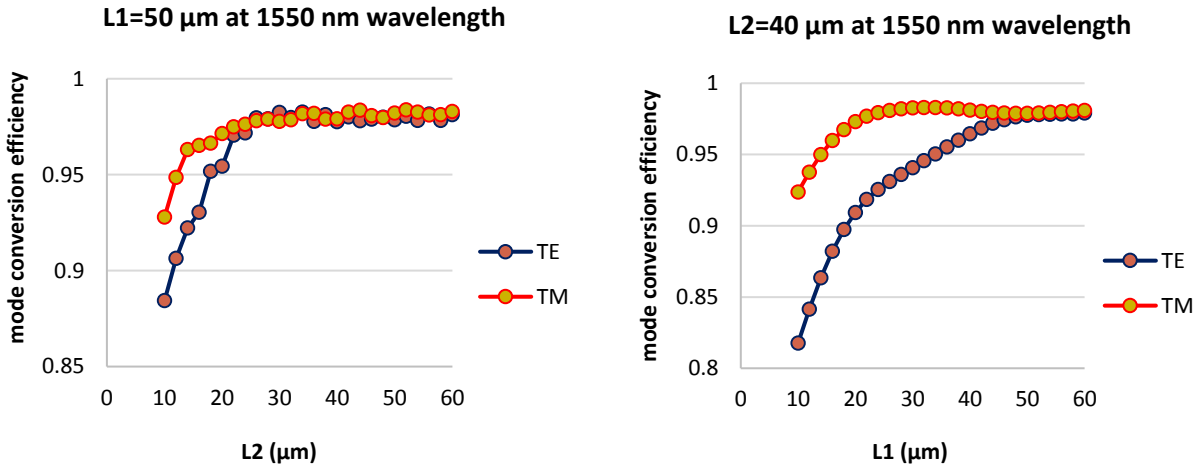


Figure 2.51 EME scanned results for various L1 and L2

To calculate the coupling loss of the real structure, 3D FDTD is used on the 3 µm BOX device. EME calculation does not account for leakage since Si substrate cannot be included in EME. With FDTD, PML boundary is used which includes several microns of Si substrate. FDTD calculation (assuming perfect sidewalls) considers the initial mode mismatch loss at edges, mode transition loss as well as leakage.

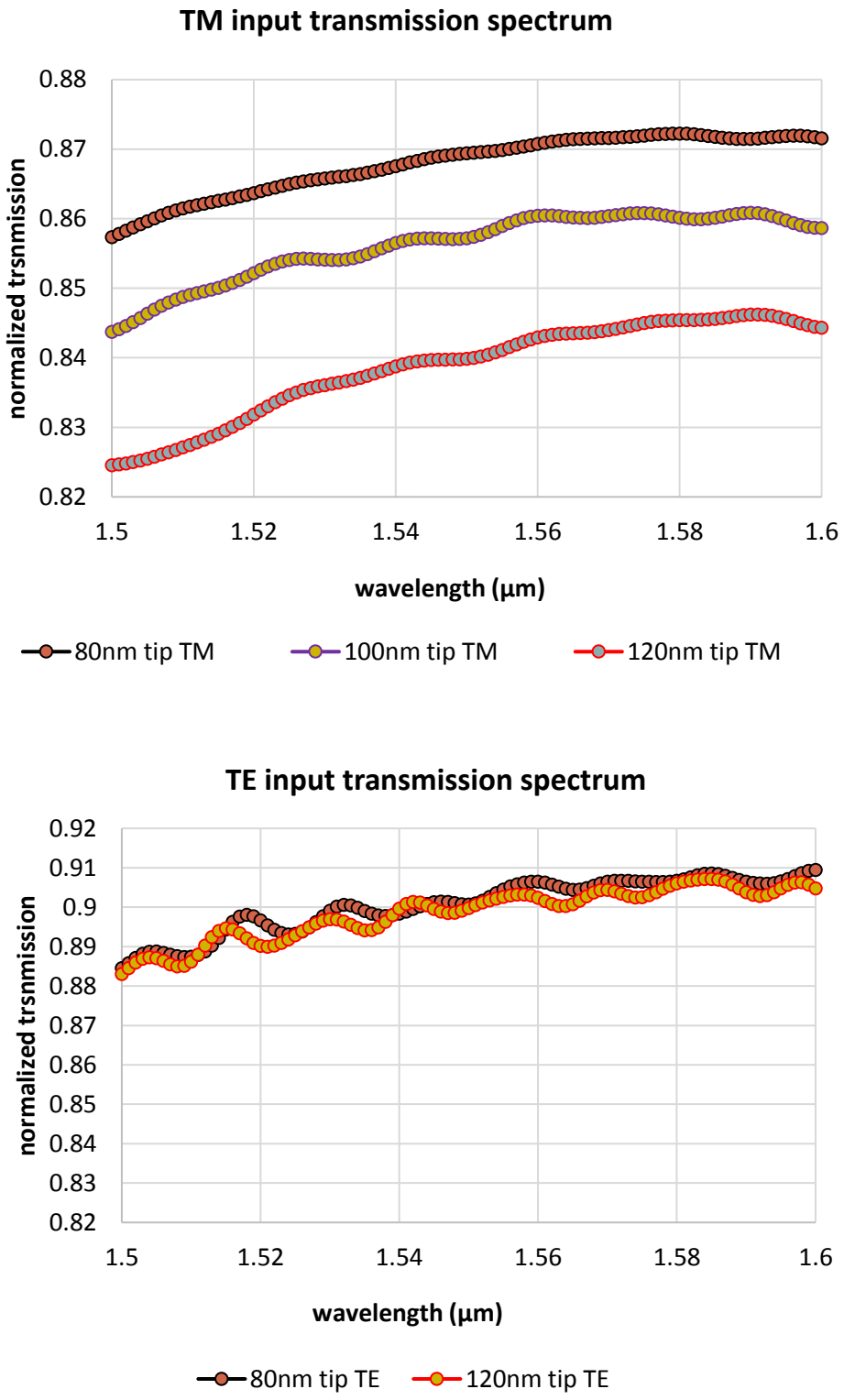


Figure 2.52 3D FDTD power transmission spectrum for TM and TE polarization

Given the parameter L1 = L2 = 50 μm and W_swg1 = W_swg2 = 400 nm, 3D FDTD simulation is done by Lumerical as shown in Fig.2.52. Assuming no sidewall roughness, flat band transmission over 86% can be obtained for both TE and TM polarization, given 80 nm inverse taper tip width is used. Increasing the tip width will lead to non-trivial mode mismatch loss for TM but only trivial loss for TE. However, as tip width of solid Si taper expands, TM shows considerable power transmission drop due to increased mode mismatch loss. Fig.2.52 shows roughly 3% TM efficiency drop when tip width is expanded from 80 nm to 120 nm. Nonetheless, TE power remains almost not affected because TE mode is better confined than TM (width > height) and better confined mode is more robust against perturbations.

To further investigate the mode mismatch loss at L1/L2 interface, field monitors with taper tip section (zoomed in) is are shown in Fig.2.53. At junction, TE Bloch supermode is better confined hence less light is guided in the middle gap. Therefore, TE light cannot "see" the tip which shows dark color at the solid taper on |E| plot. As a comparison TM Bloch supermode is weakly confined hence significant portion of light is guided in the middle gap. Therefore, TM light can see the tip easily which caused interruption (mode and index mismatch) for beam propagation. Mode mismatch loss is calculated for various tip width and it clearly shows the trend loss (especially TM) rises with tip width. For the industrial fabrication perspective, 80 nm is too narrow linewidth for deep UV optical lithography whereas 120 nm can be a fair choice.

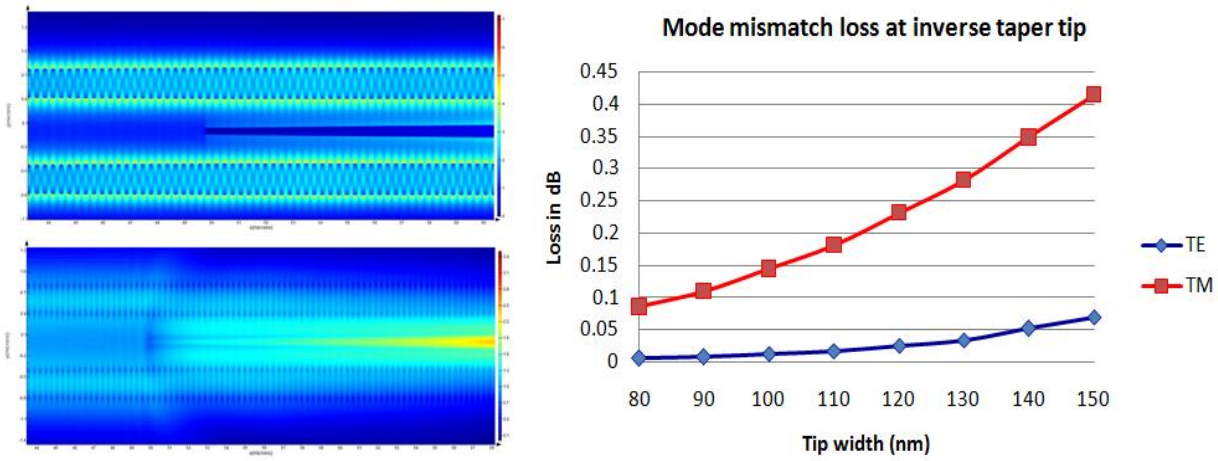


Figure 2.53 |E| top view at L1/L2 junction of (top left) TE mode (bottom left) TM mode (right) mode mismatch loss in dB as function of tip width at 1550 nm wavelength

Further modifications are introduced to reduce the TM mode mismatch loss at L1/L2 junction for large tip width. Modified structure is shown in Fig.2.54, where a SWG buffer stage is added between L1 and L2. The SWG buffer region gradually tunes the equivalent refractive index to better match the mode on both sides. Ideally SWG buffer does not need to be long and even when too narrow width (80 nm) cannot be used, mode mismatch loss can still be reduced for its low equivalent refractive index.

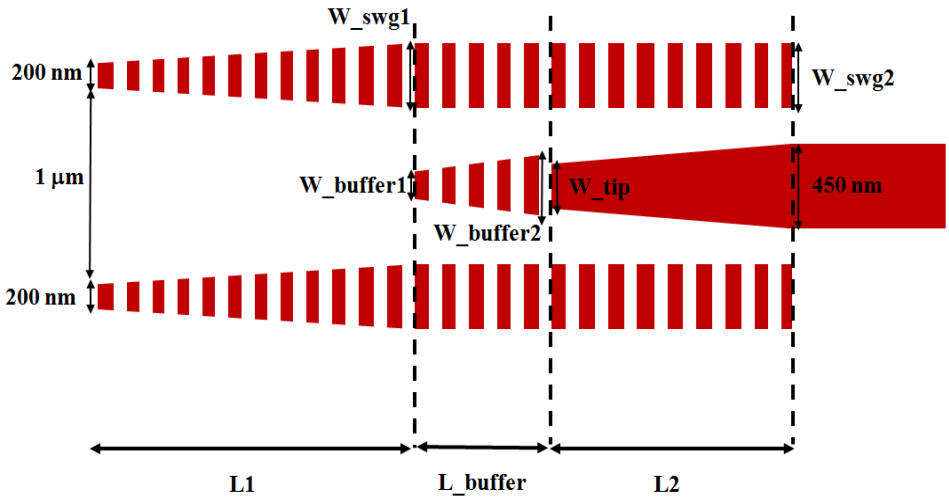


Figure 2.54 Modified structure with SWG buffering region

The buffering region is designed to tolerate 120 nm min feature size. As an example, in Fig.2.55, a 5 µm long L_buffer with W_buffer1 = 120 nm (40% duty cycle) and W_buffer2 = 180 nm (50% duty cycle), is a fair choice. It is assumed that duty cycle increases linearly along the SWG buffer.

Figure 2.55 Equivalent buffer region in 3D FDTD simulation

The buffer region can be calculated by FDTD with an equivalent structure as shown in Fig.2.55, where dual SWG are replaced by dual strip waveguide with index of 2.457. The reason for mode excitation in an equivalent structure is Bloch mode cannot be directly launched by Lumerical mode source. FDTD simulation shows over 98% efficiency over the buffer region can be obtained for TM where TE is almost lossless given strip supermode launched at equivalent structure.

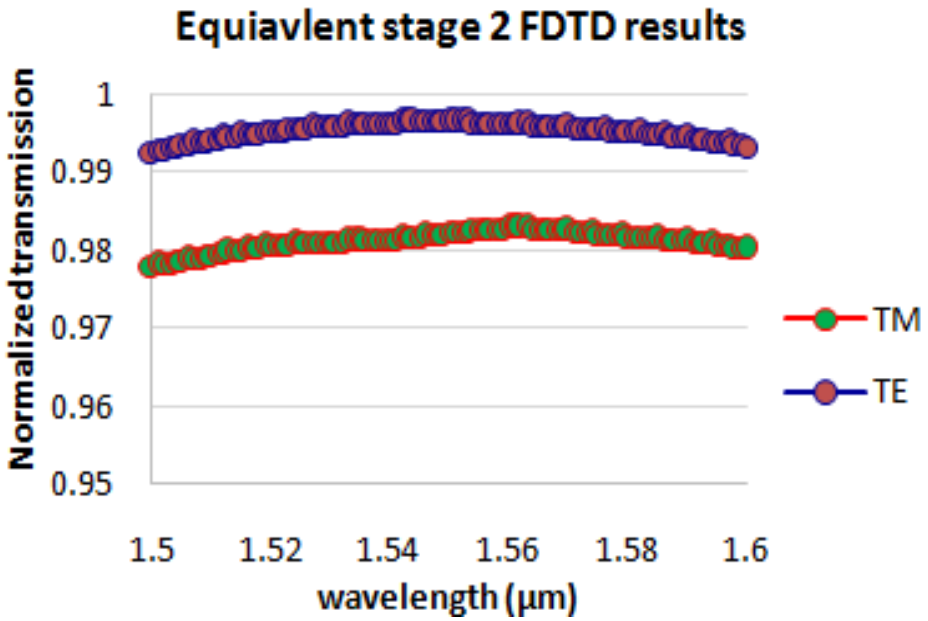


Figure 2.56 3D FDTD calculated buffer section efficiency

The entire structure with 3 μm BOX is simulated with 3D FDTD to determine the total edge coupler efficiency. As shown in Fig.2.57, our modified structure with SWG buffer achieves TE efficiency > 89% (0.5 dB loss) and TM > 87% (0.6 dB loss) over 100 nm bandwidth. With 120 nm min feature size here with buffered SWG, we achieved TM performance comparable than using inverse taper tip width of 80 nm or smaller (50% min feature size relaxation).

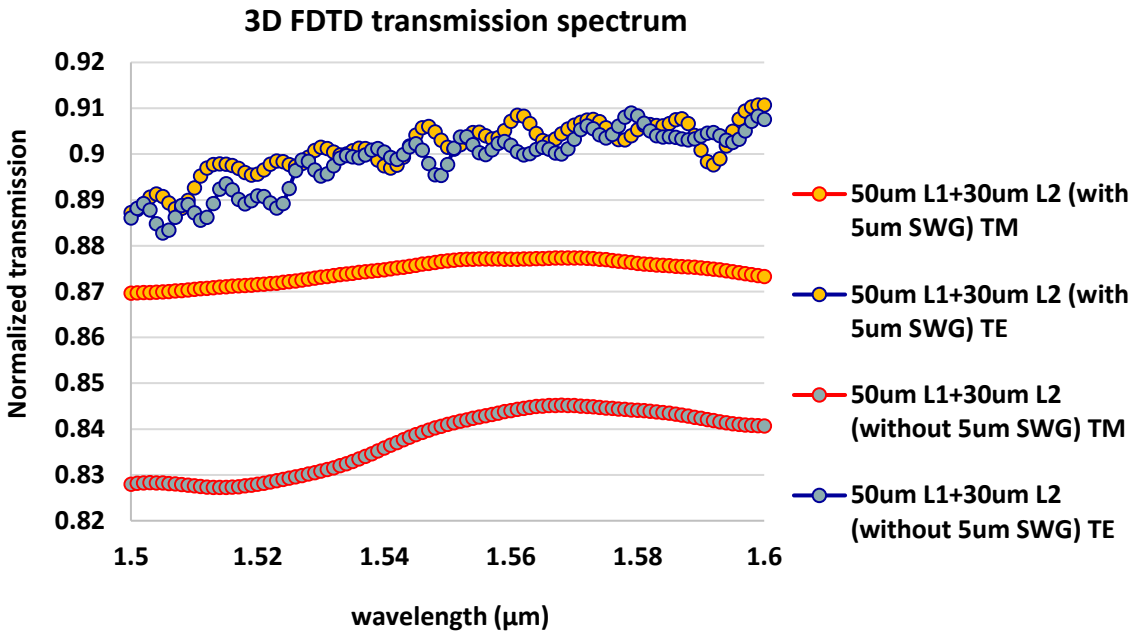


Figure 2.57 FDTD calculated edge coupler efficiency for the modified structure at 120 nm min feature size with and without SWG buffer

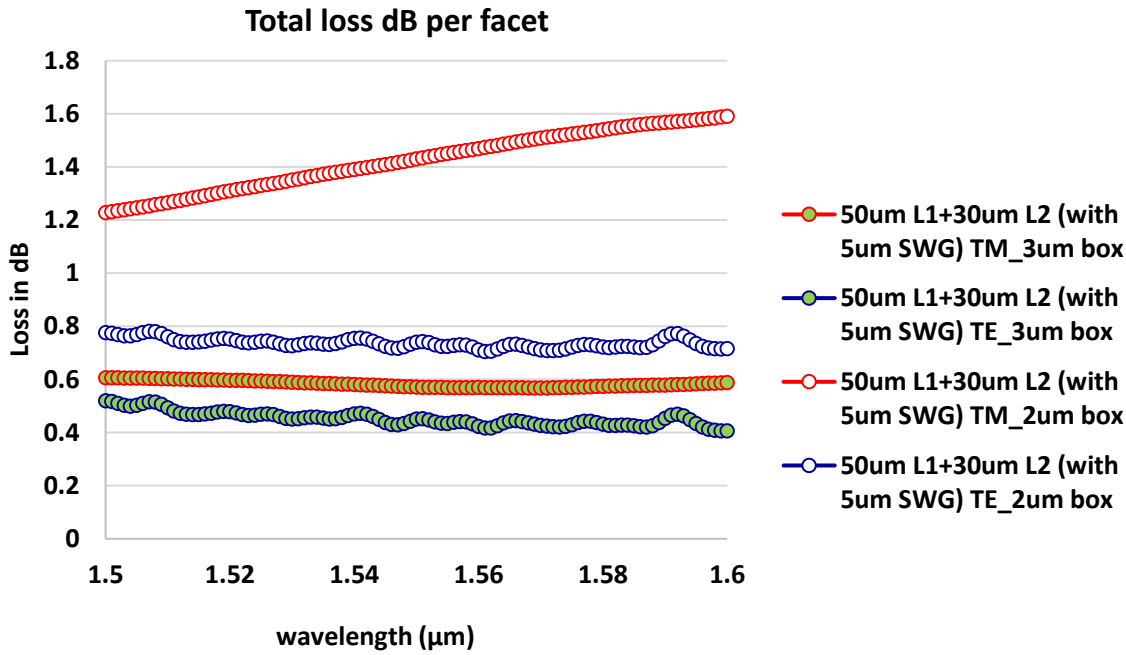


Figure 2.58 FDTD calculated edge coupler loss with 2 µm and 3 µm BOX thickness

Fig.2.58 shows the simulation results for the device with 2 μm and 3 μm BOX thickness. Simulation indicates that longer wavelength suffer higher leakage since mode is less confined. With 2 μm BOX wafer, 0.8 dB/facet TE loss and 1.2-1.6 dB/facet TM loss can be obtained. The complete |E| plot for 3 μm BOX simulation is illustrated in Fig.2.59.

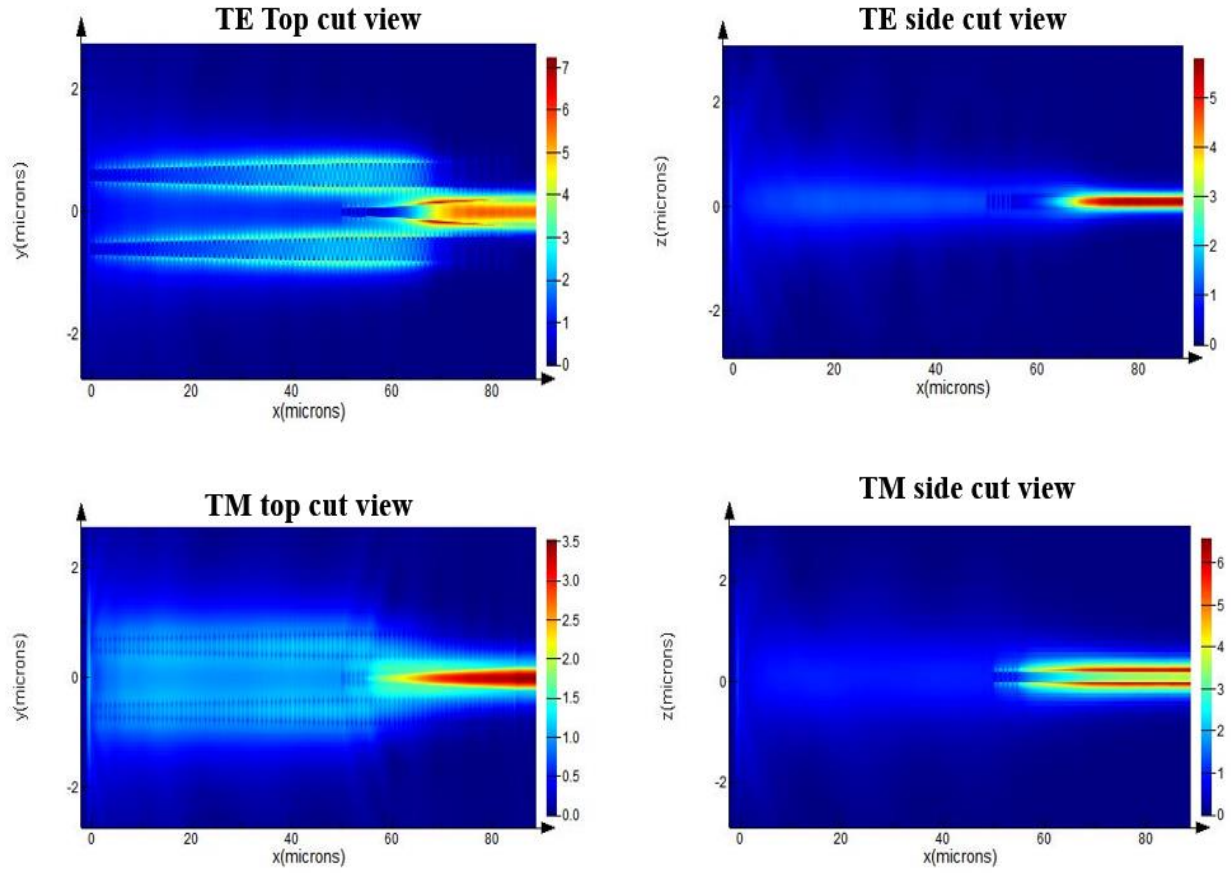


Figure 2.59 FDTD |E| plot of final structure for TE and TM mode

Meta-trident chip has been fabricated on a SOI wafer with 2 μm BOX thickness. On the chip they meta-trident edge coupler with 80 nm and 120 nm solid taper tip width (with and without buffer) as well as linear inverse tapers are all tested.

Fig.2.60 shows the measured spectrum of meta-trident edge coupler with 80 nm tip with without buffer and 120 nm tip width with buffer. Since too large ring radius is still used, identifying polarization from resonance is difficult. Due to the leakage concern, we can predict low loss

polarization is TE. Larger tip width indeed increase insertion loss (especially for TE) and SWG buffer can help TE loss at 120 nm min feature size to be almost comparable to device at 80 nm min feature size.

Measurement results in Fig.2.61 and Fig.2.62 shows for TM, 80 nm tip without buffer achieves 2.85 dB/facet but the loss rapidly grows up to 3.65 dB/facet at 120 nm tip width. With SWG buffer 3.25 dB/facet TM loss has been measured (0.4 dB loss retrieved) but we cannot really retrieve that entire 0.8 dB TM mode mismatch loss.

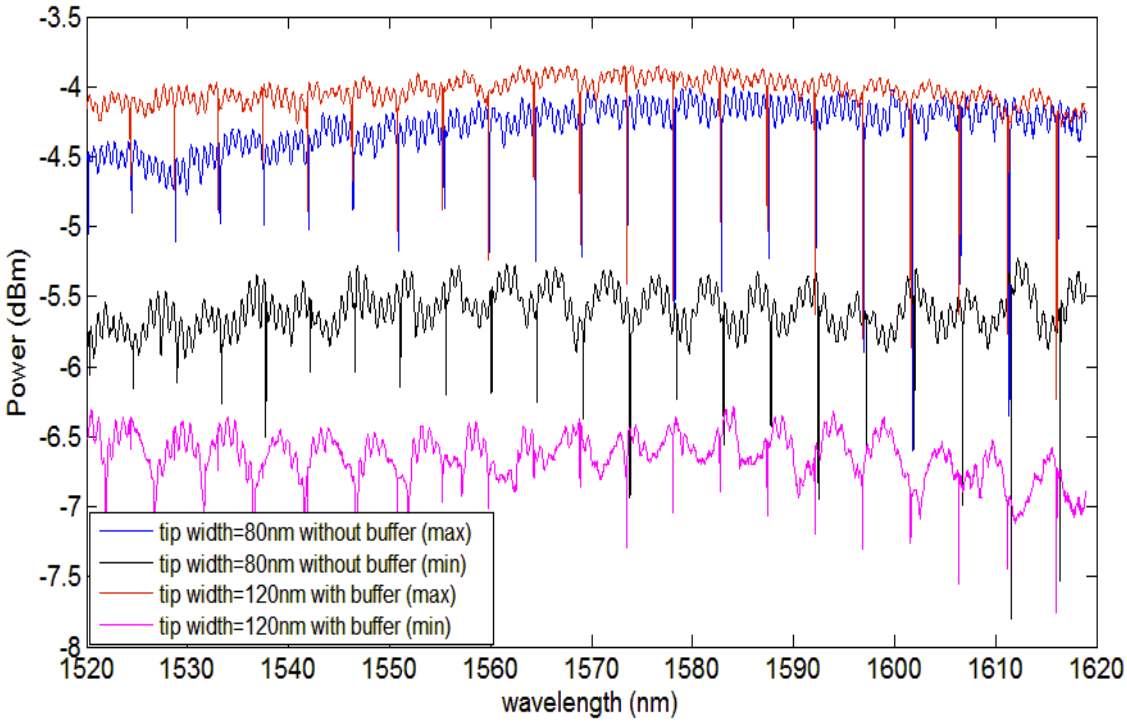


Figure 2.60 Measured power transmission spectrum for meta-trident edge coupler at 80 nm tip width without SWG buffer and 120 nm tip width with SWG buffer (0 dBm input baseline)

For maximum transmission polarization (assume TE), both 80 nm and 120 nm without SWG buffer show ~ 2.2 dB/facet loss, which agrees with our simulation that 120 nm tip does not include noticeable TE mode mismatch loss. Fig.2.63 shows the TE coupling loss given 120 nm tip width, SWG buffer shows additional 0.15 dB coupling loss can be reduced, leading to 2.05 dB/facet. Measured performance is summarized in Table 1, indicating meta-trident is indeed a more superior design in terms of performance and min feature size restriction.

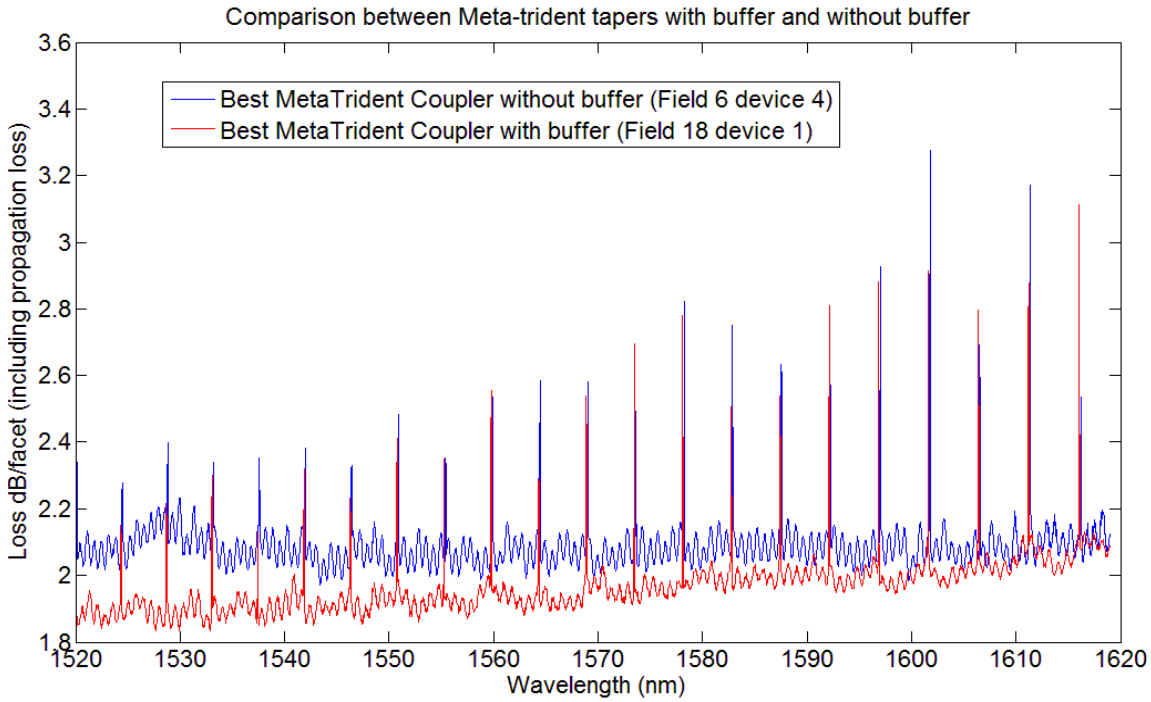


Figure 2.61 Measured coupling loss spectrum for meta-trident edge coupler with and without SWG buffer at TE polarization (~ 0.5 dB/facet fiber cleavage loss is included)

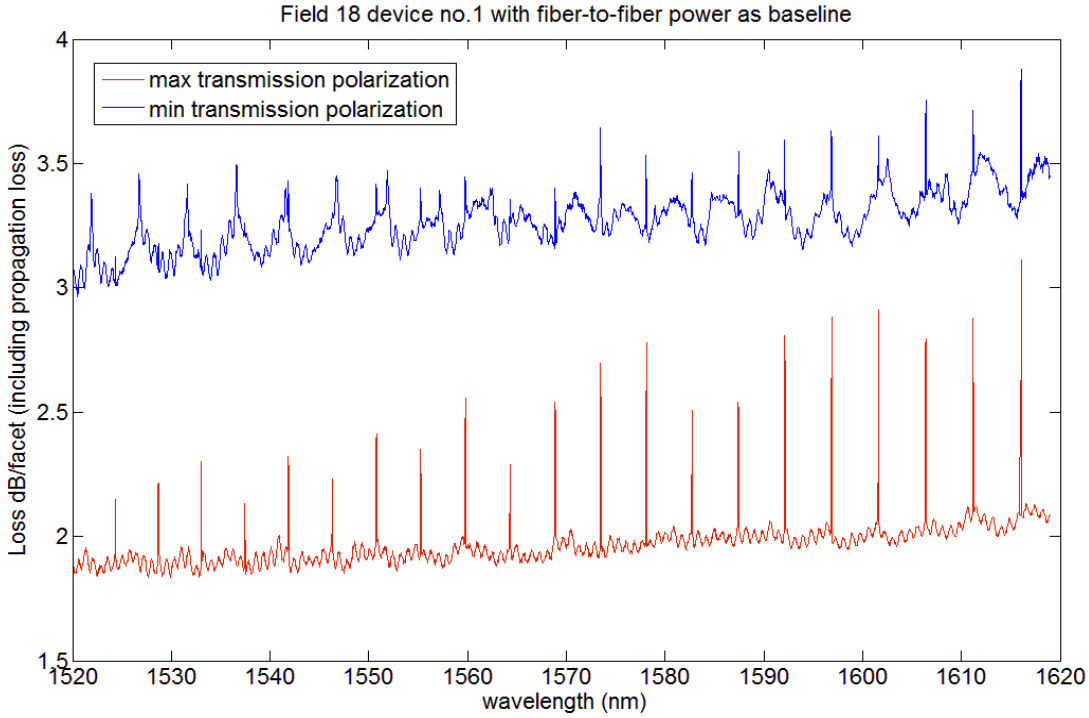


Figure 2.62 Measured coupling loss spectrum for meta-trident edge coupler with 120 nm min feature size and SWG buffer at both polarization (~ 0.5 dB/facet fiber cleavage loss is included)

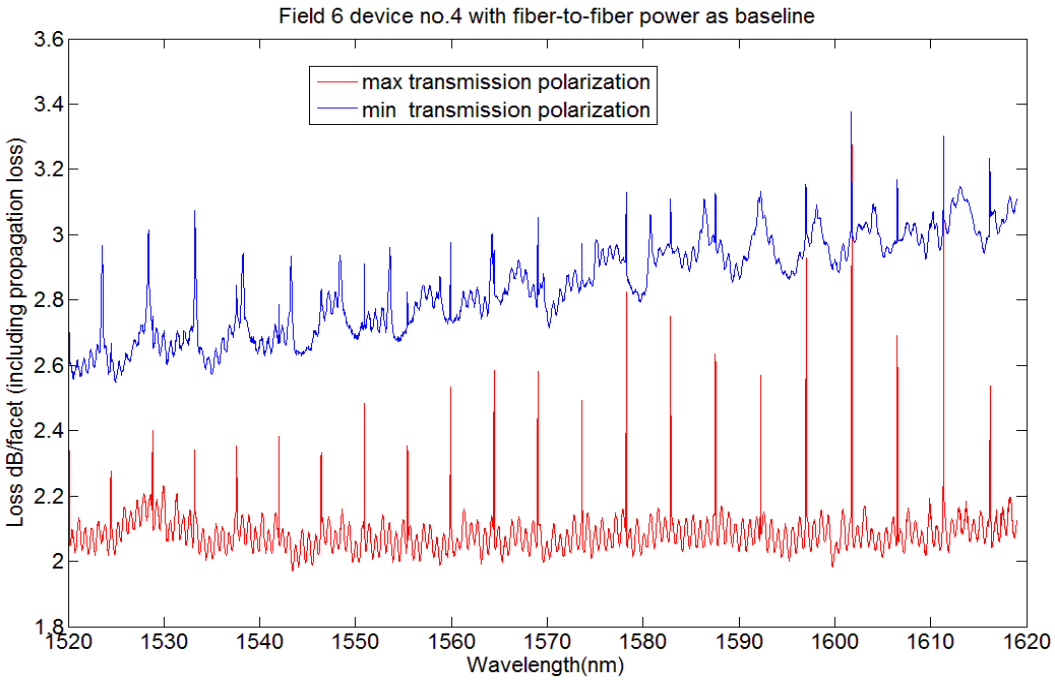


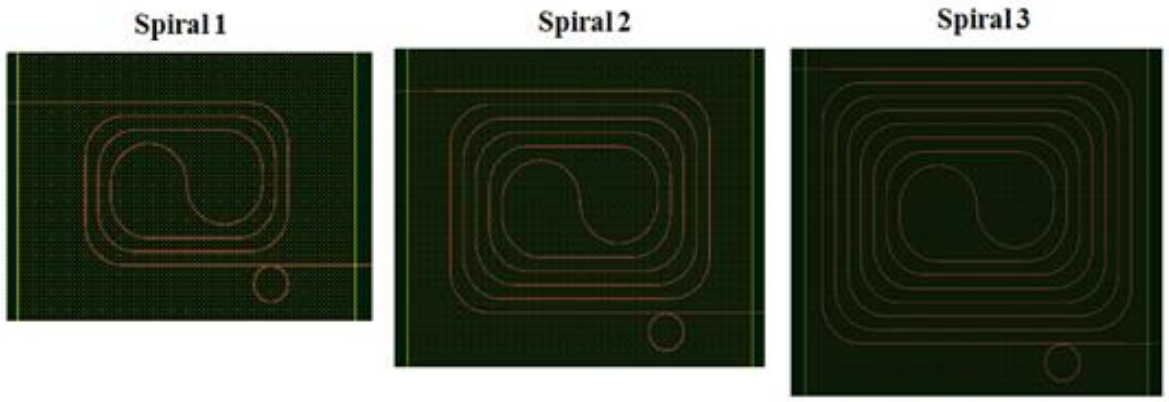
Figure 2.63 Measured coupling loss spectrum for meta-trident edge coupler with 80 nm min feature size without SWG buffer at both polarization (~ 0.5 dB/facet fiber cleavage loss is included)

Table 1 Measured loss (including bending and propagation loss) with 2 μm BOX vs. 3D FDTD simulation results, assuming 0.5 dB/facet fiber cleavage loss is included in simulation

Designs	**Max loss measured (TM assumed)**	**Max loss measured (TE assumed)**	**Simulated TM loss (2 μm BOX no roughness)**	**Simulated TE loss (2 μm BOX no roughness)**
80 nm min feature size(meta-trident)	2.85 dB/facet	2.1 dB/facet	1.2 to 1.6 + 0.5 dB/facet	0.8+0.5 dB/facet
120 min feature size (meta-trident)	3.65 dB/facet	2.2 dB/facet	1.4 to 1.8 + 0.5 dB/facet	0.8+0.5 dB/facet
120 min feature size with SWG buffer (meta-trident)	3.25 dB/facet	1.85 to 2.05 dB/facet	1.2 to 1.6 + 0.5 dB/facet	0.8+0.5 dB/facet
100 min feature size (uni-meta)	3.2 to 3.6 dB/facet	2.6 dB/facet	1.7 to 2.3 + 0.5 dB/facet	1.1 + 0.5 dB/facet

Propagation loss and scattering loss can be characterized by measuring groups of spiral waveguides. With linear inverse taper, waveguide is spiraled for various loops before reaching the output, which give a variety of straight and bend waveguide length. Spiral groups with detailed

parameters are shown in Fig.2.64, where all bends are set the same bending radius (45 μm) for S bends on the chip. Spectrum of both TE and TM are measured while for calculation purposes only data points at 1550 nm wavelength is used. The longer spirals lead to higher accumulated propagation and bending loss which is obtained for both polarizations in experiment.



	Straight Len(μm)	Bend No	Bend Len(μm)	Total Len(μm)
Spiral 1	1180	14	990	2170
Spiral 2	2440	22	1555	3995
Spiral 3	4180	30	2120	6300

Figure 2.64 GDS layout of three spirals with polarization detection ring and spiral parameters

Fig.2.65 shows the transmission spectrum through three spiral and longer the spiral gives lower power transmission. Cut-back method is used which assumes the bending and straight waveguides share equal propagation loss (bending loss is included in propagation loss). With linear approximation in Fig.2.66, one can easily determine the propagation loss by slope of line. 0.51 dB/mm TE propagation loss and 0.56 dB/mm TM propagation loss is derived based on measured results at 1550 nm wavelength. It's noticeable that we claimed TE should suffer higher propagation loss than TM due to sidewall roughness. However, since TM suffers higher bending loss which is included in propagation loss as approximation (not very rigorous), we do get a comparable propagation loss ~ 0.5 dB per mm for both polarizations.

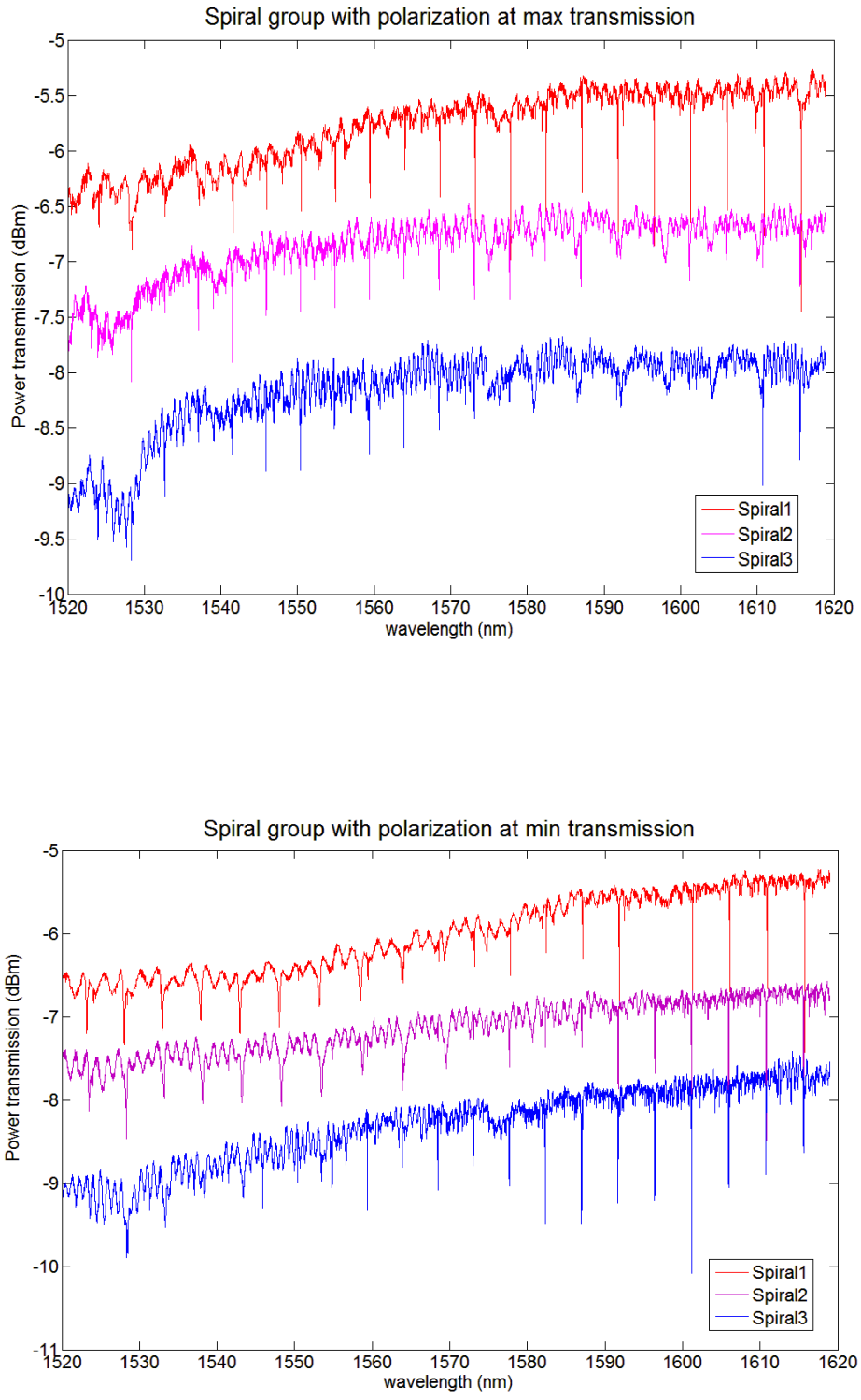


Figure 2.65 Transmission spectrum of both TE and TM for three sets of spirals

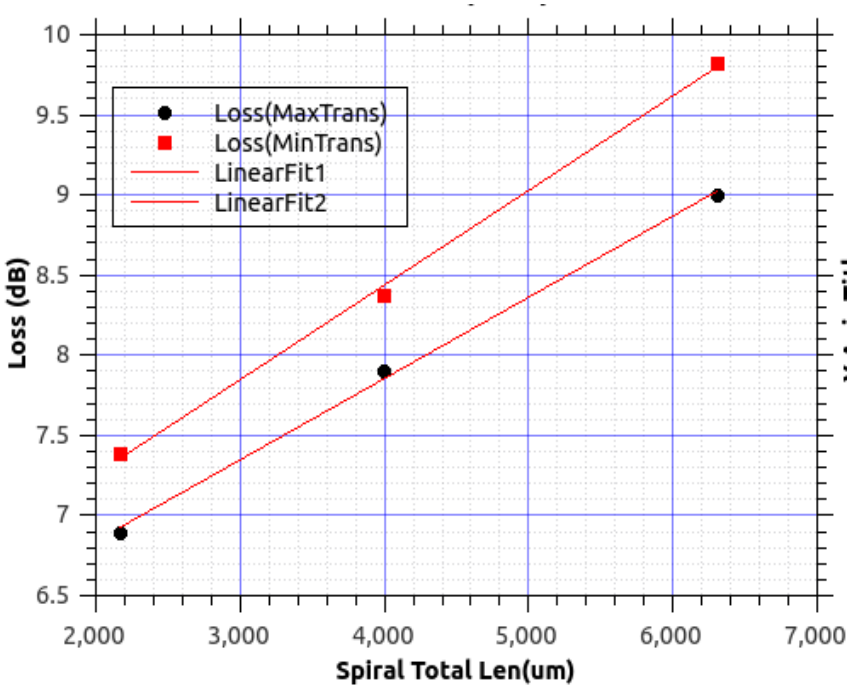


Figure 2.66 Cut-back method linear approximation

As most of our devices on chip take total waveguide length around 450 μm (S bend and straight wavelength length summed together), total propagation loss of 0.27 dB for TM and 0.24 dB for TE can be derived. This means 0.135 dB/facet TM loss and 0.12 dB/facet TE loss can be subtracted from measured edge coupler loss spectrum. Ultimately 1.73 dB/facet loss is obtained for meta-trident edge coupler with SWG buffers at TE polarization.

Meta-material edge coupler can also be designed with lensed fiber input. Conventional trident edge coupler can already achieve decent overlap to lensed fiber input without too much polarization dependence. Nonetheless the interface where inverse taper in the middle is abruptly introduced undesirably introduce mode mismatch loss. As a solution, the SWG buffer idea is adopted from previous meta-trident design to confine beam power more in the middle. The design can be directly converted that SWG is positioned in the middle directly from the beginning, which also provide benefits of tunable mode size by adjusting the SWG duty cycle.

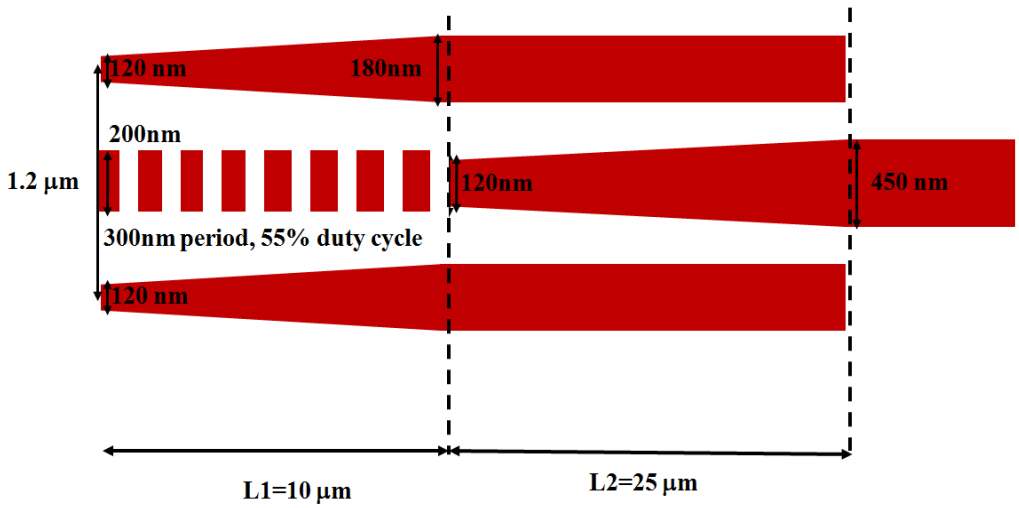


Figure 2.67 Proposed meta-trident structure for lensed fiber

As shown in Fig.2.67, 120 nm width dual waveguides with 1.2 µm center-to-center spacing together with 200 nm width SWG at 55% duty cycle are designed at device edge. At the edge, 95% overlap and 91% power coupling (with Fresnel's reflection) can be achieved for both polarizations, assuming 2.5 µm MFD Gaussian mode input. Then the dual waveguide width expands up to 180 nm to increase mode confinement while SWG remains unchanged. Finally, a linear inverse taper is butt coupled with minimal mode mismatch loss and finish the rest mode conversion.

In FDTD, total device length of 35 µm is selected (L1 = 10 µm & L2 = 25 µm) according to similar EME equivalent structure estimation. In 3D FDTD, the proposed structures as well as linear inverse tapers are calculated with the same device length of 35 µm. Simulation (Fig.2.68) shows inverse taper tip width 180 nm works better for TE whereas 160 nm for TM. With meta-trident structure, both polarization shows considerable loss reduction and the spectrum is even flatter with less than 0.2 dB polarization dependent loss. With 3 µm BOX in simulation, 0.45 dB TE loss and 0.6 dB TM loss can be obtained, assuming no sidewall roughness. The field plot is shown in Fig.2.69 and at junction between L1 and L2, minimal scattering (mode mismatch) is observed due to SWG buffer even with 120 nm min feature size.

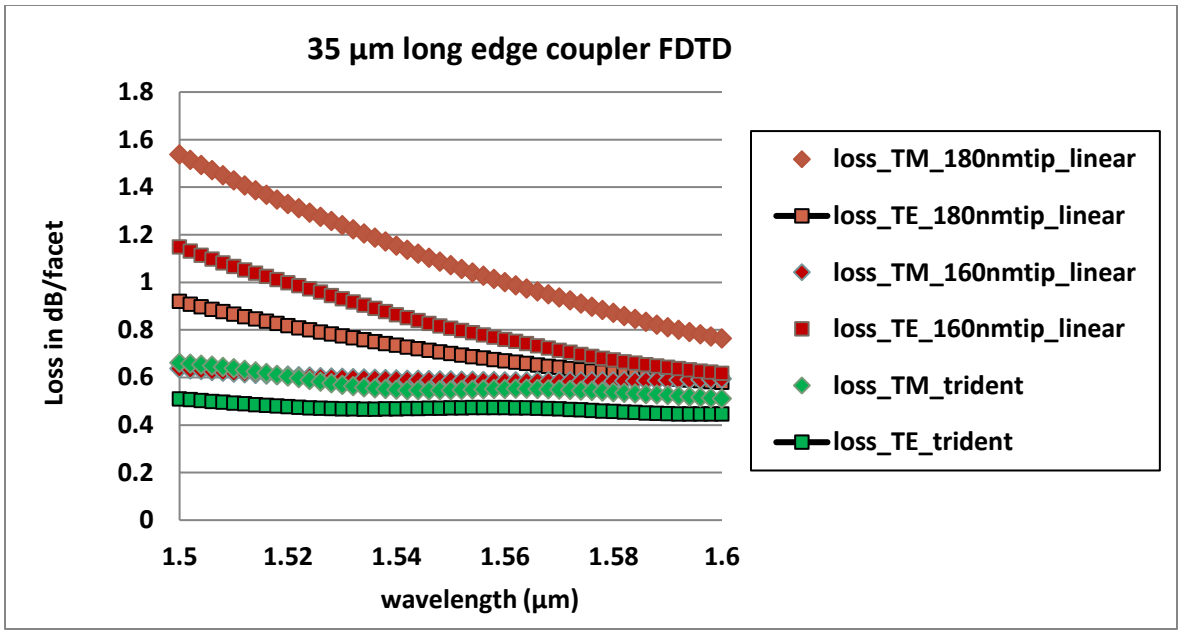


Figure 2.68 3D FDTD spectrum comparison between purposed structure and inverse taper

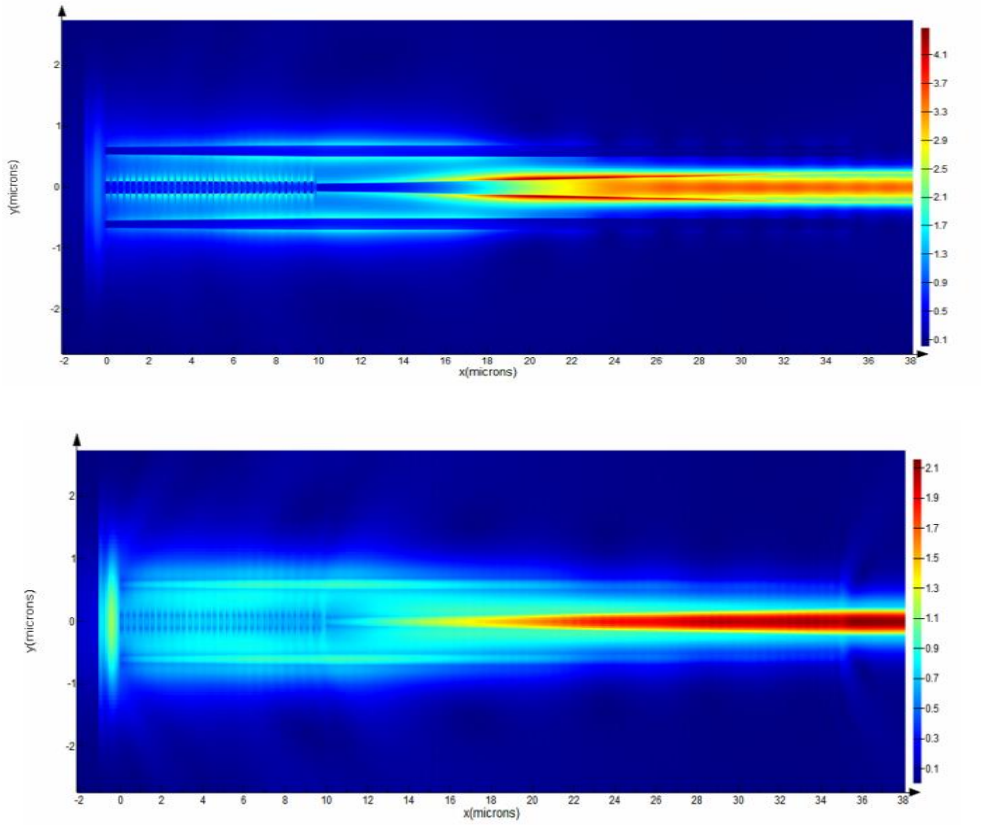


Figure 2.69 |E| top view of (left) TE polarization and (right) TM polarization

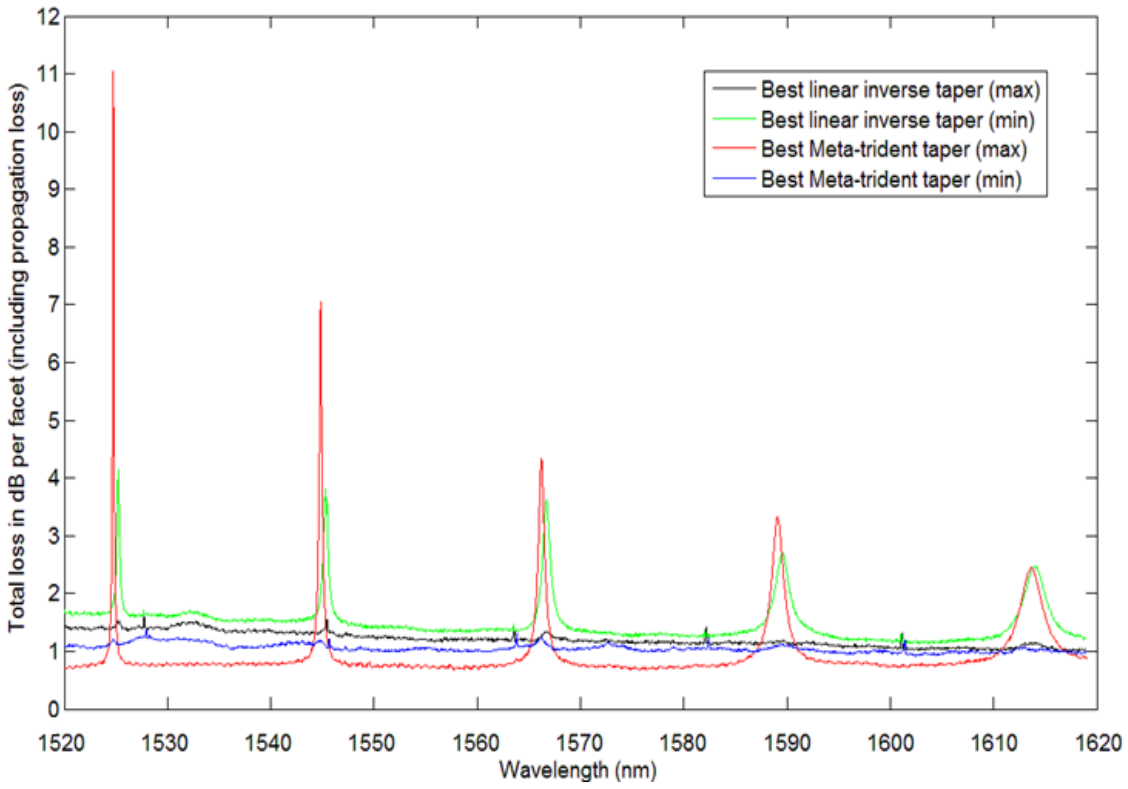


Figure 2.70 Measurement spectrum of meta-trident and inverse tapers

During measurement, chip on 3 μm BOX SOI wafer is used. Fig.2.70 shows the edge coupler loss spectrum, which include propagating loss (0.12 dB for TE and 0.135 dB for TM). With 5 μm radius ring, TM can couple though 400 nm gap while TE cannot. Therefore, in the spectrum, curves with strong loss spikes are TM while others are TE. Subtracting propagation loss, 0.56 dB TM loss and 0.88 dB TE loss can be obtained, which matches reasonably well with 0.54 dB TM and 0.45 dB TE loss in simulation, where higher TE loss is caused by sidewall roughness. The measurement of the best performed conventional linear inverse taper shows 1.1 dB loss for TE and 1.6 dB loss for TM. This value is comparable to our old measurement result. Comparing with best performed linear inverse taper, TM shows about 1 dB improvement while TE shows only less than 0.3 dB improvement at low wavelength.

Table 2 Comparison with state-of-art edge coupler performance

State-of-art works for comparison	**Fiber used**	**Special fabrication requirement**	**Measured coupling loss**
Linear inverse taper (this work) [19]	Lensed fiber with 2.5 μm MFD	2 μm thick BOX layer	1.7 dB per facet for TE and 1.37 dB per facet for TM
Trident edge coupler [22]	Lensed fiber with 2.5 μm MFD	2 μm thick BOX layer	1.6 dB per facet for TE and 1.9 dB per facet for TM
Cantilever edge coupler [37]	Tapered fiber tip with 1.5 μm MFD	Suspended structure with substrate removal	0.6 dB per facet for TM and 0.5 dB per facet for TE
Polymer cladded inverse taper [45]	Tapered fiber tip with 2.9 μm MFD	Oxide taper and polymer waveguide	0.66 dB/facet for TM and 0.36/per facet for TE
O-band Metamaterial edge coupler for SMF28 fiber [29]	SMF28 fiber with 9 μm MFD	Etch Si substrate and replace with index matching material	1.2 dB to1.5 dB per facet (measured with water)
SOI bilayer inverse taper [41]	Focused SMF with 5 μm MFD	Double layer Si structure	1.7 dB/facet with 1 dB polarization dependent loss
C-band Metamaterial edge coupler for lensed fiber [28]	Lensed fiber with 3 μm MFD	3 μm thick BOX layer with 100 nm min feature size	0.5 dB/facet with polarization dependent loss < 0.05 dB
C-band Meta-trident edge coupler for high NA fiber (this work)	High NA flat fiber with 4 μm MFD	2 μm thick BOX layer with 120 nm min feature size	< 2 dB per facet TE loss and 3.25 dB per facet TM loss (including 0.5 dB per facet fiber cleavage loss)
C-band Meta-trident edge coupler for lensed (this work)	Lensed fiber with 2.5 μm MFD	3 μm thick BOX layer with 120 nm min feature size	0.88 dB per facet TE loss and 0.56 dB per facet TM loss

Eventually the measured performance in this chapter is compared with previously reported specs as shown in Table 2. For CMOS-compatible edge couplers, the best performance reported is meta-material edge coupler, claiming 0.5 dB/facet measured. However, this value may not be quite accurate since conventional linear inverse taper benchmark is reported to offer 0.5 dB/facet TE loss, which is far too low comparing with other publications. The similar structure is evaluated by our group using high NA fiber, leading to quite mediocre performance. Meta-trident edge coupler shows more than 0.5 dB improvement with relaxed min feature size restriction. Meta-trident design also shows improved performance over conventional linear taper, leading to near 0.5 dB/facet loss for TM input.

As a part of contract agreement, our group shipped 6 chips of SOI edge coupler to Futurewei Technologies Inc. In addition, two patent applications have been filed and licensed by Futurewei company. The first patent is licensed for multi-layer Si/Si_3N_4 hybrid edge coupler and another one for meta-trident edge coupler.

Figure 2.71 Delivered chip to Futurewei Technologies Inc.

In summary, meta-material edge coupler is conventionally designed as to use SWG to trap the input beam in form of Bloch mode with high overlap for both TE and TM polarization. Then by various approaches, Bloch mode is converted into strip waveguide mode as output. Our investigation found out that with high NA flat fiber (4 μm MFD), conventional meta-material edge coupler can reach less than 2.6-3.4 dB/facet for both polarizations on 2 μm BOX SOI wafer (including 0.5 dB/facet fiber cleavage loss). To further improve the performance, meta-trident edge coupler is designed to eliminate Bloch-to-strip conversion loss as well as improve facet coupling. With 2 μm BOX SOI wafer, 1.76 dB/facet TE loss and 2.85 dB/facet TM loss have been measured over 100 nm bandwidth. If high NA fiber is perfectly cleaved, additional 0.5 dB loss reduction can be applied to both polarizations. Higher TM loss compared with TE is caused by power leakage towards substrate and ~ 0.8 dB TM loss can be reduced if using a 3 μm BOX SOI wafer. With lensed fiber input, meta-trident couplers on 3 μm BOX SOI wafer demonstrates 0.56 dB TM loss and 0.88 dB TE loss, which outperform inverse tapers with various tip widths. We believe that with better fabrication quality and more accurate measurement, half decibel loss per facet can be achievable at least for TM polarization.

CHAPTER 3. ON-CHIP MODE DIVISION MULTIPLEXING (MDM)

3.1 Introduction

Coupling light into the chip is the initial part of on-chip optical communication. Over recent years, researchers are also utilizing optical multiplexing technologies on chip to increase data bandwidth for photonic transceiver chip.

Wavelength division multiplexing (WDM) is the most widely used solution for commercial applications, where various channels are multiplexed with different wavelength [46]. The strength of WDM lies in the strong potential to deploy many channels within one shared bus waveguide and its good compatibility with optical fiber. Nonetheless, on-chip WDM is a fairly "expensive" solution because multiple on-chip laser sources with accurate wavelength control are required and device footprint for (de)multiplexing is massive [47]. Polarization division multiplexing (PDM) has also been developed to use two orthogonal polarizations (TE and TM) to represent two channels [48]. Although data capacity can be enhanced only twice, PDM is typically compatible with WDM.

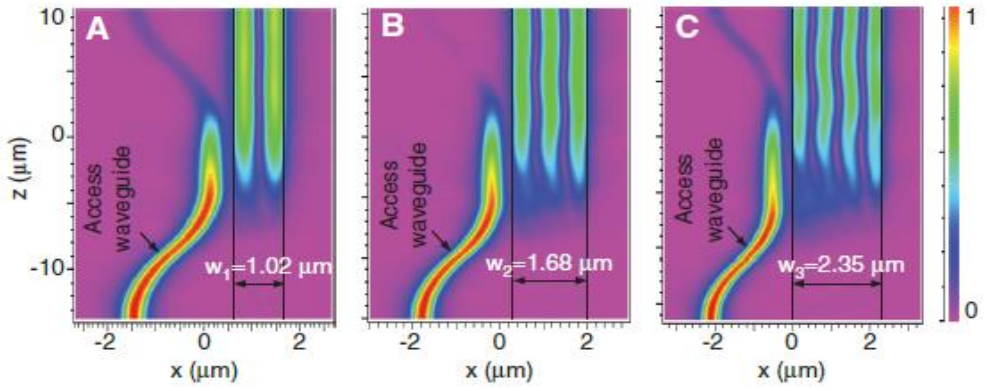


Figure 3.1 The simulated beam propagation that excite TM_1, TM_2 and TM_3 modes in bus waveguide using three ADCs [49]

Another approach mode division multiplexing (MDM), that utilizes orthogonal eigenmodes of a multi-mode waveguide [50][51] as different channels. This idea theoretically allows more than two channels [52] to be deployed, and Fig.3.1 shows a typical solution to excite various eigen-mode channels using asymmetric direction coupler (ADC). Unlike WDM or PDM, on-chip MDM

is not even close to commercialization due to several technical challenges. Most critical problem is on-chip PDM has no capability to fiber PDM due to mode mismatch. That means on-chip PDM cannot be extended outside the photonic chip, which severely limits its commercial application. In addition, on-chip MDM signal manipulation is very difficult, including sharp waveguide bends [53][54] with low modal crosstalk, abilities to filter specific mode [55], efficient multiplexer [49][56][57] and mode order conversion devices [58][59]. Without those fundamental passive devices to offer basic passive functionalities, on-chip MDM could do almost nothing but sharing a single bus waveguide. That makes even on-chip data capacity enhancement using MDM questionable or meaningless.

Chapter 3 begins with a phenomenon called phase sensitivity which widely exists for on-chip MDM devices. Many preciously reported devices claim if device works for each individual channel, it intuitively works for multiple input simultaneously. This widely convinced concept is however wrong when multiple inputs are injected concurrently the device's performance becomes dependent on relative phase shift between input modes. The phase sensitivity issue has been overlooked by most MDM device designer and in this chapter a semi-analytic model is developed to explain such behavior. In addition, three design guidelines are proposed to design phase insensitivity on-chip MDM devices.

The following section of this chapter explores (both numerically and experimentally) sharp bends, mode filter and 3 dB splitter for on-chip MDM systems. With three examples based on different design guidelines, phase insensitive passive MDM devices are demonstrated. The 3 μm radius bend for TE_0/TE_1 two-mode division multiplexing is demonstrated and published in CLEO conference in 2018, which is known as the sharpest MDM bend ever reported on SOI platform.

A two-mode-division-multiplexed spot size converter is numerically demonstrated in this chapter as well, which provides theoretical solution to inter-chip communication through MDM. However, such device is not yet theoretically immune to phase sensitivity.

Mode order converter work based on inverse design is also covered in this chapter. The numerical design of this work is based on author's intern work at Mitsubishi Electric Research Laboratories (MERL), which is published in OFC conference in 2018 and patented by MERL. The experimental part of the inverse design project is demonstrated in Purdue University as an extended collaboration with MERL.

3.2 Phase sensitivity problem of multiplexing devices

Most MDM devices are treated as a linear system that if the device work for multiple inputs individually, it's equivalent as working concurrently. Hence hardly anyone try to investigate what will happen if multiple inputs are injected simultaneously. In fact, multiple input beams will interfere with each other, leading to device's performance sensitive to relative phase of multiple input. Such phase sensitivity problem is a killer for multiplexing devices since they device must be able to handle multiple inputs simultaneously regardless of phase relationship. This requirement applies to all multiplexing techniques (WDM, PDM and MDM) since various channels have different phase velocity and there's no control over their relative phase shifts.

To better illustrates this phenomenon, a MMI based TE_0/TE_1 (de)multiplexer is given in Fig.3.2. The device uses a symmetric Y junction to splits TE_0 into in-phase TE_0 pairs and TE1 into anti-phase pairs. Then TE_0 pairs will be used to drive a 2by2 MMI after phase delay line, which routes beams from two modes into separate ports. Simulation shows around 95% efficiency and less than -25 dB modal crosstalk over 100 nm bandwidth, assuming TE_0 and TE_1 are injected individually. Fig.3.3 shows the E field distribution on a SOI mode Demux at 1550 nm wavelength.

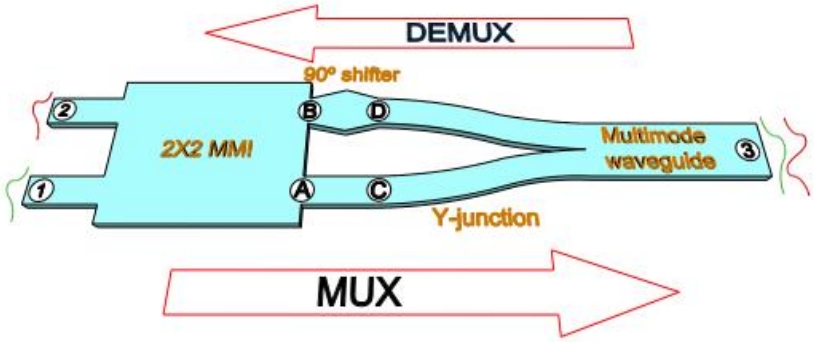


Figure 3.2 Schematic MMI based TE_0/TE_1 (de)multiplexer

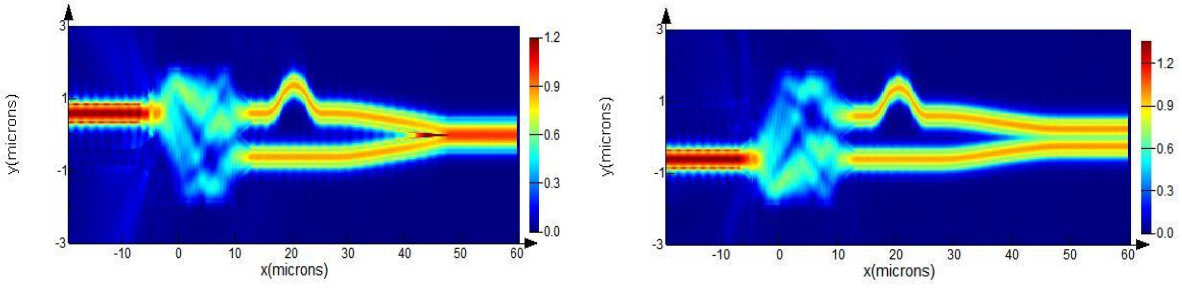


Figure 3.3 |E| plot of MMI based TE_0/TE_1 (de)multiplexer (a) under TE_0 input (b) under TE_1 input

However, the story becomes different when dual modes are injected concurrently, where the actual input becomes the mode beating pattern from TE_0 and TE_1. Fig.3.4 show the field plot under concurrent input at 0 and -0.5 π phase shift and the device respond differently due to phase sensitivity. Ideally both top and bottom output ports should obtain around 95% broadband efficiency but power of two output ports are no longer balanced. Both ports show spectral fluctuation and phase dependence.

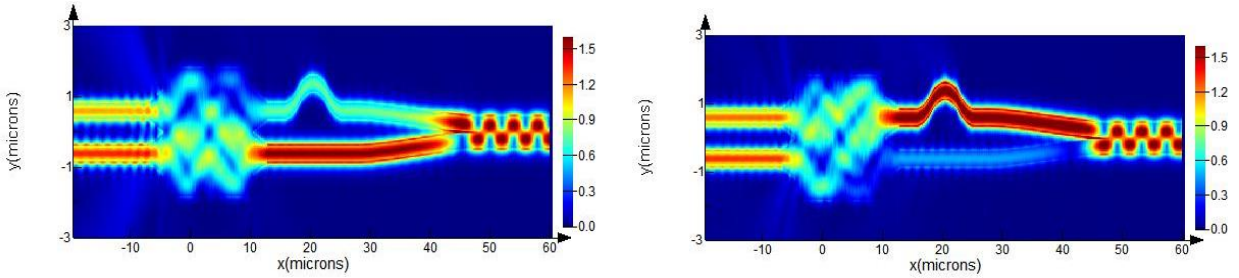


Figure 3.4 |E| plot of MMI based TE_0/TE_1 (de)multiplexer (a) under TE_0/TE_1 concurrent input with 0 phase shift (b) under TE_0/TE_1 concurrent input with -0.5 π phase shift

There are two ways of explaining the phase sensitivity phenomenon seen in Fig.3.4. The mode beating pattern breaks down symmetry or anti-symmetry hence won't be equally divided by the Y junction. The field distribution after Y junction strongly depends on relative phase between dual modes hence also drives the MMI differently based on phase relationship. Another explanation is the crosstalk power will strongly interfere with the main beam at the same wavelength and polarization. To analytically describe such phenomena, a transfer matrix of the Demux is established as following.

$\begin{pmatrix} \overrightarrow{E_{top}} \\ \overrightarrow{E_{bot}} \end{pmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{pmatrix} \overrightarrow{E_{TE0}} \\ \overrightarrow{E_{TE1}} \end{pmatrix}$ where 95% efficiency with 1% crosstalk is assumed under individual mode input. Assuming top port is output port for TE_0 and bottom port is for TE_1, then $A^2 = D^2 = 0.95$ and $B^2 = C^2 = 0.01$. Here let's use φ_1 & φ_2 to represent phase shift at top port from TE_0/TE_1 input respectively while use φ_3 & φ_4 to represent phase shift at top port from TE_0/TE_1. Then the transfer matrix becomes as following, which can also give formula for top port E field (φ_A is phase of TE_0 mode input and $\varphi_A + \Delta\varphi$ is phase of TE_1 mode input).

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \sqrt{0.95}e^{j\varphi_1} & \sqrt{0.01}e^{j\varphi_2} \\ \sqrt{0.01}e^{j\varphi_3} & \sqrt{0.95}e^{j\varphi_4} \end{bmatrix}$$

$\overrightarrow{E_{top}} = \sqrt{0.95}\, e^{j\varphi_1}\overrightarrow{E_{TE0}} + 0.1\, e^{j\varphi_2}\overrightarrow{E_{TE1}} = \sqrt{0.95}\, \left|\overrightarrow{E_{TE0}}\right| e^{j(\varphi_1+\varphi_A)} + 0.1 \left|\overrightarrow{E_{TE1}}\right| e^{j(\varphi_2+\varphi_A+\Delta\varphi)}$

Then top port power can be represented as $\left|\overrightarrow{E_{top}}\right|^2 = \overrightarrow{E_{top}}\,\overrightarrow{E_{top}}^*$

$\overrightarrow{E_{top}} = \sqrt{0.95}\, \left|\overrightarrow{E_{TE0}}\right| \cos(\varphi_1 + \varphi_A) + 0.1\left|\overrightarrow{E_{TE1}}\right| \cos(\varphi_2 + \varphi_A + \Delta\varphi)$

$+ j\{\sqrt{0.95}\, \left|\overrightarrow{E_{TE0}}\right| \sin(\varphi_1 + \varphi_A) + 0.1\left|\overrightarrow{E_{TE1}}\right| \cos(\varphi_2 + \varphi_A + \Delta\varphi)\}$

$\left|\overrightarrow{E_{top}}\right|^2 = \overrightarrow{E_{top}}\,\overrightarrow{E_{top}}^* =$

$0.95 \left|\overrightarrow{E_{TE0}}\right|^2 \cos^2(\varphi_1 + \varphi_A) + 0.01 \left|\overrightarrow{E_{TE1}}\right|^2 \cos^2(\varphi_2 + \varphi_A + \Delta\varphi) + 0.2 \times \sqrt{0.95} \times \left|\overrightarrow{E_{TE0}}\right|\left|\overrightarrow{E_{TE1}}\right| \cos(\varphi_1 + \varphi_A) \cos(\varphi_2 + \varphi_A + \Delta\varphi)$

$+ 0.95 \left|\overrightarrow{E_{TE0}}\right|^2 \sin^2(\varphi_1 + \varphi_A) + 0.01 \left|\overrightarrow{E_{TE1}}\right|^2 \sin^2(\varphi_2 + \varphi_A + \Delta\varphi) + 0.2 \times \sqrt{0.95} \times \left|\overrightarrow{E_{TE0}}\right|\left|\overrightarrow{E_{TE1}}\right| \sin(\varphi_1 + \varphi_A) \sin(\varphi_2 + \varphi_A + \Delta\varphi)$

Hence

$\left|\overrightarrow{E_{top}}\right|^2 = \overrightarrow{E_{top}}\,\overrightarrow{E_{top}}^* =$

$0.95 \left|\overrightarrow{E_{TE0}}\right|^2 + 0.01 \left|\overrightarrow{E_{TE1}}\right|^2 + 0.2 \times \sqrt{0.95} \times \left|\overrightarrow{E_{TE0}}\right|\left|\overrightarrow{E_{TE1}}\right| \times \{\cos(\varphi_1 + \varphi_A) \cos(\varphi_2 + \varphi_A + \Delta\varphi) + \sin(\varphi_1 + \varphi_A) \sin(\varphi_2 + \varphi_A + \Delta\varphi)\}$

$= 0.95 \left|\overrightarrow{E_{TE0}}\right|^2 + 0.01\left|\overrightarrow{E_{TE1}}\right|^2 + 0.2 \times \sqrt{0.95} \times \left|\overrightarrow{E_{TE0}}\right|\left|\overrightarrow{E_{TE1}}\right| \cos(\varphi_1 + \varphi_A - (\varphi_2 + \varphi_A + \Delta\varphi))$

$= 0.95 \left|\overrightarrow{E_{TE0}}\right|^2 + 0.01\left|\overrightarrow{E_{TE1}}\right|^2 + 0.2 \times \sqrt{0.95} \times \left|\overrightarrow{E_{TE0}}\right|\left|\overrightarrow{E_{TE1}}\right| \cos(\varphi_1 - \varphi_2 - \Delta\varphi)$

As a result, there is a nontrivial nonlinear term appears which depends on phase difference $(\varphi_1 - \varphi_2)$ between input & crosstalk optical path and relative phase shift $(\Delta\varphi)$ between two input modes. $(\varphi_1 - \varphi_2)$ term various the spectrum, which leads to spectral fluctuation meanwhile $\Delta\varphi$ instead of φ_A dictates the phase sensitivity. In this example if it's assumed $\left|\overrightarrow{E_{TE0}}\right|^2 = \left|\overrightarrow{E_{TE1}}\right|^2 = \left|\overrightarrow{E_{TE0}}\right|\left|\overrightarrow{E_{TE1}}\right| = 1$, then the maximum spectrum fluctuation is $\pm 0.2 \times \sqrt{0.95} \approx \pm 20\%$. To reduce this fluctuation, the crosstalk power must be reduced dramatically. Assuming modal crosstalk

under single mode input can be control down to -40 dB (0.01%), then B term in the transfer matrix becomes 0.01, which adjust the maximum spectrum fluctuation to $\pm 0.02 \times \sqrt{0.95} \approx \pm 2\%$. Therefore, it's can be concluded that for on-chip MDM devices, at least less than -40 dB (0.01%) modal crosstalk is required for phase insensitive operation of the device. However, such ultralow crosstalk has hardly been demonstrated in previously reported work due to its extreme difficulty.

The analytical expression with nonlinear term derived can become quite useful to predict the device's performance under concurrent input. Since transfer matrix requires simulation with single mode input, this approach is more like semi-analytic. This method becomes powerful such that once device is simulated individual mode input, direct derivation of output spectrum is possible based on any user specified $\Delta\varphi$. With the same geometry, now input modes are injected at exactly the starting position of Y junction to avoid dephasing on the same waveguide (if dual modes are injected several micrometers before the Y junction). Here the entire transfer matrix values are wavelength dependence, which generate the spectral fluctuations as shown in Fig.3.5. Fig.3.5 shows semi-analytical approach can very accurately predict the output spectrum under any arbitrary $\Delta\varphi$.

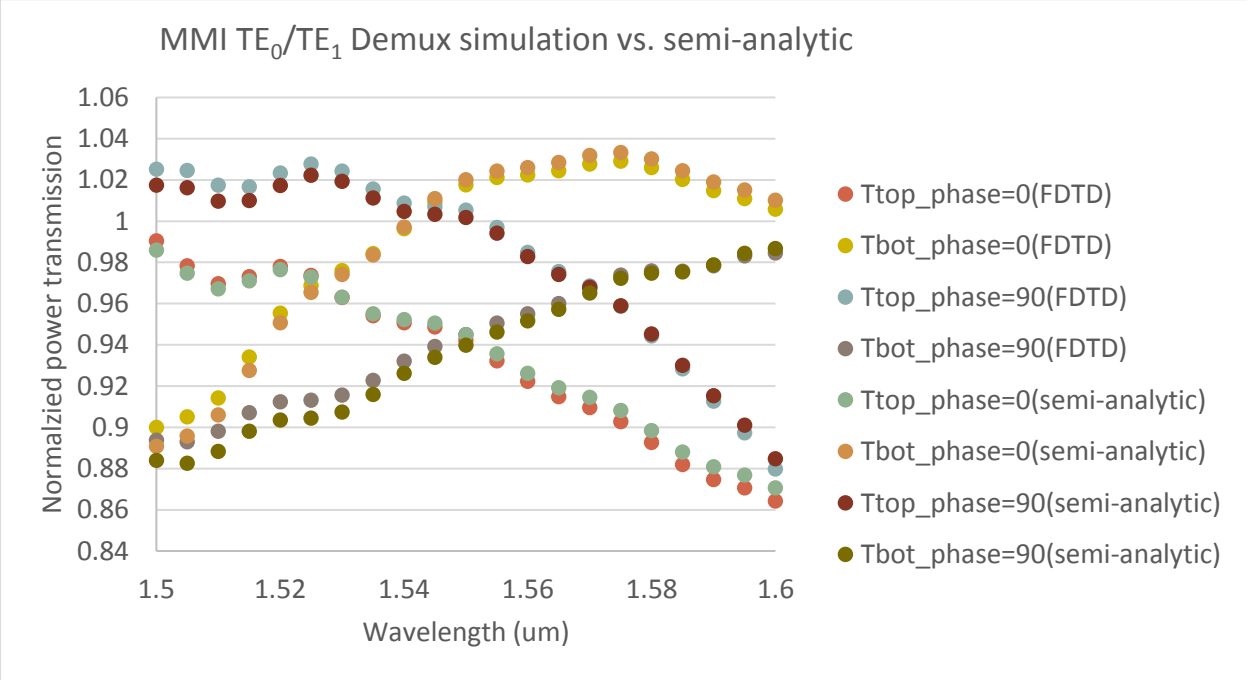


Figure 3.5 FDTD calculated spectrum vs. semi-analytical approach calculated spectrum

3.3 MMI based TE_1 pass TE_0 filter

Another vital device for on-chip MDM is the mode filter, which serves to clean the channel. Typically to filter high order mode (weaker guidance) is easy since high order modes can be cut-off by adiabatic waveguide taper. To filter the better guided low order mode remains challenging for on-chip MDM.

X.Guan published his TE_1 pass TE_0 filter based on subwavelength grating structure (Fig.3.6) [60], where the grating is designed to provide bandgap for TE_0 mode while TE_1 mode can still propagate through. X. Guan has experimentally demonstrated 2 dB insertion loss for TE_1 but TE_0 can be filter down by > 40 dB over broad bandwidth. Although this is impressive, X. Guan filters TE_0 using photonic bandgap hence TE0 attenuation is strongly attributed to reflection and radiation. However, any highly reflective device is not going to be practical for product point of view and meanwhile such subwavelength structure is also difficult for fabrication. Therefore, alternative solution to filter TE_0 mode with negligible reflection and reduced fabrication challenge is still needed.

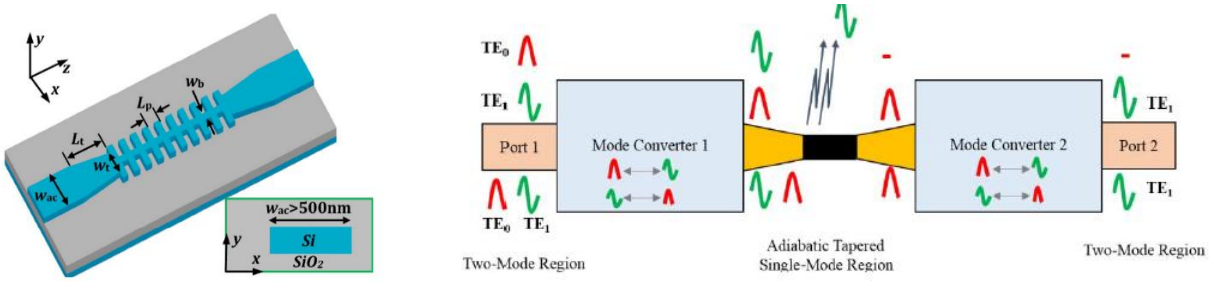


Figure 3.6 (a) High order mode pass filter based on 1D photonic crystal [60] (b) High order mode pass filter based on back-to-back mode switch [55]

In 2017, Ahmmed et al. showed a TE_1 pass TE_0 filter on a polymer material platform [55]. The idea is to switch TE_0 and TE_1 first before using sharp bend to filter the TE_1 mode (originally TE_0) and ultimately proper mode order is restored by another mode switch. With massive polymer filter device (11 mm long), 2.2 dB excess loss with 20 dB TE_0 rejection is measured. Even though this idea may work for SOI platform, using two mode switches and cascaded sharp bends may not be a favorable solution when considering footprint, wavelength sensitivity and fabrication tolerances. More importantly, such device although works for both TE_0 and TE_1 mode separately, does not mean it can handle TE_0/TE_1 mode beating pattern well under various relative phase shift. The

crosstalk is not sufficiently low enough to ensure phase insensitive operation under dual-mode concurrent excitation. Hence a more effective and practical high order mode pass filter solution remains to be demonstrated on SOI platform.

Here we present out innovative TE_1 pass TE_0 filter design based on MMI, as shown in Fig.3.7. The idea is transformed from TE_0/TE_1 mode demultiplexer proposed by T. Uematsu [61] where input TE_1 mode will form one anti-phase TE_0 pairs at outer rims of MMI. With reciprocity when two anti-phase TE_0 input are injected from MMI outer rims, beam should focus at middle output port as TE_1 mode as well. On the other hand, when injecting an anti-phase TE_0 pair, two in-phase TE_0 images can be obtained at approximately the same image distance. Therefore, a Y junction is deployed first to split TE_0 into an in-phase TE_0 pair while TE_1 into two one pair of anti-phase TE_0. Then two beams are used to excite a MMI structure from outer rims where TE_1 will refocus at central output port and TE_0 getting out from two outer ports equally.

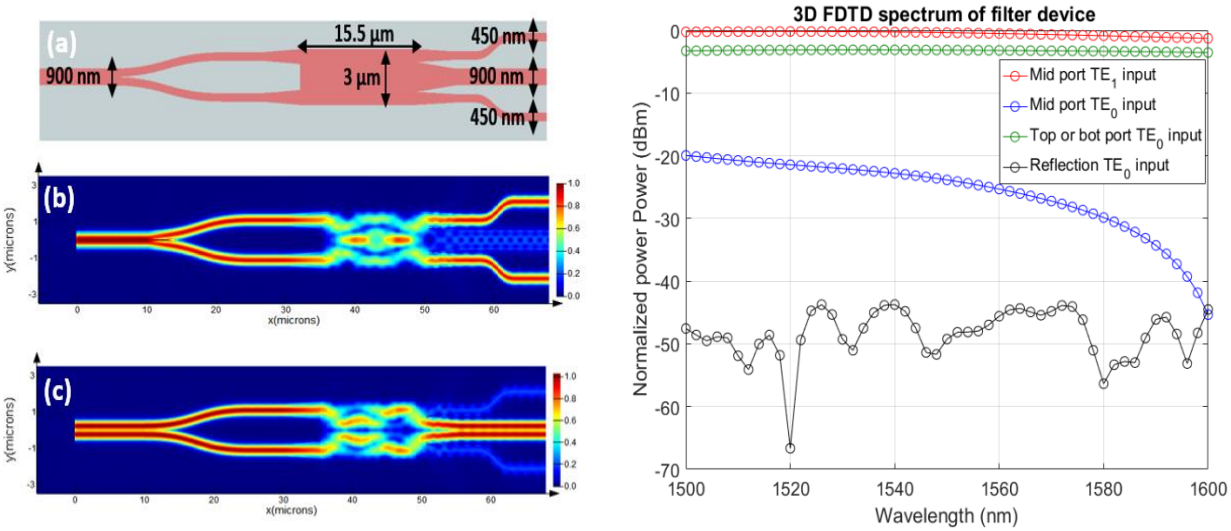


Figure 3.7 (a) schematic of SOI TE_1 pass TE_0 filter device based on MMI (b) FDTD |E| plot with TE_0 input (c) FDTD |E| plot with TE_1 input (d) 3D FDTD spectrum

The device is simulated using Lumerical 3D FDTD over 100 nm bandwidth. Fig.3.7 (b) and (c) show the FDTD calculated E field distribution through the filter device, indicating efficient TE_1 transmission and strong TE_0 rejection. TE_0 power can be further dumped by radiation using two inverse tapers. Due to horizontal symmetry, mode conversion between TE_0 and TE_1 is prohibited, which is ideal for TE_0/TE_1 two-mode division multiplexing. Minimized TE_1 insertion loss occurs at 1530 nm wavelength while maximized TE_0 rejection appears near 1600 nm wavelength. Given the tradeoff between TE_1 insertion loss

and TE_0 rejection, MMI dimension or operating wavelength can also further tweaked for lower loss or stronger filtering purposes. With given geometry (3 μm by 15.5 μm MMI body), < 1.2 dB TE_1 insertion loss and > 15 dB TE_0 rejection is numerically demonstrated over 100 nm bandwidth. TE_0 input only suffers less than -40 dB reflection when rejected because TE_0 power is passing through top/bot port at high efficiency (-3.2 dB).

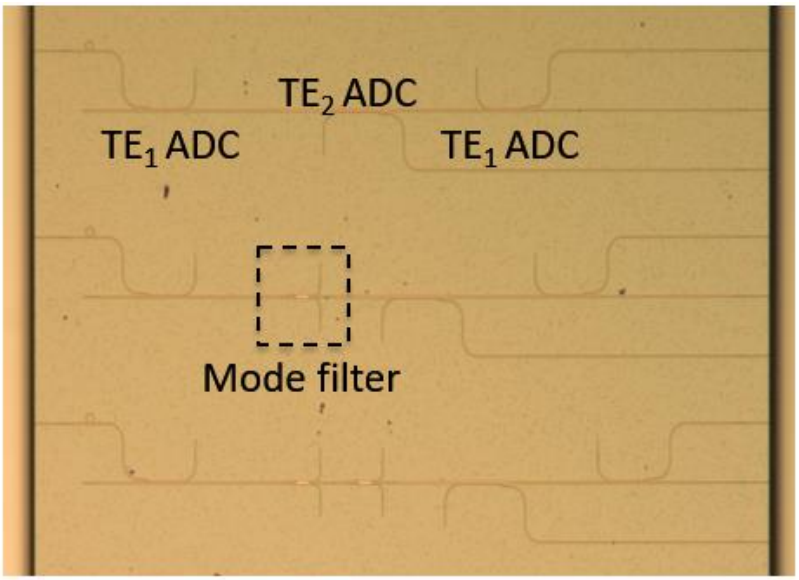


Figure 3.8 Optical microscope image of high order mode measurement device with ADC

The TE_1 insertion loss is measured by using asymmetric directional coupler (ADC). ADC is designed at input side to excite TE_1 power and another set of ADCs are deployed at output to demultiplex different mode orders. To characterize the TE_1 excitation efficiency, back-to-back TE_1 ADC configuration is measured at the top port, which shows ~ 1 dB ADC insertion loss at C band. The back-to-back device power can then be used as a baseline for TE_1 insertion loss measurement. Then filter device is inserted between back-to-back TE_1 ADC and power the deviation from baseline is treated as device insertion loss with TE_1 input. Fig. 3.8 shows optical microscope image of ADC back-to-back baseline and filter device measurement scheme.

Fig,3.9 shows the measured power spectrum under back-to-back TE_1 ADC with single and double filtering devices compared with ADC baseline (no filter device). Measurement shows < 1.5 dB insertion loss over C band and the best performance (sub-decibel loss) occurs at around 1530 nm. The spectrum of filter device is relatively broadband due to nature of MMI.

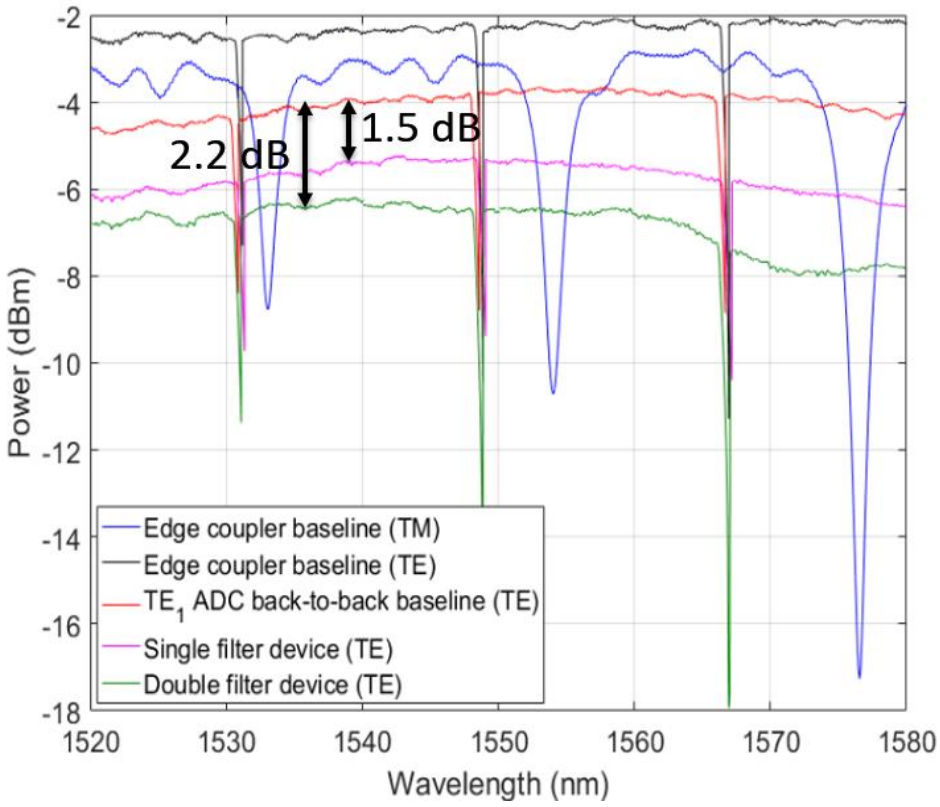


Figure 3.9 Measurement spectrum of filter device with TE_1 input

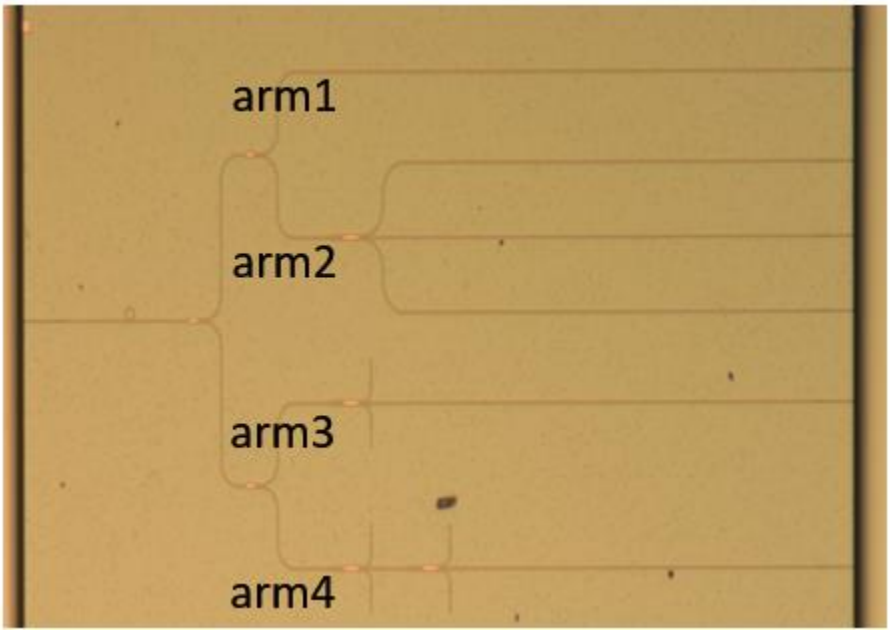


Figure 3.10 Measurement scheme for TE_0 rejection inside a cascaded MMI system

To further valid the performance of TE_0 mode rejection, filter device is tested within a cascaded MMI network as shown in Fig.3.10. With a cascaded 1to2 MMI network, all devices within the MMI system are sharing the same input edge coupler to further reduce measurement uncertainty caused by edge coupling (~ ±0.5 dB). On the other hand, MMI network will build up accumulated reflection, which can make measurement spectrum slightly noisier.

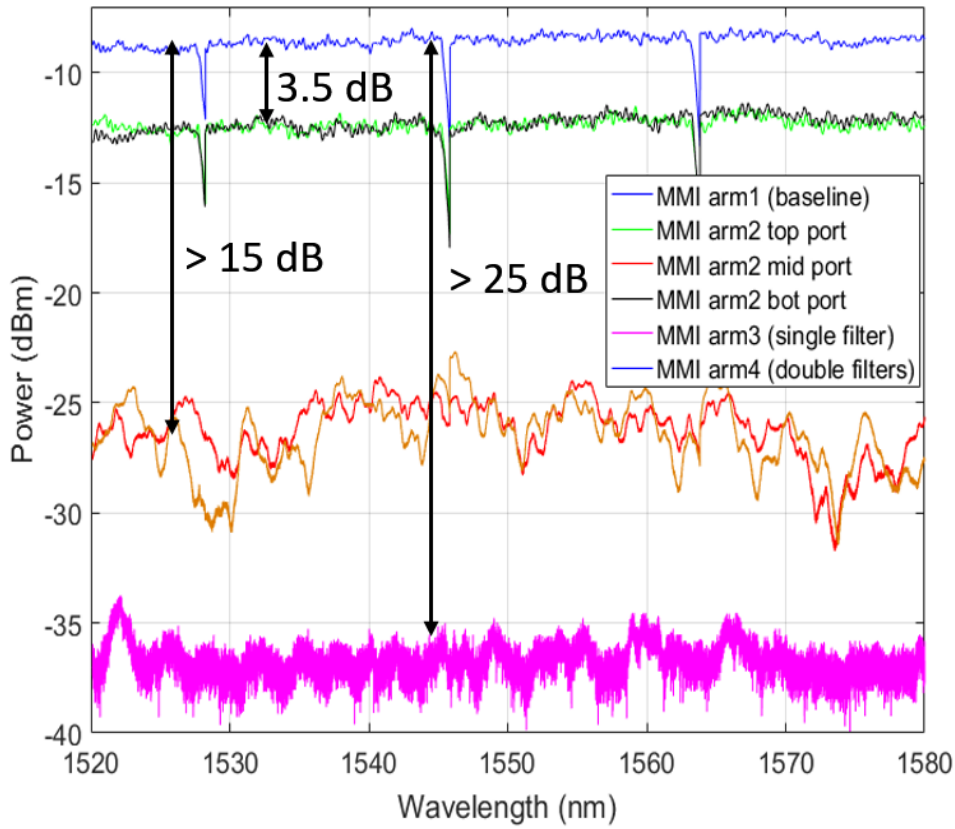


Figure 3.11 Measurement spectrum of filter device with TE_0 input

Fig.3.11 shows the measurement results of arm 3 in the MMI system that investigate the TE_0 rejection through a single filter device. Comparing with MMI baseline, over 15 dB TE_0 rejection (mid port) has been demonstrated over 60 nm bandwidth. The attenuated power however, is strongly measured at top and bottom port, which agrees with simulation. Around -3.5 dB efficiency is measured at both top and middle port, which agrees nicely with -3.2 dB normalized transmission in simulation. Although reflection is not directly measured from the chip, strong power transmission via top and bottom port still gives strong indication that TE_0 is rejected by radiation instead of reflection.

Eventually mode filter under two mode concurrent input is numerically investigated. It's worth mentioning that a truly practical MDM device must remain in operation when multiple mode channels are injected simultaneously. Almost all reported MDM devices are merely treated as linear systems and claim to work under separate mode inputs. However, this does not mean those devices can still operate when input is the mode beating pattern from multiple orthogonal modes, which is also challenging especially because there is no control over the phase relationships between modes.

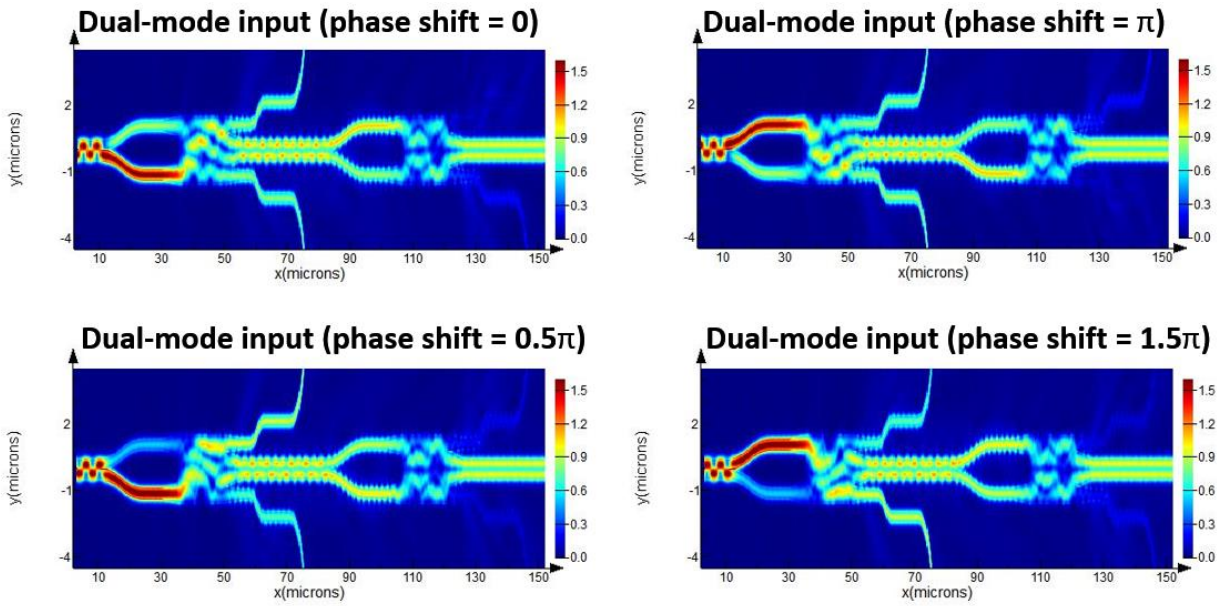


Figure 3.12 |E| distribution for cascaded filter under 1:1 TE_0/TE_1 mode input

Fig.3.12 shows the FDTD calculated |E| distribution under TE_0 and TE_1 concurrent input with various phase relationship. The powers along the central waveguide are consistent over four phase conditions, showing clean TE_1 mode profile without mode beating after two mode filters. The calculated spectrums are also phase insensitive, though spectrum figure is not shown here. Phase insensitivity only appears along the central waveguide since beam travels along such horizontal symmetric structure prohibit mode conversion between TE_0 and TE_1 mode. Therefore, to design a two-mode-division multiplexing device with horizontal symmetry and make the beam of interest to travel along the symmetry axis can be one solution to solve the phase sensitivity problem.

The following table shows the comparison with other pervious demonstrations. Although SWG/Bragg reflector based filter gives the best performance, TE_0 rejection by reflection makes such device impractical. Mode switch based filter is bulky and more importantly TE_1 mode power transmission suffers phase dependent spectral fluctuations. The MMI based filter proposed in this work offers decent performance with reasonable footprint. In addition, TE_0 is rejected by radiation and TE_1 transmitted immune to phase sensitivity.

Table 3 Comparison with previous reported high order mode pass filter

State-of-art works for comparison	**Footprint**	**Measured performance**	**Problems or comments**
SWG/Bragg reflector based filter	15 μm long on SOI platform	1.8 dB excess loss for TE_1 and 50 dB TE_0 rejection	TE_0 is filtered by strong reflection (not practical)
Mode switch based filter [55]	11 mm long polymer waveguide	2.2 dB excess loss for TE_1 and 20 dB TE_0 rejection	Massive footprint and theoretically suffer from phase sensitivity
MMI based filter (this work)	60 μm long on SOI platform	< 1.5 dB TE_1 excess loss over C band and 15 dB TE_0 rejection	TE_0 is filter by strong radiation and theoretically immune to phase sensitivity

In conclusion, an SOI high order mode pass filter is proposed and experimentally demonstrated. The filter device shows < 1.5 dB insertion loss over C band and > 15 dB TE_0 filtering. TE_0 power is rejected by radiation and the filter device based on MMI suffers negligible reflection compared with the previous Bragg reflector solution [60]. The same principle should also work for TM polarization as well where alternative MMI dimension is needed. To our knowledge, this is the first practical experimental demonstration of high order mode pass filter on SOI platform. Surprisingly, this filter device also numerically proves to works for dual modes input under various

relative phase shift. Such feasible filtering solution can be widely used for on-chip two-mode division multiplexing system to cleanse the channel crosstalk.

3.4 TE_1/TE_0 multiplexed 3 dB power splitter

Another challenge for on-chip MDM system is power splitting, which severely hinder its applications. To split MDM signal is not straightforward by conventional methods such as Y junction, MMI or star coupler. There exists a challenge to split high order modes and fundamental mode simultaneously.

Over recent years, some MDM 3 dB power splitting solutions are proposed, which mainly works for dual mode multiplexing at TM polarization. Fig.3.13 shows the dual-mode 3 dB directional coupler published by Y. Luo in 2016 [62]. This design efficiently splits both two modes into 50:50 ratio at targeted wavelength and less than 25 μm long device footprint is impressive. Nonetheless, directional coupler is not a truly ideal power splitting solution because power splitting ratio is strongly wavelength dependent. In addition, phase difference will always be introduced at through port and cross port [63], leading to in phase 3 dB power splitting impossible. In phase 3 dB splitting is vital because it allows the reverse operation as power combiner when two inputs are in-phase.

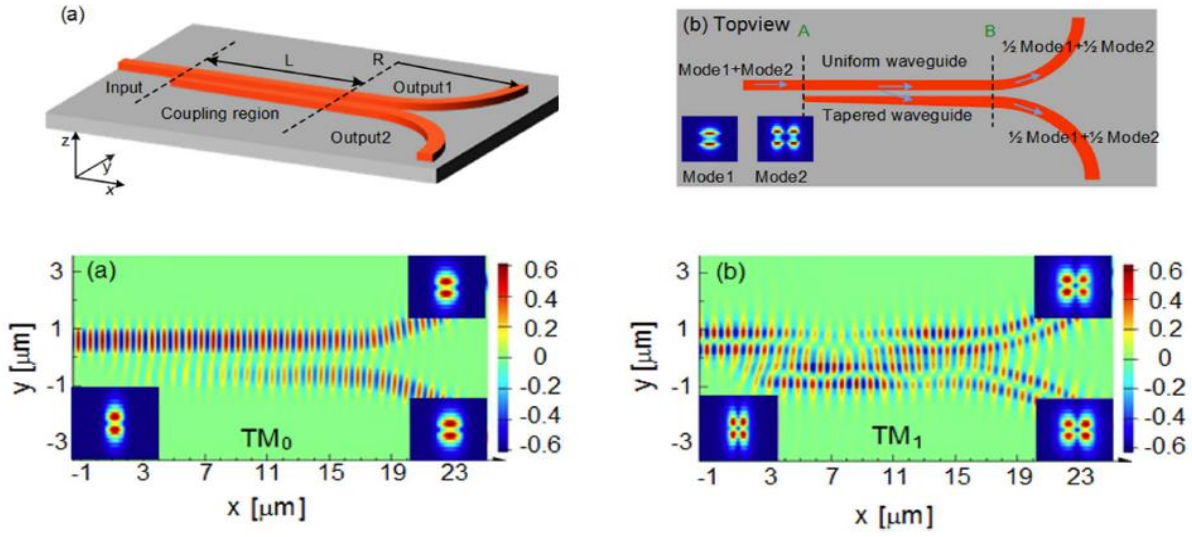


Figure 3.13 Previously reported 3 dB directional coupler for TM_0/TM_1 multiplexing [62]

Another 3 dB power splitting solution (Fig.3.14) is published by H. Xu in 2016 [64], which utilize ADC to convert dual input modes into TM1 and TM3 and ultimately to splits into TM_0 and TM_1 pairs using a symmetric Y junction. This design takes ~ 120 μm long footprint but offers lower wavelength dependent splitting ratio, but such device based on ADC still does not lead to broadband operation. More importantly, this splitter will split TM_0 into anti-phase TM_0 pairs while TM_1 into in-phase TM_1 pairs. The inability to split both modes in phase also hinder its applications and it's almost impossible to introduce phase delay to one mode only without affecting the other one.

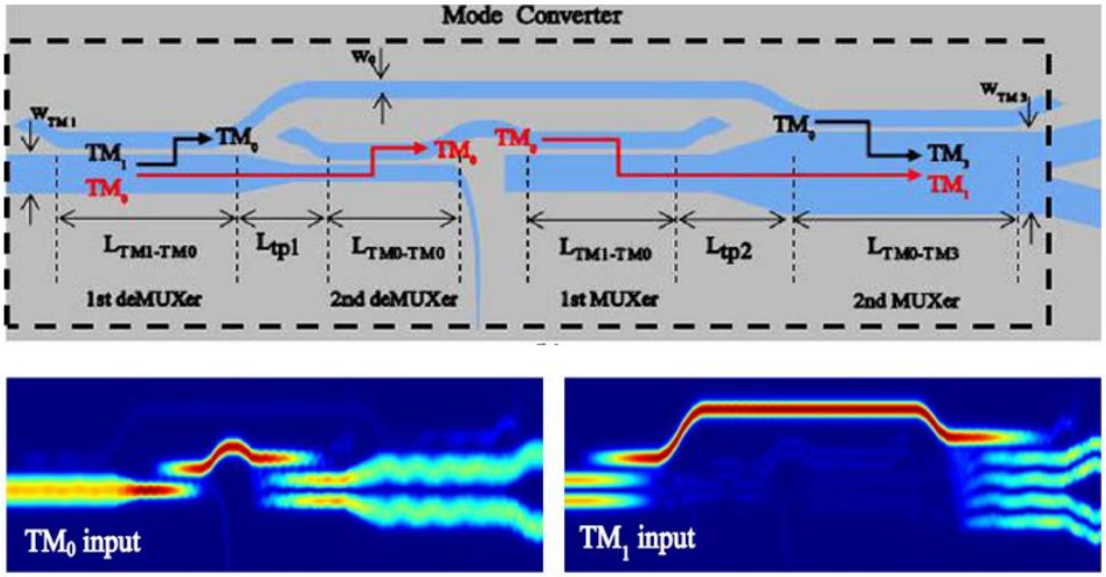


Figure 3.14 Previously reported 3 dB splitter for TM_0/TM_1 multiplexing on SOI platform based on Y junction and ADC [64]

More recently a dual-mode 3 dB splitter based on inverse design is demonstrated and published in 2018 CLEO conference. Such design shows extreme compactness and it can split dual modes in-phase over broad bandwidth. This is the best demonstration so far, yet the disadvantages of high reflection and extreme fabrication sensitivity cannot be ignored.

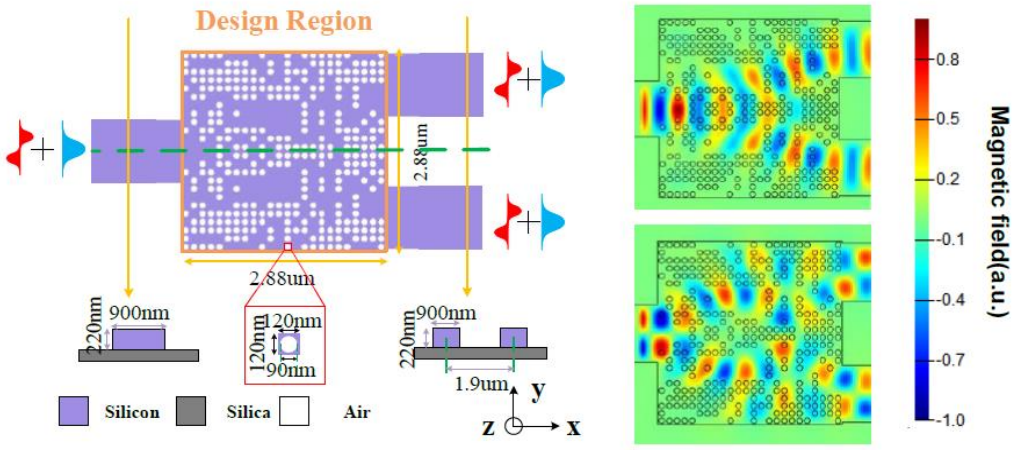


Figure 3.15 TE_0/TE_1 multiplexed 3dB splitter on SOI platform based on inverse design [65]

Nonetheless, all previously reported dual-mode 3dB splitter does not offer phase insensitivity operation under dual-mode concurrent input. Due to nonlinear term at power both top and bottom port, both shows phase dependent spectral fluctuation, leading to splitting ratio far away from 1:1. From mode beating point of view, due to the absence of symmetry the input field also cannot be equally divided into two pieces.

This section introduces several theoretical in-phase splitting solutions for TE_0/TE_1 multiplexing are proposed and numerically investigated. The first solution based on single Si layer MMI offers broadband 1:1 power split but suffers phase sensitivity under dual mode concurrent input. The second solution is based on polarization rotation relying on SiN/Si hybrid structure, which is theoretically immune to phase sensitivity when dual modes are injected simultaneously. Both broadband 3 dB splitter with large foot print and narrowband 3 dB splitter with compact footprint are proposed.

Fig.3.16 illustrates the schematic of phase sensitive broadband 3 dB splitter on a single-layer SOI platform. The device starts with MMI mode splitter used in two-mode Demux [61]. The central output port is further split equally by a MMI, leading to inner TE_0 pairs from TE_0 input and outer TE_0 pairs from TE_1 input. Ultimately two identical demultiplexer are deployed to couple back to TE_0 and TE_1 mode respectively. Here 2 by 2 MMI with 90-degree phase shift is used due to good balance between efficiency, crosstalk, and footprint. Theoretically other demux solutions (such as ADC, asymmetric Y junction [66] and inverse design [67]) can also be used. Due to the nature of

MMI, broadband operation can theoretically be achieved. Due to the mirrored Demux device, the entire splitter could surprisingly lead to in-phase splitting for both TE_0 and TE_1 input individually. This happens because the mirror symmetry introduces another 180-degree phase shift, which compensate the phase difference between TE_0 and TE_1 pairs.

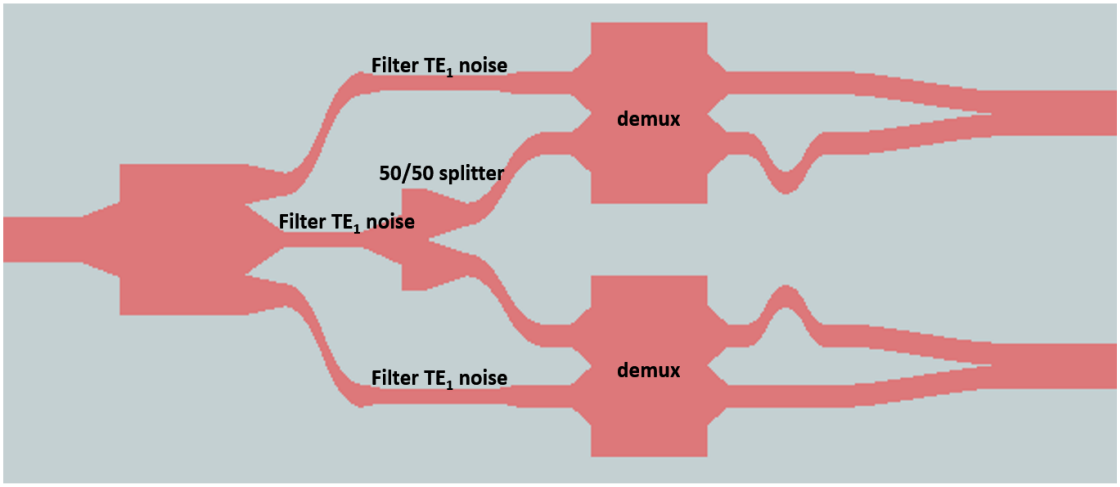


Figure 3.16 Schematic of the TE_0/TE_1 multiplexed 3 dB splitter

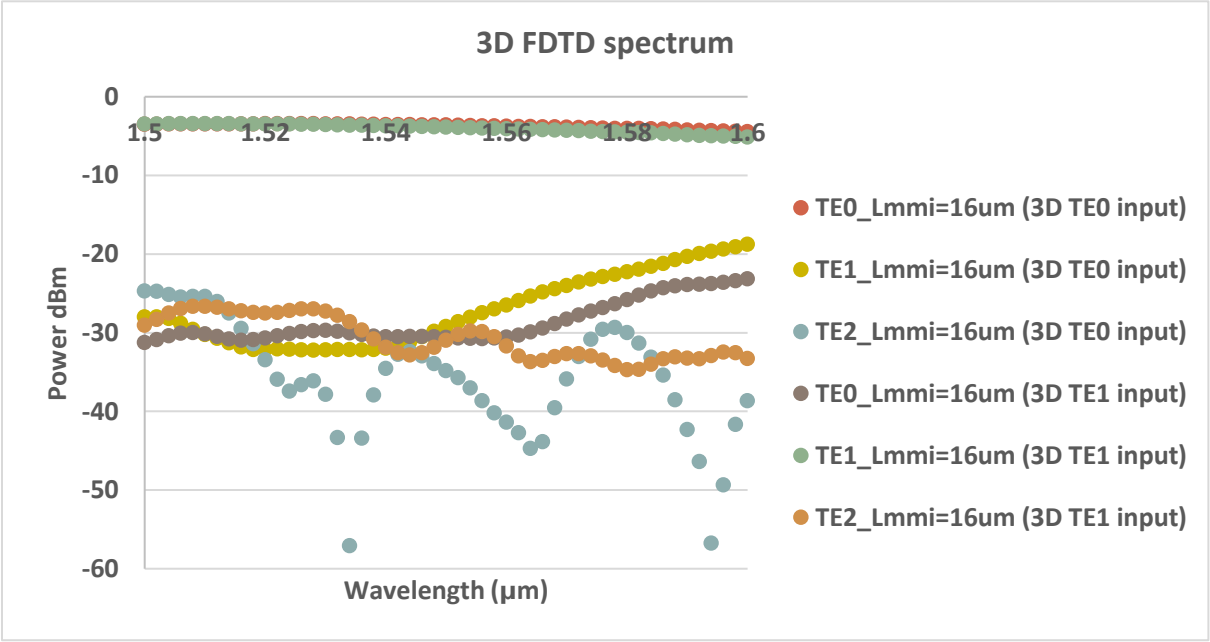


Figure 3.17 FDTD calculated output spectrum (top waveguide)

The entire splitter device is simulated with TE_0 and TE_1 mode input respectively using Lumerical FDTD. Simulation shows both output waveguides obtain the correct mode with 3 dB power splitting at high extinction ratio. Fig.3.17 illustrates the top output port spectrum which is identical to the bottom port, showing around 4 dB insertion loss and over 20 dB extinction ratio over broad bandwidth for both mode inputs. Field distribution plot in Fig.3.18 also shows clearly that both TE_0 and TE_1 can be split into two pieces with little modal crosstalk.

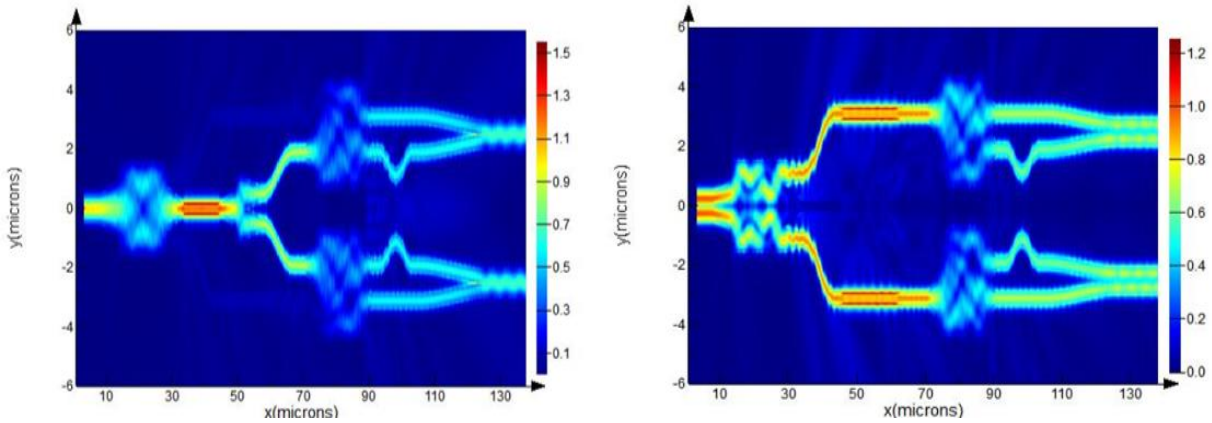


Figure 3.18 Simulated |E| top view for TE_0 and TE_1 mode input respectively

To validate the TE_0 or TE_1 mode pairs after splitter are in phase, GDS layout is designed to excite TE_0 or TE_1 pairs in phase and use the splitter in reverse direction as a combiner. Such design is simulated in Fig.3.19 and Fig.3.20. TE_0 mode input is split into in-phase TE_0 pairs by a 1-to-2 MMI and subsequently travel through the combiner to get combined. Simulation clearly shows that an in-phase TE_0 pairs generated from MMI can recombine into a single TE_0 mode. Similarly, an in-phase TE_1 pair can be generated by cascading compact TE_0-to-TE_1 converters [68] on both output arms of MMI. FDTD simulation also shows an in-phase TE_1 pairs can combine into a single TE_1 mode effectively. As a result, it's safe to claim such dual mode splitter gives in-phase 3 dB power splitting and such configuration will be used on GDS layout for experimental validation.

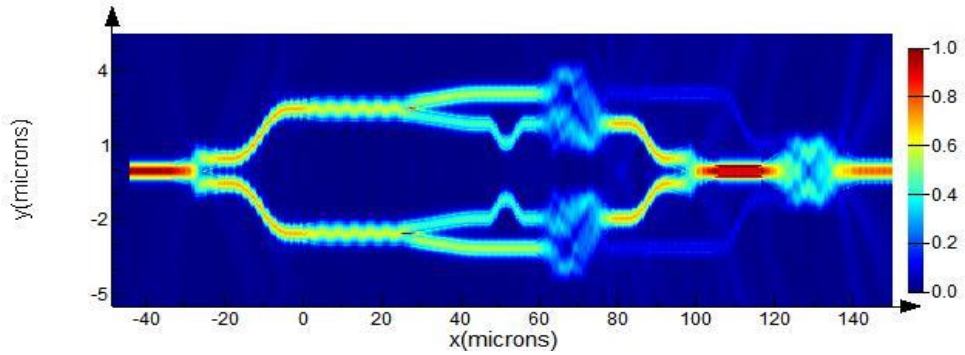


Figure 3.19 FDTD calculated |E| top view of MDM combiner with in-phase TE_0 pair input

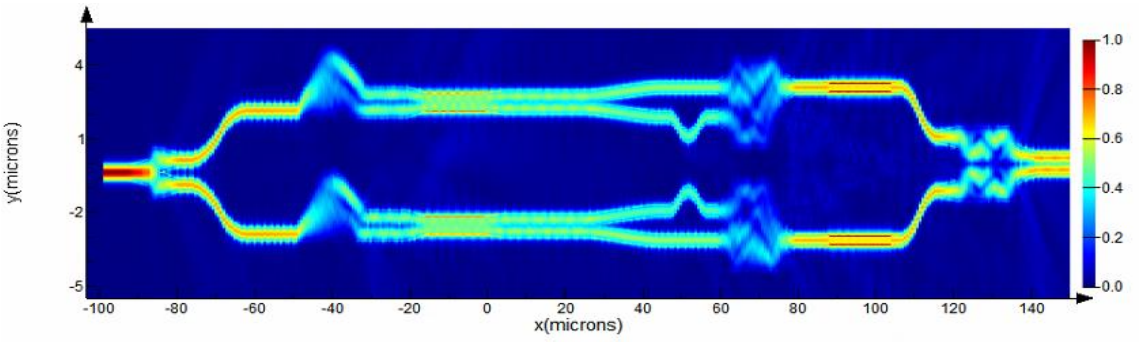


Figure 3.20 FDTD calculated |E| top view of MDM combiner with in-phase TE_1 pair input

While this solution seems to perform well for TE_0 and TE_1 mode input individually, when TE_0/TE_1 mode beating pattern is injected the story becomes quite different. Here the same structure is excited under TE_0 and TE_1 two modes concurrently under various relative phase shift. When input mode is the beating pattern which is neither symmetric nor antisymmetric, the first stage MMI cannot always ensure equal power split into top and bottom port. In Fig.3.21, clearly 0 phase shift between TE_0 and TE_1 renders more power though top port than bottom, leading to power splitting deviating from 1:1 ratio. The splitting ratio is becoming more ideal under certain phase (such as 90-degree phase shift) that drives the first stage MMI to offer similar power splitting at top and bottom port. Due to non-trivial mode crosstalk (~ -25 dB), phase insenstive operation is difficult to achieve, which requires approximately -40 dB crosstalk.

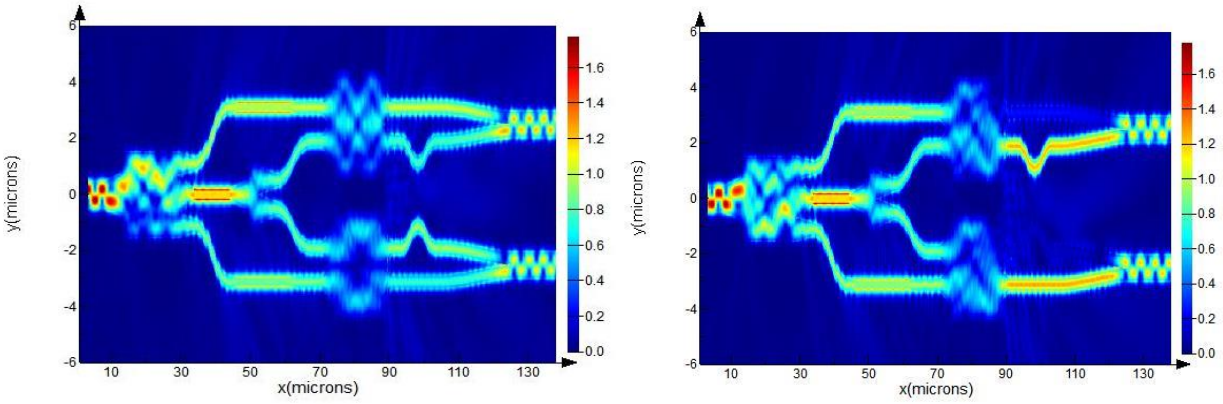


Figure 3.21 FDTD calculated |E| top view under 0 phase shift (left) and 90-degree phase shift (right)

Another way of undertanding the phase sensivity phoenomon is that optical paths of two individual mode inputs are overlapped, which can interfere with each other when two modes are concurrently injected. Although dual modes are orthognal inside the bus waveguide, the self imaging patterns in side the MMI from two different modes are no longer orthognal hence strong interefnce behavior will occur. With various phase shift between two inputs, interference pattern behave differently, leading to phase sensitive behavior. The special case is the beam that travels along the central axis with horizontal symmtry (such as mode filter devcie) where TE_0 and TE_1 mode conversion is prohibted. However, for such MMI based power splitter it's difficult to make all three routes from 1st stage MMI to have horizontal symmetry hence MMI based splitter is unlikely to avoid phase sensntivity problem under dual modes input.

Another design for TE_0/TE_1 3 dB splitter is illustrated in Fig.3.22, which utilize polarization rotation. The basic idea is to transform TE_1 input into TM_0 mode while preserving TE_0 input unchanged using a tapered structure. Polarization rotation is only possible when vertical symmetry is broken [69][70][71] and here 200 nm thick nitride structure is stacked on Si to allow polarization rotation. The entire structure is under SiO_2 top cladding and a Y junction is used to equally split power at both polarizations. Y junction is deployed without SiN film to eliminate polarization rotation at the Y junction where vertical symmetry is sustained.

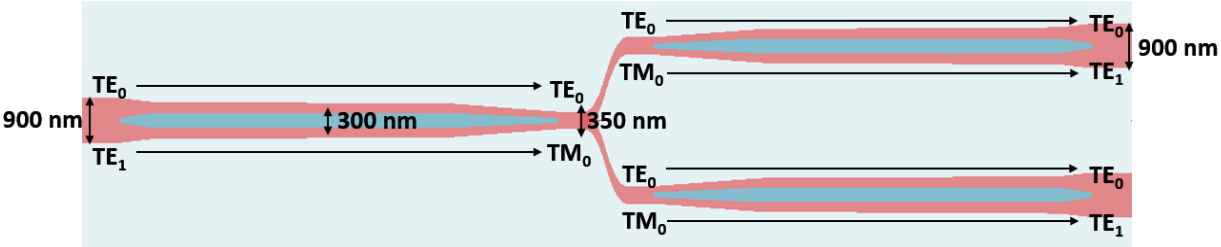


Figure 3.22 Schematic of the SiN on SOI TE0/TE1 multiplexed 3 dB splitter

The polarization rotator (PR) section design starts with neff calculation where 200 nm thickness SiN film (300 nm width) is stacked on top of Si waveguide. Figure 3.23 shows the scanned neff of top three best guided modes (TE_0, TM_0 and TE_1) under various Si waveguide width at 1550 nm wavelength. Obviously, mode crossing appears at 732.5 nm Si waveguide width, where neff difference is less than 0.04 to ensure effective phase matching.

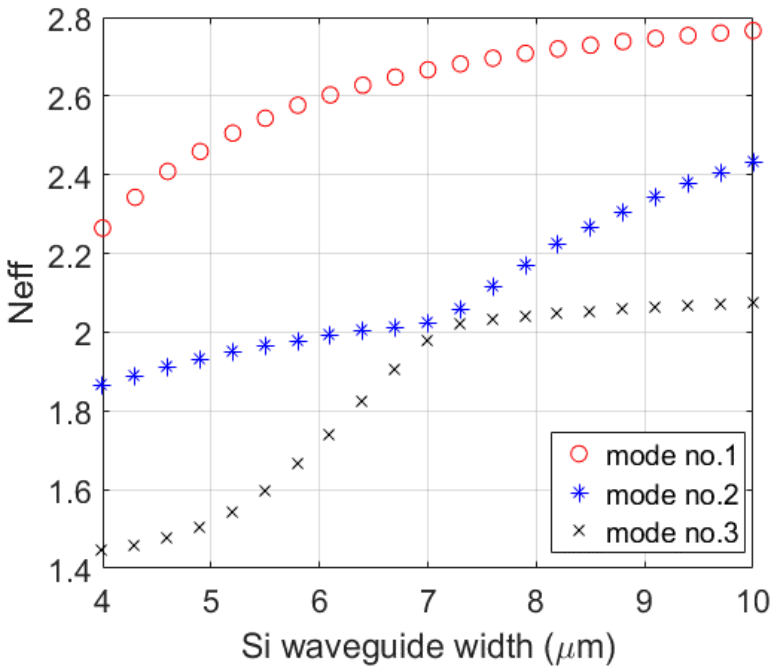


Figure 3.23 Neff of Si waveguide width scan with 300 nm wide 200 nm thick SiN stacked on Si

There are two methods to utilize the mode crossing [72] to achieve TE_1-to-TM_0 conversion. The first solution is to use long taper around the mode beating region to achieve broadband polarization rotation. For example, with mode crossing at 732.5 nm Si waveguide width, ± 70 nm width around

mode crossing is assigned to the majority part of taper (L2) and remaining segment (L1 and L3) of width variation can be kept short. EME simulation at 1550 nm wavelength dictates very long taper is needed for efficient polarization rotation as shown in Fig.3.24. When L1 and L3 are short there are observable efficiency oscillations along L2 scan due to non-adiabatic transition. For footprint concern, 75 µm L1 and L3 are chosen for non-adiabatic transition and 250 µm L2 is used which gives > 98% broadband efficiency.

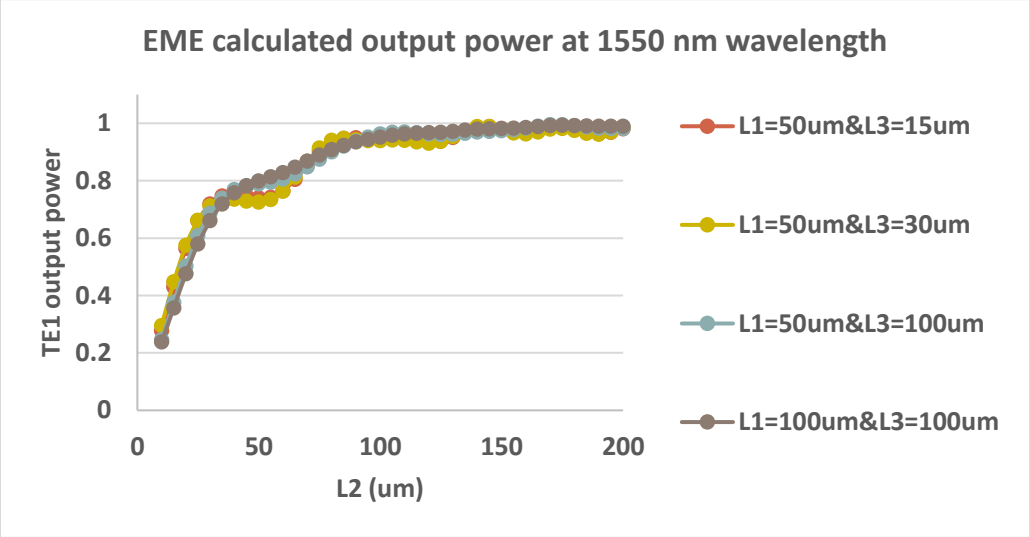


Figure 3.24 PR taper EME scan of L2 at 1550 nm wavelength

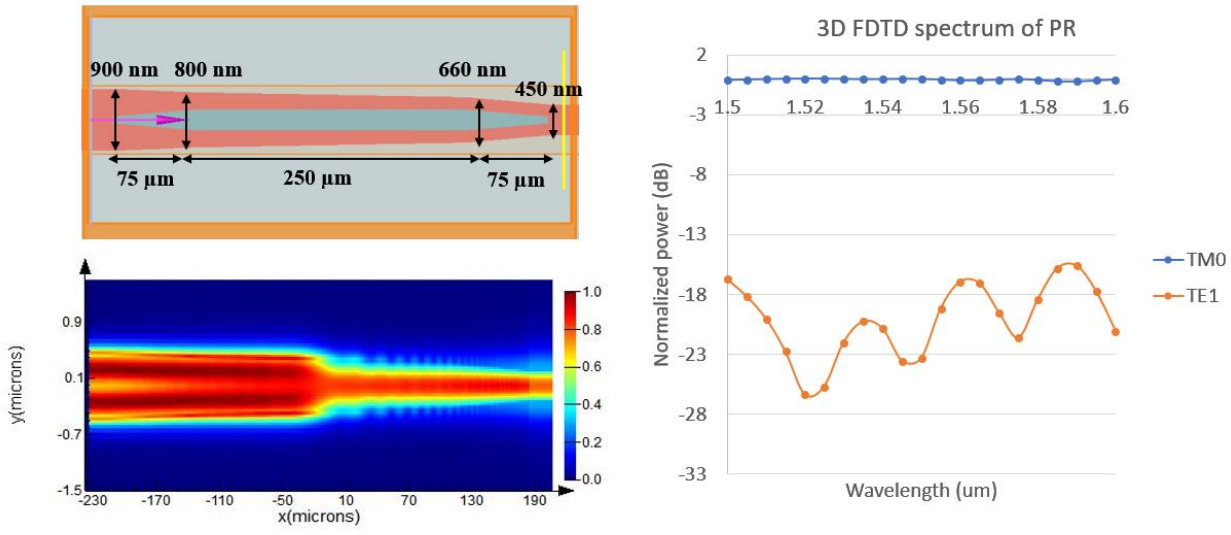


Figure 3.25 PR taper structure and FDTD simulation results

It's worth mentioning that no matter how long the taper is used, there will always be unconverted TE_1 mode power (around -20 dB in this example) remaining [73]. The ripple of TE_1 power remaining also indicates some spectral fluctuation of TM_0 power after PR and theoretically longer L1 & L3 can help reducing the fluctuation. Before cascading the Y junction, the TE_1 residual must be removed by tapering the waveguide. The reason is that remaining TE_1 will beat with TE_0 when dual modes are simultaneously injected, and the field pattern is phase sensitive and without symmetry hence will again cause power splitting ratio deviating from 1:1. To filter TE_1 power, the waveguide is tapered down to a 15 μm long 300 nm wide section to cut off TE_1 mode and meanwhile TE_0 and TM_0 will suffer some propagation loss. Hence, it's also important that TE_1 mode cannot be filtered too heavily such that TE_0 and TM_0 suffer considerable loss.

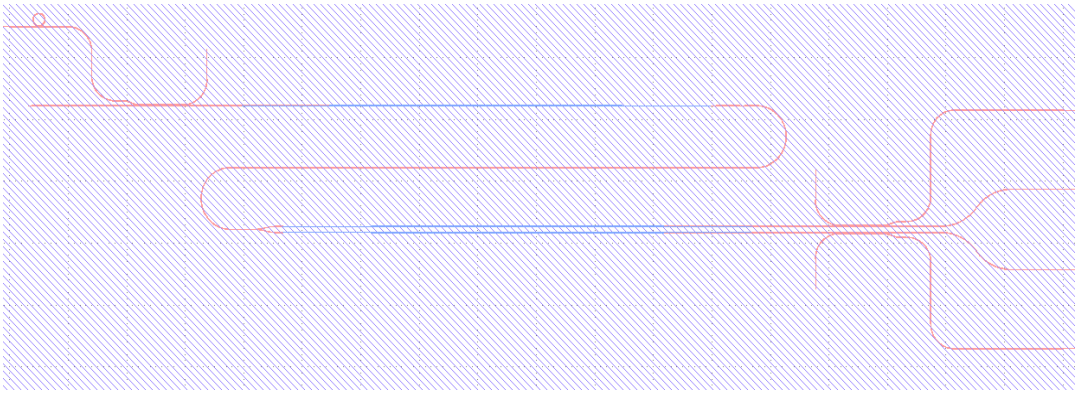


Figure 3.26 GDS layout for dual modes 3 dB splitter measurement under TE_1 input

The entire splitter is not going to be simulated by 3D FDTD because of its massive footprint. Since the actual splitter device based on 400 μm long PR is too long, on the GDS layout a S bend is used to squeeze the total device length in order to fit into a single field size of Ebeam lithography. This solution (Fig.3.26) however includes ~ 400 μm long Si waveguide where additional propagation loss and bending loss will be incorporated. Hence during measurement additional loss can be characterized and estimated using spiraled waveguides (see chapter 2) or can be normalized by making baseline device also ~ 400 μm longer.

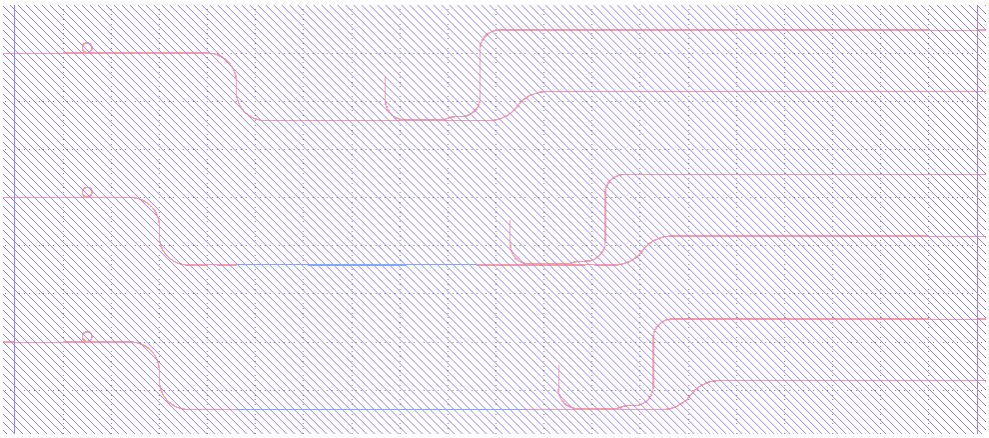


Figure 3.27 GDS layout for PR efficiency measurement

The efficiency of PR should also be experimentally characterized and Fig.3.27 gives the layout design for PR measurement. Here input mode becomes TM_0 and pure TM polarization can be found by maximizing the low Q (TM) ring resonance. Then after PR in reverse direction, majority of power is converted into TE_1, that can be subsequently extracted from TE_1 ADC. Both TE_1 and remaining TM_0 power can be measured and by normalizing the insertion loss of TE_1 ADC, efficiency of PR can be experimentally quantified. On the layout, multiple L2 length is used to validate the trend in Fig.3.24.

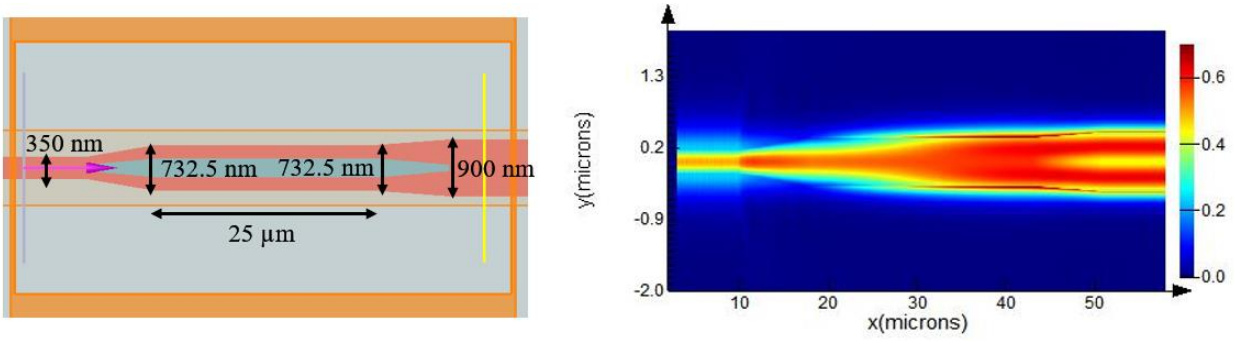


Figure 3.28 (a) Top view schematic of compact narrowband PR (b) Top view FDTD |E| plot at 1550 nm wavelength

Another solution is much more compact, which however sacrifice the bandwidth of PR [74][75]. To best utilize the mode crossing section, a 732.5 nm wide straight waveguide is deployed between two sharp tapers. As shown in Fig.3.29, EME scan the straight PR section to find 25 µm gives the

highest mode conversion efficiency in the power oscillation pattern. Unlike using lengthy taper PR, the straight waveguide PR can be much more compact but also very dimension and wavelength sensitive.

The PR is simulated using 3D FDTD to give the entire spectrum where the peak efficiency of 98% can be obtained at 1550 nm wavelength. The results slightly deviate from EME because the best efficiency in EME is spectrally shifted. Eventually the entire splitter device (140 μm long) based on such PR is simulated and Fig.3.30 gives the |E| plot at central wavelength, indicating efficient 50/50 power split. With the same strategy, short TE1 cut-off section is deployed before the Y junction.

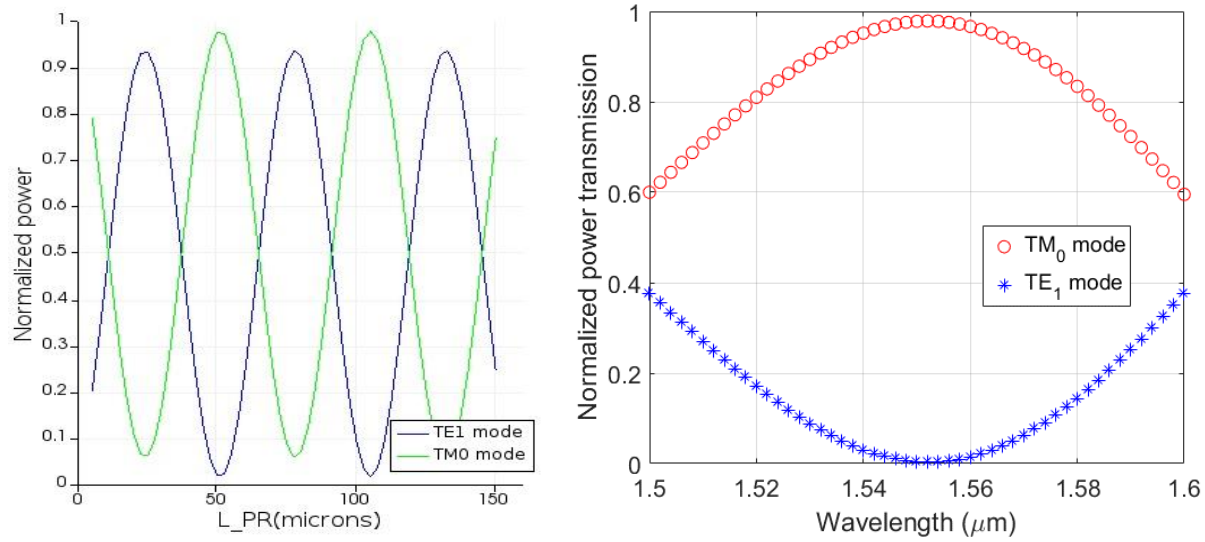


Figure 3.29 (a) EME calculated output power at 1550 nm wavelength with scanning waveguide length where L1 = L3 = 8 μm (b) 3D FDTD spectrum of compact narrowband PR

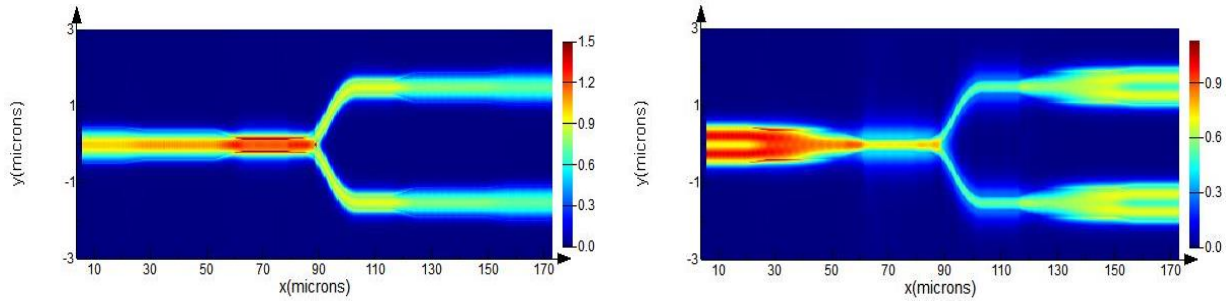
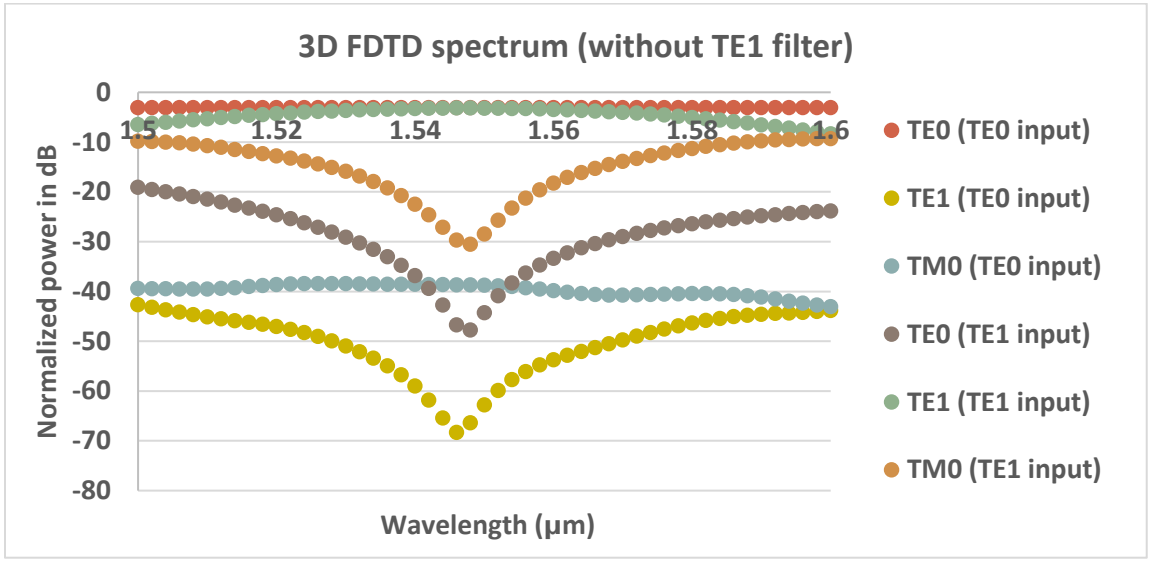


Figure 3.30 (a) 3D FDTD |E| top view at 1550 nm wavelength with TE_0 input (b) 3D FDTD |E| top view at 1550 nm wavelength with TE_1 input

Fig.3.31 gives the spectrum of splitter under two mode input individually. TE_0 input is almost lossless because it does not experience any mode polarization rotation due to phase (Neff) mismatch. TE_0 input suffers 3.07 dB insertion loss over 100 nm bandwidth in simulation where the loss is only attributed from the Y junction. TE_1 mode input shows narrowband insertion loss due to PR yet < 3.25 dB insertion loss is numerically demonstrated over 20 nm bandwidth. When deviating from central wavelength, both TE_1 insertion loss and TM_0 crosstalk will increase. Accumulated TM_0 power may not necessarily a threat and it can be removed by rigorously designed ADC (see section 4.2).



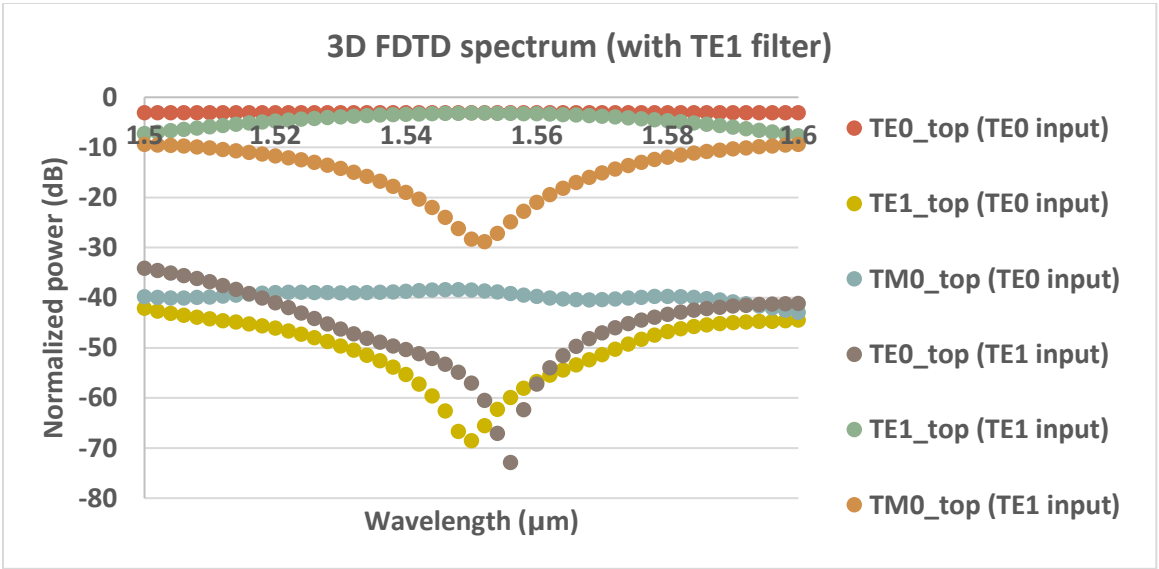


Figure 3.31 (a) 3D FDTD spectrum of one output port without TE_1 cut off (b) 3D FDTD spectrum of one output port with TE_1 cut off

The effect of TE_1 cut off section can be observed under TE_1 mode input directly. Especially when away from central wavelength, TE_1 residual can couple to TE_0 after Y junction. This potentially makes device phase sensitive because the TE_0 component from TE_1 residual (modal crosstalk) will interfere with TE_0 mode input. With TE_1 cut off section however, additional 15-20 dB TE_1 attenuation is introduced to further alleviate such phase sensitive interference phenomenon. This will further squeeze the modal crosstalk down to -50 dB over C band to reduce phase sensitivity.

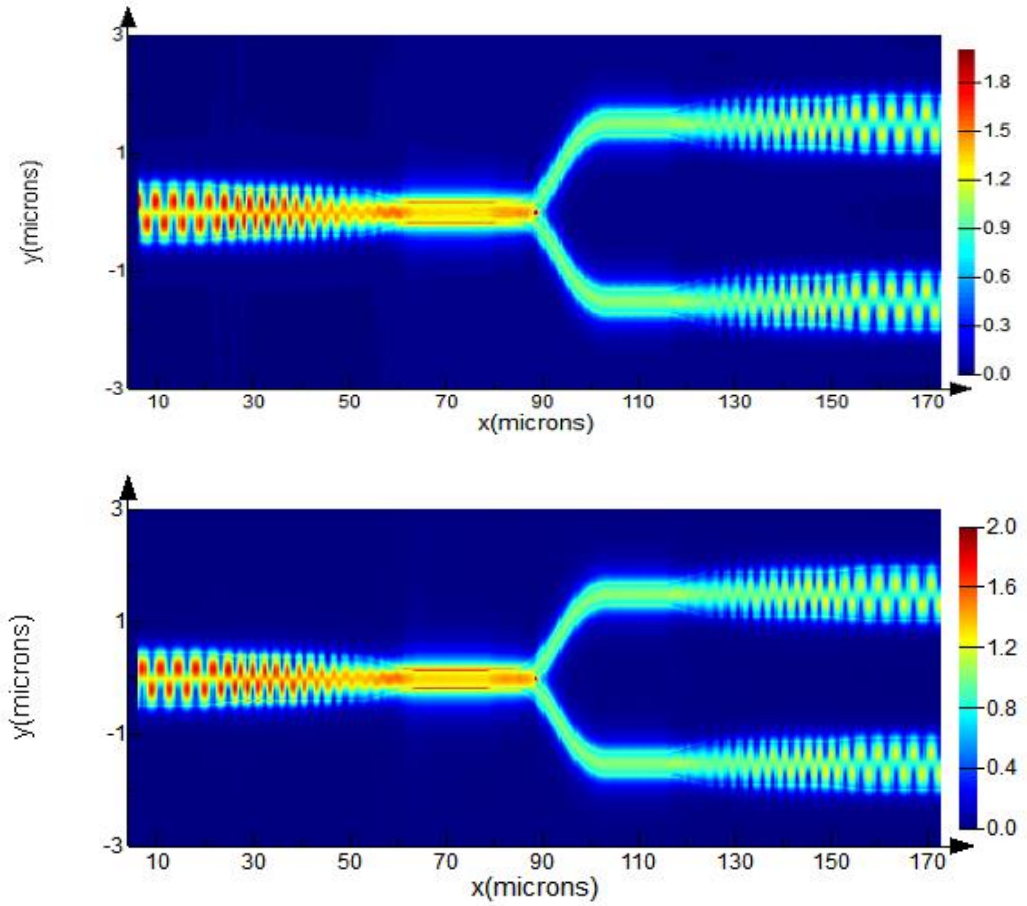


Figure 3.32 (a) FDTD |E| top view of under dual modes concurrent input with 0-degree relative phase shift (b) FDTD |E| top view of under dual modes concurrent input with 90-degree relative phase shift

Simulation results are shown in Fig.3.32 and Fig.3.33. With TE_1 power cut off section, TE_1 only suffer marginally phase sensitivity spectral fluctuation. Since the device is designed for narrowband operation, it's safe to claim within 20 nm bandwidth around central wavelength phase sensitivity problem is negligible. Once deviating away from central wavelength, increased TE_1

residual will occur even after TE_1 cut off section, which will disrupt the power splitting ratio. Of stronger TE_1 attenuation can be used at cut off section to eliminate TE_1 mode, yet higher TE_0 and TM_0 propagation loss can be included. For the MDM splitter based on broadband long PRs, TE_1 power residual remains low over broad bandwidth thus phase sensitivity becomes much less threatening compared with MDM splitter based on narrowband compact PRs.

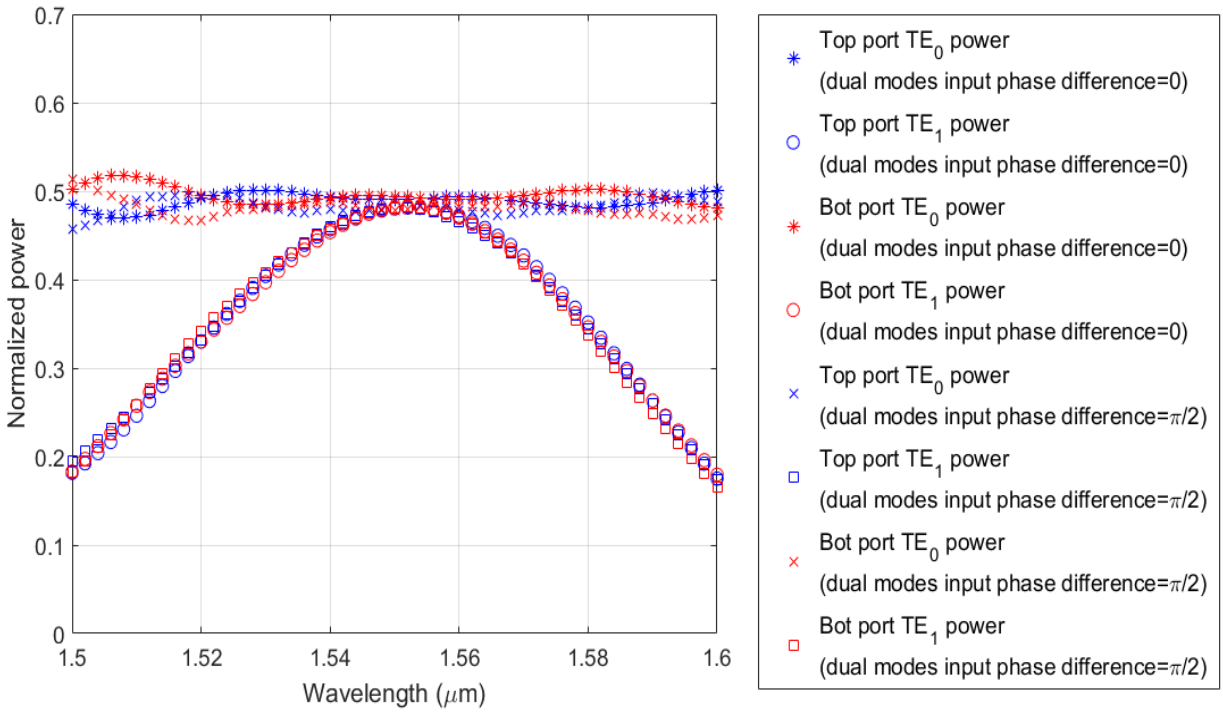


Figure 3.33 3D FDTD calculated spectrum of MDM splitter under dual modes concurrent input with 0-degree and 90-degree relative phase shift

Additionally, such splitting scheme is easily scalable. For some applications such as OPA to split power into many (~ 128) pieces in phase is needed. Although it's not clear whether high order modes can be useful in OPA yet, to split MDM signals into many pieces is potentially demanded. The MDM splitter based on PR is very convenient to scale up by cascading Y junctions only without significant insertion loss elevation because two PRs primarily limit the device's efficiency. By cascading Y junction only also saves the device footprint and Fig.3.34 shows 1-to-8 is numerically demonstrated on 270 μm long device. -9.2 dB TE_0 power and -9.3 dB TE_1 power is simulated at central wavelength, showing it can be scaled up with ultra-low loss.

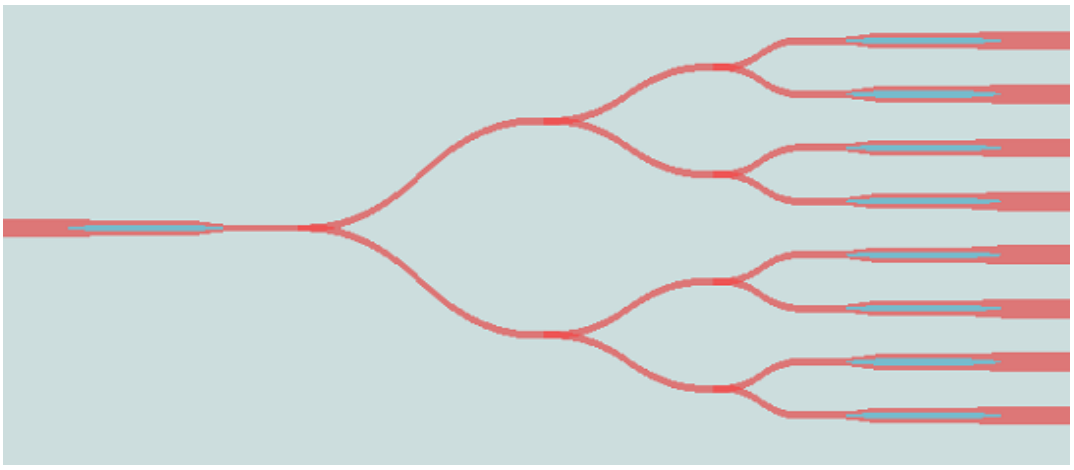


Figure 3.34 schematic of 1-8 dual-mode3 dB splitter

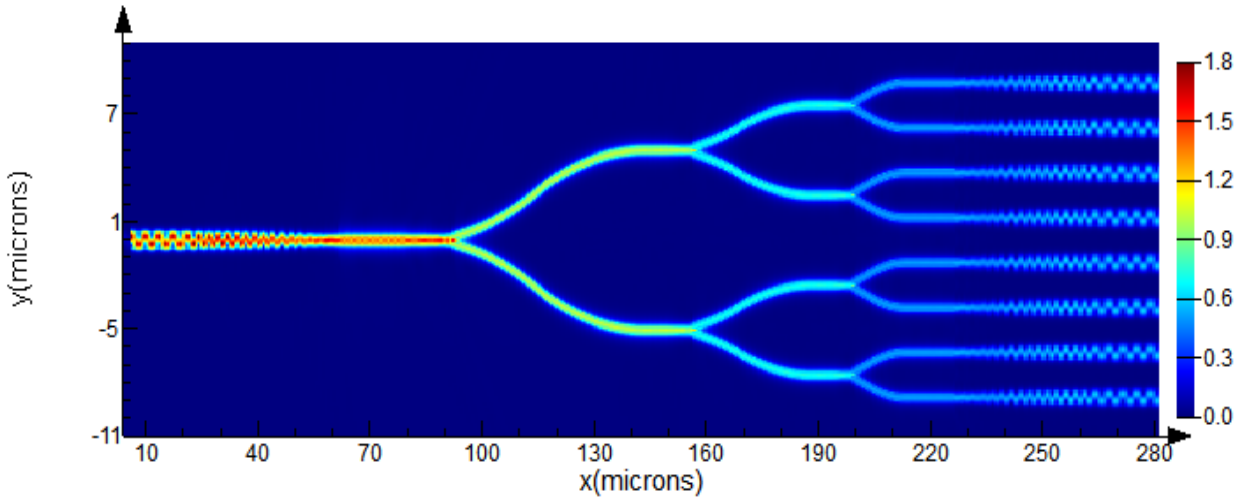


Figure 3.35 3D FDTD |E| top view of 1-to-8 splitter under TE_0/TE_1 concurrent input

As a summary, the dual mode 3 dB splitter is reported with previously reported works as shown in Table 4. Although our design is not quite compact, it appears to be the only phase insensitive solution. The reason is that modal crosstalk under TE_1 input (caused by TE_1 residual from PR) can always be annihilated with TE_1 filter under costs of insertion loss. A crosstalk-free splitter can be numerically demonstrated to get immune to phase sensitivity while all previous demonstration cannot. Our design is also easily scaled up with little loss and reflection, which stands as another unique advantage.

Table 4 Comparison with previously reported dual mode 3 dB splitter

State-of-art works for comparison	**Footprint**	**Performance at central wavelength**	**Pros and Cons**
Dual mode (TM) 3 dB directional coupler	~ 20 μm length	0.7 dB insertion loss and -14 dB crosstalk measured	Not in-phase splitting and narrowband performance Phase sensitivity
Dual mode (TM) splitter based on ADCs and Y junction	~ 120 μm length	0.86 dB insertion loss and -15.7 dB crosstalk measured	Not in-phase splitting and narrowband performance. Phase sensitivity.
Inverse design splitter (air cladding)	~ 3 μm length	1.5 dB insertion loss and -20 dB crosstalk measured	Extremely compact, in-phase splitting and broadband performance Phase sensitivity, fabrication sensitivity & high reflection
Splitter with polarization rotation (this work)	~ 150 μm length	0.2 dB insertion loss, negligible crosstalk and -27 dB TM_0 residual simulated	In-phase splitting and narrowband performance Require double layer fabrication Immune to phase sensitivity and easily scalable

3.5 TE_1/TE_0 multiplexed sharp waveguide bend

Sharp bending has been another well-known technical challenge for on-chip MDM system. A single-mode waveguide on SOI platform can be sharply bent (radius < 2 μm) without significant insertion loss and modal crosstalk. Nonetheless, multi-mode waveguide suffers severely from modal crosstalk when under sharp bending, mainly attributed from power coupling between incorrect modes at straight and bending waveguide sections. Therefore, conventionally large bending radius (> 30 μm) is typically required for SOI multi-mode waveguide.

For more condense packing of on-chip MDM systems, a number of sharp bends have been proposed for modal crosstalk suppression. In 2012, transformation optics method is proposed to

design a graded-index multi-mode bend based on grayscale lithography [53]. There's also more recent demonstration of a SOI sharp bend (5 μm radius) with slender shape (width < thickness) [54]. Nonetheless both techniques are not practical for CMOS compatible fabrication.

Two CMOS compatible sharp bend solutions are demonstrated on SOI platform. In 2017, C. Sun [76] used a mode converter to reshape input high order mode profile to match with high order bend mode and consequently suppress the modal crosstalk. The author experimentally achieved 0.2 dB insertion loss and < -22 dB modal crosstalk on a 10 μm radius bend under TE_0 and TE_1 mode input individually. While these results are remarkable, a 10 μm bend radius is still quite large compared with sharp single-mode Si waveguide bend (~ 2 μm radius). The design utilizes mode converters (5 μm long) at two ends of a 90-degree multi-mode waveguide bend (5 μm radius) makes further reduction of bending radius very difficult. More importantly, such bend theoretically does not work under TE_0 and TE_1 mode concurrent input because modal fields from two input modes at mode converter regions (without modal orthogonality) will interfere with each other.

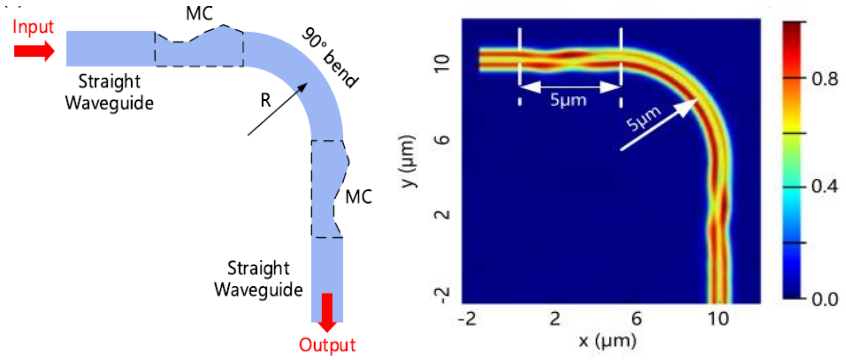


Figure 3.36 TE_0/TE_1 multiplex bend based on mode converter [76]

Most recently in 2018, W. Chang developed a more compact SOI bending solution based on air cladded asymmetric Y junctions [77]. A 3.6 μm radius ultra-sharp bend was achieved with inverse-designed subwavelength structure to mimic two asymmetric Y junction (DEMDM & MUX) deployed with diagonal symmetry. 0.8 dB insertion loss with -24 dB modal crosstalk was experimentally demonstrated under TE_0 and TE_1 input separately. Although performance is quite impressive for an air cladded sharp bend, with SiO_2 top cladding such small bending radius may not be achievable since both asymmetric Y junction and Phc-like subwavelength structure prefer large index contrast. Furthermore, inverse design based on topology optimization is well known

for fabrication sensitivities. Even with Phc-like subwavelength structure, tiny hole radius deviation will cause significant performance degradation. In addition, inverse design cannot be easily adapted to various design, meaning completely new topology needs to be re-optimized for any different bending radius.

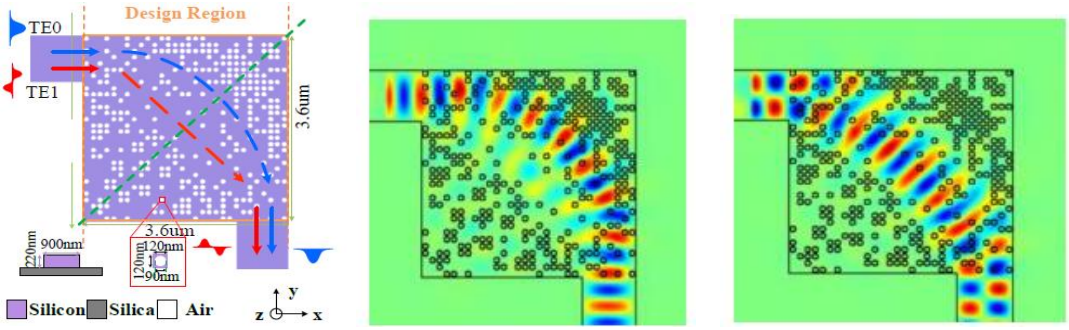


Figure 3.37 dual-mode bend based on subwavelength asymmetric Y junction using inverse design [77]

In terms of TE_0 and TE_1 concurrent input, inverse design bend should also suffer from phase sensitivity issue but less severely than mode converter bend. Although optical paths are different inside asymmetric Y junction for two input modes, some portions of evanescent fields still overlap leading interference. With fabrication error, phase sensitivity phenomenon under concurrent input will become even worse. Considering those disadvantages, on-chip MDM sharp waveguide bend based on inverse design may not be regarded as mature solution for industry.

In this section, an alternative of TE_0/TE_1 multiplexed bend based on symmetric Y junction is proposed. Initially a 3 μm radius bend is developed for TE_0 and TE_1 input individually. A 10.5 μm radius bend is also proposed for phase insensitive dual modes concurrent input. Our bending scheme based on Y junctions works even better for S bend, which is intrinsically phase insensitive. The basic idea of the bend is to mimic a back-to-back symmetric Y junction, which splits TE_0 (TE_1) and merge into TE_0 (TE_1). Due to horizontal symmetry, mode conversion between TE_0 and TE_1 is prohibited. back-to-back symmetric Y junction also works for concurrent two mode input as well, as shown in figure above. For certain phase such that TE_0 and TE_1 combine power solely on one arm and completely cancel power on the other arm, due to reciprocity power will excite 1:1 TE_0/TE_1 beating pattern again at the output waveguide. Since the phase that drives all power choose top or bottom arm work, any different phase should also work as weighted sum of top and bottom routes.

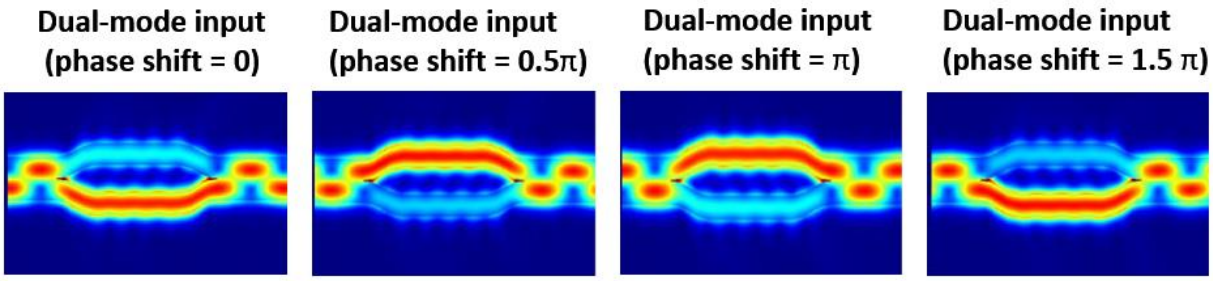


Figure 3.38 Back-to-back Y junction |E| plot under TE_0 and TE_1 concurrent input with various phase shift

The idea can be easily converted to an S bend where the same optical path can be established for inner and outer routes. For a sharp 90-dgree bend the same path length is difficult hence inner and outer routes are designed to offer multiple integer of 2π phase shift for a targeted wavelength. For a targeted wavelength multiple integer of 2π phase shift is equivalent as zero phase shift hence the sharp 90-degree bend is expected to offer high efficiency and low crosstalk over narrow bandwidth around targeted wavelength.

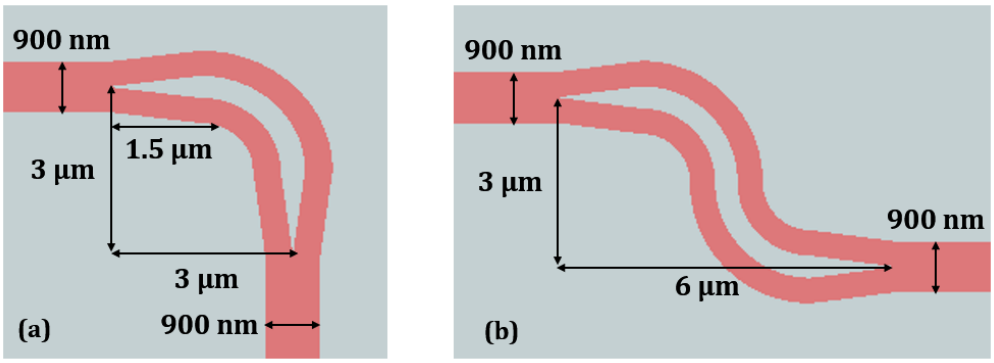


Figure 3.39 (a) 3 µm radius 90-degree bend for TE_0/TE_1 multiplexing (b) S bend for TE_0/TE_1 multiplexing

Figure 3.39 shows the schematic of the TE_0/TE_1 multiplexed 90-degree bend with 3 µm effective radius. Input multi-mode waveguide (900 nm width & 220 nm thickness) first goes through a 1.5 µm long symmetric Y junction, which splits one multi-mode waveguide into two identical single mode waveguides. Then two single mode waveguides are bent by 90 degrees with the same bending origin and ultimately merged by another Y junction as output. Inner and outer quarter-rings are carefully designed to yield a 4π phase shift at 1550 nm wavelength. |E| plot top view at

1550 nm wavelength under TE_0 and TE_1 separate input are shown, indicating at TE_0 (TE_1) is bent as TE_0 (TE_1) with low crosstalk at targeted wavelength.

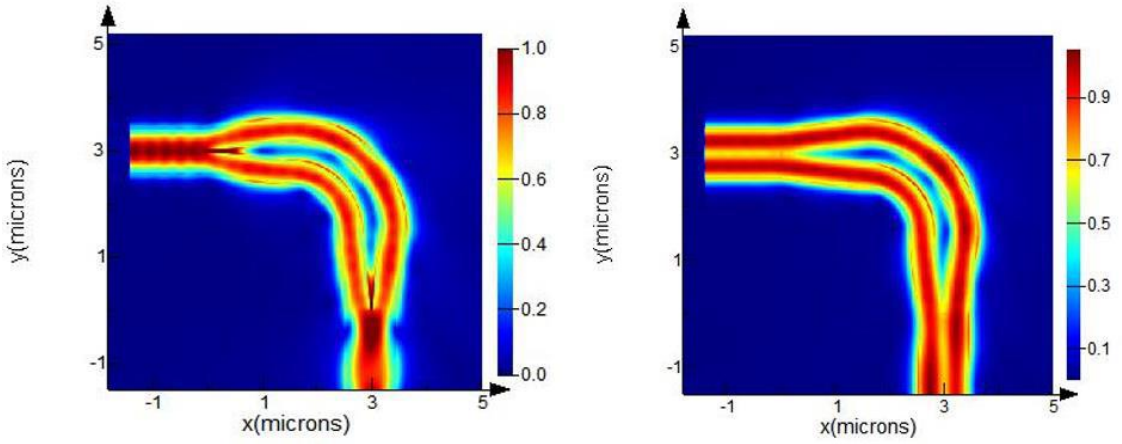


Figure 3.40 (a) |E| top view of 90-degree bend for TE_0 input at 1550 nm wavelength (b) |E| top view of 90-degree bend for TE_1 input at 1550 nm wavelength

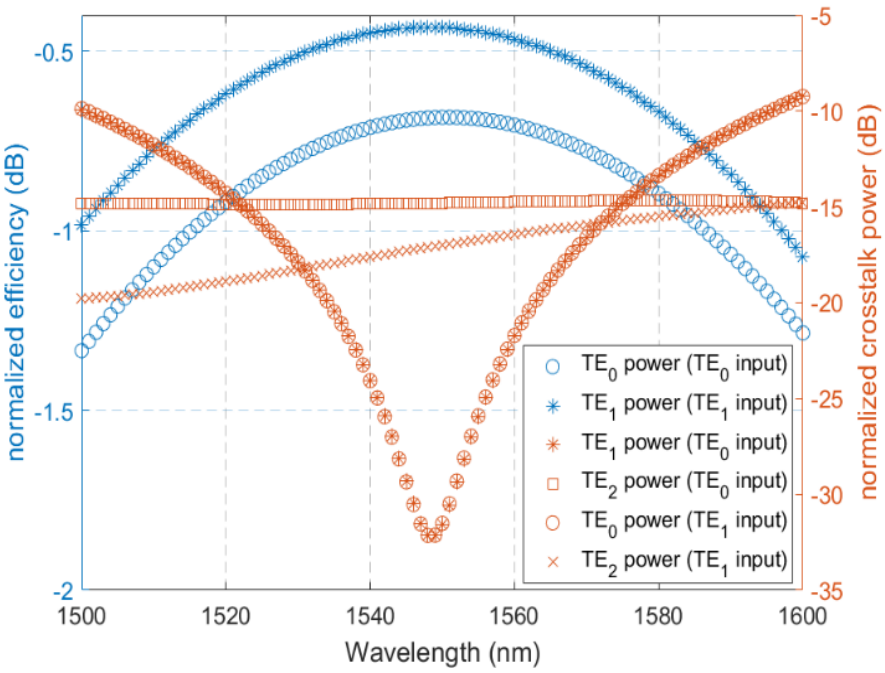


Figure 3.41 Simulated efficiency and crosstalk of 90-degree bend under TE_0 and TE_1 individual input

Fig.3.41 shows the FDTD calculated spectrum of the 3 μm radius 90-dergee bend, which shows 0.8 dB insertion loss and 17 dB crosstalk suppression over 40 nm bandwidth. At central

wavelength the best performance can be obtained, leading to 0.7 dB insertion loss and over 30 dB crosstalk suppression. The ultra-high extinction appears to be narrowband because phase relationship degrades when further away from central wavelength. Due to reciprocity, TE_1 crosstalk excited from TE_0 input is equivalent to TE_0 crosstalk given TE_1 input. There's also around -15 dB TE_2 modal crosstalk, which is not a threat since TE_2 mode can be easily cut off without disturbing better guided TE_0 and TE_1 modes.

TE_0 shows higher insertion loss than TE_1, which is mainly attributed to power loss at two steep Y junctions. If larger bending radius is allowed, longer Y junctions can be used to reduce insertion loss even further. Numerically a larger bend with 5 μm radius (3.5 μm long Y junction) could perform even better. Simulation shows 0.3 dB broadband insertion loss reduction while modal crosstalk spectrum gives similar trend with the best 45 dB crosstalk suppression at a slightly shifted central wavelength.

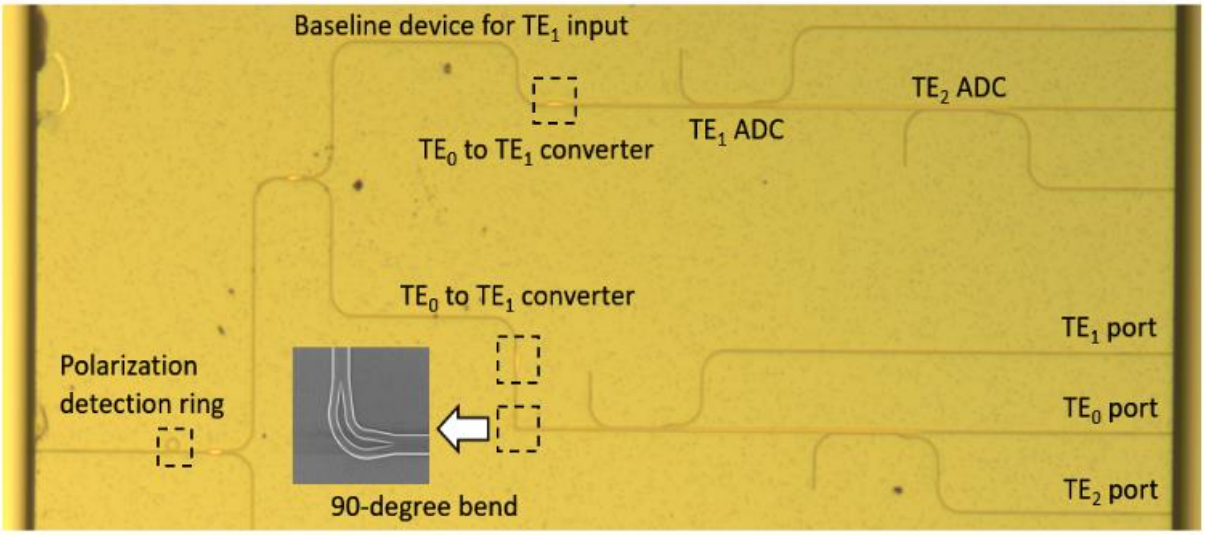


Figure 3.42 Optical microscope image of measurement setup for 90-dgree sharp bend (courtesy of Mr. Yun Jo Lee)

The 3 μm radius sharp bend is experimentally evaluated as shown in Fig.3.42. Lensed fibers are used to couple light into SOI chip using edge couplers. To further reduce coupling loss uncertainty, cascaded 1to2 MMI network is used to share the same input edge coupler, at cost of accumulated reflection from MMI though. Input TE_0 mode will be initially converted to TE_1 using a compact taper shaped mode converter [68]. Then TE_1 mode will propagate with/without sharp bend and ultimately get demultiplexed by asymmetric directional coupler (ADC). After ADC, TE_0, TE_1 and

TE_2 are measured at middle, top and bottom output port respectively in the form of TE_0. Measurement setup for 90-dergee bend with TE_0 input is also very similar to Fig.3.42, expect for absence of mode converter.

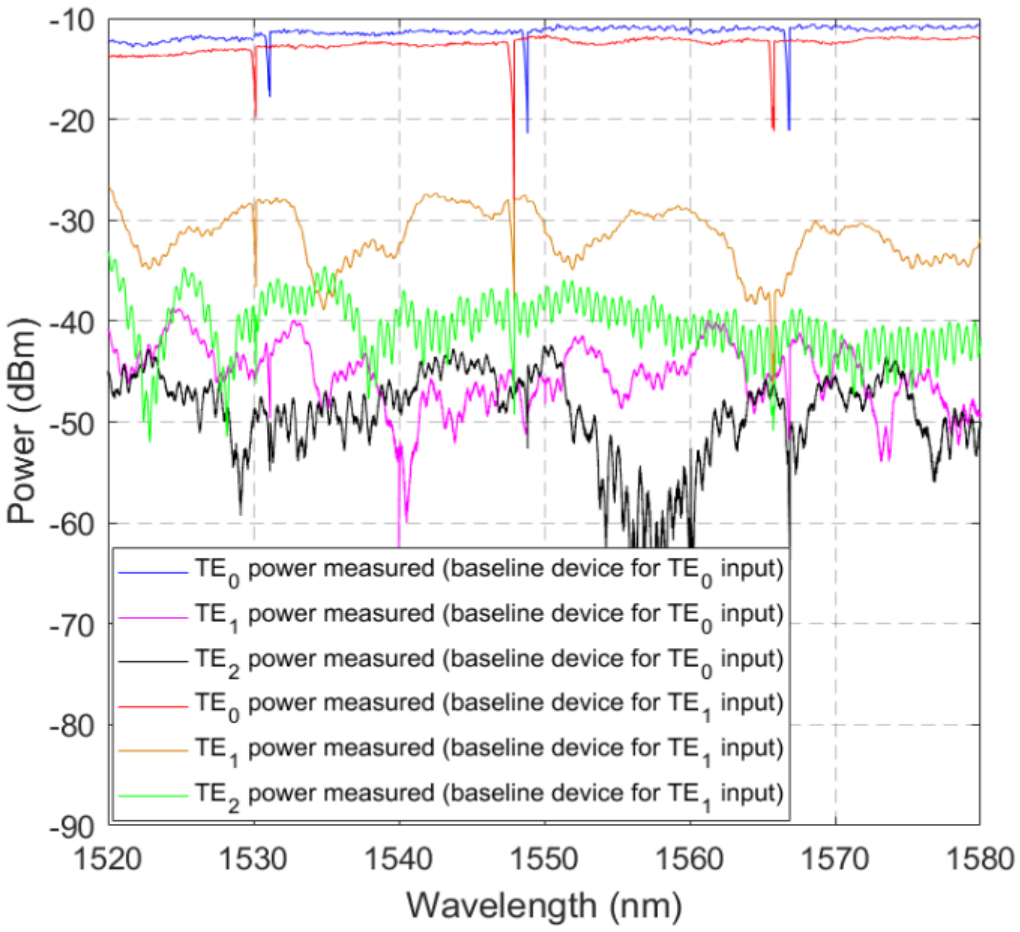


Figure 3.43 Measurement spectrum of baseline devices for TE_0 mode and TE_1 mode input

The measured power spectrums of baseline devices are shown in Fig.3.43. Resonances in measured spectrums are the TE mode resonance at polarization detection (PD) ring. PD ring is deployed on the chip to distinguish TE and TM since edge coupling gives small polarization dependence. PD ring is designed with 5 μm radius and 250 nm gap size to strongly resonant at both polarizations. By adjusting the polarization controller, TE high Q resonance is be maximized (TM low Q resonance minimized) to reach pure TE polarization. Measrument shows significant higher measured TE_0 crosstalk as TE_1 mode generated from mode converter is not very pure. Therefore, to measure the modal crosstalk of a sharp bend under TE_1 input is not going to be

accurate. Due to reciprocity, however, TE_0 crosstalk from TE_1 is equivalent to TE_1 crosstalk from TE_0 input, which is numerically demonstrated in Fig.3.41. As a result, modal crosstalk of a 90-degree bend is only evaluated under fundamental mode input as shown in Fig.3.44.

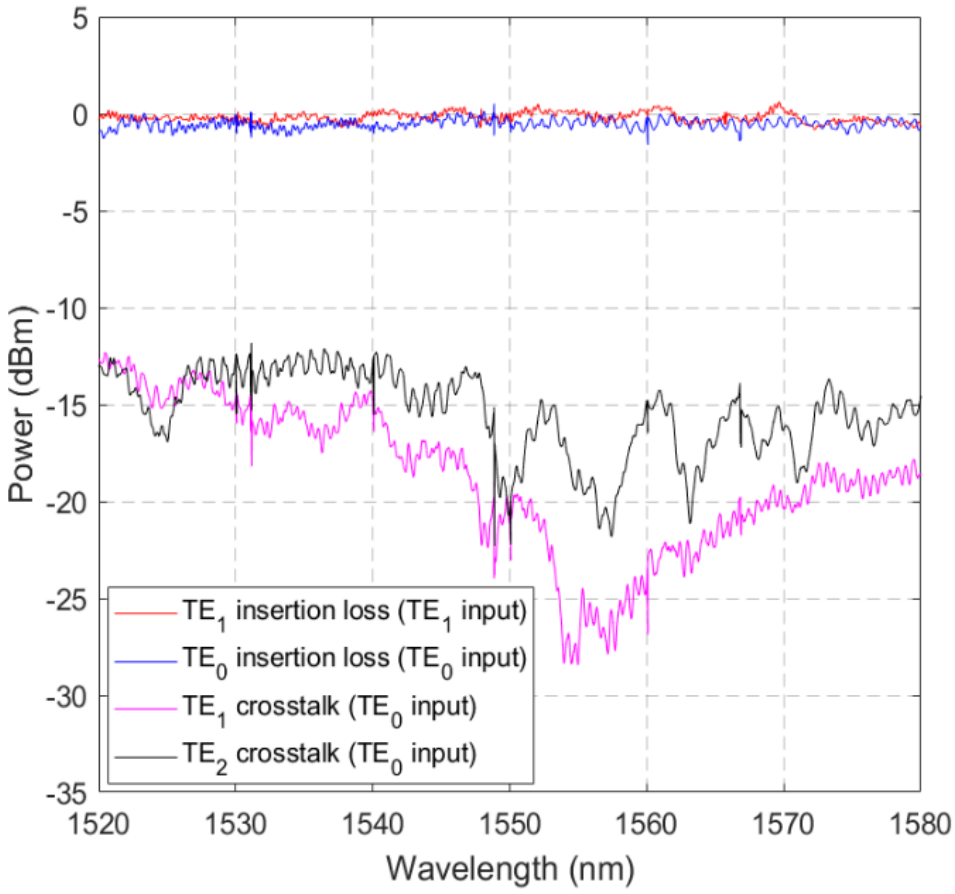


Figure 3.44 Measurement and simulation spectrum of TE_0 and TE_1 insertion loss and modal crosstalk for a 90-degree bend

Measurement spectrums for the 90-dergee sharp bend are given in Fig.3.44, with power normalized to 0 dBm. For better visualization, resonance spikes are removed by data post-processing. Less than 0.8 dB TE_1 insertion loss and 1.2 dB TE_0 insertion loss are measured over 60 nm bandwidth, agreeing with FDTD simulations. Minimum TE_1 crosstalk of -27 dB is measured at 1555 nm, which is slightly shifted from designed 1550 nm. This can be explained by fabrication deviations that Y junction with 5 nm width offset can introduce such spectral shift. Overall ultra-low crosstalk (less than -20 dB) over 20 nm bandwidth is experimentally

demonstrated, which is sufficient for single-wavelength on-chip MDM systems. TE_2 crosstalk around -15 dB is measured via TE_2 ADC port, which is also consistent with FDTD simulations.

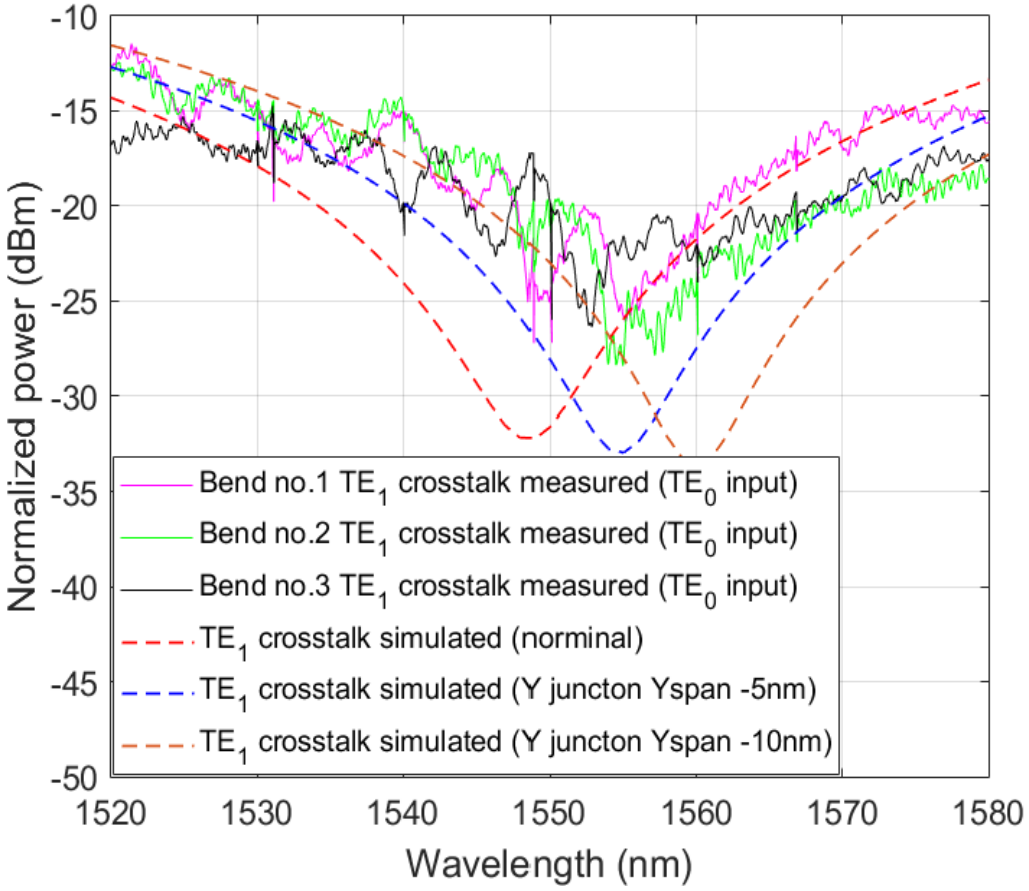


Figure 3.45 Measurement and simulation spectrum of modal crosstalk for three identical 90-degree bends

To validate the reproducibility of the sharp bend device, identical bends are fabricated on the same chip for reliability testing. Fig.3.45 gives measured TE_1 crosstalk spectrums of three identical bends. Measurement shows relatively consistent trends of crosstalk with small differences caused by fabrication deviations. Similarly, TE_0 insertion loss is also measured over three identical bends to see if low insertion loss is repeatable. Fig.3.45 gives the measurement and simulation spectrums showing reasonably consistent low insertion loss results.

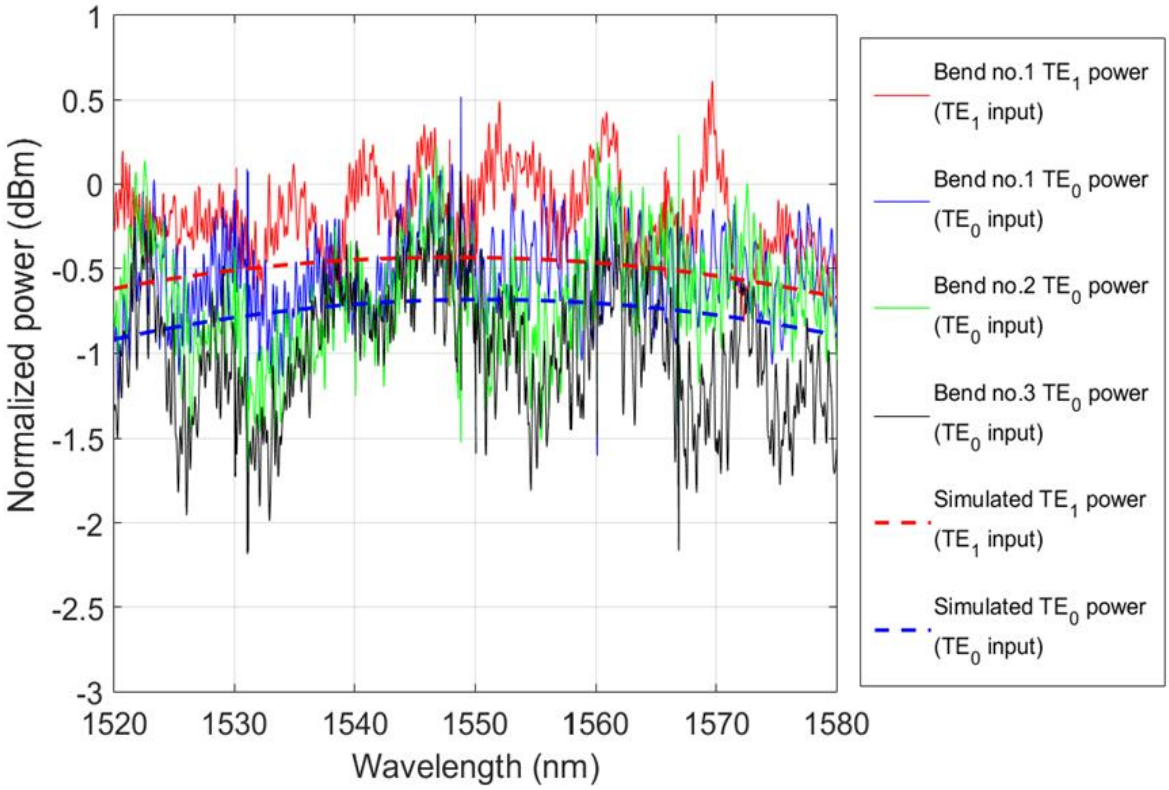


Figure 3.46 Measurement and simulation spectrum of insertion loss for three identical 90-degree bend

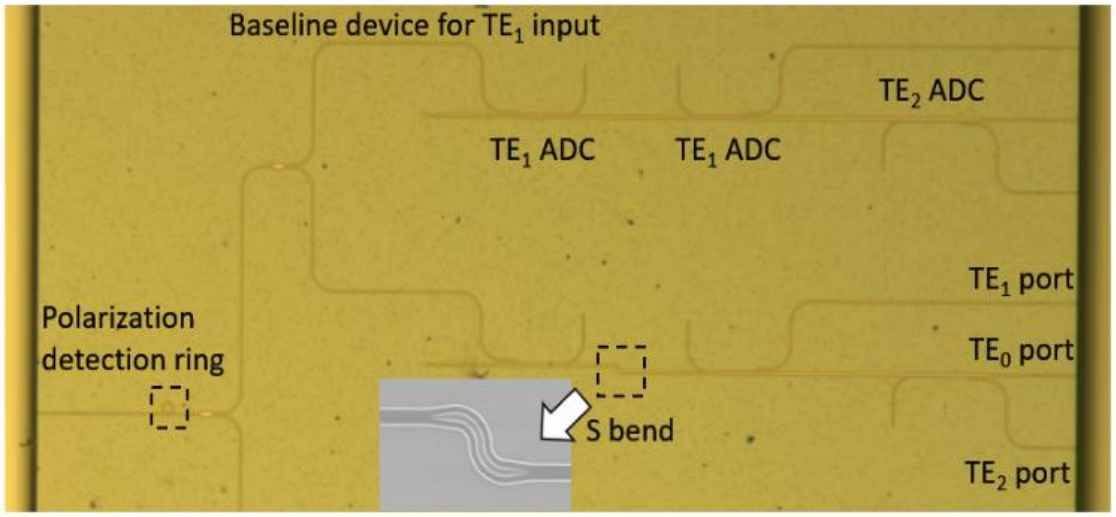


Figure 3.47 Optical microscope image of measurement setup for 90-dgree sharp bend (courtesy of Mr. Yun Jo Lee)

The TE_0/TE_1 multiplexed S bend is experimentally evaluated with back-to-back ADCs to excite and demultiplex high order modes as shown in Fig.3.47. Similar setup without input ADC is used

to evaluate TE_0 insertion loss, though modal crosstalk is not evaluated using mode demultiplexer. Measured spectrums are shown in Fig.3.48 where < 1.5 dB insertion loss and flatband 19 dB crosstalk suppression are measured. The TE0 crosstalk power measured from TE1 input is almost overlapped with crosstalk of baseline device caused by back-to-back ADC, indicating even less than -18 dB modal crosstalk might exist.

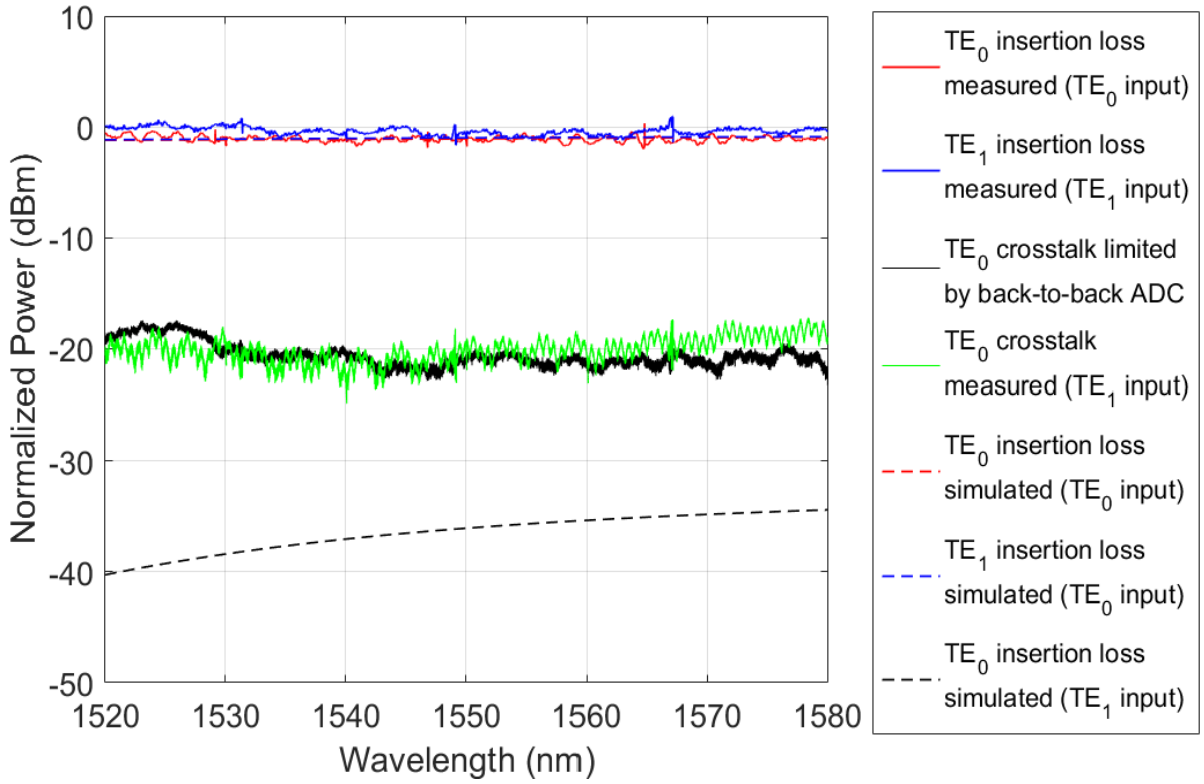


Figure 3.48 Simulated and measured spectrum for S bend

Eventually performance of our device is compared with all previous CMOS-compatible sharp bend solutions. With 3 μm bending radius, 1.2 dB insertion loss and -20 dB modal crosstalk are experimentally demonstrated over 20 nm bandwidth. Although inverse design bend (air cladding) shows better performance under comparable bend radius, with SiO_2 top cladding inverse design typically takes larger footprint hence such sharp bending might not be achievable. Our bending scheme based on Y junction in this letter indeed offers decent fabrication tolerance and design flexibility. In addition, the sharp S bend proposed in this letter provides colorless low insertion loss and strong crosstalk suppression, which can be a much better solution than cascading multiple previously reported 90-degree bends.

Table 5 Comparison with previously reported MDM sharp bends

State-of-art works for comparison	Bend radius	Insertion loss	Modal crosstalk
Bend with mode converter [76]	10 μm	0.2 dB	-22 dB
Inverse design (air cladding) [77]	3.6 μm	0.8 dB	-24 dB
Y junction 90-degree bend (this work) [78]	3 μm	1.2 dB	< -20 dB over 20 nm bandwidth
Y junction S bend (this work) [78]	3 μm each	1.5 dB	< -19 dB over 60 nm bandwidth

MDM bend under dual mode concurrent input is also investigated, which is failed to be covered by previous report. For conventional on-off-keying (OOK), dual mode input will cause problem when both channel is "on" and optical field of dual modes will interfere along the bending structure. Due to interference some portion of TE_0 can be converted TE_1 (or vice versa) hence potentially one mode is more lossy while the other mode can have gain. Numerically the previously reported 10 μm radius bend based on mode converter [76] can result in as much as 20% additional loss for one mode and 20% gain for the other one ($\pm\mathbf{20}$% phase dependent spectral fluctuation).

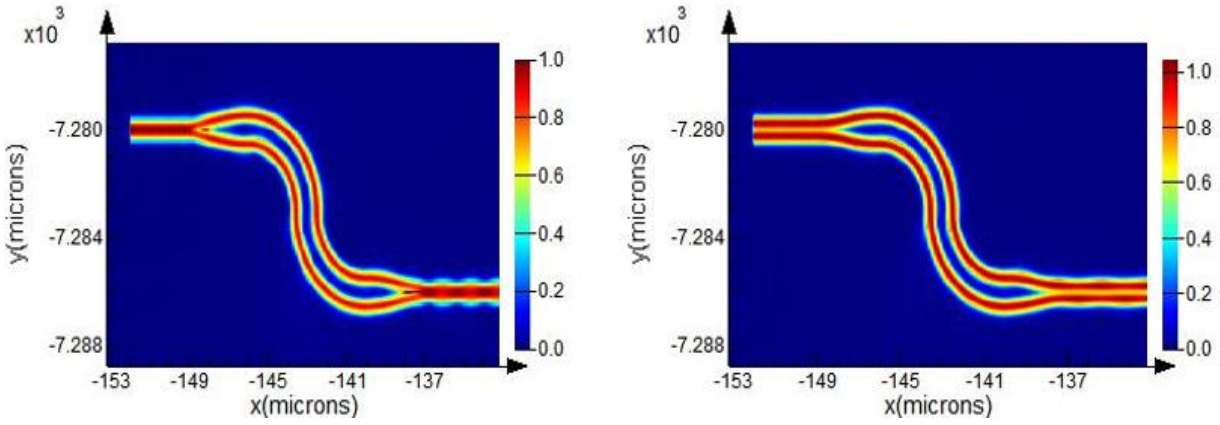


Figure 3.49 FDTD |E| top view of S bend under TE_0 and TE_1 mode input respectively

The bend proposed in this section is claimed to solve this problem by using reciprocity. Optical reciprocity dictates that input TE_0/TE_1 beating pattern will be reproduced by back-to-back Y junctions. MDM S bend can easily mimic such structure since identical pathlength and routes are used on two arms hence S bend should offer phase insensitive performance. Here a larger S bend (5 μm radius each) is simulated under both single and dual modes input. Fig.3.50 shows for various relative phase shift, the same dual mode beating pattern can be reproduced after S bend just like a back-to-back Y junction does. The simulated spectrum shows < 1.5% deviation from single mode input over 100 nm bandwidth, which is almost negligible.

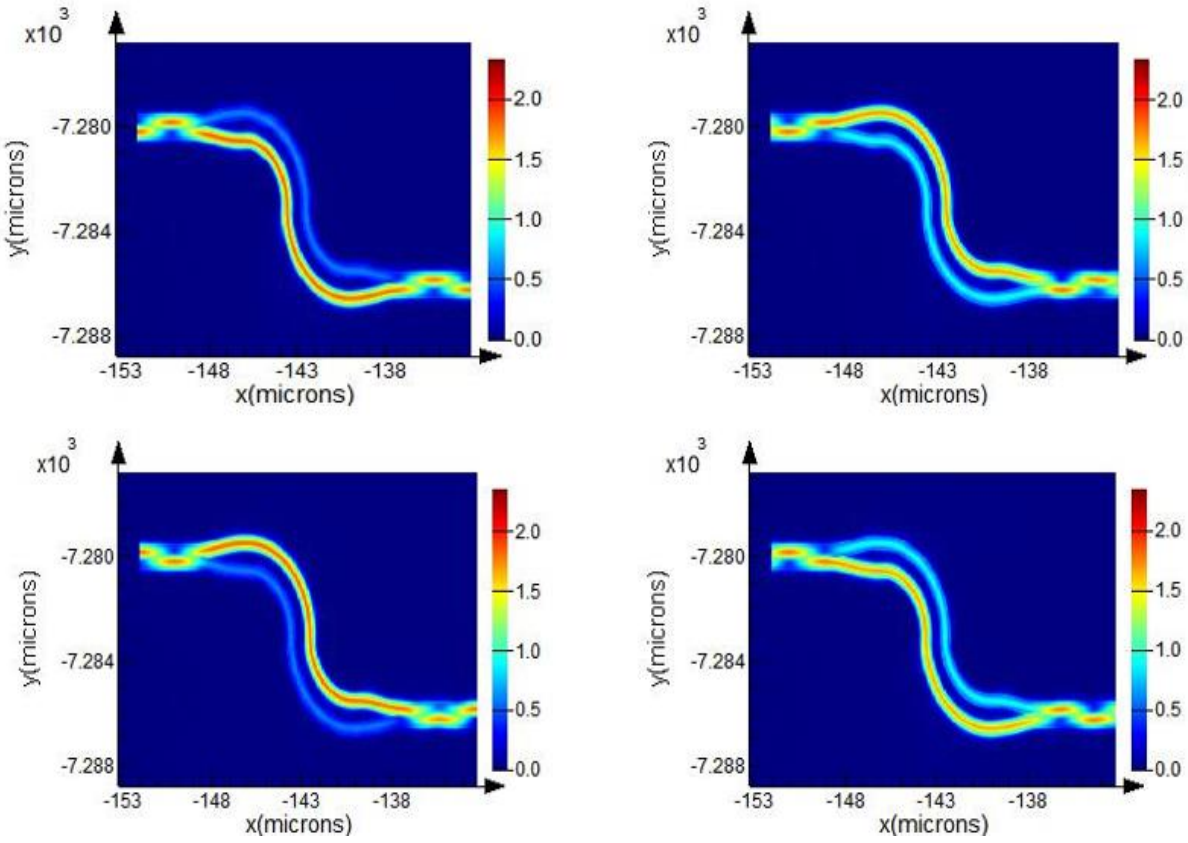


Figure 3.50 FDTD |E| top view of S bend under dual mode beating input of -90-degree, 0-degree, 90-degree, and 180-degree relative phase shifts respectively

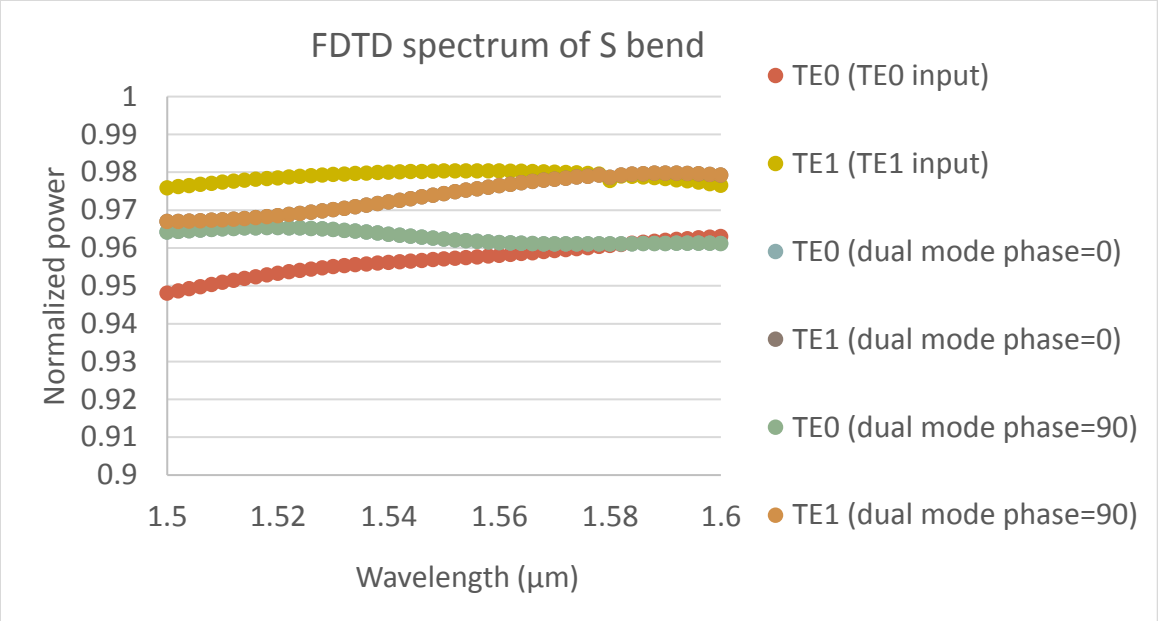


Figure 3.51 FDTD spectrum of dual mode input

For a 90-dgeree bend with different inner and outer arms, the performance usually depends on relative phase between dual modes. For instance, at certain phase all power travels through inner arm (higher bending loss) whereas at some other phase when all power travel through outer arms (lower bending loss). To truly mimic a back-to-back Y junction, the design will become more complicated, which cannot be contained inside 3 μm radius. Here a larger bend with 10.5 μm radius is proposed to balance pathlength and insertion loss of two routes, leading to almost phase insensitive performance under dual mode input.

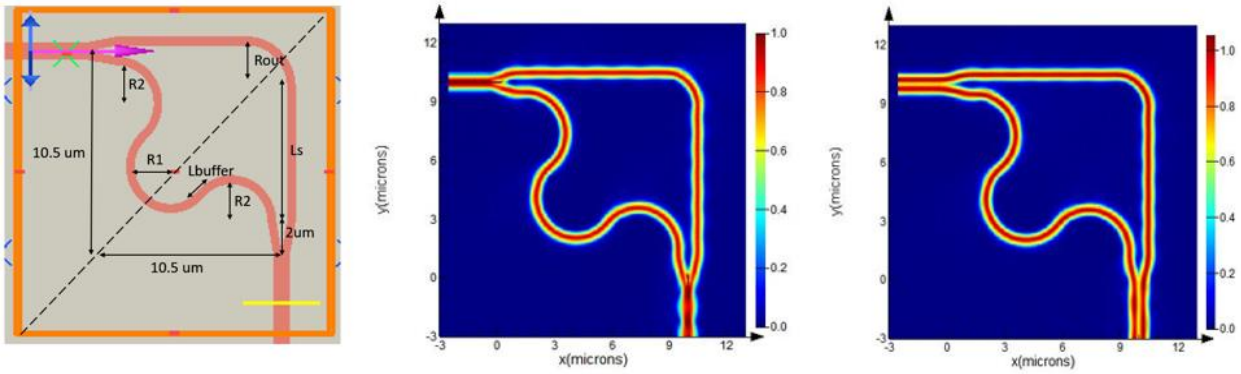


Figure 3.52 (a) Schematic of 10.5 μm radius bend with balanced pathlength and loss between two routes (b) |E| plot under TE0 input (c) |E| plot under TE_1 input

Fig.3.52 (a) shows the bend structure under investigation, where Lbuffer and Ls (hence Rout) value can be adjusted to tweak path length and propagation loss. The bend geometry is optimized such that under TE_0 (or TE_1) mode input modal crosstalk is minimized. This strategy is based on the fact that at output Y junction, only in-phase modes with 1:1 power can add up perfectly without exciting the wrong mode. Simulation gives less than -35 dB modal crosstalk over 100 nm bandwidth which indicates balance pathlength and loss is found. With more rigorous geometry optimization, even lower modal crosstalk is technically possible.

The entire bend geometry is simulated under dual mode concurrent injection as shown in Fig.3.53. Simulation shows only less than 2% power deviation over 100 nm bandwidth from single mode input. This is a significant improvement compared with previous reported bends. The experimentally validate the phase insensitive performance, the preliminary layout is shown in Fig.3.54. The input TE_0 mode is divided equally into two pieces and one of them is passed to ADC to couple TE_1 power into the other waveguide. Before multiplexing one to vertical bus waveguide, hardwire phase shift can be included to introduce arbitrary relative phase shift between two modal channels. A new fabrication run is expected to take place soon based on such GDS layout for experimental validation.

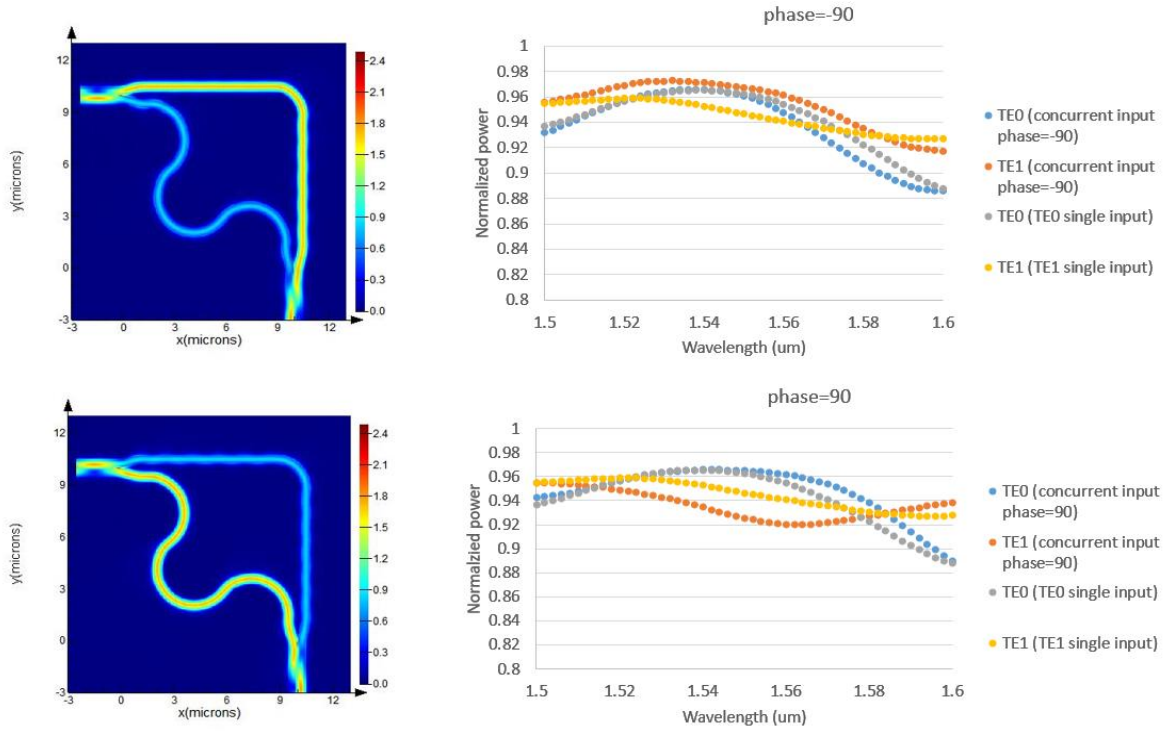


Figure 3.53 Field pattern and spectrum under dual mode input with ± 90-degree relative phase shift

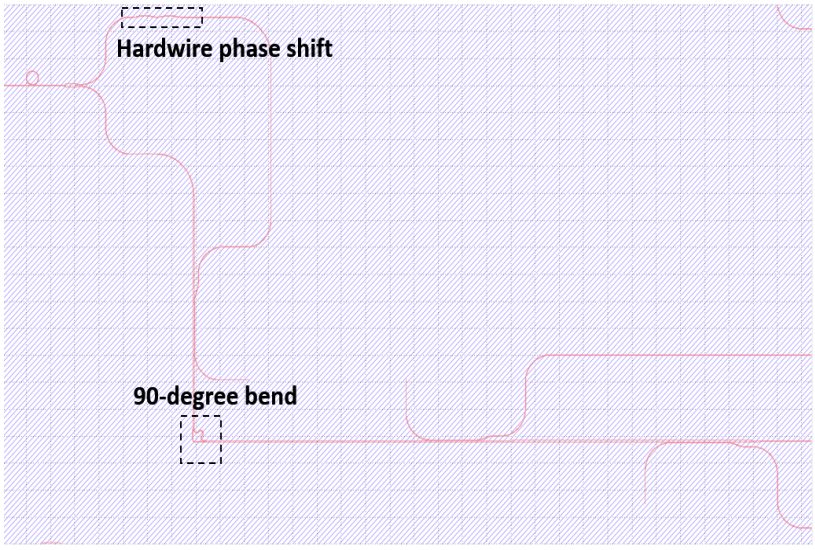


Figure 3.54 GDS layout for 90-degree bend under dual mode input with adjustable relative phase shift

3.6 Spot size converter for two-mode-division multiplexing

Over the past decade on-chip mode division multiplexing (MDM) has been heavily investigated but the difficulty to couple high order mode signals out of photonic chips [79] has severely hindered its commercial applications. Many previously reported works [80][81][82] proposed to use multi-mode fibers (MMFs) for inter-chip MDM interconnect. However there has been no experimental support that multiplexed modes can travel long distance once being coupled into MMFs. The fundamental challenge is linearly polarized modes in fibers are superpositions of several vectorial modes, inevitably getting dephased along propagation [83]. For this reason, using MMFs to build inter-chip MDM interconnect is unlikely to succeed.

Here we propose to use few-mode polymer waveguides instead of MMFs for inter-chip interconnect. Previously, J. Kang [84] experimentally demonstrated a polarization selective polymer waveguide with 28 dB polarization extinction ratio and 0.5 dB/cm propagation loss at 1550 nm. This is promising for board-level optical interconnect between chips. To enable MDM optical links, here we present a spot size converter (SSC) that can efficiently couple four (TE_0, TE_1, TM_0, and TM_1) multiplexed signals between SiN chip and polymer waveguide.

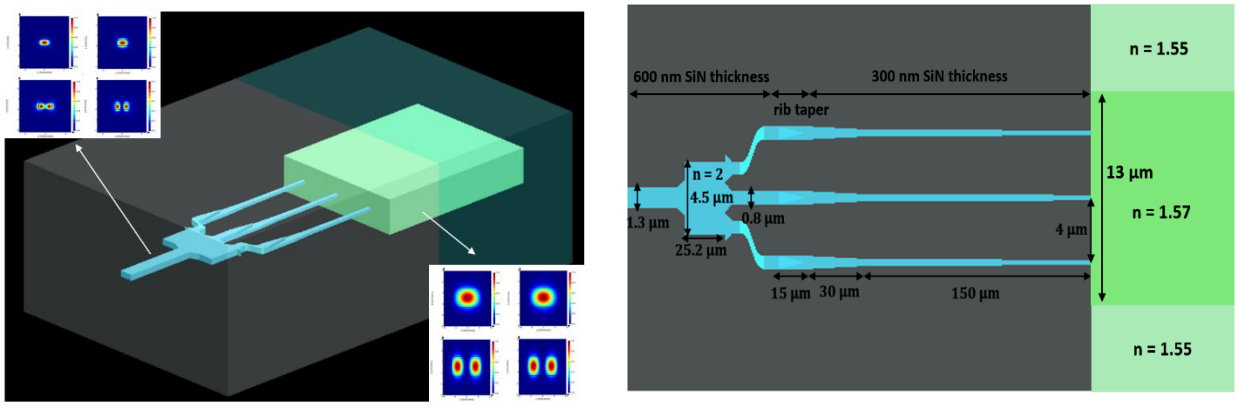


Figure 3.55 (a) Schematic and (b) top view of MDM SSC for butt coupling between SiN chip and few-mode polymer waveguide

Fig.3.55 shows an example configuration that a polymer waveguide is butt-coupled to the SiN chip. The polymer has index contrast of 0.02 [84] and 3.5 µm thickness is chosen to cut off high order modes in vertical directions. The polymer waveguide core is 13 µm wide which supports more than 2 modes in horizontal directions, and higher order modes can be cut off later by adiabatic tapering. Input mode source (TE_0, TE_1, TM_0 or TM_1) is injected from multi-mode SiN waveguide, aiming to couple to the corresponding mode at polymer waveguide. Launched beam first travels through a 600-nm thick nitride MMI that splits fundamental mode and the first high order mode. Then with a rib taper, thickness of nitride is reduced to 300 nm for better mode overlap design purposes. Eventually three 300 nm thick single-mode SiN waveguides are tapered out by inverse tapers to achieve spot-size conversion.

600 nm thick MMI mode splitter is intially used to compensate polarization dependence of MMI mode splitter, which is initially proposed by T. Uematsu [61]. MMI mode splitter works such that input fundamental mode will travel through the middle output port while first high order mode will be evenly divided as anti-phase fundamental mode pairs through two outer ports. With a 4.5 µm wide & 25.2 µm long nitride MMI, > 80% broadband efficiency can be obtained for all four modes (TE_0, TE_1, TM_0 and TM_1).

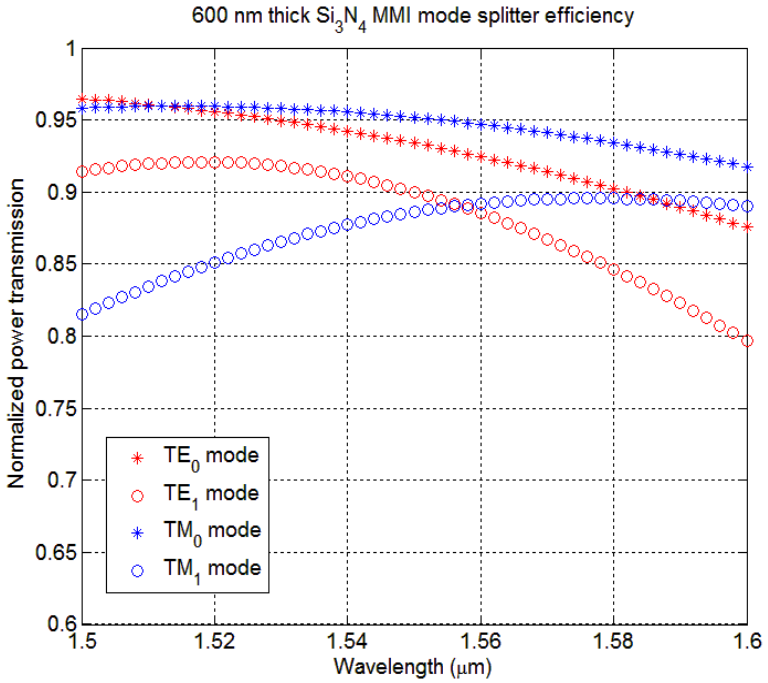


Figure 3.56 3D FDTD calculated efficiency of MMI mode splitter

Edge couplers (inverse tapers) are designed at 300 nm thick SiN waveguide to better match mode overlap at both polarizations. 330 nm central tip width and 280 nm outer tip width are chosen, with 4 μm adjacent tips center-to-center spacing. Fig.3.57 shows the mode profiles support by triple tips, targeted respectively for coupling with fundamental and high order modes. To bridge different SiN thickness, 15 μm long rib tapers (rib width linearly tapers from 800 nm to 100 nm) are used to trim down nitride thickness to 300 nm. After rib tapers, three 300 nm thick nitride waveguides are tapered out by two stages. Widths of three parallel waveguides are linearly tapered down to 500 nm in 30 μm length first, then followed by 150 μm long linear tapers towards the edge.

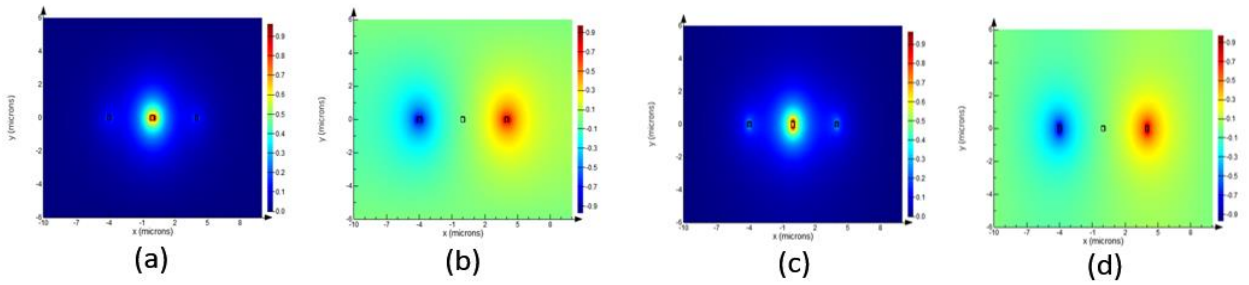


Figure 3.57 (a) Ex for TE_0 (b) Ex for TE_1 (c) Ey for TM_0 (d) Ey for TM_1

Device is numerically evaluated with 3D FDTD assuming polymer waveguide is perfectly aligned with central nitride tip. Fig.3.58 shows the simulated transmission power spectrums for four different mode excitations. From simulations, < 2 dB loss over 100 nm bandwidth and < 1.5 dB over C band (1530 nm – 1565 nm) can be obtained for all four modes. Spectrum also shows < -55 dB crosstalk power and ultralow crosstalk is attributed to the horizontal symmetry of the structure which prohibits mode conversion between fundamental and first order modes. Fig.3.59 shows the normalized electric fields (|E|) with four different input modes separately, indicating correct modes with much larger sport size are excited at output polymer waveguide.

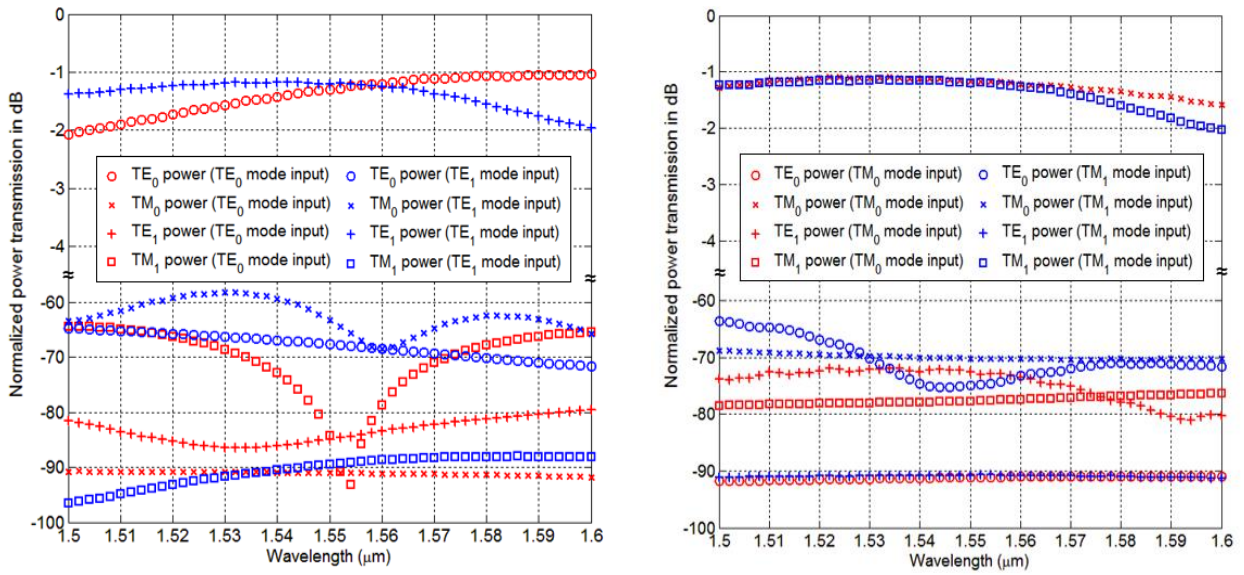


Figure 3.58 3D FDTD coupling loss spectrum with (a) TE_0 (red) and TE_1 (blue) inputs and (b) TM_0 (red) and TM_1 (blue) inputs

In this design 4 μm polymer thickness is chosen and this dictates 13 μm width of polymer waveguide, which can support more than two modes in horizontal directions. That means two-mode multiplexed spot size converter can inevitably excite higher order modes during butt coupling. Fortunately, higher modes can be cut-off by adiabatic tapering the polymer waveguide, which is numerically investigated in Fig.3.60.

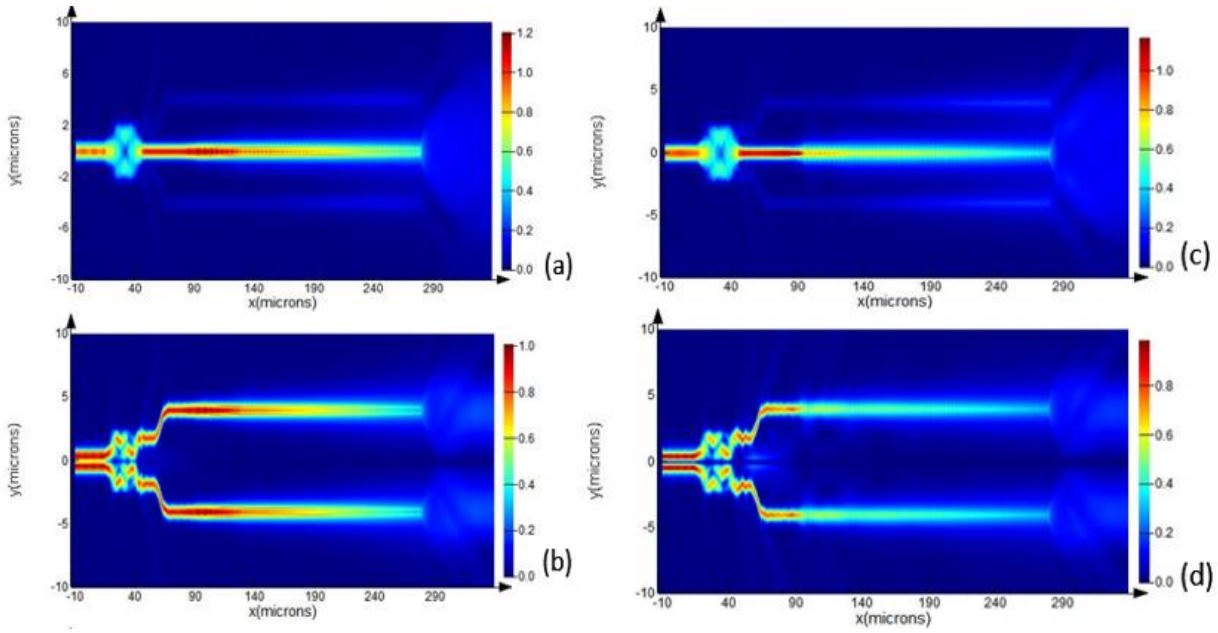


Figure 3.59 |E| top view of (a) TE_0 input (b) TE_1 input (c) TM_0 input (d) TM_1 input from nitride waveguide

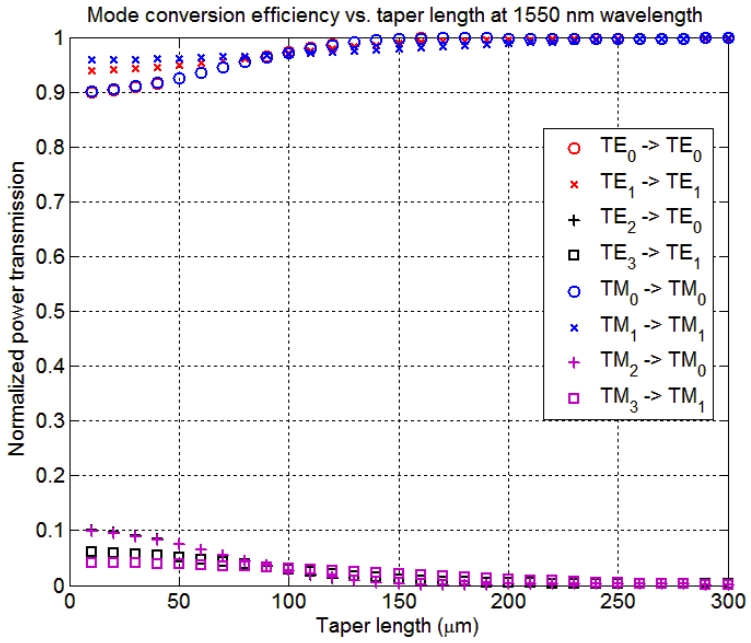


Figure 3.60 EME calculated mode conversion efficiency for various modes at 1550 nm wavelength

Here 13 μm wide polymer core is linearly tapered down to 7 μm to support only two modes horizontally at each polarization. With Eigen-mode Expansion (EME) method, coupling efficiency

of various modes are scanned at 1550 nm wavelength. Theoretically with a too short taper, TE_2 can be couple into TE_0 while TE_3 can also be squeezed into TE_1 due to similar modal phases. With scanned taper length, it's found that beyond 200 μm the taper can achieve negligible mode transition loss for fundamental and second order modes while the crosstalk becomes < 1% (-20 dB). Further extending the taper length can help reduce crosstalk even more and EME predicts that at a 300 μm long polymer taper crosstalk around -30 dB can be obtained.

As a summary, we numerically demonstrate a spot size converter that allow the four modes (TE_0, TE_1, TM_0, and TM_1) to simultaneously couple from on-chip SiN waveguide to the corresponding modes at few-mode polymer waveguide. Theoretically < 1.5 dB insertion loss and < -55 dB crosstalk over C band can be obtained for all four modes, which grants considerable tolerance to laser wavelength drift. With 4 times data bandwidth enhancement without requiring multiple laser sources, our design can be particularly useful at inter-chip communications on optical PCB board.

For integrated photonics, SOI is a more important platform compared with silicon nitride and Si/SiN hybrid platform has been an active research topic over recent years. Here our two-mode SSC can be further developed into a MDM interface to bridge between Si and SiN layer. The prototype device is shown in Fig.3.61 where a 1 μm thick nitride layer is on top of Si. In simulations it is assumed device has 2 μm BOX and SiO_2 top cladding. The Si TE_0 mode will transfer to nitride layer at 99% efficiency (calculated by EME) after 70 μm long linear inverse taper. When mode is transferred at nitride layer, a nitride MMI mode splitter with larger footprint is deployed reversely to act as combiner.

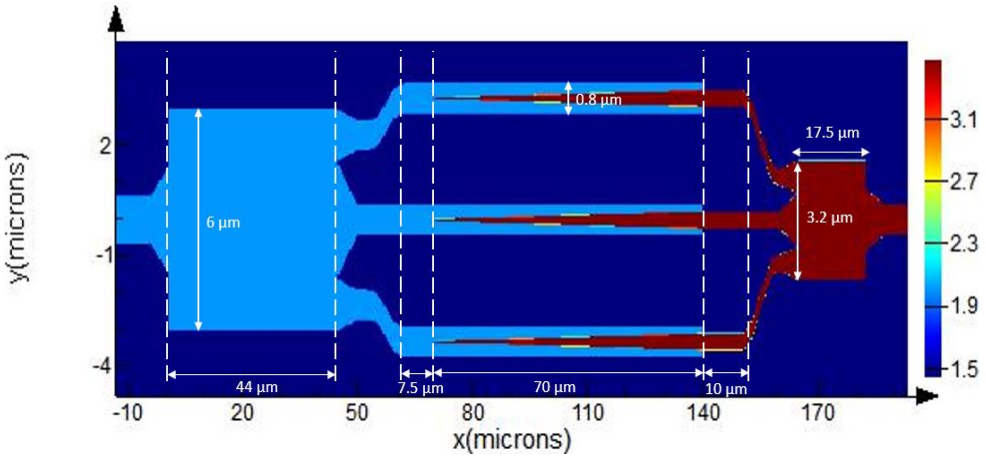


Figure 3.61 Refractive index monitor of the Si/ SiN MDM interface

In FDTD simulation, mode source in injected from Si waveguide and two field monitors record the mode profile at Si and SiN layer separately. In simulation, mode source is set at Si waveguide and beam propagation direction is from right to left. The steady state E field distribution is shown in Fig.3.62. TE_0 mode injection from Si waveguide travels through the central path and get completely transferred to nitride layer after inverse taper. Then TE_0 mode transmits through nitride MMI via the central path and reach the output port as TE_0. As for TE_1 input, tapers at two outer branches take the power from Si and couple into nitride MMI as two anti-phase TE_0 and ultimately becomes TE_1 at output port.

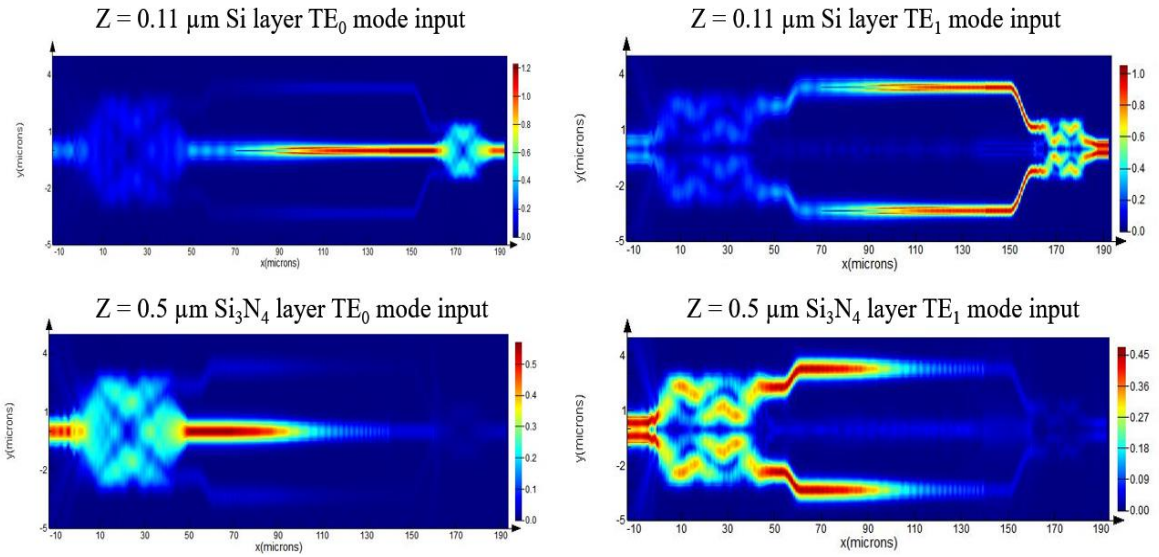


Figure 3.62 |E| cut view at Si and Si_3N_4 (or SiN) layer

The calculated spectrum is shown is Fig.3.63 and Fig.3.64, where less than 1 dB insertion loss is obtained while < -90 dB channel crosstalk appears over 100 nm bandwidth. The ultralow crosstalk is caused by the symmetry of our design. In the horizontally symmetry structure TE_1 and TE_0 cannot convert to each other due to π phase shift. Even if TE_0 mode after Si layer couple some power to two outer branches, such TE_0 modes are in phase and can only contribute to TE_0 output instead of TE_1. Therefore, the MMI splitter back-to-back configuration can theoretically become a broadband low loss low crosstalk MDM interface between Si and S_3iN_4. Horizontal misalignment between Si and nitride layer has also been investigated, and in FDTD simulation of 50 nm (typically ~ 30 nm) is introduced. Simulation shows less than 1.4 dB insertion loss while crosstalk below -40 dB can still be maintained under such horizontal misalignment.

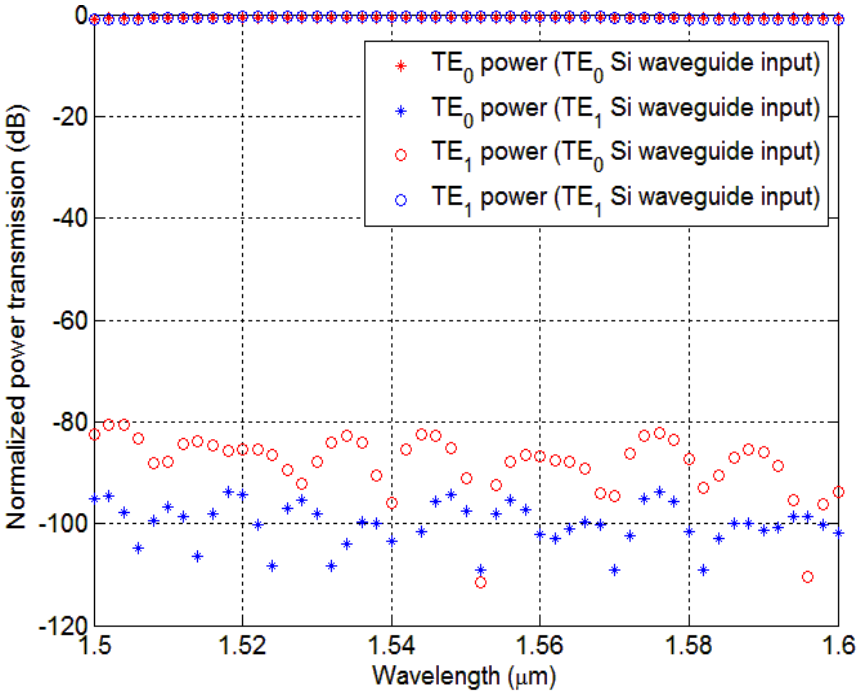


Figure 3.63 3D FDTD spectrum of MDM interface with TE_0 input and TE_1 input at perfect alignment

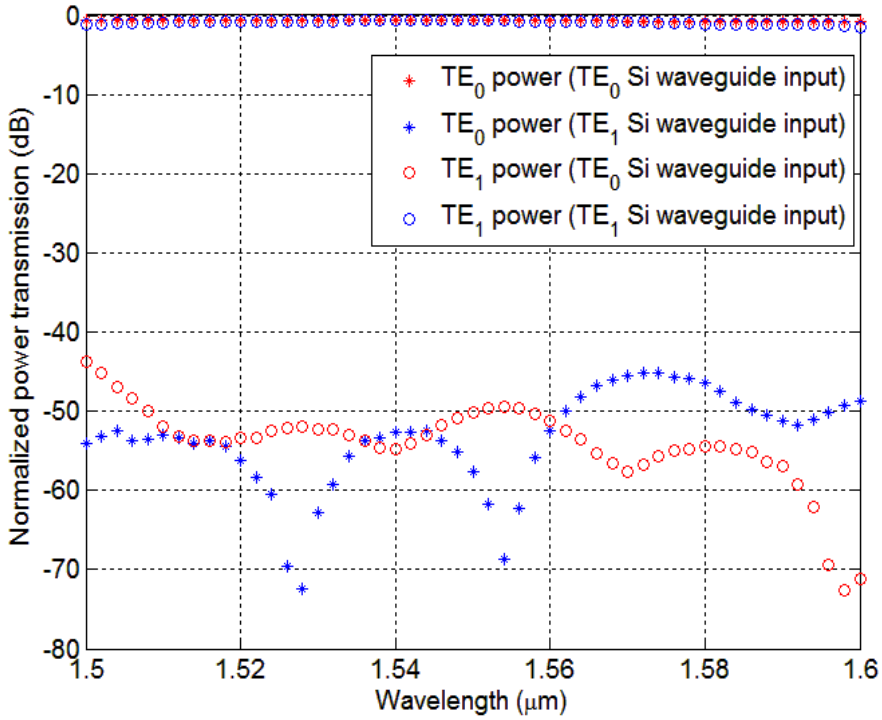


Figure 3.64 3D FDTD spectrum of MDM interface with TE_0 input and TE_1 input under 50 nm horizontal misalignment

3.7 SOI mode order converter based on topology optimization

Another important component for on-chip MDM is mode order converter, which serves as channel converter. Several converter designs have already been reported, while most designs convert fundamental mode to arbitrary high order mode. For more versatile applications, arbitrary mode order converter with compact footprint is needed.

Design based on adiabatic taper is reported as shown in figure below, where particle swarm algorithm calculates vertices of taper. Fundamental mode to high order mode conversion is demonstrated on a 20 μm long taper while two tapers are needed for arbitrary high order mode conversion with fundamental mode as steppingstone.

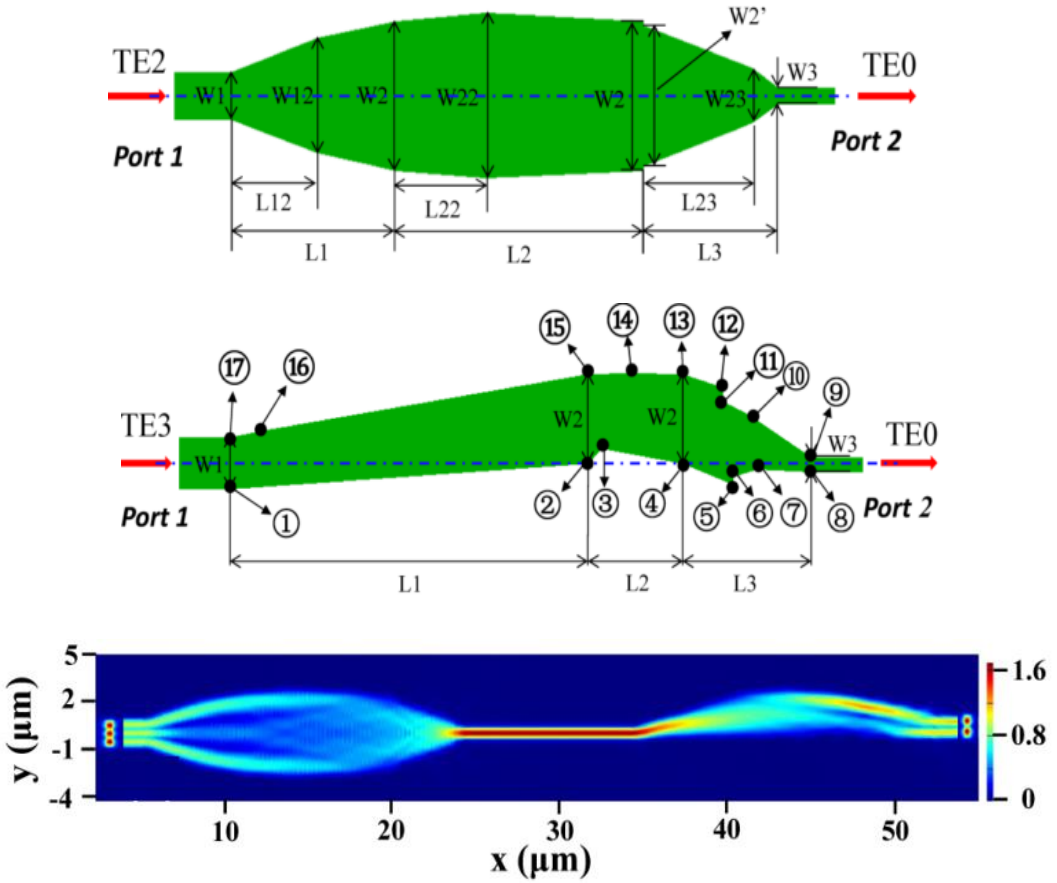


Figure 3.65 Previously reported mode order converter based on adiabatic taper [68]

There is also a mode order converted based on nano-trenches [85] reported in 2017. Although such device shows ultra-compact footprint, only TE_0 to TE_1 conversion is experimentally demonstrated and double layer geometry is not quite favorable from fabrication point of view.

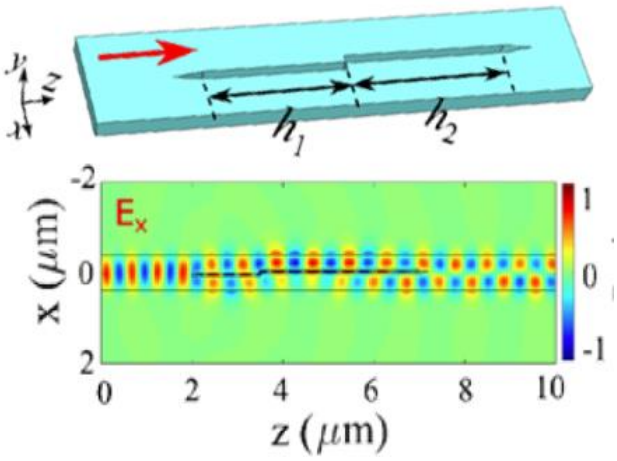


Figure 3.66 TE_0 to TE_1 converter based on cascaded nano-trenches [85]

Alternatively, researchers reported TE_0-to-TE_1 conversion using topology optimized photonic crystal waveguide, offering 70% conversion efficiency over 40 nm bandwidth. However photonic crystal waveguide is not a good broadband solution due to narrow bandgap, hence broadband topology optimized mode order converter can potentially be a good option, which can be much more compact and versatile than using adiabatic taper.

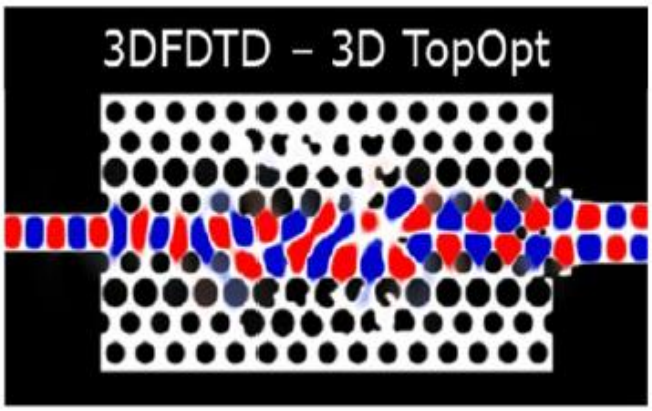


Figure 3.67 Previously reported TE_0-to-TE_1 converter based on topology optimized photonic crystal waveguide [86]

In addition to mode order conversion, photonic inverse design by topology optimization has been widely implemented over several applications, including MDM MUX/DEMUX [67][87], polarization beam splitter (PBS) [88], polarization rotator [89] and MUX/DEMUX for coarse wavelength division multiplexing (CWDM) [90][91]. For broadband operation, the device should be designed like colorless dielectric meta-material by avoiding the Bragg reflection zone [92]. Here a family of ultracompact (~ 4 μm length) mode order converters is proposed, allowing mutual conversion between TE_0, TE_1 and TE_2 over broad bandwidth. Most impressively TE_1-to-TE_2 conversion can be achieved inside single device without using TE_0 as a steppingstone, which indicates such compact devices can be used for arbitrary mode order conversion [93].

This section of works is part of author's intern work at Mitsubishi Electric Research Lab (MERL) at Cambridge MA, which has been reported in OFC 2018 [93]. After the intern, MERL continue working on the projects with Purdue to jointly investigate the inverse design.

Unlikely conventional design where the geometry is predicted from physics analysis, inversed design treats the geometry as a blackbox and to use thousand times of optimizations to find a geometry that serves certain functionalities. For example, a rectangular Si region is discretized into binary pixels like a chessboard where each pixel can be either "0" (doing nothing) or "1" (drill a hole). The hole is drilled with 50 nm radius and 150 nm lattice constants (pitch) such that Bragg reflection zone is avoided as shown in following equation, where neff is the highest effective index of Si waveguide mode (~3).

$$\frac{1550\ nm}{pitch} \gg 2 \times neff$$

To solve the binary optimization problem, direct binary search (DBS) is used while MERL's team also proposed to utilize neural network (NN) approach to accelerated 3D FDTD based DBS process [94]. The NN accelerated DBS algorithm is illustrated by the figure below with a problem size of 200 as an example. Conventionally DBS requires each time when one hole is flipped, one 3D FDTD is needed. NN DBS once large number of training data is available (quickly generated from cluster), NN can directly predict the performance without running FDTD simulations hence flipping the all 200 holes (refresh the entire optimization pattern) can be done almost instantly. After 200 flipping, FDTD simulation is used to validate if NN predicted candidate is indeed better. If the predicated candidate the candidate will overwrite the previous best candidate, otherwise

conventional DBS is used once can DBS training results (regardless performance) is stored into training pull. Figure below shows 3 dB splitter regression plot as an example reported by MERL's team [94], which shows much faster at initial regression when using NN based DBS.

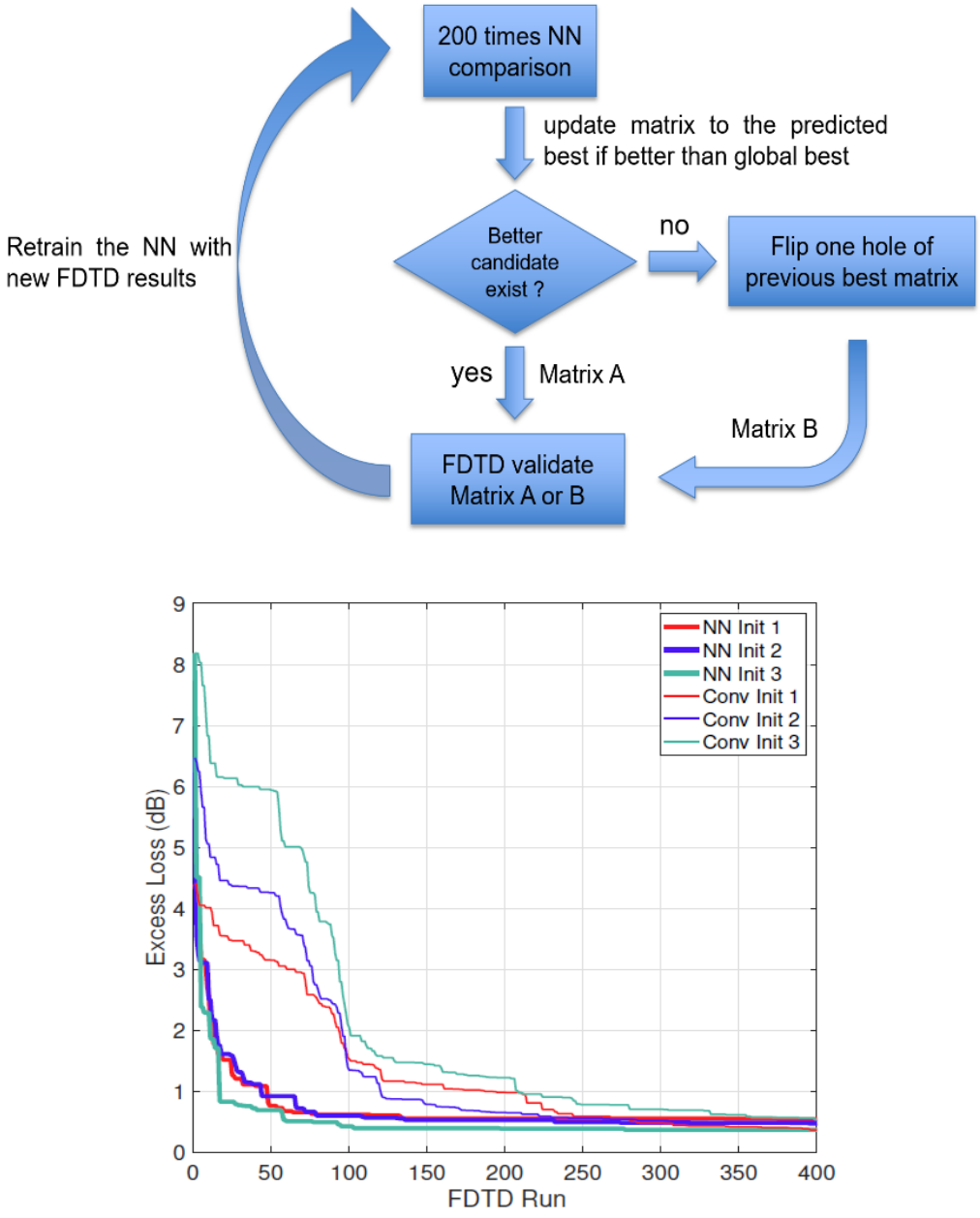


Figure 3.68 (a) Algorithm of neural network accelerated DBS optimization method (b) Convergence comparison between conventional DBS and NN DBS [94]

The topology optimized mode order conversion is also optimized by NN based DBS. The device assumes to have fully etched holes on 220 nm thick SOI wafer then cladded by SiO_2. During optimization, coarse mesh (25 nm) and vertical symmetry boundary condition is used to save FDTD computation time. After optimization the final geometry is simulated under fine mesh (5 nm) and PML on all boundaries to validate the performance.

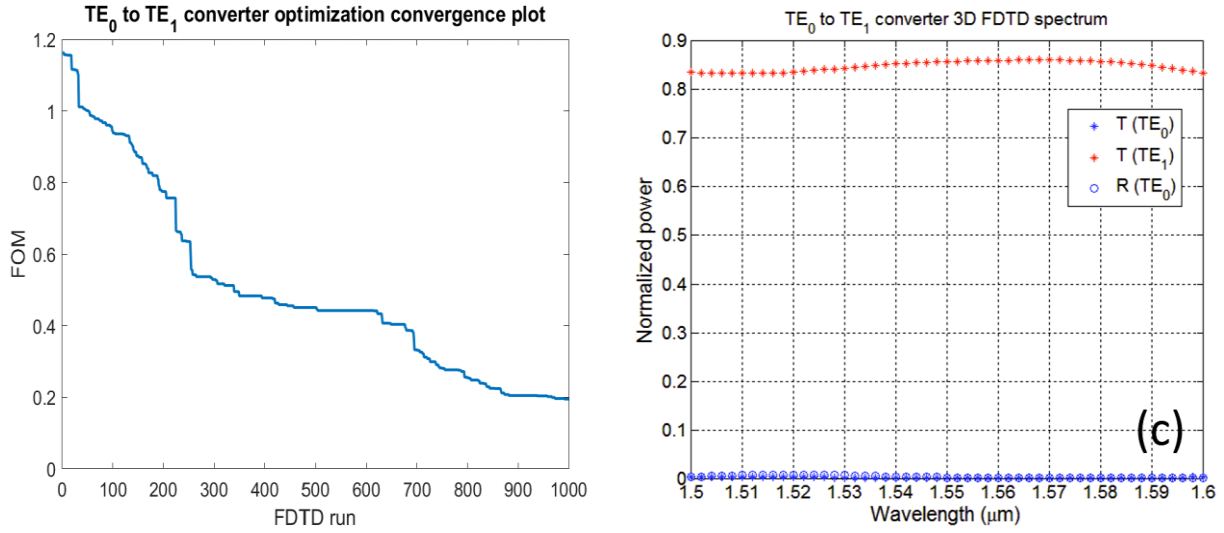


Figure 3.69 (a) Convergence plot of TE_0-to-TE_1 converter optimization using NN DBS (b) 3D FDTD spectrum of finalized TE_0-to-TE_1 converter with high mesh resolution

To start with a TE_0-to-TE_1 converter is optimized on a 3.85 μm × 2.35 μm silicon region, which is discretized into 15 × 25 pixels. Figure of merit (FOM) is defined as TE_1 insertion loss + TE_0 crosstalk + reflection and we attempt to decrease FOM during optimization. Lumerical 3D FDTD is used to calculate 11 spectral points from 1.5 μm to 1.6 μm, and the worst spectral value of FOM (worst case scenario) is being tracked and optimized to reduce wavelength dependence. Fig.3.69 shows the convergence plot using NN based DBS up to 1000 FDTD runs, and the geometry optimization is continued with DBS for additional several hundred runs for finer optimization.

Fig 3.70 shows the finalized geometry after optimization and the major E field component (Ey) distribution plot is also shown. From the field distribution, the input beam is split and then merged at the output with the top beam delayed by π phase shift relative to bottom beam. Distributed holes increase the phase velocity of the beam compared with Si region without holes since the average

refractive index is reduced. FDTD spectrum shows ~ 85% efficiency with ~ 0.5% crosstalk and reflection obtained over 100 nm bandwidth. The efficiency of the converter can potentially be improved by using a larger matrix, although larger footprint and higher computational effort will be required. Compared with the reported TE_0-to-TE_1 converter based on photonic crystal, the proposed converter works over a substantially broader bandwidth since the device avoids the Bragg reflection zone.

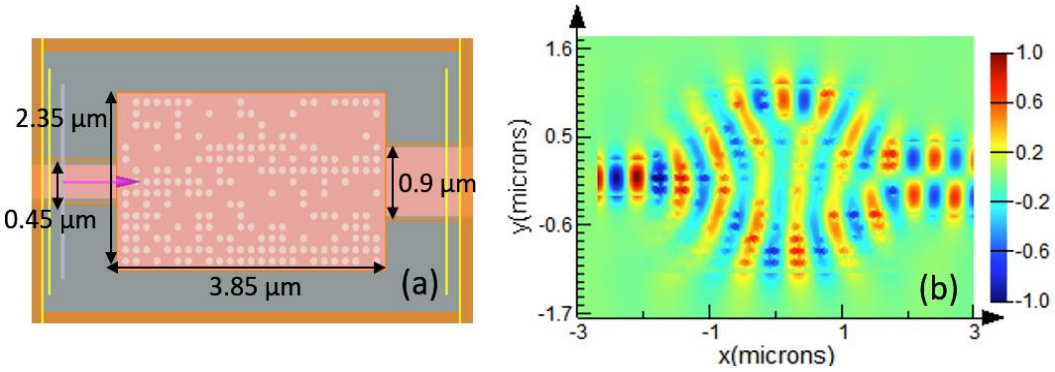


Figure 3.70 (a) finalized geometry of TE_0-to-TE_1 converter (b) |E| top view of TE_0-to-TE_1 conversion

A TE_0-to-TE_2 converter is also designed with a similar procedure. In this case, the two outer lobes of TE_2 should be delayed equally and merged with the center lobe. Therefore, a horizontally symmetric structure (20 × 30) is being evaluated on a 4.6 µm × 3.1 µm rectangular silicon region. During inverse design, a 10 × 30 matrix (top half of the geometry) is optimized and mirrored to the bottom half of the Si region. Fig.3.71 shows the finalized geometry after optimization. Field plot shows most majority of input TE_0 splits equally into two outer routes and some fraction of TE_0 is diffracted and refocused at the output waveguide along the middle route. FDTD spectrum of finalized device shows over 85% efficiency with less than 1% crosstalk and reflection. TE_1 crosstalk power is almost negligible here because TE_0 input cannot excite TE_1 along a horizontally symmetric structure.

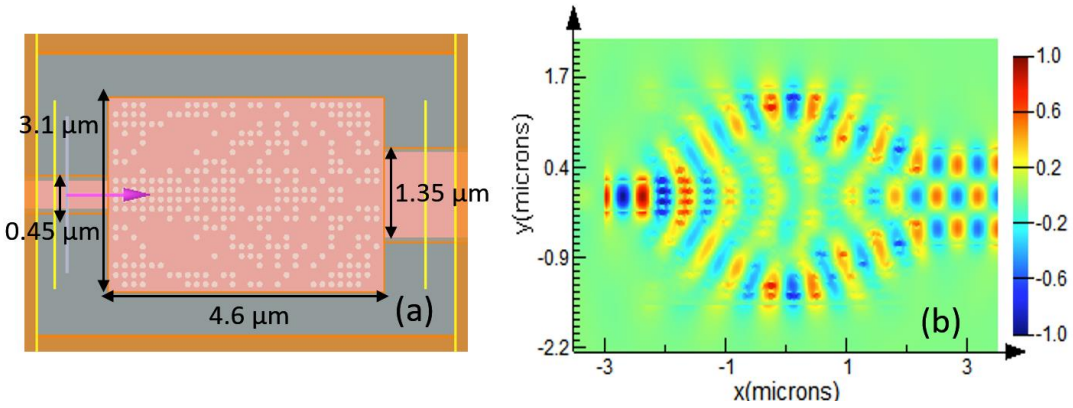


Figure 3.71 (a) finalized geometry of TE_0-to-TE_2 converter (b) |E| top view of TE_0-to-TE_2 conversion

A TE_1-to-TE_2 converter is also demonstrated (see Fig.3.72) in the same manner as the TE_0-to-TE_1 converter. The optimized device can obtain roughly 87% efficiency with crosstalk/reflection into TE_0 and TE_1 both below 1%. The direct conversion between TE_1 and TE_2 does not demand conversion via TE_0 as a stepping stone. Unlike using a 60 µm-long cascaded TE_0 to high order mode converter based on an adiabatic taper [1], our direct TE_1-to-TE_2 converter can achieve 87% efficiency with device length less than 4 µm.

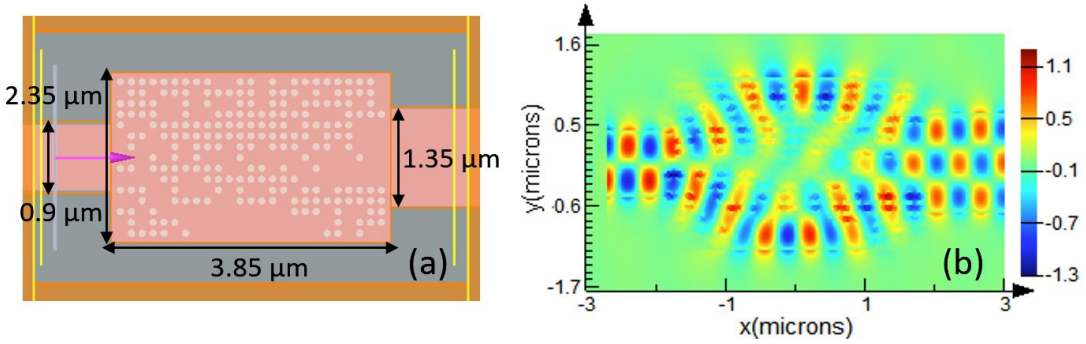


Figure 3.72 (a) finalized geometry of TE_1-to-TE_2 converter (b) |E| top view of TE_1-to-TE_2 conversion

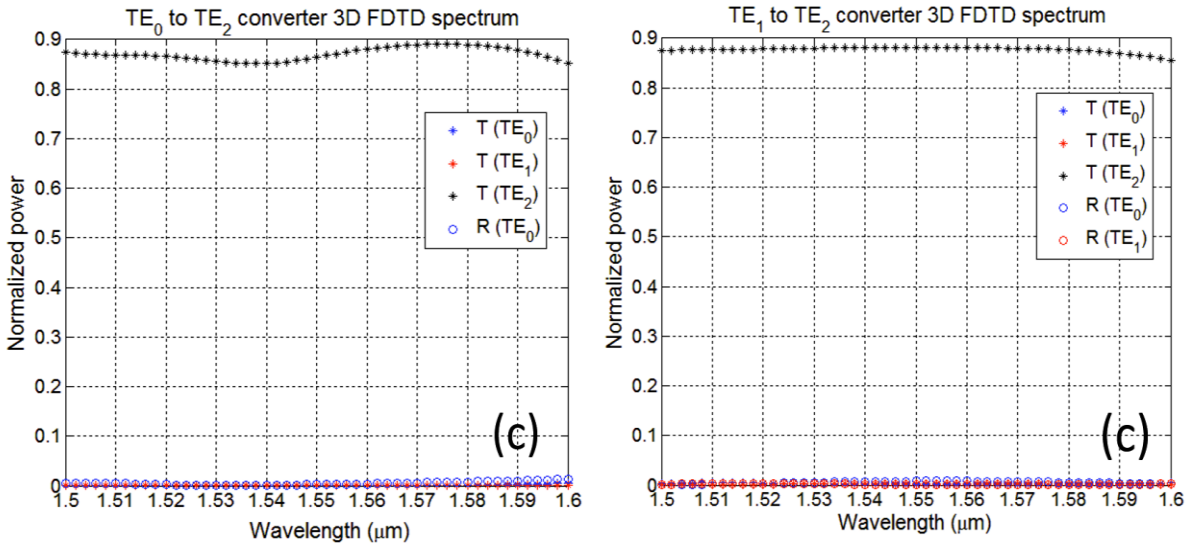


Figure 3.73 (a) FDTD spectrum of finalized TE_0-to-TE_2 converter with high mesh resolution (b) FDTD spectrum of finalized TE_1-to-TE_2 converter with high mesh resolution

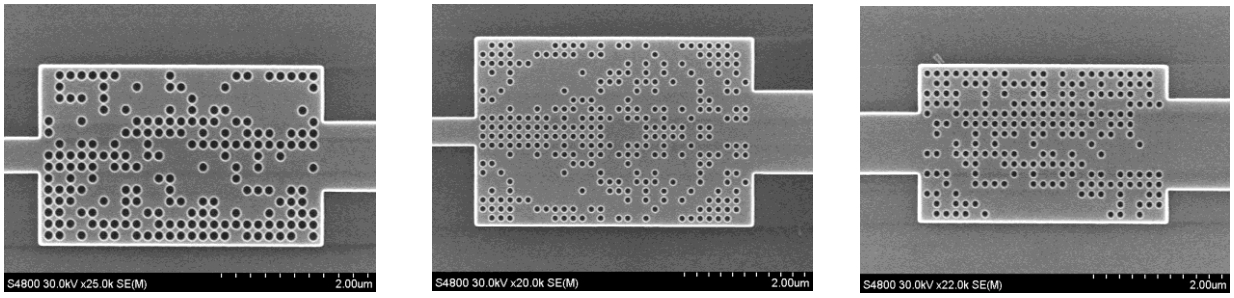


Figure 3.74 (a) SEM image of TE_0-to-TE_1 converter (b) SEM image of TE_0-to-TE_2 converter (c) SEM image of TE_1-to-TE_2 converter (courtesy of Mr. Yun Jo Lee)

The design is fabricated in Birck Nanotechnology Center at Purdue University and conventional cleanroom process without proximity effect correction is used. The inverse design devices are fabricated using Ebeam lithography and SEM images are given in Fig.3.74.

The layout for chip under tests is shown as figure below, which is an example of measurement under TE_1 input. TE_1 mode is excited using TE_1 ADC and its insertion loss can be characterized by back-to-back method. Without mode order converter beam should reach the top port, which is used to calculate measurement baseline. When converter is included in the circuit, beam will choose the bottom port as output where top and middle port gives the measured modal crosstalk. For input from TE_1 ADC, normalized input baseline is the power through double ADCs (assuming

TE_1 ADC and TE_2 ADC have similar loss). Power difference between TE_2 power measured (with converter) and normalized input baseline is regarded as converter's insertion loss.

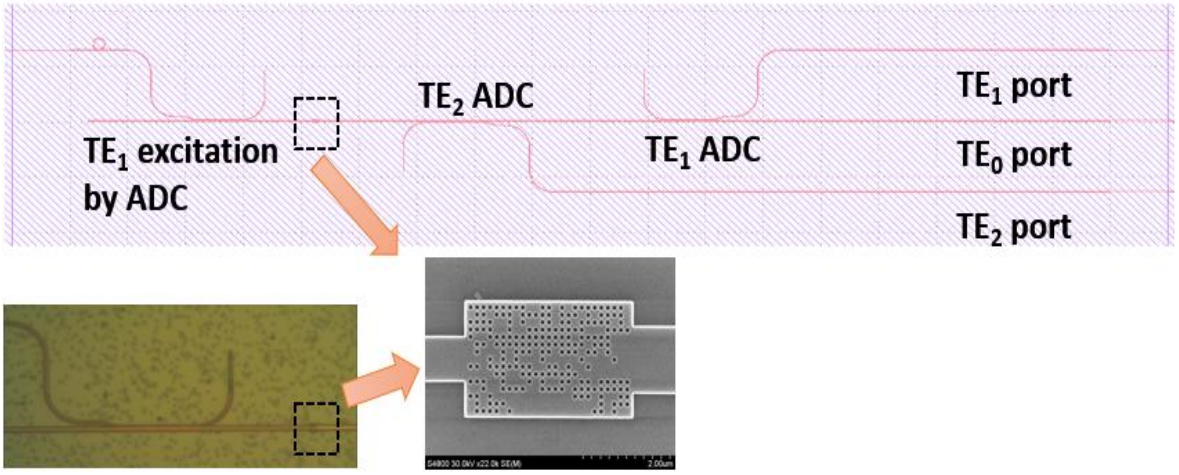


Figure 3.75 Measurement setup for TE_1-to-TE_2 converter with TE_1 input from single ADC

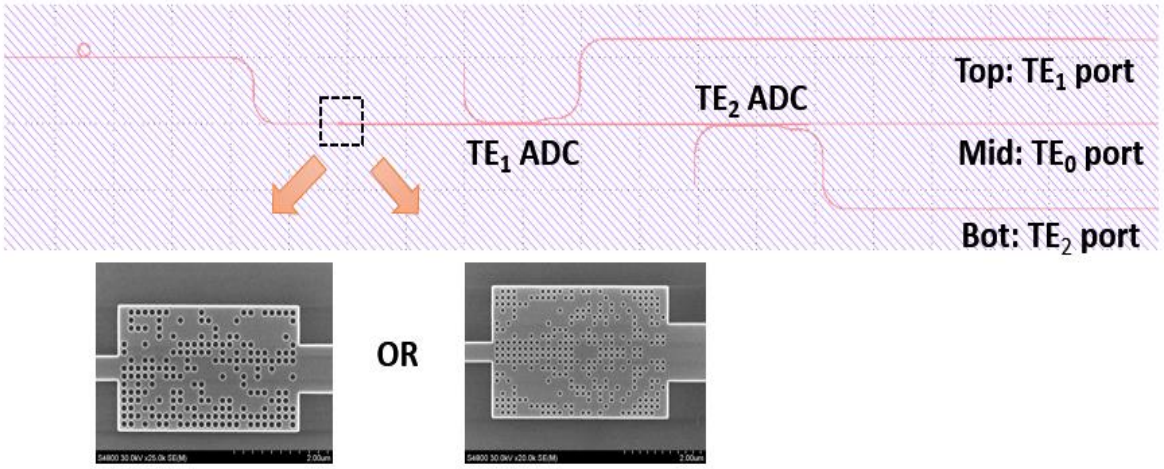


Figure 3.76 Measurement setup for TE_0-to-TE_1 converter and TE_0-to-TE_1 converter with TE_0 input

TE_0-to-TE_1 converter and TE_0-to-TE_2 are measured differently which uses TE_0 as input as shown in figure below. In this case power measurement baseline is the power (without converter) through single ADC and with similar approach insertion loss and modal crosstalk can be characterized.

Fig.3.77 shows measurement results of TE_1-to-TE_2 mode converters under various hole sizes. On the chip standard hole radius (50 nm), ± 5 nm and ± 10 nm radius is used on the chip to investigate

the fabrication sensitivity of inverse design. If input mode (TE_1) is not converted, majority of power will flow through top port (T3). Since input is efficiently converted to TE_1 with little modal crosstalk, output power is mostly measured at bottom port (T1) and only marginal power is measured at middle (T2) and top port (T3). This agrees with simulation that direct conversion between two high order modes can be achieved on such compact device.

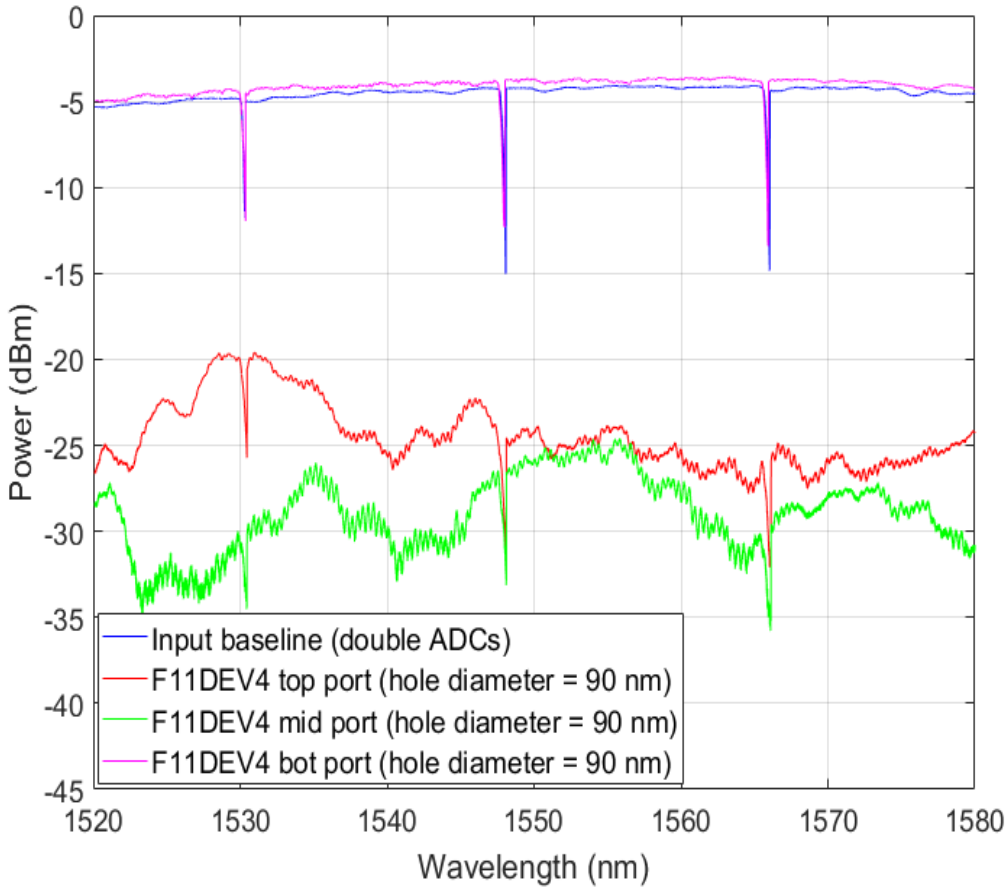


Figure 3.77 Measured spectrum of the best performed TE_1-to-TE_2 converter device

The best performed TE_1-to-TE_2 mode converter appears to have 45 nm hole radius due to fabrication deviation and its spectrum is shown in Fig.3.77. Surprisingly the power through converter device is even measured as 0.5 dB higher than double ADC baseline, which can be acceptable due to ± 0.5 dB edge coupling uncertainty. This at least means mode conversion is super-efficient at the best hole size. In terms of modal crosstalk, over 15 dB crosstalk is measured over 100 nm bandwidth, which is relatively consistent with -20 dB crosstalk in simulations.

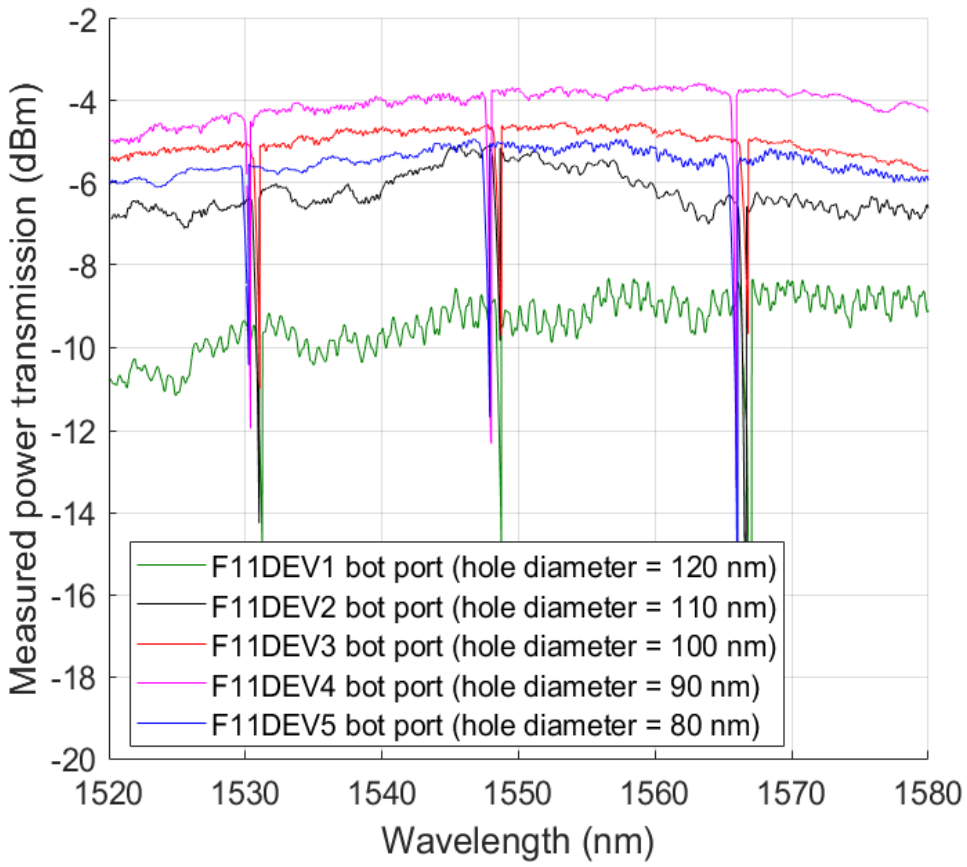


Figure 3.78 Measured spectrum of TE_1-to-TE_2 converters with various hole sizes

Fig.3.78 gives the mode conversion efficiency (insertion loss) measured over different hole diameters, where 90 nm gives the highest power measured. Although 100 nm hole radius is the nominal hole size in simulation, the best dimension is slighted shifted to 90 nm due to fabrication deviations. Fig.3.78 also shows that ± 10 nm offset from the best dimension (90 nm diameter) leads to more than 1.5 dB additional insertion loss, which also increases modal crosstalk and reflection. 120 nm hole diameter shows observable spectral noise which indicates strong reflection due to large scattering volume. Our experimental result shows quite strong fabrication sensitivities, which is a major drawback of topology optimized devices. If such device is based on air cladding, even more severe fabrication sensitivity is expected.

The TE_0-to-TE_1 converter and TE_0-to-TE_2 measured spectrum is shown in the figure below. Measurement shows almost lossless broadband conversion between TE_0 and TE_1 on the nominal hole sizes. However, TE_0-toTE_2 converter with the best hole size are damaged and cannot be

measured. The 80 nm and 110 nm diameter devices show 1.5 to 2 dB insertion loss. Based on dimension sensitivity analysis of TE_1-toTE_2 converter that ± 10 nm offset from nominal diameter leads to up to 1.5 dB additional insertion loss, ultralow insertion loss should theoretically be measured of the device with targeted hole sizes are intact.

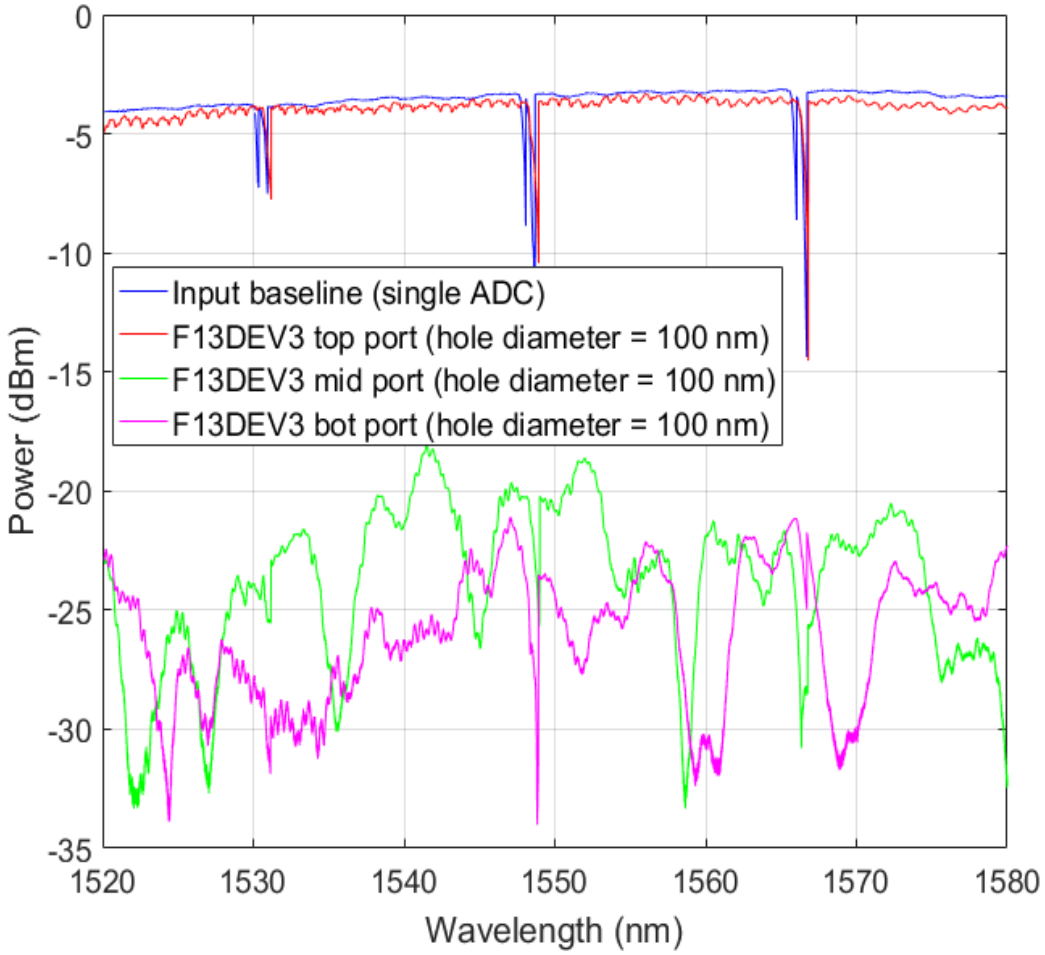


Figure 3.79 Measured spectrum of TE_0-to-TE_1 converters

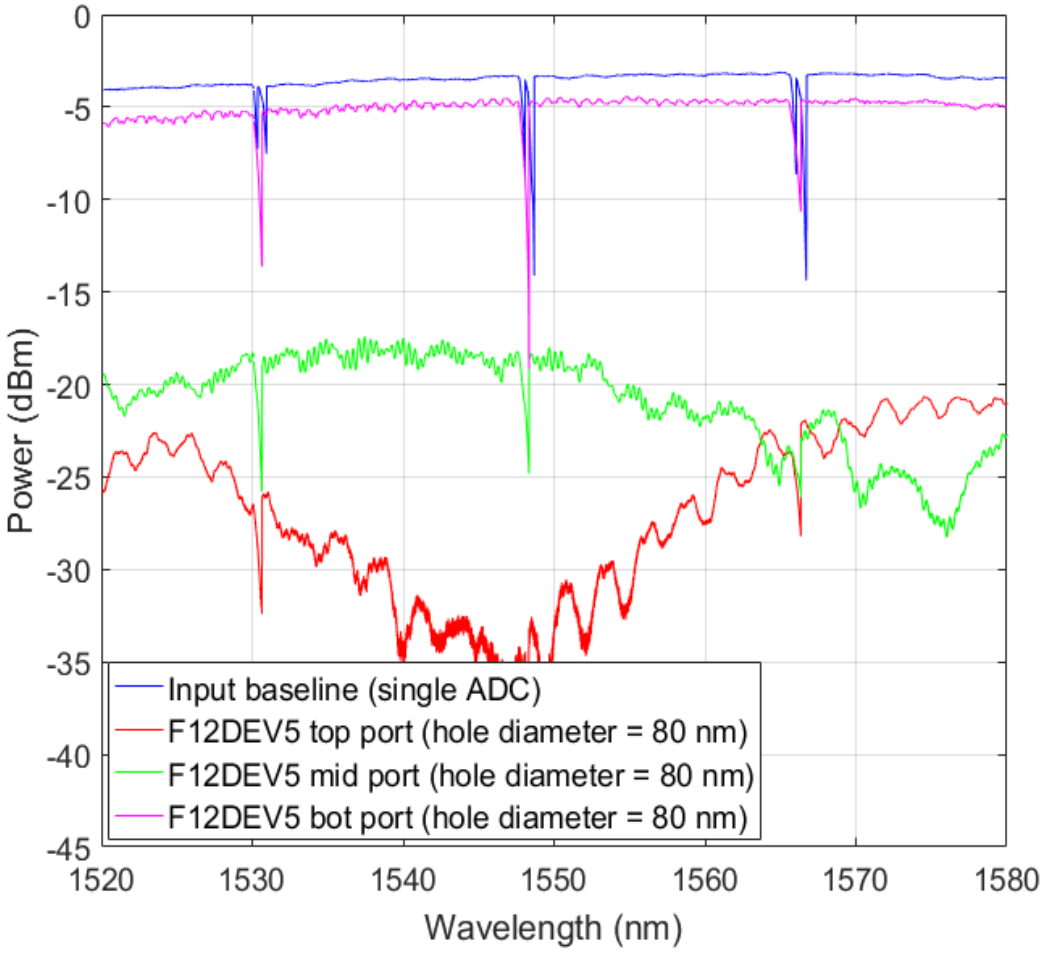


Figure 3.80 Measured spectrum of TE_0-to-TE_2 converters

Measured performance is compared with previous report in table 5. Adiabatic taper solution is the most efficient one from simulation, yet no experimental support has been demonstrated and such taper cannot achieve direct conversion between different high order modes. Both converter based on nano-trenches and photonic crystal waveguide can merely demonstrates TE_0-to-TE_1 conversion and performance is quite limited. The broadband converter based on inverse design (this work) shows experimental demonstration of mutual conversion between TE_0, TE_1 and TE_2 modes. Different high order modes can be directly converted without relying on TE_0 as a stepping stone.

Table 6 Comparison with previously reported mode order converters

State-of-art works for comparison	**Footprint**	**Performance**	**Comments**
Adiabatic taper [68]	~20 μm long	0.1 dB broadband insertion loss simulated	TE_0 conversion to TE_1, TE_2 and TE_3 Crosstalk and reflection not evaluated
TE_0 to TE_1 converter (photonic crystal) [86]	6.3 μm long	2 dB insertion loss and -12 dB crosstalk over 43 nm bandwidth measured	No other types of mode conversion is achieved
TE_0 to TE_1 converter based on cascaded trenches [85]	5 μm long	85% broadband efficiency (0.7 dB insertion loss) simulated	No other types of mode conversion is achieved Very small min feature size (~30 nm)
Colorless subwavelength structure by inverse design (this work) [78]	~ 4 μm long	< 0.5 dB insertion loss near nominal hole size, -15 dB modal crosstalk measured	Mutual conversion between TE_0, TE_1 and TE_2 in experiment Can theoretically be applied for arbitrary mode order conversion

CHAPTER 4. ON-CHIP PHOTONIC DEVICES FOR POLARIZATION AND WAVELENGTH HANDLING

4.1 Introduction

More widely used on-chip multiplexing techniques are wavelength division multiplexing (WDM) and polarization division multiplexing (PDM). Though widely used in the industry, passive devices for WDM and PDM are still research areas in order to obtain better balance between performance, footprint and fabrication robustness.

Polarization handling devices are widely used for on-chip (PDM) system. The on-chip PDM allows dual polarizations to be used as two orthogonal channels, which doubles the data capacity. A number of PBS have been demonstrated on high index contrast material platform (such as SOI) [95][96][97], where TE and TM can be more easily split due to different optical confinement. Fig.4.1 [98] shows an example that TM couples to cross port while TE remains in through port on SOI platform.

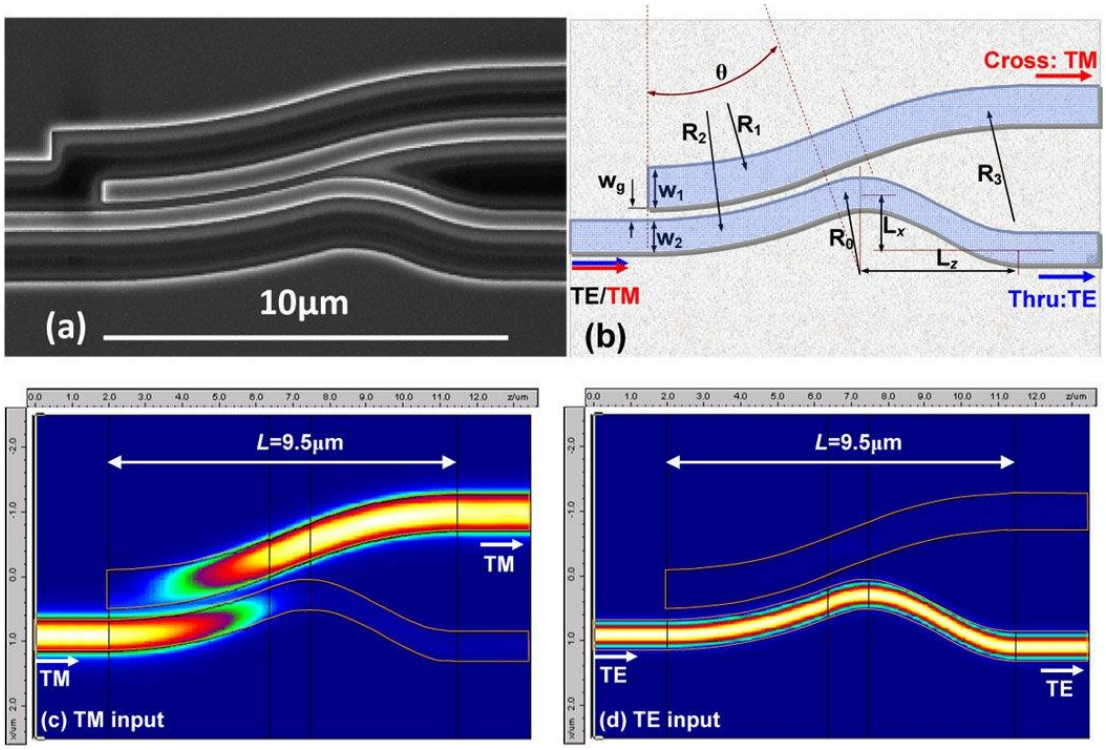


Figure 4.1 previously reported PBS on SOI platform based on evanescent coupling [98]

Another essential device for polarization handling is called polarization splitter and rotator (PSR). PSR has been actively developed for of photonic transceiver chips. For example, fiber edge coupling cannot guarantee the input polarizations while several essential SOI components are still polarization dependent. As a result, polarization diversity scheme is proposed to split input beam polarizations and rotate the TM fraction into TE. A vast number of PSR designs have been reported on both Si and Si_3N_4 and breaking vertical symmetry is required for polarization rotation. Hence SOI PSR with alterative top cladding (air, nitride and polymer) [99] is a popular option whereas another approach is to develop partially etched Si waveguide to break vertical symmetry and SiO_2 can still be used for top cladding.

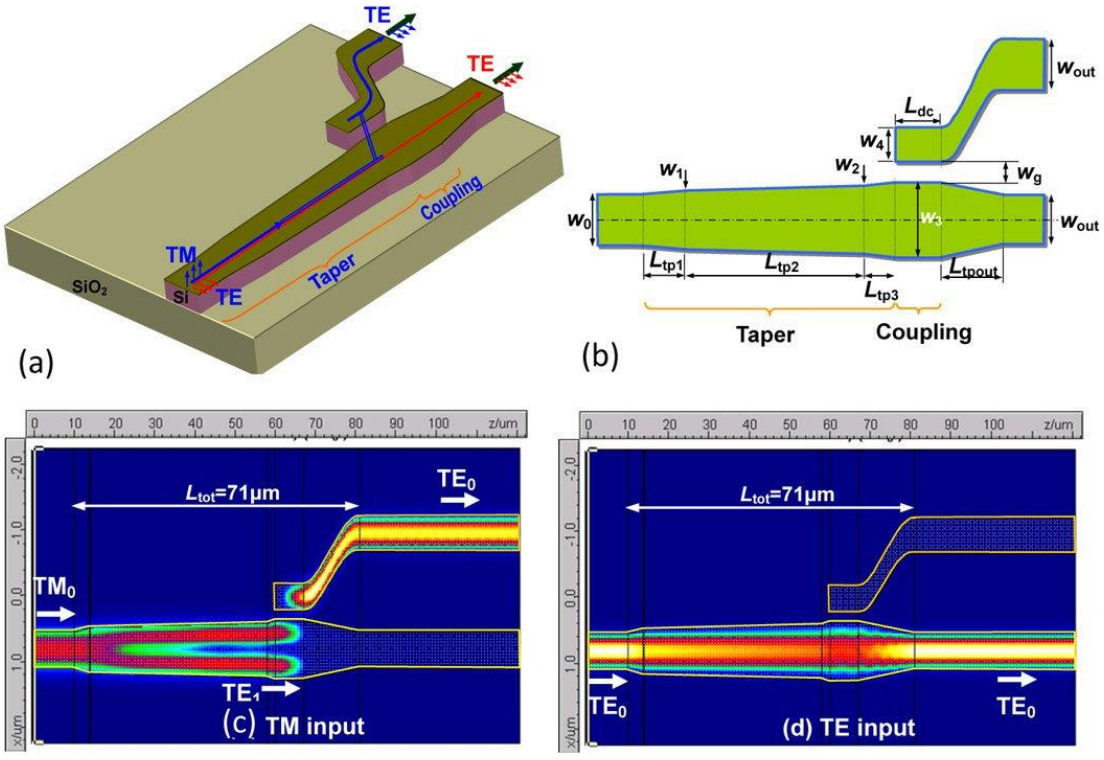


Figure 4.2 previously reported PSR on SOI platform based on evanescent coupling [73]

One problem for PBS and PSR is the insufficient extinction ratio since no more than 30 dB has been experimentally demonstrated. In addition, industry is seeking for a broadband PBS and PSR with similar spectrum response for both TE and TM polarizations, but this is almost impossible by any existing approach based on evanescent coupling. Typically, the polarization without evanescent coupling (usually TE) is perfect while the other polarization shows narrowband

performance [73][99] due to evanescent coupling. Here in this chapter we investigate PBS and PSR and try to seek theoretical solutions for these problems. The numerical demonstration of silicon nitride PBS has been reported on CLEO conference in 2017 [100].

Another topic for this chapter is the multiplexing device for WDM and array waveguide grating (AWG) is the industrial standard option [47]. WDM is a widely implemented multiplexing technology and various multiplexing devices including AWG, Echelle grating and micro-ring resonators are used for WDM MUX and DEMUX. AWG has been the most powerful and reliable one among all options. Only the other hand, AWG requires massive device footprint and it's known as the most complicated passive photonic device. This this chapter a technology-free (without relying on foundry PDK) design toolbox is designed for AWG including automatic layout generation and numerical simulation.

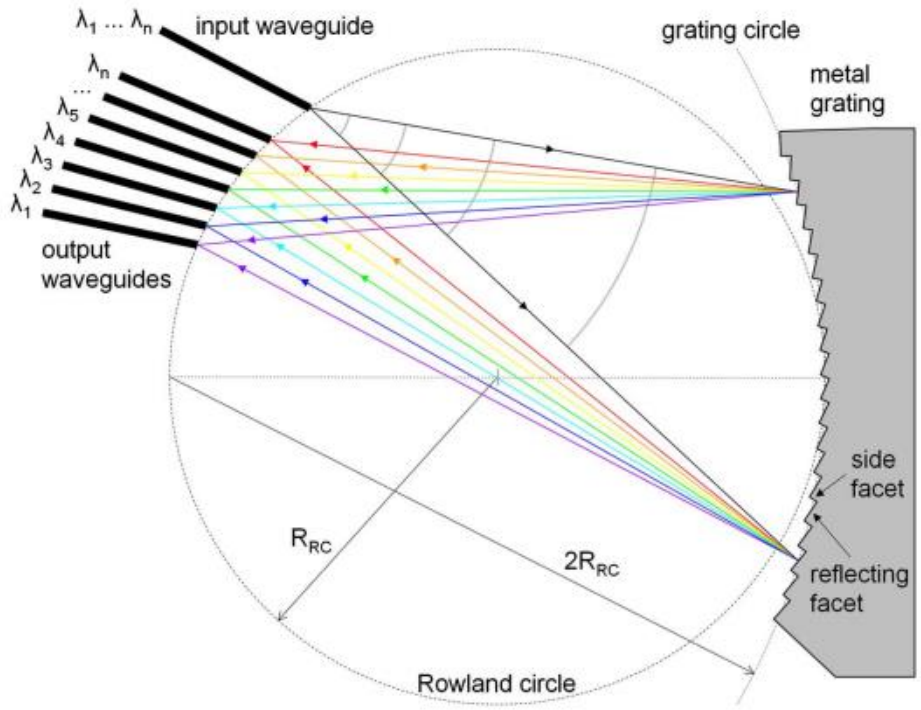


Figure 4.3 WDM MUX and DEMUX based on Echelle grating [101]

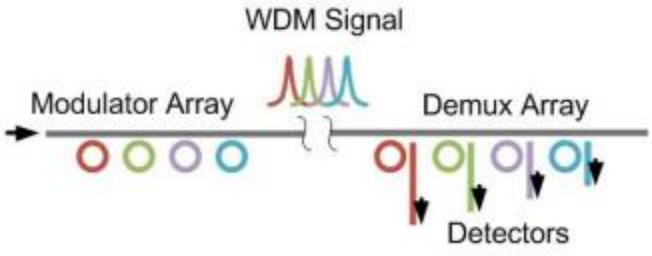


Figure 4.4 WDM MUX and DEMUX based on micro-rings [102]

4.2 MMI with phase delay line based Si3N4 polarization beam splitter (PBS)

Silicon nitride (Si_3N_4) is a promising integration platform for on-chip optical interconnects due to its CMOS compatibility. With lower index contrast than silicon-on-insulation (SOI) platform, nitride waveguides suffer much lower scattering loss from sidewall roughness [38]. Such benefit pushes the progress on developing nitride integrated devices on like high Q ring resonators [3] and arrayed waveguide grating (AWG). However, due to the low birefringence property, it is challenging to achieve polarization handling due to close effective index between TE and TM mode.

An ideal PBS should offer broadband high efficiency and extinction ratio (ER) and the spectrum should be symmetric for both polarizations. PBS also prefers single layer structure, compact footprint as well as fabrication robustness. Here a single-layer Si_3N_4 PBS is designed to meet those expected requirements.

Here we demonstrate a single layer Si_3N_4 PBS based on 2 by 2 MMI with phase delay line on one arm [103][100]. Given $\pm \pi/2$ relative phase shift [103], the input beam will selectively choose the output port which can be utilized to split polarizations. Our proposed design shows 20 dB extinction over 100 nm bandwidth and 30 dB extinction covering C band. With insertion around 0.5 dB, our PBS can be even cascaded [104] to further enhance ER without considerable insertion loss penalty. A flat-band extinction response can also be achieved with two-stage PBS cascade where each stage is designed with center wavelength shifted.

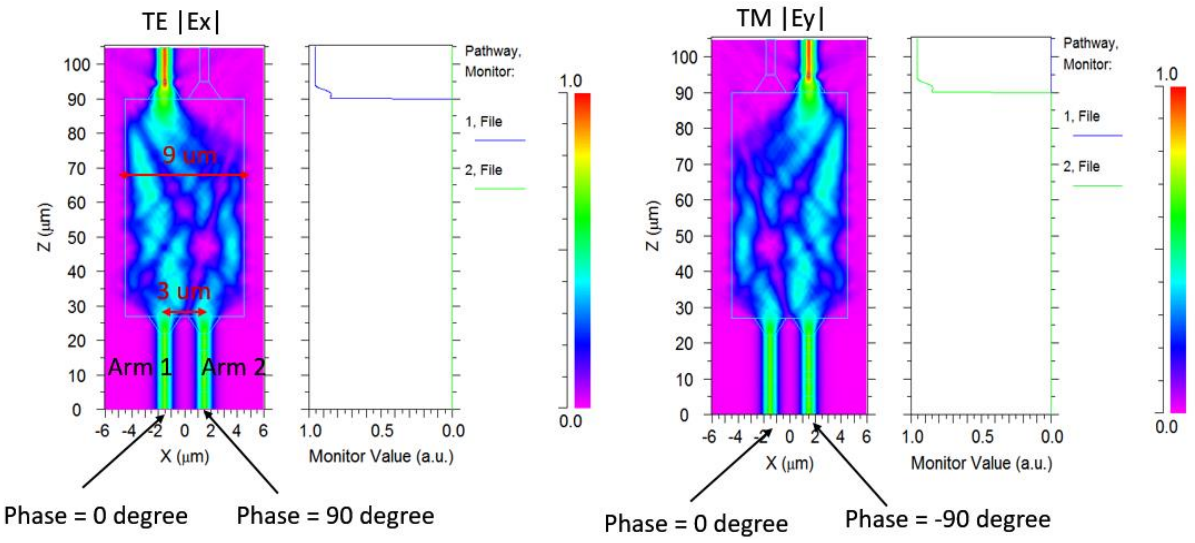


Figure 4.5 3D BPM simulation assume TE arm2 has π/2 phase shift while TM arm2 has -π/2 phase shift

The basic idea is based on MMI with pair excitations. Theoretically at $\pm W_{MMI}/6$ with $\pm \pi/2$ relative phase shift, two beams will be mapped to different image locations. When this idea is applied in order to split TE and TM polarizations, one should try to develop a scheme that allow two polarizations to be evenly split and then phase shifted by $\pm \pi/2$. Such PBS can theoretically obtain similar extinction ratio spectrum for both polarizations, provided that MMI with low index contrast is designed with little polarization dependence. Fig.4.5 shows 3D BPM calculations from Rsoft, where a 450 nm thick nitride MMI is simulated at 1550 nm wavelength with two input beam given proper phase shift. A 2 by 2 MMI with W_{MMI} = 9 μm & L_{MMI} = 61.5 μm is used where MMI port waveguides are linearly tapered to 2 μm wide with 3 μm center-to center spacing. BPM simulation shows both TE and TM modes can travel through with trivial insertion loss, which validating the polarization independence. Here we term this structure "intrinsic", which represents perfect phase condition can be obtained by dictating phase of source injection.

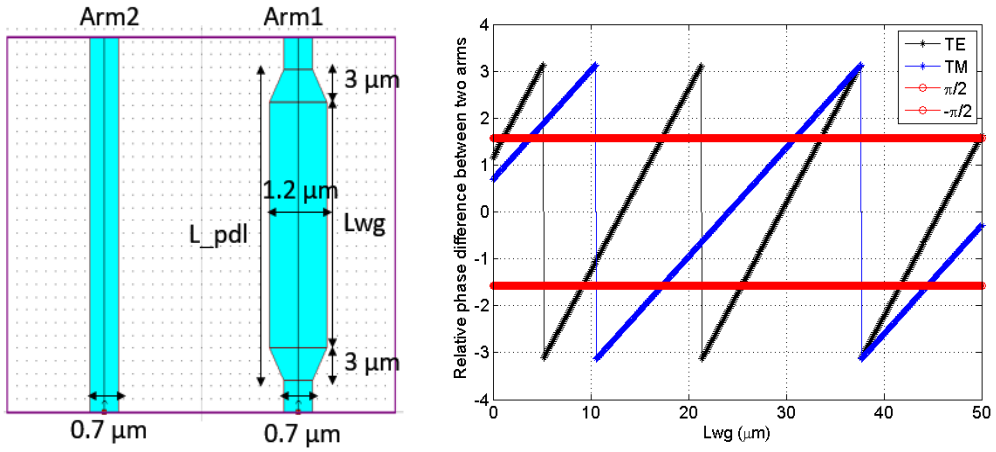


Figure 4.6 (a) Phase delay line schematic used in Rsoft BPM simulation (b) analytic calculation of phase delay vs. L_{wg}

Phase delay line (PDL) is the challenging part of design because TE and TM requires ± π/2 relative phase shift between two arms at the same time. As shown in fig.4.6, PDL is designed such that one arm is tapered to a wider width of 1.2 µm in 3 µm taper length, followed by a uniform section (L_{wg}) and then is tapered back. Analytic phase calculation is taken which assumes that at linear taper section effective index is estimated as average value from narrow and wide end. As L_{wg} is scanned in Matlab, there can be a solution found with one arm leads π/2 phase for one polarization while lags π/2 phase for the other polarization. With analytic calculation 17.2 µm turns to be the shortest solution but with BPM optimization L_{wg} = 16.6 µm seems to give the best extinction at 1550 nm wavelength. With 3D FDTD simulation, we further validate best performance occurs at L_{wg} = 16.6 µm and deviation from analytic model might be caused by inaccuracy of phase velocity estimation at linear taper section.

Fig.4.7 shows 3D FDTD calculated field plot and power transmission spectrum for the intrinsic structure and real structure with Y splitter and PDL. Field plot clearly shows that TM beam propagate through the top port while TM travels though bottom plot. FDTD calculated intrinsic spectrum shows theoretically the upper bound performance the device can achieve. However, the real device (entire PBS) only a fraction of intrinsic performance obtained, leading to a narrowband ultrahigh extinction ratio spectrum over C band. This happens because PDL is only designed at a single wavelength (1550 nm) and away from central wavelength increasing phase error can further

reduce the extinction ratio (ER). In summary, our proposed PBS can achieve a symmetric response for both polarizations with > 20 dB ER over of 100 nm bandwidth and > 30 dB ER over C band.

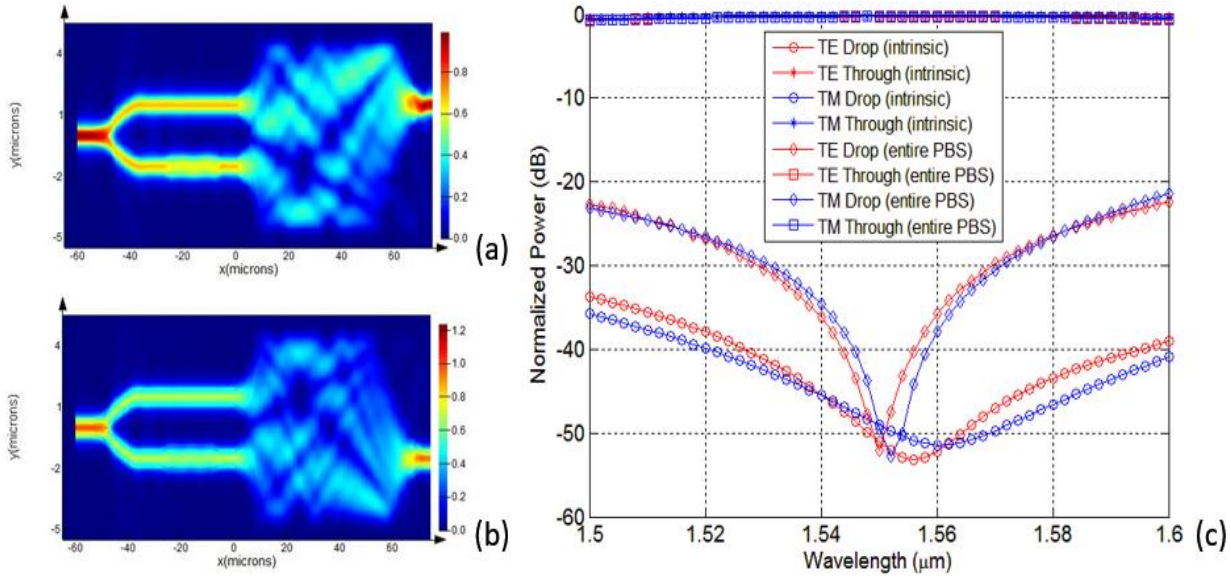


Figure 4.7 (a) |E| plot for TM input (b) |E| plot for TE input (c) FDTD calculated PBS transmission spectrum of both intrinsic and actual performance

Our designed PBS splits polarizations in a linear process, which means performance can be boosted by multi-stage cascade. With calculation, single stage PBS leads to ~ 0.5 dB insertion loss with 30 dB ER over C band only. Nonetheless there is opportunity to obtain a broadband high ER by PBS cascade. Fig.4.8 illustrates the schematic of cascaded PBS configuration TE will choose the lowermost port as output while TM choose the uppermost one.

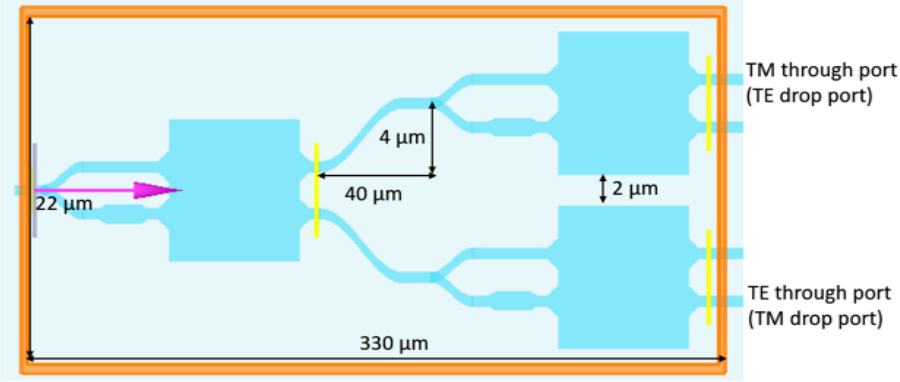


Figure 4.8 Schematic of cascaded PBS configuration

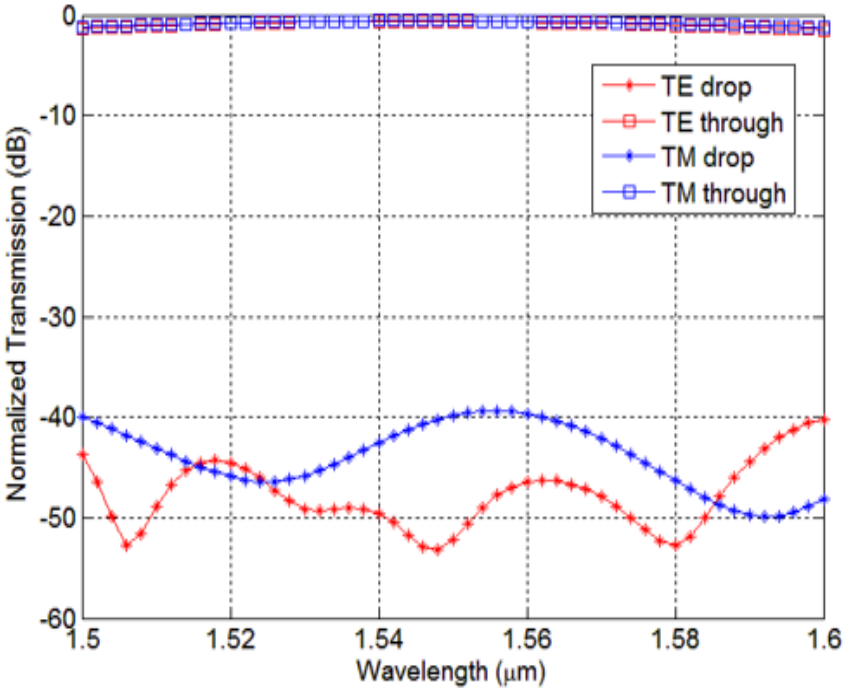


Figure 4.9 FDTD spectrum of cascaded PBS with adjusted PDL

In order to flatten the ER spectrum, PDL of both stages are tuned slightly. Stage 1 PBS is designed with 30 nm wider PDL width to redshift the center wavelength from 1550 nm while stage 2 PBS with 30 nm narrower PDL width to obtain the similar amount of blueshift. The combination of two shifted narrowband curve yields a relatively broad ER spectrum with ER ~ 38 dB over 100 nm spectrum. The E field distribution plot at 1550 nm wavelength is shown in Fig.4.9.

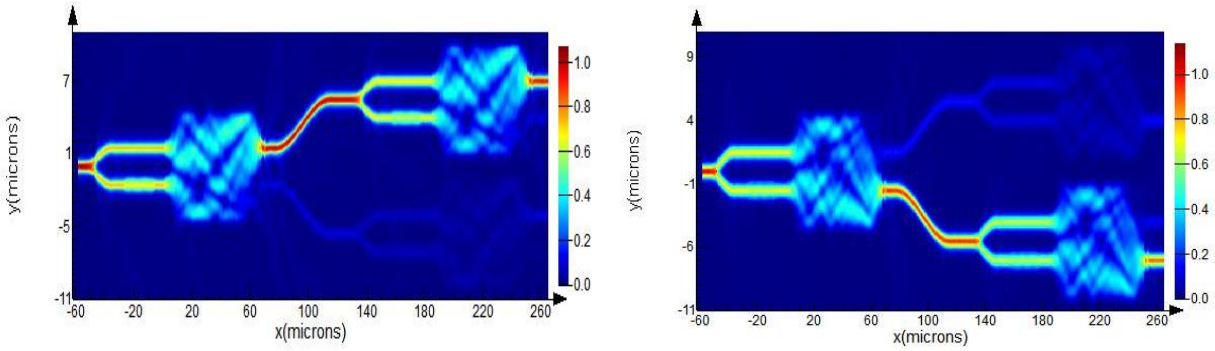


Figure 4.10 (a) |E| plot for TM input (b) |E| plot for TE input

In conclusion, a PBS based on MMI with phase delay line is proposed on silicon nitride platform. With one stage PBS, 20 dB extinction with 0.5 dB insertion loss is theoretically demonstrated over 100 nm bandwidth with peak extinction at 1550 nm wavelength. With cascaded PBS, flat-band extinction over 38 dB can be achieved for both polarizations. This structure based on PDL can be dimension sensitive yet by multi-stage cascade with central wavelength offset, fabrication sensitivity can be partially alleviated.

Although this numerical solution is neat, it's worth mentioning that such PBS requires ~ 450 nm nitride thickness, which is not CMOS compatible (nitride thickness within 300 nm). Since MMI prefer thick nitride and PDL prefer thin nitride, with 450 nm thickness is chosen after some tradeoff. If nitride thickness within 300 nm is demanded, such PBS solution may not perform well.

4.3 SOI polarization splitter and rotator (PSR) with cascaded ADC

PSR has been developed by many researchers with various approaches. However, one of the most widely used configuration is reported by D.Dai (Fig.4.2) which starts with a taper under asymmetric cladding to convert TM_0 into TE_1 while TE_0 remains unchanged [73]. Then by ADC (phase matched with TE_1) the TE_1 power is extracted by evanescent coupling while TE_0 remains propagating ignoring ADC due to phase mismatch. This initial setup is originally proposed with limited ER and in 2016 [99], The author claimed that MMI mode splitter which filters TE_1 can improve ER. Nonetheless, with experiment still less than 20 dB is demonstrated and this section further investigate this specific type of PSR.

The device cross-section is shown in Fig.4.11 (a) where Si waveguide with 600 nm thickness nitride [73] top cladding is used. Breaking the vertical symmetry is important to allow polarization rotation and by scanning the waveguide width, effective index of first three modes are plotted in Fig.4.11 (b). There is a mode crossing region at around 750 nm width where TM_0 and TE_1 modes get hybridized. As a result, with a linear taper covering 750 nm width TM_0 can be converted to TE_1 and conversion efficiency increases with longer taper length. Hence in geometry setup, a three-stage piecewise taper is used such stage 1 width expands from 400 nm to 650 nm, stage 2 width from 650 nm to 800 nm and ultimately stage 3 expands from 800 nm to 1000 nm to evade from that mode conversion region.

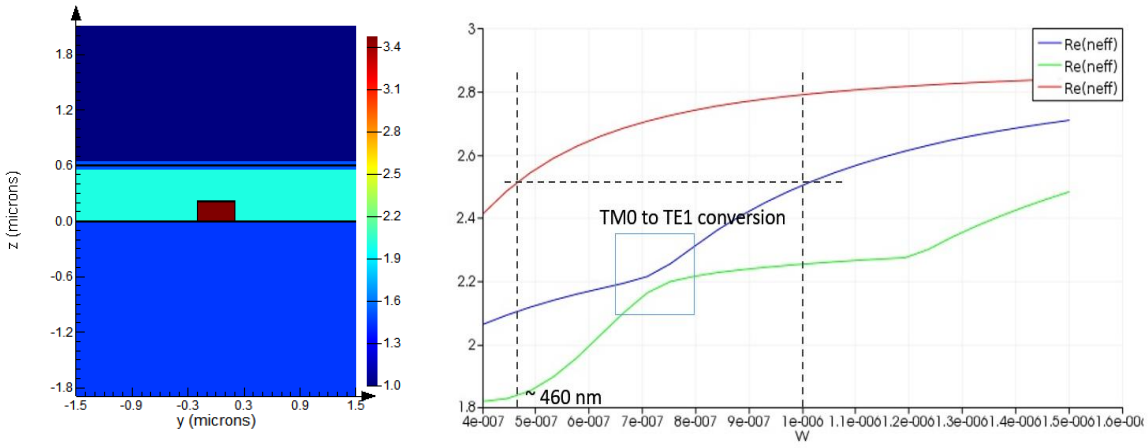


Figure 4.11 (a) PSR device cross-section (b) scanned effective index vs. Si waveguide width at 1550 nm wavelength

Fig.4.12 shows the |E| plot where TM_0 is converted to TE_1 with FDTD spectrum illustrated. Although insertion loss becomes almost negligible, there's still roughly -20 dB TM_0 power remaining as crosstalk. With EME calculation, further extension of L2 can reduce crosstalk which inevitably leads to larger footprint. However, with FDTD simulation, even longer L2 (~150 μm) still gets very limited returns for crosstalk suppression. In reality, no matter how long taper is used, TM_0 residual cannot be eliminated. TM_0 residual sets up an upper bound for ER and additional TM_0 filter can be deployed to improve ER.

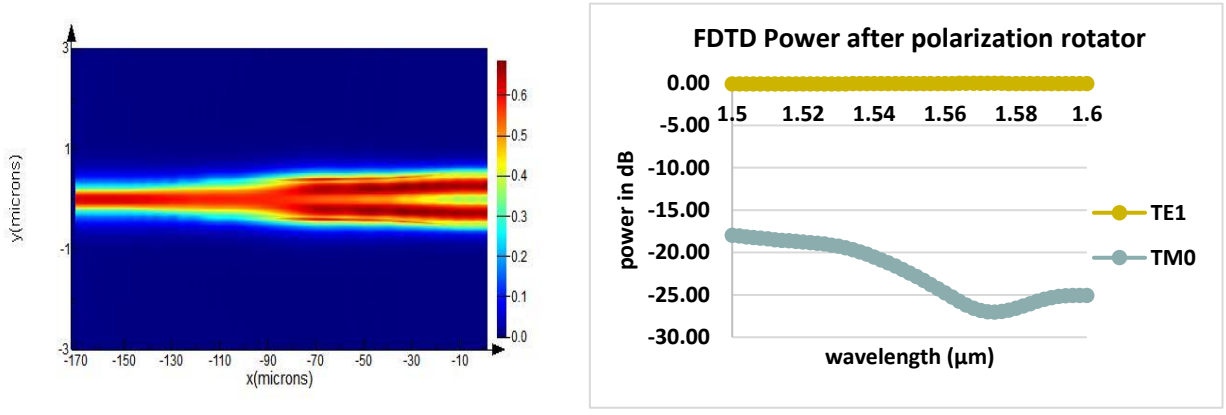


Figure 4.12 (a) |E| plot for a three-stage piecewise taper that converts TM_0 to TE_1 (b) 3D FDTD transmission spectrum for L1 = 30 μm, L2 = 80 μm and L3 = 30 μm

After TM_0 to TE_1 converter, ADC is designed such that TE_1 (from TM_0 input) would couple away as TE_0 while TE_0 mode input remains unaffected. With some optimizations, Fig.4.13 (a) shows the ADC design with 200 nm coupling gap size assuming input mode is purely TE_0 or TM_0 (which cannot be realized in PSR). Disadvantage of this ADC is that TE_1 to TE_0 coupling is narrowband and fabrication sensitive, resulting in residual TE_1 after ADC which turns back to TM_0 with certain proportion after taper. As a result, D. Dai claimed the MMI mode filter to be used to filter those TE_1 power as shown in Fig.4.13 (b). D.Dai's design [99] failed to include two output ports which is theoretically mistaken, leading to strong reflection.

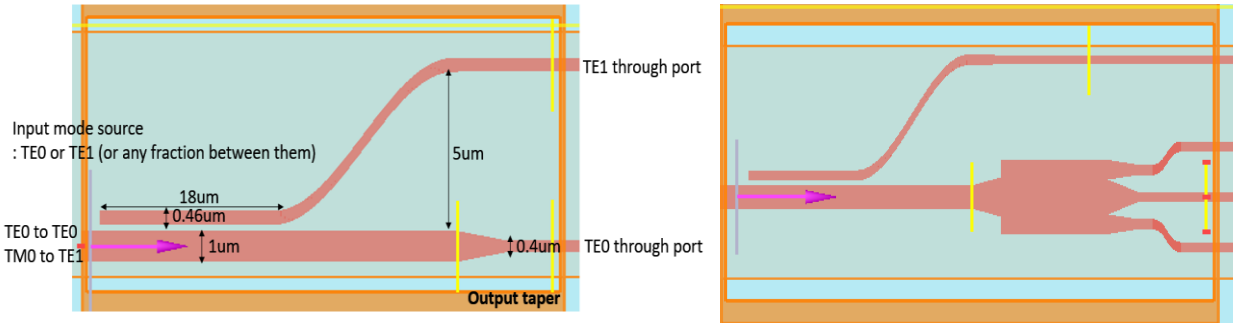


Figure 4.13 (a) ADC for conventional PSR (b) ADC with MMI TE_1 filter

The geometry is further corrected in Fig.4.13 (b) where top and bottom ports are included [72] to reduce reflection. With FDTD simulation, result indeed shows ~ 10 dB crosstalk power deduction (total power curve), which seems to agree with D. Dai's argument. Nonetheless this simulation assumes that stage 1 TM_0-to-TE_1 converter is perfect which is not true. In fact, after stage 1 there's ~ -20 dB TM_0 noise power remaining, which overwhelm the result shown in Fig.4.14. When the entire PSR is simulated, only 20 dB ER is obtained due to imperfect stage 1 design, which makes MMI TE_1 filter almost meaningless. Hence, we design a TM_0 filter to replace MMI TE_1 filter to further suppress TM_0 crosstalk power.

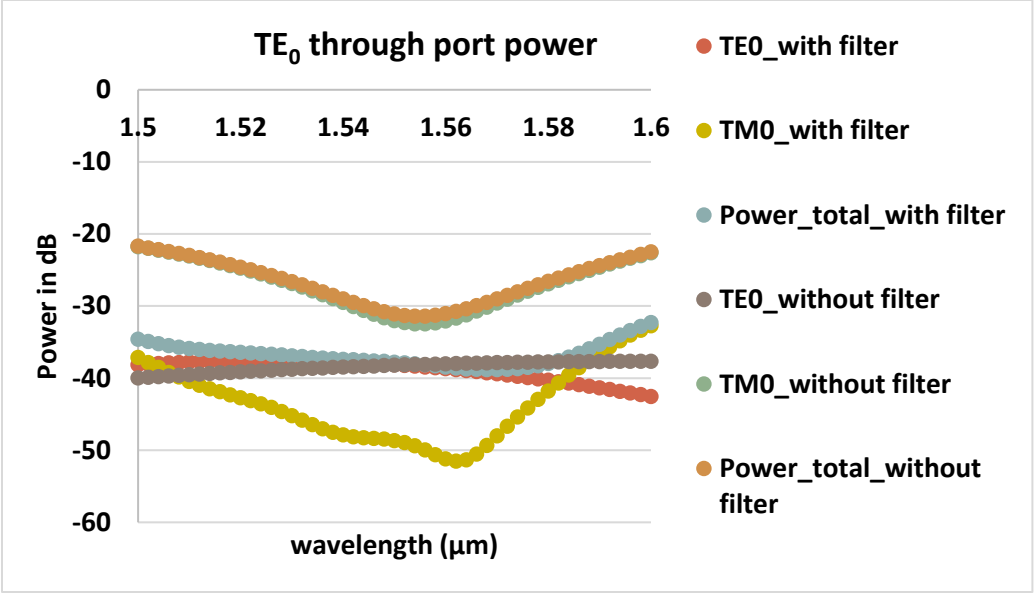


Figure 4.14 FDTD calculated power spectrum assuming TE_1 mode is launched in structure shown at Fig.4.13 (b)

TM_0 filter is designed as cascaded ADC where TM_0 is coupled away while TE_0 remains unaffected. 420 nm coupling gap and 1.12 µm access waveguide width are used such that effective index of TM_0 at 400 nm wide waveguide matches with that of TM_1 at access waveguide. As consequence TM mode will be filtered (coupled) away by ADC while TE_0 remains unaffected due to phase mismatch. Nonetheless, ADC only gives a narrowband filtering centered at 1550 nm. In order to achieve broadband TM_0 filtering, two identical ADCs with different length are used which redshift and blueshift the extinction curve and a combination of both renders a broadband high extinction spectrum.

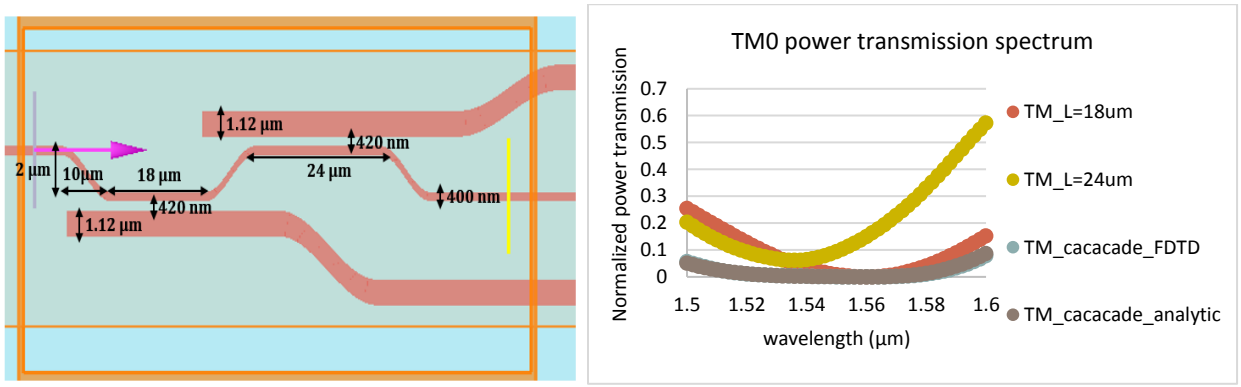


Figure 4.15 (a) TM_0 filter based on cascaded ADC with nitride top cladding (b) FDTD calculated TM power after ADC

As illustrated in Fig.4.15 (b), two individual ADCs with length at 18 μm and 24 μm are simulated, which shows minimum crosstalk at wavelength offset from 1550 nm. The cascaded structure illustrated in Fig.4.15 (a) is also simulated and spectrum shows much broader bandwidth with lower TM noise power remaining. FDTD simulated spectrum also agrees well with analytic multiplication of power transmission through each individual stage. Theoretically even large number of ADCs can be cascaded here to further suppress TM power but for simplicity only two ADCs are used here. The complete PSR schematic is shown in Fig.4.16.

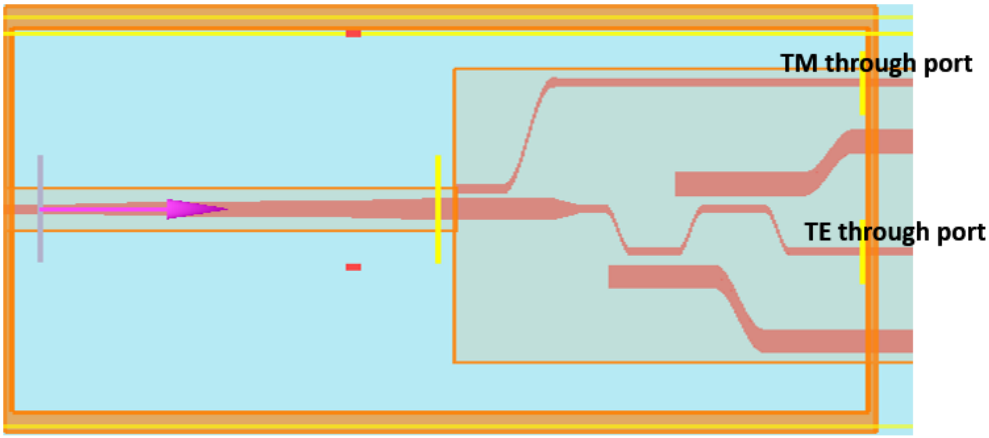


Figure 4.16 Complete structure of PSR with ADC based TM filter

Fig.4.17 shows the |E| distribution for 3D FDTD simulation while Fig.4.18 shows the calculated spectrum of PSR with ADC filter. Obviously, field plot indicates the TM_0 residual is indeed extracted by ADCs. Simulation spectrum shows < 0.5 dB insertion loss and ~ 30 dB ER over 80 nm wide bandwidth which is a significant improvement. TM crosstalk can be further reduced if additional ADC is cascaded.

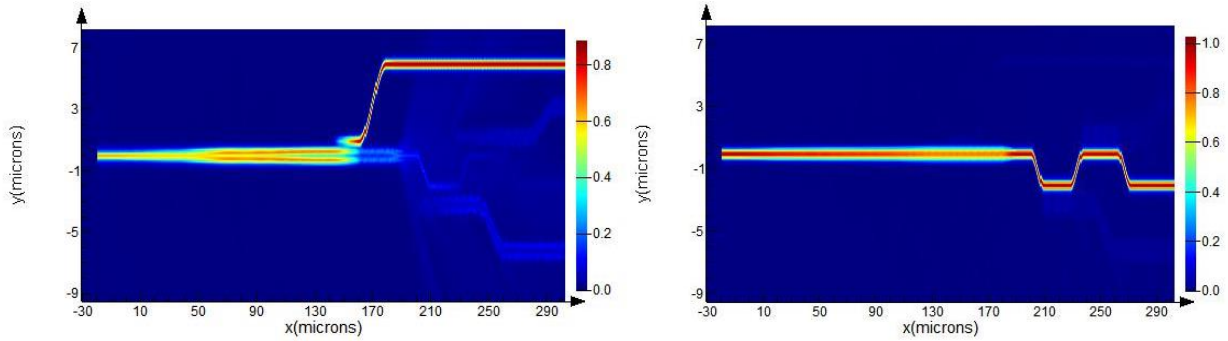


Figure 4.17 (a) PSR |E| plot for TM_0 input (b) PSR |E| plot for TE_0 input

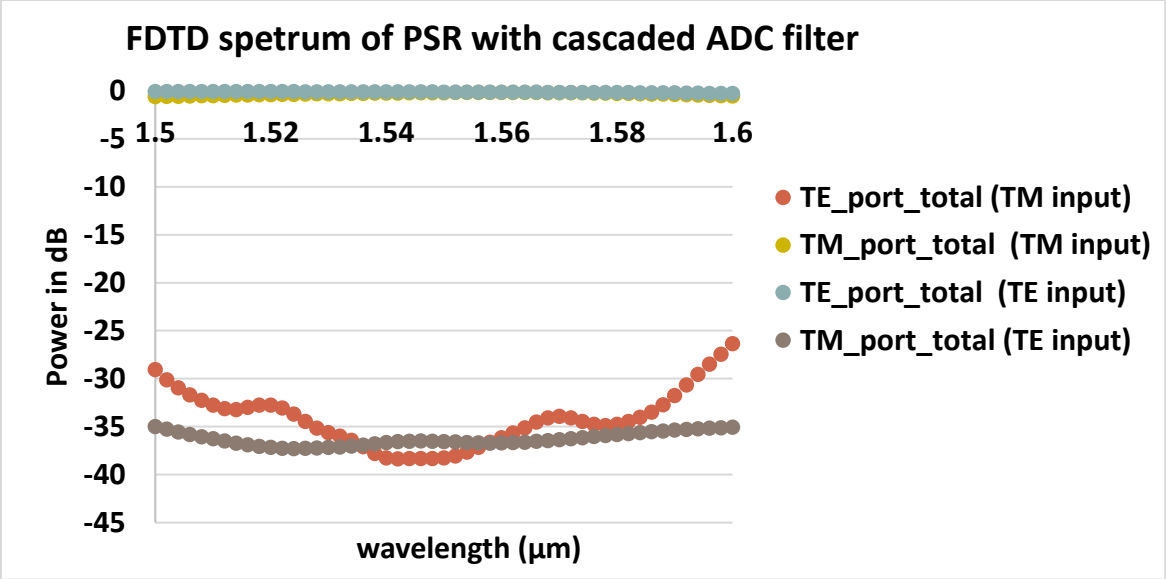


Figure 4.18 3D FDTD calculated spectrum for PSR with cascaded ADC filter

In summary PSR based on TM_0-to-TE_1 conversion is investigated and underlying causes for insufficient ER are explored. With imperfect TM_0-to-TE_1 converter, simply filtering residual TE_1 after ADC is almost meaningless. Instead, TM_0 filter based on cascaded ADC is deployed which helps PSR achieving a broadband 30 dB ER spectrum.

4.4 Arrayed waveguide grating (AWG) design

AWG is known as the industrial standard (de)multiplexing device for on-chip WDM [47], AWG operates by wavelength dependent phase front, which leads to in-plane beam steering depending on wavelength [105][106]. AWG is consisting of input and output star couplers connected by arrayed waveguides and adjacent arrays offer fixed path length difference (dL). dL is rigorously calculated to offer multiple integer of 2π phase shift at central wavelength and that integer is called grating order [47][107]. At central wavelength the phase front after arrayed waveguide is flat hence beam is not steered and will refocus at central output waveguide due to optical reciprocity. Any other wavelength offers linearly tilted phase front, which steers the beam into different direction in plane.

Unlike other WDM multiplexing devices such as echelle grating and ring resonator, AWG demands nice phase front to steer beam. Hence AWG performance can be strongly affected by

phase error, especially on high index contrast platform (such as SOI). Waveguide sidewall roughness will accumulate phase errors along arrayed waveguides [106], causing negative impact on spectrum of AWG.

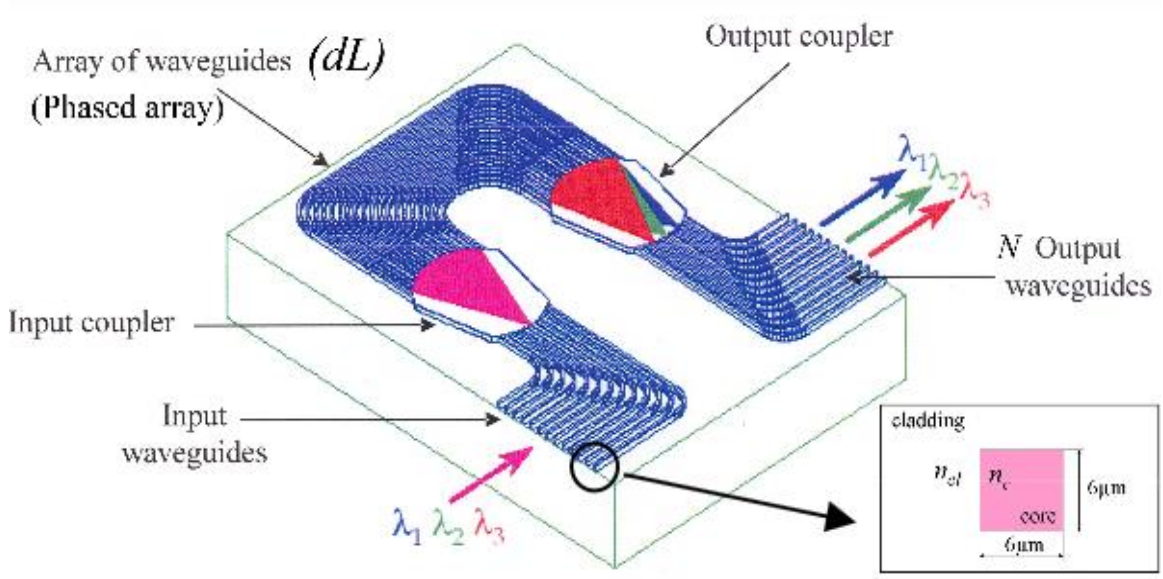
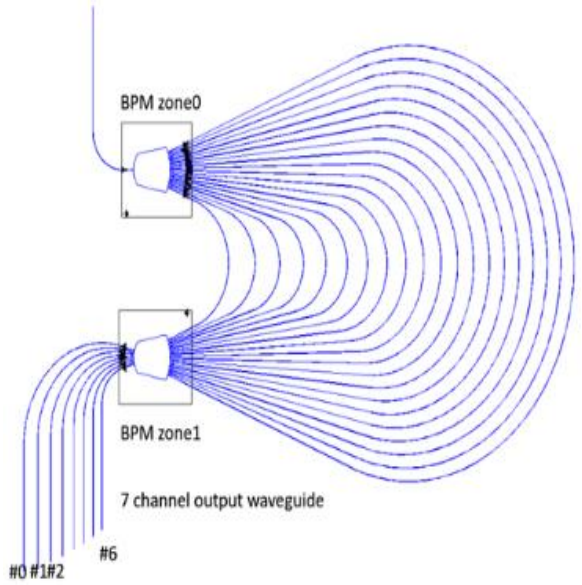


Figure 4.19 Schematic of AWG [107]

Phoenix Optodesigner is leading electronic design automation (EDA) tool in photonics industry that allow user to draw complicated photonic structure. Here for example, a 700-nm thick nitride 1-to-7 AWG structure with dioxide cladding is first generated by some scripts (~ 100 lines code). User can specify some initial parameters such as waveguide dimension, number of input/output and arrayed waveguides, grating order spacing between waveguide ports etc. Here it's assumed that no sidewall roughness is included on nitride waveguides and the assumption is safe since roughness is not giving strong influence due to low index contrast.




```
double Wwg = 0.7, Twg=0.7, nclad=1.444, ncore=2.0;
int A=90, Nin = 1, Nout = 8;
int M = 20, Md = 0, Nchan = 8, Nd = 0;
double Di = 3, Do = 3;
double Rin=60,Rout=60,L_extend_max=200;
double Wt_a=3,Wt_b=3,Ltaper=10,Lwg=15, Lwg2=30;
double Lspan=300, L0_ratio=1.8, L_start=600;

double DispersionFactor=ngroup/neff;
double GratingOrder = round(Lambda0/(Nchan*DLambda*DispersionFactor));
double Ro=(neff/GratingOrder)*((Di*Do)/(DLambda*DispersionFactor));
double Ri=Ro/2;
```

Figure 4.20 1-to-7 AWG layout generated by Phoenix and some sample scripts for model setup

Fig. 4.21 shows complicated script hierarchy for the AWG toolbox I developed. The first step is to specify the wavelength domain information such as central wavelength, each individual BPM simulation wavelength as well as AWG channel spacing. Once wavelength information is obtained, a file that runs mode solver is called to start calculating effective index and propagation constants of nitride waveguide modes for all wavelength samples. In this example, 1.55 μm central wavelength (Lamda0) and 1.6 nm AWG channel spacing (DLambda) is targeted.

Then AWG is treated as a 2.5D model for BPM TE simulation and user dictates the simulation domain as BPM zone. For AWG simulation, the basic configuration is to simulate input and output start couples by BPM and the arrayed waveguides are analytically calculated for phase adjustment as shown in Fig.4.22. for BPM zone 0 covers the entire input star coupler and some portions of arrayed waveguides. Here all mode overlap monitors are tilted to be orthogonal to the arrayed waveguides meanwhile they maintain the same distance to the input of star coupler. The monitor captured phase plus the arrayed waveguide phases are passed to BPM zone 1 for output coupler BPM simulation.

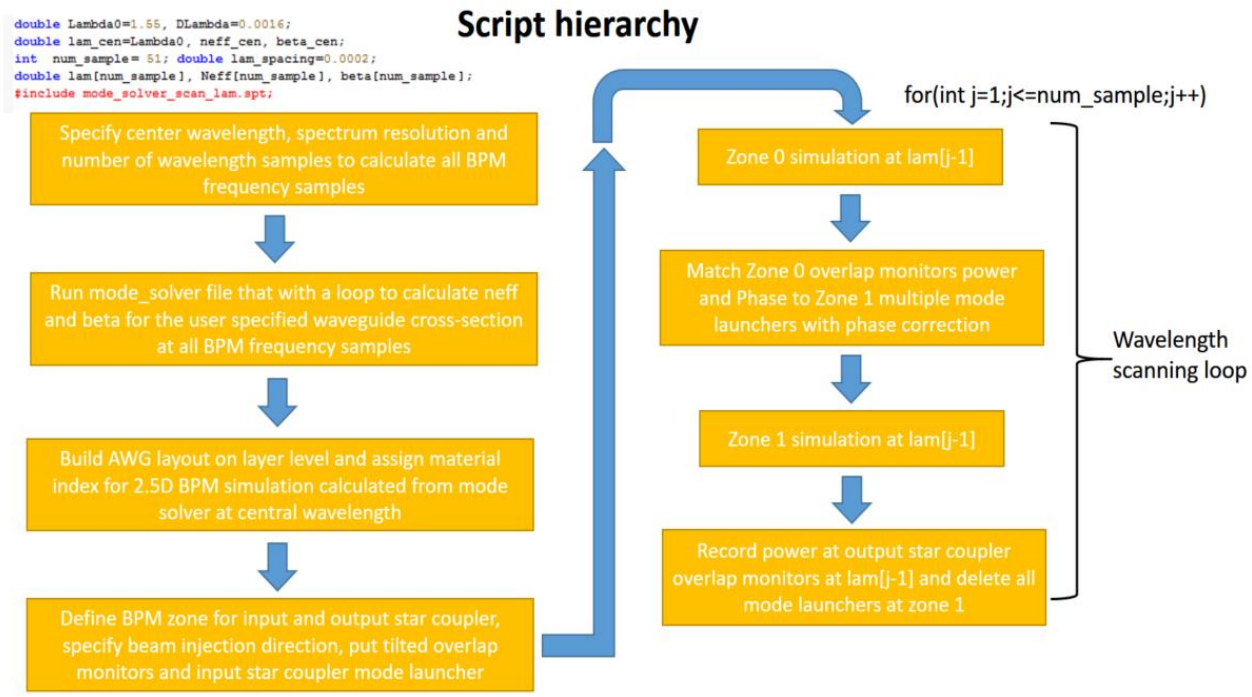


Figure 4.21 AWG toolbox script hierarchy (totally ~ 500 lines code)

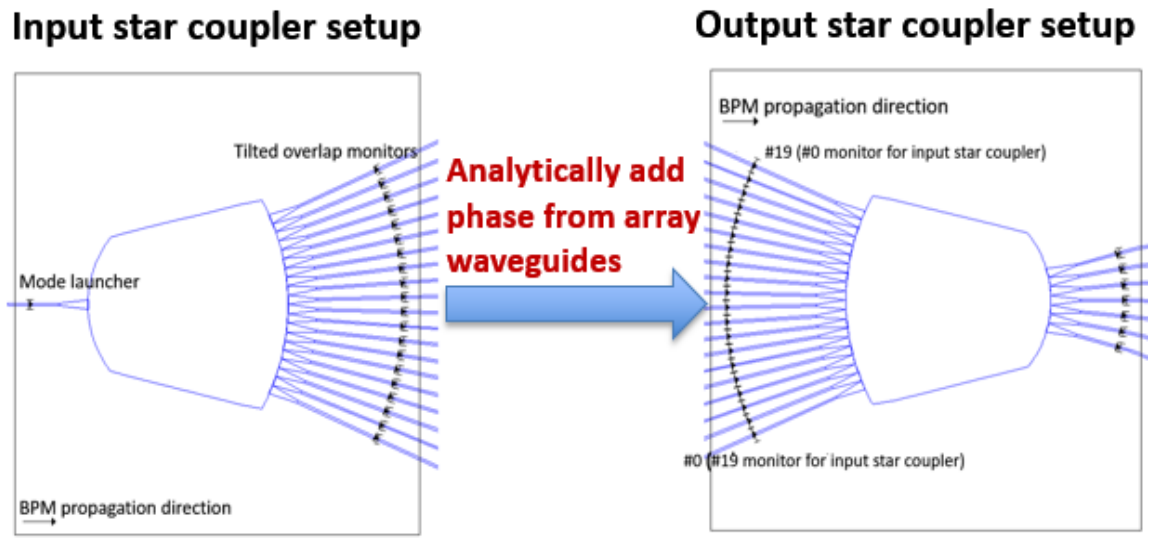


Figure 4.22 Basic simulation setup and illustration

Phase setup however can be rather complicated since both arrayed waveguide phase change and phase error need to be considered. The phase is first calculated as propagation constants multiplied

by arrayed waveguide length (between monitors at BPM zone 0 and sources at BPM zone 1) then angle converted within 360-degree range. Then the BPM/analytic hybrid simulation is first excited at central wavelength, where output beam is not steered. BPM simulation at central wavelength should ideally be just the inverse process of input star coupler where a single beam is diverged among arrayed waveguides with uniform phase. Hence if that can be fully accomplished in BPM, at output star coupler mode launchers with according power distribution and uniform phase should also mainly focus at the center output port.

|E| distribution plots of both BPM zones are given in Fig.4.23, where input star couple behave nicely but field inside output star coupler is chaotic. Theoretically at central wavelength all beams from arrayed waveguides should add up in phase at central output waveguide. However, there's a well-defined problem that even without beam steering, beams won't be able to merge in phase.

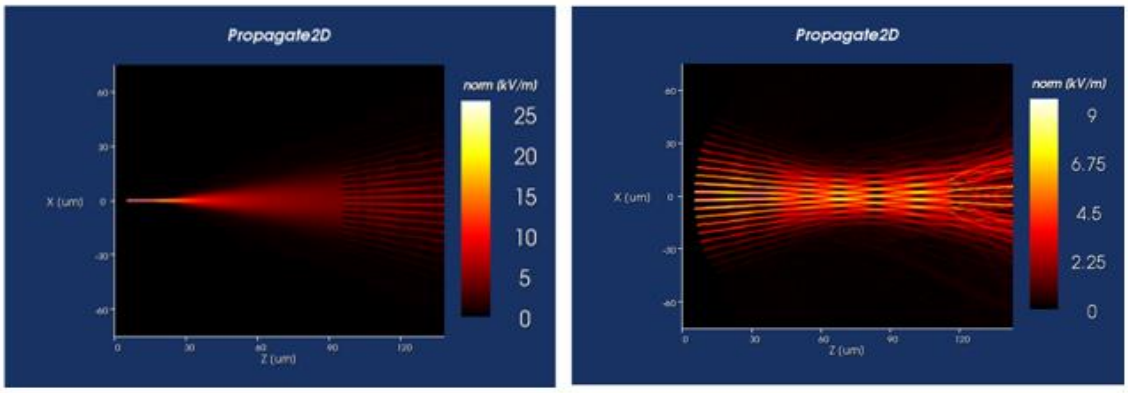


Figure 4.23 (a) Input star coupler |E| plot at central wavelength (b) Output star coupler |E| plot at central wavelength

To further analyze this simulation problem, monitor results in BPM zone 0 is investigated as shown in Fig.4.24. BPM simulation shows power follows like a Gaussian shape [108] after beam diverging in free space, which agree with convention. The phase plot however seems to show random but symmetric phase distribution among arrayed waveguides. This is a numerical error caused by BPM algorithm. Since BPM is a paraxial approximation [109], numerical accuracy of BPM simulation decreases with increasing beam divergence angle. Even with high Pade order [110] to compensate, BPM still cannot behave like FDTD to give omni-directional simulation. That means even at central wavelength beams where phase front is flat (in phase), they would not

be able to merge in phase anyway. Hence that inaccuracy is reflected on the phase error among arrayed waveguides, yet due to horizontal symmetry of the device a random but symmetric phase distribution is obtained.

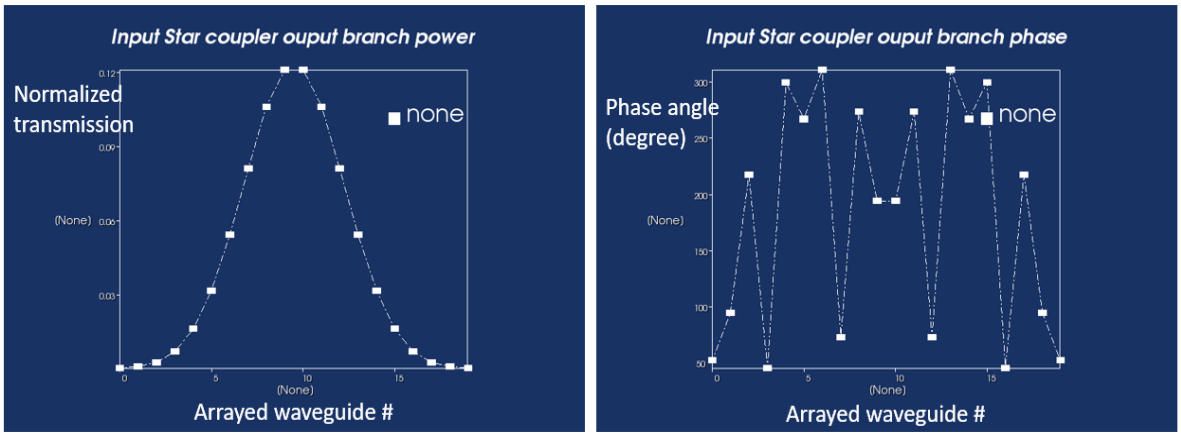


Figure 4.24 Input star coupler output power and phase among arrayed waveguides

```
    for(int i=1;i<=M;i++)
    {
 //L_array[i-1]= L_start + (i-1)*Delta_L_array;
 Phase_array[i-1]=L_array[i-1]*(1e-6)*beta_temp;
 Phase_array_degree[i-1]=degree(Phase_array[i-1]);
 B1= Phase_array_degree[i-1]/360;
 Phase_array_Degree[i-1] = Phase_array_degree[i-1]- B1*360;
    }

ml::Straight( cin->Star_coupler_out0@"out"+(i-1): wfix(Wwg), Lwg);
var offset = ml::Offset( cin-> Star_coupler_out0@"out"+(i-1) : 0, 0, 180);
source_out[i-1]= ml::ModeLauncher( inp -> offset@cout :
/* Result Name = */ "simname",
/* Method = */ BPM,
/* Power [W] = */ outputA[M-i] ,
/* Phase [deg] = */ -phaseA[M-i]+ Phase_array_Degree[i-1],
/* Tilt [deg] = */ {0.0},
/* Mode-X = */ 0,
/* Range-X [um] = */ 5,
/* Mode-Y = */ 0,
/* Range-Y [um] = */ 5,,,,,,,
/* Pump = */ false,
/* Signal Number = */ 0);
}
```

Phase correction term

Figure 4.25 Phoenix Optodesigner scripts for phase setup and correction

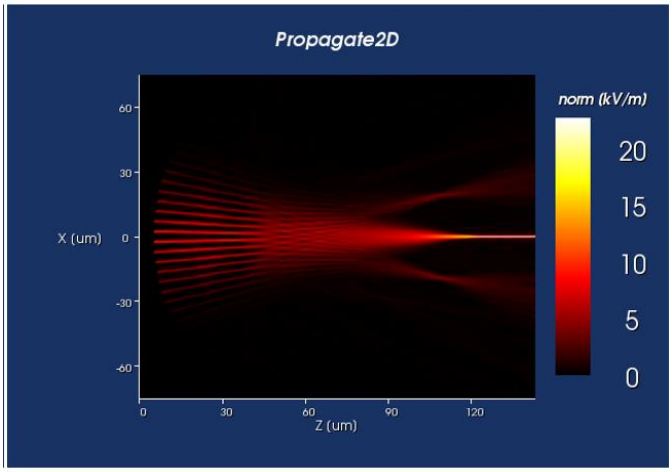


Figure 4.26 BPM zone 1 |E| plot at 1550 nm wavelength

For solve the BPM phase error problem, the phase error can be first predicted and then manually removed before running output star coupler simulation. Since both input and output star coupler share the same geometry of free propagation region, it can be anticipated that both star couplers incur the same phase error. Phase error at input star coupler can be calculated as phase front deviation from being in phase. Once the input star coupler BPM phase error is quantified, it automatically predicts the error at output star coupler hence phase error term will be included before BPM zone 1 simulation. Fig.4.25 shows the scripts to setup phases of mode launchers in BPM zone 1 and the phase error correction part.

With phase error treated at BPM zone 1, beam is mainly focus at central output port (#3) with 71% power transmission where two weaker focus points also appear as beam focus at ±1 times FSR. With correct simulation at central wavelength, then investigation at other individual wavelengths becomes the next. It is designed with 1.6 nm channel spacing, meaning at wavelength ± 1.6 nm from central wavelength, beam should focus at the output ports adjacent to central waveguide. Fig.4.27 shows the |E| plot at 1551.6 nm at 1548.4 nm wavelength respectively and beam indeed focus at output port #2 and #4 accordingly with power transmission reduced to 64%. Investigation at other wavelengths (± N × channel spacing) are also done but not displayed here. Results show higher the N value, lower power transmission can be obtained, which agrees with non-uniformity nature of AWG.

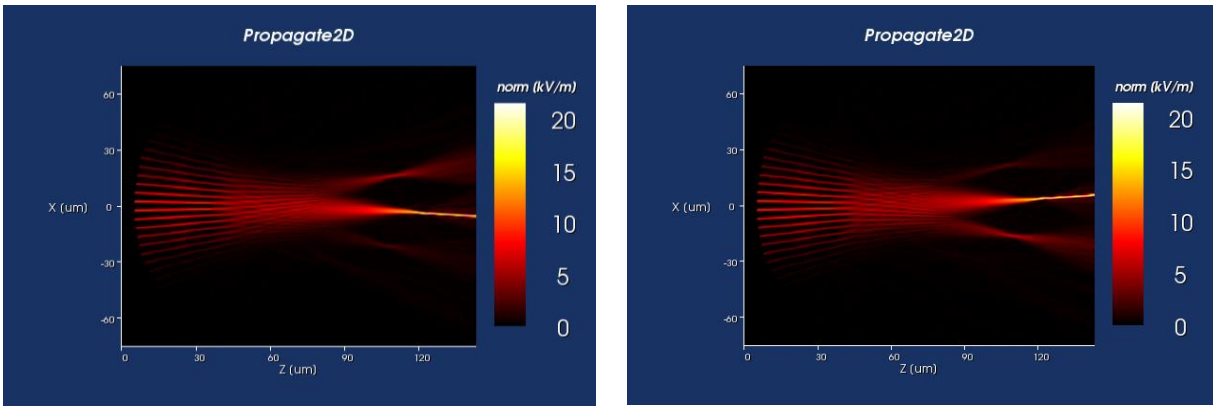


Figure 4.27 (a) |E| plot at central wavelength + 1×channel spacing (1.6 nm) (b) |E| plot at central wavelength - 1×channel spacing (1.6 nm)

With simulation at each individual wavelength correct, then the final important step is to package that single wavelength hybrid calculation scripts (BPM + analytic + BPM) into a wavelength scanning loop as shown in script hierarchy. Since phase error is predicted at BPM zone 0 which determines the phase at BPM zone 1, mode launcher at BPM zone 1 must be updated at each wavelength sample. Therefore, after each single wavelength calculation, output power is recorded among all 7 output ports then mode launchers and monitors are deleted for initialization. If not deleted after each simulation run, multiple mode launchers can be stacked over multiple runs which is incorrect. With everything setup, simulation over multiple wavelength is done which gives transmission spectrum for designed AWG as shown in Fig.4.28.

Calculated AWG spectrum looks almost correct, expect for the insufficient FSR which causes channel collision. Insufficient FSR is caused by too large grating order (~ 120) where normally speaking grating order > 80 can start to cause FSR problem. However, this is discovered after Phoenix evaluation, which makes it impossible to further modify this in-house AWG toolbox. It's suggested by technical supports from Photon Design Inc. that smaller grating order can change the dispersion and different output port spacing will be required. Existing result however still shows correct central wavelength (1550 nm), channel spacing (1.6 nm), proper non-uniform channel transmission shape as well as -40 dB crosstalk which is a typical value.

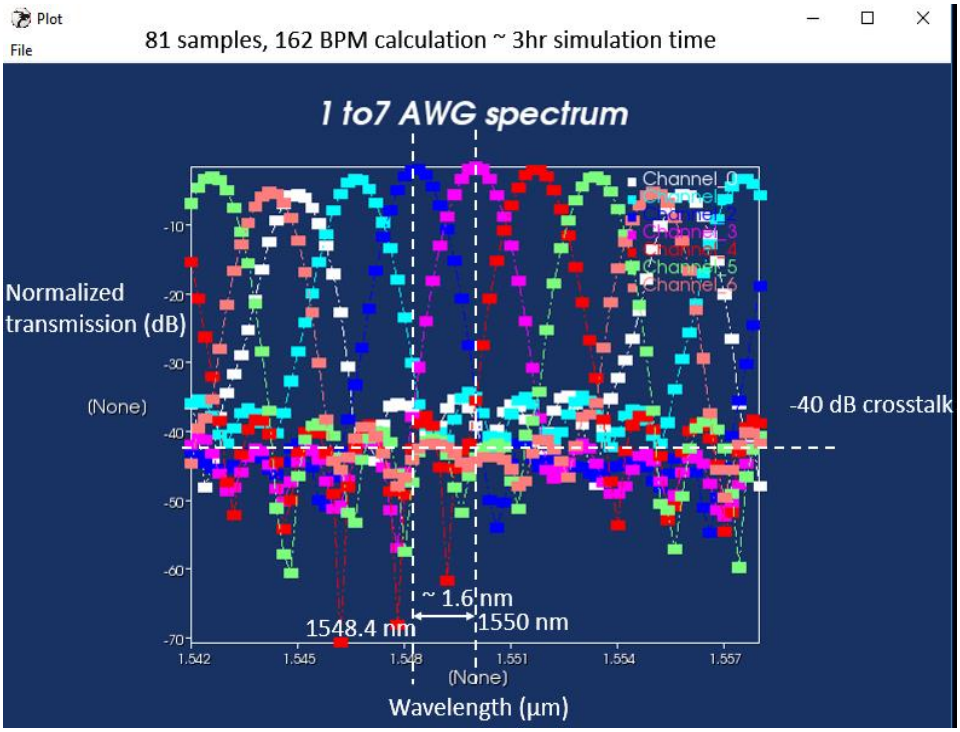


Figure 4.28 Calculated 1-to-7 AWG power transmission spectrum

```
double discretization_unit = 0.001 ;
int WG = mask::AddLayer("WG",LD(37,0),RGB(255,128,168),true,true);
mask::CScreate("cs0",filter,RGB(0,0,255),true,0);
mask::AddGrid(WG, discretization_unit);
mask::CSadd(matEffWaveguide());
cs::background(matEffBackground() );
```

From layer to GDS, the structure needs to be discretized

Set layer index to n_slab for 2.5D BPM and background index also setup
Setting index is for BPM simulation purpose (rather than layout export)

... create geometry

```
string maskfilename = "C:/temp/PhoeniX/mask/"; //where to save the gds files?
string cellname     = "AWG 1to7"; //GDS-II cellname
int exported_layer [1] = {WG};

// Menu: Mask / Mask Export / GDS-II (Stream format)
   mask::gdsii(maskfilename+"AWG.gds", exported_layer ,cellname);  // export the design into GDS-II file
```

Here we only export one layer that we defined with AWG structure on

Figure 4.29 Scripts for GDS layout export

Ultimately the AWG layout is exported from Phoenix as GDS by scripts. AWG structure plotted in Phoenix is just a layer with assigned refractive index. For GDS export, first step is to discretize the entire layout and 1 nm discretization grid size is used here according to Fig.4.29. Then file name and cell name are specified by user and exported_layer [1] ={WG} command exports only one layer of our designed layout (layer name is WG). If a layout includes several layers,

exported_layer [1,2,3] = {WG , WG2, WG3} command shall be used assuming layer 2 and layer 3 are named as WG2 and WG3.

Fig.4.30 (a) gives the exported AWG layout and it can be used to build up complicated layout that contains several AWG. Our group indeed try a fabrication but fabricated pattern shows strong overexposure at star coupler region, as shown in Fig. 4.30 (b). Probably Ebeam is not a good tool for writing bulky region where secondary electrons can accumulate exposure more easily. One possible solution is to use optical lithography at CMOS foundry since Purdue machine at not handle sub-micron accuracy. Nonetheless, for CMOS compatible nitride fabrication, nitride thickness will be restricted down to 300 nm, which cannot be used for polarization independent AWG (thick nitride required). As our group is waiting for Phoenix license purchase, the AWG project would proceed upon the software license arrival and further effort for AWG fabrication shall be done by our group.

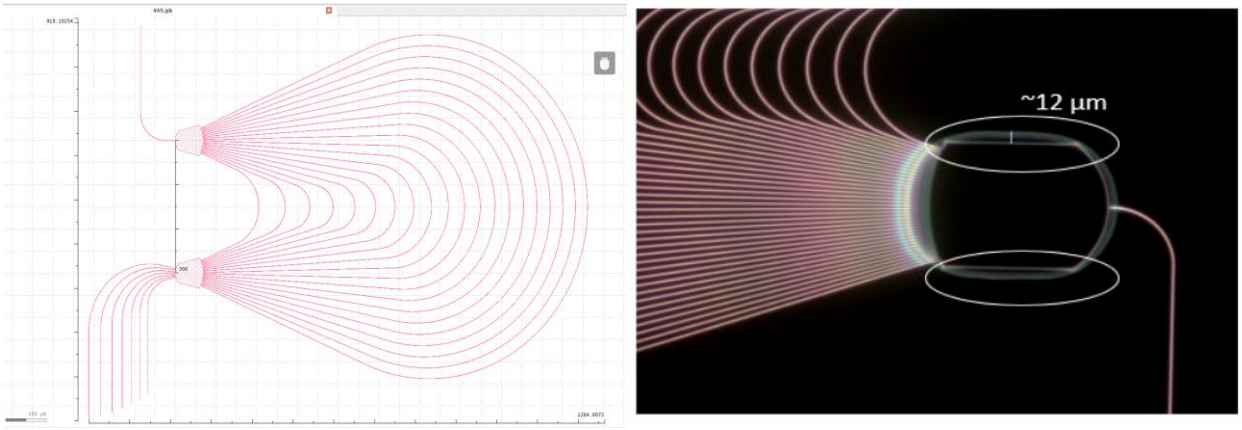


Figure 4.30 (a) Exported GDS file used for cleanroom fabrication (b) dark field microscope image of pattern after RIE etch and strip-off HSQ (courtesy of Mr. Yun Jo Lee)

In summary, an AWG tool box is developed by Phoenix Optodesigner during software evaluation period. Design challenges such as phase error and channel collision are encountered and solutions are proposed. Although not perfect, my designed AWG toolbox can generate AWG structure and simulate the spectrum for performance evaluation. The layout exported is fabricated in university cleanroom but seems severe fabrication problem is still unresolved. Upon software license arrival, more in-depth theoretical investigation as well as fabrication effort shall be invested.

CHAPTER 5. CHIP-SCALE LIDAR EMITTER BASED ON OPTICAL PHASE ARRAY

5.1 Introduction

Optical phase array (OPA) has been a active research direction over recent years, aiming to offer chip-scale solution for LiDAR emitter. Although alternative solutions based on mirror, MEMS and mechanical moving parts are also attractive options, only OPA can offer chip-scale emitter to reduce size, price and increase steering speed.

OPA is an array of identical optical antennas where antennas are emitting identical optical powers with calibrated phase. Fig.5.1 (a) shows illustrate the principle of 1D OPA where antenna arrays are emitting at linearly tilted phase front. Spacing between antennas dictates the beam steering efficiency and far field pattern. Fig.5.1(b) shows the far field pattern in Mr. Poulton's thesis [111] under various antenna spacings (pitches). The rule of thumb is pitch less than half wavelength is required to suppress high order grating sidelobes. Grating sidelobe is detrimental for OPA due to two reasons. First and foremost, optical beam output power will be equally distributed among the main lobe and all high order sidelobes. However only single lobe (usually main lobe) power is utilized hence most of optical power get wasted. In addition, the ultimate beam steering angle cannot go beyond the angle between two first order sidelobes, meaning beam steering angle is severely limited.

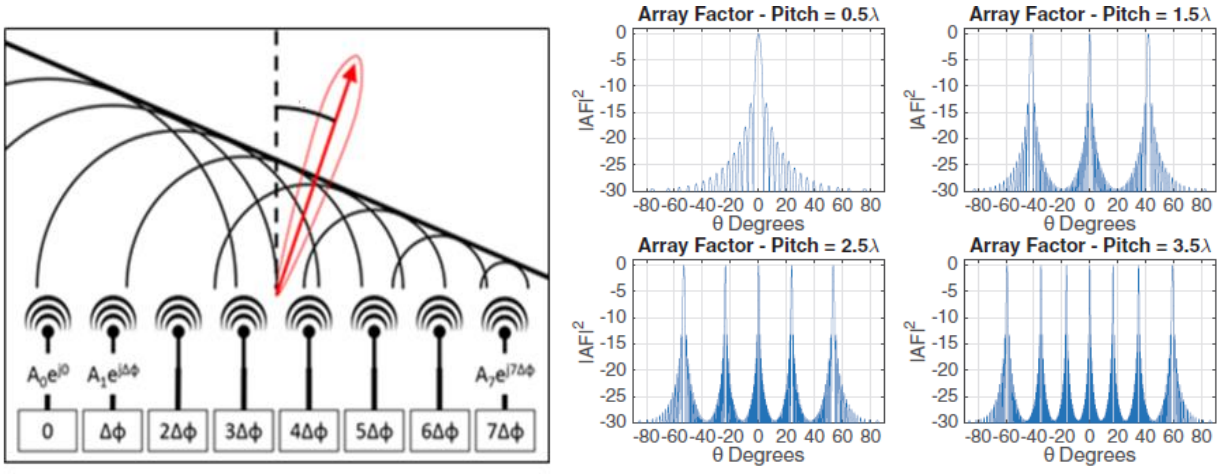


Figure 5.1 (a) Illustration of 1D OPA operation principle [112] (b) Far field optical field pattern of 1D OPA under various pitches [111]

In order to steer beam in two dimensions, 2D OPA is intuitively needed. Fig.5.1.2 show the passive 2D OPA reported by MIT's group where compact antennas are deployed in a 2D array. The problem of such configuration is the grating emitter footprint limits the channel spacing (pitch), inevitably leading to high order grating sidelobes on both dimensions [113]. In addition, to rapidly control phase of each individual antenna becomes tremendously difficult.

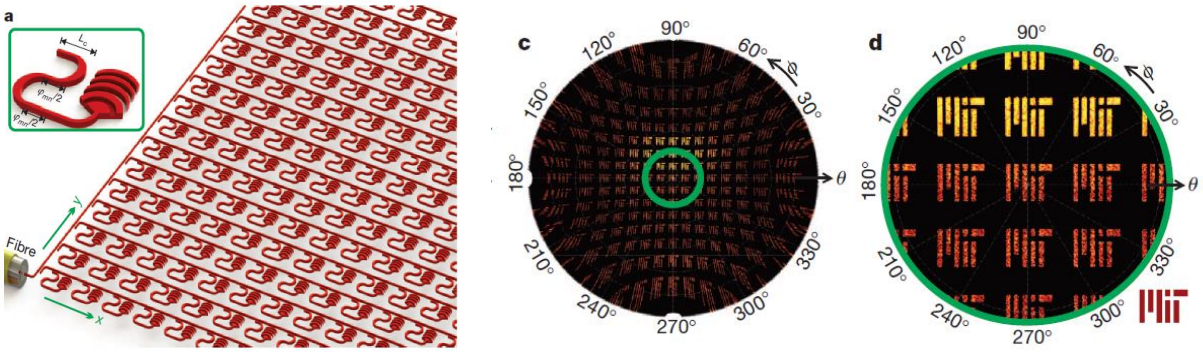


Figure 5.2 (a) Previously reported passive 2D OPA (b) Far field image of 2D OPA [113]

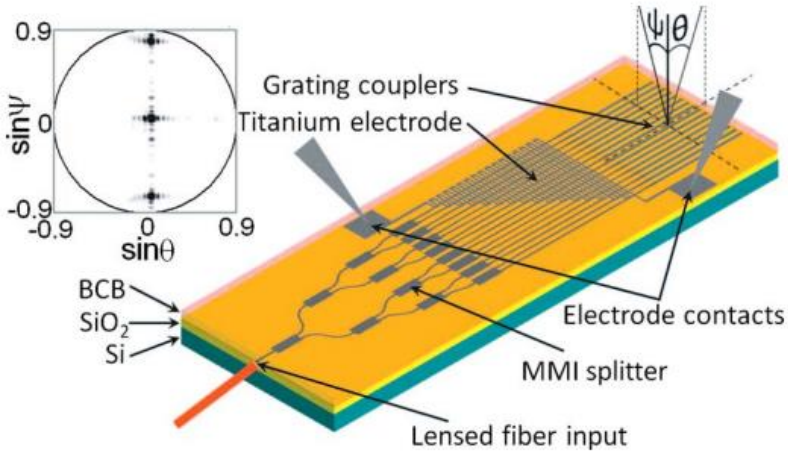


Figure 5.3 1D OPA with thermal phase tuning [114]

A more popular option is to deploy 1D grating array as shown in Fig.5.1.3 [114]. The input beam is equally divided (in-phase) and transmitted to multiple channels by cascaded 1-2 MMI binary tree. Then closely packed 1D grating arrays are deployed to gradually dissipate the optical power along propagation direction. The linearly tilted phase front can be implemented by suspend heaters on top of grating arrays such that length under thermal modulations are linearly increased (or

decreased). Such 1D OPA can only use phase front in one dimension. In terms of another dimension, wavelength tuning would offer small amount of beam steering. With thermal tuning, recently reported works can steer the beam at ~ 100 KHz speed.

While thermal tuning is efficient and compact, some researchers prefer electrical phase tuning due to its rapid tuning speed (~ GHz). Fig.5.4 shows professor John Bower's group work on a fully integrated LiDAR chip with electrical tuning [115]. Since electrical tuning is lossy, semiconductor optical amplifiers are deployed after phase modulator to compensate the optical loss.

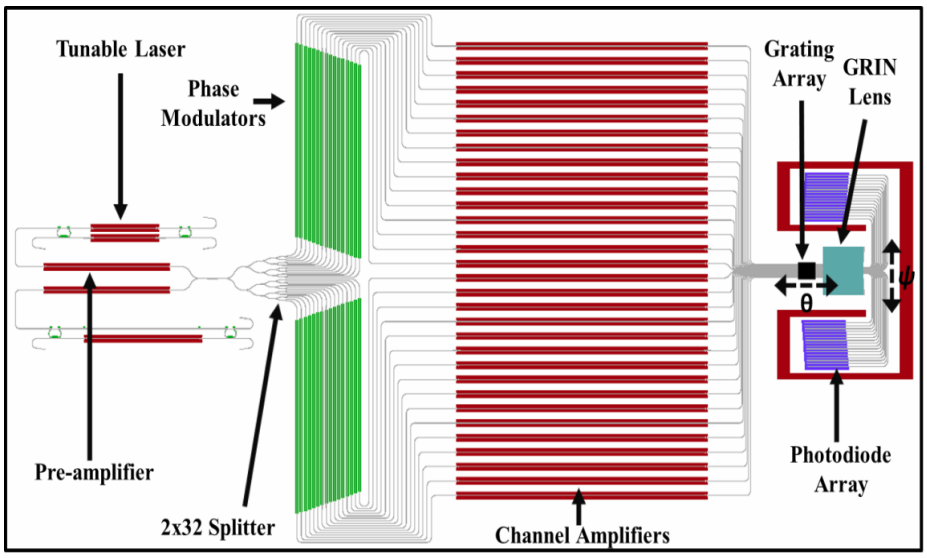


Figure 5.4 Fully integrated LiDAR chip with electrical tuning [115]

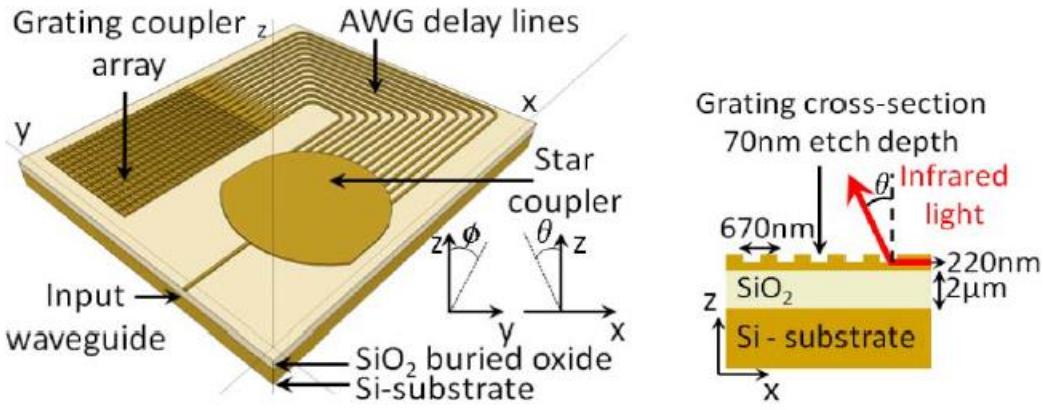


Figure 5.5 SOI 1D OPA driven by AWG [116]

Other fancy beam steering techniques have also been reported. Fig.5.5 shows a AWG driven 1D OPA [116] where the input wavelength dictates the linearly tilted phase front, which drives grating arrays to steer beam out of plane. It's worth mentioning that beam steering by wavelength tuning is not truly an attractive option for industry because tunable lasers are expensive and usually fast beam steering is difficult to achieve (limited by wavelength tuning speed).

5.2 Passive Silicon Nitride optical phase array for infrared wavelength

The OPA project starts with design and implementation of passive element. Our group's passive work aimed to reproduce professor Mike Watt's paper in 2017 [117] as shown in Fig.5.6, where a passive SiN OPA for visible wavelength is reported.

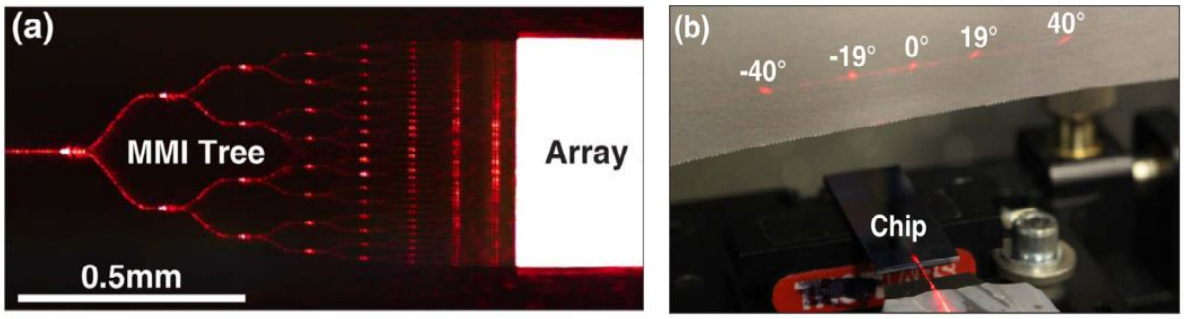


Figure 5.6 (a) Top view image of SiN OPA (b) Far field pattern of passive OPA [117]

The grating array is the most important passive element for design. As shown in Fig.5.6, a very short SiN grating is simulated where grating period is calculated to give around 5-degree emission angle based on 1st order grating assumption. Then gratings with various etch depths are simulated to estimate the propagation loss. From FDTD simulation (Fig.5.7), 100 nm etch depth would lead to about 20 dB propagation loss hence the it can be assumed safely that power is dissipated (emitted) enough to get utilized for far field generation.

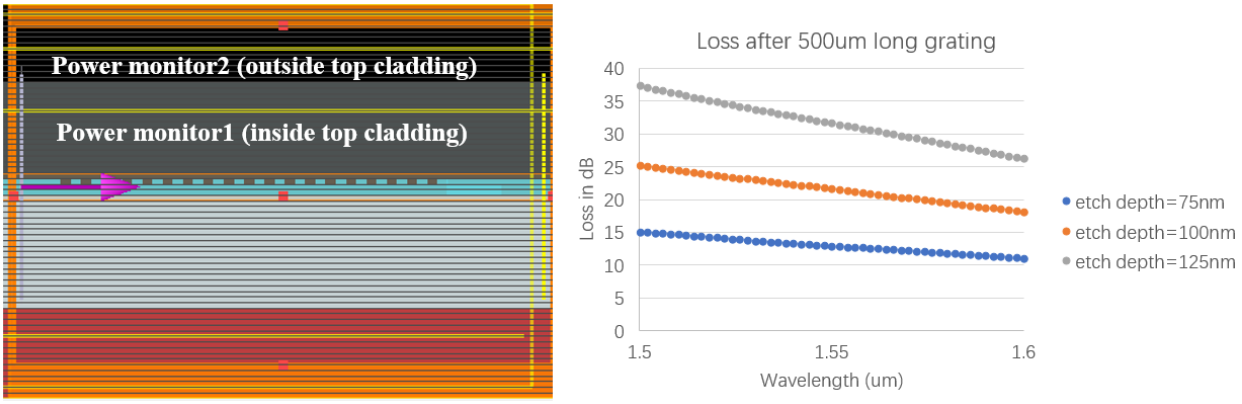


Figure 5.7 (a) Side view of FDTD simulation setup (b) Calculated propagation loss spectrum

Then to simulate the phase array, multiple identical gratings are deployed with user defined pitches. Fig.5.8 shows FDTD calculated far field pattern with all channels in phase. Simulation shows less high order sidelobes under smaller pitch. However due to relatively weak optical confinement of nitride waveguide, decent channel spacing must exists to prevent from evanescent coupling. Hence in the finalized layout, no pitch less than 3.5 um are used. In reality if much shorter gratings are used, smaller pitch may be acceptable due to weaker evanescent coupling. Nonetheless, large light emitting area is demanded to reduce far field spot divergence angle and thus with some tradeoff grating length around half millimeter is chosen.

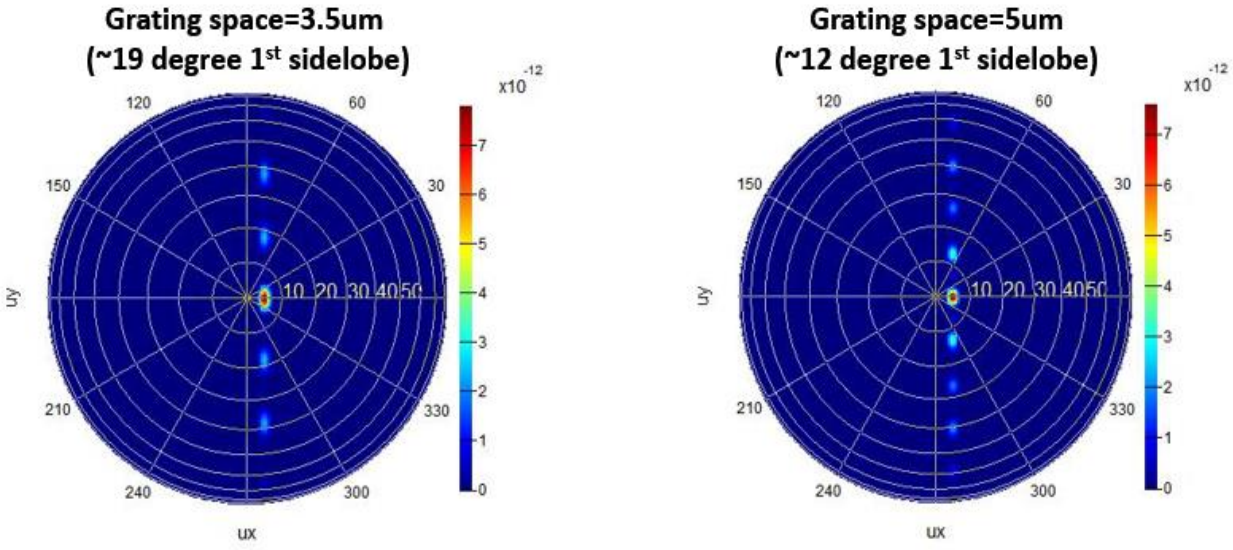


Figure 5.8 (a) Far field plot of 3.5um pitch OPA (b) Far field plot of 5um pitch OPA

Fig.5.9 illustrates an sample device on the finalized layout. U-grooves are deployed on both sides of edge coupler because high optical power is needed and U-grooves would help stabilize the fiber under high power. The input beam is initially split into 64 routes with MMI binary tree and after vertically etched grating arrays waveguides are tapered out to radiate residual power to avoid reflection. Only one channel after grating is routed to output edge coupler in order to measure the remaining power.

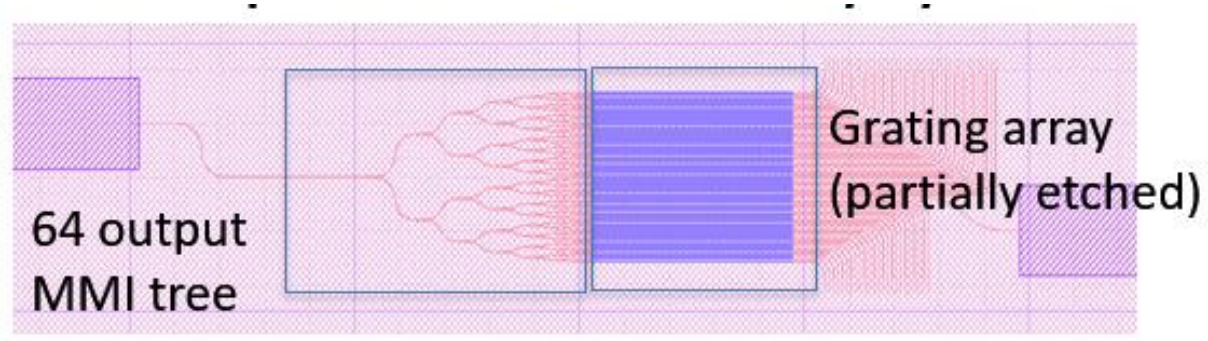


Figure 5.9 Sample OPA device (64 channels) on the GDS layout

Optical microscope image and SEM images are taken as shown in Fig.5.10. SEM image show that even at the last stage where waveguides are becoming close, Ebeam lithography over-exposure does not happen.

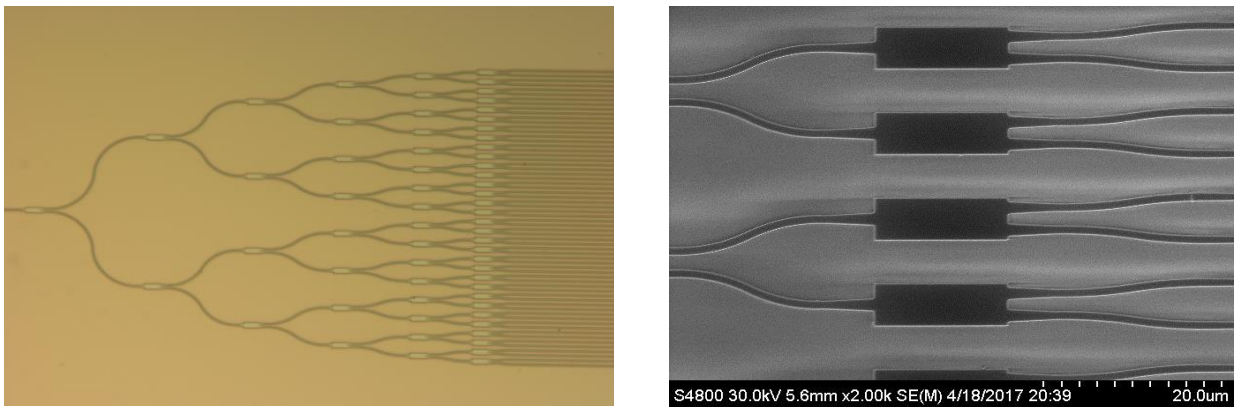


Figure 5.10 (a) Optical microscope image of a 64 channel MMI tree (b) SEM image of the last stage MMIs (courtesy of Dr. Kyunghun Han)

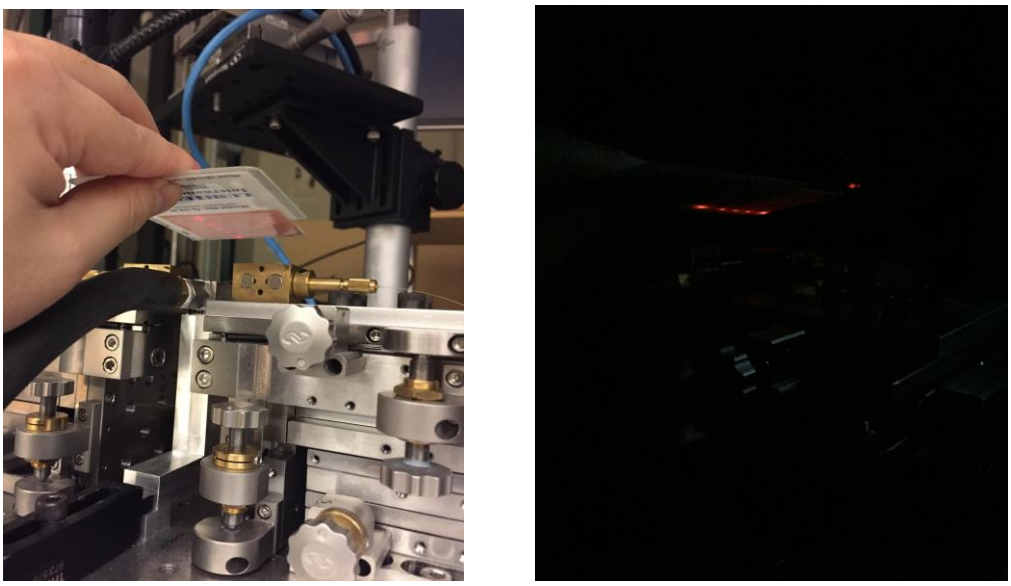


Figure 5.11 (a) Measurement setup (b) Far field pattern on IR card

The measurement setup is shown in Fig.5.11 where power is coupled from lensed fiber into the chip through edge coupling. With power maximized at output edge coupler, fiber alignment can be optimized and polarization is also adjusted to TE. To pump the input power up, EDFA is used to provide optical gain. With IR card deployed on top of chip, far field optical pattern can be captured when power transmission of single channel reaches about hundred mW level. The far field pattern agrees well with simulated pattern in Fig.5.8 (a). The clear far field sidelobe pattern indicates the all channels are in phase after MMI tree as expected.

5.3 Optical phase array design for high order grating sidelobe suppression

High order grating sidelobe is a fatal technical problem for OPA and this section explores the effect and potential solution for grating sidelobes. The most effective solution for grating sidelobe suppression is to reduce grating emitter spacing, which inevitably increase channel crosstalk due to evanescent coupling. In this section, SOI platform is used for numerical investigation for its tight confinement.

Here SOI OPA (~ 10 μm length) are simulated with various adjacent channel phase shift at 800 nm and 550 nm channel spacing (center-to-center). Lumerical FDTD calculates the far field projection as shown in Fig.5.3.1 where two configurations can obtain 80-degree and 100-degree

beam steering respectively under ± π phase shift. It's worth mentioning that when sidelobe angle is relatively large, far field pattern without sidelobes does not mean they are fully suppressed. Instead, sidelobes can be near or beneath the horizon such that additional phase shift is needed to steer the sidelobes into the far field plot.

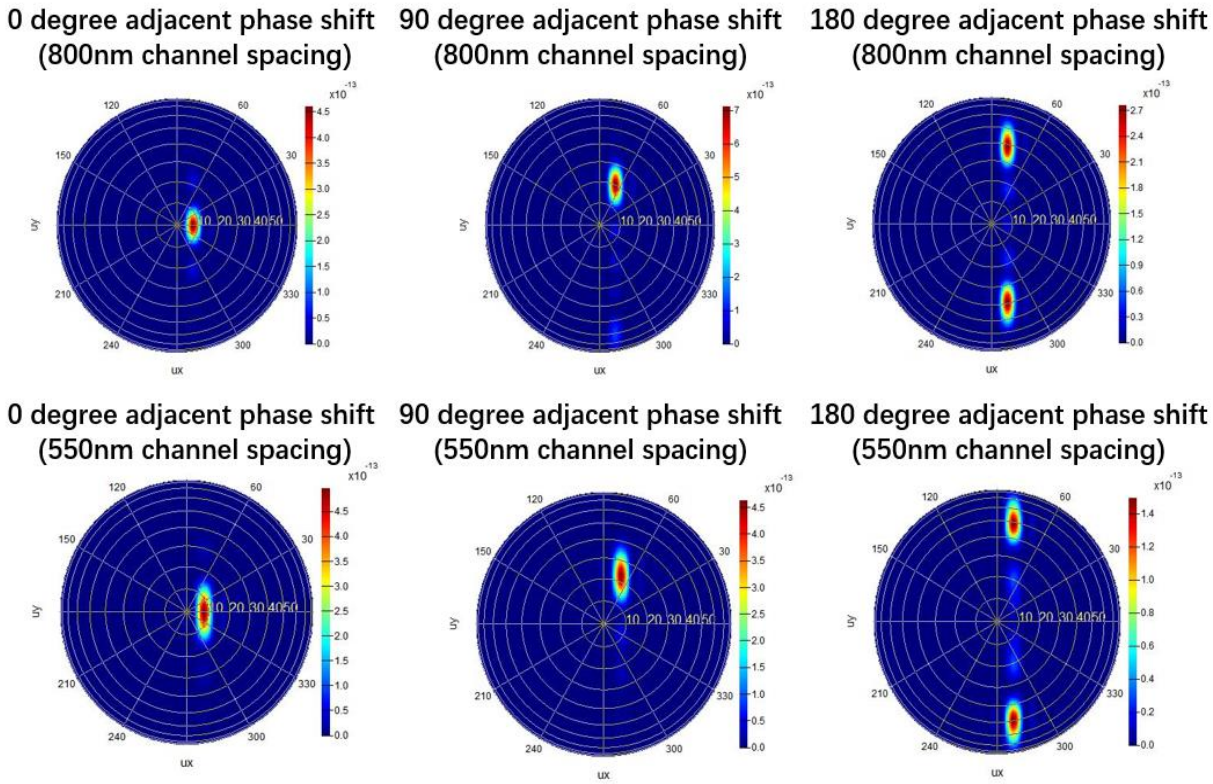


Figure 5.12 FDTD calculated far field distribution at 800 nm and 550 nm grating spacing respectively

Although clean far field projection can be obtained on short OPA, it does not mean a long OPA can also get clear far field image due to channel crosstalk. To investigate the negative impact of evanescent coupling, a much longer (~ 100 μm length) OPA under 750 nm grating spacing is simulated.

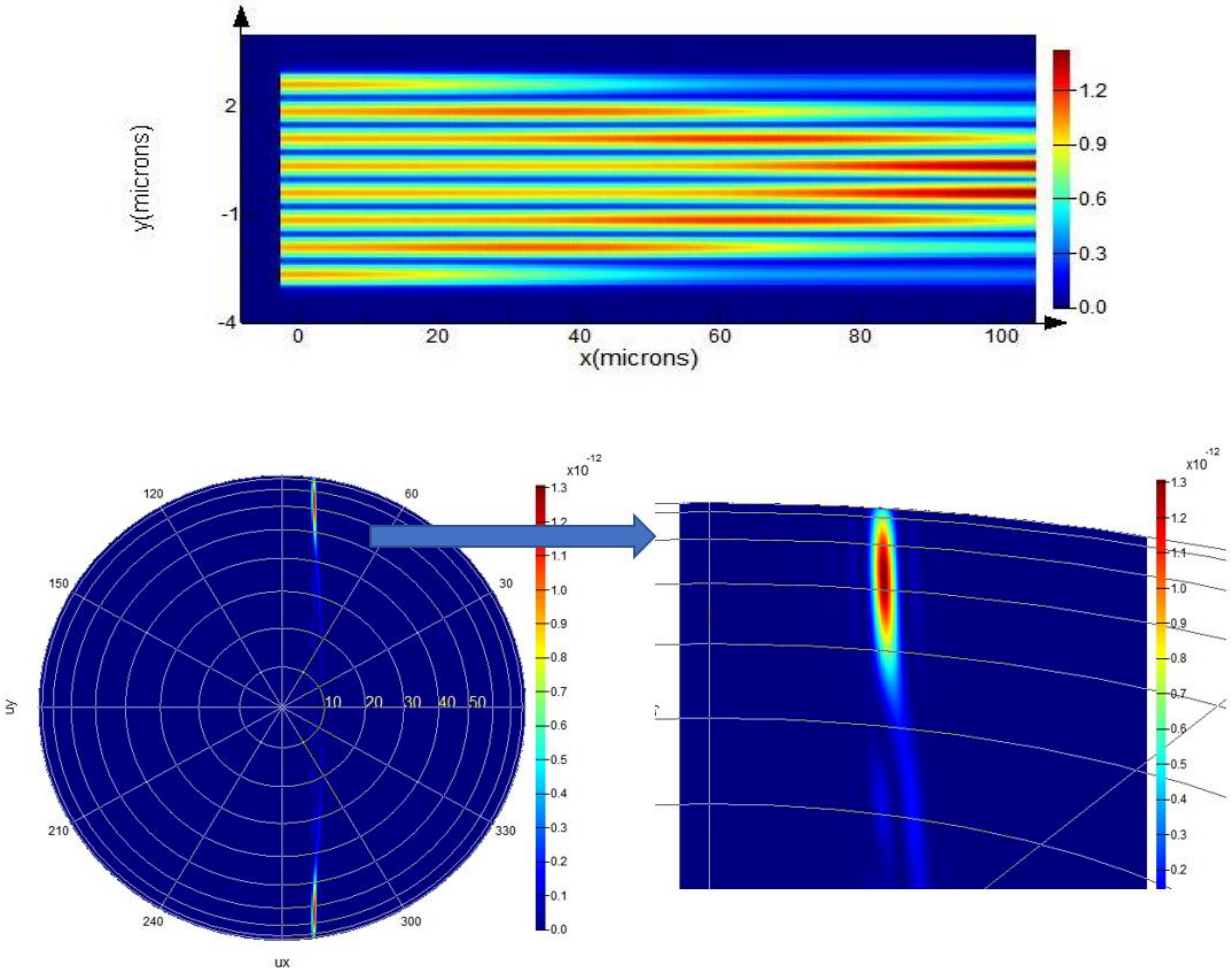


Figure 5.13 |E| distribution along a 100 μm long 16-channel OPA under 180-degree channel phase shift and its far field projection pattern

Fig.5.13 shows results of 8-channel OPA with 180-degree adjacent channel phase shift. Due to strong evanescent coupling, among 8 channels, clearly near field |E| plot shows non-uniform power distribution along the horizontal direction. Ideally the far-field pattern should show two spots with straight line of weak since component (such as two additional dimmer spots in the middle in Fig.5.12) should present. Far field is illustrated in Fig.5.13 is quite different from Fig.5.12. The spot has become very narrow in Ux dimension because much longer grating is simulated hence spot size (divergence angle) in longitudinal direction is squeezed down.

Here crosstalk power twisted far field pattern along the Ux direction such that spot size beginw to deviate from sinc function shape. This negative impact will become even more significant if OPA with higher number of channels are used, which amplify the channel crosstalk. Fig.5.14 shows the

16-channel OPA with the same length and simulation shows even the main spot no longer follow the correct shape. Usually OPA chip requires grating length on the order of millimeters and large number of channels (> 64) is desired to reduce spot divergence angle. Based on analysis of channel crosstalk and its impact on far-field pattern, half pitch channel spacing is simply unrealistic.

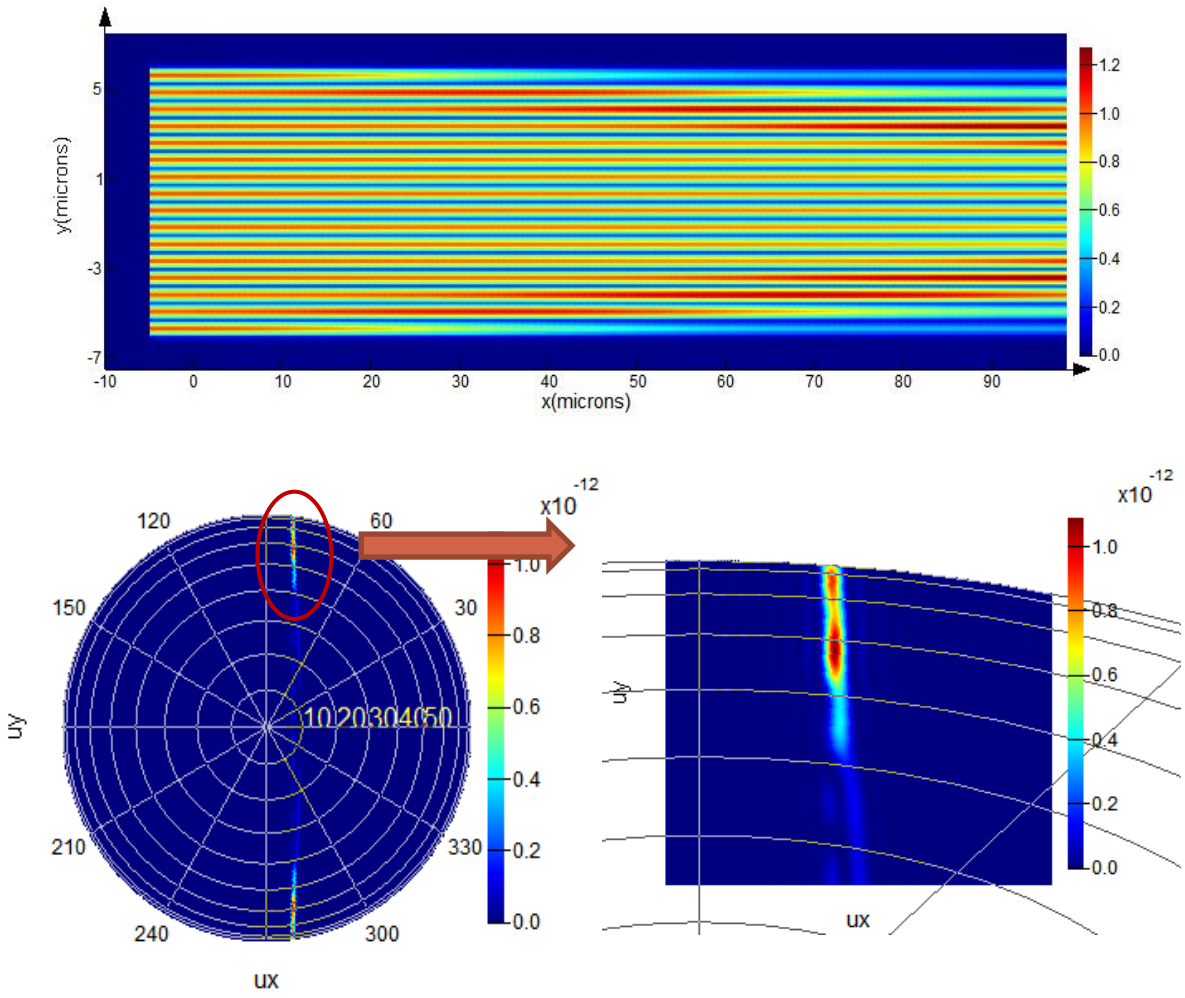


Figure 5.14 |E| distribution along a 100 μm long 16-channel OPA under 180-degree channel phase shift and its far field projection pattern

To reduce evanescent coupling without sacrificing grating spacing is a quite challenging task for OPA design. Here one theoretical solution based on skin-depth engineered waveguide [118]. Extreme skin-depth (Eskid) waveguide has recently been reported for crosstalk suppression on SOI platform and Fig.5.15 shows its geometry. Eskid waveguide uses periodic all-dielectric

cladding to strongly confine the evanescent field [118]. Based on such principle, Eskid waveguide can potentially help reducing channel crosstalk due to evanescent coupling, which may lead to high order sidelobe suppression.

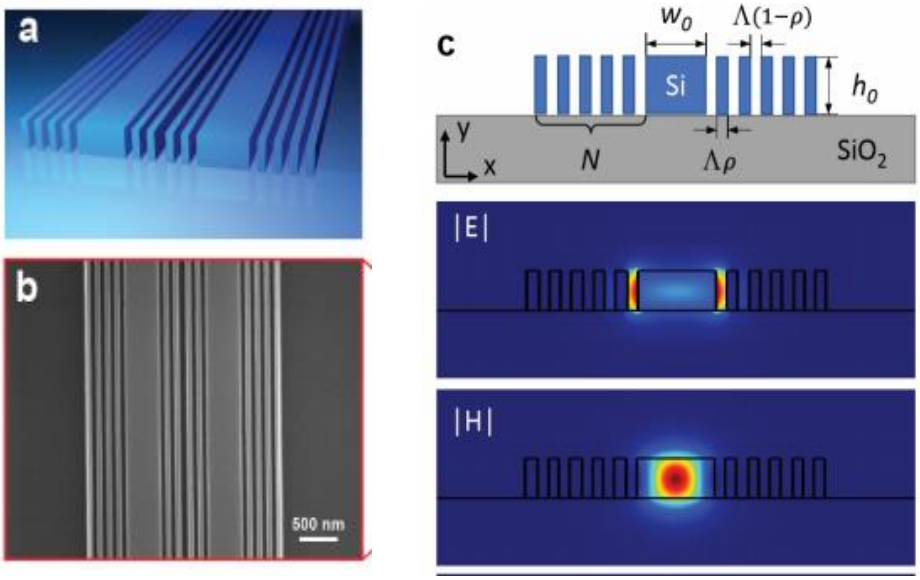


Figure 5.15 Geometry and field distribution of extreme skin-depth (Eskid) waveguide [118]

EME simulation is initially used for SOI waveguides with 750 nm grating spacing. Fig.5.16 simulates three parallel grating with the central one excited. In the simulation setup only one grating period is included but Lumerical EME engine can override cell periodicity to dictates the number of periods on each cell. For example, Fig.5.16 shows 10 grating period calculation by overriding period of cell no. 3 by 10.

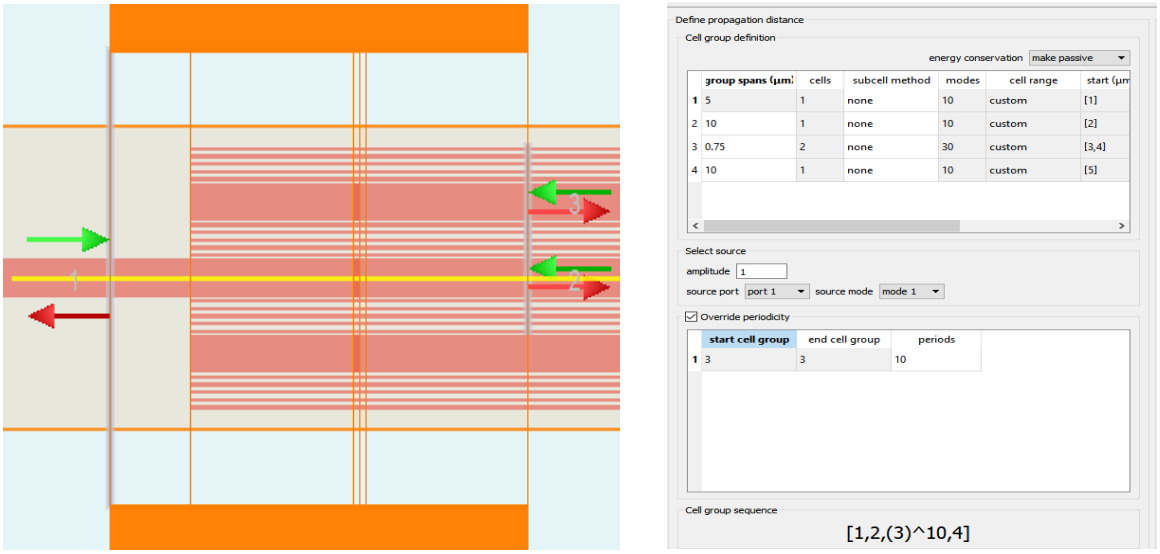


Figure 5.16 EME simulation setup

With this approach, grating of any length can be calculated to give power remaining in the top, central or bottom channel. Power in the central channel is expected to gradually get radiated by grating but meanwhile some power will also couple to its top and bottom neighbors. The crosstalk power however will also radiate along the grating hence there's certain grating length that crosstalk power reaches the peak. With Eskid waveguides clearly crosstalk is suppressed such that even the maximum crosstalk is below 2%, indicating effective crosstalk suppression.

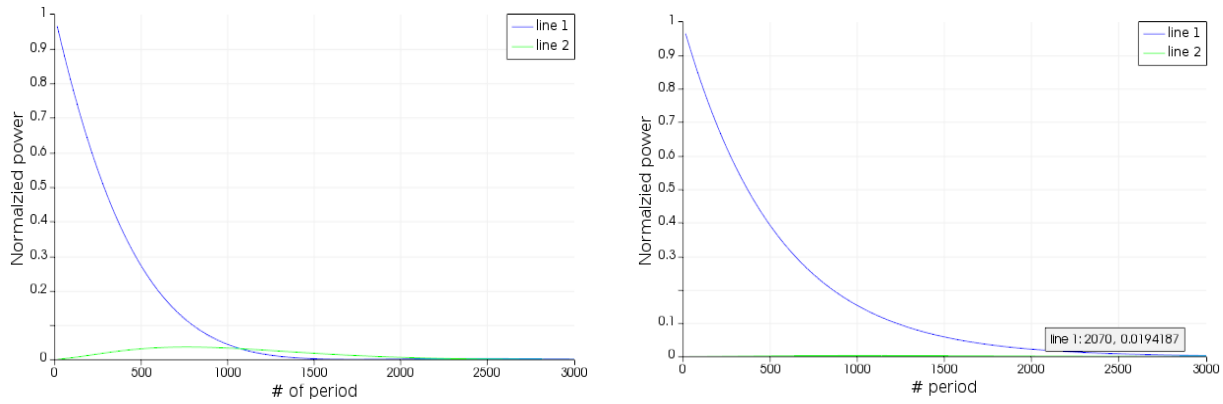


Figure 5.17 Transmitted power (line 1) and crosstalk power (line 2) along (a) normal waveguides (b) Eskid waveguides at 1550 nm wavelength

EME can only predict how one or more fixed input mode is coupled to different output modes. Nonetheless for realistic OPA applications where all ports are excited together with arbitrary phase relationship, FDTD must be used which can also generate far field projection plot.

Eskid simulation with massive footprint however, becomes quite unstable due to strong field discontinuity. Here a 60 μm long 8-channel OPA based on Eskid waveguide is simulated as shown in Fig.5.18. Here Eskid waveguide is designed to have 25 nm pitch, 50% duty cycle multilayer stacked Si/SiO2. Theoretically air cladded Eskid waveguide offers even better crosstalk suppression due to strong high index contrast. However, since SiO_2 top cladding can help amplify the beam steering angle hence air cladding option is used. |E| top view shows up to 60 μm long grating, power nonuniformity using Eskid is much less than without Eskid (Fig.5.13).

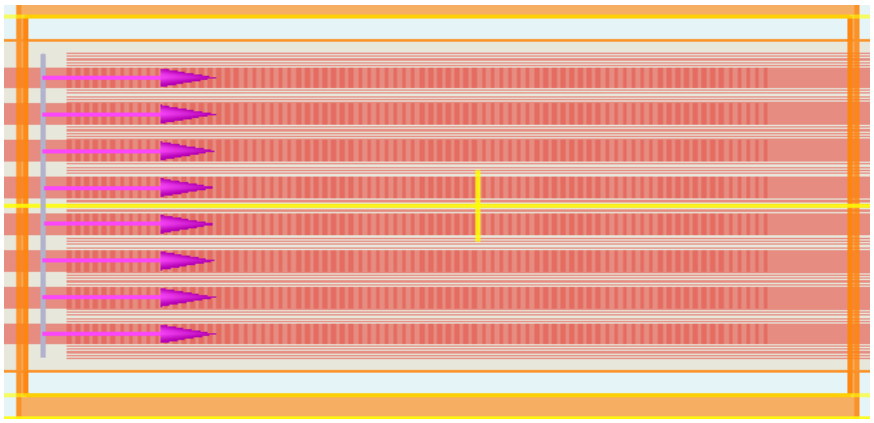


Figure 5.18 FDTD simulation setup for 8-channel 1D OPA with 180-degree adjacent channel phase shift

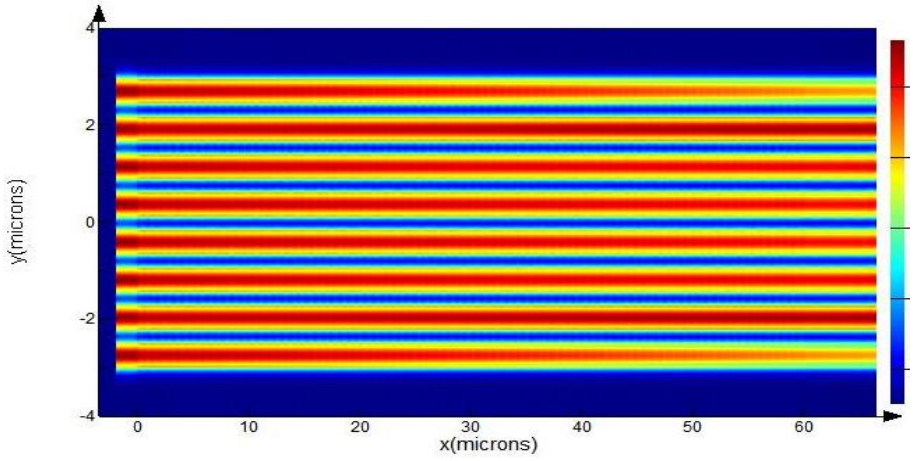


Figure 5.19 Near field FDTD |E| plot

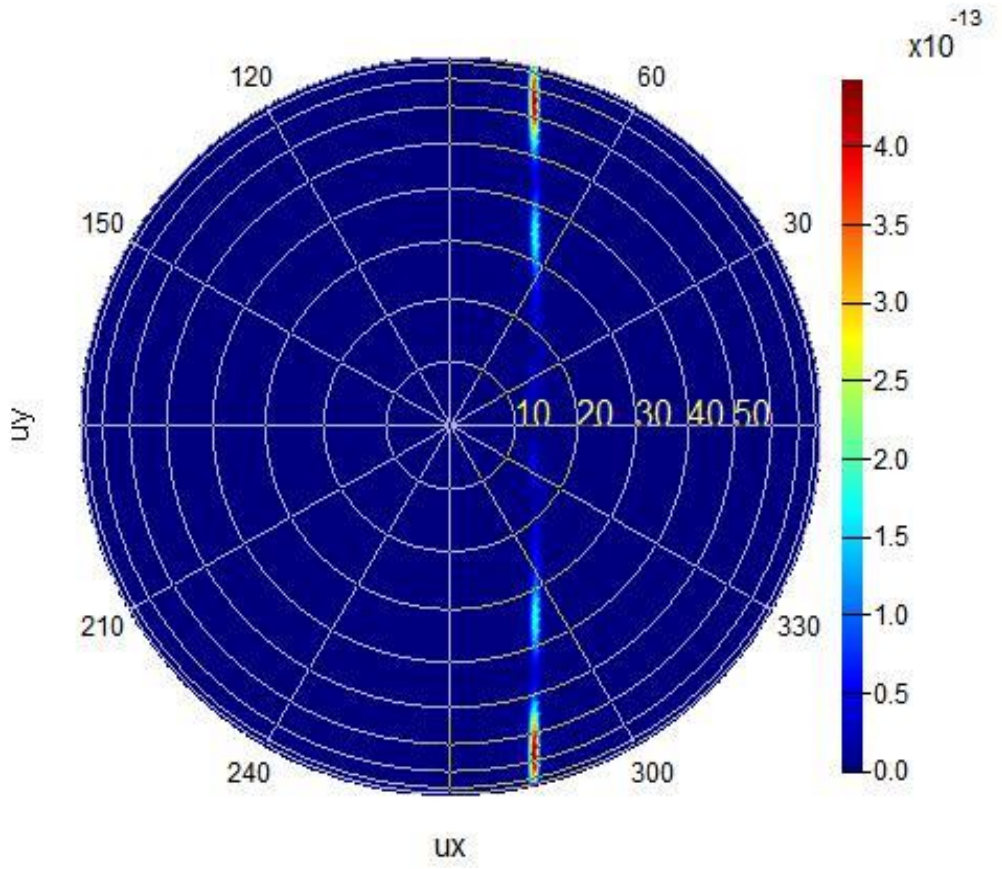


Figure 5.20 Far field projection pattern of 60 μm long 8-channel OPA with 180-degree phase shift

Far field pattern shows quite consistent results comparing to Fig.5.12, where crosstalk is almost negligible. However, for larger number of channels or longer gratings, it's still unclear if Eskid can completely solve the problem. Still simulation indicates Eskid can help alleviate the crosstalk caused by evanescent coupling hence maintain good far field pattern.

CHAPTER 6. SUMMARY AND FUTURE WORKS

The thesis shows mainly the design and characterization of optical fiber-to-chip edge couplers and on-chip mode division multiplexed devices. Conventional multiplexing topics based on polarization and wavelength is also numerically explored in this work. Eventually integrated optical phase array is investigated, with emphasis on passive design of grating arrays.

In the edge coupler projects, effect of sidewall roughness on edge coupler efficiency is discovered. Edge coupler based on meta-material subwavelength structure has also been heavily investigated. Our ultimate design "meta-trident" edge coupler shows 1.76 - 2.85 dB/facet loss (0.5 dB/facet due loss to fiber cleavage and 0.8 dB TM loss due to leakage) for high NA fiber input and 0.56 - 0.88 dB/facet loss for lensed fiber input. Numerically solution for standard SMF28 fiber is also proposed on a Si/SiN hybrid platform. Upon competition of the project, two patent applications are filed with exclusive license granted to Futurewei Technologies Inc.

On-chip MDM has been deeply explored both numerically and experimentally. An edge coupling solution is numerically proposed for dual mode multiplexing at both polarizations. Essential components for on-chip MDM including mode filter, sharp bend, mode converter are also designed and experimentally validated. A dual mode 3 dB splitter solution is also numerically proposed, offering its unique advantages. Specially on-chip MDM devices under multiple concurrent input are evaluated, where various theoretical solutions are proposed to reduce performance sensitivity to relative phase shift between multiple modes. In the near future, we plan to proceed with another fabrication run to validate the phase insensitive performance of proposed devices, including bend, splitter, and filter. Currently journal manuscripts based on mode filter, mode converter based on inverse design and sharp bend are also in preparation. Since most researchers failed to realize the phase sensitivity problem under multiple input concurrently, there is even a plan to submit a manuscript based on impact of phase sensitivity and its potential solutions.

Novel polarization handling devices (PBS and PSR) are also proposed with improved extinction ratio. A toolbox is also developed for AWG, including layout generation and numerical simulation. LiDAR emitter based on OPA has also been numerically and experimentally investigated. Upon arrival of Phoenix software license, we may try to work on AWG driven OPA in the future, exploring beam steering based on wavelength scan. It's also planned to continue working on Eskid

OPA in the simulation part to explore its extreme numerical performance. If impressive simulation results can be obtained, our group may try to proceed with fabrication and testing of Eskid OPA. Upon competition of my PhD. Degree, I will be joining Imec USA Nanoelectronics Design Center in Florida as Photonics IC researcher. Imec newly established fabless design center is actively working on terahertz imaging, millimeter wave imaging and optical phase array projects. The author is expected to work in Imec's photonics team to work on those research projects.

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VITA

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Journal

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Patent Applications

[1] “Optical Coupler”, **M. Teng**, M. Qi, B. Niu, S. Kim, K. Han, Y. Xuan, Y. Lee (patent filed, 2017 September, licensed by FutureWei Technologies, Inc)

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