8-2018

III-V and 2D Devices: from MOSFETs to Steep-Slope Transistors

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III-V AND 2D DEVICES: FROM MOSFETS TO STEEP-SLOPE TRANSISTORS

A Dissertation

Submitted to the Faculty

of

Purdue University

by

Mengwei Si

In Partial Fulfillment of the

Requirements for the Degree

of

Doctor of Philosophy

August 2018

Purdue University

West Lafayette, Indiana

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To my parents and my wife

ACKNOWLEDGMENTS

I would first like to thank my advisor, Professor Peide Ye, for his support, encouragement and guidance during my PhD study at Purdue University. In particular, I appreciate that he taught me to understand something that I'll remember for my whole life. That is to spend all the efforts to focus on the most important thing.

I would also like to give my great appreciation to my committee members: Professor Mark Lundstrom, Professor Joerg Appenzeller and Professor Zhihong Chen for their insightful suggestions and discussions during my PhD study.

My thanks also go to all my colleagues in Professor Ye's group. They provide innovative discussions and overcome technical obstacles. In particular, I would like to many thanks to Dr. Jiangjiang Gu, for his training and guidance when I was a first year PhD student. In addition, I would also like to thank Dr. Lin Dong, Dr Han Liu, Dr. Adam T. Neal, Dr. Heng Wu, Dr. Jingyun Zhang, Dr. Xuefei Li, Nathan Conrad, Dr. Hong Zhou, Dr. Yuchen Du, Dr. Linming Yang, Dr. Yexin Deng, Sami Alghamdi, Gang Qiu, Wonil Chung and Jinhyun Noh for their help in the past years.

I would also like to thank to all my collaborators, Prof. Roy G. Gordon, Dr. Xinwei Wang, Dr. Xiabing Lou from Harvard University, Prof. Muhammad A. Alam and Dr. Sanghoon Shin from Purdue University, Dr. Chun-Jung Su from National Nano Device Laboratories of Taiwan and Dr. Chunsheng Jiang from Tsinghua University.

Thanks to Birck Nanotechnology Center and all the staffs, Bill Rowe, Kenny Schwartz, Dave Lubelski, Jeremiah Shepard, Dan Hosler, Lorraine Fox, Geoff Gardner, John Coy and Ira Young for their technical support on cleanroom facilities and Mary Jo, Nancy Black and other clerical staffs for their helps.

And thanks to my parents for their continuous support.

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SYMBOLS

m	mass
v	velocity
f	frequency
k, k_B	Boltzmann constant
q	elementary charge
T	temperature
Q	charge
A	area
V_{DD}	supply voltage
V_{GS}	gate-to-source voltage
V_{DS}	drain-to-source voltage
V_S	source voltage
V_D	drain voltage
V_G	gate voltage
V_T	threshold voltage
V_c	coercive voltage
t	time
C_L	load capacitance
C_{ox}	oxide capacitance
C_D	depletion capacitance
C_S	semiconductor capacitance
C_{GB}	gate to top barrier capacitance
C_{SB}	source to top barrier capacitance
C_{DB}	drain to top barrier capacitance

C_{FE}	capacitance of ferroelectric insulator
C_{fr}	fringe capacitance
C_{it}	interface trap capacitance
D_{it}	interface trap density
ϵ_{ox}	oxide permitivity
I_{ON}	on-current
I_{OFF}	off-current
I_{DS}	drain-to-source current
I_D	drain current
I_S	source current
μ	mobility
W	channel width
W_{Fin}	fin width
W_{NW}	nanowire width
T_{NW}	nanowire thickness
T_{ch}	channel thickness
T_{ox}	oxide thickness
t_{FE}	ferroelectric insulator thickness
L_{NW}	nanowire length
L, L_{ch}	channel length
L_{mask}	mask length
P	power
P_D	dynamic power
P_S	static power
P_r	remnant polarization
N_T	number of transistors per unit area
N	number of carriers
E_G	bandgap
E_c	coercive field

E_F	fermi level
E_C	conduction band energy level
E_V	valence band energy level
g_m	transconductance
g_D	drain conductance
R_{SD}	S/D series resistance
R_S	source series resistance
R_D	drain series resistance
R_C	contact resistance
R_{sh}	sheet resistance
Φ_S	surface potential
S_{I_S}	source current power spectral density
S_{Vg}	input gate noise
τ_c	capture time constant
τ_e	emission time constant

ABBREVIATIONS

FET	field-effect transistor
MOSFET	metal-oxide-semiconductor field-effect transistor
MOSHEMT	metal-oxide-semiconductor high-electron-mobility transistor
CMOS	complementary metal-oxide-semiconductor
CPU	central process unit
C-V	capacitance voltage
I-V	current voltage
ALU	arithmetic logic unit
IC	integrated circuit
GND	ground
SOI	semiconductor on insulator
2D	2-dimensional
3D	3-dimensional
SCE	short channel effect
CNL	charge neutral level
TNL	trap neutral level
EOT	equivalent oxide thickness
GAA	gate-all-around
TFET	tunneling field-effect transistor
NC-FET	negative-capacitance FET
MEMS	microelectromechanical system
TMD	transition metal dichalcogenide
BTBT	band-to-band tunneling
SS	subthreshold slope

TMA	trimethylaluminum
S/D	source and drain
n+	highly n-doped
p+	highly p-doped
MBE	molecular beam epitaxy
ALD	atomic layer deposition
RTA	rapid thermal annealing
DIBL	drain induced barrier lowering
WN	tungsten nitride
FGA	forming gas anneal
TEM	transmission electron microscope
STD	standard deviation
LFN	low frequency noise
RTN	random telegraph noise
FDSOI	fully depleted SOI
PSD	power spectral density
PBTI	positive bias temperature instability
HCI	hot carrier injection
SOG	spin on glass
NDR	negative differential resistance
BP	black phosphorus
P-E	polarization-electric field
P-V	polarization-voltage
FE	ferroelectric
AFE	anti-ferroelectric
LK	Landau-Khalatnikov
MIM	metal-insulator-metal
HZO	hafnium zirconium oxide
XRD	X-ray diffraction

JL	junctionless
IMG	internal metal gate
EDS	energy dispersive X-ray spectrometry

ABSTRACT

Si, Mengwei PhD, Purdue University, August 2018. III-V and 2D Devices: from MOSFETs to Steep-Slope Transistors. Major Professor: Peide D. Ye.

With silicon CMOS technology approaching the scaling limit, alternating channel materials and novel device structures have been extensively studied and attracted a lot of attention in solid-state device research. In this dissertation, solid-state electron devices for post-Si CMOS applications are explored including both new materials such as III-V and 2D materials and new device structures such as tunneling field-effect transistors and negative capacitance field-effect transistors. Multiple critical challenges in applying such new materials and new device structures are addressed and the key achievements in this dissertation are summarized as follows: 1) Development of fabrication process technology for ultra-scaled planar and 3D InGaAs MOSFETs. 2) Interface passivation by forming gas anneal on InGaAs gate-all-around MOSFETs. 3) Characterization methods for ultra-scaled MOSFETs, including a correction to subthreshold method and low frequency noise characterization in short channel devices. 4) Development of short channel InGaAs planar and 3D gate-all-around tunneling field-effect transistors. 5) Negative capacitance field-effect transistors with hysteresis-free and bi-directional sub-thermionic subthreshold slope and the integration with various channel materials such as InGaAs and MoS_2.

1. INTRODUCTION

1.1 Computer and Binary Logic

The digital revolution, known as the "Third Industrial Revolution", origins from the invention of modern computers. Modern computers are digital machines using binary logic with "1" and "0" only in the Boolean algebra. Computing machines with continuous values are the analog computers. They used machinery that represented continuous numeric quantities such as angle of shark rotation or electrical potential. However, digital computers have shown their superior over analogy ones in terms of robustness, complexity and speed.

Binary logic is the logic system used in modern digital computers, in which "1" represents by a electrical potential, usually a high supply voltage, and "0" represents by a different electrical potential, usually a ground potential. The formal theory of binary computing dates back to 18^{th} century, when G. W. Leibnitz invented the binary number system. The binary logic was proved by G. Boole to be a complete system that allows computational processes to be mathematically modeled [1].

There are three basic logic gates, NOR, AND and OR with logic "1" and logic "0" as inputs and outputs. All other logics can be obtained from these three simple logics. They are the building blocks of the arithmetic logic unit (ALU) of the central process unit (CPU). Mathematically, with the three basic logic gates, any complicated arithmetic process can be achieved. Therefore, to build up a computer system, a major task is to found physical states to represent the logic "0" and logic "1", and find the physical method to do all the three basic operations. The logic "0" and logic "1" can be different in different type of computers. For example, in the old mechanical computer, the position of an object or the angle of rotation can be used for different

logic levels. In more advanced computing concepts, electrons with quantized spin state, spin up and spin down can be used for logic levels, so-called spin transistors [2].

1.2 Charge Based Logic and High Performance Computing

In current silicon based complementary metal-oxide-semiconductor (CMOS) technology, the logic "1" and logic "0" are represented by a high voltage and a low voltage. The NOR, AND and OR operations are achieved through the proper connection of a set of metal-oxide-semiconductor field-effect transistors (MOSFETs). Traditionally, supply voltage (V_{DD}) is used as high voltage for logic "1" and ground (GND) is used as low voltage for logic "0". The pMOSFETs are used to drive the output voltage from GND to V_{DD} through current flow from V_{DD} to the output capacitor and the nMOSFETs are used to drive the output voltage from V_{DD} to GND through current flow from the output capacitor to GND. The time to complete this single logic operation can be estimated as

$$t = \frac{C_L V_{DD}}{I_{ON}} \tag{1.1}$$

where t is time consumed in a single logic operation, C_L is the load capacitance and I_{ON} is the drive current of the MOSFET. Therefore, the requirements for high performance MOSFETs are divided into three parts if the three items are independent of each other.

- small load capacitance C_L
- small supply V_{DD}
- large on-current I_{ON}

According to the square law of current-voltage characteristics of a MOSFET [3], explicitly

$$I_{DS} = \frac{W\mu C_{ox}}{L}[(V_{GS} - V_T)V_{DS} - V_{DS}^2] \qquad for \qquad V_{DS} < V_{GS} - V_T, \tag{1.2a}$$

and

$$I_{DS} = \frac{W\mu C_{ox}}{L}(V_{GS} - V_T)^2 \qquad for \qquad V_{DS} \geq V_{GS} - V_T \tag{1.2b}$$

where

$$C_{ox} = \frac{\epsilon_{ox}}{T_{ox}} \tag{1.2c}$$

and I_{DS} is drain-to-source current, W is channel width, L is channel length, μ is the mobility, V_{GS} is gate-to-source voltage , V_{DS} is drain-to-source voltage and V_T is threshold voltage. Meanwhile, I_{ON} is defined as I_{DS} at V_{GS}=V_{DS}=V_{DD}, which is given by

$$I_{ON} \sim \frac{W\mu C_{ox}}{L}V_{DD}^2. \tag{1.3}$$

Considering both eq. (1.1) and (1.3), we can get the conclusion that reducing V_{DD} is not a good idea as V_{DD} and I_{ON} are correlated. Therefore, the criteria for high speed integrated circuits (ICs) should be modified as following

- small load capacitance C_L
- large on current I_{ON}

As a result, by reducing L, I_{ON} becomes larger while C_L becomes smaller as part of C_L is the gate capacitance which is proportional to L. So the time per logic operation will be reduced so that the speed of the ICs can be improved. Therefore, for transistors and ICs, it is always said, *"Smaller is better"*.

1.3 The Moore's Law and Power-constraint Scaling

Then it comes to the famous "Moore's Law", which originated from 1965 by G. E. Moore, states that the number of transistors per unit area has doubled and will double approximately every 18 months. Moore observed and predicted the revolution of semiconductor industry which last even until the author writes this thesis at 2018. However, although transistor number per unit area keeps increasing and transistor

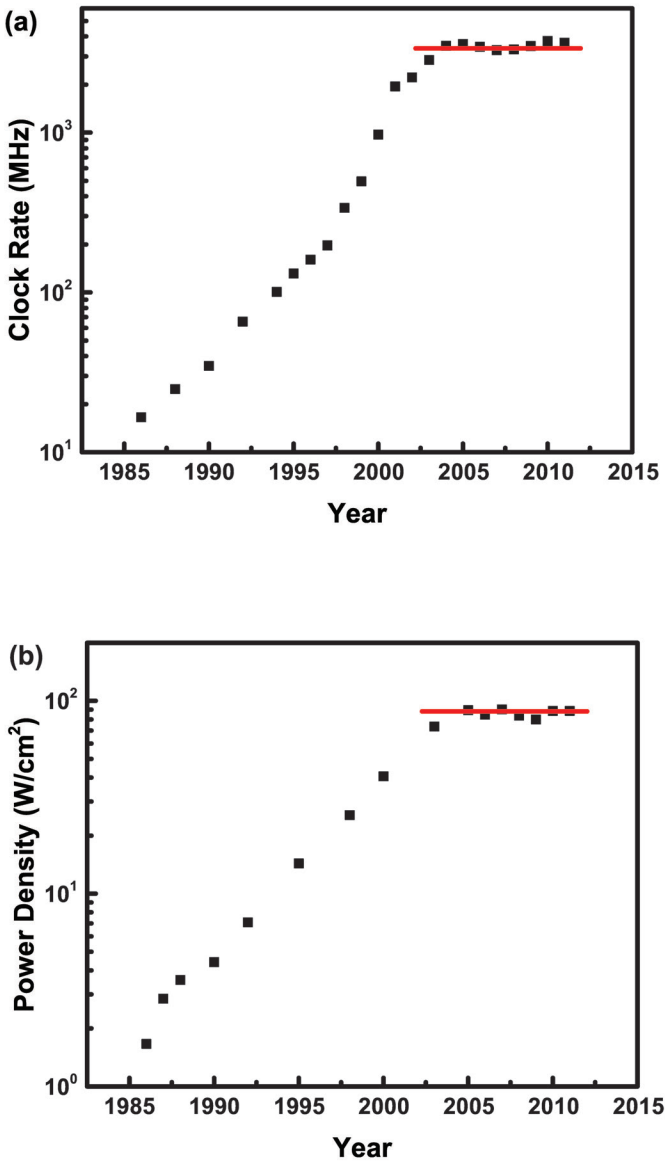

Fig. 1.1. (a) Clock rate of selected CPU versus year. (b) Power density of selected CPU versus year. Data source from Ref. [4].

size keeps shrinking, the power density of CPU saturates at $\sim 100\,\mathrm{W/cm^2}$ and clock rate saturates at $\sim 4\,\mathrm{GHz}$ since 2000 [4, 5], as shown in Fig. 1.1. It shows that the scaling down of CMOS technology is now limited by the power density, which lead to

too much heat generation to dissipate. The power density of an IC can be expressed as,

$$P = P_S + P_D \tag{1.4}$$

where P is power, P_S is static power when the circuits are in off-state and P_D is the dynamic power which represents the power consumption during a logic operation. The dynamic power is mainly due to the charging or discharging to the load capacitor when the logic level is changed. The static power is mainly caused by off-state leakage current, such as subthreshold current, junction leakage and tunneling leakage current. Here we assume subthreshold current dominate the off-current (I_{OFF}), which is the general case in ICs. The dynamic power and static power can be expressed approximately as

$$P_D \sim N_T C_L V_{DD}^2 f, \tag{1.5}$$

and

$$P_S \sim N_T I_{OFF} V_{DD} \tag{1.6}$$

where N_T is transistor density and f is the clock frequency or clock rate. If we reduced the size of the transistor by a factor of α ($\alpha < 1$) so that $L \to \alpha L$, $W \to \alpha W$, $T_{ox} \to \alpha T_{ox}$. Thus, $N_T \to \frac{1}{\alpha^2} N_T$ and $C_L \to \alpha C_L$ for a simple gate capacitor approximation. The actual C_L is larger than this approximation due to other parasitic effects. Therefore, if f and V_{DD} keep unchanged, the dynamic power density of the IC will increase by at least $1/\alpha$ and the static power of the IC will increase by $1/\alpha^2$, which will make the chip too hot to work. The clock frequency should not be reduced because reducing clock frequency means the reduction of CPU performance. Thus, the only way to keep the CMOS scaling trend is to reduce V_{DD}.

However, to reduce V_{DD} is not as simple as just reduce the supply voltage. Firstly, simply reduce V_{DD} without doing anything will result in I_{ON} reduction so that device performance will degrade, according to eq. (1.2b). Second, if I_{ON} is kept unchanged

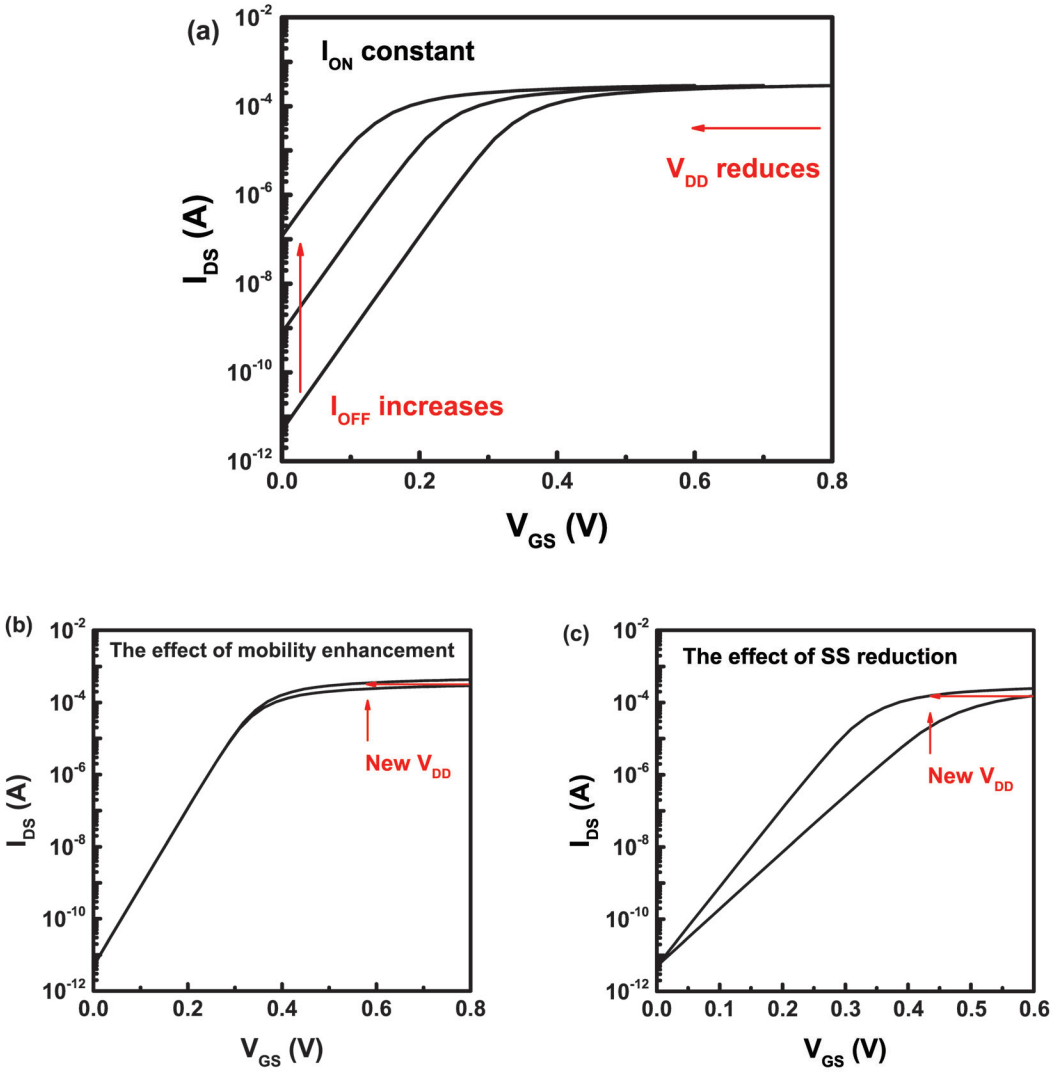

Fig. 1.2. (a) V_{DD} reduces while I_{ON} is kept the same in MOSFETs. (b) The effect of mobility enhancement at same I_{OFF}. (c) The effect of SS reduction at same I_{OFF}.

by engineering threshold voltage (V_T), I_{OFF} will increase so that P_S is increased, as shown in Fig. 1.2(a).

There are two ways to solve this problem. Both of them are hot research topics in electron device research currently. The one is to use high mobility material as

channel material so that I_{ON} will increase so that a lower V_{DD} can be applied, as shown in Fig. 1.2(b). No I_{OFF} increase will happen if V_T and subthreshold slope (SS) are the same. The other way is to reduce SS or use steep-slope transistors. SS reduction in traditional MOSFETs can be achieved using advanced 3-dimensional (3D) structure or thin-body semiconductor on insulator (SOI) structure in terms of short channel effects (SCEs) reduction but it has a thermionic limit of $\sim 60\,\mathrm{mV/dec}$ at room temperature. Steep-slope transistor are transistors with SS less than the thermionic limit of MOSFETs. As a result, steep-slope transistors can work at a lower V_{DD} comparing with MOSFETs without decrease of I_{ON} or increase of I_{OFF}, as shown in Fig. 1.2(c). Both MOSFETs with high mobility channel materials and steep-slope transistors will be discussed further in the following sections.

1.4 MOSFETs with High Moblity Channel Materials

Silicon has many unique advantages so that it is the channel material in semiconductor industry for logic applications in the past decades.

- Only homogeneous oxide, SiO_2, is formed during thermal oxidation while never happens on compound semiconductors or even on Ge.
- Low interface trap density (D_{it}) on SiO_2/Si interface.
- Suitable bandgap (E_G)
- Balanced mobility for both electrons and holes

However, silicon has little advantage in electron and hole mobilities over other high mobility III-V materials and Ge. Fig. 1.3 shows the electron and hole mobilities comparison among group IV and III-V semiconductor materials. The first thing to consider is that which material is the most suitable for transistors other than silicon. Here, the concept of fermi level pinning is introduced before the study of Ge and III-V materials. The fermi level pinning problem is mainly caused by the

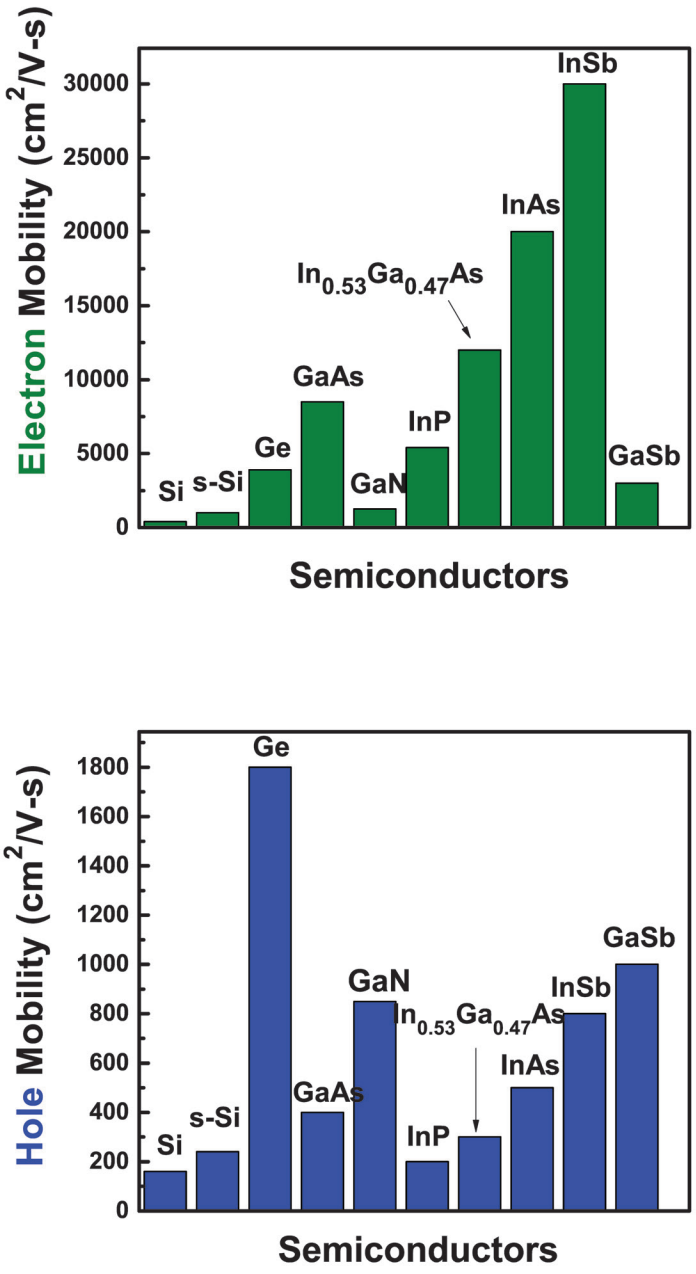

Fig. 1.3. (a) Electron and (b) hole mobilities comparison among group IV and III-V semiconductor materials.

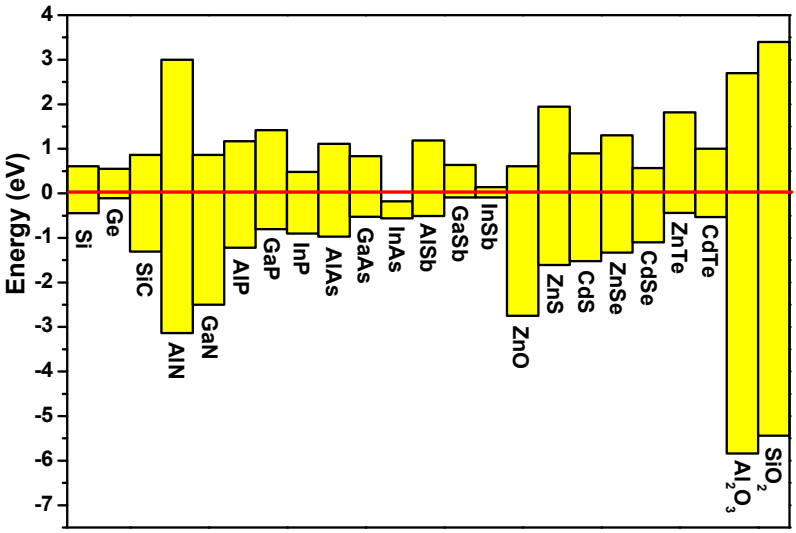

Fig. 1.4. Charge neutral level alignments over selected semiconductor materials.

interface traps such that fermi level (E_F) at the oxide/semiconductor interface are pinned to a certain energy level, as shown in the charge neutral level (CNL) alignments over selected semiconductor materials in Fig. 1.4. For III-V materials, the E_F at the oxide/semiconductor interface is difficult to move too far from the CNL due to the relatively high and U-shape D_{it} [6]. As a result, if the CNL aligns to near the conduction band (E_C), it is easier to have electrons accumulated in the oxide/semiconductor interface while if the CNL aligns to near the valence band (E_V), it is easier to have holes accumulated in the oxide/semiconductor interface. Therefore, by selecting semiconductors with proper CNL, the fermi level pinning problem can be reduced.

Other than interface quality, bandgap of semiconductor is also an important character for solid state devices. For MOSFETs targeting on high speed and low power applications, too small bandgap will result in high thermal emission leakage current, large tunneling leakage current and high impact ionization current. Meanwhile, too

wide bandgap causes difficulties in channel inversion at same D_{it} level. Table 1.1 summaries the bandgap of common semiconductor materials at room temperature.

Table 1.1.
Bandgap of common semiconductors at 300 K

Semiconductor	E_G **(eV)**
Si	1.12
Ge	0.661
GaAs	1.424
InAs	0.354
$In_{0.53}Ga_{0.47}As$	0.74
InP	1.344
GaSb	0.726
InSb	0.17
GaN (Wurtzite)	3.39
GaN (Zinc Blende)	3.2
AlN	6.2
InN	1.9-2.05
SiC	2.36
GaP	2.26

*Data source from [7]

Summarizing the above discussion, to apply high mobility channel materials into CMOS ICs, here are the requirements which have to be considered.

- Higher electron or hole mobility comparing with silicon.
- Relative low D_{it}. CNL aligns near E_C for nMOSFETs while CNL aligns near E_V for pMOSFETs.

- Suitable bandgap (E_G)
- Ability to co-integrate onto same wafer for both nMOSFETs and pMOSFETs.

Therefore, considering both Fig. 1.3, Fig. 1.4 and Table 1.1, InGaAs has the most potential for nMOSFETs because its high electron mobility, CNL aligns near E_C and reasonable bandgap (0.74 eV in $In_{0.53}Ga_{0.47}As$). Although it has lower mobility comparing with InAs and InSb, but InAs and InSb have too small E_G. In the same way, Ge is considered to be a potential channel material for pMOSFETs because its high hole mobility, CNL aligns near E_V and reasonable bandgap (0.661 eV).

1.5 SS Reduction in MOSFETs and Steep-slope Transistors

1.5.1 Device Scaling and Short Channel Effects

As discussed in chapter 1.3, scaling is one of the major driven force in semiconductor industry. Currently, silicon CMOS technology has entered 10 nm technology node. SS has a thermionic limit of 60 mV/dec for MOSFETs. However, at short channel devices, it becomes more difficult to approach this limit due to SCEs because SS becomes larger when SCEs become stronger. The key to reduce the SCEs in MOSFETs is to make the distance between channel area and gate electrode as close as possible, in other words, to improve the gate control ability. To achieve this goal, there are several methods that can be applied in MOSFET engineering [8–12]. Firstly, reducing the equivalent oxide thickness (EOT) in gate dielectric to improve the gate control. Second, increasing the channel doping so that the depletion width can be reduced. Thus, channel area is closer to the gate. But to increase channel doping means to reduce carrier mobility. Halo technology is to increase channel doping only near the source and drain which has the same mechanism as increase channel doping uniformly but it has other benefits such as lower doping channel for higher carrier mobility. These two methods are applied for decades before 22 nm technology node was introduced to replace planar bulk silicon CMOS technology. Third,

by introducing thin body SOI structure, depletion width is limited by the thickness of the semiconductor so that channel is more close the gate electrode. Note that 2-dimensional (2D) materials play the same role as SOI structure in terms of SCEs control. Forth, applying 3D structure, such as FinFET structure or gate-all-around (GAA) structure to improve the channel control ability. FinFET was introduced in 22 nm node by Intel. The GAA structure has stronger immunity to SCEs than FinFET structure so that it might be applied in future CMOS technology nodes. Here the methods to reduce SCEs in MOSFETs are summarized.

- Reducing EOT.
- Increasing channel doping, uniformly or halo.
- Applying thin body SOI structure or 2D materials.
- Applying 3D structures such as FinFET or GAA.

Although it seems that there are many methods to further scale the devices, people are really approaching the physical limit of MOSFETs. Now in the smallest device, there are only less than 100 silicon atoms between source and drain. Quantum effects might destroy the MOSFET operation once the device is further scaled to ten silicon atoms or less.

1.5.2 Steep-slope Transistors

The motivation of steep-slope transistors has already been discussed in chapter 1.3. Many device concepts have been proposed to surpass this limitation such as the Tunneling FET (TFET) [13, 14], negative-capacitance FET (NC-FET) [15–17] and microelectromechanical (MEMS) switch [18, 19]. The SS of traditional MOSFET can be expressed as

$$SS = ln(10)\frac{kT}{q}(1 + \frac{C_{it} + C_S}{C_{ox}}) \tag{1.7}$$

where k is Boltzmann constant, T is temperature, q is elementary charge, C_{it} is interface trap capacitance and C_S is the semiconductor capacitance. In most cases, C_S can approximately equal to depletion capacitance (C_D). For transistor with ideal interface (C_{it}=0) and $C_S \ll C_{ox}$, eq. 1.7 becomes

$$SS = ln(10)\frac{kT}{q}. \tag{1.8}$$

It is also known as the thermionic limit of SS for MOSFET ($\sim 60\,\mathrm{mV/dec}$ at room temperature) because thermal emission over the channel barrier dominates the subthreshold current, which is a temperature dependent process.

Currently there are two popular ways to overcome this limit, tunneling field-effect transistor and negative capacitance field-effect transistor. Both of the above device concepts can be CMOS compatible and are explored in this thesis.

Tunneling field-effect transistors

TFET is basically a gated p-i-n diode. Such structure was proposed back to 1970s [20, 21] with surface tunneling as carrier transport mechanism. The first TFET with sub-60 mV/dec at room temperature was demonstrated at 2004 [13] which attracted a lot of attention and extensively studied as a steep-slope transistor since then. In the operation mode, the p-i-n diode is reversely biased so that the main current transport mechanism from source to drain is the Zener band-to-band tunneling (BTBT). With a gate voltage on the intrinsic region to control the band bending, such device can be abruptly switched on and off. Moreover, as BTBT isn't a temperature dependent process and subtreshold current in a normal MOSFET induced by thermal emission is blocked due to the existence of the bandgap (no barrier modulation), the SS of a TFET can break the thermionic limit of the subtreshold slope.

Negative capacitance field-effect transistors

Salahuddin and Datta [15] proposed the negative capacitance field-effect transistor by inserting a ferroelectric insulator into the gate stack the MOSFET. By replacing oxide capacitance to the capacitance of ferroelectric insulator (C_{FE}) in eq. 1.7 as

$$SS = ln(10)\frac{kT}{q}(1 + \frac{C_{it} + C_S}{C_{FE}}) \tag{1.9}$$

where C_{FE} can be negative so that the overall SS can be less than the thermionic limit ln(10)kT/q. The real negative capacitance in ferroelectric insulators cannot be directly measured by capacitance-voltage (C-V) or polarization-voltage (P-V) measurement because it is unstable. However, the negative capacitance effect can exist when it is in series with a positive capacitor, so that the total capacitance can be larger than the positive capacitor. Therefore, the negative capacitance in the ferroelectric insulator can provide a overall internal amplification to break the thermionic limit of MOSFET at 60 mV/dec at room temperature.

1.6 Thesis Outline

This thesis mainly pursues the potential channel materials and novel device structures and innovations, targeting on high speed and low power device applications at the end of silicon CMOS scaling. Chapter 2 mainly discusses nMOSFETs made of high mobility III-V material, InGaAs. InGaAs MOSFETs are studied in terms of device scaling, 3D structure and interface trap reduction. Chapter 3 studies the advanced electrical characterization in MOSFETs with small channel lengths. Chapter 4 discusses the fabrication and characterization of planar and 3D III-V TFETs. Chapter 5 discusses the fabrication and characterization of NC-FET made of III-V and 2D materials. Chapter 6 summaries the thesis and presents a outlook to the development of post-CMOS electron devices.

2. III-V MOSFETS FOR LOW POWER AND HIGH PERFORMANCE CMOS LOGIC APPLICATIONS

2.1 Introduction

In 2002, Ye and Wilk started to deposit Al_2O_3 on GaAs [22], which later was proved to have the ability to effectly remove the native oxide of GaAs due to the reaction between Trimethyl Aluminum (TMA) and the native oxide of GaAs [23–25]. This work opens a hot research on MOSFETs with high mobility III-V materials [11, 12, 26–45]. Currently, InGaAs has been considered as one of the most promising channel materials for future CMOS logic circuits because of its high electron injection velocity, properly aligned CNL and suitable bandgap [46]. People have spent a lot of efforts on fabricating InGaAs MOSFETs with short channel length and high I_{ON} and many works have been done on improving the oxide/InGaAs interface.

In this chapter, section 2.2 studies a novel dry etching method to obtain sub-10 nm L_{ch} beyond the lithography resolution limit and this type of MOSFET with L_{ch} down to $\sim$3 nm are demonstrated on both planar devices and FinFETs. To further improve the immunity to short channel effects, in section 2.3, the InGaAs GAA MOSFETs with raised S/D and ultrathin body structures are studied and performance improvement with thinner body are demonstrated. In section 2.4, the effect of forming gas anneal (FGA) on Al_2O_3/InGaAs interface are studied and it is found that FGA can significantly improve the quaility of Al_2O_3/InGaAs interface.

2.2 Ultimately Scaled Sub-10 nm V-Gate InGaAs MOSFETs

There has been several works focusing on the scaling of InGaAs transistors. InGaAs MOSFETs with implanted source and drain (S/D) have already been demon-

strated with channel length down to 20 nm [11, 12, 29]. However, InGaAs MOSFETs with implanted S/D structure suffer from large series resistance due to solid solubility limit and source starvation [47, 48]. Meanwhile, InGaAs MOSFETs with n+ (highly n-doped) raised S/D structure have been reported by regrowth method [30–33, 37, 49] or wet etching related methods [34, 35] with high on-current. InGaAs MOSFETs with sub-7 nm was also demonstrated by anisotropic wet etching method [36]. In this work, by fully using the anisotropic dry etching properties of III-V, using anisotropic dry etching process is proposed to fabricate the V-Gate InGaAs MOSFETs, featured with n+ reaised S/D and extremely short channel. Lithography etch window length modulation technique is applied to push the L_{ch} down to sub-10 nm (minimum $L_{ch} \sim$ 3 nm) beyond the lithography resolution limit. Ultimately scaled InGaAs FinFETs and planar MOSFETs with channel length down to sub-10 nm are demonstrated. InGaAs FinFETs with sub-10 nm L_{ch} shows better immunity to SCEs than planar MOSFETs which is promising for CMOS logic circuits beyond 10 nm technology node.

Fig. 2.1(a) shows the schematic diagram of a sub-10 nm InGaAs V-Gate FinFET and a Planar MOSFET. The top-down fabrication process is shown in Fig. 2.1(b). The starting material was a 2 inch semi-insulating InP substrate. 100 nm undoped $In_{0.52}Al_{0.48}As$ etch stop layer, 80 nm undoped InP layer, 10 nm undoped $In_{0.65}Al_{0.35}As$ channel layer, 2 nm undoped InP etch stop layer, 45 nm n+ ($1 \times 10^{19}\,cm^{-3}$ silicon doping in this work) $In_{0.53}Ga_{0.47}As$ and 10 nm n+ $In_{0.7}Ga_{0.3}As$ layer were sequentially grown by molecular beam epitaxy (MBE). The V-Gate structure was formed by anisotropic dry etching process with BCl_3/Ar reactive ion etching. The actual L_{ch} is 70-90 nm smaller than etch window length defined by electron beam lithography (L_{mask}) which means we can fabricate InGaAs MOSFET with sub-10 nm channel length with 90 nm lithography resolution limit. Then, fin structure was formed using BCl_3/Ar reactive ion etching while in the control group sample surface was protected by photoresist, there are four fins with 100 nm fin width (W_{Fin}) in parallel in each device. After 10 min 10% $(NH_4)_2S$ passivation, 8 nm Al_2O_3 was grown by atomic layer deposition (ALD) at 300 °C as gate dielectric with EOT=3.5 nm. The S/D

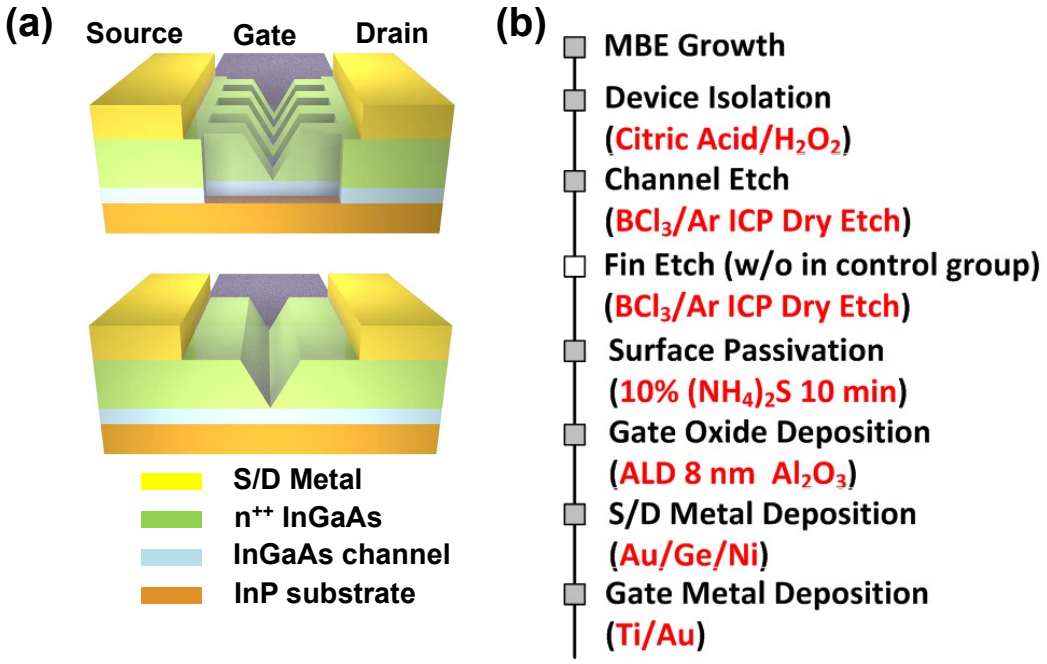

Fig. 2.1. (a) Schematic diagram of a sub-10 nm V-Gate FinFET and a planar MOSFET. (b) Fabrication process flow of V-Gate FinFETs and planar MOSFETs.

ohmic contacts were made with Au/Ge/Ni alloy and followed by a 350 °C 15 s rapid thermal annealing (RTA) process in N_2. All patterns were defined by a Vistec UHR electron beam lithography system.

Fig. 2.2(a)-(e) show the SEM images of V-Gate structure for InGaAs MOSFET fabricated by anisotropic dry etching. Fig. 2.2(a) shows the L_{ch} modulation effect by L_{mask} modulation. As the SEM cross section is rotated by 45°, L_{ch}=66 nm, 30 nm and 11 nm were obtained with L_{mask}=150 nm, 100 nm and 95 nm. With L_{mask} less than 90 nm, we can have L_{ch} less than 10 nm. Sub-10 nm L_{ch} was obtained as shown in Fig. 2.2(c) and the inset. The actual channel length is smaller than the L_{mask} because of the anisotropic property of dry etching process. Fig. 2.2(b) shows the etch

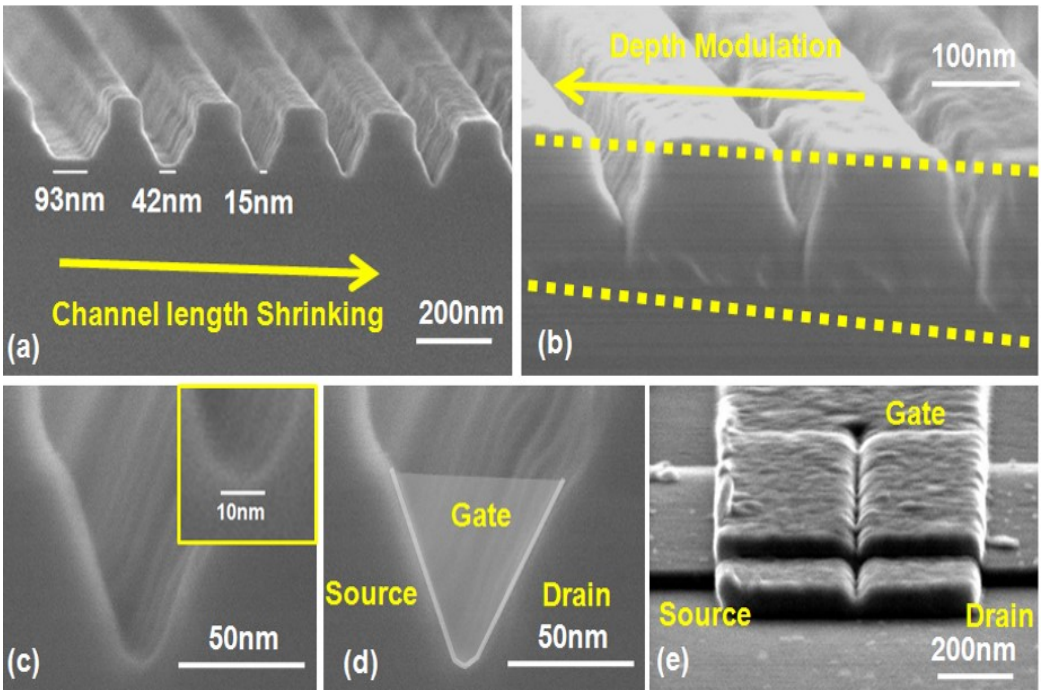

Fig. 2.2. (a) Channel length shrinking by etch window length modulation. (b) Channel thickness modulation by lithography window length modulation. (c) Illustration of sub-10 nm V-Gate channel. (d) Device structure illustration based on (c). (e) SEM image for a sub-10 nm InGaAs V-Gate MOSFET.

depth modulation by L_{mask}. Etch depth begins to be modulated after L_{ch} shrink into sub-10 nm region. By depth modulation, dry etch process can stop exactly on the InGaAs channel. Fig. 2.2(d) and 2.2(e) show the device structure with a sub-10 nm V-Gate.

Fig. 2.3(a) and 2.3(b) show the typical transfer and output $I-V$ characteristics of a planar sub-10 nm V-Gate device and a sub-10 nm V-Gate FinFET. At V_{GS}-V_T=1 V and V_{DS}=1 V, the measured I_{ON} for sub-10 nm FinFET device is 838 mA/mm while I_{ON} for planar sub-10 nm devices is 721 mA/mm. The maximum extrinsic transconductances (g_m) are 916 mS/mm and 565 mS/mm for the same FinFET device and planar device, respectively. The better on-state performance for the sub-10 nm V-Gate FinFET is ascribed to the quantum confinement in fin structure. The sub-

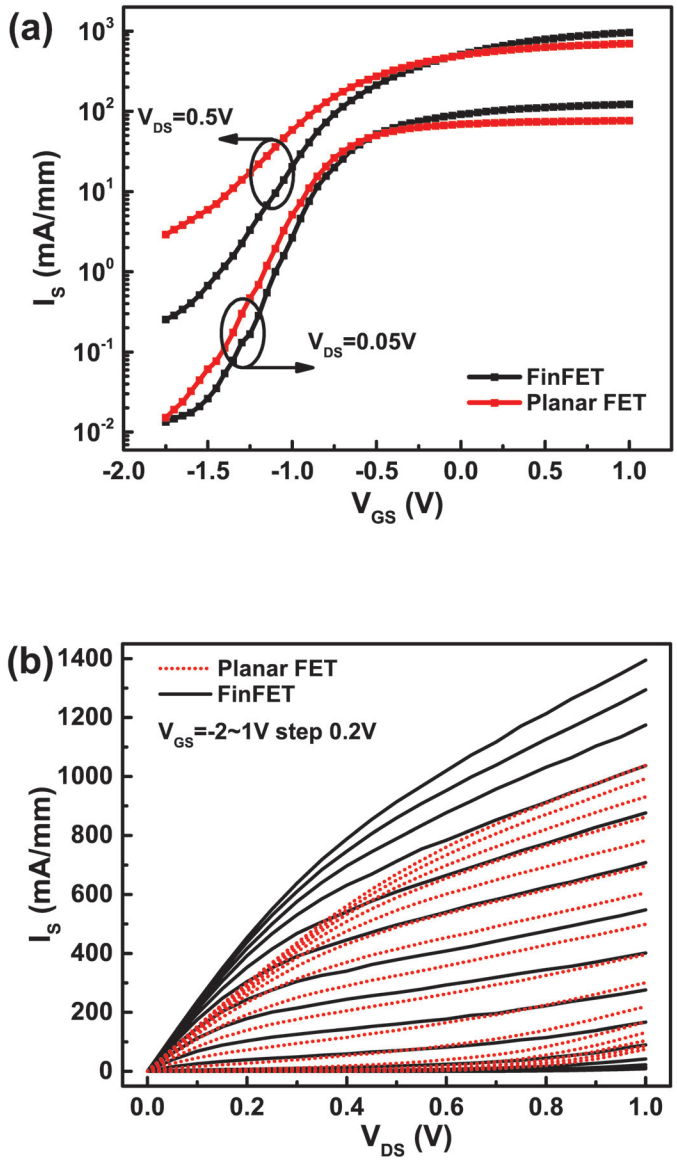

Fig. 2.3. (a) Transfer and (b) output characteristics of two well-behaved sub-10 nm V-Gate InGaAs FinFET and Planar MOSFET with an estimated channel length of 3 nm. Due to the drain to substrate leakage current and huge area difference between contacts and wires, I_S is presented instead of I_D, showing the fundamental transport properties inside channel.

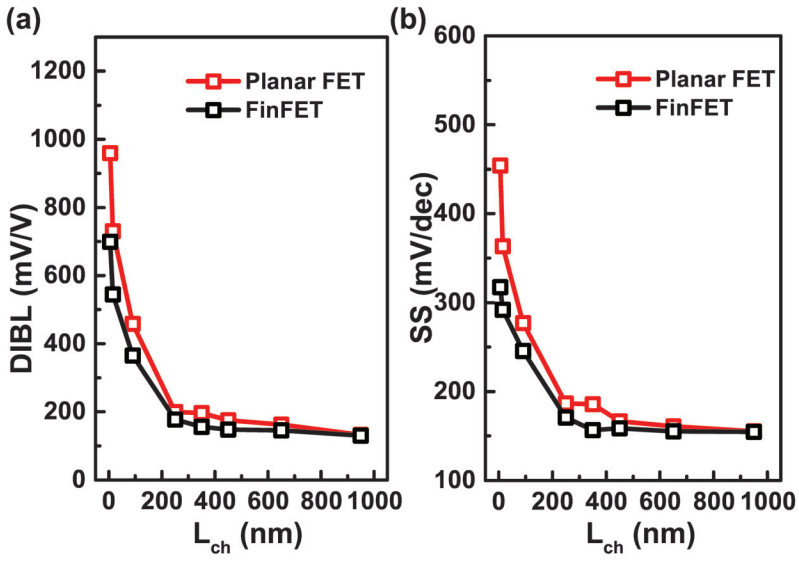

Fig. 2.4. (a) SS and (b) DIBL scaling metrics for planar V-Gate devices and V-Gate FinFETs. SS is extracted at V_{DS}=0.5 V.

10 nm FinFET device shows a SS of 173 mV/dec at V_{DS}=0.05 V and SS of 245 mV/dec at V_{DS}=0.5 V, Drain induced barrier lowering (DIBL) of 459 mV/V, I_{ON}/I_{OFF} ratio of 5.4×10^3 at V_{DS}=0.5 V while in the planar sub-10 nm device, SS of 209 mV/dec at V_{DS}=0.05 V and SS of 440 mV/dec at V_{DS}=0.5 V, DIBL of 916 mV/V, I_{ON}/I_{OFF} ratio of 0.43×10^3 at V_{DS}=0.5 V were obtained. The off-state performance in the sub-10 nm FinFET is significantly better than planar sub-10 nm device, especially when V_{DS} is large in terms of the SS, DIBL, I_{ON}/I_{OFF} ratio and the sub-10 nm FinFET is easier to be turned off. The planar sub-10 nm device is harder to be turned off, as shown in the output characteristics in Fig. 2.3 (b), suggesting short channel effects (SCEs) severely degrade the off-state performance of planar sub-10 nm device at high V_{DS} due to DIBL. The V_T of the sub-10 nm FinFET is -0.87 V while V_T of planar sub-10 nm device is -0.98 V. V_T shows a positive shift from planar device to 3D FinFET device also confirms better gate control in 3D structure.

Furthermore, we study the scaling metrics of InGaAs planar V-Gate devices and V-Gate FinFETs with L_{ch} from 1 µm down to sub-10 nm. It is found that SS and DIBL increase dramatically when the L_{ch} shrinks into sub-10 nm regime. Meanwhile, the increasing of SS and DIBL is obviously suppressed with a V-Gate FinFET structure in sub-100 nm region. Further suppression of SCEs can be achieved by reducing W_{Fin}, EOT scaling or introducing the 3D nanowire structure.

In summary, ultimately scaled V-Gate planar MOSFETs and FinFETs with channel length from 1 µm to sub-10 nm were demonstrated experimentally. A novel anisotropic dry etch and lithography etch window length modulation technique were applied to push the channel length down to sub-10 nm beyond the lithography limitation. V-Gate devices with FinFET structure show better on-state performance than devices with planar V-Gate structure. Meanwhile, V-Gate devices with FinFET structure show better immunity to SCEs in sub-10 nm regime. SS of 245 mV/dec, DIBL of 459 mV/V, I_{ON}/I_{OFF} ratio of 5.4×10^3 at V_{DS}=0.5 V were obtained in a sub-10 nm V-Gate FinFETs.

2.3 InGaAs Gate-all-around MOSFETs with Raised Source and Drain and Ultrathin Body Structures

In last section, InGaAs MOSFETs with raised S/D and highly scaled channel length. The advantages of raised S/D structure have been discussed. 3D InGaAs devices such as FinFETs and the GAA MOSFETs have been shown to offer large drive current and excellent immunity to SCEs [11,12,29,38–45,49]. In particular, the GAA MOSFETs provide the best gate electrostatic control and therefore the ultimate channel length scalability. It is known that better SCE control can be obtained by reducing the nanowire size, enabling further L_{ch} scaling. To further improve the immunity of SCEs of this type of structures, in this section, InGaAs GAA MOSFETs with raised S/D and ultrathin body structures are fabricated and discussed [50].

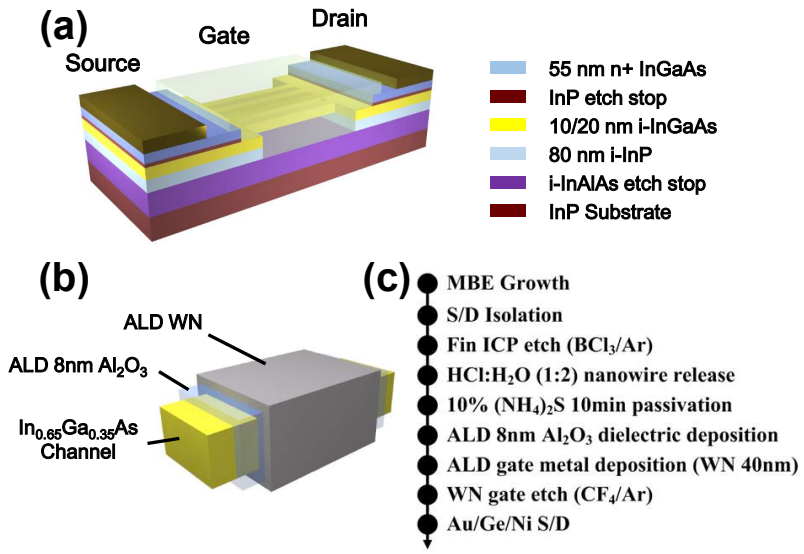

Fig. 2.5. (a) Schematic diagram, (b) cross sectional view and (c) fabrication process flow of n+ raised source and drain InGaAs gate-all-around MOSFETs.

Fig. 2.5(a) and 2.5(b) show the schematic diagram and cross sectional view of the n+ raised S/D InGaAs GAA MOSFET. The top-down fabrication process is shown in Fig. 2.5(c). The starting material was a 2 inch semi-insulating InP substrate. 100 nm undoped $In_{0.52}Al_{0.48}As$ etch stop layer, 80 nm undoped InP layer, 10 nm or 20 nm undoped $In_{0.65}Al_{0.35}As$ channel layer, 2 nm undoped InP etch stop layer, 45 nm n+ $In_{0.53}Ga_{0.47}As$ and 10 nm n+ $In_{0.7}Ga_{0.3}As$ layer were sequentially grown by molecular beam epitaxy (MBE). n+ raised S/D structure was formed by citric acid and H_2O_2 based selective wet etching and device isolation was also done in the same process. 400 nm gap between n+ raised S/D was obtained. The wet etching stopped just on the 2 nm InP etch stop layer due to the strong etch selectivity between InGaAs and InP. Nanowire fins were defined by BCl_3/Ar reactive ion etching. HCl based release process was then performed to create free standing 200 nm long InGaAs nanowires. After 10 min 10% $(NH_4)_2S$ passivation, 8 nm Al_2O_3 and 40 nm tungsten nitride (WN)

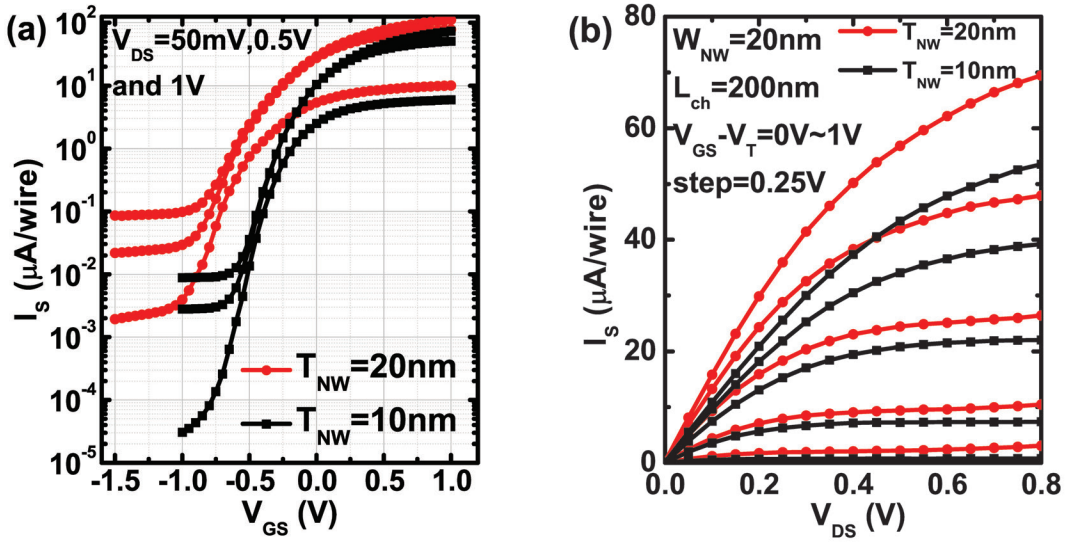

Fig. 2.6. (a) Transfer and (b) output characteristics of two well-behaved n+ raised source and drain InGaAs gate-all-around MOSFETs.

gate metal were grown by ALD at 300 °C and 385 °C as gate insulator and gate metal, respectively. After WN gate etch process, S/D contacts were formed with Au/Ge/Ni alloy and followed by a 350 °C 15 s RTA process in N_2. Thermal budget as low as 350 °C was maintained with the implantation free process. Each device has four wires in parallel. All patterns were defined by a Vistec UHR electron beam lithography system.

Fig. 2.6(a) and 2.6(b) show the typical transfer and output $I-V$ characteristics of devices with 10 nm and 20 nm nanowire thickness (T_{NW}), 20 nm nanowire width (W_{NW}) and 200 nm L_{ch}. Maximum I_{ON} over 1 mA/μm at V_{GS}-V_T=1 V and V_{DS}=1 V is obtained, normalized by the perimeter of nanowires. The average normalized I_{ON} and g_m at V_{GS}-V_T=1 V and V_{DS}=1 V of the 10 nm nanowire devices are 645 μA/μm and 837 μS/μm, while the average I_{ON} and g_m of the 20 nm nanowire devices are 735 μA/μm and 993 μS/μm. The 10 nm thick nanowire devices show an average SS of 117 mV/dec, DIBL of 83 mV/V, I_{ON}/I_{OFF} ratio of 1.5×10^5 at V_{DS}=0.05 V while the

20 nm thick nanowire devices show an average SS of 158 mV/dec, DIBL of 117 mV/V, I_{ON}/I_{OFF} ratio of 7×10^3 at V_{DS}=0.05 V. The average V_T of 10 nm nanowire devices is -0.25 V while the average V_T of 20 nm nanowire devices is -0.45 V. V_T shows a positive shift with nanowire dimension shrinking. The slightly better on-state performance of devices with 20 nm thick nanowire is mainly ascribed to three reasons. First, the ultrathin nanowire structure suffers more mobility degradation because ultrathin nanowires are more sensitive to surface roughness. Second, the impact of quantum capacitance is stronger in thinner nanowires so that carrier concentration in the channel is reduced. Third, S/D series resistance (R_{SD}) increases as nanowire dimension shrinking. The R_{SD} of devices with different nanowire thickness are extracted using the method described in Ref. [51] and the average R_{SD}, normalized by the perimeter of the devices, for 10 nm thick nanowire is 0.61 Ω mm while the average R_{SD} for 20 nm thick devices is 0.42 Ω mm. Comparing to devices with implanted S/D and ultrathin structure [29], the n+ raised S/D ones have a larger saturation current and low R_{SD}. R_{SD} of both devices with implanted S/D (average R_{SD}=1.3 Ω mm) [11] and devices with n+ raised S/D are extracted. It is understood that the MBE grown n+ S/D has a much higher carrier density, thus a lower contact resistance with Au/Ge/Ni metal contacts. At the same time, the high carrier density and low defects in MBE materials also reduces the resistivity of the semiconductor. Therefore, n+ raised S/D structure is a preferable structure for high-performance InGaAs GAA MOSFETs.

Another performance improvement induced by n+ raised S/D InGaAs GAA MOSFETs with ultrathin nanowire is the reduction of off-state leakage current because of the ultrathin body structure, as shown in Fig. 2.6(a) and Fig. 2.7. The average I_{OFF} decreases by about one order of magnitude at V_{DS}=1 V and by 30 times at V_{DS} =50 mV when T_{NW} decrease from 20 nm to 10 nm. The prominent difference in off-state performance is attributed to the quantum confinement effect so that both tunneling leakage and thermal emission leakage can be suppressed.

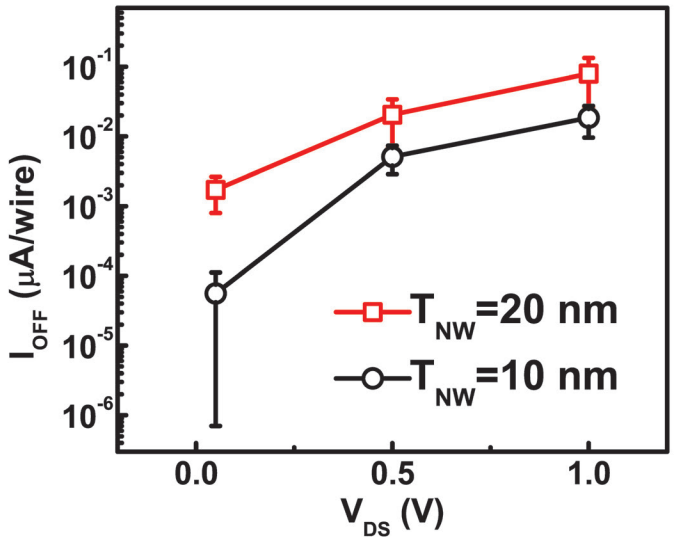

Fig. 2.7. Off-state leakage current comparison between the devices with 10 nm and 20 nm T_{NW} at different drain voltages.

2.4 Effects of Forming Gas Anneal on Ultrathin InGaAs Nanowire Metal-oxide-semiconductor Field-effect Transistors

InGaAs nanowires fabricated by top-down technology with sub-10 nm wire dimension, either W_{NW} or T_{NW}, was reported for the first time in this work. On the other hand, the interface quality is one of the critical problems for III-V MOSFETs. Superior interface quality is required for optimizing both the on-state and off-state performance of MOSFETs. Al_2O_3 is commonly used as the gate insulator for InGaAs MOSFETs for the relatively low D_{it}. Various passivation methods have been developed and optimized on the Al_2O_3/InGaAs interface such as $(NH_4)_2S$ passivation [52, 53], surface nitridation [54, 55] and phosphor passivation [56]. Forming gas anneal is another common post metallization treatment used to improve the interface quality of Al_2O_3/InGaAs. Interface traps, oxide charges and border traps reduction after FGA have been reported by C-V methods [57, 58]. Recent study of effects of

FGA on planar devices shows that on state performances such as I_{ON} and g_m are improved after FGA [59]. However, the impacts of FGA have not been studied in short channel devices with GAA structure. The compatibility between FGA and other passivation methods have not been studied either.

20-80 nm L_{ch} short channel $In_{0.65}Ga_{0.35}As$ GAA MOSFETs with 6 nm T_{NW} and 30 nm W_{NW} have been fabricated with or without FGA treatment. FGA offers improvement in the on-state and off-state performance of the devices. The reduction of SS and the increase of g_m and I_{ON} verify the improvement of the interface quality. The average interface trap density drops by 40% on average after FGA. Moreover, SS and DIBL do not increase when L_{ch} scales from 80 nm down to 20 nm, demonstrating the excellent scalability of InGaAs GAA MOSFET with sub-10 nm nanowire dimension. It is also found that the 30 min 400 °C FGA passivation is fully compatible with the $(NH_4)_2S$ passivation. The interface trap density is significantly improved in devices with $(NH_4)_2S$ passivation and FGA together than those with $(NH_4)_2S$ passivation only.

Fig. 2.8(a) shows the schematic diagram of the InGaAs GAA MOSFET fabricated in this work and the cross sectional TEM image of an InGaAs nanowire with 6 nm T_{NW}. The fabrication process flow of the devices is shown in Fig. 2.8(b). The top-down fabrication process is similar to that demonstrated in [12]. The starting material is a 2 inch semi-insulating InP substrate. 100 nm undoped $In_{0.52}Al_{0.48}As$ etch stop layer, 80 nm undoped InP layer, 10 nm undoped $In_{0.65}Al_{0.35}As$ channel layer and 2 nm undoped InP layer were sequentially grown by MBE. Source/drain implantation was performed at an energy of 20 keV and a dose of 1×10^{14} cm^{-2}, followed by dopant activation at 600 °C for 15 s in nitrogen ambient. After fabricating nanowire fins using BCl_3/Ar reactive ion etching, HCl based release process was performed to create the free-standing InGaAs nanowires. Before the gate stack deposition, 10% $(NH_4)_2S$ passivation was performed. The gate dielectric is 5 nm ALD Al_2O_3 to study the effect of FGA on Al_2O_3/InGaAs interface while maintaining a low gate leakage current. Following ALD WN gate metallization process, the devices are divided into

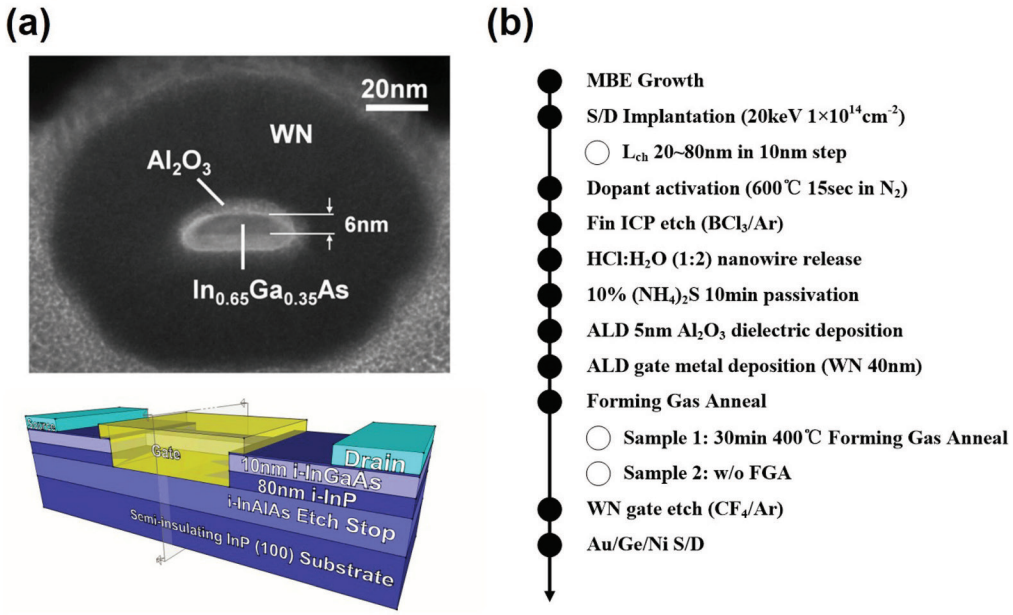

Fig. 2.8. (a) Cross sectional TEM image and schematic diagram of an InGaAs GAA MOSFET with T_{NW} = 6 nm. (b) Fabrication process flow of the InGaAs GAA MOSFETs.

two groups. One is treated with 30 min 400 °C FGA (4% H_2 / 96% N_2) and the other serves as the control group. After gate etch process, source/drain contacts were formed with Au/Ge/Ni alloy. Each device has four nanowires fabricated in parallel. All patterns were defined by a Vistec UHR electron beam lithography system.

Fig. 2.9(a) and (b) show the $I-V$ characteristics comparison between two typical devices with L_{ch}=20 nm, W_{NW}=30 nm with and without 30 min 400 °C FGA. Device with FGA shows an 89% increase in on-current I_{ON} at V_{GS}-V_T=0.8 V and the SS of device with FGA is 93 mV/dec, which is 23 mV/dec smaller than that of device without FGA. Maximum g_m of device with FGA is also found to be 59% larger than that of control device without FGA. After being normalized by the perimeter of the nanowire, the best I_{ON} and peak g_m at at V_{GS}-V_T=1 V is 505 µA/µm and 665 µS/µm, respectively. The saturation-currents of devices in this work are lower compared to InGaAs GAA MOSFETs with 30 nm T_{NW} and the same W_{NW} and L_{ch} [12]. The

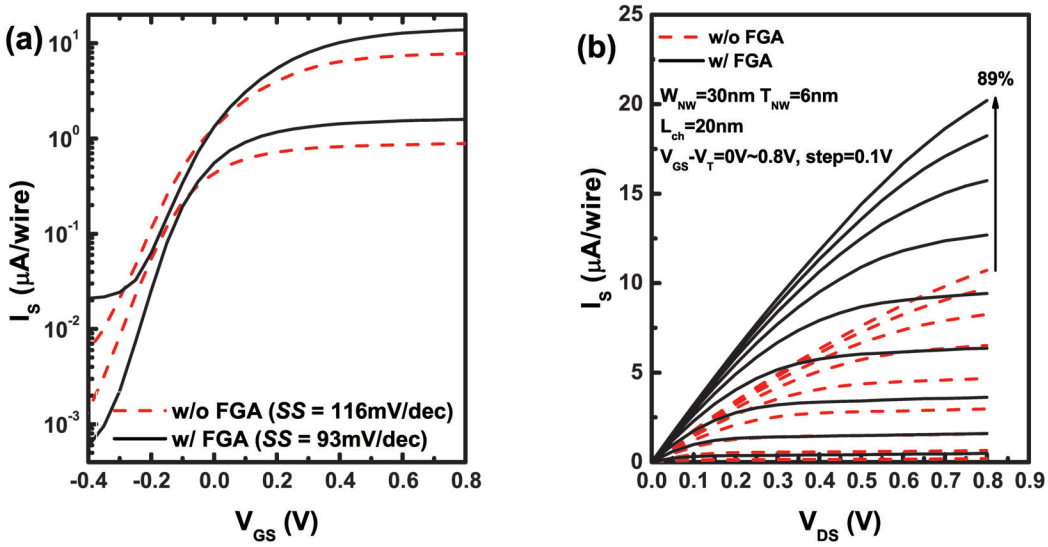

Fig. 2.9. (a) Output and (b) transfer characteristics of two typical InGaAs GAA MOSFETs with L_{ch} = 20 nm, W_{NW} = 30 nm and T_{NW}=6 nm with and without FGA treatment. Due to the significant reverse junction leakage current, I_S is presented instead of I_D.

reduction in drive current is attributed to the larger impact of surface roughness which decreases the channel mobility. Details of the transport properties of the ultra-thin nanowires are under investigation.

To study the effects of FGA, the average SS, threshold voltage V_T, and I_{ON} of InGaAs GAA MOSFETs with L_{ch} between 20 nm and 80 nm have been extracted. Fig. 2.10(a), 2.10(b) and Fig. 2.11(a) show the statistical data of SS, V_T and I_{ON} for devices with and without FGA. As shown in Fig. 2.10(a), devices with FGA has a much lower SS for all channel lengths compared to the control devices without FGA. The average of SS shows an obvious reduction from about 117 mV/dec to 93 mV/dec. The improvement of the off-state performance indicates that FGA can reduce the interface traps within the bandgap. The threshold voltage is found to increase with FGA treatment, as shown in Fig. 2.10(b). It is known that traps at the Al_2O_3/InGaAs

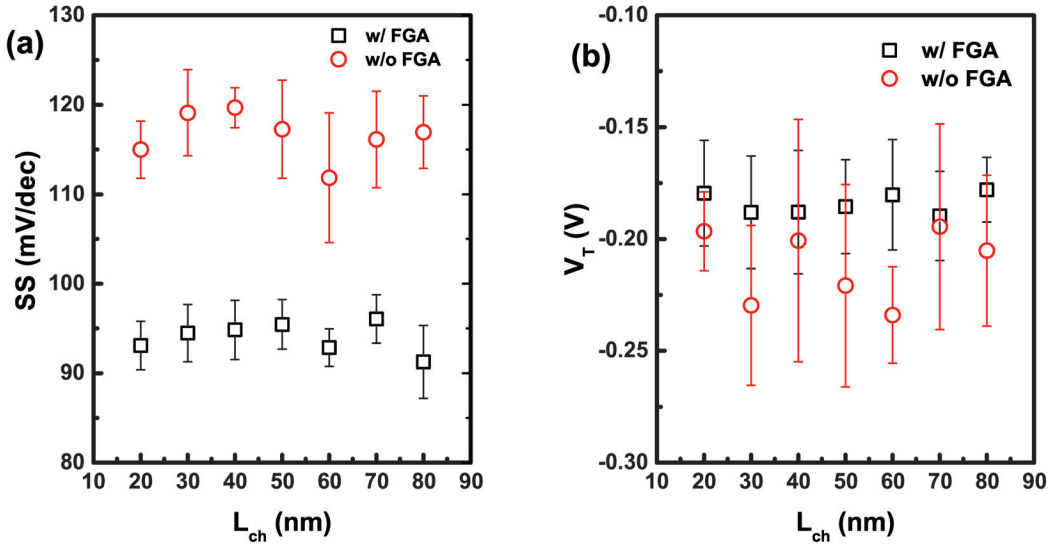

Fig. 2.10. (a) SS and (b) V_T of these devices with W_{NW}=30 nm and T_{NW}=6 nm versus L_{ch}. With FGA and their control devices are in comparison. Each data point represents 5-10 measured devices. V_T is extracted from linear extrapolation at V_{DS} = 50 mV.

interface are mostly donor type. The reduction of donor interface trap does not have a significant impact on the threshold voltage while the reduction of acceptor trap leads to negative V_T shift [60]. Thus, the positive shift of V_T in this study is attributed to the reduction of positive fixed charge density and the I_{ON} charge density in oxide layer. Fig. 2.11(a) shows the comparison of on-current. I_{ON} is found to increase by 14% on average with FGA, accompanied by 25% g_m enhancement (not shown). One origin for the I_{ON} enhancement is the reduction of interface trap density near the conduction band edge. Another origin is that mobility is improved due to the reduction in Coulomb scattering as a result of oxide charge reduction.

Interface trap density of the devices are extracted with the approximate formula as in eq. (1.7). The depletion capacitance can be neglected for its weak impact on SS due to undoped channel. Devices in [12] shows the minimum SS of 63 mV/dec, which

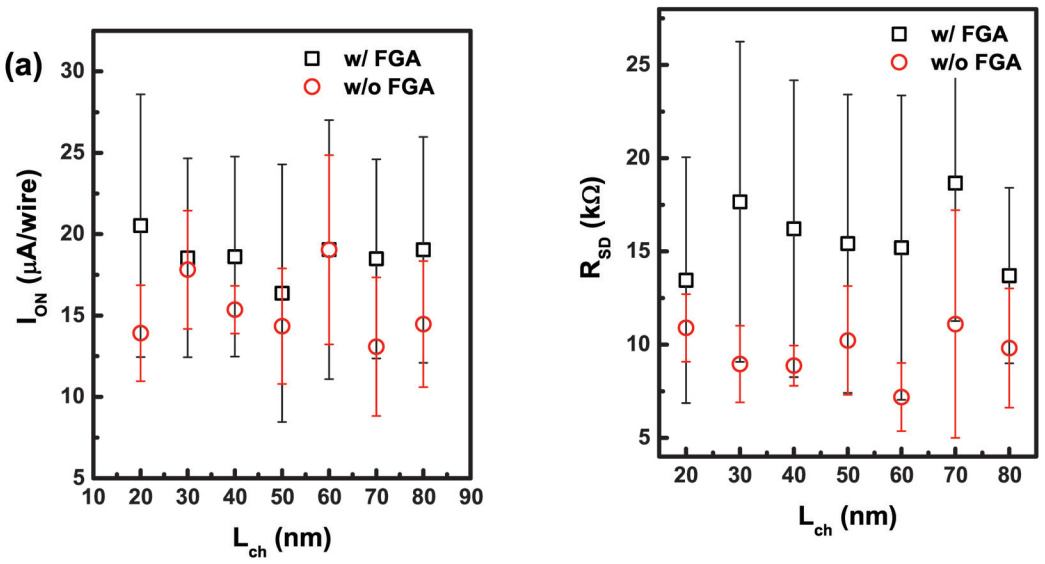

Fig. 2.11. (a) I_{ON} and (b) R_{SD} versus L_{ch} in comparison between FGA devices and their control ones.

indicates C_D contribute to at most 3 mV/dec to SS in the InGaAs GAA MOSFET structure. As the device structure is similar as [12], C_D is also negligible in this work. It is estimated that the upper limit of mid-gap D_{it} is reduced by 40% percent with FGA, indicating that FGA can improve the interface quality of the Al_2O_3/InGaAs interface.

Another interesting phenomenon found in this work is the standard deviation (STD) comparison for SS, V_T, and I_{ON}. The SS STD and V_T STD of devices with FGA are smaller than the control devices without FGA, while the I_{ON} STD and g_m STD of devices with FGA are larger than devices without FGA. The STD of SS and V_T reduces with FGA treatment because of the improvement of the interface quality as shown earlier. However, the larger on-state STD seems unexpected and contradictory to the D_{it} reduction. The most possible reason is that the ohmic contact of the devices with FGA is worse than those without FGA, which can in turn increase on-state variation. To confirm this hypothesis, R_{SD} is extracted by linear fitting total

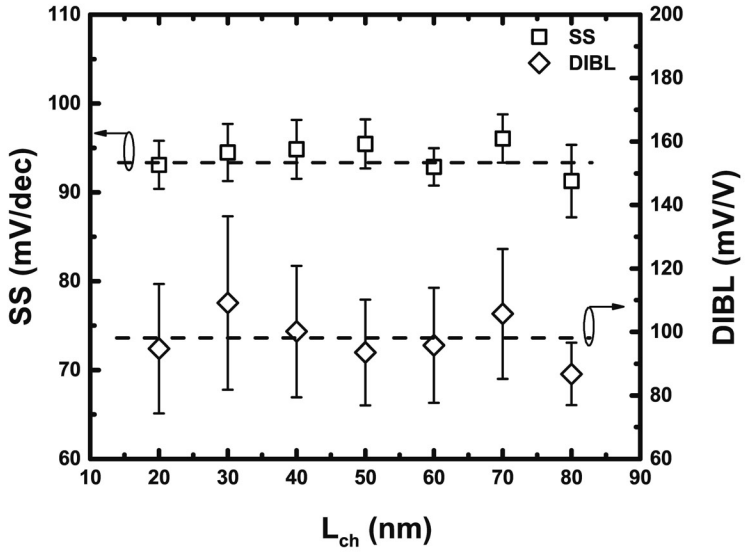

Fig. 2.12. SS and DIBL versus L_{ch} of FGA treated InGaAs GAA MOSFETs with W_{NW} = 30 nm and T_{NW}=6 nm

resistance and $1/(V_{GS}$ - V_T - $V_{DS}/2)$ at small V_{DS} [61]. As shown in Fig. 2.10(b), both average value of R_{SD} and STD of R_{SD} of devices with FGA is much larger than devices without FGA. The larger R_{SD} of devices with FGA suggests that the intrinsic current improvement of devices with FGA is even larger than that shown in Fig. 2.10(a). Though the exact reason for the increased R_{SD} after FGA has not been clearly understood, it is likely that the Au/Ge/Ni alloy based ohmic contact is sensitive to FGA treatment. More advanced source/drain contact technologies need to be explored to reduce the R_{SD} and improve on-state variation.

Furthermore, we investigate the scaling metrics of InGaAs GAA MOSFETs with 6 nm T_{NW} and FGA. The T_{NW} scaling of an InGaAs GAA MOSFET theoretically has the same effect as the W_{NW} scaling in terms of the electrostatic control [12]. However, the scaling of T_{NW} can reduce the surface area that has underwent dry etching process during the nanowire formation, leading to the reduced surface roughness. Fig. 2.12 shows SS and DIBL versus L_{ch} with W_{NW}=30 nm. No evidence of L_{ch} dependence of

SS and DIBL are observed in this work, as opposed to the InGaAs GAA MOSFETs with larger T_{NW} [12]. The results show that the InGaAs GAA MOSFETs with extremely thin T_{NW} offer better immunity to SCE and improved scalability which can be further improved by EOT scaling.

In conclusion, InGaAs GAA MOSFETs with 6 nm T_{NW} have been fabricated. The effects of FGA on the performance of the devices are systematically studied. It is found that the 30 min 400 °C forming gas anneal results in a improved Al_2O_3/InGaAs interface and is also fully compatible with the $(NH_4)_2S$ passivation. A scaling metrics study of the InGaAs GAA MOSFETs has also been carried out. The extremely thin nanowire structure has been shown to improve SCE immunity and it is very promising for future logic applications.

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3. CHARACTERIZATION OF ULTRA-SCALED III-V MOSFETS

3.1 Introduction

To accurately evaluate the performance of a MOSFET is important. Accurate and reliable characterization techniques enable device researchers and engineers to locate the problems with the MOSFETs and to further improve the device performance. Meanwhile, interface and contact qualities have the most importance to device performance. However, as MOSFETs have been scaling down to 14 nm technology node currently, the most classic characterization techniques become difficult to characterize such small devices.

Interface quality is one of the major determinants of the performance for MOSFETs. Relatively high D_{it} is the main issue to prevent using MOSFETs made of high mobility materials beyond silicon [6, 46, 62]. Tremendous efforts have been spent to minimize the D_{it} on III-V and Ge with different dielectric techniques in the past decades, making high-mobility ultra-scaled MOSFETs a reality [63–66]. Therefore, how to correctly evaluate D_{it} on nanoscale MOSFETs becomes very important. However, the first problem is, L_{ch} of MOSFETs are rapidly decreasing to deep sub-100 nm region, the conventional D_{it} extraction methods, such as C-V, charge pumping and DC-IV methods, becomes difficult due to the very small gate area. Meanwhile, a second problem is that the subthreshold method becomes more inaccurate at smaller channel length, because SS increases as L_{ch} scaling down due to SCEs but not D_{it} [8, 9, 67–73].

In this chapter, a new and simple method to solve the SCE problem is proposed in section 3.2, which demonstrates a correction to the conventional subthreshold method in D_{it} extraction. Section 3.3 utilizes low frequency noise (LFN) and random tele-

graph noise (RTN) as probes to analyze the interface quality using the advantage that noise signals are stronger in smaller devices.

3.2 On the Interface Trap Density Extraction of Ultra-scaled MOSFETs: A Correction to Subthreshold Method

The subthreshold method of D_{it} using eq. (1.7) becomes more inaccurate at smaller channel length, because SS increases as L_{ch} scaling down due to SCEs but not D_{it}. Without eliminating the impact of SCEs from SS, SS method is less accurate at shorter L_{ch}. As a result, comparing interface quality of short channel MOSFETs between different works becomes difficult. In this work, an analytic model on DIBL-SS relation is first derived. Then, a simple D_{it} extraction method on ultra-scaled MOSFETs is introduced, in which the impact of SCEs on SS is eliminated by a simple linear fitting of SS with respect to DIBL. Finally, experimental and simulation results are provided to verify the DIBL-SS relation and the D_{it} extraction method.

Fig. 3.1 shows the capacitor model of 2D electrostatics of a four-terminal MOSFETs. The surface potential of the top barrier (Ψ_S) is calculated as [67]

$$\Psi_S = \frac{C_{GB}}{C_\Sigma}V_G + \frac{C_{DB}}{C_\Sigma}V_D + \frac{C_{SB}}{C_\Sigma}V_S + \frac{C_D + C_{it}}{C_\Sigma}V_B + \frac{Q}{C_\Sigma} \tag{3.1}$$

where Q is the charge density at the top barrier when all terminals are grounded in the capacitor model, C_Σ is the parallel combination of all the five capacitors, explicitly,

$$C_\Sigma = C_{GB} + C_{DB} + C_{SB} + C_D + C_{it} \tag{3.2}$$

Eq. (3.1) explains the impact of SCEs on DIBL and SS. At short L_{ch}, C_{DB} and C_{SB} are comparable with C_{GB} so that V_D and V_S can also affect the charge in the channel. As L_{ch} decreases, C_{GB} becomes smaller so that C_{DB}/C_Σ increases which lowers the barrier. Meanwhile, C_{GB}/C_Σ decreases which increases the SS. DIBL and SS can be expressed as [72, 73]

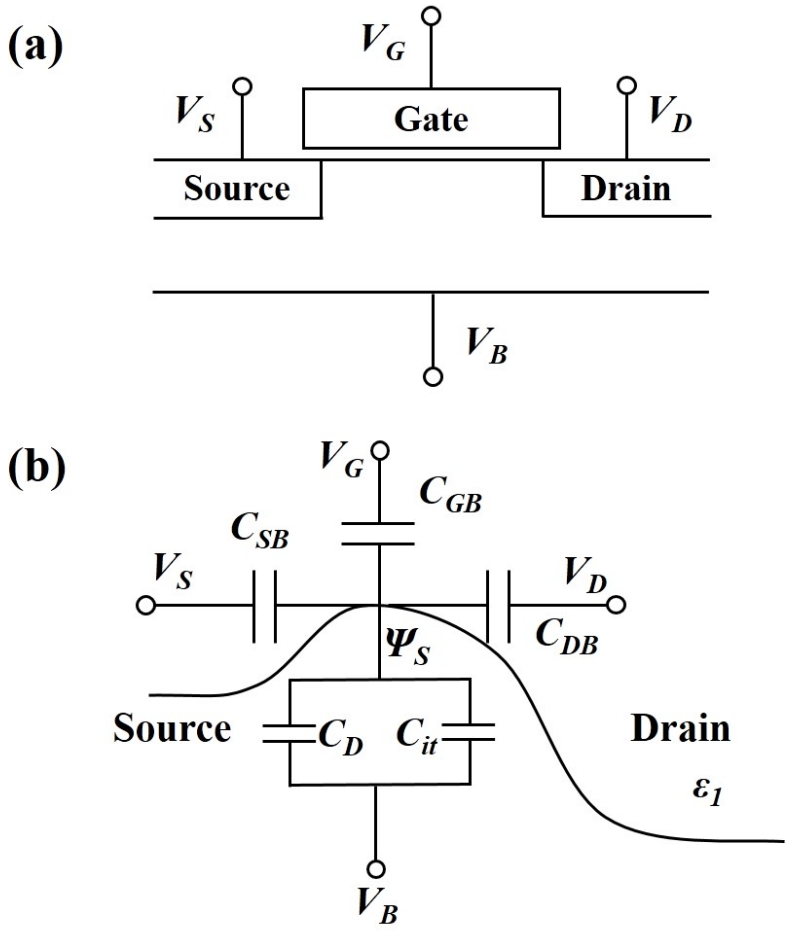

Fig. 3.1. Illustration of the capacitor model of 2D electrostatics on MOSFETs. Ψ_S is the potential at the top barrier which is controlled by gate, source, drain and body potentials. C_{SB}, C_{DB} and C_{GB} represent source to body capacitance, drain to body capacitance and gate to body capacitance, respectively. C_D is the depletion capacitance, it is sometimes absent in the thin-body SOI and nanowire structures considered. C_{it} is the interface trap capacitance. The model describes the electrostatic control of the potential on the top of the barrier.

$$DIBL = \left.\frac{\partial V_G}{\partial V_D}\right|_{\Psi_S} = \frac{C_{DB}}{C_{GB}} \tag{3.3}$$

and

$$SS = \frac{\partial log(I_D)}{\partial \Psi_S}\frac{\partial \Psi_S}{\partial V_G} = \frac{ln(10)kT}{q}\frac{C_\Sigma}{C_{GB}}. \tag{3.4}$$

By inserting eq. (3.2) and eq. (3.3) into eq. (3.4) and using C_{GB}=C_{ox}, SS as a function of DIBL is obtained as follows,

$$SS = \frac{ln(10)kT}{q}(1 + \gamma DIBL + \frac{C_D + C_{it}}{C_{ox}}), \tag{3.5a}$$

$$SS = \frac{ln(10)kT}{q}\gamma DIBL + SS_L, \tag{3.5b}$$

where

$$\gamma = 1 + \frac{C_{SB}}{C_{DB}}, \tag{3.6}$$

and

$$SS_L = \frac{ln(10)kT}{q}(1 + \frac{C_D + C_{it}}{C_{ox}}), \tag{3.7}$$

which is the classic long channel SS formula that is the same as in eq. (1.7). The γ defined here is a function of C_{SB}/C_{DB}. In particular, at low drain bias, γ equals to 2 because of the source and drain symmetry (C_{SB}=C_{DB} when V_D=V_S). If DIBL is measured at high drain bias, it is reasonable to assume that γ deviates from 2 but still a constant number, as suggested by experiment and simulation in Fig. 3.2. Thus, in a set of devices with the same device structure and DIBL evaluated at the same bias condition, γ is close to a constant number. Eq. (3.7) is the model of SS typically seen at long channel devices without considering SCEs. The depletion capacitance, C_D, sometimes is absent in the thin-body SOI and nanowire structures considered. In classical subthreshold D_{it} extraction method, eq. (3.7) is used to calculate D_{it} from SS_L without considering SCEs. However, eq. (3.4) and eq. (3.5) point out that classical subthreshold method in D_{it} extraction, which assumes $C_{DB}/C_{GB} \rightarrow 0$, would give a significant overestimation of D_{it} in ultra-scaled MOSFETs due to the failure to take C_{DB} into account. DIBL-SS relation can be used here to eliminate the SCEs in SS as SS is a first order linear function DIBL. As shown in eq. (3.5b), the slope of SS with respect to DIBL is γln(10)kT/q while the intersection with y-axis at DIBL=0 is SS_L. Therefore from the y-axis intersection of DIBL-SS relation, SS_L can be extracted. Then, D_{it} can be evaluated classically using eq. (3.5b). By using

C_{it}=q^2D_{it} and assuming C_D is small, D_{it} can be calculated by simple algebra. The result is

$$D_{it} = \frac{C_{ox}}{q^2}(\frac{qSS_L}{ln(10)kT} - 1). \tag{3.8}$$

When eq. (3.5) and eq. (3.8) are applied to extract D_{it}, we need to have the devices with different DIBL. This can be done simply by fabricating devices with different L_{ch} at similar scale and with SCEs to obtain a clear range of DIBL. Device-to-device variability also provides source of various DIBL. Fig. 3.2(a) shows SS versus DIBL on three sets of silicon MOSFETs with different L_{ch} and structures to verify eq. (3.5). The devices are fabricated with L_{ch} from 30 nm to 60 nm for silicon gate-all-around (GAA) MOSFETs [74], from 35 nm to 85 nm for SOI silicon MOSFETs [75], from 30 nm to 120 nm for fully depleted SOI (FDSOI) silicon MOSFETs as simulation results [76]. It is found by both experiments and simulations that SS_L extracted from silicon devices is close to ideal 60 mV/dec at room temperature due to the low D_{it} in silicon devices and negligible C_D in thin-body SOI and GAA structures. Fig. 3.2(b) shows the application of this method to D_{it} evaluation of InGaAs GAA MOSFETs. The detailed device fabrication process and device performance can be found in [12]. The devices are fabricated with L_{ch} from 20 nm to 80 nm, nanowire width from 20 nm to 35 nm and with 0.5 nm Al_2O_3/4 nm $LaAlO_3$ as gate dielectric, EOT is 1.2 nm. The SS_L is extracted to be 66.3 mV/dec. The estimated D_{it} from eq. (3.8) is 1.9×10^{12} $eV^{-1}\,cm^{-2}$ which is a factor of 2 smaller than the overestimated value of $\sim 4 \times 10^{12}$ $eV^{-1}\,cm^{-2}$ from the measured SS [12].

To further verify the proposed D_{it} extraction method. TCAD simulation is done on silicon GAA MOSFETs. The simulated devices have a cylinder silicon nanowire channel with L_{ch} from 15 nm to 60 nm, 10 nm nanowire diameter (D_{NW}) and with 2 nm SiO_2 as gate dielectric. The channel material is intrinsic silicon so that C_D is negligible. D_{it} from 0 to 1×10^{12} $eV^{-1}\,cm^{-2}$ is used in simulation. DIBL-SS relations of the silicon GAA devices with different D_{it} are plotted as shown in Fig. 3.3 and D_{it} is extracted by eq. (3.5) and eq. (3.8) at the same time. The D_{it} extracted from

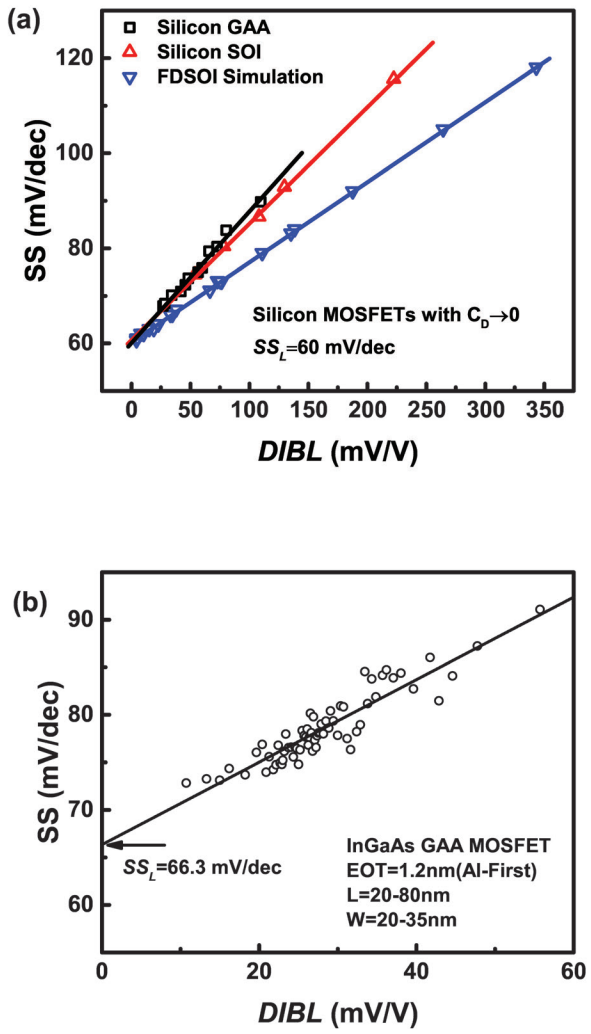

Fig. 3.2. SS versus DIBL of (a) silicon GAA MOSFETs [74], SOI silicon MOSFETs [75], simulation of FDSOI silicon MOSFETs [76], (b) InGaAs GAA MOSFETs (Sample A in [12]). The SS at long channel limit is extracted by linear fitting of SS with respect to DIBL. For (b), SS is extracted at V_{DS}=0.05 V and DIBL is extracted at a constant current in subthreshold region, each data point represents the average of 10 nearby devices.

DIBL-SS relation shows consistent results comparing with D_{it} used in simulation, as shown in TABLE 3.1.

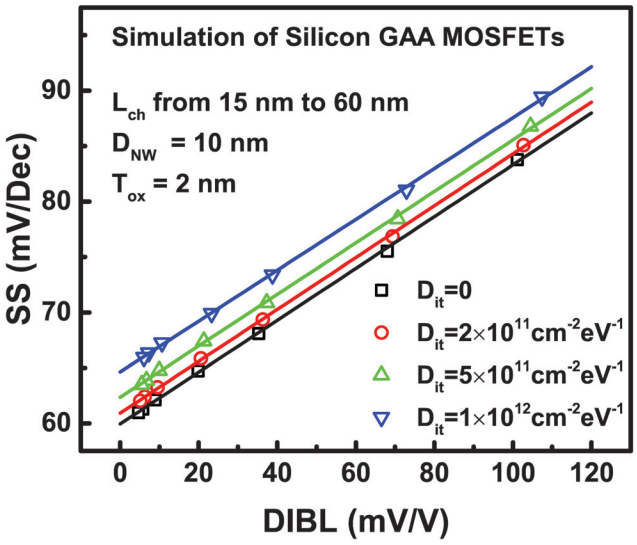

Fig. 3.3. Simulation of SS versus DIBL of silicon GAA MOSFETs with various D_{it} values. The simulated devices have a cylinder silicon nanowire channel with L_{ch} from 15 nm to 60 nm, 10 nm nanowire diameter and with 2 nm SiO_2 as gate dielectric. D_{it} from 0 to 1×10^{12} $eV^{-1}\,cm^{-2}$ are used in simulation.

Table 3.1.
D_{it} extraction results from DIBL-SS relation on simulation data of silicon GAA MOSFETs

D_{it} **in Simulation (in** $eV^{-1}\,cm^{-2}$)	D_{it} **From DIBL-SS relation (in** $eV^{-1}\,cm^{-2}$)
2×10^{11}	1.68×10^{11}
5×10^{11}	4.59×10^{11}
1×10^{12}	8.97×10^{11}

In this work, a simple D_{it} extraction method is introduced for ultra-scaled MOSFETs. The DIBL-SS relation for short channel MOSFETs is derived based on the

capacitor model of 2D electrostatics. The proposed D_{it} extraction method is based on classical subthreshold method but SCEs are eliminated from the DIBL-SS relation by linear fitting of SS with respect to DIBL. The model is shown to be in good agreement with both experimental and simulation results. The proposed D_{it} extraction method provide clear guideline on reliability and radiation effect studies of oxide/semiconductor interfaces on ultra-scaled MOSFETs [77].

3.3 Low Frequency Noise and Random Telegraph Noise on Near-ballistic III-V MOSFETs

Low frequency noise and RTN characterizations can be used as alternate probes to quantitatively analyze performance, variability and reliability of highly scaled devices [78–86]. Furthermore, low noise is required in advanced digital or analog circuit applications so that it is important to systematically study the noise performance and identify noise sources for transistors made of new material systems such as InGaAs MOSFETs. In this work, we report the observation of RTN in highly scaled InGaAs GAA MOSFETs fabricated by a top-down approach. RTN and low frequency noise were systematically studied for devices with various gate dielectrics, channel lengths and nanowire diameters. Mobility fluctuation is identified to be the source of $1/f$ noise. The $1/f$ noise was found to decrease as the channel length scaled down from 80 nm to 20 nm comparing with classical theory, indicating the near-ballistic transport in highly scaled InGaAs GAA MOSFET. Low frequency noise in ballistic transistors is discussed theoretically.

It has been generally admitted that the low frequency noise in MOSFETs can be well described by carrier number fluctuation model or mobility fluctuation model [87]. RTN is attributed to the trapping and de-trapping event in a single defect. $1/f$ noise is the superposition of a number of individual RTNs in the carrier number fluctuation theory. On the other hand, classical theories suggest that $1/f$ noise increases inversely with decreasing channel length [88–95]. If true, this may negate some of the perfor-

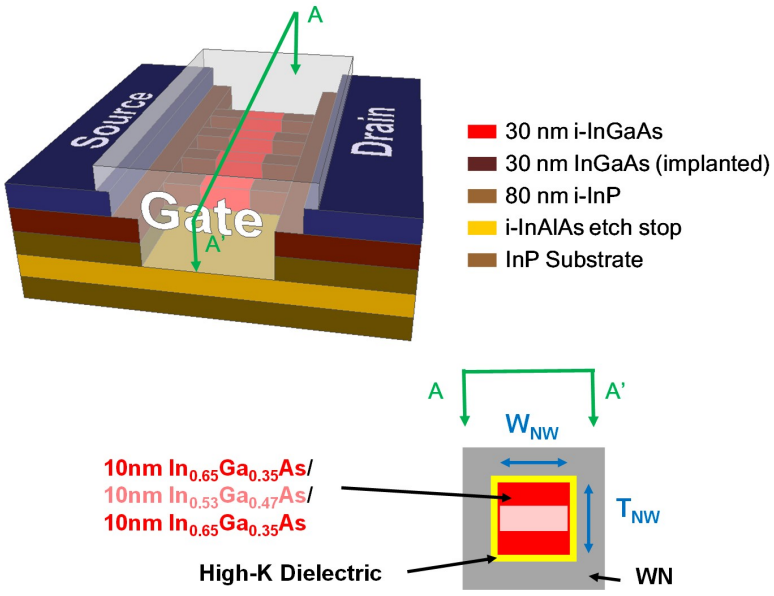

Fig. 3.4. Schematic and cross-section of the present InGaAs GAA MOSFETs.

mance gain of short channel transistors [78–80]. Several groups have recently reported RTN of bottom-up synthesized long-channel InAs nanowire MOSFETs [96–98], and InGaAs FinFETs [99]. However, there havent been any work systematically studies low frequency noise and RTN on highly scaled InGaAs MOSFETs.

Here, this section (i) reports the observation of RTN on top-down fabricated InGaAs GAA MOSFETs, (ii) examines the origin of low frequency noise on highly scaled InGaAs GAA MOSFETs, (iii) systematically studies the property of low frequency noise and RTN characteristics on near-ballistic InGaAs GAA nanowire MOSFETs with nanowire width varying from 20 nm to 35 nm, channel length varying from 20 nm to 80 nm and with various gate dielectrics, (iv) theoretically studies and predict the low frequency noise behavior in transistors working in ballistic limit [86, 100].

Fig. 3.4 shows the schematic diagram and cross-sectional view of an InGaAs GAA MOSFET. The top-down fabrication process can be found in [12]. The samples used for noise characterizations and device dimensions are summarized in Table 3.2.

Table 3.2.
Description of samples and device dimensions

	Sample A (Al_2O_3 first)	**Sample B ($LaAlO_3$ first)**	**Sample C (Al_2O_3 only)**
Channel Material	10 nm $In_{0.65}Ga_{0.35}As$ /10 nm $In_{0.53}Ga_{0.47}As$ /10 nm $In_{0.65}Ga_{0.35}As$		
L_{ch} (nm)	20	20, 30, 50, 80	20
L_{NW} (nm)	200	200	200
W_{NW} (nm)	20	20, 25, 30, 35	20
T_{NW} (nm)	30	30	30
Gate Stack	0.5 nm Al_2O_3 /4 nm $LaAlO_3$	4 nm $LaAlO_3$ /0.5 nm Al_2O_3	3.5 nm Al_2O_3
EOT (nm)	1.2	1.2	1.7

Samples A and B have a 0.5 nm Al_2O_3/4 nm $LaAlO_3$ stack (EOT = 1.2 nm), where Al_2O_3 was grown before $LaAlO_3$ for sample A and vice versa for sample B. Sample C has 3.5 nm Al_2O_3 as gate dielectric (EOT = 1.7 nm). The InGaAs channel layer consists of one 10 nm $In_{0.53}Ga_{0.47}As$ layer sandwiched by two 10 nm $In_{0.65}Ga_{0.35}As$ layers. Devices with L_{ch} varying from 20 nm to 80 nm, W_{NW} varying from 20 nm to 35 nm, T_{NW} of 30 nm and L_{NW} of 200 nm are measured. L_{NW} is the physical length of the nanowire while L_{ch} is the channel length defined by implantation.

Source current power spectral density (S_{I_S}) was measured in the linear region of operation (V_{DS}=50 mV). The gate voltage (V_{GS}) is supplied by a digital controllable voltage source. A Stanford SR570 battery-powered current amplifier is used as source voltage supply and current amplifier for the source current (I_S). I_S is used due to the relatively large junction leakage current in I_D. I_S shows more clearly the fundamen-

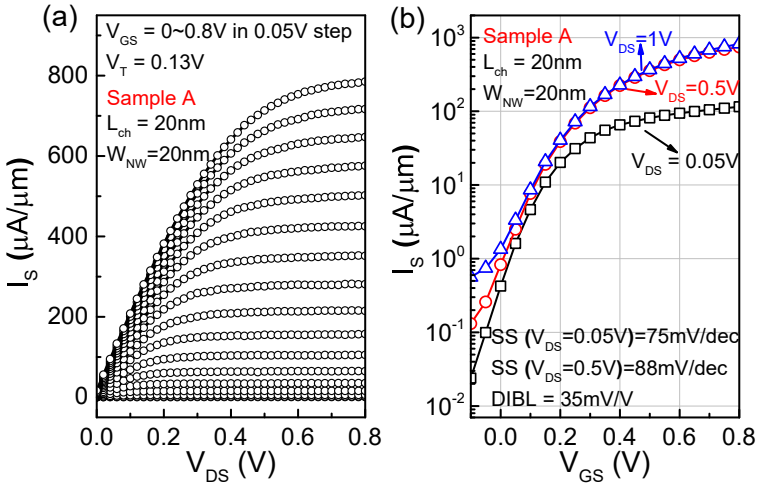

Fig. 3.5. (a) Output and (b) transfer characteristics of a L_{ch}=20 nm InGaAs GAA MOSFET with $Al_2O_3/LaAlO_3$ gate dielectric (Sample A, EOT=1.2 nm) and W_{NW}=20 nm. I_S is used due to relatively large junction leakage current in I_D.

tal transport properties inside the nanowire. The SR570 current amplifier output is directly connected to a Tektronix TDS5032B oscilloscope to record RTN signal and an Agilent 35670A dynamic signal analyzer to obtain the power spectrum density (PSD) of the noise of I_S at the same time. All noise measurements were performed at V_{DS}=50 mV and at V_{GS} from −0.2 V to 0.4 V and at room temperature unless otherwise specified. Positive bias temperature instability (PBTI) measurement confirms that V_T shift less than 10 mV during noise measurement (Maximum V_{GS}=0.4 V) is ensured [86] so that I_S shift is negligible during noise measurement.

Fig. 3.5(a) and 3.5(b) show a typical output and transfer characteristics of a GAA MOSFET measured in this work with L_{ch}=W_{NW}=20 nm. Fig. 3.6(a) and (b) show RTN signals in time domain of an InGaAs GAA MOSFET, with L_{ch}=20 nm, W_{NW}=20 nm and 3.5 nm Al_2O_3 as gate dielectric, at V_{GS}=−0.025 V and V_{GS}=−0.075 V at 15 °C. Two distinct current switching levels are observed, which clearly indicates the existence of a single active trap. Fig. 3.7 shows S_{I_S} normalized

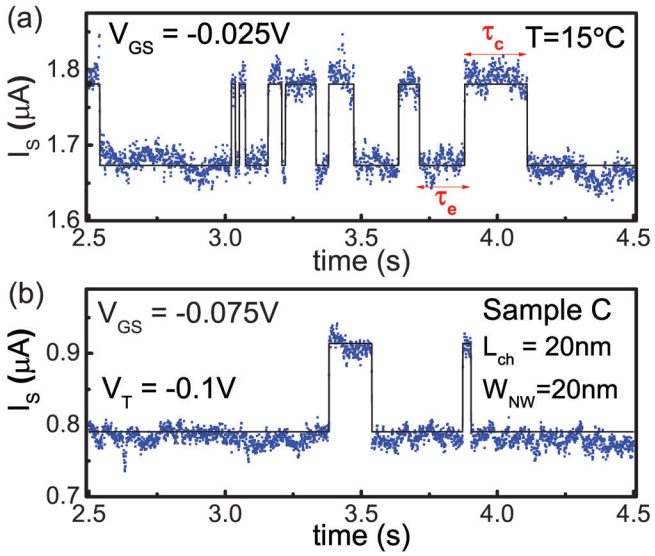

Fig. 3.6. I_S fluctuation due to RTN in (a) V_{GS}=−0.025 V, (b) V_{GS}=−0.075 V on InGaAs GAA MOSFETs measured at 15 °C. Capture/emission time constants (τ_c/τ_e) are defined in (a).

by I_S^2 (i.e., S_{I_S}/I_S^2) of the RTN signal shown in Fig. 3.6(a). A typical Lorentzian spectrum is shown in the noise spectrum with $1/f^2$ characteristics. Clear RTN signals were observed on about 1/3 of devices measured on Sample A, B and C, but only when V_{GS} is near V_T. PSD of devices without RTN signals shows $1/f$ characteristics.

Fig. 3.8 shows (a) I_S histogram and (b) RTN signal in time domain on an L_{ch}=20 nm, W_{NW}=25 nm device of Sample B, (c) a time segment inside (b), showing the superposition of two switching level signal and a Gaussian-like noise. In the device without a RTN signal, the I_S histogram shows only Gaussian-like distribution and with a $1/f$ noise spectrum. This phenomenon suggests the fact that mobility fluctuation (rather than number fluctuation) is the origin of the $1/f$ noise on devices without RTN signal. In classical noise theory, $1/f$ noise in MOSFETs can be well described by carrier number fluctuation model or mobility fluctuation model [87]. For carrier number fluctuation theory, current fluctuation in a MOSFET is attributed to the trapping and de-trapping events within a number of traps which induce V_T

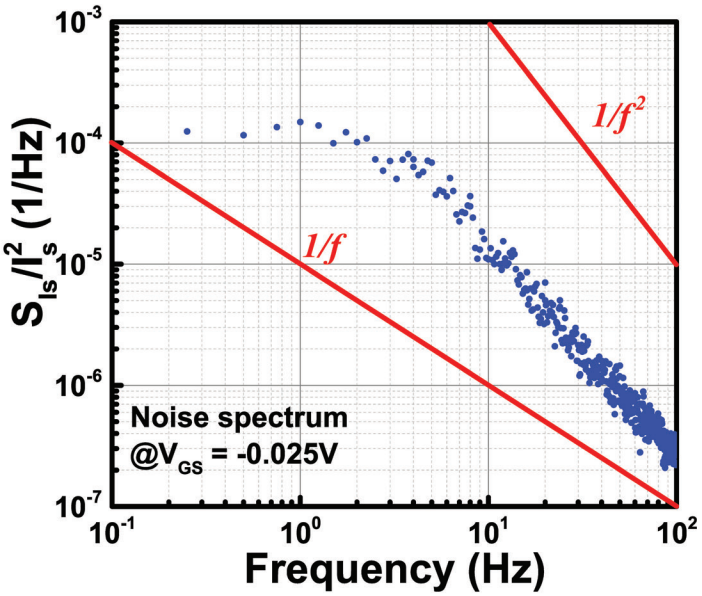

Fig. 3.7. Normalized I_S noise of RTN signal shown in Fig. 3.6(a), showing $1/f^2$ characteristics.

shift. Each individual trapping and de-trapping event has a Lorentzian spectrum, as shown in Fig. 3.7, so-called RTN. The $1/f$ spectrum is the superposition of these Lorentzian spectrums, as suggested by McWorther model [101]. In this work, the number of traps are not likely to be enough to support a $1/f$ spectrum and that explains why RTN is observed. Fig. 3.9 shows the measurement of hysteresis of a typical device of Sample A with L_{ch}=20 nm and W_{NW}=20 nm. By estimating the electron trapping events that are responsible for the hysteresis, we can estimate the number of defects in the oxide. The estimated number of active defects is calculated as $AC_{ox}\Delta V_T/q$, where A is the gate area for the devices, C_{ox} is the gate capacitance calculated from EOT, ΔV_T is the hysteresis V_T shift. ΔV_T of Sample A is on the order of several mV measured with maximum V_{GS}=0.8 V, corresponding to several active traps. Furthermore, not all traps will be effective to the current fluctuation because of distribution of trap energy levels, in other words, not all oxide traps are

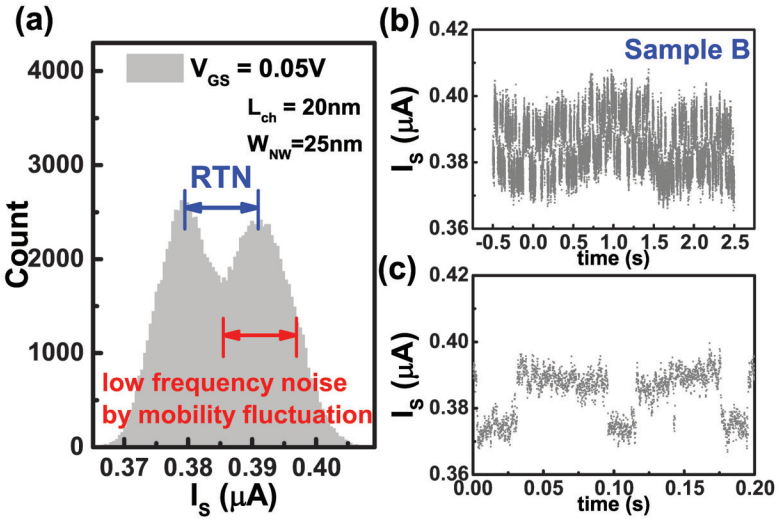

Fig. 3.8. (a) Histogram of a RTN signal of sample B with L_{ch}=20 nm and W_{NW}=25 nm. (b) and (c) RTN signals in time domain of the same signal as (a). (c) is a time segment inside (b).

active at a certain gate voltage. Moreover, the inversion charges in this work is farther from the interface than planar MOSFETs due to the volume inversion nature of GAA MOSFETs, as suggested by simulation results [102]. It could potentially reduce the interaction between oxide traps and inversion charges, as suggested in low frequency noise study in silicon nanowire MOSFETs [94].

Therefore, for those devices with $1/f$ spectrum in which RTN signal cannot be observed, mobility fluctuation is the source of low frequency noise. Fig. 3.10 shows the comparison of noise spectrum between a device with RTN signal and a device without RTN. The two devices share the same device dimension with L_{ch}=20 nm, W_{NW}=25 nm and 3.5 nm Al_2O_3 as gate dielectric. It is clear that noise spectrum of the device without RTN shows $1/f$ characteristic, while the noise spectrum of the device with RTN is the superposition of $1/f$ noise spectrum and a Lorentzian spectrum. This is not the only evidence for the identification of noise source as mobility fluctuation in this work. This fact will be further discussed in the following

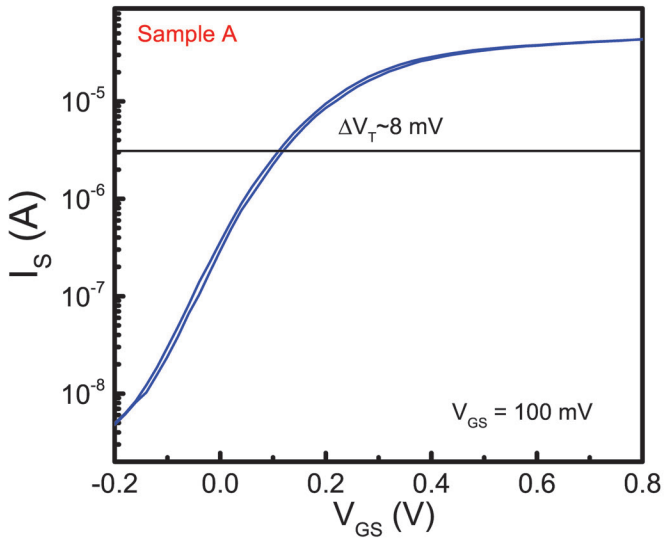

Fig. 3.9. Measurement of hysteresis of a typical device of Sample A with L_{ch}=20 nm and W_{NW}=20 nm. The device shows negligible hysteresis. The estimated trap number by hysteresis is on the order of several traps.

part. Fig. 3.11 shows S_{I_S}/I_S^2 as a function of I_S on Sample A, B and C with L_{ch}=20 nm and W_{NW}=20 nm at f=10 Hz, which is weakly dependent on interface and oxide quality. All the three selected devices show $1/f$ spectrum and no RTN was observed. S_{I_S}/I_S^2 can be modulated by I_S indicates the noise source is from channel rather than series resistance. Meanwhile, S_{I_S}/I_S^2 depends only weakly on types of gate oxide and interface, suggesting that oxide trapping and de-trapping induced carrier number fluctuation might not be the source of low frequency noise in this work.

Fig. 3.12 shows source current power spectrum density normalized by I_S^2 (S_{I_S}/I_S^2) versus I_S at f=10 Hz, W_{NW}=20 nm and various channel lengths for Sample B. S_{I_S}/I_S^2 versus I_S shows weakly dependence on L_{ch}, which is opposite to the classical noise L_{ch} scaling characteristics ($S_{I_S}/I_S^2 \sim 1/L_{ch}$ at a given current). Fig. 3.13 shows the input gate noise (S_{Vg}) normalized by channel area (WLS_{Vg}) vs. I_S. It can be seen clearly that the normalized input noise is reduced by channel length scaling down, while

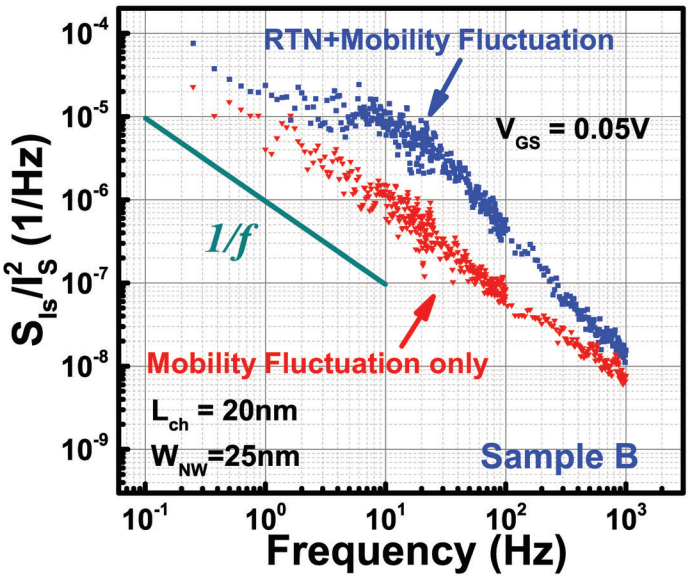

Fig. 3.10. Normalized I_S noise of Sample B devices with RTN signal and without RTN signal. Noise spectrum of device without RTN is attributed to mobility fluctuation.

in classical theory WLS_{Vg} should be independent of channel area. In both classical carrier number fluctuation model and mobility fluctuation model, S_{Vg} and S_{I_S}/I_S^2 is inversely proportional to L_{ch}. The experimental data shows the I_S noise measured in the InGaAs GAA MOSFETs is reduced at short channel devices comparing with classical theory. This phenomenon cannot be explained by carrier number fluctuation theory because the V_T shift caused by a single trapping and de-trapping event can be estimate simply by $\Delta V_T = q/(AC_{ox})$, where A is proportional to L_{ch}. We will have larger ΔV_T at smaller channel length so that amplitude of the single trapping and de-trapping event is increased. As current fluctuation is the combination of a number of single trapping and de-trapping events, noise will be increased while channel length scaling down if carrier number fluctuation noise dominates the S_{I_S}/I_S^2. Thus, the anomalous scaling trend in Fig. 3.12 and Fig. 3.13 also indicate carrier number fluctuation is not the source of $1/f$ noise in the highly scaled InGaAs GAA

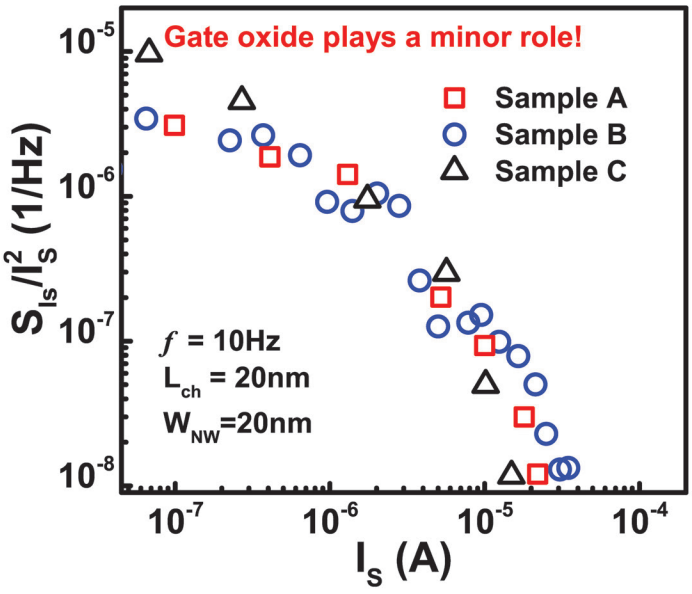

Fig. 3.11. PSD of I_S normalized by I_S^2 vs. I_S at f=10 Hz for Sample A, B and C devices with L_{ch}=20 nm and W_{NW}=20 nm. Devices with different gate oxides exhibit similar noise level, showing weakly dependent on interfaces and types of oxides.

MOSFETs. In classical theory of noise sources diagnosis, S_{I_S}/I_S^2 is proportional to $(g_m/I_S)^2$ for carrier number fluctuation while S_{I_S}/I_S^2 is proportional to $1/I_S$ in mobility fluctuation theory [103]. However, there haven't been any theoretical study on whether this diagnosis will still work on ballistic or near-ballistic transistors. In this work, the slope of S_{I_S}/I_S^2 versus I_S is extracted in Fig. 3.12 to be -1.3, which is close to -1, by linear fitting of all the measured data in log-log plot from weak inversion to on-state. But it is still open to question that whether classical theory on this slope still to be correct in near-ballistic regime. The Hooges parameter is estimated as 3×10^{-4}-1.2×10^{-3} depending on the channel length [104].

This weak dependence of S_{I_S}/I_S^2 versus I_S on L_{ch} leads to the conclusion of this work that the near-ballistic transport of electrons in the channel is achieved through noise study. Although mobility fluctuation model also suggests $1/L_{ch}$ scaling met-

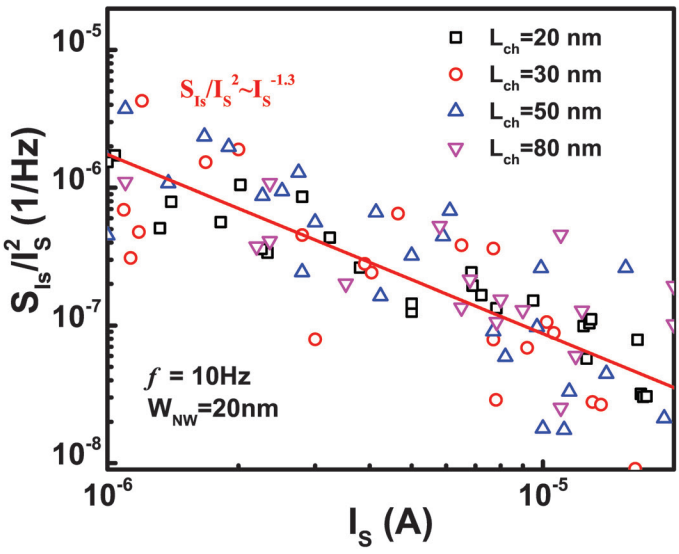

Fig. 3.12. PSD of I_S normalized by I_S^2 at f=10 Hz for various L_{ch} and W_{NW}=20 nm at V_{DS}=0.05 V on Sample B. Normalized I_S noise versus I_S of devices with different L_{ch} weakly depend on interfaces and types of oxides. At least 5 devices are measured for each L_{ch}, showing a statistical trend.

rics for S_{I_S}/I_S^2, this conclusion might not be the truth in devices with short channel length and long mean free path in high mobility channel materials. As electrons from source cannot equilibrate to lattice temperature immediately at drain contact, the classical mobility fluctuation model, which assumes uniform carrier distribution and diffusive transport, is no longer valid. In our near-ballistic InGaAs GAA MOSFETs, electrons encounter less scattering at smaller L_{ch} during transport from source to drain. Therefore, scattering induced mobility fluctuation decreases at small L_{ch} so that normalized I_S noise is reduced at small L_{ch} comparing with the prediction of classical theory. This property also confirms that mobility fluctuation is the origin of low frequency noise for highly scaled InGaAs MOSFETs. To confirm the transport property of the devices, an ultra-fast high resolution thermo-reflectance imaging technique is applied to image the local surface temperature of the InGaAs GAA devices [105]. Fig. 3.14 shows the top-view thermo-reflectance image on an InGaAs

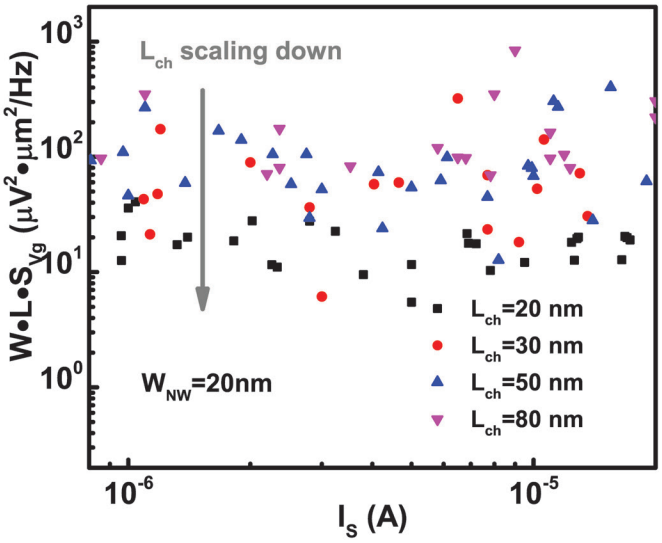

Fig. 3.13. Input gate voltage noise normalized by channel width times channel length of the same data set as Fig. 3.12. W is the channel width and L is the channel length in this figure.

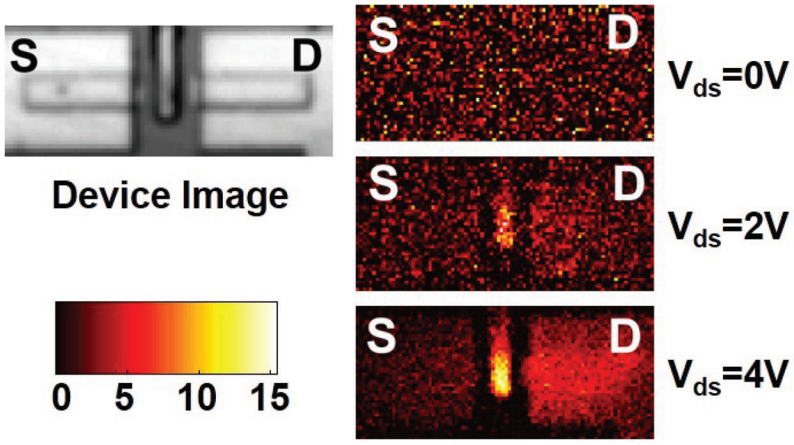

Fig. 3.14. Thermo-reflectance image on an InGaAs GAA MOSFET with L_{ch}=80 nm, W_{NW}=30 nm at V_{GS}=1 V and at V_{DS} from 1 V to 4 V. Color scale shows the temperature difference (ΔT) in kelvin. The drain side is heated at high V_{DS} by ballistic electrons, indicating that electrons travel substantial distance into the contact before reaching equilibrium which indicates near-ballistic transport.

GAA MOSFET with L_{ch}=80 nm, W_{NW}=30 nm at V_{GS}=1 V and V_{DS} varying from 0 V to 4 V. The drain side is heated at high V_{DS} by ballistic electrons, indicating that electrons travel substantial distance into the drain contact before reaching equilibrium with the lattice. It supports the conclusion of Fig. 3.12 and Fig. 3.13 that InGaAs GAA MOSFETs in this work are near-ballistic. Hot Carrier Injection (HCI) measurement on Sample C shows HCI degradation is weakly dependent on L_{ch} because less electrons would interact with interface and oxide at the end of channel. It further confirms the near-ballistic transport in the devices as we reported in [106].

To further understand the low frequency noise behavior in near-ballistic MOSFETs, low frequency noise is theoretically studied in ballistic transistors. In principle, in a ballistic MOSFETs, electrons transport from source to the drain without any scattering processes and then equilibrate to lattice temperature at drain contact. Therefore, mobility fluctuation will not happen inside the channel of ballistic transistors. There have been theoretical and experimental study on long channel carbon nanotube ballistic transistor [107, 108]. Carrier number fluctuation is proposed to dominate the $1/f$ noise in the long-channel (600 nm) carbon nanotube transistors because the large number of defects inside the gate oxide. However, this theory will not be applied in the short channel III-V MOSFETs because the highly scaled channel length make it impossible to have enough number of defects in gate oxide to have a $1/f$ noise spectrum. In this work, low frequency noise in ballistic transistors with no trapping and de-trapping events in gate oxide is studied. In ideal case, if there are no active defects meanwhile no scattering process inside channel, there will be no current fluctuation with fixed V_{GS} and V_{DS} in an ideal ballistic transistor. However, as R_{SD} exists in every transistor and resistor noise also has a $1/f$ noise spectrum, current fluctuation from series resistor is one the noise source in ballistic transistors. The noise originating from S/D resistances can be modeled as the combination of mobility fluctuation noise and thermal noise. Thermal noise can be negligible in low frequency noise analysis because it is independent of frequency in noise spectrum. As R_{SD} is fluctuated, the V_{GS} and V_{DS} of the ballistic transistor will also be fluctuating.

Thus, it is important to understand the effect of R_{SD} on the low frequency noise of ballistic transistors. If we consider R_{SD} and ballistic transistor together, the total source current PSD can be expressed as [87],

$$S_{I_S} = \frac{S_{I_{ch}} + g_{ch}^2 R_D^2 S_{I_{R_D}} + R_S^2 (\mathrm{g}_m + g_{ch})^2 S_{I_{R_S}})}{[1 + \mathrm{g}_m R_S + g_{ch}(R_S + R_D)]^2} \tag{3.9}$$

where $S_{I_{ch}}$ is the source current PSD inside channel, $S_{I_{R_D}}$ is the source current PSD in drain series resistance (R_D), $S_{I_{R_S}}$ is the source current PSD in source series resistance (R_S), g_{ch} is the channel conductance and g_m is the transconductance. If we consider ballistic transistor and symmetric S/D so that $S_{I_{ch}}$=0, R_S=R_D=$R_{SD}/2$ and $S_{I_{R_S}}$=$S_{I_{R_D}}$=$2S_{I_{R_{SD}}}$, eq. (3.9) becomes

$$S_{I_S} = \frac{R_{SD}^2 [g_{ch}^2 + (\mathrm{g}_m + g_{ch})^2] S_{I_{R_{SD}}}}{2[1 + (\mathrm{g}_m + 2g_{ch}) R_{SD}/2]^2} = \beta S_{I_{R_{SD}}} = \frac{\beta \alpha_H I_S^2}{fN}, \tag{3.10a}$$

$$\beta = \frac{R_{SD}^2 [g_{ch}^2 + (\mathrm{g}_m + g_{ch})^2]}{2[1 + (\mathrm{g}_m + 2g_{ch}) R_{SD}/2]^2}, \tag{3.10b}$$

$$\frac{S_{I_S}}{I_S^2} = \frac{\alpha_H}{fN} \tag{3.10c}$$

where we consider $S_{I_{R_{SD}}}$=$\frac{\alpha_H I_S^2}{fN}$, α_H is the Hooge parameter and N is the number of carriers in S/D region [104]. Thus, in ballistic transistors, S_{I_S}/I_S^2 will be independent of L_{ch}. If $(\mathrm{g}_m + 2g_{ch})R_{SD}/2 \gg 1$, S_{I_S}/I_S^2 is independent on I_S to the zeroth order approximation. If $(\mathrm{g}_m + 2g_{ch})R_{SD}/2 \ll 1$, S_{I_S}/I_S^2 has a positive correlation with I_S. Fig. 3.15 shows the relation between S_{I_S}/I_S^2 and I_S/V_{DS} in an InGaAs GAA MOSFETs with L_{ch}=20 nm, W_{NW}=25 nm and at V_{DS} from 0.1 V to 0.5 V. S_{I_S}/I_S^2 is plotted versus I_S/V_{DS} because S_{I_S}/I_S^2 is inversely proportional to I_S/V_{DS} in mobility fluctuation model of MOSFETs [87]. S_{I_S}/I_S^2 shows weaker negative correlation with I_S/V_{DS} as V_{DS} increases. This phenomenon suggests noise from series resistance has a higher contribution to the source current noise as V_{DS} increases. In near-ballistic transistors, ballistic efficiency at high V_{DS} increases which reduces the noise from the channel so that low frequency noise depends more on the series resistance.

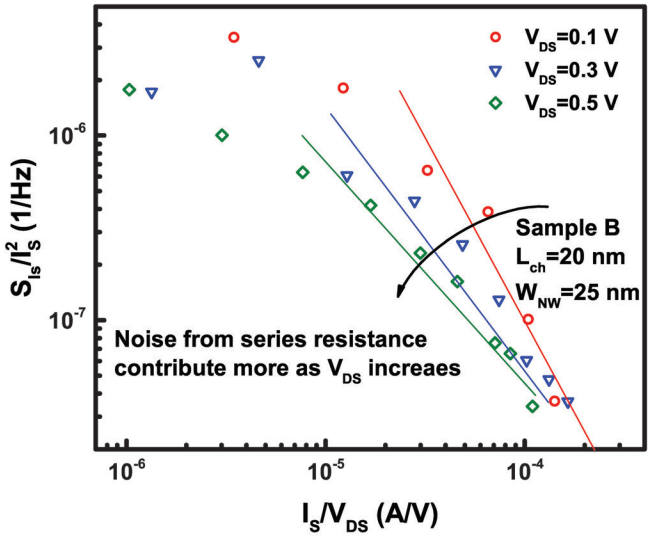

Fig. 3.15. S_{I_S}/I_S^2 vs. I_S/V_{DS} at different V_{DS}. S_{I_S}/I_S^2 shows weaker negative correlation with I_S/V_{DS} as V_{DS} increases. This phenomenon suggests noise from series resistance has a higher contribution to the source current noise as V_{DS} increases.

Classical number fluctuation and mobility fluctuation theory was setup based on diffusive transport assumption. In diffusive assumption, electrons are in thermal-equilibrium while in ballistic transistors, electron transport is a non-equilibrium process. In particular, electrons equilibrate to the lattice temperature at drain side. We should identify that if this non-equilibrium process is the source of $1/f$ noise in the near-ballistic transistors. To achieve this goal, noise measurement is performed before and after hot carrier injection (HCI) stress. HCI degradation study on InGaAs GAA MOSFETs suggests that the maximum damage condition is at $V_{GS} \sim V_{DS}$ [106]. In this work, V_{GS}=2 V and V_{DS}=2 V is applied as HCI stress for 1×10^4 s to generate defects by the injection of hot electrons into drain side. The generated defects will interact with electrons in the relaxation process at drain side. Fig. 3.16 shows (a) transfer characteristics and (b) S_{I_S}/I_S^2 versus I_S of an InGaAs GAA MOSFET before and after HCI stress. The PSD of I_S shows similar level on fresh device and stressed

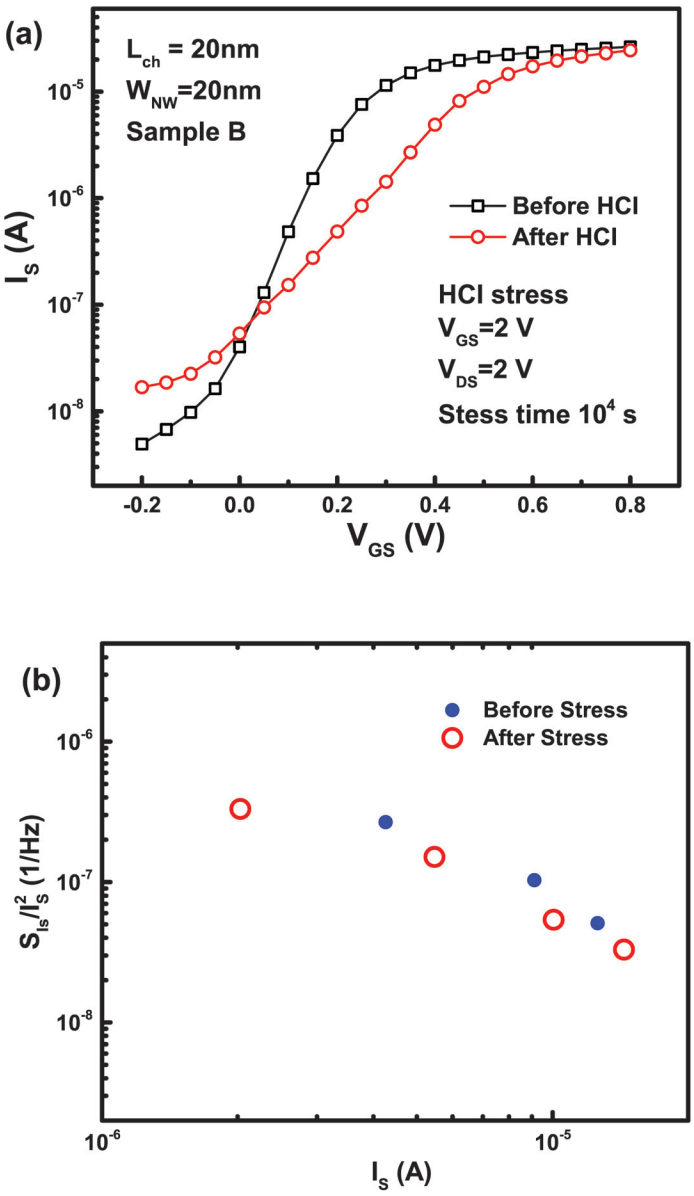

Fig. 3.16. (a) Transfer characteristics of an L_{ch}=20 nm, W_{NW}=20 nm device of Sample B, fresh device (square) and after V_{GS}=2 V, V_{DS}=2 V stress for 1×10^4 s (circle). (b) S_{I_S}/I_S^2 vs. I_S of the device in (a) before stress and after stress measured at V_{DS}=0.05 V. Although defects are generated at drain side, the PSD of I_S shows similar level on fresh device and stressed device.

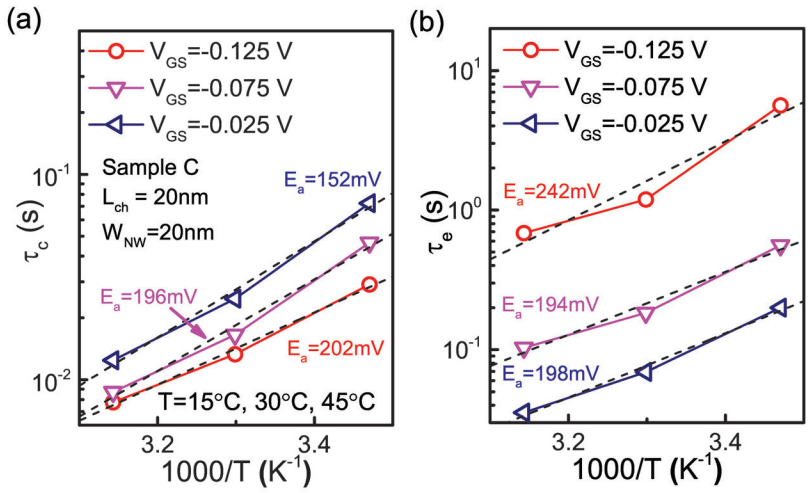

Fig. 3.17. Temperature dependent (a) capture and (b) emission time constant of RTN in device shown in Fig. 3.6.

device, indicating the relaxation of electrons at drain side is not the source of $1/f$ noise.

In Figs. 3.17 and 3.18, the time domain characteristics of RTN in the same condition as in Fig. 3.6 from V_{GS}=−0.15 V to 0 V are studied. Capture time constant (τ_c) is defined as time duration in the lower state while emission time constant (τ_e) is defined as time duration in the higher state, as shown in Fig. 3.6(a). Fig. 3.17 shows the relation between time constants and the reciprocal of temperature ($1000/T$). τ_c and τ_e are extracted at 15 °C, 30 °C and 45 °C and the activation energy (E_a) is extracted by linear extrapolation of $\ln(\tau_c$ or $\tau_e)$ vs. $1/kT$. Both τ_c and τ_e are reduced by increasing the temperature, suggesting thermal emission contributes to the trapping and de-trapping event in $LaAlO_3$/InGaAs or Al_2O_3/InGaAs systems. Fig. 3.18(a) shows the relation between τ_c, τ_e and V_{GS}. Fig. 3.18(b) studies the relation between τ_c/τ_e and V_{GS}. The positive correlation between τ_c/τ_e and V_{GS} indicates electrons trapping and de-trapping happen between channel and gate oxide rather than between gate metal and gate oxide, as suggested in [85].

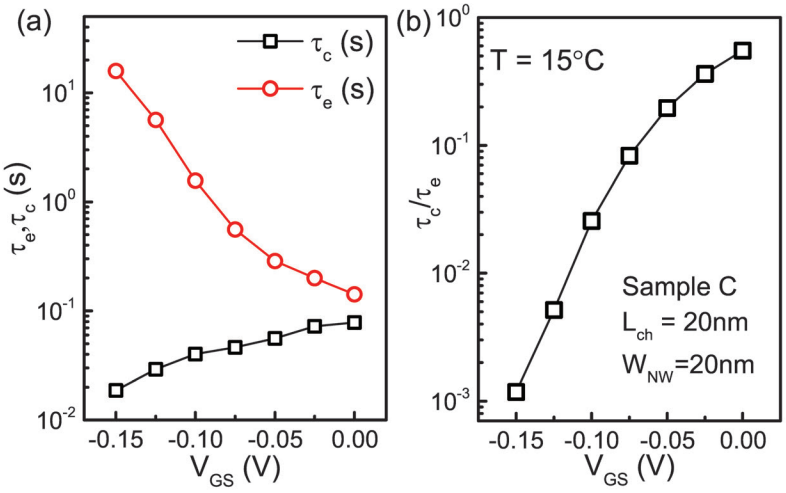

Fig. 3.18. (a) Mean capture and emission time constant corresponding to different gate voltages. (b) τ_c/τ_e dependence on V_{GS}. The positive correlation indicates electron trapping happens between channel and gate oxide.

In conclusion, low frequency noise and RTN in highly scaled InGaAs GAA MOSFETs are systematically studied. For highly scaled InGaAs GAA MOSFETs, both number fluctuation and mobility fluctuation exist in the low frequency current fluctuation. Noise from number fluctuation typically is random telegraph noise because the lack of defects to support a $1/f$ spectrum. Mobility fluctuation is confirmed to be the source of $1/f$ noise of devices without RTN or at high V_{GS}. It is experimentally observed that low frequency noise is suppressed at shorter channel length due to the near-ballistic transport at this length scale. The short channel length, long mean free path (high mobility) and volume inversion nature of InGaAs GAA structure are believed to be the origin of the noise reduction in the devices of this work. The reduced low frequency noise in highly scaled InGaAs MOSFETs suggests their potential for low noise MOSFET applications. Low frequency noise is also studied in ballistic transistors and series resistance plays an importance role in the low frequency noise of ballistic transistors with negligible oxide defects. RTN is observed on

top-down InGaAs GAA MOSFETs and only around threshold voltage because RTN is negligible comparing with mobility fluctuation induced noise at high V_{GS}.

4. III-V TUNNELING FIELD-EFFECT TRANSISTORS

4.1 Introduction

The motivation of steep-slope transistors and the working mechanism of TFETs for steep-slope switching have already been discussed in section 1.3 and 1.5. In this chapter, section 4.2 discusses planar TFETs made of III-V materials by Zn diffusion and the scaling metrics. Section 4.3 discusses the impact of 3D structure on the performance of InGaAs TFETs.

4.2 Channel Length Scaling of Planar InGaAs Tunnel Field-effect Transistors

TFETs are considered as strong candidates for low power CMOS applications in future technology node because of the potential for sub-60 mV/dec operation at room temperature [13, 38, 109–122]. InGaAs is a material gaining interest due to its high tunneling efficiency [38, 113–117]. SS down to 60 mV/dec has been demonstrated on InGaAs planar TFET based on a CMOS compatible Zn diffusion process technology [115, 116]. Meanwhile, deep sub-100 nm L_{ch} is requested for real device applications. At the same time, the understanding of low frequency noise and RTN for small dimension devices are important as RTN only can be observed in scaled devices for MOSFETs. However, there were no reports on RTN and any scaling metrics studies of InGaAs TFETs and no sub-micrometer planar-type InGaAs TFETs were demonstrated. In this section, InGaAs TFETs are fabricated with L_{ch} from 20 µm down to 75 nm and with ALD Al_2O_3 as gate dielectric from 8 nm down to 2.3 nm (EOT from 3.9 nm to 1.2 nm). RTN is observed on InGaAs TFETs for the first time on almost all L_{ch} devices. RTN is found to originate from electron trapping

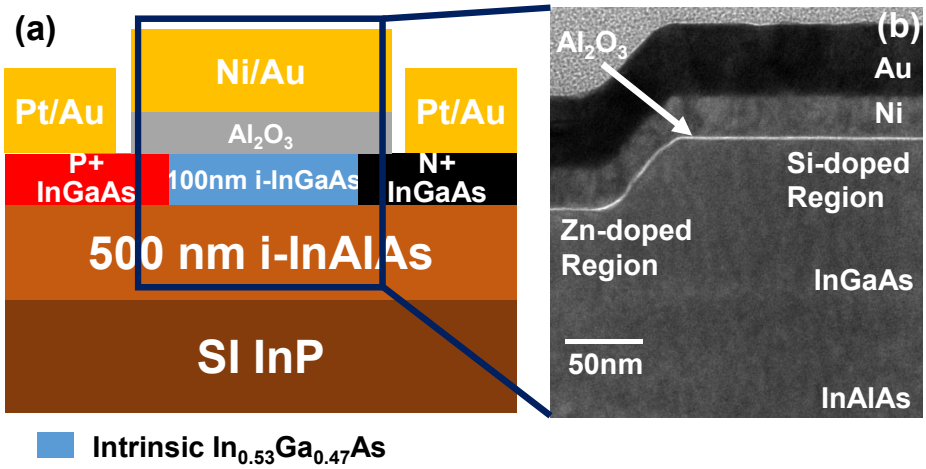

Fig. 4.1. (a) Schematic diagram and (b) TEM cross-sectional image of an InGaAs planar TFET.

and de-trapping near source-channel junction because it is weakly dependent on L_{ch} and this is also confirmed from SS reduction in fast I-V measurement. A detailed scaling metrics study (SS, DIBL, V_T, I_{ON}, g_m) are carried out, showing immunity to SCEs with scaled EOT and well-behaved device performance down to sub-100 nm and better immunity to SCEs comparing with InGaAs planar MOSFETs with lightly p-doped channel.

Fig. 4.1 shows the (a) schematic diagram and (b) TEM cross-sectional image of a fabricated InGaAs planar TFET. The device fabrication process flow is shown in Fig. 4.2. The 500 nm intrinsic InAlAs and 100 nm intrinsic $In_{0.53}Ga_{0.47}As$ layers were epitaxially grown on semi-insulating (100) InP substrates as starting material. After solvent clean and $(NH_4)_2S$ pretreatment, 10 nm Al_2O_3 was grown by ALD at 300 °C as an encapsulation layer and diffusion mask for Zn diffusion. Source and drain Si implantation was then performed at 20 keV with a dose of 1×10^{14} cm^{-2}

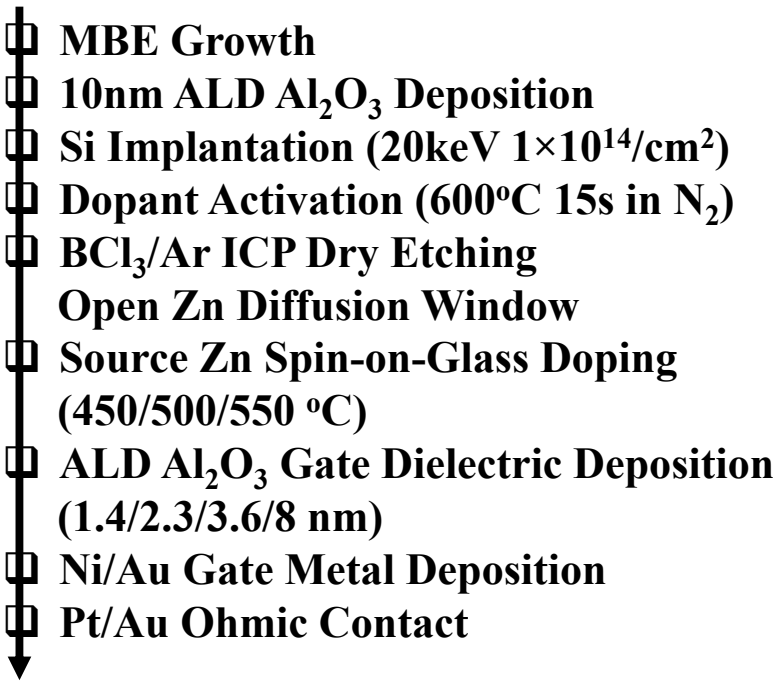

Fig. 4.2. Fabrication process flow for the InGaAs TFET.

followed by dopant activation at 600 °C for 15 s in N_2. After source patterning using diluted ZEP520A and BCl_3/Ar based dry etching, the 10 nm Al_2O_3 was removed in selected area as open window for Zn diffusion. Dry etching is preferred here to avoid undercut in wet etching process so that short channel devices can be achieved. Zn-doped spin-on-glass (SOG) was then spinned on top of the wafer followed by RTA in N_2 at 450/500/550 °C for 1 min. Zn-doped p+ InGaAs region is etched down partly because of the less selective dry etching process and oxidation from O_2 in SOG during Zn diffusion process [115]. After SOG and Al_2O_3 removal in diluted BOE:H_2O=1:5 solution for 10 min and 10 min passivation in 10% $(NH_4)_2S$, 2.3/3.6/8 nm Al_2O_3 were grown by ALD at 250 °C as gate dielectric. Then, Ni/Au was deposited as the gate and Pt/Au Ohmic contacts were formed for both source and drain. All RTN measurements are done in same setup as [100].

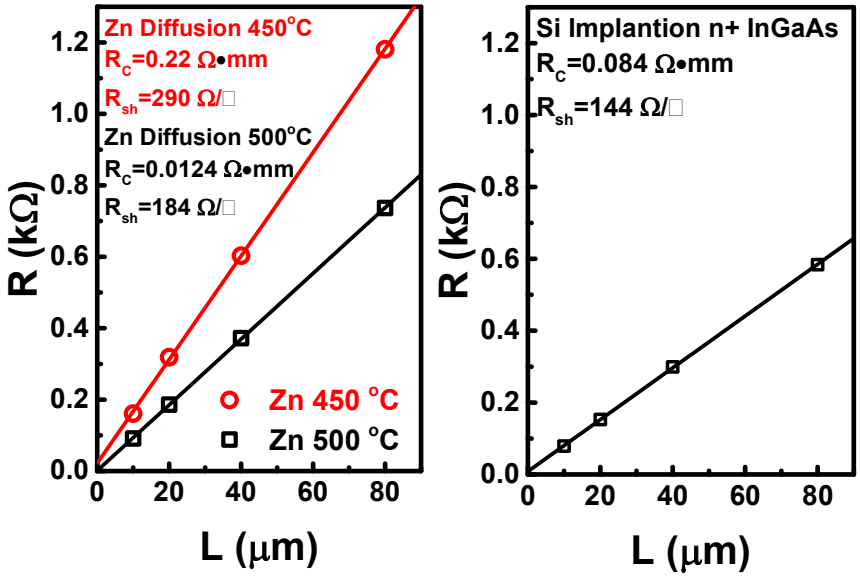

Fig. 4.3. TLM measurement on doped InGaAs by (a) Zn diffusion and (b) Si implantation.

Fig. 4.3 shows the TLM measurements of (a) Zn-doped p+ InGaAs with Pt/Au contact (b) Si Implanted n+ InGaAs with Pt/Au contact. The p+ InGaAs is doped through Zn diffusion from Zn-doped SOG at 450 °C and 500 °C. Both n-type and p-type TLMs were fabricated together along with InGaAs TFET devices. Contact resistance (R_C) is extracted to be 0.22 Ω mm for Zn diffusion at 450 °C and 0.0124 Ω mm for Zn diffusion at 500 °C, showing comparable results comparing with R_C=0.084 Ω mm for n+ InGaAs formed by Si implantation and with Pt/Au contact. Sheet resistance (R_{sh}) is extracted to be 290 Ω/□ for Zn diffusion at 450 °C, 184 Ω/□ for Zn diffusion at 500 °C and 144 Ω/□ for n+ InGaAs formed by Si implantation. Although R_C and R_{sh} are larger for Zn diffusion at 450 °C than for Zn diffusion at 500 °C, the resistance is still small enough for the InGaAs TFET devices as discussed in on-state scaling metrics in the following.

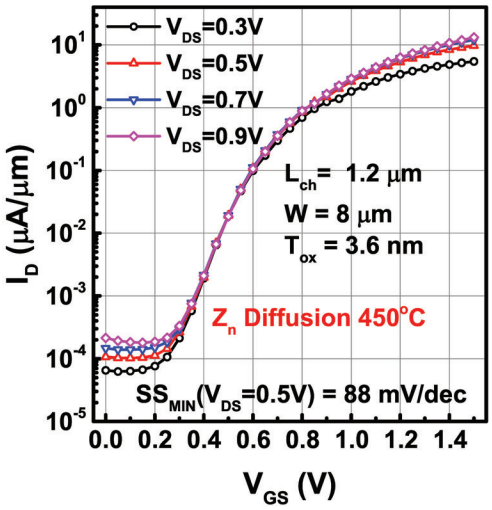

Fig. 4.4. Transfer characteristics of an InGaAs TFET with L_{ch}=1.2 µm and 3.6 nm Al_2O_3 (EOT=1.8 nm) as dielectric. P+ region is doped through Zn Diffusion at 450 °C.

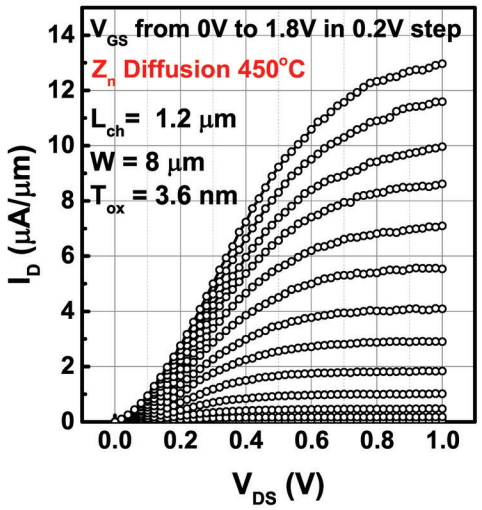

Fig. 4.5. Output characteristics of the same device shown in Fig. 4.4.

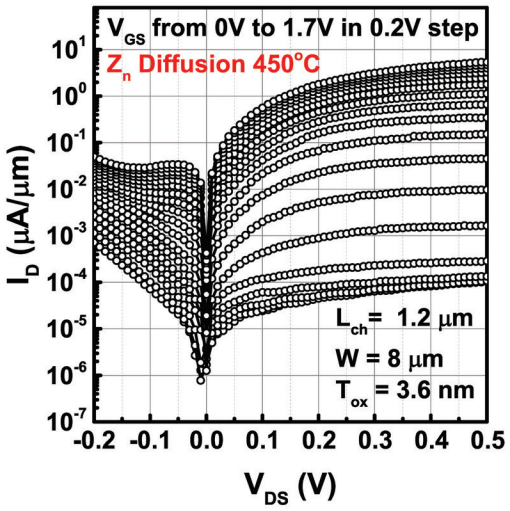

Fig. 4.6. Output characteristics in log-scale of the same device shown in Fig. 4.4. Negative differential resistance is observed in negative V_{DS} region.

Figs. 4.4-4.6 show the transfer and output characteristics of a well-behaved InGaAs TFET with L_{ch}=1.2 µm, channel width = 8 µm and oxide thickness =3.6 nm (EOT=1.8 nm). This device shows subthreshold slope (SS) of 88 mV/dec at V_{DS}=0.5 V and negligible DIBL. DIBL in this work is defined as threshold voltage shift per V_{DS} change at constant current (10 nA/µm). Negative differential resistance (NDR) is observed where V_{DS} changes to negative bias in Fig. 4.6, indicating tunneling is the dominated electron transport mechanism.

Fig 4.7 shows two typical RTN signals measured on InGaAs planar TFET, with (a) L_{ch}=600 nm, (b) L_{ch}=100 nm, both the devices have 2.3 nm Al_2O_3 as gate dielectric. It is not shown here but RTN signals are widely observed on all channel lengths, indicating traps near the source/channel junction (p+i junction) contribute to the RTN phenomena. Typical time constants observed are on the order of from ms to s.

Fig. 4.8 shows SS (V_{DS}=0.5 V) scaling metrics for InGaAs planar TFET with 8 nm Al_2O_3 as gate dielectric with L_{ch} down to 100 nm. Note that L_{ch} here is the

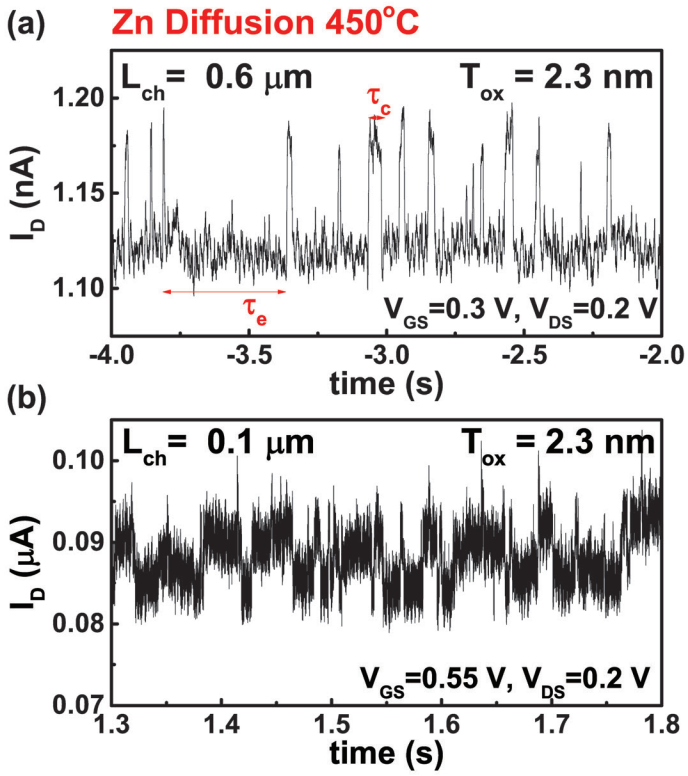

Fig. 4.7. I_D fluctuation due to RTN in (a) InGaAs TFET with L_{ch}=0.6 µm (b) InGaAs TFET with L_{ch}=0.1 µm.

mask gap length between n+ drain and p+ source. As Zn diffusion during annealing, the actually channel length is smaller than that defined by lithography masks. It is shown that SCEs start to appear at longer L_{ch} at higher Zn diffusion temperature because Zn diffuses faster at higher temperature. This observation indicates that to make short channel devices, we have to keep Zn diffuses slow. As a result, the smallest L_{ch} (75 nm) with functional device in this work is achieved using 450 °C Zn diffusion. Figs. 4.9-4.11 shows SS at V_{DS}=0.5 V, DIBL and V_T scaling metrics for InGaAs planar TFETs using 450 °C Zn diffusion and with EOT from 3.9 nm to 1.2 nm. V_T is defined as V_{GS} where I_D=100 nA/µm here. It is shown that InGaAs TFETs with smaller EOT show better immunity to SCEs than larger EOT ones.

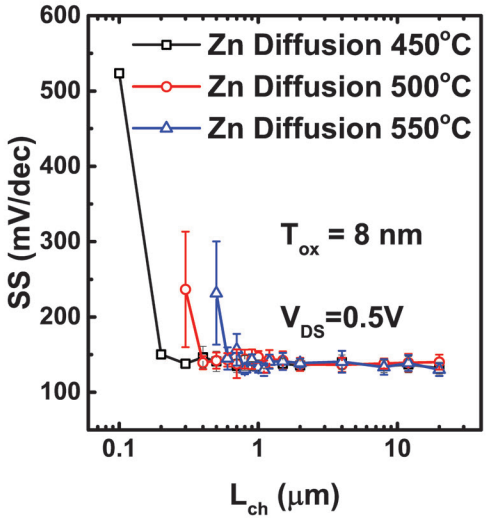

Fig. 4.8. SS scaling metrics for InGaAs TFET with 8 nm Al_2O_3 as gate dielectric and p+ region is doped by Zn diffusion from 450 °C to 550 °C.

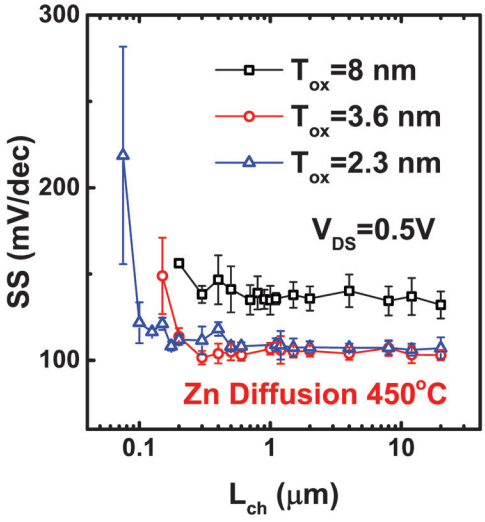

Fig. 4.9. SS scaling metrics for InGaAs TFETs with 2.3 nm to 8 nm Al_2O_3 as gate dielectric and p+ region is doped by Zn diffusion from 450 °C.

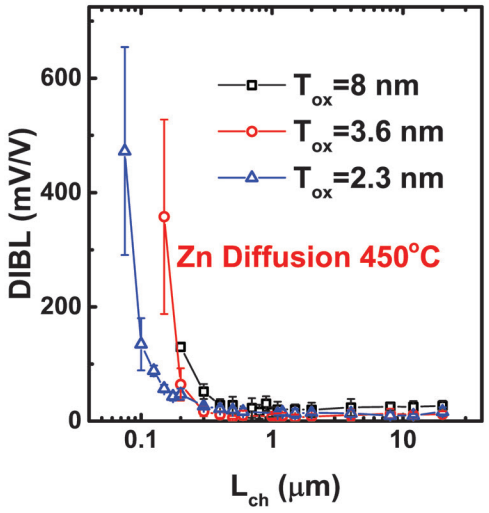

Fig. 4.10. DIBL scaling metrics for InGaAs TFETs with 2.3 nm to 8 nm Al_2O_3 as gate dielectric and p+ region is doped by Zn diffusion from 450 °C.

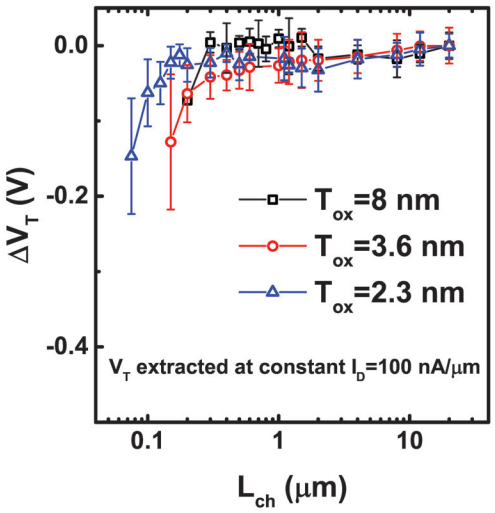

Fig. 4.11. V_T roll-off for InGaAs TFETs with 2.3 nm to 8 nm Al_2O_3 as gate dielectric and p+ region is doped by Zn diffusion at 450 °C.

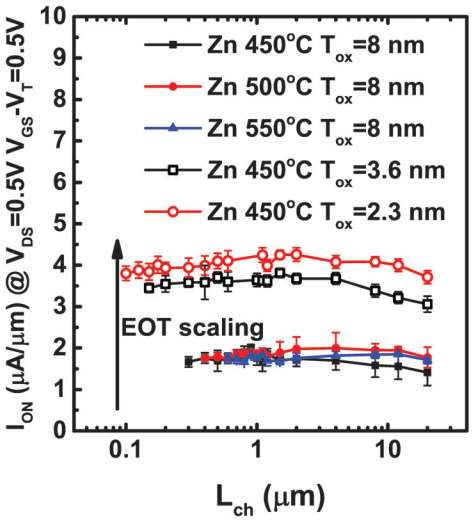

Fig. 4.12. I_{ON} scaling metrics for InGaAs TFETs with 2.3 nm to 8 nm Al_2O_3 as gate dielectric and p+ region is doped by Zn diffusion from 450 °C to 550 °C.

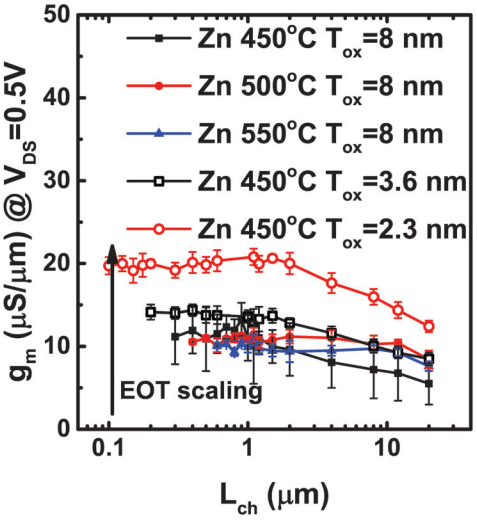

Fig. 4.13. Maximum g_m scaling metrics for InGaAs TFETs with 2.3 nm to 8 nm Al_2O_3 as gate dielectric.

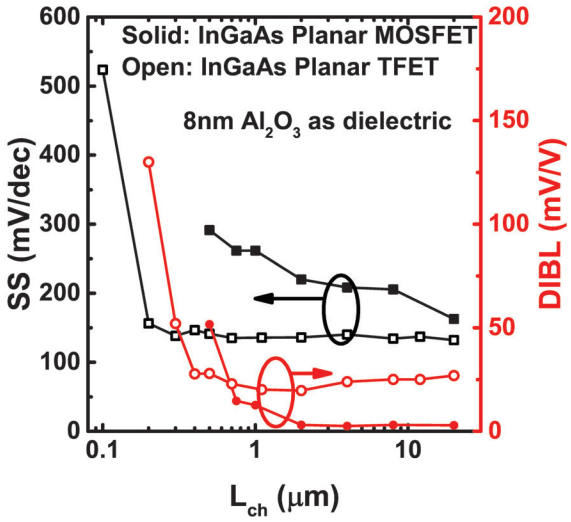

Fig. 4.14. Comparison of SS scaling metrics between InGaAs TFETs and InGaAs planar MOSFETs with 8 nm Al_2O_3 as gate dielectric. The InGaAs planar MOSFETs has a lightly doped channel with N_A=1×10^{17} cm^{-3}.

Figs. 4.12-4.13 show I_{ON} at V_{DS}=0.5 V and $V_{GS} - V_T$=0.5 V and maximum g_m at V_{DS}=0.5 V scaling metrics for InGaAs planar TFETs using 450 °C Zn diffusion and with EOT from 3.9 nm to 1.2 nm. It is found I_{ON} and maximum g_m are improved significantly after EOT scaling. It is also shown that Zn diffusion temperature doesn't play an important role at short channel devices but it is important for long channel devices. This is because of R_{sh} induced R_{SD} difference, at short channel device the impact of R_{SD} become smaller due to shorter source/drain extensions. As a result, on-state performance in short channel devices has weak dependence on Zn diffusion temperature. Fig. 4.14 shows SS and DIBL comparison between InGaAs planar TFETs in this work and InGaAs planar MOSFETs [123] with lightly doped p-type channel with acceptor density (N_A)=1×10^{17} cm^{-3}. The TFETs and MOSFETs both use 8 nm Al_2O_3 as gate dielectric. It is found TFET structure have stronger immunity to SCEs than MOSFETs. In the MOSFETs, SCEs start to be observed at L_{ch} ~1 µm while in the TFETs it is 200-300 nm.

In summary, the scaling properties of InGaAs planar TFETs are systematically studied. RTN is observed on InGaAs TFET on both long channel and short channel devices for the first time. RTN is found to origin from trapping and de-trapping near source-channel junction so that weakly dependent on L_{ch}. EOT scaling is confirmed to improve both the on-state and off-state performance and reduce SCEs. It is found InGaAs planar TFET has better immunity to SCEs comparing with InGaAs planar MOSFETs.

4.3 3D Gate-all-around InGaAs Tunnel Field-effect Transistors

3D MOSFETs such as FinFETs and GAA MOSFETs are well known to offer better gate control so that they have better immunity to the short channel effects. Therefore, by using such structures in TFETs, the performance of TFETs in both on- and off-states can be enhanced [121,124]. In this section, 3D InGaAs GAA TFETs are fabricated and studied with different nanowire dimensions. It is found that InGaAs GAA TFETs with smaller W_{NW} have smaller SS, larger I_{ON} and g_m, showing both on- and off-state performance improvement, suggesting InGaAs 3D TFETs are promising for future low power and high speed logic applications.

Fig. 4.15 shows the (a) cross-sectional view and (b) top view schematic diagram a fabricated InGaAs gate-all-around TFET. The device fabrication process flow is shown in Fig. 4.16. The starting material was a 2 inch semi-insulating (100) InP substrate. InP buffer layer and 50 nm intrinsic $In_{0.53}Ga_{0.47}As$ layers were epitaxially grown by MBE. After solvent clean and $(NH_4)_2S$ pretreatment, 10 nm Al_2O_3 was grown by ALD at 300 °C as an encapsulation layer and diffusion mask for Zn diffusion. Source and drain Si implantation was then performed at 20 keV with a dose of $1 \times 10^{14}\,cm^{-2}$ followed by dopant activation at 600 °C for 15 s in N_2. After source patterning using diluted ZEP520A and BCl_3/Ar based dry etching, the 10 nm Al_2O_3 was removed in selected area as open window for Zn diffusion. Dry etching is preferred here to avoid undercut in wet etching process so that short channel de-

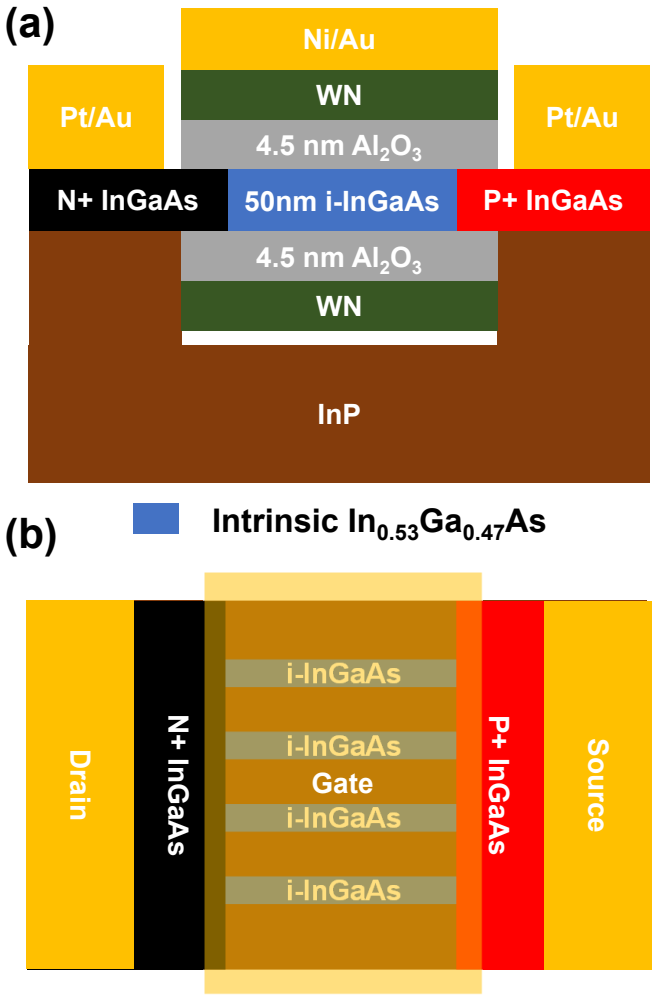

Fig. 4.15. (a) Cross-sectional view and (b) top view schematic diagrams of an InGaAs GAA TFET.

vices can be achieved. Zn-doped spin-on-glass (SOG) was then spinned on top of the wafer followed by RTA in N_2 at 450 °C for 1 min. Zn-doped p+ InGaAs region is etched down partly because of the less selective dry etching process and oxidation from O_2 in SOG during Zn diffusion process [115]. SOG and Al_2O_3 were removed in diluted BOE:H_2O=1:5 solution for 10 min. Nanowire fins were then defined by BCl_3/Ar reactive ion etching. HCl based release process was then performed to create free standing InGaAs nanowires, using similar process as in [29]. After 10 min

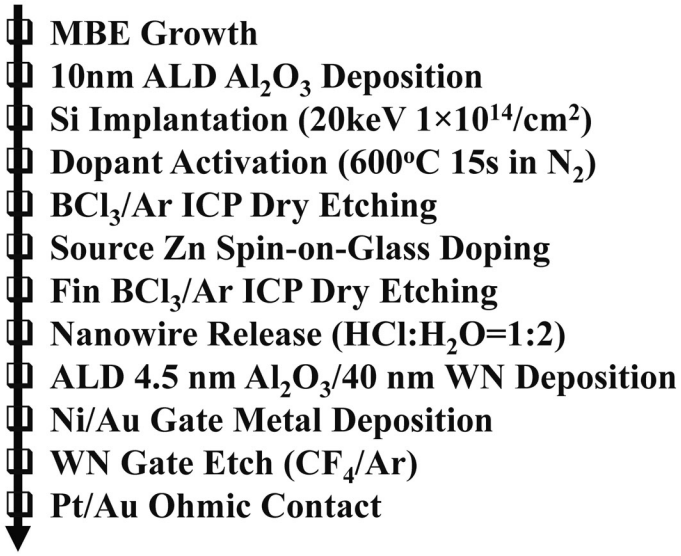

Fig. 4.16. Fabrication process flow for the InGaAs GAA TFET.

10% $(NH_4)_2S$ passivation, 4.5 nm Al_2O_3 and 40 nm tungsten nitride gate metal were grown by ALD at 250 °C and 385 °C as gate insulator and gate metal, respectively. After WN gate etch process, S/D contacts were formed with Pt/Au. Each device has four wires in parallel. All patterns were defined by a Vistec UHR electron beam lithography system.

Fig. 4.17 shows the transfer characteristics of a representative InGaAs GAA TFET. The device has L_{ch}=0.5 µm, W_{NW}=40 nm, T_{NW}=50 nm, and T_{ox}=4.5 nm. The device exhibits SS as low as 74 mV/dec at V_{DS}=0.05 V, which is better than any planar InGaAs TFET fabricated using similar process in previous section.

Fig. 4.18 shows SS (V_{DS}=0.05 V) scaling metrics for InGaAs GAA TFET with 4.5 nm Al_2O_3 as gate dielectric (EOT=2 nm) with L_{ch} down to 50 nm and with W_{NW} from 30 nm to 500 nm. Note that L_{ch} here is the mask gap length between n+ drain and p+ source. As Zn diffusion during annealing, the actually channel length is smaller than that defined by lithography masks. A significant reduction of SS is achieved comparing with planar InGaAs TFETs using similar process and even

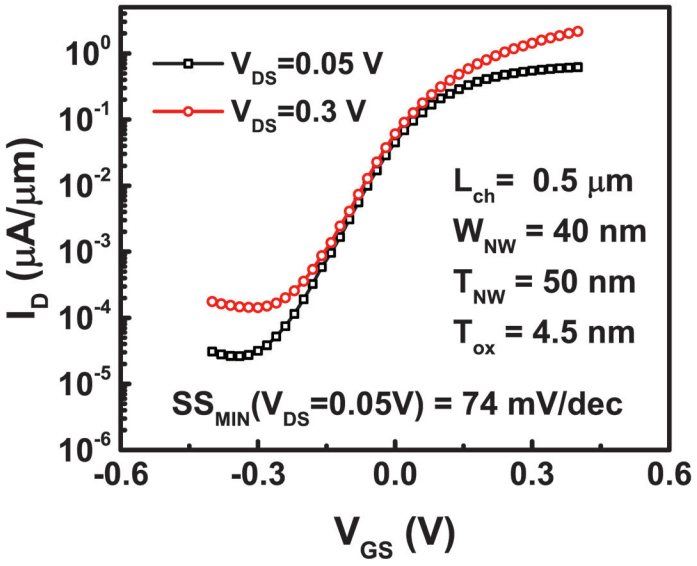

Fig. 4.17. Transfer characteristics of an InGaAs GAA TFET with L_{ch}=0.5 µm and 4.5 nm Al_2O_3 (EOT=2 nm) as dielectric.

smaller EOT (Fig. 4.9). The SS of InGaAs GAA TFETs with W_{NW}=500 nm exhibits much larger SS comparing with devices with W_{NW}=30-50 nm fabricated in the same sample. This further confirms the 3D structure contributes to the reduction of SS in InGaAs TFETs.

Figs. 4.19 and 4.20 shows I_{ON} at V_{DS}=0.3 V and $V_{GS} - V_T$=0.3 V and maximum g_m at V_{DS}=0.3 V scaling metrics for InGaAs GAA TFETs with different W_{NW}. It is found I_{ON} and maximum g_m are improved significantly after W_{NW} scaling. This also confirms the 3D structure contributes to the enhancement of on-state performance of InGaAs TFETs.

In summary, 3D InGaAs GAA TFETs are fabricated and studied with different nanowire dimensions. It is found that InGaAs GAA TFETs with smaller W_{NW} have smaller SS, larger I_{ON} and g_m, showing both on- and off-state performance improvement.

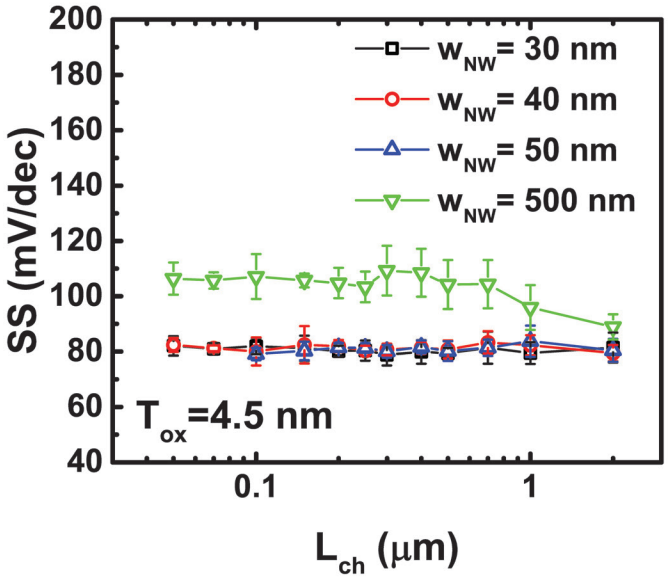

Fig. 4.18. SS scaling metrics for InGaAs GAA TFETs with 4.5 nm Al_2O_3 as gate dielectric and with various W_{NW}.

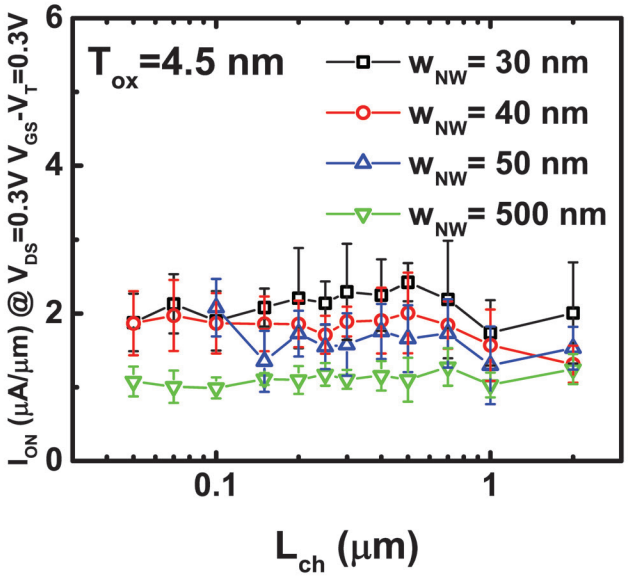

Fig. 4.19. I_{ON} scaling metrics for InGaAs GAA TFETs with 4.5 nm Al_2O_3 as gate dielectric and with various W_{NW}.

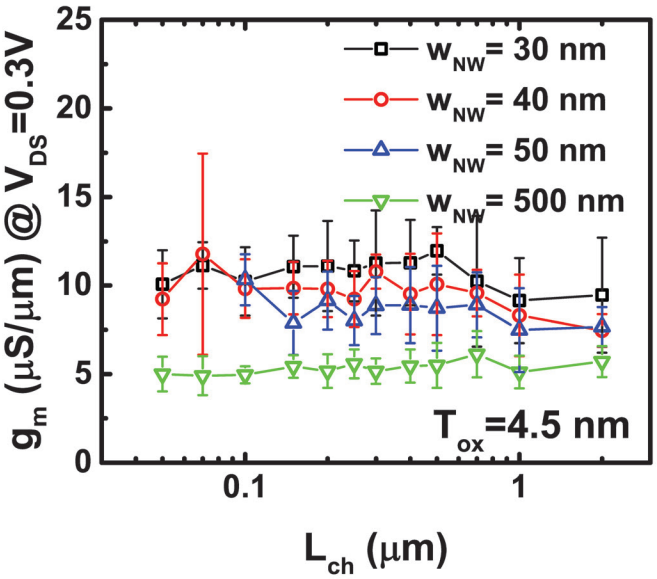

Fig. 4.20. g_m scaling metrics for InGaAs GAA TFETs with 4.5 nm Al_2O_3 as gate dielectric and with various W_{NW}.

5. NEGATIVE CAPACITANCE FIELD-EFFECT TRANSISTORS WITH III-V AND EMERGING SEMICONDUCTOR MATERIALS

5.1 Introduction

The motivation of steep-slope transistors has already been discussed in chapter 1.3. The origin of the fundamental thermionic limit of the subthreshold slope in a MOSFET is from the thermal distribution of electrons. In a NC-FET, the insulating ferroelectric layer served as a negative capacitor so that channel surface potential can be amplified more than the gate voltage, and hence the device can operate with SS less than 60 mV/dec at room temperature [15]. In this chapter, section 5.2 studies the physics of NC-FETs as steep-slope transistors. Section 5.3 discusses the ferroelectric properties in ALD deposited HZO, which is used as in the gate stack of the following sections. Section 5.4 studies MoS_2 2D NC-FETs. Section 5.5 discusses NC-FETs using InGaAs as channel material.

5.2 Physics of Negative Capacitance Field-effect Transistors

The device physics of a NC-FET is discussed here. A back-gate 2D NC-FET structure is used as an example. The NC-FET device physics for other structures such as 3D NC-FETs, top-gate NC-FETs can be treated similarly. As shown in Fig. 5.1(a) a negative capacitance 2D transistor can be treated as an intrinsic 2D transistor in series with an ferroelectric capacitor. In addition, the electrical behavior of ferroelectric capacitor can be described by Landau-Khalatnikov (LK) equation [15, 125, 126]. The potential distribution is essentially uniform (as illustrated by a metal in Fig. 5.1(a)) across the interface between oxide and ferroelectric insulator,

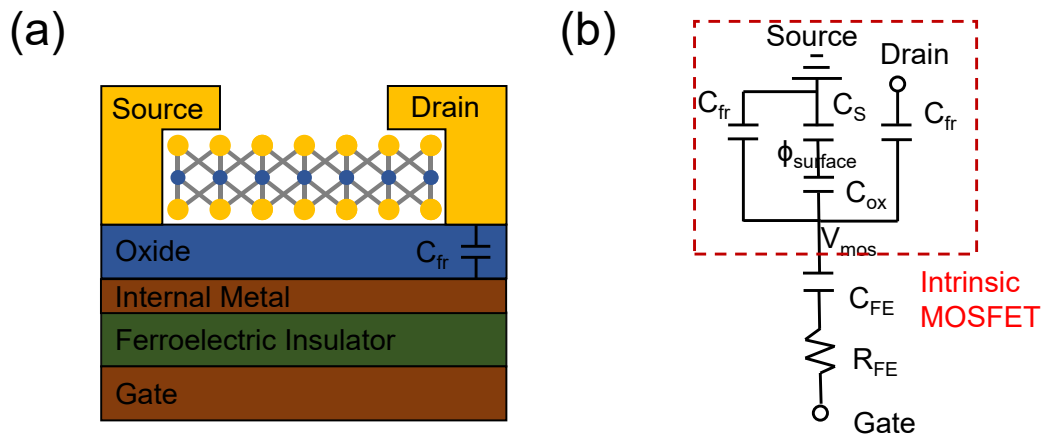

Fig. 5.1. (a) Schematic diagram of a back-gate 2D NC-FET. (b) Simplified small-signal capacitance representation of the 2D NC-FET. C_S is the capacitance of 2D channel, C_{ox} is the capacitance of the oxide layer, and C_{FE} is the capacitance of the ferroelectric insulator layer.

which simplifies the overall analysis by allowing one to decouple the ferroelectric insulator from the standard MOSFET structure. In fact, the errors caused by this approximation can be ignored when the thickness of ferroelectric layer is not too thick [127, 128].

Fig. 5.1(b) shows a small-signal capacitance circuit of the NCFET. From this capacitance network, SS can be written as,

$$SS = \frac{2.3k_BT}{q}\frac{1}{\frac{\partial\Phi_S}{\partial V_{GS}}} = \frac{2.3k_BT}{q}(1+\frac{C_S}{C_{ox}})(1-\frac{C_{device}}{|C_{FE}|}) \tag{5.1}$$

$$C_{device} = 2C_{fr} + \frac{C_S C_{ox}}{C_S + C_{ox}} \tag{5.2}$$

Note that C_{fr} is the parasitic capacitance. SS must satisfy the condition, $0<\text{SS}<2.3k_BT/q$, so that non-hysteretic behavior and a sub-thermionic SS (internal gain>1) could be obtained at the same time. The constraint conditions as the equations (5.3, 5.4) deduced from (5.1) are,

$$C_{device} < |C_{FE}| \tag{5.3}$$

$$|C_{FE}| > C_{eq} \tag{5.4}$$

To satisfy non-hysteretic conditions, $|C_{FE}|$ need to be greater than C_{device} (eq. (5.3)), while to satisfy internal gain condition (internal gain>1, SS<$2.3k_BT/q$), $|C_{FE}|$ need to be less than C_{eq} (eq. 5.4).

The complete LK equation of ferroelectric insulator is written as [129, 130],

$$V_{FE} = 2t_{FE}\alpha Q + 2t_{FE}\beta Q^3 + 6t_{FE}\gamma Q^5 + \rho t_{FE}\frac{\mathrm{d}Q}{\mathrm{d}t} \tag{5.5}$$

where α, β, and γ are landau coefficients. α is less than zero for ferroelectric insulators so that when Q is around zero, the capacitance of ferroelectric insulator can be less than zero.

In summary, the NC-FET structure can achieve sub-60 mV/dec operation without hysteresis at room temperature by inserting a ferroelectric insulator into the gate stack of a MOSFET. The theory of such operation is discussed.

5.3 ALD Deposited Hafnium Zirconium Oxide as Ferroelectric Insulators

ALD hafnium zirconium oxide (HZO) is chosen as the ferroelectric insulator for NC-FETs here for its ferroelectricity, CMOS compatible manufacturing, and ability to scale down EOT to ultra-thin dimensions [131–134].

The TiN/HZO/TiN MIM capacitor shown in Fig. 5.2 is used as the test ferroelectric capacitor. The fabrication process is discussed as follows. After standard solvent clean, 30 nm TiN was deposited by ALD at 250 °C, using $[(CH_3)_2N]_4Ti$ (TDMAT) and NH_3 as precursors. $Hf_{1-x}Zr_xO_2$ film was deposited at 250 °C, using $[(CH_3)_2N]_4Hf$ (TDMAHf), $[(CH_3)_2N]_4Zr$ (TDMAZr), and H_2O as the Hf precursor, Zr precursor, and O precursor, respectively. The $Hf_{1-x}Zr_xO_2$ film with different x can be achieved by controlling HfO_2:ZrO_2 cycle ratio, x=0.5 unless otherwise specified. Then, 30 nm TiN was deposited on top of HZO using the same process. Sample transfer in the ALD deposition processes was within a glovebox, in which samples only exposed to Ar environment. The sample was then annealed at different temperatures in N_2 for 1

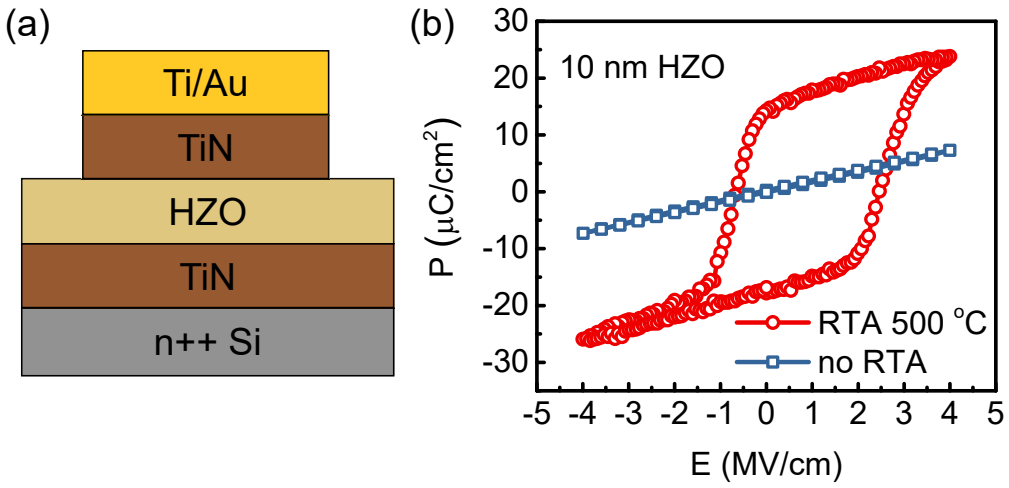

Fig. 5.2. (a) Schematic diagram of a HZO MIM capacitor. (b) Polarization-electric field measurement of HZO MIM capacitors without RTA and RTA at 500 °C in N_2 for 1 min.

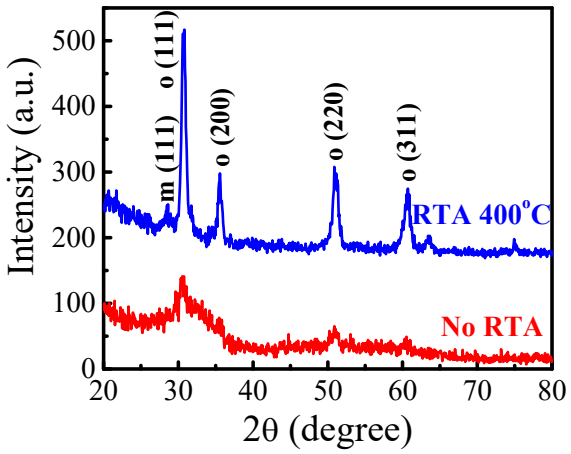

Fig. 5.3. GI-XRD diffractograms of HZO. The formation of non-centrosymmetric o-phase is believed to lead to the ferroelectricity of HZO films after annealing at 400 °C.

min. 20 nm Ti/50 nm Au top electrodes were fabricated by photo lithography, e-beam evaporation and lift-off process, followed by CF_4/Ar dry etching process to isolate the different Ti/Au top electrodes.

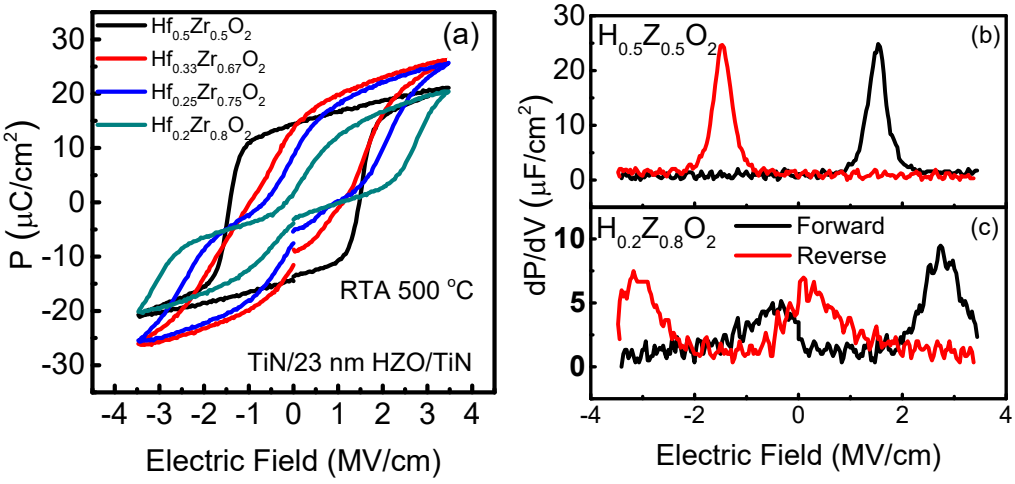

Fig. 5.4. (a) Hysteresis loop of P-E for TiN/23 nm HZO/TiN MIM capacitors with different Hf:Zr ratio. dP/dV vs. electric field for both (b) ferroelectric and (c) anti-ferroelectric HZO with different Hf:Zr ratio.

The annealing temperature is critical in the ferroelectricity of HZO film. Fig. 5.2 shows the polarization-electric field measurement of HZO MIM capacitors without RTA and RTA at 500 °C in N_2 for 1 min. Clear dielectric to ferroelectric transition can be seen after annealing on the metal-insulator-metal (MIM, TiN/10 nm HZO/TiN) capacitor. The origin of such impact is studied by X-ray diffraction (XRD) measurement. Grazing incidence XRD analysis in Fig. 5.3 depicts the crystallization behaviors of HZO with no RTA and after RTA. The sample with 400 °C reveals apparent orthorhombic phases (o-phases). The formation of non-centrosymmetric o-phase is believed to lead to the ferroelectricity of HZO films after annealing [135, 136], as confirmed in Fig. 5.3.

The ferroelectricity and anti-ferroelectricity can be controlled by Hf:Zr ratio in ALD HZO. Fig. 5.4(a) shows the hysteresis loop of polarization vs. electric field (P-E) of TiN/HZO/TiN (MIM, ALD at 200 °C, RTA in N_2 at 500 °C) capacitors with different Hf:Zr ratio from 1:1 to 1:4. It is clear to see HZO shows ferroelectric hysteresis loop when Hf:Zr ratio=1:1, while with more Zr composition in HZO, the

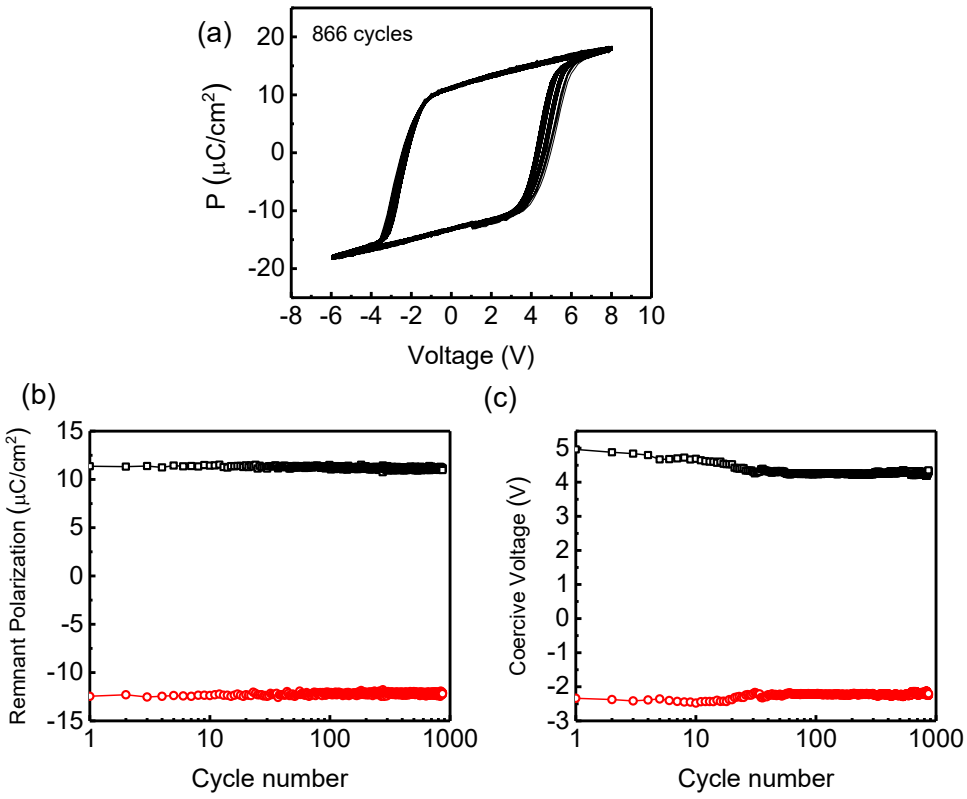

Fig. 5.5. (a) Polarization-voltage measurement for 866 cycles (4 ms measurement time for each) on the same HZO MIM capacitor. (b) Remnant polarization versus cycle number. (c) Coercive voltage versus cycle number.

P-E hysteresis loop becomes anti-ferroelectric. Fig. 5.4 shows dP/dV vs. electric field for (b) FE HZO and (c) AFE HZO. HZO with Hf:Zr ratio=1:1 shows two spikes corresponding to ferroelectric switching while HZO with Hf:Zr ratio=1:4 shows four spikes corresponding to anti-ferroelectric switching.

Fig. 5.5(a) shows the repeated cycling P-V measurement on a HZO MIM capacitor device for 866 cycles (4 ms for each measurement). It can be seen that the P-V characteristics remain almost ideal ferroelectric hysteresis loop. Fig. 5.5(b) shows the remnant polarization (P_r) versus cycle number. P_r shows negligible change during the repeated cycling measurement. Fig. 5.5(c) shows the coercive voltage (V_c) versus

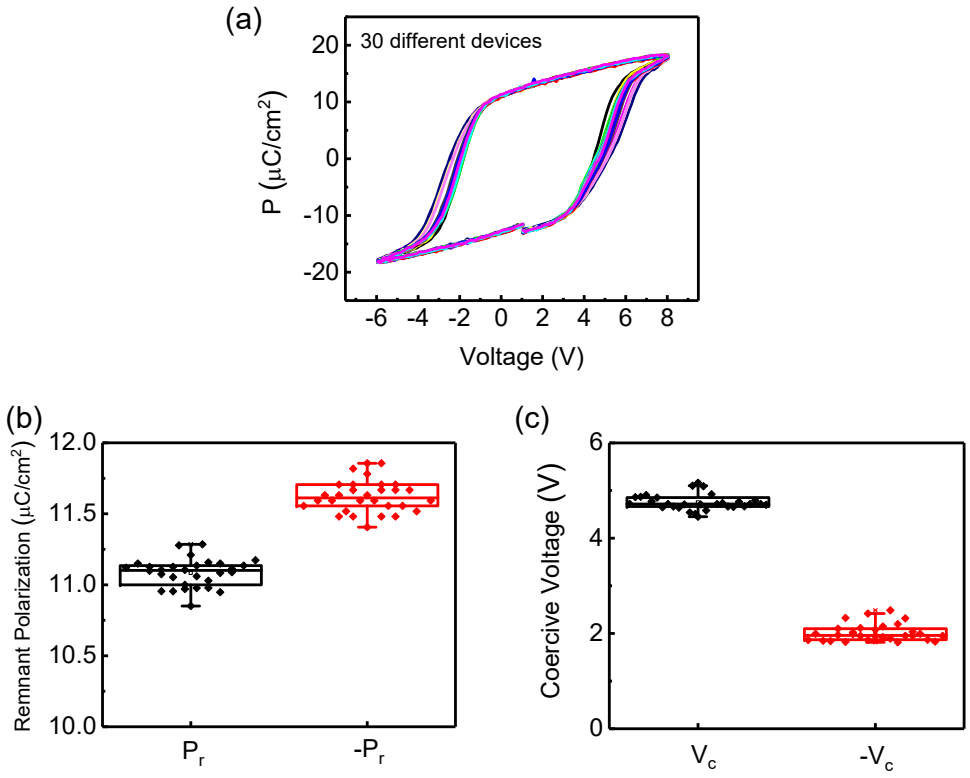

Fig. 5.6. (a) P-V measurement of 30 different HZO MIM capacitor devices. (b) Box plot of statistical distribution of remnant polarization. (c) Box plot of statistical distribution of coercive voltage.

cycle number. V_c shows negligible change after first 30 cycles in the repeated cycling measurement. The slight change of V_c in the first 30 cycles suggests the result of initial charge trapping effects. Fig. 5.6(a) shows the statistical P-V measurement of 30 HZO MIM capacitors over the entire sample. Fig. 5.6(b) and 5.6(c) show the box plot of statistical distribution of P_r and V_c. A very small variation in the P-V characteristics is obtained among all 30 measured devices. The statistical measurement and repeated cycling measurement confirm the ALD ferroelectric HZO process is repeatable, reliable and reproducible as a ferroelectric insulator for NC-FET applications.

5.4 Negative Capacitance Field-effect Transistors with 2D Semiconductors

Transition metal dichalcogenides (TMDs) have been intensely explored as 2D semiconductors for future device technologies. Atomically thin MoS_2 has been extensively studied as a highly promising channel material because it offers the ideal electrostatic control of the channel, ambient stability, an appropriate direct bandgap and moderate mobility. The TMD is generally configured in a junctionless (JL) form, where metal-semiconductor contacts replace the source/drain p-n junctions of a bulk transistor. Junctionless MoS_2 FETs exhibit high on/off ratio and strong immunity to short channel effects for transistor applications with channel length down to sub-5 nm [137–142]. However, the power dissipation issue remains unresolved as silicon-based MOSFETs scaling. In a NC-FET [15, 125, 131–134, 143–148], the insulating ferroelectric layer served as a negative capacitor so that channel surface potential can be amplified more than the gate voltage, and hence the device can operate with SS less than 60 mV/dec at room temperature. The simultaneous fulfillment of internal gain and non-hysteretic condition is crucial to the proper design of capacitance matching in a stable NC-FET. Meanwhile, the channel transport in NC-FETs remains unperturbed. Therefore, coupled with the flatness of the body capacitance of TMD materials and symmetrical operation around the zero-charge point in a junctionless transistor, performance in 2D JL-NCFET is expected to improve for both on- and off-states. Therefore, it would be highly desirable to integrate ferroelectric insulator and 2D ultrathin channel materials as a 2D JL-NCFET to achieve high on-state performance for high operating speed and sub-thermionic SS for low power dissipation.

5.4.1 Steep-slope Hysteresis-free Negative Capacitance MoS_2 Transistors

Here, we demonstrate steep-slope MoS_2 NC-FETs by introducing ferroelectric HZO into the gate stack. These transistors exhibit essentially hysteresis-free switching characteristics with maximum drain current of 510 µA/µm and sub-thermionic

subthreshold slope. The maximum drain current of the NC-FETs fabricated in this work is found to be around five times larger than MoS_2 FETs fabricated on 90 nm SiO_2 using the same process. As will be discussed below, this is a direct consequence of on-state voltage application in a JL-NCFET. Negative differential resistance, correlated to the negative DIBL at off-state, is observed because of drain coupled negative capacitance effect. Remarkably, the high performance sustains despite significant self-heating in the transistors, as opposed to traditional bulk MOSFETs.

The experimental device schematic of a MoS_2 NC-FET NC-FET, as shown in Fig. 5.7(a), consists of a mono-layer up to dozen layers of MoS_2 as channel, 2 nm amorphous aluminum oxide (Al_2O_3) layer and 20 nm polycrystalline HZO layer as the gate dielectric, heavily doped silicon substrate as the gate electrode and nickel source/drain contacts. An amorphous Al_2O_3 layer was applied for capacitance matching and gate leakage current reduction through polycrystalline HZO.

The fabrication started from a heavily doped silicon substrate. 20 nm $H_{0.5}Z_{0.5}O_2$ was deposited by ALD as a ferroelectric insulator layer on heavily doped silicon substrate after standard surface cleaning. Another 10 nm aluminum oxide layer was deposited as an encapsulation layer to prevent the degradation of HZO by the reaction with moisture in air. BCl_3/Ar dry etching process was carried out to adjust the thickness of Al_2O_3 down to 2 nm for capacitance matching. The annealing process was then performed in rapid thermal annealing in nitrogen ambient for 1 minute at various temperatures. MoS_2 flakes were transferred to the substrate by scotch tape-based mechanical exfoliation. Electrical contacts using 100 nm nickel electrode were fabricated using electron-beam lithography, electron-beam evaporation and lift-off process.

A cross-sectional transmission electron microscopy (TEM) image of a representative MoS_2 NC-FET is shown in Fig. 5.7(b) and detailed energy dispersive X-ray spectrometry (EDS) elemental mapping is presented in Fig. 5.7(c). The EDS analysis confirms the presence and uniform distribution of elements Hf, Zr, Al, O, Mo and S. No obvious inter-diffusion of Hf, Zr and Al is found.

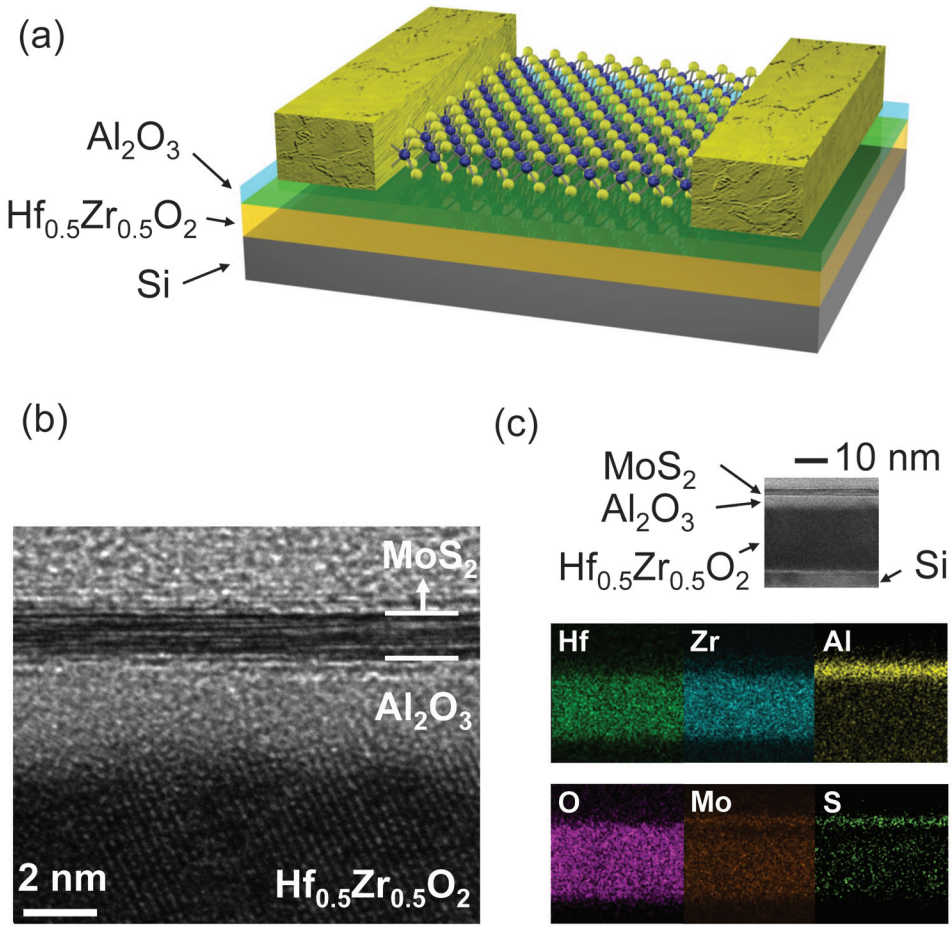

Fig. 5.7. (a) Schematic view of a MoS_2 NC-FET. (b) Cross-sectional view of a representative sample showing bi-layer MoS_2 channel, amorphous Al_2O_3 and polycrystalline HZO gate dielectric. (c) Corresponding EDS elemental mapping showing the distribution of elements of Hf, Zr, Al, O, Mo and S.

The electrical characteristics of MoS_2 NC-FETs are strongly dependent on the ferroelectricity of HZO layer, defined by the film annealing temperature and V_{GS} sweep speed. In addition to standard $I - V$ measurements, the hysteresis is measured as V_{GS}-difference between forward (from low to high) and reverse (from high to low) V_{GS} sweeps at I_D=1 nA/µm and at V_{DS}=0.1 V. Here, we first study the room temperature characteristics of MoS_2 NC-FETs. Fig. 5.8(a) shows the $I_D - V_{GS}$ characteristics of a device with 500 °C annealed gate dielectric, measured at V_{GS} step of 5 mV. This

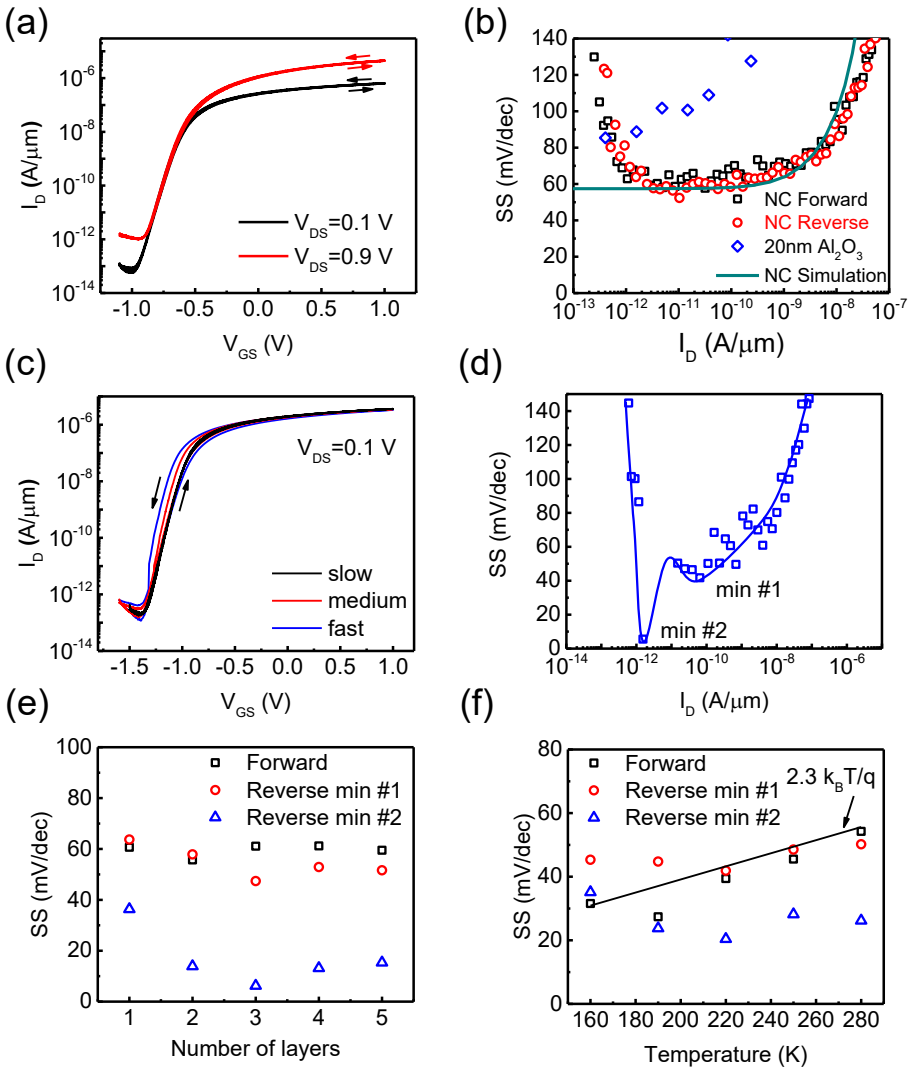

Fig. 5.8. (a) $I_D - V_{GS}$ characteristics measured at room temperature and at V_{DS} from 0.1 V to 0.9 V. (b) SS versus I_D characteristics of the same device in (a), showing minimum SS below 60 mV/dec for both forward and reverse sweep. (c) $I_D - V_{GS}$ characteristics measured at room temperature and at V_{DS}=0.1 V at different gate voltage sweep speed. (d) SS versus I_D characteristics during fast reverse sweep of the same device in (c). The SS versus I_D characteristics show two local minima, defined as min #1 and min #2. (e) Layer dependence of SS from 1 layer to 5 layers. The SS of MoS_2 NC-FETs shows weak thickness dependence. (f) Temperature dependence of SS from 160 K layer to 280 K.

device has a channel length of 2 µm, channel width of 3.2 µm and channel thickness of 8.6 nm. The hysteresis (∼12 mV) is small and essentially negligible, consistent with the theory of NC-FET. Fig. 5.8(b) shows SS vs. I_D data of the same device as in Fig. 5.8(a), and the comparison with simulation results and experimental results with 20 nm Al_2O_3 only as gate dielectric. The MoS_2 FETs fabricated on a 20 nm Al_2O_3 conventional dielectric present the typical SS of 80-90 mV/dec, much larger than the values from NC-FETs. SS is extracted for both forward sweep (SS_{For}) and reverse sweep (SS_{Rev}). The device exhibits SS_{Rev}=52.3 mV/dec, SS_{For}=57.6 mV/dec. SS below 60 mV/dec at room temperature is conclusively demonstrated for both forward and reverse sweeps at this near hysteresis-free device.

Since the HZO polarization depends on sweep-rate, the electrical characterization for the MoS_2 NC-FETs is also carried out at different V_{GS} sweeping speeds. The sweeping speed is controlled by modifying the V_{GS} measurement step, from 0.3 mV to 5 mV. Fig. 5.8(c) shows the $I_D - V_{GS}$ characteristics of a few-layer MoS_2 NC-FET measured at slow, medium and fast sweep speed, corresponding to V_{GS}=0.3, 1 and 5 mV. Hysteresis of the MoS_2 NC-FETs is found to be diminished by reducing the sweeping speed. A plateau and a minima characterize the SS (vs I_D) during reverse sweep. These features ($SS_{Rev,min\#1}$ and $SS_{Rev,min\#2}$) are observed among almost all fabricated devices when measured with fast sweep V_{GS}, as shown in Fig. 5.8(d). The second local minimum of SS is the result of the switching between two polarization states of the ferroelectric oxide, associated with loss of capacitance matching at high speed. When measured in fast sweep mode where V_{GS} step is 5 mV, the device exhibits SS_{For}=59.6 mV/dec, $SS_{Rev,min\#1}$=41.7 mV/dec, and $SS_{Rev,min\#2}$=5.6 mV/dec. Overall, average SS less than 60 mV/dec for over 4 decades of drain current. In slow sweep mode, no obvious second local minima and hysteresis can be observed as shown in Fig. 5.8(a), reflecting well-matched capacitances throughout the subthreshold region. Fig. 5.8(e) shows the thickness dependence of SS from mono-layer to 5 layers of MoS_2 as channels. No obvious thickness dependence SS is observed. Fig. 5.8(f) shows the temperature dependence of SS for a MoS_2 NC FET measured from 280 K

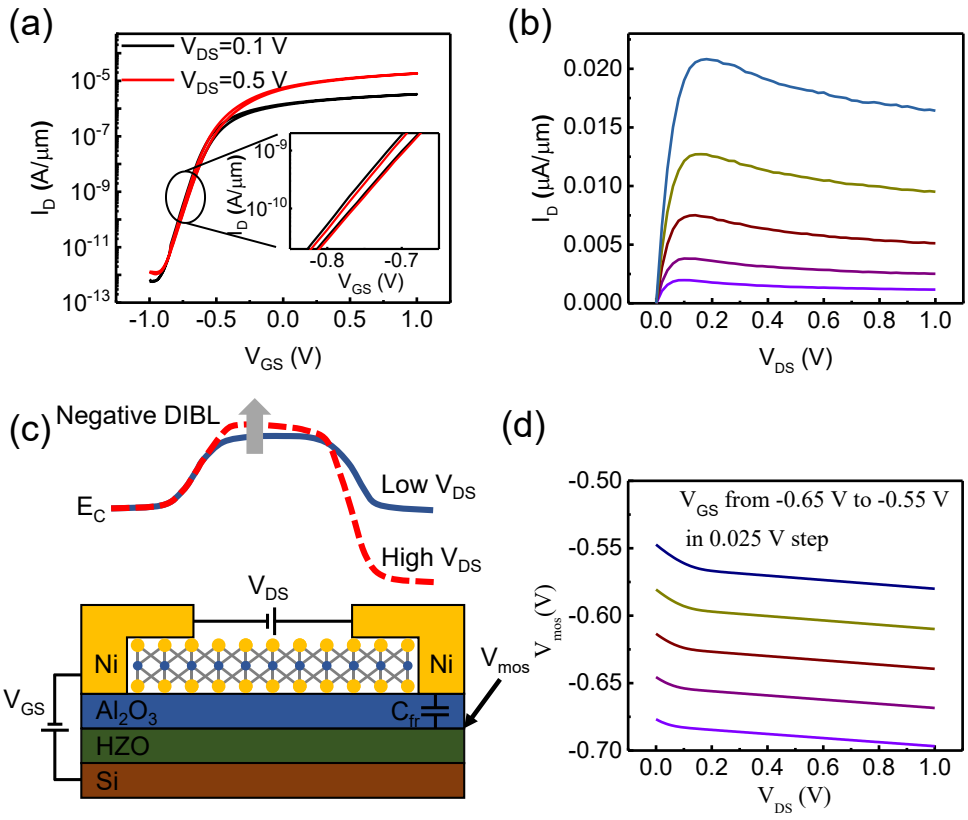

Fig. 5.9. (a) $I_D - V_{GS}$ characteristics measured at room temperature and at V_{DS} at 0.1 V and 0.5 V. Inset: zoom-in image of $I_D - V_{GS}$ curve between −0.8 V to −0.7 V. (b) $I_D - V_{DS}$ characteristics measured at room temperature at V_{GS} from −0.65 V to −0.55 V in 0.025 V step. Clear NDR can be observed because of the negative DIBL effect induced by negative capacitance. (c) Illustration of band diagram of negative DIBL effect. (d) Simulation of interfacial potential vs. V_{DS}.

down to 160 K. Measured SS is below the thermionic limit down to 220 K. SS below 190 K is above the thermionic limit because of the stronger impact of Schottky barrier at lower temperatures.

Drain-induced-barrier-lowering is widely observed as one of the major evidences for the short channel effects in MOSFETs [3]. In conventional MOSFETs, the threshold voltage (V_T) shifts toward the negative direction as drain voltage. The DIBL, defined as DIBL=$-\Delta V_T/\Delta V_{DS}$, is usually positive. It has been theoretically predicted that

with ferroelectric insulator introduced into gate stack of a practical transistor, the DIBL could be reversed in NC-FETs [148]. NDR can naturally occur as a result of the negative DIBL effect. Fig. 5.9(a) shows the negative DIBL in $I_D - V_{GS}$ characteristics of another device with a channel length of 2 µm, a channel width of 5.6 µm, a channel thickness of 7.1 nm and 2 nm Al_2O_3 and 20 nm HZO as gate dielectric. It is evident that the $I_D - V_{GS}$ curve shifts positively when V_{DS} is increased from 0.1 V to 0.5 V. As this negative DIBL happens around off-state, NDR is also observed simultaneously in the same device at the off-state as shown in Fig. 5.9(b). Fig. 5.9(c) shows the illustration of band diagram of negative DIBL effect. The negative DIBL origins from the capacitance coupling to from drain to interfacial layer between Al_2O_3 and HZO. The interfacial layer potential (V_{mos}) can be estimated as a constant when the thickness of ferroelectric oxide layer is thin. Simulation of V_{mos} shows when V_{DS} is increased, the interfacial potential is reduced (Fig. 5.9(d)), indicating the carrier density in MoS_2 channel is reduced. Thus, the channel resistance is increased which lead to the NDR effect.

The EOT of the gate stack (2 nm Al_2O_3 and 20 nm HZO) in this work is measured to be 4.4 nm by C-V measurement. The breakdown voltage is consistently measured to be around 11 V. The breakdown voltage/EOT is 2.5 V/nm, which is about 2.5 times larger than the value of SiO_2. It can be easily verified that the breakdown voltage/EOT is proportional to the electric displacement field. As it is well known from Maxwells equations that electric displacement field is proportional to the charge density, higher breakdown voltage/EOT could lead to higher carrier density. Fig. 5.10(a) shows the $I_D - V_{DS}$ characteristics measured at room temperature of a MoS_2 NC-FET with 100 nm channel length. The thickness of the MoS_2 flake is 3 nm. The gate voltage was stressed up to 9 V and maximum gate voltage over EOT in this device is about 2 V/nm. Maximum drain current of 510 µA/µm is achieved, which is about 5 times larger than the control devices using 90 nm SiO_2 as gate dielectric. Note that this maximum drain current is obtained without special contact engineering such as doping [142] or heterostructure contact stack [149]. It is an important but unexplored

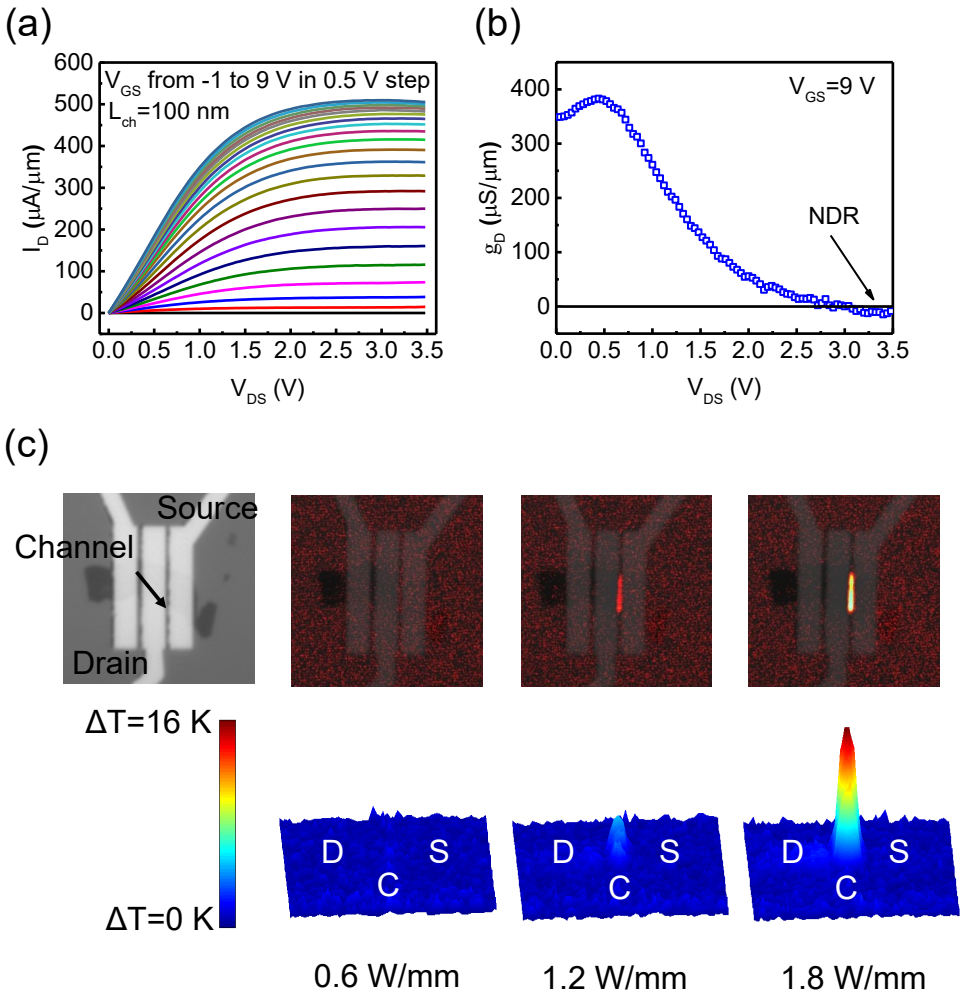

Fig. 5.10. (a) $I_D - V_{DS}$ characteristics measured at room temperature at V_{GS} from -1 V to 9 V in 0.5 V step. This device has a channel length of 100 nm. (b) $g_D - V_{DS}$ characteristics from (a) at V_{GS}=9 V. g_D less than zero at high V_{DS} highlights the NDR effect due to self-heating. (c) Thermo-reflectance image and (d) temperature map at different power density from 0.6 W/mm to 1.8 W/mm.

advantage in applying ferroelectric gate stack to enhance on-state performance. Another type of NDR (Fig. 5.10(b)) is also clearly observed when the device is biased at high V_{GS} because of the self-heating effect from large drain current and voltage. Fig 5.10(c) shows the thermo-reflectance image taken at different power density from

0.6 W/mm to 1.8 W/mm. The heated channel with the increased temperature up to ∼40 °C suggests the self-heating effect, which potentially degrades channel mobility and limits the maximum drain current, has to be considered in MoS_2 NC-FETs.

In conclusion, we have successfully demonstrated MoS_2 2D NC-FETs with the simultaneous promising on- and off-state characteristics. The stable, non-hysteretic and bi-directional sub-thermionic switching characteristics are unambiguously confirmed to be the result of negative capacitance effect. On-state performance is enhanced at the same time with a maximum drain current of 510 µA/µm at room temperature, which leads to self-heating effect. Finally, weve shown that the observed negative differential resistance is induced by the negative DIBL effect.

5.4.2 MoS_2 Negative Capacitance Field-effect Transistors with Internal Metal Gate

Here, we demonstrate steep-slope MoS_2 NC-FETs with ferroelectric hafnium zirconium oxide (HZO) and internal metal gate (IMG) in the gate stack. SS less than 50 mV/dec is obtained for both forward and reverse gate voltage sweeps, with minimum SS_{For}=37.6 mV/dec and minimum SS_{Rev}=42.2 mV/dec. A second minimum of SS_{Rev} as low as 8.3 mV/dec can be measured as the result of dynamic switching at high speed in ferroelectric HZO.

Fig. 5.11 show the schematic diagram of MoS_2 NC-FETs with internal metal gate. The MoS_2 NC-FETs with IMG consist of few-layer MoS_2 as channel, 20 nm polycrystalline HZO layer, 3 nm amorphous aluminum oxide (Al_2O_3) layer, 20 nm Ni layer and 10 nm HfO_2 as the gate dielectric, heavily doped silicon substrate as the gate electrode and nickel as the source/drain contacts.

The device fabrication process of MoS_2 NC-FETs with IMG is discussed as follows. HZO film was deposited by ALD at 250 °C on a heavily doped low resistivity silicon substrate after standard RCA cleaning, diluted HF dip and deionized water rinse. Another 3 nm Al_2O_3 was subsequently in-situ deposited using TMA and H_2O as pre-

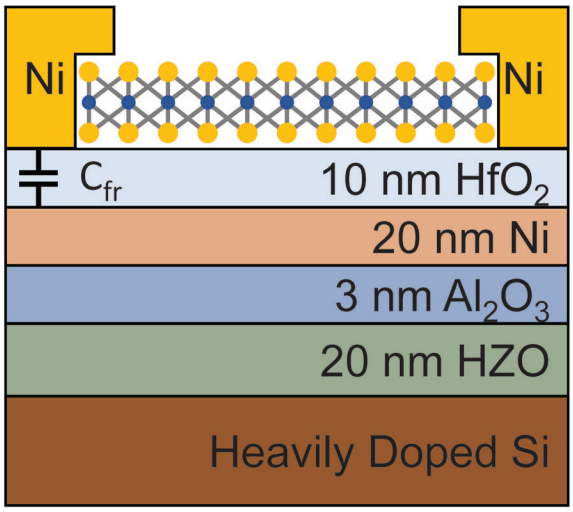

Fig. 5.11. Schematic of a MoS_2 NC-FETs with internal metal gate.

cursors at 250 °C. An amorphous Al_2O_3 layer was applied for capacitance matching and gate leakage current reduction through polycrystalline HZO. Then, the IMG pattern was defined by electron-beam lithography, followed by 20 nm Ni electron-beam evaporation and lift-off process. Another 10 nm nm HfO_2 was deposited by ALD at 250 °C using TDMAHf and H_2O as precursors. The annealing process was then performed by rapid thermal annealing (RTA) in nitrogen ambient for 1 minute at 400 °C. MoS_2 flakes were transferred to the substrate by scotch-tape based mechanical exfoliation. 100 nm nickel electrodes as electrical source/drain contacts were fabricated using electron-beam lithography, electron-beam evaporation and lift-off process.

Fig. 5.12(a) shows the $I_D - V_{GS}$ characteristics of a MoS_2 NC-FET with IMG and with 0.5 µm channel length and 8 nm channel thickness. Fig. 5.12(b) shows the $I_D - V_{GS}$ characteristics of the internal MoS_2 FET of the same device as in Fig. 5.12(a). Fig. 5.13 shows SS vs. I_D in the off-state of the same devices as in Fig. 5.12, to compare MoS_2 NC-FET with IMG and the internal MoS_2 FET with 10 nm HfO_2 only as gate dielectric. A plateau and a minimum characterize the sub-60 mV/dec SS (vs I_D) during reverse sweep for MoS_2 NC-FETs. These fea-

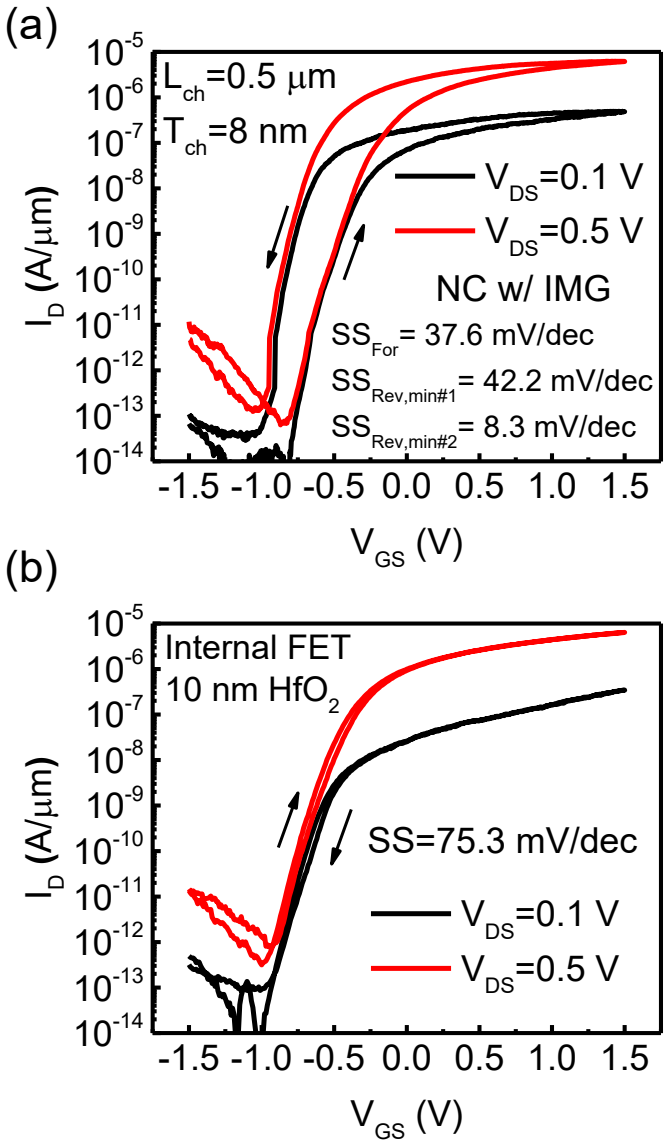

Fig. 5.12. (a) $I_D - V_{GS}$ characteristics of a MoS_2 NC-FET with IMG measured at room temperature, same structure as Fig. 5.11. (b) $I_D - V_{GS}$ characteristics of the internal MoS_2 FET of the same device as (a) but has 10 nm HfO_2 as gate dielectric.

tures ($SS_{Rev,min\#1}$ and $SS_{Rev,min\#2}$) are observed among almost all fabricated devices. The second local minimum of SS is the result of the switching between two polarization states of the ferroelectric oxide, associated with loss of capacitance match-

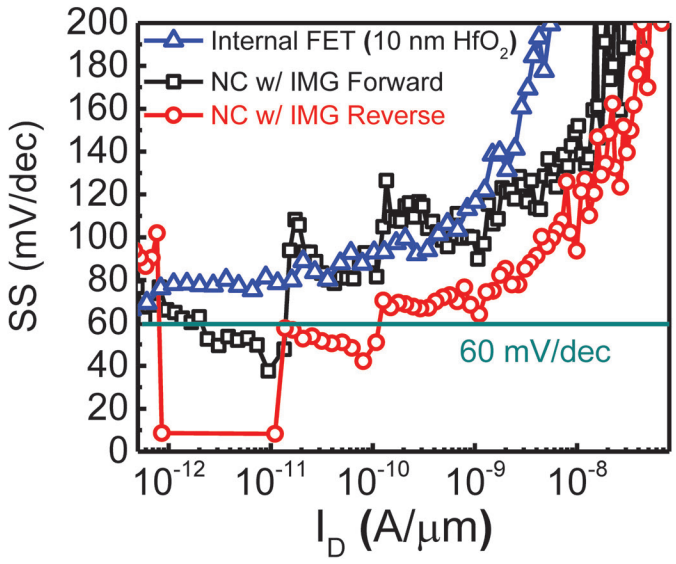

Fig. 5.13. SS vs. I_D characteristics of MoS_2 NC-FET with IMG and internal MoS_2 FET of the same device.

ing at high speed. All the device $I_D - V_{GS}$ characterization are kept at the same measurement speed. The MoS_2 NC-FET with IMG exhibits SS_{For}=37.6 mV/dec, $SS_{Rev,min\#1}$=42.2 mV/dec, and $SS_{Rev,min\#2}$=8.3 mV/dec but with a negative −0.33 V hysteresis at I_D=1 nA/μm, comparing to a negative −0.1 V hysteresis in MoS_2 NC-FET without IMG (Fig. 5.8(c)). This suggests the enhanced C_{fr} lead to a larger hysteresis and smaller SS. The SS of the MoS_2 NC-FET with IMG is much smaller than the SS measured from the internal MoS_2 FET, indicating the exist of internal amplification of the 20 nm HZO/3 nm Al_2O_3 stack.

Fig. 5.14(a) shows the comparison of $I_D - V_{GS}$ characteristics measured at V_{DS}=0.1 V between the MoS_2 NC-FET with IMG and the internal MoS_2 FET. The improved drain current suggesting the reduction of contact resistance by the internal amplification of negative capacitance gate stack. Fig. 5.14(b) and Fig. 5.14(c) show the internal amplification measured from MoS_2 NC-FET (V_G) and the internal MoS_2 FET (V_{int}), where the internal amplification is defined as dV_{int}/dV_G. Internal

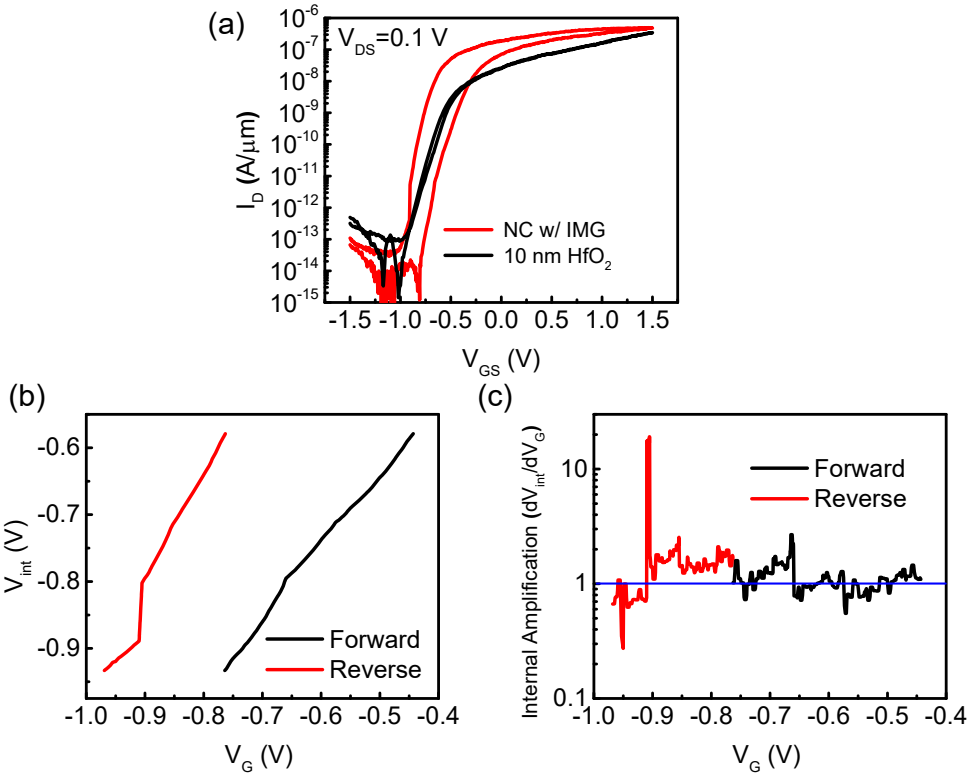

Fig. 5.14. (a) $I_D - V_{GS}$ characteristics comparison between MoS_2 NC-FET with IMG and the internal MoS_2 FET of the same device. (b) V_{int} vs. V_G for MoS_2 NC-FET with IMG calculated based on internal MoS_2 FET as in (a). (c) Internal amplification calculated based on dV_{int}/dV_G in (b).

amplification greater than 2 is achieved for both forward and reverse gate voltage sweeps.

The gate leakage current density is measured for both gate stack with and without internal metal gate using capacitor structure and Ni as top electrode. The gate leakage current of the whole stack (I_1 for NC-FET with IMG and I_2 for NC-FET without IMG) within ± 2 V is negligible to device $I - V$ characteristics as shown in Fig. 5.15. The leakage current through the internal gate dielectric (I_3) and the ferroelectric stack (I_4) are also measured, as shown in Fig. 5.15(d). It is found that within ± 2 V, the leakage current density to the floating IMG (I_3 and I_4) is sufficiently small.

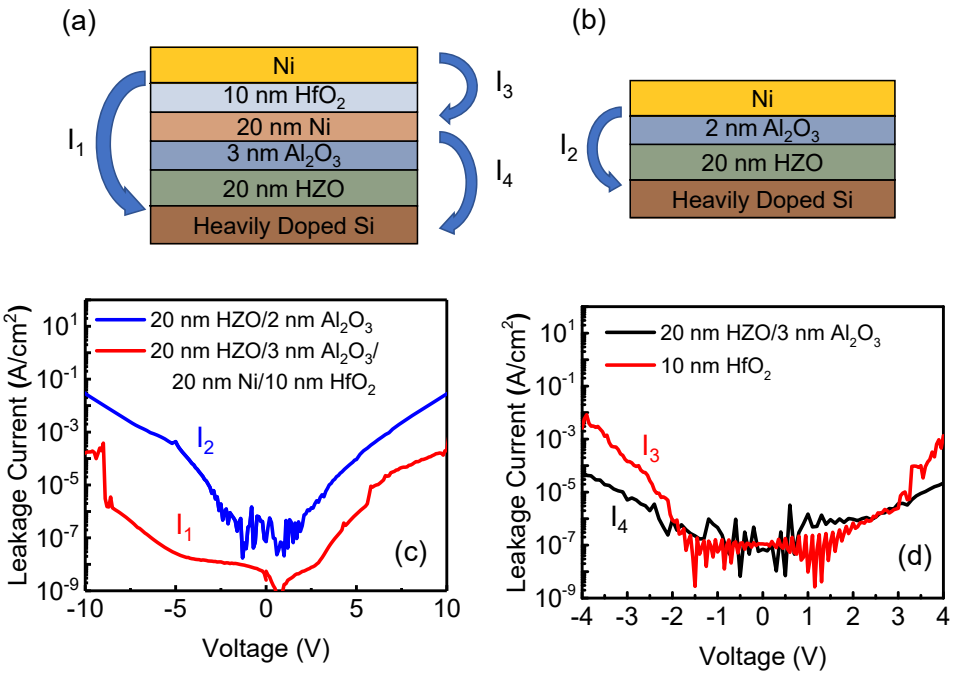

Fig. 5.15. (a) Cross-sectional view of a capacitor for leakage current measurement with same gate stack as MoS_2 NC-FET with IMG. (b) Cross-sectional view of a capacitor for leakage current measurement with same gate stack as MoS_2 NC-FET without IMG. (c) Leakage current density of the gate stack of MoS_2 NC-FET with/without IMG (I_1/I_2). (4) Leakage current density of internal gate dielectric (I_3) and of ferroelectric stack (I_4).

In conclusion, steep-slope MoS_2 NC-FETs with ferroelectric HZO and internal metal gate in the gate dielectric stack are demonstrated. SS less than 50 mV/dec is obtained for both forward and reverse gate voltage sweeps, with minimum SS_{For}=37.6 mV/dec and minimum SS_{Rev}=42.2 mV/dec.

5.5 III-V Negative Capacitance Field-effect Transistors

III-V materials such as InGaAs are well known as a promising high mobility semiconductor material as discussed in chapter 2. In this section, we combine the ad-

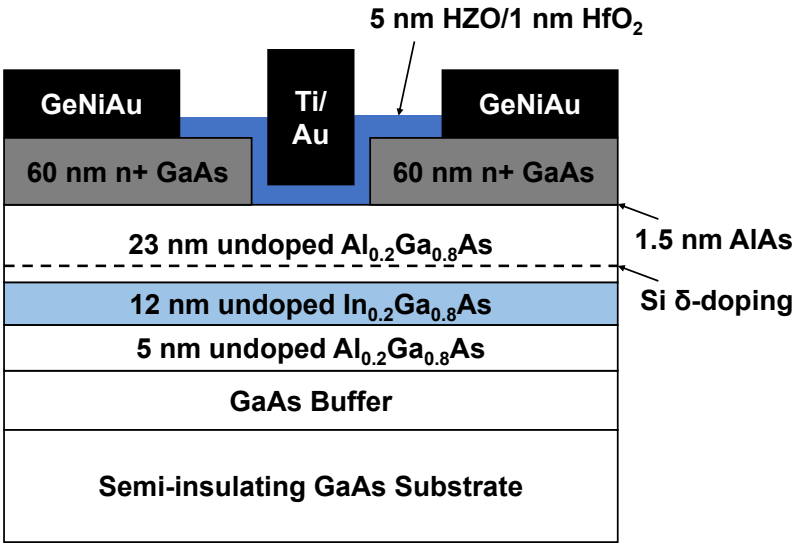

Fig. 5.16. Cross-sectional view of an InGaAs NC-FET with ferroelectric MOSHEMT structure.

vantage of III-V high mobility material together with NC-FET structure and demonstrate a III-V NC-FET with ferroelectric MOSHEMT structure. The devices exhibit enhanced performance comparing with the III-V dielectric MOSHEMT using same structure.

Fig. 5.16 illustrates the cross-sectional schematic diagram of the III-V NC-FET. A 5 nm undoped $Al_{0.2}Ga_{0.8}As$, 12 nm undoped $In_{0.2}Ga_{0.8}As$ and 23 nm undoped $Al_{0.2}Ga_{0.8}As$ with $4 \times 10^{12}\,cm^{-2}$ Si δ-doping layer located 3 nm above InGaAs, 1.5 nm n-doped $1 \times 10^{18}\,cm^{-3}$ AlAs etch stop layer, and 60 nm n-doped $5 \times 10^{18}\,cm^{-3}$ GaAs top layer have been sequentially grown on a GaAs buffer layer and semi-insulating GaAs substrate.

Device isolation was done by wet etching using a H_2SO_4:H_2O_2:H_2O (2:16:150) solution. The etch rate is about 10 nm/s. Gate recess was performed using a citric acid:H_2O_2:H_2O (16g:4 ml:70 ml) solution (high seletivity between GaAs and AlAs)

for 2 min. The etch rate of GaAs is about 1 nm/s. After gate recess, the sample was dipped in HCl:H_2O (1:2) solution for 5 s to remove the AlAs etch stop. Then, ALD deposition of 5 nm HZO and 1 nm HfO_2 was done at 250 °C using $[(CH_3)_2N]_4Hf$ (TDMAHf), $[(CH_3)_2N]_4Zr$ (TDMAZr), and H_2O as the Hf precursor, Zr precursor, and O precursor, respectively. The ALD process is discussed in great details in section 5.3. The source/drain ohmic contacts were formed by electron-beam evaporation of Au/Ge/Au/Ni/Au (5 nm/12.5 nm/15 nm/9 nm/50 nm) metal layers and lift-off process, followed by a 400 °C RTA in N_2 for 30 s. The oxide between ohmic metals and GaAs was removed by a BCl_3/Ar dry etching process. The gate metal (Ti 20 nm/Au 50 nm) was then deposited by electron-beam evaporation and lift-off process.

Fig. 5.17 shows the $I_D - V_{GS}$ characteristics of a representative InGaAs NC-FET with 2 µm channel length. The transfer characteristics show a counterclockwise hysteresis which is the result of ferroelectric HZO in the gate stack. SS as low as 82 mV/dec is achieved, which is smaller than device using same structure but using Al_2O_3 only as gate dielectric (90 mV/dec in [150]), suggesting the enhancement by NC-FET structure. Fig. 5.18 shows $g_m - V_{GS}$ at V_{DS}=1 V characteristics of the same InGaAs NC-FET as in Fig. 5.17. A maximum g_m of 117 µS/µm is achieved in reverse sweep. Fig. 5.19 showing SS versus V_{GS} characteristics at V_{DS}=0.1 V of the same InGaAs NC-FET as in Fig. 5.17, showing a reduced SS in reverse sweep.

Although sub-thermionic SS is not achieved because of the well-known oxide/III-V interface traps and the relatively thick AlGaAs barrier, a reduction of SS in NC-FET structure comparing with normal MOSHEMT and the counterclockwise hysteresis confirms the NC-FET operation and the performance improvement also suggests the NC-FET structure is promising for future low power post-CMOS applications.

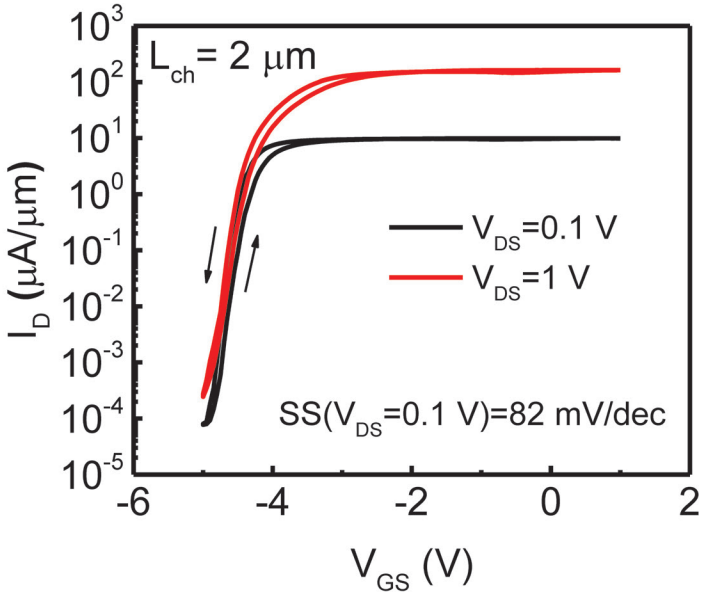

Fig. 5.17. $I_D - V_{GS}$ characteristics of a representative InGaAs NC-FET with 2 µm channel length.

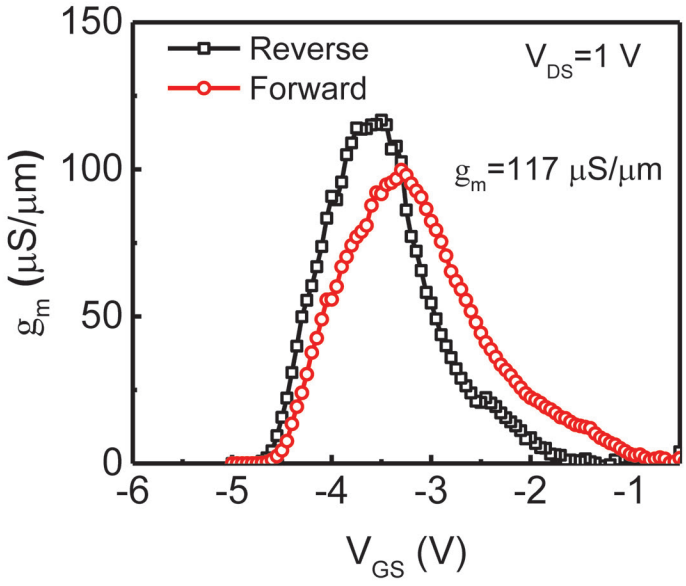

Fig. 5.18. $g_m - V_{GS}$ characteristics at V_{DS}=1 V of the same InGaAs NC-FET as in Fig. 5.17.

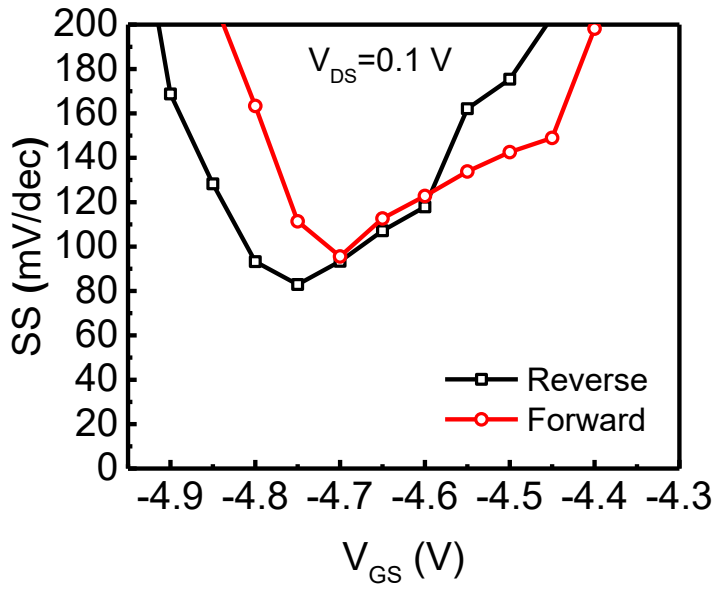

Fig. 5.19. SS versus V_{GS} characteristics at V_{DS}=0.1 V of the same InGaAs NC-FET as in Fig. 5.17.

6. CONCLUSION AND OUTLOOK

6.1 Conclusion

The dissertation explores the post-CMOS device candidates from material and device innovations.

- In chapter 2, fabrication process technology are developed for high performance and ultra-scaled InGaAs nMOSFETs for future high speed and low power applications. In particular, we developed a novel dry etching method to obtain sub-10 nm L_{ch} with L_{ch} down to $\sim$3 nm are demonstrated on both planar devices and FinFETs. Meanwhile, the InGaAs GAA MOSFETs with raised source/drain and ultrathin body structures are studied and performance improvement with thinner body are demonstrated. Forming gas anneal passivation on Al_2O_3/InGaAs interface are studied and confirmed to significantly improve the quaility of Al_2O_3/InGaAs interface.

- In chapter 3, characterization methods on ultra-scaled devices are explored. Firstly, a new and simple method to solve the SCE problem in D_{it} extraction is proposed, which demonstrates a correction to the subthreshold method. Second, low frequency noise and RTN characterizations are used as alternate probes to quantitatively analyze performance, variability and reliability of highly scaled devices. The first observation of RTN in highly scaled InGaAs GAA MOSFETs fabricated by a top-down approach is reported. The $1/f$ noise was found to decrease as the channel length scaled down from 80 nm to 20 nm comparing with classical theory, indicating the near-ballistic transport in highly scaled InGaAs GAA MOSFET.

- In chapter 4, TFETs are studied as a candidate for steep-slope transistors. InGaAs planar and 3D TFET fabrication process are developed. A detailed scaling metrics study (SS, DIBL, V_T, I_{ON}, g_m) are carried out, showing immunity to SCEs with scaled EOT and well-behaved device performance. RTN was observed on InGaAs TFET for the first time, which originates from electron trapping and de-trapping near source-channel junction. Meanwhile, 3D InGaAs GAA TFETs are fabricated with channel length down to 50 nm and studied with different nanowire dimensions. It is found that InGaAs GAA TFETs with smaller W_{NW} have smaller SS, larger I_{ON} and g_m, showing both on- and off-state performance improvement.

- In chapter 5, NC-FETs are studied as another candidate for steep-slope transistors. ALD ferroelectric HZO process is developed and confirmed to repeatable, reliable and reproducible as a ferroelectric insulator for NC-FET applications. Steep-slope MoS_2 NC-FETs are demonstrated by introducing ferroelectric HZO into the gate stack with high drain current, bi-directional sub-thermionic subthreshold slope and negative differential resistance in drain current. The impact of internal metal gate on 2D NC-FETs are also systematically studied. The advantage of III-V high mobility material are also combined together with NC-FET structure and a III-V NC-FET with ferroelectric MOSHEMT structure is demonstrated, exhibiting enhanced performance comparing with the III-V dielectric MOSHEMT.

6.2 Outlook

Material innovations and device structure innovations are currently the main stream in solid-state device research. The current status and the future of device research for logic applications are discussed.

For material point of view, the majorly studied materials are listed as follows,

- III-V, such as InGaAs

- Ge
- 2D materials, such as MoS_2 and BP

However, all these materials are currently experiencing particular problems that limits their possibilities for immediate industrial digital logic applications. The material research for logic device applications will still be driven by solving these problems.

- III-V
  - oxide/interface
  - reliability
  - pFET counterpart
- Ge
  - high performance nFET
  - oxide/interface
  - reliability
- MoS_2
  - single crystal wafer scale synthesis
  - low mobility
  - stable doping technique
- BP
  - single crystal wafer scale synthesis
  - air stability
  - stable doping technique
  - small bandgap in few layers

From structure point of view, the majorly studied novel structures are listed as follows,

- tunneling field-effect transistors
- negative capacitance field-effect transistors

However, all these structures are also currently experiencing challenges that limits their immediate industrial digital logic applications. The device structure research for logic device applications will still be driven by solving these problems.

- tunneling field-effect transistors
  - low on-current in homojunction TFETs
  - large SS in heterojunction TFETs with high on-current
  - defects induced trap assistant tunneling
- negative capacitance field-effect transistors
  - the origin of the negative capacitance is still in debating.
  - time response
  - high speed performance

In summary, although promising materials and device structures are emerging in device research, the ongoing materials and device structures need to address many problems to be used in real CMOS logic applications. The Si CMOS technology will be likely to continue in commercial technology for next 5-10 years. But there are a lot of opportunities for device researchers to explore for the future post-Si CMOS technology from both material and device innovations.

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VITA

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