Control Circuitry for Self-Repairable MEMS Accelerometers

Xingguo Xiong[1], Yu-Liang Wu[2], Wen-Ben Jone[3],
[1] Department of Electrical and Computer Engineering, University of Bridgeport, Bridgeport, CT 06604, USA
[2] Dept. of Computer Science & Engineering, The Chinese University of Hong Kong, Shattin, Hong Kong
[3] Department of ECECS, University of Cincinnati, Cincinnati, OH 45221, USA
Email: [1] xxiong@bridgeport.edu, [2] ylw@cse.cuhk.edu.hk, [3] wjone@ececs.uc.edu

***Abstract*— A BISR (Built-in Self-Repairable) MEMS comb accelerometer with modularized design has been previously reported. In this paper, the differential capacitance sensing circuitry for MEMS comb accelerometer is discussed. The BISR control circuitry based on CMOS transmission gates (TGs) is proposed. Each BISR module is connected to the capacitance sensing circuitry through a transmission gate. By turning *on* or *off* a transmission gate, the corresponding module can be either connected to or isolated from the capacitance sensing circuitry. In this way, the faulty module can be easily replaced with a good redundant module for self-repair. The parasitic model for the BISR control circuitry is also analyzed. The analysis results show that the parasitic capacitance will not affect the proper operation of the BISR control circuitry. Furthermore, the signal strength will not be degraded due to the insertion of analog multiplexers. The control circuitry can effectively isolate the faulty module of the BISR MEMS comb accelerometer. Both BISR and non-BISR MEMS accelerometer designs are suggested and their performances are also extracted for comparison.**

Keywords: MEMS (Microelectromechanical System), redundancy repair, parasitic model, capacitance sensing, accelerometer.

I. INTRODUCTION

MEMS comb accelerometers have the advantages of small size, low cost, low energy consumption and better compatibility with VLSI technology. They have been widely used for many applications such as automobile airbag deployment system, aerospace inertial navigation, consumer products [1]. MEMS comb accelerometers generally contains large number of repeated comb finger groups in a very compact manner. For example, an ADXL50 accelerometer contains 42 differential comb finger groups [2], while an ADXL150 accelerometer contains 54 differential comb finger groups [3]. Such a highly dense comb structure with many long and narrow capacitance gaps is extremely vulnerable to various defects such as particle contamination, stiction [4]. Taking the ADXL50 accelerometer as an example, the length of each movable finger is 120μm, while the capacitance gap between each pair of fixed and movable fingers is only 1.3μm. If a conductive particle with diameter larger than 1.3μm falls into any of the 84 capacitance gaps, it will lead to short-circuit of the device capacitance and result in a failure of the entire device. Thus, a large number of finger groups unavoidably lead to the decrease in yield as well as reliability. Furthermore, for some safety-critical applications (e.g. aerospace, biomedical device), the failure of a small MEMS device may lead to catastrophic disaster or the loss of human life. For such applications, extremely high reliability of MEMS devices is required. In order to improve the yield and reliability of MEMS comb accelerometer devices for safety-critical applications, we proposed a built-in self-repairable (BISR) MEMS comb accelerometer device design [5]. As shown in Figure 1 [5], the main device of the comb accelerometer consists of *n* (n=4) identical modules, and *m* (m=2) modules are introduced as the redundancy. If any of the working modules in the main device is found faulty during a built-in self-test (BIST), the control circuit will replace it with a good redundant module. In this way, the faulty device can be self-repaired through redundancy. Due to the redundancy repair, both the yield and reliability of the MEMS comb accelerometer can be improved [5][6].

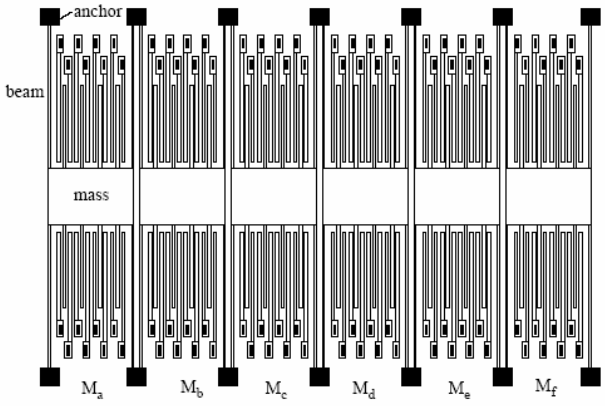


Figure 1. BISR MEMS comb accelerometer design based on redundancy repair

The MEMS comb accelerometer relies on a high-resolution differential capacitance sensing circuit to sense the capacitance change due to input acceleration. Furthermore, a BISR control circuitry is needed for the self-repair of the BISR accelerometer. Whenever a faulty module is found in the self-test, the control circuitry should be able to immediately isolate the faulty module and replace it with a good redundant module. In this way, the whole device is still ensured to work properly. In order to control which modules will be connected as main device, an analog switch (transmission gate) is inserted between each individual module and the capacitance sensing circuitry. By turning *on* or *off* these transmission gates, each module can be either connected to or isolated from the main device. Since the differential capacitance change of MEMS comb accelerometer is generally very small (in the range of fF), the parasitic capacitance introduced by the BISR control circuitry cannot be ignored. It is important to find out how the parasitic capacitance will affect the operation of the BISR device, and whether the faulty module can be isolated effectively once it's identified. In this paper, both the BISR control circuitry and its parasitic model will be analyzed.

II. Circuit Support for BISR MEMS Accelerometer

2.1. Differential Capacitance Sensing Circuit

Various circuit schemes [7]-[11] for signal detection of MEMS differential capacitance sensors have been reported. Among them, capacitance measurement by sensing the current flow through a transducer [11] is very attractive. Due to the high-frequency probe signal utilized, very high sensitivity and speed can be achieved. Further, this circuit scheme is especially suitable for BISR MEMS device, since it ensures better separation of the faulty modules in the BISR device. By turning off the corresponding analog switch, the faulty module will have no contribution to the total current sensed by the OPAMP. Hence, the load effect of the faulty module to the main device can be eliminated. The circuit diagram [11] is shown in Fig. 2.

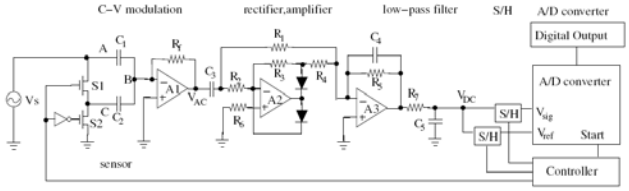


Figure 2. The differential capacitance sensing circuit.

As shown in Figure 2, the sensing circuit [11] consists of five stages: capacitance-to-voltage (C-V) modulation, rectifier and amplifier, low-pass filter, S/H, and A/D converter. A high frequency (1MHz) carrier V_s is used for signal modulation. The differential capacitance of the accelerometer is denoted as C_1 and C_2 separately. The switches S1 and S2 stay in opposite states (on or off) alternately, so that the signal detection circuit senses capacitances (C_1+C_2) and (C_1) in a time-sharing scheme. Assume the OPAMP and switches are ideal, when S1 is on and S2 is off (phase 1), capacitance C1 and C2 are connected in parallel to the voltage source Vs. The output voltage of OPAMP A1 at phase 1 (denoted as V_{AC1}) is:

$$V_{AC1} = -j\omega(C_1 + C_2)R_f V_s$$

This voltage will be converted into a dc signal and applied to the A/D converter as the reference voltage V_{ref}. When S1 is off and S2 is on (phase 2), the capacitance C1 is connected to Vs and C2 is shorted to ground. The output voltage of OPAMP A1 at phase 2 (denoted as V_{AC2}) becomes

$$V_{AC2} = -j\omega C_1 R_f V_s$$

This voltage will also be converted into dc signal and applied to the A/D converter as signal voltage V_{sig}. Thus, the ratio r of V_{AC2} and V_{AC1} is

$$r = \frac{V_{AC2}}{V_{AC1}} = \frac{C_1}{C_1 + C_2}$$

The ratiometric change *x* of the differential capacitance of the accelerometer can be given by [11]

$$x = \frac{C_1 - C_2}{C_1 + C_2} = \frac{2C_1}{C_1 + C_2} - 1 = 2r - 1$$

By measuring the ratio r of V_{AC2} and V_{AC1}, we can know the ratiometric differential capacitance change x. This will in turn be converted into a digital representation by the A/D converter as the final output.

2.2. BISR Control Circuit Design

To support the BISR MEMS structure, the BISR control circuit must be designed to electronically isolate a faulty module and replace it with a good redundant module. This replacement is implemented by a group of analog switches made of transmission gates (TGs) as shown in Figure 3. Here, all six identical modules of the BISR comb accelerometer are labeled with *a~f*. For each module, the pair of differential capacitances are labeled with 1 and 2 respectively. For example, C_{e1} and C_{e2} stand for the differential capacitance pair of module *e*. The selection signals for all six transmission gates are T_a to T_f respectively. The movable portions of all modules are connected together through common anchors, and are directly connected to the OPAMP A1 for signal sensing. The left fixed fingers of each module are connected to the voltage source V_s through an analog switch. The right fixed fingers of each module are connected to the common node of two NMOS transistors. The *on* and *off* states of each transmission gate decide whether the corresponding module is connected or separated from the main device. If the TG is *on*, the voltage source Vs is applied to the working capacitances of the module. The resulted current flowing through the capacitances of the module contributes to the total current sensed by the

OPAMP *A1*. Hence, the module is electronically connected into the main device. If the TG is *off*, the voltage V_s cannot be applied to the working capacitances of the module. Thus, the current flowing through the module is zero, so the module does not contribute any current to the OPAMP input. In this way, the module is electronically separated from the main device. The BISR control circuit sets the selection signals to their appropriate states according to the BIST result of each corresponding module.

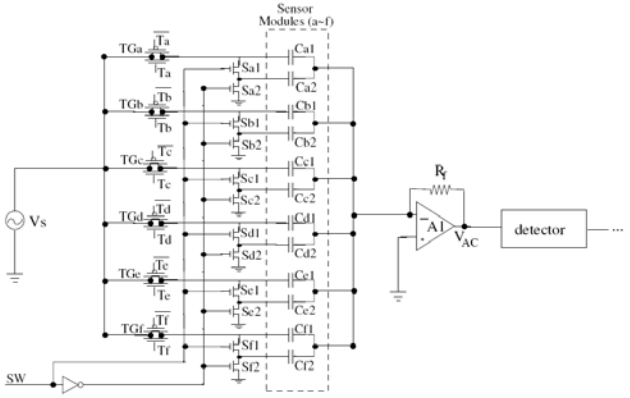


Figure 3. Switching circuit for redundancy repair.

When the device enters the BISR mode, it will first perform the BIST process [12] for each individual module to determine whether it is good or faulty. According to the BIST result, the BISR controller will set the selection signals T_a~T_f to their appropriate values. If any of the four working modules (initially assigned by default) becomes faulty, the BISR controller will set the corresponding TG selection signal of the faulty module to 0 to separate it from the main device. Simultaneously, the BISR controller changes the selection signal of a good redundant module from 0 to 1 to activate it as a working module, and connect it to the main device electronically. After the BISR process is completed, the MEMS device enters the normal mode. During the normal mode, four of the selection signals T_a~T_f are set to "high" and the other two are set to "low". That is, four out of the six modules (restructured by the BISR controller) will be connected as the main device, while the other two modules are separated as either redundant or defective ones.

III. Parasitic Analysis of BISR Circuitry

3.1. Parasitic Capacitance Analysis

Due to the tiny size of MEMS devices, their working capacitances are generally very small (in the range of 1pF or below). The parasitic capacitances of a MEMS device can easily go beyond this value. Hence, it is necessary to find out the influence of the parasitic capacitances, and a parasitic capacitance model needs to be developed for the analysis.

Taking module *a* in Figure 3 as an example, a model taking into account the parasitic capacitances is shown in Figure 4 where all major parasitic capacitances are extracted by ANSYS. Note that C_{a1} and C_{a2} are the differential working capacitances of module *a*, while C_{a10}, C_{a20} and C_{a30} are the parasitic capacitances between the left fixed fingers/right fixed fingers/movable fingers and the ground, respectively. Further, C_{a12} is the parasitic capacitance between the left fixed fingers and right fixed fingers. If the transmission gate TG and both NMOS transistors are treated as ideal switches, in phase 1, S1 is on and S2 is off, and the circuit can be simplified as Figure 5(a). In phase 2, S1 is off and S2 is on, and the circuit can be simplified as shown in Figure 5(b).

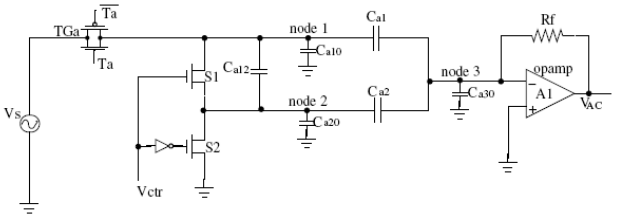
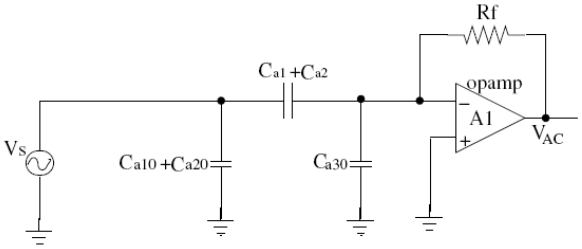
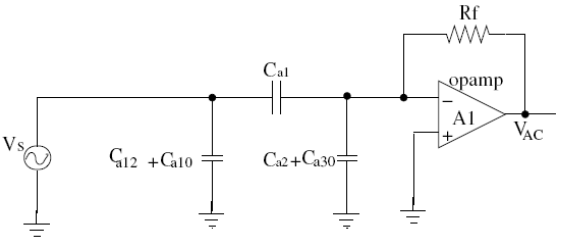


Figure 4. Parasitic capacitance analysis for one BISR module.



(a). Parasitic capacitance equivalent circuit in phase 1



(b). Parasitic capacitance equivalent circuit in phase 2

Figure 5. Simplified parasitic analysis circuit in two phases.

Assume the open-loop gain of the OPAMP *A1* as *A*. The output voltage V_{AC} in phase 1 can be expressed as

$$V_{AC1} = \frac{-V_{in} R_f \omega (C_{a1} + C_{a2})}{1 + \frac{1 + R_f \omega (C_{a1} + C_{a2} + C_{a30})}{A}}$$

The output voltage V_{AC} in phase 2 can be expressed as

$$V_{AC2} = \frac{-V_{in} R_f \omega C_{a1}}{1 + \frac{1 + R_f \omega (C_{a1} + C_{a2} + C_{a30})}{A}}$$

From the above analysis, we can see that only parasitic capacitance C_{a30} has influence on the output voltage, while other parasitic capacitances (e.g., C_{a10}, C_{a20}, C_{a12}) will not affect the output voltage. Since the open-loop gain *A* of an OPAMP is generally very large ($A \geq 10^5$), the denominators of the above two equations are approximately 1. Hence, the influence of parasitic capacitances will not be a problem for signal detection. In reality, the transmission gate and both NMOS transistors cannot be ideal. Although their off-resistances can be treated as infinity, their on-resistance are about 16kΩ and 32kΩ in our model.

In this case, the equivalent circuits of both phases for parasitic effects can be derived. Here, mathematical expressions of the output voltage for both phases cannot be directly accessible, and HSPICE simulations have been used for analysis. The transmission gates and NMOS switches are designed with Magic and extracted for HSPICE simulation. The device parasitic capacitances are extracted through ANSYS. Simulation results showed that the BISR device maintained the same sensitivity (V_{AC2}=6.83mV/g) with and without parasitic capacitances being considered. For example, even when we have C_{a1}=0.15pF, C_{a2}=0.05pF, C_{a10}=C_{a20}=C_{a30}=2pF, the circuit can still work properly for signal detection.

3.2. Analog Multiplexers and Signal Strength Analysis

In the BISR design, transmission gates are used to determine whether a module is connected to or separated from the main device. The output signal of a MEMS device is generally weak due to its tiny size. It is necessary to analyze the possibility of signal degradation caused by the added transmission gates. In order to ensure that the signal strength is not weakened, it is important to avoid passing the MEMS signals through transmission gates. In a MEMS accelerometer, generally, the signal is sensed from the movable portion. Thus, in our BISR design, the movable portions of all modules are intentionally connected together through the common anchors between neighboring modules. They are in turn directly connected to the OPAMP without bypassing through transmission gates. This ensures that the small current signal sensed from the movable fingers will not be degraded. The transmission gates are inserted between the signal source and the left fixed fingers of each module to determine the selection of the modules, as shown in Figure 3. The internal resistance of the voltage source is very small when compared with the on-resistance of the transmission gate R_{on}, which is around 16kΩ. Assume the total capacitance of the MEMS device is about 1pF, and the frequency *f* of voltage source V_s is 1MHz. The impedance of the MEMS device capacitance can be estimated as

$$Z_c = \frac{1}{2\pi fC} = 159.2k\Omega >> R_{on}$$

Thus, the on-resistance of each transmission gate can be ignored when compared with the impedance of the MEMS device capacitance. The signal source V_s can pass the transmission gate without significant degradation.

In summary, all movable plates are jointed together and connected to the signal sensing circuit directly, while a transmission gate is inserted between the left fixed fingers of each module and the voltage source.

In this way, the insertion of transmission gates will not degrade the signal strength sensed by the moving fingers. This has been verified using HSPICE simulation. All transmission gates are designed using *Magic* and the layout is extracted to *HSPICE* for simulation. This ensures that the parasitic effects from transmission gates are all considered. Simulation results show that the BISR device has nearly the same signal strength as the non-BISR device.

3.3. Defective Module Isolation and Load Effect Analysis

The separation of a faulty module from the main device is accomplished through the transmission gates inserted between the left fixed fingers and the voltage sources. As discussed, the movable portions of all modules are physically connected together. When a faulty module is separated out of the main device by turning off the corresponding transmission gate, its movable plate is still connected to the main device. Whether this will cause any load effect to the sensing circuit must be analyzed. According to the working principle of the BISR MEMS structure, the current flowing through the working capacitances in each module will be summed at the input of the OPAMP. If the transmission gate of the faulty module is turned off, there will be no current flowing through the working capacitances of that module. Hence, the contribution of current flow from the faulty module is zero. In this way, the capacitive load of a defective module will not affect the signal strength of the accelerometer. This has been verified with HSPICE simulation. For example, we ever changed the capacitance of a faulty module to different values (very large or very small), and the output signal remains the same as before. This proves that the capacitance of a faulty module will not cause any load effect to the sensing circuit. Even if the capacitance of the faulty module is changed to extremely large or small value due to defects, the output signal of the sensing circuit is still not affected. Further, we introduced a bridging defect by connecting a pair of movable and fixed fingers with a small resistor (0.001Ω), and the output signal is not affected either. This is because the fixed fingers of each faulty module are connected to the insulation layer instead of the silicon substrate. In case of bridging defect between movable and fixed fingers in a faulty module, the fixed fingers of the faulty module just share the same voltage level as the movable plates, and the movable fingers will not be shorted to ground. This demonstrates that the BISR technique is effective to bridging defect between the movable/fixed fingers. Actually the BISR design is effective to almost any

kind of local defect which falls into an individual module. However, for global defects which occur to every module, the redundancy repair cannot be applied since there is no working module.

3.4. BIST Circuit for BISR

In order to implement the built-in self-repair technique of a MEMS device, the device must first perform built-in self-test for each individual module to decide whether it is faulty. The BIST result of each module will be fed into the BISR control circuit. Based upon this information, the BISR control circuit will virtually disconnect the faulty module and replace it with a good redundant module. In this way, MEMS BIST is the prerequisite for MEMS BISR.

Without an efficient and robust BIST solution, MEMS BISR cannot be realized because the control circuit cannot know which module is good and which module is faulty. A dual-mode BIST scheme has been proposed in [12].

Circuit support for the BIST method, especially the voltage biasing scheme, has also been presented in [12]. The proposed dual-mode BIST can serve as an effective BIST solution for the BISR of capacitive MEMS devices.

3.5. Design and Simulation of BISR Accelerometer

The geometry parameters of the BISR comb accelerometer with m=2 and n=4 are listed in Table 1, using a set of design rules comparable to ADXL accelerometers [2]. For comparison, a none-BISR accelerometer with the same number of capacitance groups (as that at the main device of the BISR accelerometer) is also designed. The geometry parameters of the non-BISR accelerometer are also listed in the same table. The simulation results for the performance of both BISR and none-BISR accelerometers are shown in Table 2. From Table 2, we can see that, by narrowing the beam width, the sensitivity loss of the BISR accelerometer due to device modularization can be fully compensated. The BISR accelerometer shows approximately the same displacement sensitivity as that of the none-BISR accelerometer.

Table 1. Design of BISR/non-BISR accelerometers.

Design Parameters	BISR device	non-BISR Device
device area (μm^2)	1500×900	980×900
thickness t (μm)	6	6
no. of capacitance groups	20×6	80
capacitance gap d_0(μm)	2	2
beam width W_b(μm)	2	3.2
beam length L_b(μm)	300	300
mass width W_m(μm)	200	200
mass length L_m(μm)	220×6	880
finger width W_f(μm)	4	4
finger length L_f (μm)	200	200

Table 2. Performances of BISR/non-BISR accelerometers.

Performance	BISR device	non-BISR Device
Sensing mass M_s (μg)	0.84×4=3.36	3.36
Capacitance C_0 (pF)	0.103×4=0.41	0.41
Sensitivity S_d (nm/g)	6.8	6.64
Sensitivity S_c (fF/g)	0.7×4=2.8	2.74
Spring constant k_m *(N/m)*	1.21×4=4.84	4.95
Frequency f_0 *(kHz)*	6.05	6.12

Given a non-BISR accelerometer design, its sensitivity and resonant frequency can be determined. As discussed before, in order to maintain the sensitivity, several alternatives are available. Assume the sensitivity loss is compensated by shrinking the beam width and enlarging the mass width simultaneously. How much should these two parameters be adjusted? The curves of displacement sensitivity S_d v.s. different beam/mass width values are drawn with MathCAD as shown in Figure 6.

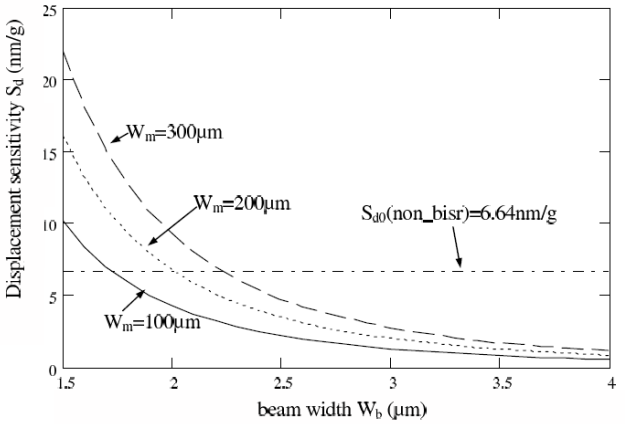


Figure 6. Sensitivity of BISR accelerometer design.

The sensitivity of the non-BISR design is also shown in the same figure as a horizontal line. The cross points between the sensitivity curves and the horizontal line suggest the possible solutions for the BISR design, with the same sensitivity as that of the non-BISR design. The frequency compensation can also be performed in a similar way (Figure 7).

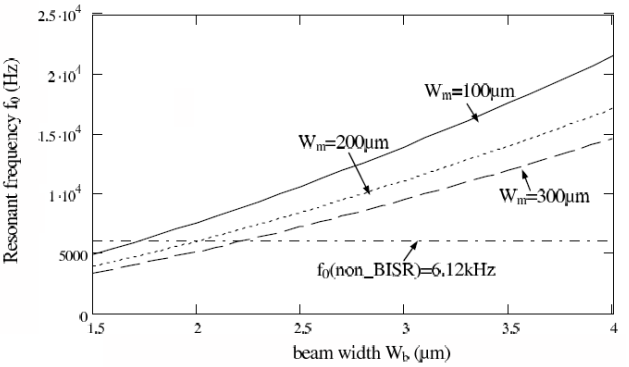


Figure 7. Frequency of BISR accelerometer design.

As shown in Figure 7, the displacement sensitivity of the non-BISR accelerometer is demonstrated as the horizontal line S_d=8.1nm/g.

The beam/mass width of the non-BISR design are 3.2μm and 200μm separately, as given in Table 1. If the beam width of the BISR design is shrunk to W_b=2μm, then displacement sensitivity will be approximately the same as that of the non-BISR device.

ANSYS simulation results for the displacement sensitivities of both non-BISR and BISR accelerometers in response to acceleration from 0 to 50g are shown in Figure 8. For the non-BISR accelerometer, the beam width W_b is 3.2μm. For the BISR MEMS accelerometer, the beam width is shrunk to 2μm. According to Figure 8, the sensitivity of the non-BISR accelerometer (expressed as the voltage output of OPAMP A_1 in phase 2, i.e., V_{AC2}) is 6.68mV/g, while the sensitivity of the BISR accelerometer after compensation is 6.83mV/g. The sensitivity of the BISR device is about the same as that of the non-BISR device.

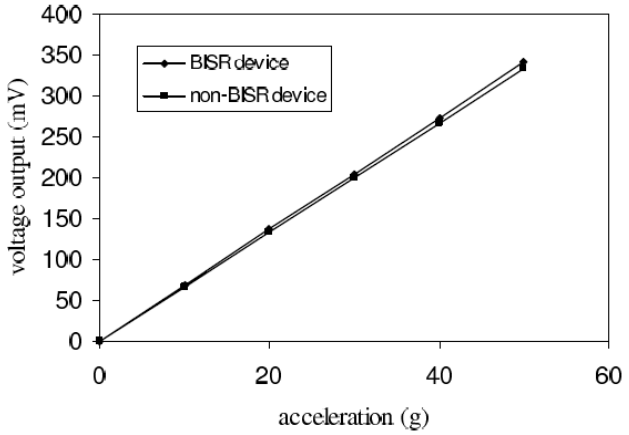


Figure 8. ANSYS simulation results for sensitivity of BISR/non-BISR accelerometers.

IV. CONCLUSIONS AND FUTURE WORK

In this paper, the control circuitry for BISR MEMS comb accelerometer is proposed. A transmission gate (analog switch) is inserted between each individual module and the differential capacitance sensing circuit. Whenever a module is found to be faulty during the built-in self-test, the BISR control circuitry will switch off the transmission gate for the faulty module and turn on the transmission gate of a good redundant module. In this way, the whole device is self-repaired. The parasitic capacitance model of the BISR control circuitry is analyzed. The analysis results show that the parasitic capacitance will not affect the proper operation of the BISR control circuitry. Furthermore, the signal strength will not be degraded due to the insertion of analog multiplexers. The control circuitry can effectively isolate the faulty module of the BISR MEMS comb accelerometer.

In the future work, we will continue to develop the built-in self-test circuitry for the BISR MEMS comb accelerometers. Furthermore, there may be slight differences (e.g. sensitivity, working capacitance, parasitic effects) among the modules due to process variation. As a result, when a faulty module is replaced by a good redundant module, the whole device needs to be re-calibrated. In the future, a built-in self-calibration circuitry will also be developed so that the BISR device will maintain the same sensitivity after redundancy repair.

REFERENCES

[1] Navid Yazdi, Farrokh Ayazi, and Khalil Najafi, "Micromachined Inertial Sensors", *Proceedings of the IEEE*, Vol. 86, No. 8, Aug. 1998, pp. 1640-1659.

[2] W. Kuehnel, and S. Sherman, "A Surface Micromachined Silicon Accelerometer with On-chip Detection Circuitry," *Sensors and Actuators A: Physical*, Vol. 45, pp. 7-16, 1994.

[3] "ADXL150/ADXL250: _5g to _50g, Low Noise, Low Power, Single/ Dual Axis iMEMS Accelerometers", *ADXL150/ADXL250 datasheet*, URL: http://www.analog.com.

[4] B. Stark (editor), "MEMS Reliability Assurance Guidelines for Space Applications", Jet Propulsion Laboratory Publication 99-1, Pasadena, USA, Jan. 1999.

[5] X. Xiong, Y. Wu, and W. Jone, "Design and analysis of self-repairable MEMS accelerometer," *Proceedings of the 20th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT'05)*, Monterey, CA, USA, pp. 21-29, Oct. 3-5, 2005.

[6] X. Xiong, Y. Wu, and W. Jone, "Reliability Analysis of Self-Repairable MEMS Accelerometer", *Proc. of 21th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT'06)*, pp. 236-244, Arlington, VA, USA, Oct. 2006.

[7] S. Ogawa, Y. Oisugi, K. Mochizuki, and K. Watanabe, "A Switched-Capacitor Interface for Differential Capacitance Transducers", *IEEE Transactions on Instrumentation and Measurement*, Vol. 50, Issue 5, pp. 1296-1301, 2001.

[8] S. Chatzandroulis, D. Tsoukalns, "Capacitance to Frequency Converter Suitable for Sensor Applications Using Telemetry", *Analog Integrated Circuits and Signal Processing*, Vol. 27, No. 1-2, pp. 31-38, Apr. 2001.

[9] J. C. Lotters, W. Olthuis, P. H. Veltink, and P. A. Bergveld, "A sensitive differential capacitance to voltage converter for sensor applications", *IEEE Transaction on Instrumentation and Measurement*, Vol. 48, Issue 1, pp. 89-96, 1999.

[10] K. Mochizuki, K. Watanabe, T. Masuda, and M. Katsura, "A Relaxation-Oscillator-Based Interface for High-Accuracy Ratiometric Signal Processing of Differential-Capacitance Transducers", *IEEE Transactions on Instrumentation and Measurement*, Vol. 47, Issue 1, pp. 11-15, 1998.

[11] K. Mochizuki, T. Masuda, and K. Watanabe, "An Interface Circuit for High-Accuracy Signal Processing of Differential-Capacitance Transducers", *IEEE Transactions on Instrumentation and Measurement*, Vol. 47, No. 4, pp. 823-827, Aug. 1998.

[12] X. Xiong, Y. Wu, and W. Jone, "A Dual-Mode Built-In Self-Test Technique for Capacitive MEMS Devices", *IEEE Transactions on Instrumentation and Measurement,* Vol. 54, No. 5, pp. 1739-1750, Oct. 2005.