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# Dual Slope ADC Design from Power, Speed and Area Perspectives

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**Abstract**

The increasing digitalization in all spheres of electronics applications, from telecommunications systems to consumer electronics appliances, requires analog-to-digital converters (ADCs) with a higher sampling rate, higher resolution, and lower power consumption. In this paper, the design optimization of a 8-bit dual-slope ADC from power, speed and area perspectives is proposed. The proposed ADC consists of an analog part (including an integrator and a comparator) and a digital part (including a controller, counter and 8-bit register). Both D and T flip-flops are utilized in the ADC design to demonstrate its influence on area, performance (speed) and power by using different types of flip-flops. The layout of the ADC is designed with Mentor Graphics IC Station. The netlisted is extracted from the layout to include the parasitic capacitances for a more accurate power analysis. PSPICE power simulation is performed to read the power consumption of the ADC for the given inputs. Some efforts on reducing the power consumption of the ADC are also made. For example, the clock signal feeding to the flip-flops is revised to be data dependent so that the clock may be disabled to avoid unnecessary switches whenever it is possible. In this way, the overall power consumption of the ADC is reduced. Double-edge triggered (DET) flip-flops are also used in register circuitry. Since the DET flip-flops trigger at both the rising and falling edges, the clock signal is utilized to the fullest. The proposed dual-slope ADC can be used for applications requiring an optimum chip area, minimum power consumption and excellent performance.

## I. Introduction

If one electronic component is to be nominated as the workhorse inside test-and-measurement equipment, it would be the analog-to-digital converter (ADC). ADCs convert voltages that represent real-world signals into bits that microprocessors and software use to manipulate test data and control test equipment. Even if work is carried out on digital signals exclusively, probably an ADC is used in an oscilloscope to look at the analog characteristics of the signals. Most DMMs, from handheld units to metrology-grade meters, use a very common and simple ADC architecture called integrating type or dual-slope ADCs. DMMs use integrating ADCs because these instruments require high resolution with superior noise rejection. The concept behind the integrating ADC is far less complex than the other types of ADC architectures. Figure 1 shows the basic working principle behind the integrating ADC. The sampled signal, charges a capacitor for a fixed amount of time, usually one power-line cycle (50 Hz or 60 Hz). By integrating over one line cycle, any power-line noise integrates out of the conversion. When the charging time ends, the ADC discharges the capacitor at a fixed rate while a counter counts the ADC's output bits. A longer discharge time results in a higher count.

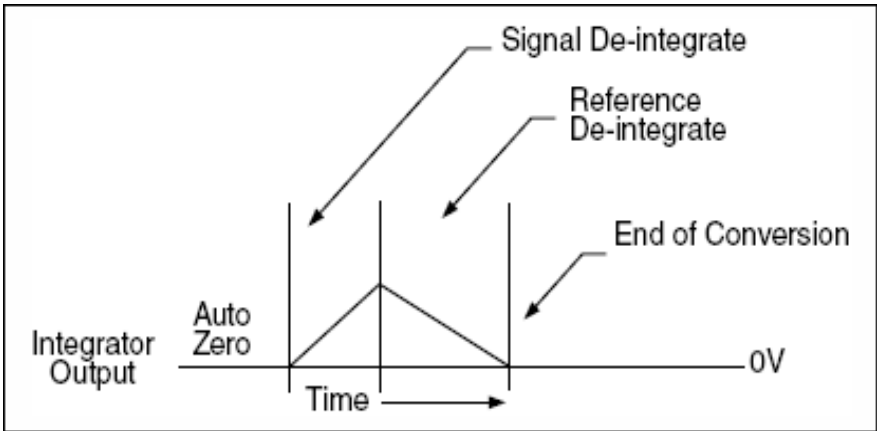


**Figure 1 Integrating ADC**

Integrating ADCs work best in high-accuracy, fine-resolution systems because they remove any power-line frequency noise from the input signal. Integrating ADCs can run at higher sample rates, but as speed increases, noise immunity decreases. Today, most DMMs use proprietary integrating ADC designs. Handheld DMMs with up to 20,000-count resolution (14-bits) often use off-the-shelf integrating ADCs. This research work concentrates on power consumption, area and performance issues in integrating ADC design by investigating and developing techniques and circuit structures suitable for today's and the future's low power technologies. A conventional 8-bit dual-slope ADC is first designed using digital circuit structures such as Controller, Counter and Register using D flip-flops. After functional verification of the circuit, performance and power consumption results are determined from the netlist extracted from the physical layout. Once the satisfactory results are obtained for the conventional dual-slope ADC, now the T flip-flops are implemented for the Counter and DET flip-flops are implemented for the Register. Also the clock for the Counter and Controller circuitries is made data dependent in a way that when the circuit is in a sleep mode, the clock signals are blocked thereby minimizing the power consumption. Mentor Graphics design tools and ORCAD are used for the above mentioned purposes of schematic capture, physical layout, functional verification, netlist extraction and power estimation. Finally, the comparison of the results obtained for conventional and low power dual-slope ADC designs prove that the proposed design has better performance, lesser silicon area requirement and lesser power consumption.

## II. Device Design

The basic block diagram of a conventional dual-slope ADC is as shown in figure 2. As can be seen, the entire unit can be sub-divided into analog and digital sub-units, the analog unit comprising of the Integrator and Comparator and the digital unit comprising of Control Logic, Counter, Switch Driver and Register (not shown). The reference input is applied to the Integrator first, which charges the capacitor for a known value of time (clock cycles) after which the switch driver pulls off the switch and connects it to the primary analog input. Now depending on the magnitude of the analog input, the capacitor discharges after a specific number of clock cycles. The time utilized for discharging the capacitor is converted into the digital output by the counter circuitry. The comparator indicates the end of the conversion cycle, the output of which is utilized by the control logic to drive the digital sub-unit. During the initial phase when the reference input is applied to the integrator, the counter counts the pre-determined number of clock cycles, thereby giving an overflow, which is utilized by the control logic to switch the primary inputs through Switch Driver. During the second phase, the same counter is utilized to count the unknown number of clock cycles and at the end of the conversion cycle, it determines the correct 8-bit digital output. This 8-bit digital output is finally stored in 8-bit Register.

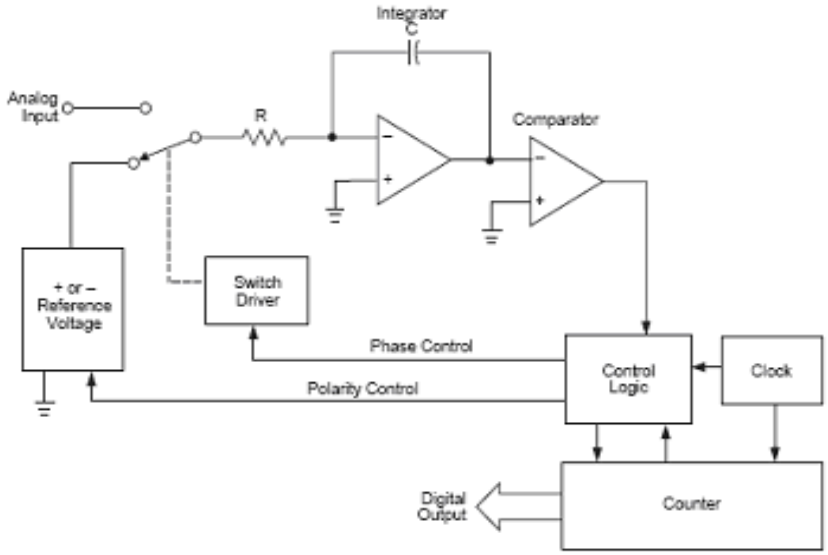


**Figure 2 Dual-slope ADC block diagram**

A two-stage op-amp is used in the analog sub-unit as an Integrator and a Comparator. The integrator uses a resistor at the input, which along with the capacitor in the feedback path integrates the input voltage over a specified period of time depending on the value of the capacitor and the resistor. The output of this integrator is passed on to the comparator, which compares the integrated output with the reference input voltage (which ideally should be zero, but due to the imperfect nature of the comparator, it is a very small fraction of the applied input). Thus, the comparator gives a pulse every time the integrated voltage crosses this pre-defined voltage level. "Two-Stage" refers to the number of gain stages in the op-amp. But actually there are three stages – two gain stages and a unity-gain output stage. The first gain stage is a differential-input single-ended output stage. The second gain stage is a common-source gain stage that has an active load. Capacitor is included (between the output and the input of the second gain stage) to ensure stability when the op-amp is used with feedback. Figure 3 shows the schematic capture of the designed dual-slope ADC.

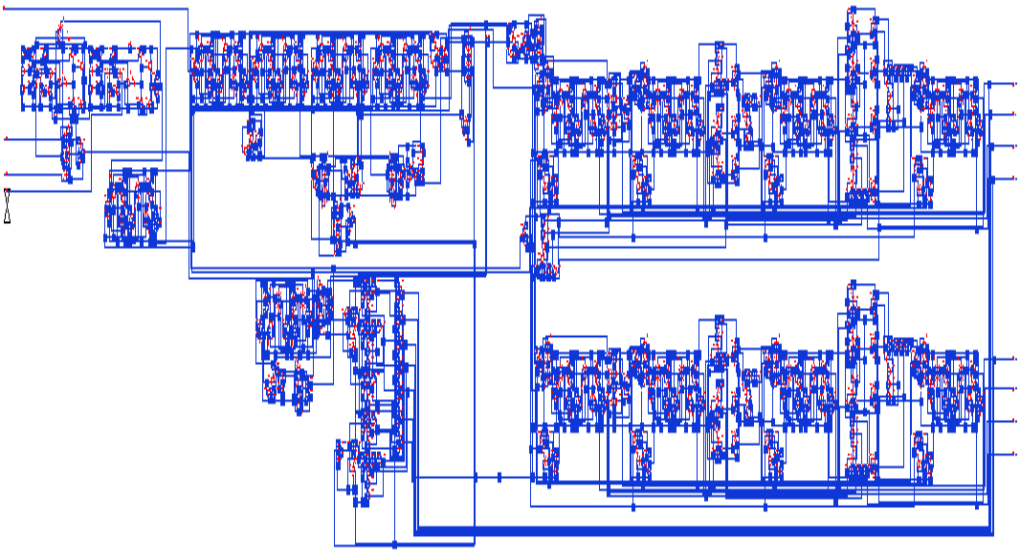

**Figure 3 Schematic capture of the dual-slope ADC**

## II. Performance Analysis and Optimization

The performance analysis for the proposed dual-slope ADC unit mainly takes into consideration the Control Logic, Counter and Register modules. The functional verification is done using Accusim, a tool from Mentor Graphics.

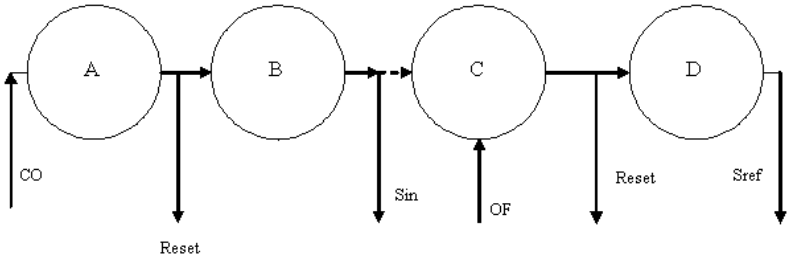


**Figure 4 State diagram for the Control Logic**

Figure 4 above shows the state diagram for the Control Logic. This is the heart of the ADC unit, which controls all the individual blocks in a timely fashion. It is basically a Finite State Machine having four states and uses the output of the comparator unit to control the Digital unit. It can be seen from the state diagram that in state 'A', a signal called "CO" (Comparator Output) is received from the Analog unit or in other words, the controller waits for the comparator's pulse indicating that the capacitor is fully discharged before it sets the counter. Now as soon as it receives the "CO", it resets the counter first so that the digital output doesn't get corrupted. The same output from the state 'A' is taken as input for the state 'B', which sets the Counter through the signal "$S_{in}$". Now the counter starts counting for a pre-defined clock cycles and during that time the capacitor is charged in the analog unit by the reference voltage. The broken line between the output of the state 'B' and the input of the state 'C' indicates that the output of the state 'B' doesn't effect the process in the state 'C' rather it depends on the overflow of the counter and it indirectly helps the counter to know whether it is counting for the pre-defined clock pulses or for the unknown analog input voltage (in which case the counter shouldn't give the overflow in case the capacitor takes more time discharging depending upon the input analog voltage and hence crossing the overflow limit). From state 'C' onwards it is the same cycle but once the counter is reset after the overflow, it knows that it is now counting for the unknown analog input voltage. The necessary logic is included both at the controller end as well as at the counter end by which the controller keeps track of both the counter and itself. Figure 5-a shows the functional verification of the analog unit and figure 5-b shows the functional verification waveforms for the designed Control Logic.

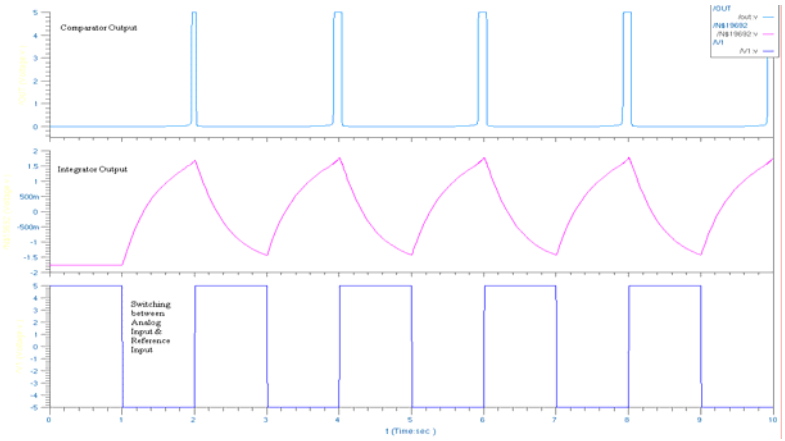


**Figure 5-a Functional verification of the Analog Unit**

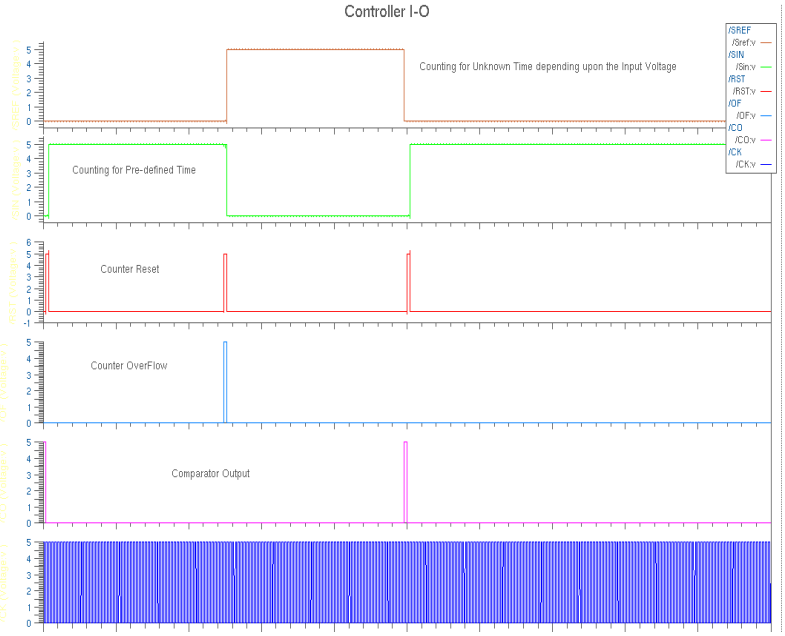


**Figure 5-b Functional verification for the Control Logic**

The Counter unit basically consists of eight flip-flops along with some digital logic. The truth table for a basic 4-bit counter is used as a reference for creating an 8-bit counter unit. Thus, if the D flip-flops are used as is typically the case, K-maps are obtained for the excitation functions, $D_3$, $D_2$, $D_1$ and $D_0$ from the next states. The optimized excitation functions are:

$D_3 = Q_1'Q_3 + Q_2'Q_3 + Q_0'Q_3 + Q_0Q_1Q_2Q_3'$
$D_2 = Q_1'Q_2 + Q_0Q_1Q_2' + Q_0'Q_2$
$D_1 = Q_0Q_1' + Q_0'Q_1$
$D_0 = Q_0'$

From the above realization, the 8-bit Counter unit is easily derived based on the fact that it requires only a 4-input AND gate between the two 4-bit counter units. The second 4-bit unit increments every time the first one overflows and thus gives the full 8-bit binary count. The D flip-flops in the Counter circuitry are a bit different from the ones in the controller circuitry based on the fact that the counter is required to be set and reset and hence includes 2-to-1 multiplexers, which resets all the flip-flops when the 'Reset' signal is issued by the controller. Also each flip-flop has an additional AND gate between its clock terminal and the global clock signal. The purpose of this AND gate is to freeze the clock every time, the Comparator Output is '1'. Doing this allows the exact instant of time when the capacitor in the analog part discharges completely and hence the exact 8-bit digital output is determined. Before the first flip-flop, there is an OR gate and yet another 2-to-1 multiplexer to distinguish between the $S_{in}$ ($S_{ref}$) and the 'Reset'.

It can be seen from the above analysis that even though it is just a 4-bit counter circuit, it requires sufficiently large amount of silicon area due to the heavy combinational logic used therein. The requirement for the proposed dual-slope ADC is 8-bit counter, which will again double the area. If there are flip-flops whose inputs are unchanged when a sequential circuit goes from one state to the next, we can produce a *don't-trigger signal T* from the original state to cutoff the path from the master clock to these flip-flops. As a result, these flip-flops are not subjected to the clock signal and their power dissipation is reduced accordingly. Also it will reduce the additional combinational logic and hence reduce the area as well. Thus the low power counter is designed using T flip-flops, which not only

reduces the area but also minimizes the power consumption as a whole. Table 1 is a new state table using T flip-flops, where the present and next states are Ex-ORed for every flipflop.

| $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ | $Q_3^+$ | $Q_2^+$ | $Q_1^+$ | $Q_0^+$ | $T_3$ | $T_2$ | $T_1$ | $T_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

**Table 1 State table for 4-bit counter using T flip-flops**

From the above state table the four optimized excitation functions are derived using K-maps which are:

$T_3 = Q_0Q_1Q_2$
$T_2 = Q_0Q_1$
$T_1 = Q_0$
$T_0 = 1$

The clock signals for these four flip-flops are:

$Clk_3 = T_3\ clk$
$Clk_2 = T_2\ clk$
$Clk_1 = T_1\ clk$
$Clk_0 = T_0\ clk$

The simple construction of the combinational circuit results in lower power dissipation. However the low power dissipation property is mostly achieved as a result of gating the clock. Besides flip-flop $Q_0$, the three flip-flops $Q_3$, $Q_2$, and $Q_1$ have no dynamic power dissipation when there is no clock triggering. Figure 6 shows the circuit realization for the proposed counter circuit based on the above discussion.

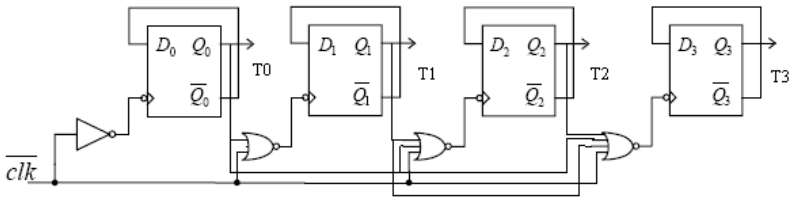


**Figure 6 Circuit realization for a low power counter using T flip-flops**

Figure 7 below shows the functional verification of the proposed low power counter.

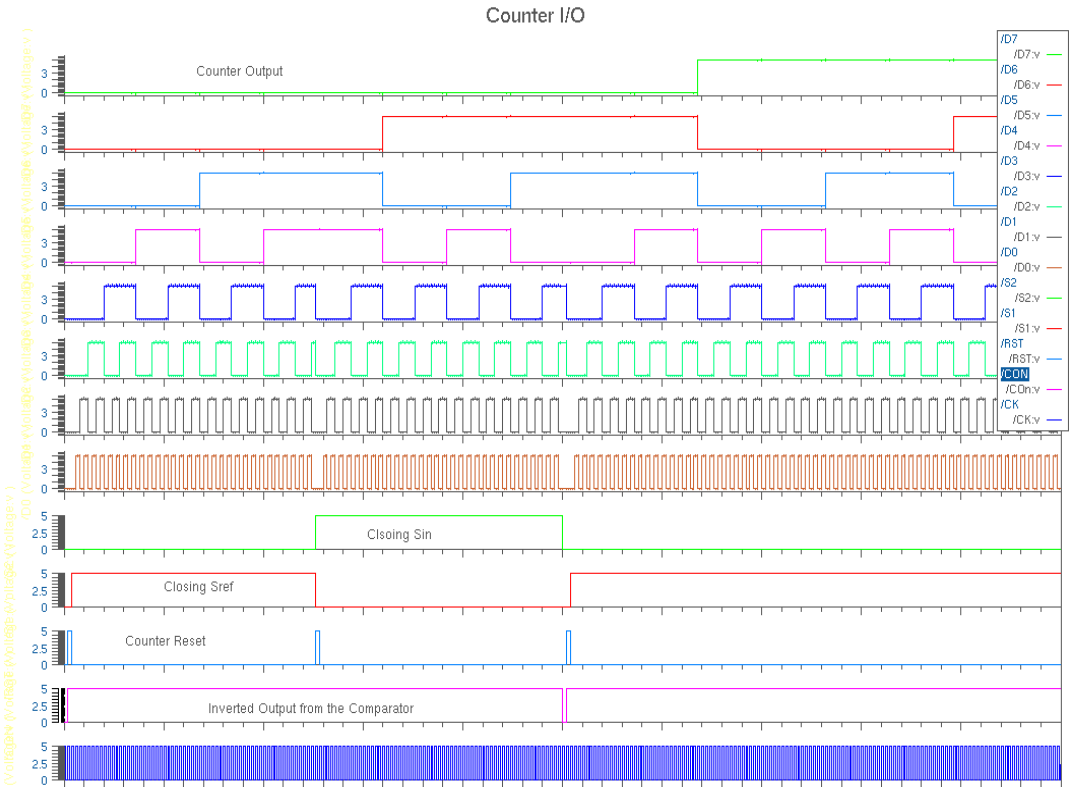


**Figure 7 Functional verification of the proposed 8-bit counter**

As can be seen from the circuit realization and simulation waveforms, the proposed counter uses very few gates as compared to the previous case where D flip-flops were used without taking into consideration the triggering signal. Also since the NOR gates are used, additional inverters are not required as in the case of OR gates. Thus, this architecture not only reduces the power consumption (since number of transistors are reduced as compared to the previous case), but it also reduces the effective chip area (because of the lesser number of gates that are required).

Double edge-triggered flip-flops are becoming a popular technique for low-power designs since they effectively enable halving the clock frequency. While a single-edge triggered flip-flop can be implemented by two transparent latches in series, a double edge-triggered flip-flop can be implemented by two transparent latches in parallel as shown in Figure 8.

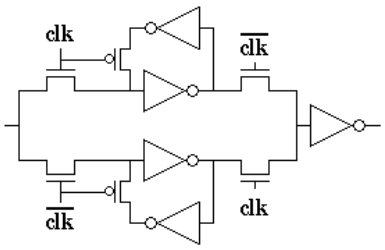


**Figure 8 Double-edge triggered flip-flop**

The clock signal is assumed to be inverted locally. In high noise or low-voltage environments, it is noted that the p-type pass-transistors may be replaced by n-types or that all pass-transistors may be replaced by transmission gates.

Using the above DET configuration the register was designed and it was found that the flip-flops' clock was not only halved but the register could also be made data dependent and hence using this design could save considerable amount of power. But at the same time, it was required to use two input AND gates for every flip-flop in order to make it data dependent so the over all area of the register circuitry is increased as compared to the normal D flip-flop register. But since the clock frequency is halved when using this configuration, the decrease in the power consumption offsets the small increase in the silicon area. Figure 9 shows the simulation of the low power Register using DET configuration.

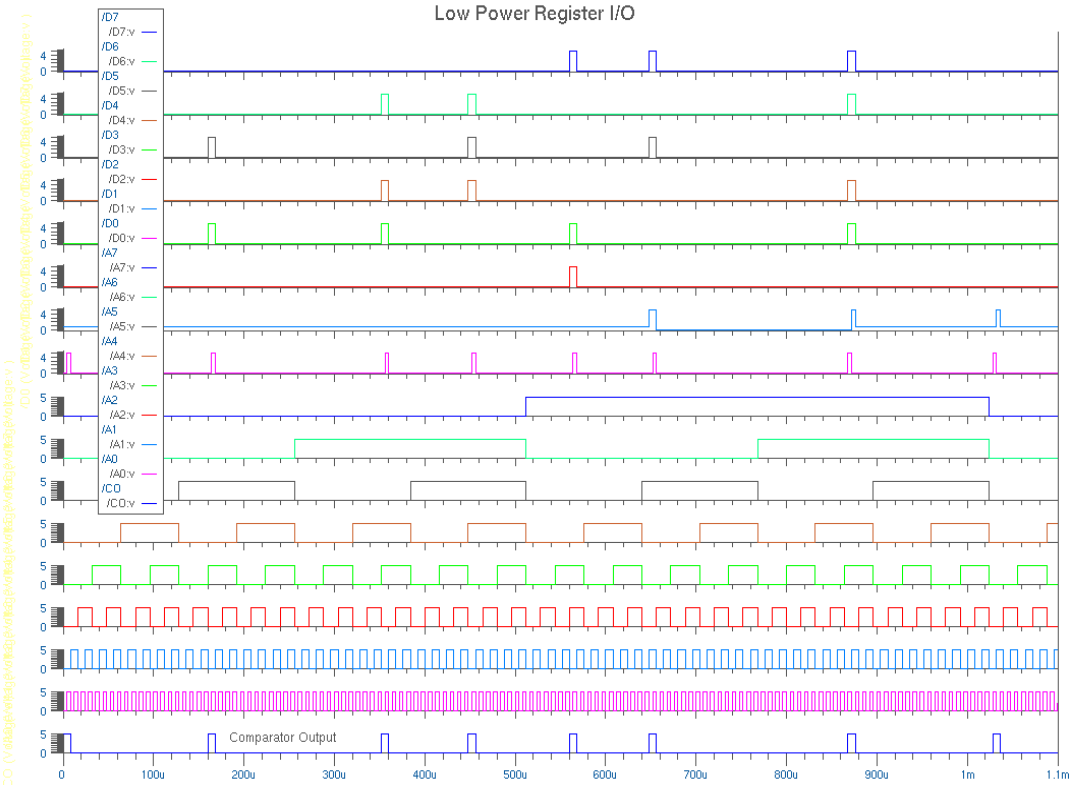


**Figure 9 Functional verification for the low power Register using DET flip-flops**

These flip-flops trigger at both the edges of the clock thereby giving the same data rate at the reduced clock frequency and at the same time saving power. As can be seen from the figure 9, whenever the comparator output is received, the present state of the flip-flops in the counter is stored in the Register. Thus, the clock signal used is halved and is also made data dependent allowing the transistors to switch only when there is an output from the comparator unit. This way the unnecessary switching of the flip-flops in the register due to the clock signal, when there is no data at the input is avoided and hence it saves power.

## III. Conclusions & Future Work

This paper presented the design, area requirement and power estimation of a proposed 8-bit dual-slope ADC in 0.5µm technology. In the proposed design, the Counter and the Register are the only building blocks where low power flip-flops were utilized and these blocks are functionally verified. Remaining

entire logic of the Dual-slope ADC being same, it was concluded that comparing only the Counter and Register units of the conventional and low power ADC units would give a good picture in the performance, speed and power consumption aspects. Thus mainly the comparison considering these aspects is done between these building blocks. Tables 2 show the basic comparison between the two.

| Parameters | Conventional ADC | Low Power ADC |
|---|---|---|
| Area (considering counter & Register circuitry) | X + (410x560)λ | X + (350x440)λ |
| Speed (as soon as the output of comparator arrives) | 390 µs | 220 µs |
| Power (Theoretical) | X | (0.65-0.85)X |

**Table 2 Comparison between the conventional and low power ADCs**

Since the counter and register units involved major contribution to the power consumption due to the clock signal that switches continuously, only these units are considered for the power consumption issues and the effect on the total chip area. Simulation results showed that not only the performance of the proposed circuit is better but it also reduces the power consumed and the overall area. As can be seen from Table 2, the term 'X' represents the rest of the area of the circuit in case of 'Area' comparison and the total power consumption of the conventional circuit in terms of 'power'. The term 'X' refers to the fact that only the counter and the register circuitry are taken into consideration while comparing the area, speed and power of the ADC unit. In CMOS circuits, the dominant component of power dissipation is that which is required to charge or discharge the capacitors in the circuit. The power dissipation of a node in the circuit is expressed by the following equation:

$$\mathbf{P=0.5C_L\ V^2DD\ f_{CLK}\ E_{SW}}$$

where $C_L$ is the physical capacitance at the node, *VDD* is the supply voltage, $f_{CLK}$ is the clock frequency, $E_{SW}$ (referred to as the average switching activity) is the average number of output transitions per clock cycle $1/f_{CLK}$.

Thus, by reducing the number of transistors, the switching activity reduces, which in turn reduces the power consumption of the circuit. Also when the DET flip-flops are used, the clock frequency is halved, this also reduces the power consumption. Thus, power consumption of the proposed circuit is 15% to 45% less as compared to the conventional ADC as seen from the Table 2.

There are many ways to improve the design presented in order to achieve high resolution, high speed and low power. For low power design it is required to look into the analog unit of the ADC unit where it is possible to implement other architectures of an op-amp, which consume less power. Since the analog signal is continuous, it is somewhat difficult to implement a low power consuming circuitry. Besides, the value of the capacitor and resistor used has the time constant of nearly 1ms. This can be reduced to microseconds whereby the clock frequency in the digital unit needs to be increased but doing so may increase the chances of the clock skew so the design parameters in digital unit needs to be further optimized. In case of digital unit, besides using the T flip-flops, one may also use other low power design techniques such as logic shut-down method, where the sections of the entire digital unit which are not being used are shut-down and hence save power. Also in case of the register, bit slicing technique may be used if the design is extended for 16 or 32 bits resolution. As the proposed design is tested under ideal conditions, therefore in order to perform real environment test it is required to add some nonlinearities and see the impact on power, speed and resolution. From the equation on power, it can be seen that if

VDD is reduced, the power consumption can be reduced. One can also use lower voltage or even dual voltage configurations in future in order to make this design more optimized.

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