A Low Power CMOS Comparator Using Logic Shut-down Technique

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Abstract

Low power VLSI has become a very hot area due to the rapid increase in energy cost and wide applications of mobile electronics. Various techniques can be used to reduce the power consumption of VLSI circuits. In this paper, a novel low-power 32-bit comparator using pass transistor and logic shut-down technique is proposed. The comparator will first compare the higher bits of the input patterns. Whenever a decision can be made, the comparison logic for the lower bits will be shut down to save power. The lower bits are compared only when a decision cannot be made from the higher bits. In this way, the unnecessary comparisons are avoided and the power savings can be maximized. Pass transistor logic is also utilized in the comparator design to further reduce the transistor count so that the power consumption can be further reduced compared to CMOS logic. Other comparators are also compared. The schematic design for proposed comparator is designed with PSPSICE. The netlists are extracted and fed to PSPICE for power analysis. An auxiliary power measurement circuitry is introduced to measure the power consumption of the circuits in a smart way. Simulation results show that using pass-transistor and logic shut down techniques can significantly reduce the consumption of the transistor and the power, furthermore, the shrinking signal path are introduced for delay improvement.

Key words: CMOS comparator, lower power, pass transistor

I. Introduction

The comparator is a very fundamental and useful element in digital system which function is used to compare the magnitude of two binary numbers and the final output points that which one is bigger or both of them are equal. This paper describes a novel comparator which inosculates pass-transistor and logic shut down techniques.

Pass-transistor logic is a widely used alternative to CMOS application, which can reduce the number of transistors required to carry out logic in some cases. A very simple example is the implementation of the AND gate as shown in Figure 1. From the schematic, the advantage of reducing the number of transistor appears obviously.

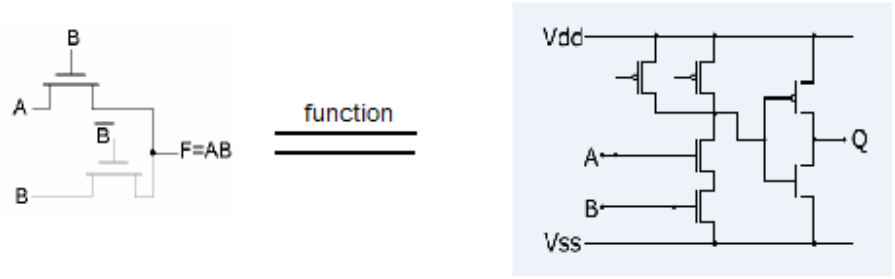

Figure 1. Comparison of PTL and complementary CMOS logic for AND gate

Logic shutdown technique using pre-computation is a kind of efficient way to reduce the power consumption. The basic idea is to identify logical conditions at some inputs to a combinational logic that is invariant to the output. Since those input values do not affect the output, the input transitions can be disabled to reduce switching activities.[8] The proposed 32bit comparator is primarily introduced by combining these two techniques.

The rest of the paper is organized as follows. Section 2 illustrates several existing comparator structure. Section 3 describes the proposed comparator. In section 4, the simulation results and comparison presented.

II. Existing Comparators

From the aspects of the architecture of the circuit, the exiting comparator can divided into serial and parallel structured comparator.

The first design as shown in Fig. 2 is a serial architecture [1]. It is a very concise circuit by using transmission-gate logic (TGL) to control all the carry out in a chain. This chain plays a significant role that it will hold all the other bit position expect the fist unequal bit accounting to the corresponding two numbers from MSB to LSB. But the problem is the serial architecture comparator is only excellent with short inputs. For the longer inputs, the chain needs to assemble more serial transistor for bunching all the inputs which will increase the delay and limit the operation speed.

The second design as shown in Fig. 3 is a parallel architecture. This comparator is an evolvement from a conditional adder, which can save more than 50% amount of transistors of classic comparator [3]. But the disadvantage is the more bits compared, the more MUXs needed. A 32bits comparator of this structure needs 57 MUXs.

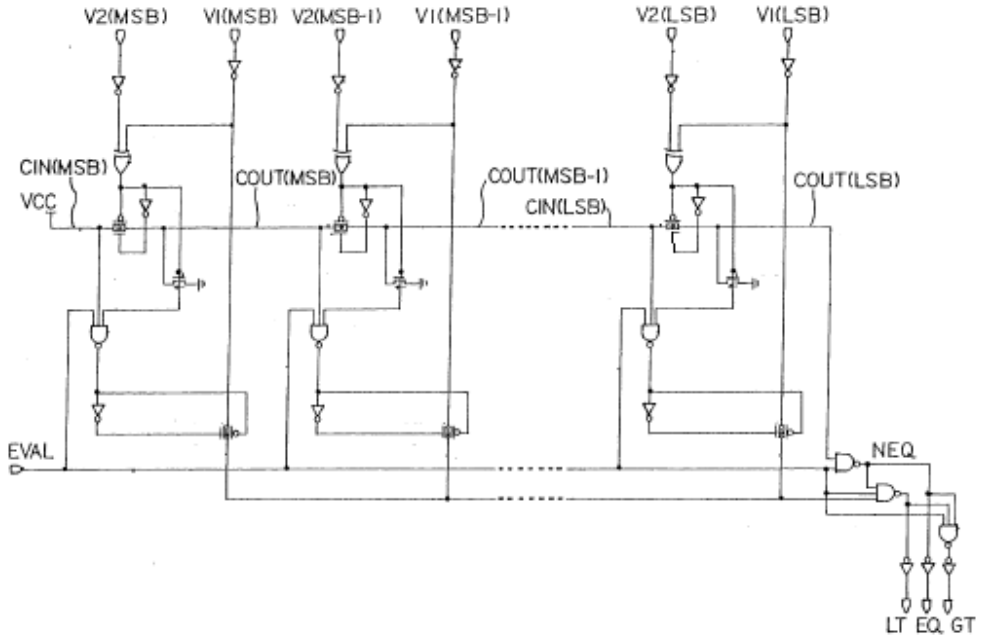

Figure 2. Existing serial comparator [1]

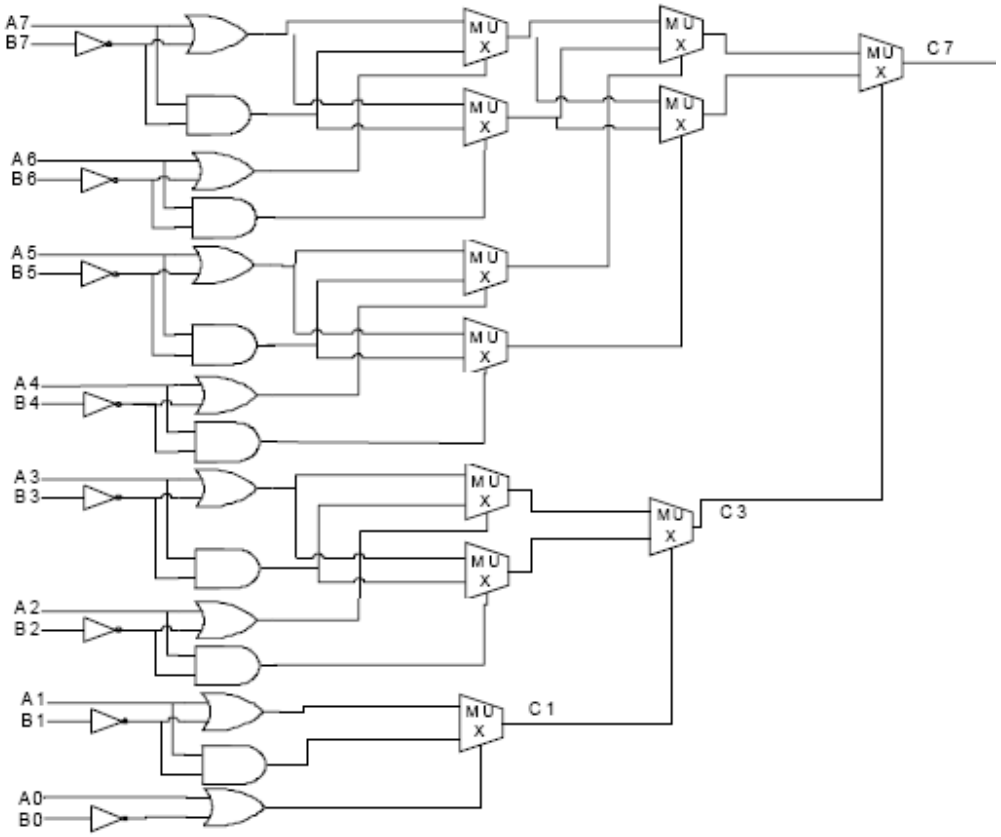

Figure 3. Existing parallel comparator

The third design is also based on parallel architecture, but uses 2 stages processing as show in fig. 4. Take this kind of 16 bits comparator as an example, in the 1st stage, it contains four 4-bit PEB comparators, each comparator will output a 4 bits comparison result according their priority. In the 2nd stage, 4 outputs from 1st stage will transfer into one 4-bit PEB for further comparison and output the final result. The huge improvement is benefit from its concise xor gate and priority-encoding structure which can reduce the layout area and power-dissipation. But a long data pass still limits its operation speed. The proposed comparator in this paper is based on this comparator.

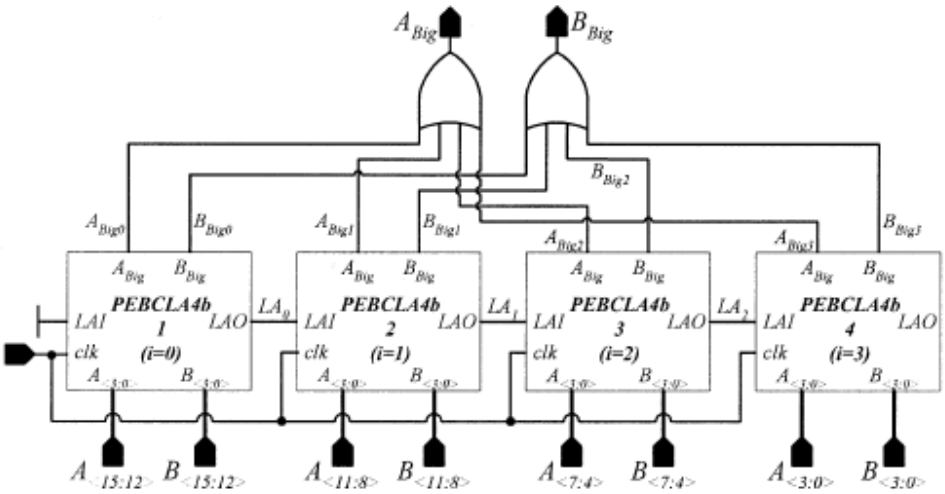

Figure 4. Existing 2 stage parallel comparator

III. Proposed Architecture and Results

The function of the proposed comparator is orderly comparing two binary inputs from higher bit, if one couple is dissimilar, circuit restrains all lower bits at input point though logic shut down and sends this couple to output though pass-transistor lead A_{big} or B_{big} to be 1 according to the practice; if no couple is dissimilar means these two number is equal, then output EQUAL will be set to 1.

Firstly, the principle will be illuminate in this part. The most basic component is a 4-bits comparator, which includes three parts: priority-shut-down (PSD) part, feedback-selection (FS) part and MUX part as shown in figure 5. Assume the two numbers A and B are A1101 and B1010. In the first step, the circuit will compare highest bits of inputs using XOR gate, according the assumed inputs A1101 and 1010 that both inputs' highest bits are 1, then feedback to the PSD, which will introduce next bits pattern into FS. Then, there will be a difference according to the pattern (1,0). The FS will feedback to the PSD restrain all lower input and let MUX select this pattern pass though and hold all other inputs.

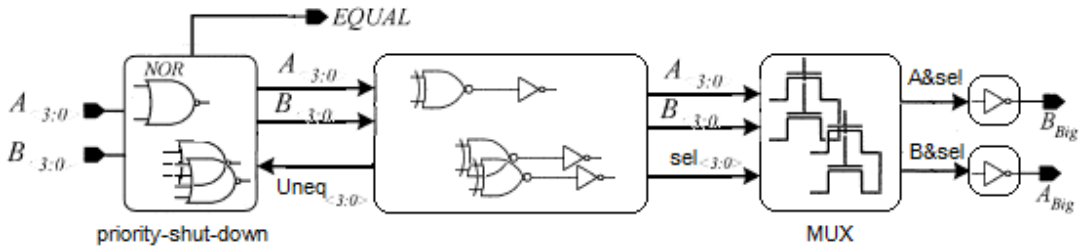

Figure 5. Principle block diagram

The functions of the logic signal Uneq and sel are implement as the following equations.

$$Sel_3 = Uneq_3$$

$$Sel_2 = \overline{Uneq_3} \cdot Uneq_2$$

$$Sel_1 = \overline{Uneq_3} \cdot \overline{Uneq_2} \cdot Uneq_1$$

$$Sel_0 = \overline{Uneq_3} \cdot \overline{Uneq_2} \cdot \overline{Uneq_1} \cdot Uneq_0 \quad (1)$$

The function of A&sel and B&sel follow the rules shown below.

$$A\&sel = A_i \cdot sel_i$$

$$B\&sel = B_i \cdot sel_i \quad (2)$$

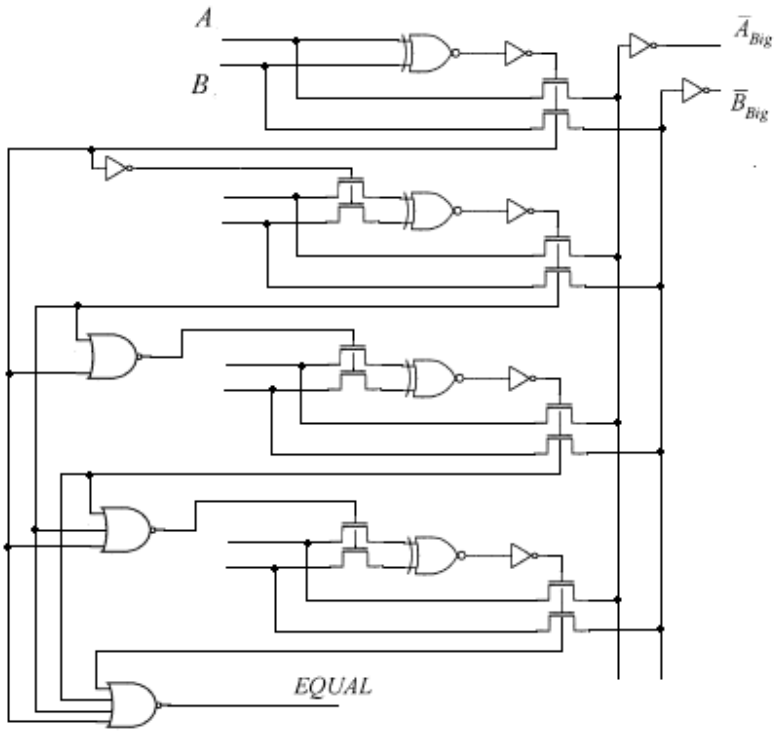

Figure 6. Schematic diagram of a 4-bit proposed comparator

The 32-bit comparator is structured by serially connecting a 4-bit comparator as a second step with four parallel connected 8-bit comparators as a first step.

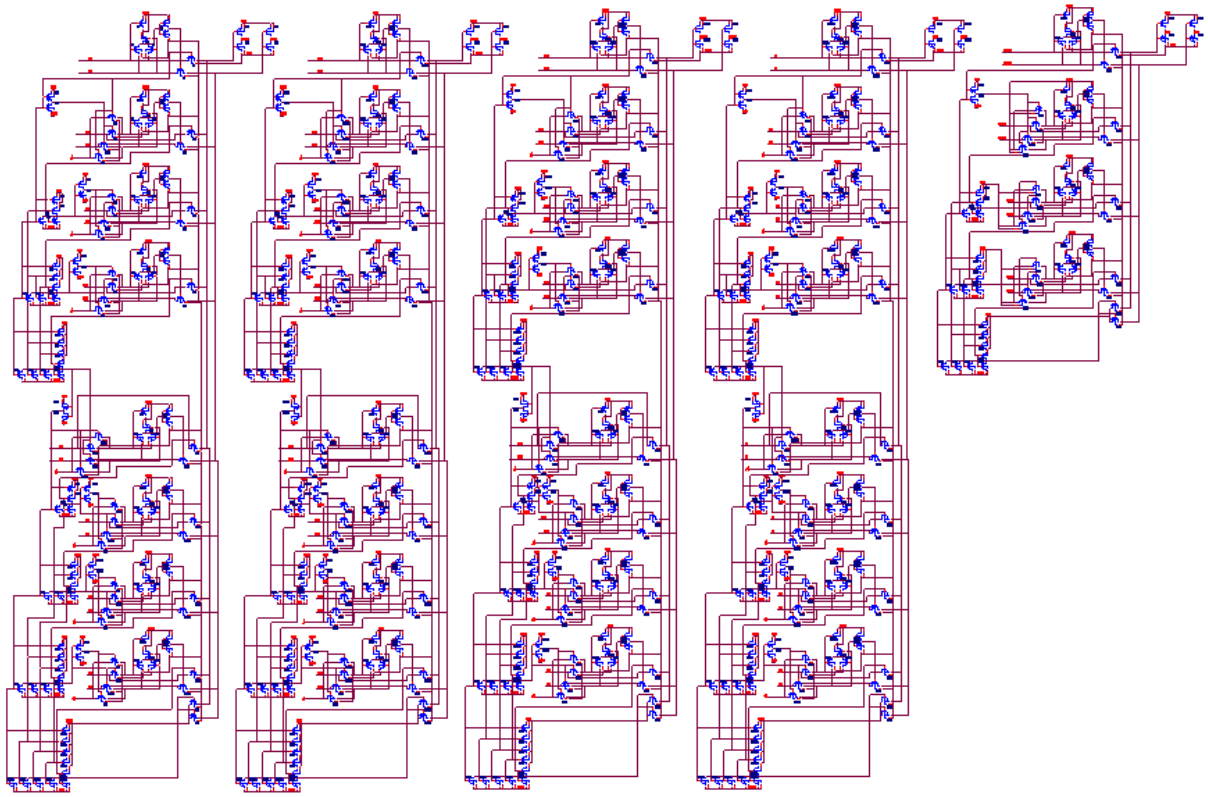

Figure 7. Schematic design using PSPICE

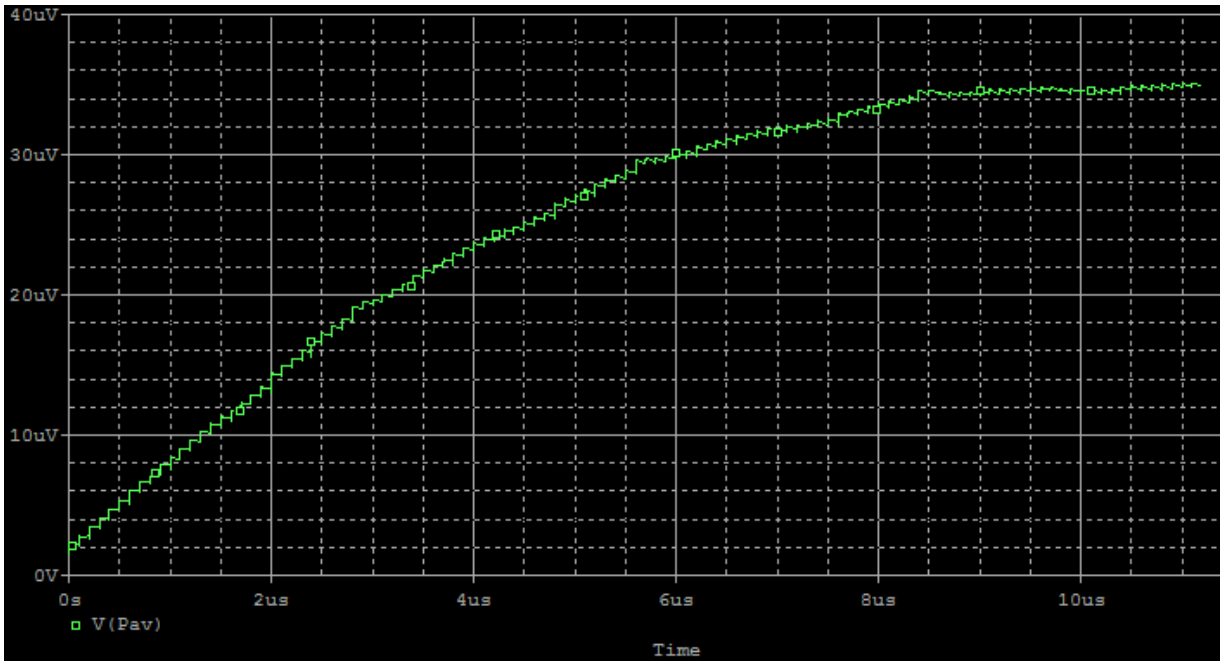

Figure 8. Power simulation using PSPICE

Power consumption after 112 input patterns are shown in figure 8. The testing input patterns are arranged for average situation that each 8-bit sub-comparator severs 14 alternating inputs. The power consumption is approximate 36μw.

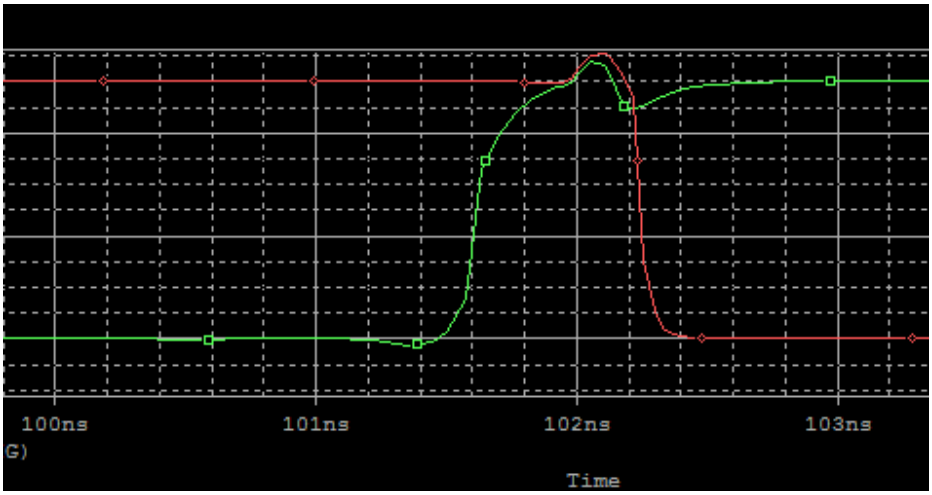

Figure 9. Worst cases delay

32-bit comparator design	Transistor count	Propagation delay
Chu-Chin Wang's comparator, IEEE Proceedings, 1998 [4].	926	6.3 ns
Chung-Hsun Huang's comparator, JSSC, Feb. 2003 [2].	912	5.4 ns
Shun-Wen Cheng's comparator, ICECS, 2003.[3]	752	4.2 ns
The Proposed comparator.	618	2.8 ns

Table 1. transistor count and simulation comparison of 32-bit comparators

IV. Conclusions

In this paper, a novel low-power 32-bit comparator using logic shut-down technique is proposed. The comparator will first compare the higher bits of the input patterns. Whenever a decision can be made, the comparison logic for the lower bits will be shut down to save power. The lower bits are compared only when a decision cannot be made from the higher bits. In this way, the unnecessary comparisons are avoided and the power savings can be maximized. Pass transistor logic is also utilized in the comparator design to further

reduce the transistor count so that the power consumption can be further reduced compared to CMOS logic. Compared to other comparator designs, the proposed design use less amount of transistors and simulation results demonstrate that its propagation delay is also smaller than other designs. The proposed comparator has improved performance with lower power consumption.

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