Glitches in Digital to Analog Converters

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Abstract

Digital-to-analog converters (DACs) are widely used for signal processing and other applications. A popular Digital-to-Analog Converter (DAC) topology is the R-2R ladder. It is a simple topology which consists of only two resistors and a switch per bit, and typically one OPAMP buffer at the output. However, such a topology is vulnerable to glitches (voltage spikes) that may occur when several bits in the digital input change at the same time. Although a DAC is often followed by a Reconstruction Filter (RCF), this filter may need to be of a high order to attenuate the voltage spikes sufficiently. Such a filter increases the size of the die in an integrated circuit (IC), or requires more spaces, components and increases cost for a printed circuit board implementation. In some applications, such as an analog control signal to a valve, the filter may not even be necessary, but it is probably desirable to not have glitches. In this work some alternative topologies that eliminate glitches are considered, primarily DACs based on R-2R ladders that accept Gray code input.

Discussion

One of the most common Digital to Analog Converter (DAC) topologies is the R-2R ladder. For each bit, the R-2R ladder consists of a two-pole switch and two resistors, one of size R, and the other of size 2R. The chain is terminated by an additional 2R resistor, and an Opamp buffer is typically used. The obvious benefit of this topology is that the size of the circuit scales linearly with the amount of bits. While the bit width can be increased by adding an additional R-2R, the matching of the resistors typically limit the accuracy that can be achieved with the R-2R ladder. Glitches, in the form of voltage spikes, can occur in the R-2R ladder when several switches change state at the same time. As explained in [2], the predominant case is when the Most Significant Bit (MSB) has a different value than all the other bits, and the input code changes such that all bits change value. E.g. for an 8-bit DAC, going from 10000000 to 01111111, or 01111111 to 10000000.

Two interesting topologies were presented in [1], which are R-2R ladders that have been altered in a way such that they can accept Gray Code input. By using Gray Code the glitches described for the R-2R ladder can be reduced, for a signal that increments with only 1 value at a time, because only 1 bit changes at a time in Gray Code for increments of 1.
Little research is available on the topic of Gray-code DAC ladders. The patent in [1] dates back to 1986, and has expired by now, so the topologies described in patent are free to be used.
There are some academic papers that describe DAC architectures that utilize Gray-code in some way, but they are rather application specific, and none of them have the simplicity of the R-2R ladder. An example is the DAC in [3], which is designed for Cellular Nonlinear Networks (CNN). A CNN cell is a mixed analog and digital electronic cell, that can operate in a network of other cells, in a way that is inspired by biological neural networks. The DAC share some similarities with a successive approximation ADC. A current ramp signal is generated, converted to digital, and compared to the digital input value. When the values match, the current signal is "frozen" in a current mirror, and sent to the output. The digital signals are all in Gray-code.
A disadvantage with this DAC, is that it has to try many combinations, maybe all of them, before reaching the right value. So it is relatively slow, and increasing the bit-width makes it slower. Another topology that incorporates Gray-code is presented in [4]. This is basically a pipelined DAC that is changed to take Gray-code input. When the digital input propagates through the pipelined, each bit adds a voltage of VREF, which is then multiplied by 1⁄2 per stage, just like in a normal pipelined DAC. The difference is when two consecutive bits are one, e.g. the LSBs are 11. Since 11 in Gray-code corresponds to 10 in binary, the LSB here is converted and then subtracted. This subtraction helps combat offset voltage, because offset voltages are also subtracted, and that is the rationale for converting using Gray-code in this converter. None of these DAC architectures have much in common with the Gray-code R-2R architecture, and they make use of Gray-code for different reasons than to combat glitches in the output.
Therefor, the main purpose of this thesis is to explore the application of Gray-code DAC ladder,
discover what are the advantages and disadvantages over the conventional R-2R DAC ladder,
which accuracies can be achieved, and what impact different circuit parameters, such as the
switches on-resistance and resistor mismatch, have on the performance of the Gray-code R-2R
DAC ladder. And of course, if there are any ways to improve any of the known circuit
topologies.
The research is primarily done from the perspective of CMOS VLSI design.
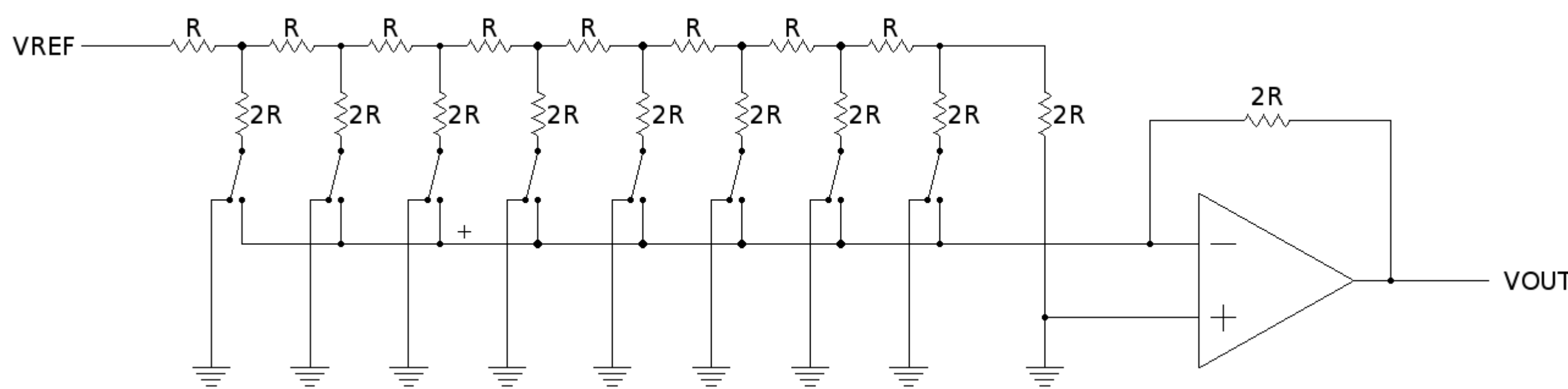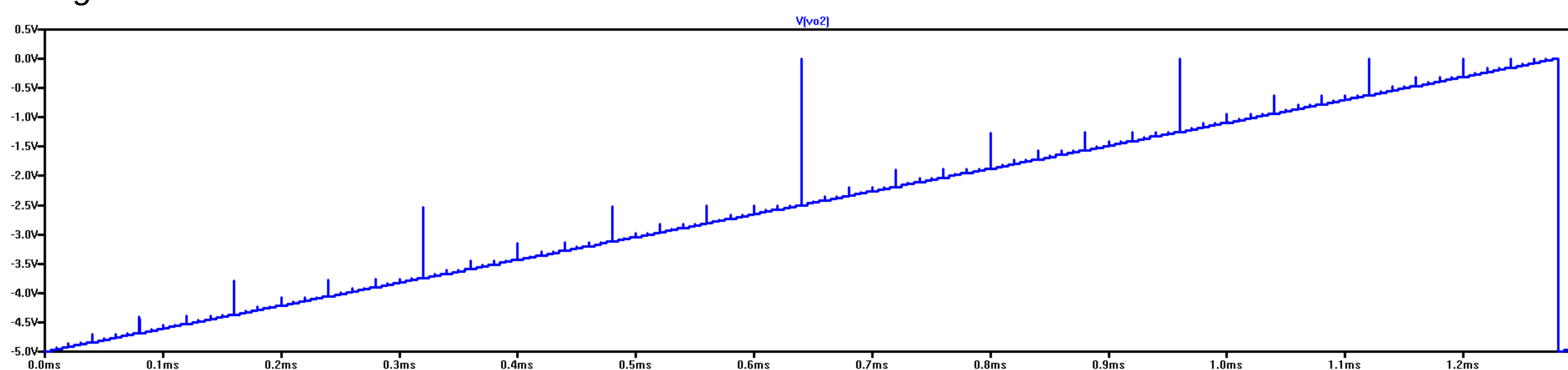
Figures

Figure 1: A traditional R-2R DAC.

Figure 2: Transient simulation of the R-2R DAC in figure 1, which demonstrates the glitches (voltage spikes) that may occur in this topology.
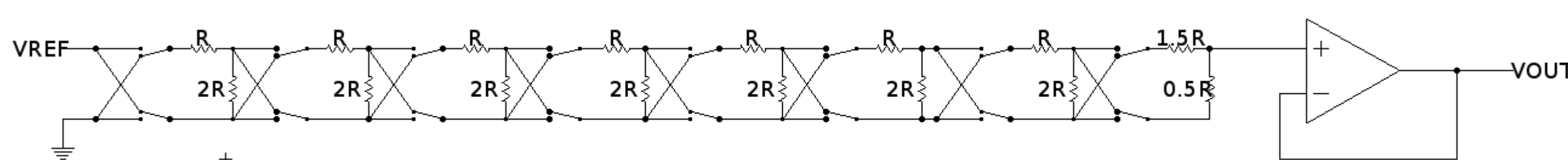

Figure 3: A gray code R-2R DAC, as described in [1]. Each input bit controls a pair of two-pole switches, and the input has to be gray coded.
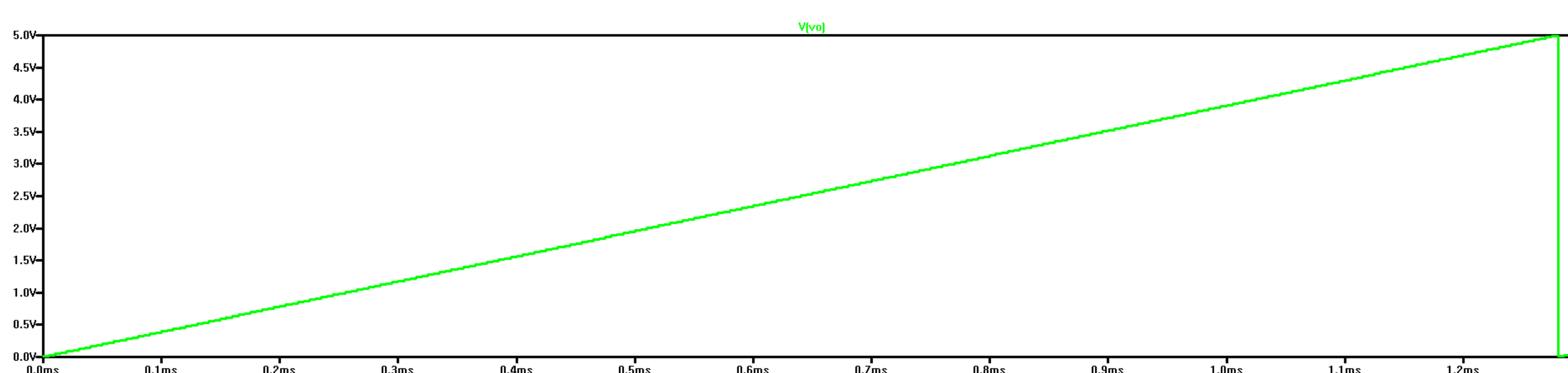

Figure 4: Transient simulation of the gray code R-2R DAC in figure 3. The output of this DAC is glitch free (for single increments),

References

[1] N.C. Seiler. *Gray code DAC ladder*, US Patent 4,591,826, 1986.

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[3] Vesalainen, L.; Poikonen, J.; Paasio, A., "A Gray-coded digital-to-analog converter for a mixed-mode processor array," Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on , vol., no., pp.3930,3933 Vol. 4, 23-26 May 2005

[4] Uddin Shaber, M.; Signell, S., "Pipelined DAC architecture using gray coding," NORCHIP Conference, 2005. 23rd , vol., no., pp.141,144, 21-22 Nov. 2005