# An Efficient Scheme for Traffic Management in ATM Networks

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***Abstract*— As ATM network is designed for broad band transmission that is high data rate (25 Mbps to 2.5 Gbps) and supports the transmission of every kind of data, congestion control and delay have been important issues for ATM networks. Data transmission is done in the form of cell (53 bytes) relay. Hence, cell sequence and the error control have to be carried out properly. ATM networks presents difficulties in effectively controlling congestion not found in other types of networks, including frame relay networks. In this paper, we present an efficient methodology for traffic management. The simulation results suggest that the proposed solution is effective for both slow and high data rate transmission.**

*Keywords*— ATM network, broad band transmission, congestion control, transmission delay

## I. Introduction

International Telecommunication Union (ITU) has defined a restricted initial set of traffic and congestion control capacities aiming at simple mechanisms and network efficiency as follow. That sets the upper bound to the traffic, variability in the pattern of cell arrival and average rate of ATM connection.

1. Connection Admission Control.
2. Usage Parameter Control.
3. Priority Control.
4. Fast Resource Management.
5. Selective Cell Discarding.

Apart from that, ATM switch is important network device in ATM network for congestion and traffic control. That switches virtual circuit identifier (VCI) from left to right. It contains buffers and switching circuits to guide the connections.

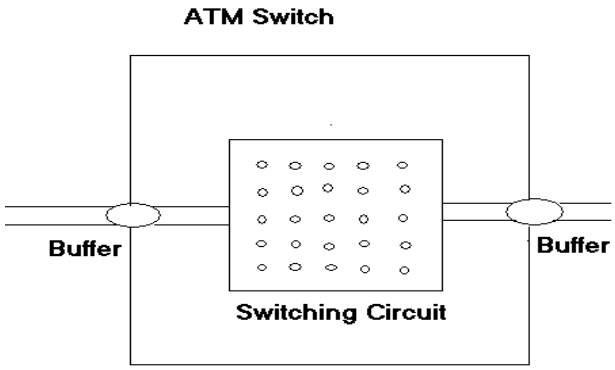


Fig. 1. Switching Architecture

### A. Problem Statement

Traffic from user nodes can exceed the capacity of the network, which causes memory buffer of ATM switches to overflow and data loses. As per high data rate of transmission, cell storage and traffic management is required in ATM switches.

The restrictions of ITU-T can be managed by upgrading the performance of ATM switches. ATM switches takes a time to process each cell's VCI through switching circuit and referring to the routing table instead of no time. That affects the continuity of the cell transmission.

ATM switches do outgoing buffering if more than one cells have same VCI, which leads to defer in transmission and affect the CBR (Constant bit rate). That results in retransmission or poor performance at receiver side especially in case of video-audio data.

## II. Proposed Solution For An Efficient Traffic Management In ATM Networks

Small buffers of ATM switches can be replaced with large memory blocks.

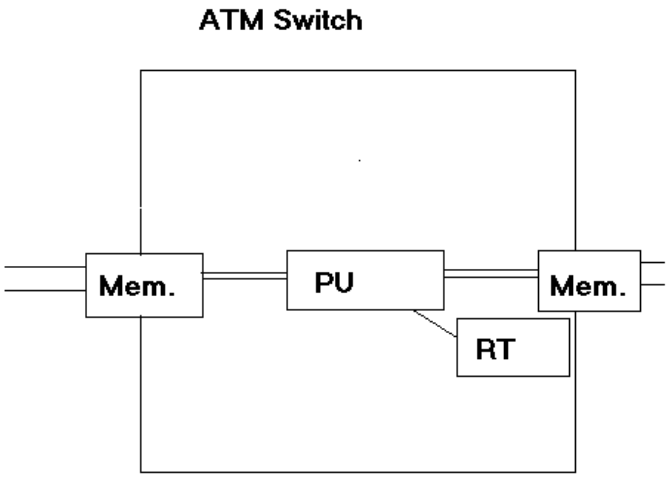


Fig. 2. A conventional ATM switch with replacement of switching circuit

### A. *Replacing Switching Circuit*

ATM switching circuit can be replaced with processing unit, which has capability of processing cells, just like CPU. By processing unit cells are transmitted faster or no time and provides continuous flow of transmission. Routing table is allocated in memory of processing unit. That does congestion control and speeds up the transmission of outgoing cells so that less buffering is required. Due to less buffering and no data lose, retransmission is not needed to perform.

### B. *Removing Output Buffers*

Another important issue, to fasten the transmission is to prevent the output buffering. ATM switches buffer the out going cells, if they have same VCIs. Processing unit can process those cells at a time that have different VCIs. And the resulting (outgoing) VCIs of those cells will be different.

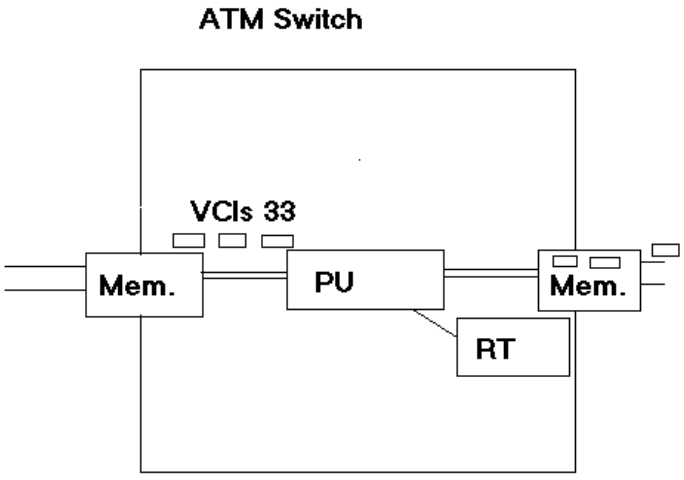


Fig. 3. A conventional ATM switch without output buffer

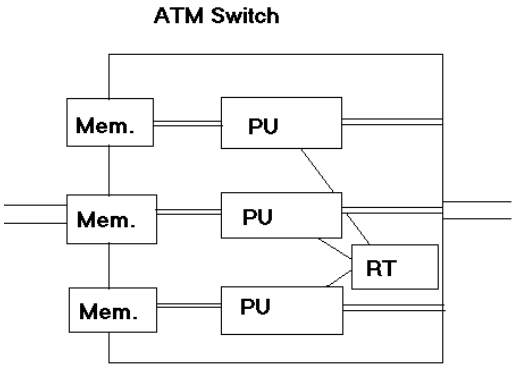


Fig. 4. An scalable ATM switch architecture

PU- processing unit.
RT- routing table.
Mem.- memory block.

Hence, outgoing cells need not to be buffered

## III. Proposed Solution For Traffic Management In ATM Networks

### A. *Scalability*

Moreover, if there is higher bandwidth, it is needed to minimize the buffering. For that, processing unit can be scaled through transmission in ATM switch. More than one processing units are implied in ATM switches. At a same time, more that one cell can be processed. Incoming flow is divided into the number of channels and assigned to the processing units having their own memory blocks.

## IV. Proposed Offset Mechanism In Routing Table

Processing unit may take some execution time to access the outgoing VCI. Instead of searching through whole routing table, table can be divided into segments having offsets. Each cell can refer to addressing table to access the offset. And using that offset outgoing VCI can be defined. Thus, instead of searching nine rows, each cell has to refer to only three rows. That way it fasten the access of VCIs and transmission of cells.

### A. *Error Control Integration*

Secondly, HEC algorithm can be implemented in ATM switch instead of in receiver. If data is corrupted in cells, that will be discarded by ATM switches. That results in improvement of quality of service in transmission.

### B. *Mathematical Model*

CBR of network depends upon the constant duration of time between arrivals of two subsequent cells to receiver.

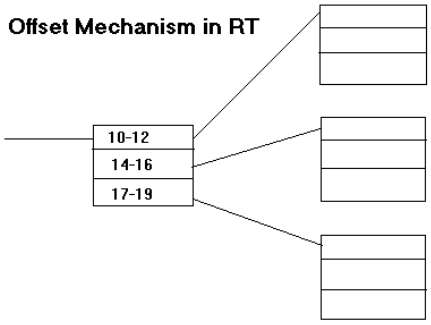


Fig. 5. A proposed approach for offset mechanism for ATM networks in RT

That, cell duration is defined as

$$\delta = 1/R \quad (1)$$

Where R= Data rate.

Hence, as data rate is higher, quality of service and CBR can be improved. And higher cell duration (δ) affects the quality of service badly.

CBR can be defined as,

$$CBR \rightarrow C\ R \quad (2)$$

Where R= Data rate, C= Channel capacity

**Case- 1**
Suppose if the velocity of cell across the medium approaches 300 km/s, then the following conclusion can be drawn:

Average holding time of ATM switch with switching circuit for one cell > 1 s = 1.4 seconds (or more than transmission medium). This leads us to the following expression:

That decrease velocity and data rate as, $R \rightarrow V$

$$\delta \rightarrow 1/R \quad (3)$$

In (3), we can conclude that the values for δ (cell duration) will be increased with respect to time. Thus, as ATM switch with processing unit has less average holding time for cells, it provides improved quality of service and CBR by formula (2).

**Case- 2**
Channel capacity of medium is defined as,

$$C \rightarrow SNR \text{ and } BER \rightarrow 1/SNR \quad \text{Property (4)}$$

Hence, as we decrease the bit error rate, signal to noise ratio and channel capacity can be improved. That results in better quality of service and CBR by formula (2).And as per the solution, ATM switch with processing unit reduces the bit error rate by HEC algorithm and by reducing possibility of retransmission.

## V. Conclusion

In this paper, we have investigated different architectures for ATM switches to improve the overall performance of ATM networks. We have shown that an appropriate architecture for ATM switch can provide a strong congestion control which can consequently use to improve the traffic management in ATM networks. In addition, we described that how scalable performance can be achieved from the ATM networks if we deploy offset mechanism in ATM switches.

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