Title: **Fast-gated 16×16 SPAD array with on-chip 6 ps TDCs for non-line-of-sight imaging**

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Fast-gated 16 × 16 SPAD array with on-chip 6 ps TDCs for non-line-of-sight imaging

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***Abstract*—We present an array of 16 × 16 single-photon avalanche diodes (SPADs) with 16 shared 6 ps time-to-digital converters (TDCs), designed for non-line-of-sight imaging. It features a timing jitter of 60 ps (FWHM), fast-gated capabilities and up to $1.6 \cdot 10^8$ photon time-tagging measurements per second.**

Keywords—SPAD array, NLOS imaging, fast-gating, time-of-flight, TDC

I. Introduction

Non-line-of-sight (NLOS) imaging is an emerging technique aiming at reconstructing images of objects hidden from the camera's direct line of sight. The operating principle of NLOS imaging is quite similar to the one of the well-known light detection and ranging (LiDAR) technique, where an active source of illumination is used for measuring the time-of-flight (TOF) of photons reflected by an object in order to retrieve its distance from the imager, while NLOS methods exploit an additional scattering mechanism involved in the process [1]. Despite such techniques being comparable from an operational standpoint, NLOS reconstructions require computational methods [2] that process the time-of-flight information, and benefit from imager features that are not required in the well-established LiDAR systems. As a result, state-of-the-art NLOS setups still rely either on single-pixels [1], or on small linear arrays of single-photon avalanche diodes (SPADs) [3], requiring long scans with external time-correlated single-photon counting (TCSPC) units for retrieving high-resolution reconstructions by processing the time-of-flight of each detected photon.

We present a fully-integrated 16 × 16 SPAD array designed for NLOS imaging, which includes a list of features currently not present in a single SPAD array among the ones described in literature: i) a picosecond-accurate single-shot precision; ii) fast-gated detection for photon time-filtering; iii) high photon detection efficiency, for harvesting the few photons that make their way back to the detector after scattering multiple times in the scene.

II. SPAD Imager for NLOS Imaging

A. BCD SPAD and array building blocks

Our NLOS imager has been fabricated in a 160 nm BCD (Bipolar-CMOS-DMOS) technology, where SPADs feature excellent performance [4]: single-pixel photon detection efficiency (PDE) reaches a 70 % at 490 nm, while timing response is as narrow as 30 ps (FWHM) when SPADs are biased at V_{EX} = 5 V above their breakdown level. Dark count rate (DCR) is low (< 1 kcps at V_{EX} = 5 V) and afterpulsing probability is negligible (well below 1 %). In addition, BCD SPADs can be integrated with transistors and electrically isolated from both the 1.8 V and 5 V fast-switching circuitry by means of deep trenches and triple-well isolation. The main building-blocks of the SPAD imager are shown in Fig. 1: i) the 16 × 16 fast-gated SPADs with their front-end circuits; ii) the 16 shared time-to-digital converters (TDCs); iii) the 16 event-driven output serializers. Squared SPADs with 32 µm sides and 100 µm pitch were chosen as a trade-off between high fill-factor and narrow time-response, with enough area for the in-pixel circuitry and for routing signals towards the peripheral electronics. The achieved fill-factor is about 9.6 % and it can be improved up to about 80 % when depositing a microlens array (MLA) on top of the detectors. The overall chip size is 4.8 × 4.8 mm^2.

B. Fast-gated frontend circuit

The SPAD frontend circuit activates the detectors in less than 400 ps by modulating the voltage across the p-n junction from below to above its breakdown level. Such fast-gating of the SPADs is needed in NLOS imaging for preventing the strong light reflections from the relay wall to easily trigger the SPADs, thus making them blind when photons scattered from the hidden scene have to be detected. With the main purpose of achieving the sharpest instrument response function (IRF), the timing jitter on the avalanche build-up is mitigated by sensing the SPAD current with a low-threshold comparator. In order to reject spurious feed-through pulses induced at the comparator input during the activation of the detectors, we employed a differential sensing, but we

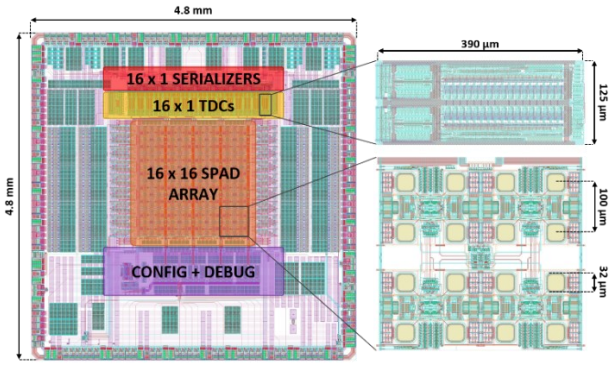

Fig. 1. Complete layout of the 16 x 16 SPAD array. The top right inset shows the layout of one TDC, placed outside the imaging area. The bottom right inset shows the layout of a group of 4 x 4 SPADs sharing the same TDC.

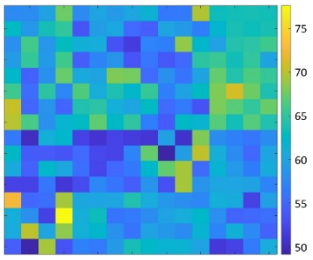

Fig. 2. Map of the IRF of the 16 x 16 SPADs. Values are in picoseconds (FWHM).

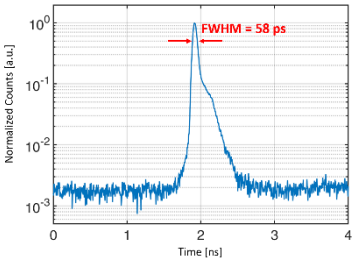

Fig. 3. Instrument response function (IRF) of a single pixel, obtained with the integrated TDC.

exploited a SPAD-SPAD couple in place of a typical SPAD-dummy one for avoiding dead areas within the array, thus maximizing the fill-factor. Additionally, such approach reduces the effect of crosstalk between adjacent detectors and lowers the power consumption.

C. Integrated TDCs and output serializers

Given the photon starved nature of NLOS imaging, each of the 16 integrated TDCs is shared among 16 SPADs. In order to improve the conversion linearity [5], the TDC includes two 10-bit interpolators: one for the START signal (i.e. the SPAD signal) and one for the STOP signal (i.e. the synchronism from the pulsed laser). A very accurate single-shot precision is granted by a two-stage architecture for each interpolator: a 6-bit fine interpolation stage featuring a single-stage cyclic Vernier delay line provides a resolution of 6 ps, which is better than the shortest intrinsic gate propagation delay achievable with this technology, thus minimizes the quantization noise contribution of the TDC to the timing jitter, while a 4-bit coarse multiphase interpolation stage, based on delay-locked loop (DLL), keeps the conversion time as short as few tens of nanoseconds. The full-scale range is extended up to 2.45 µs thanks to a 10-bit reference clock counter. Each TDC provides its 36-bit time-conversion to a dedicated dual-channel pipelined serializer, enabling TDC conversions during data transfers, thus minimizing the dead-time. Serializers are operated at 200 MHz clock frequency and exploit an event-driven readout approach, thus achieving a conversion rate up to 10 Mevents/s each, for an overall throughput of $1.6 \cdot 10^8$ conversions per second at ~ 6 Gbps transmission rate.

III. Experimental Results

The IRF of the presented NLOS imager has been characterized with a pulsed laser at 820 nm with 10 ps (FWHM) pulse width and 100 kHz repetition rate, while keeping the count rate of each TDC lower than 5% of the laser repetition rate. The timing jitter of all the pixels ranges from 50 to 75 ps (FWHM) for the whole acquisition chain, and shows a good uniformity throughout the gate window, with less than 5 ps of standard deviation within a 20 ns gate. Fig. 2 shows the timing jitter map of the 256 pixels, while an example of the IRF of a single SPAD is reported in Fig. 3.

IV. Conclusions

We present a 16 × 16 SPAD array with 16 integrated TDCs designed for NLOS imaging. Besides its fast-gating capabilities, this array features 6 ps TDCs shared among groups of 16 SPADs, thus leading to an IRF as narrow as 60 ps FWHM on average. In addition, despite the limited number of pixels, the high throughput of such imager allows to significantly cut exposure times of NLOS reconstructions when employed with fast scanning of the scene and paves the way to scaled video-rate NLOS imaging systems.

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