A PLL-Based Digital Technique for Orthogonal Correction of ADC Non-Linearity

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***Abstract*—A novel technique for automatic digital estimation and foreground correction of static distortion in Analog-to-Digital Converters (ADCs) is presented. The system exploits numerical Phase-Locked Loops (NPLLs) to autonomously generate a distortion-less replica of the input signal and to detect the spurs due to the ADC non linearity. The information is then fed to filters adaptively estimating, via Least Mean Squares (LMS) algorithms, a polynomial correction from the orthogonal inverse series. The solution is fully digital, does not require post-processing and can be expanded to cancel out the static distortion up to an arbitrary order. Performance is tested by simulations on a 12 bit ADC operating at 200MHz with a native Signal-to-Noise and Distorsion Ratio (SINAD) of 54.9dB. Polynomial compensation up to the third order is generated in 1ms, improving the SINAD by 12dB and adding 2 effective bits of resolution and more than doubling the input range of the converter.**

I. Introduction

Accuracy requirements of ADCs are becoming more and more stringent due to both the growing adoption of communication standards with increasingly complex modulation schemes, and to the intense integration of medium-high resolution applications into CMOS Systems-on-Chip at the nanoscale. Moreover, to efficiently exploit the limited voltage range of the scaled technologies, the linearity demand to analog front-ends increases, and the converter distortion is therefore becoming a limiting issue that can be addressed by adopting linearization techniques. Unfortunately, analog approaches to linearization (*e.g.* wideband feedback) are not suitable for integration into scaled CMOS nodes, since they involve high power dissipation and are limited in performance by the low supply voltage. Digital approaches, on the other hand, scale perfectly with technology, and are potentially able to compensate for the distortion generated by analog blocks with minimal digital overhead.

Figure 1(a) shows one of the most general schemes for ADC distortion compensation [1]–[4]. In this approach, the static non-linearity of the ADC is characterized in the testing phase by changing the amplitude of a harmonic input signal and comparing the input and the output signals. The information is then used to derive an inverse non-linear relationship that reduces the distortion generated by the converter. Existing implementations require parallel sampling of the analog input [1]–[3] or synthesis of the input test signal with a DAC, in order to feed the comparison block with the corresponding digital code [5]. The correction technique proposed here, evolving from [6], aims to correct distortion of ADCs whose transfer characteristic can be modeled with a non-linear polynomial and does not need the acquisition of the input signal.

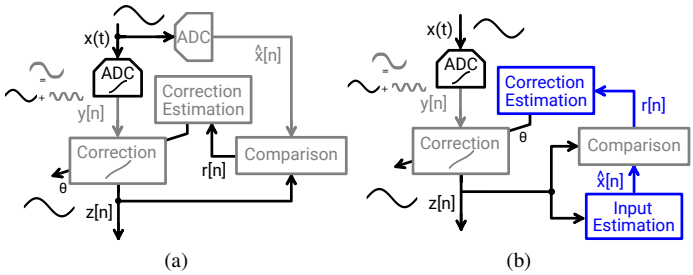

Fig. 1. (a) General scheme of ADC distortion compensation. (b) Proposed correction scheme.

The approach is fully digital and is able to automatically reconstruct the sinusoidal input signal necessary for non-linearity correction (Fig. 1(b)). Differently from [6], waveform synthesis is performed by NPLLs, as they require less hardware, and make the architecture easily scalable to any order of non-linearity correction. Furthermore, unlike prior art, the proposed correction algorithm converges to an approximation of the orthogonal series inverse [7], obtaining improved spectral performance with respect to conventional approximations of the polynomial inverse.

II. Compensation of Static Distortion

A. Post-correction scheme

To describe the compensation approach, let us consider the case of a converter with a compressive transfer, modeled as

$$y = x - ax^2 \tag{1}$$

A simple correction could be implemented using a second-order polynomial like

$$z = y + \theta_2 y^2 \tag{2}$$

The corrected output, z, is therefore given by the composition of the cascaded non-linear relationships.

$$\begin{aligned} z &= (x - ax^2) + \theta_2 (x - ax^2)^2 = \\ &= x + (\theta_2 - a)x^2 - 2\theta_2 a x^3 + \theta_2 a^2 x^4 \end{aligned} \tag{3}$$

It turns out that for $\theta_2{=}a$, the quadratic distortion term in (3) is nil. This does not mean, however, that no second order

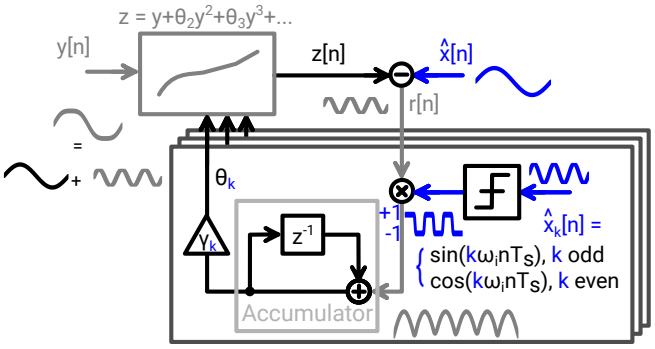

Fig. 2. Proposed static non-linearity identification and correction algorithm.

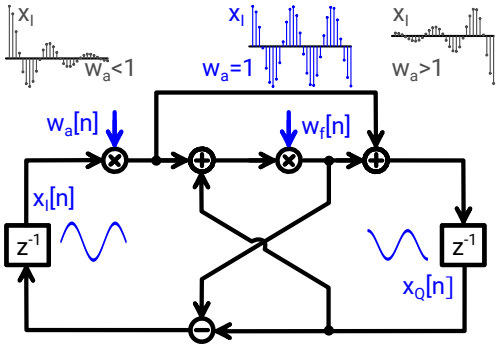

Fig. 3. DWO: frequency (w_f) and amplitude (w_a) control words change the shape of the impulse response of quadrature digital outputs x_I, x_Q.

harmonics will be present at the output. Taking the input as $x{=}A\sin(\omega_i t)$, it is

$$\begin{aligned} z &= A\sin(\omega_i t) + (\theta_2 - a)\frac{A^2}{2}[1-\cos(2\omega_i t)] + \\ &+ \theta_2 a\frac{A^3}{2}[\sin(3\omega_i t) - 3\sin(\omega_i t)] + \theta_2 a^2\frac{A^4}{4}[1-\cos(2\omega_i t)]^2 \\ &= \underbrace{(\theta_2 - a)\frac{A^2}{2} + 3\theta_2 a^2\frac{A^4}{8}}_{0} + \underbrace{\left(A - 3\theta_2 a\frac{A^3}{2}\right)\sin(\omega_i t)}_{1} + \\ &- \underbrace{\left[(\theta_2 - a)\frac{A^2}{2} - \theta_2 a^2\frac{A^4}{2}\right]\cos(2\omega_i t)}_{2} + \dots \end{aligned} \tag{4}$$

It turns out that, even if $\theta_2{=}a$ a harmonic tone at twice the input frequency is generated by the 4^{th} order term, thus resulting in a non-zero HD2. For a perfect second-harmonic cancellation, we must have

$$\theta_2 = \frac{a}{1 - a^2 A^2} \tag{5}$$

More in general, given an arbitrary non-linearity, a polynomial of degree N exists that cancels out all harmonics up to order N for a given amplitude. This polynomial can be found by computing the local inverse of the non-linear characteristic by using the orthogonal inverse series [7]. The algorithm proposed here provides an approximation of these polynomials, thus minimizing the harmonic content of the converter output up to an order N. The algorithm works directly on the sequence of the reconstructed input samples at the rate f_s, thus generating via LMS algorithms the correction coefficients without the need of further data post processing.

B. Identification implementation

Figure 2 schematically shows the procedure. During the testing phase, the converter is driven by a harmonic signal $x(t){=}A\sin(\omega_i t)$ and the converter output, $y[n]$, is fed to a polynomial correction block that should cancel out the distortion, by implementing an inverse non-linear relationship with coefficients θ_k. To properly derive the coefficients, an LMS approach is implemented. The compensated output is compared first to a clean harmonic replica of the input sine-wave. The difference generates the residual uncompensated distortion, $r[n]$, which is used to tailor the coefficients θ_k. The amplitude of each spur can be derived by multiplying the residue $r[n]$ by a set of tones, $\hat{x}_k[n]$, at integer multiples of the input radial frequency $\omega_i{=}2\pi f_i$. However, by increasing the correction order, a large number of multipliers would be needed. To limit hardware resources multipliers are therefore replaced by two-level square-wave mixing.

Moreover, since, as shown in (4), odd(even)-order harmonics of the distorted output are *in phase*(*in quadrature*) with the input, the amplitude of each intermixing term is obtained feeding the corresponding mixer with either $\hat{x}_{Ik}[n]{=}\sin(k\omega_i n T_s)$ (for k odd) or $\hat{x}_{Qk}[n]{=}\cos(k\omega_i n T_s)$ (for k even). In this way high order correction becomes feasible without large hardware penalty. To close the LMS loop, for each spur correction a simple accumulator computes the average value of the mixed residue, and having an ideally infinite DC gain tailors the coefficient θ_k to the proper value cancelling the k-th harmonic component. The scaling factor γ_k sets the trade-off between convergence time of the LMS estimate and its steady-state variance [8].

III. Harmonic Estimator

The algorithm needs an accurate estimation of the input sine-wave together with clean harmonic tones at each of the required frequencies. To this aim we propose the adoption of Numerically Controlled Oscillators (NCOs) within NPLLs.

A. Numerical oscillator

The Digital Waveguide Oscillator (DWO) shown in Fig. 3 is borrowed from the field of *Direct Digital Synthesis* (DDS), to digitally synthesize a clean sinusoidal tone with arbitrary frequency, amplitude and spectral purity [9]. The structure is very appealing for VLSI implementation, having independent amplitude and frequency controls using only two multipliers. The oscillation frequency is set by the control word $-1{<}w_f{=}\cos(2\pi f_i/f_s){<}1$. The envelope amplitude can be changed, instead, acting on w_a, which is also a number around unity (Fig. 3). When compared to a Digital-Phase-Accumulator with Look-Up-Table (DPA+LUT) implementation [10], the DWO allows to save $\approx$2 bits in the FCW for $f_i{>}f_s/40$ achieving the same frequency resolution Δf.

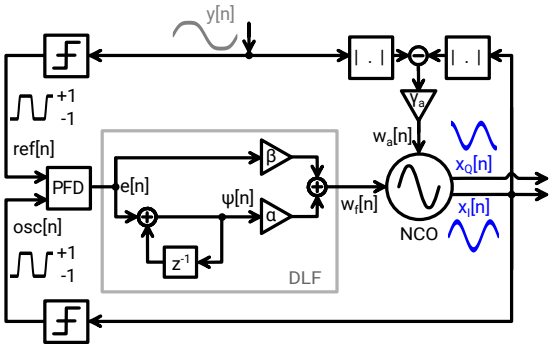

Fig. 4. Sinusoidal estimator with Amplitude tracking: A-NPLL

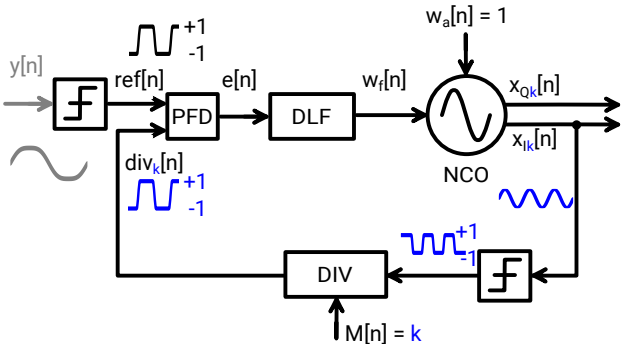

Fig. 5. Synchronous frequency multiplier: M-NPLL.

Furthermore, given a target Spurious-Free Dynamic Range (SFDR), and denoting D=SFDR$|_{\text{dB}}/6$, the DWO does not need a $\approx D\times 2^{(D+2)}$ bits LUT [10], but only a $\approx\log_2(\Delta f/f_s)$ bits multiplier. Moreover, the stage is not affected by the latency and the complexity of a CORDIC [6], being therefore better suited to be used as NCO in a PLL.

B. Fundamental tone synthesis

The fundamental tone estimate is obtained with the control loop in Fig. 4. In the testing phase, the ADC input is a harmonic signal [11], [12]. Its estimate is extracted from the ADC output, $y[n]$, by comparing the phase of the signal with the NCO waveform in a digital implementation of a PLL architecture. The *ref* and *div* signals are two-level square-waves representing the $\text{sign}(\cdot)$ function of the ADC and NCO sinusoidal outputs, respectively. Note that the $\text{sign}(\cdot)$ operation greatly reduces the impact of distortion on the signal phase, further attenuated by the loop bandwidth. A synchronous implementation of the Phase-Frequency Detector (PFD) [13] senses the phase difference between the two square-waves, generating $e[n]=\pm 1$ or 0, depending on which of the two is leading. The PFD output is fed to a standard Proportional-Integral (PI) digital loop filter, whose output $w_f[n]$ is the signal Frequency Control Word (FCW).

To remove the fundamental tone from the ADC output ($y[n]$ in Fig. 2) the estimate of the first harmonic amplitude should be very accurate. To this aim, the loop in Fig. 4 is completed with an amplitude control loop, termed A-NPLL, whose structure is inspired by the gain equalization algorithms of Time-Interleaved ADCs [14]. The difference between the absolute values of $y[n]$ and its synthesized replica $x_I[n]$ is accumulated and scaled to act on the Amplitude Control Word (ACW) w_a of the NCO. At steady state, also the error signal of this loop is ideally 0, meaning that the estimated tone has exactly the same amplitude as the corrected output. In this way, the residual signal $r[n]$ in Fig. 2 corresponds only to the tones generated by the ADC non-linearities.

C. Synthesis of higher harmonics

To complete the system in Fig. 2, auxiliary waveforms at the integer multiples of the input frequency must be generated. To this aim the synchronous frequency multiplier (M-NPLL) in Fig. 5 is adopted. The block has a Frequency Divider (DIV) in the feedback path between the NCO and the PFD. No amplitude control is needed in this case, as only the $\text{sign}(\cdot)$ of the output signal is of interest. Each additional PLL thus requires a single multiplier (for the NCO FCW) as the ACW is fixed to unity for constant amplitude. The DIV is easily synthesized as an edge counter. Since each PLL is independent of the others, the loops can be paralleled to obtain the desired harmonics with no speed penalty and minor added power.

IV. Simulation Results

Behavioral simulations of the system allow to size and test the quantization levels required for a given target spectral purity. In the example of Fig. 6 the correction is cascaded to a model of a 12 bit ADC, with distorted transfer $y(x)=x+\beta_e|x|+\beta_o x|x|$, clocked by a 200 MHz reference. The NPLL FCW and ACW are quantized to a 16 bits resolution, as well as the phase error accumulator output. The NCO output $\hat{x}[n]$ is on 12 integer and 3 fractional bits to further improve the estimation, whereas 6 bits are enough for the residue $r[n]$, as shown in Fig. 6. The square-wave mixing simply acts on the sign bit of $r[n]$, thus not requiring additional range.

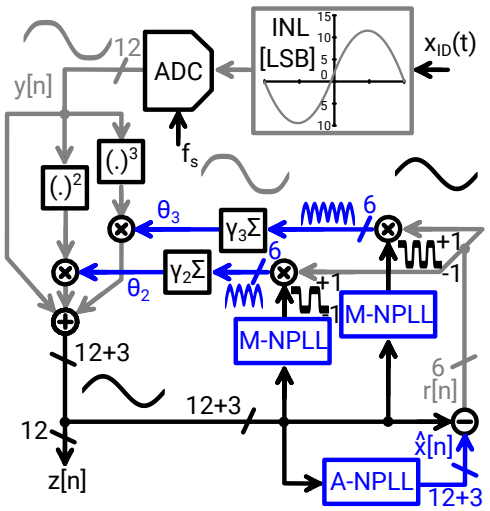

Fig. 6. Block diagram of 3rd order simulated system. The ADC has a distorted characteristic with the $-10/+12$ LSB INL reported in the input block.

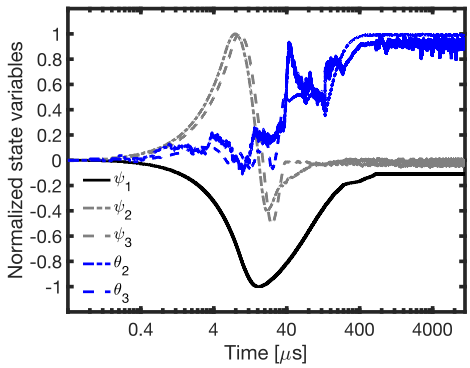

Fig. 7. Locking transients of estimator state variables (normalized).

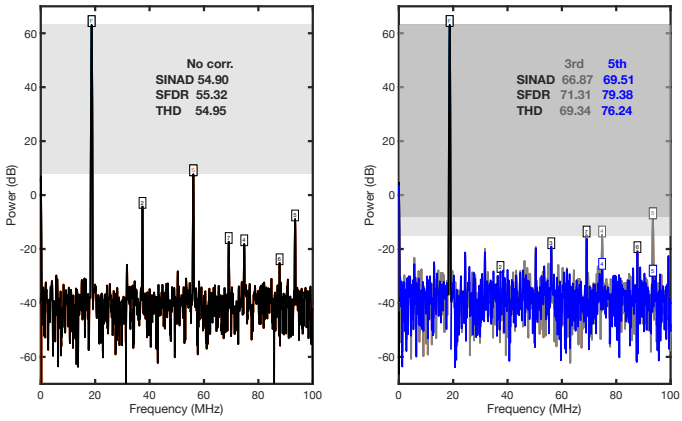

Fig. 8. Spectra before and after correction convergence: the selected harmonics are cancelled (up to the 3rd, grey, and to the 5th, blue).

Figure 7 shows the transients of the correction loop variables: ψ_k is the output of the loop filter accumulator of the k$^{\text{th}}$ NPLL, whereas θ_k is the coefficient of the corresponding monomial in the correction block, *i.e.* the scaled output of the feedback accumulator. The convergence is reached within 1ms, with negligible overhead in a testing setup. Figure 8 shows the spectra of the 12 bit words before and after the correction blocks with transfer $z(y)=y+\theta_2 y^2+\theta_3 y^3$, once the θ_k coefficients have reached their final values. The dominant spur of the output waveform is reduced by more than 30dB, improving the Signal-to-Noise And Distortion (SINAD) ratio by more than 12dB, corresponding to an increase of $+2$ Effective Number of Bits (ENOB). Figure 9 shows the ADC performance as the input amplitude sweeps from a decade before to an octave after the amplitude value adopted for distortion estimation. The ADC output, passed through the non-linear characteristic with the stored θ_k values, shows a SFDR better than 67dB over an input range that is more than double the native value. The same figures also show the case of 5$^{\text{th}}$ order correction, proving the scalability of the technique.

V. Conclusion

The work describes a novel, fully digital technique to automatically estimate distortion compensation coefficients for ADC post-correction. The system does not need direct sampling of the input signal. Numerical PLLs are used to estimate the sinusoidal testing tone and to derive information on distortion. The scheme is well suited for implementations *on chip* or on a FPGA. Simulations on a 12 bit ADC with severe INL have been provided to demonstrate performance improvements. Thanks to the independent estimation of the correction coefficients via LMS algorithms and to the adoption of polynomials from the orthogonal series inverse, the approach can be generalized to effectively cancel-out any distortion order.

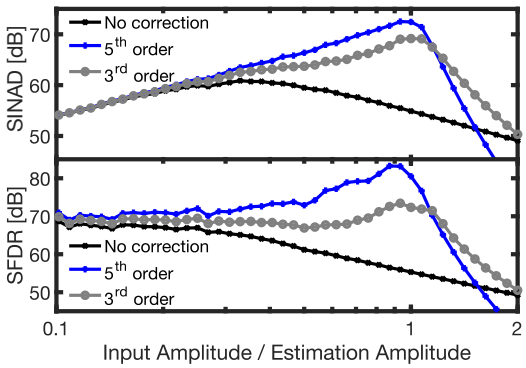

Fig. 9. Single-tone amplitude sweep with the stored correction coefficients estimated for unit amplitude (3rd order, grey, 5th order, blue).

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