Self-Biasing Dynamic Start-up Circuit for Current-Biased Class-C Oscillators

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***Abstract*—This work presents a very compact self-biasing dynamic start-up circuit for class-C voltage-controlled oscillators (VCOs). Using a reference-less nonlinear inverting stage, the solution has been implemented in a 28nm CMOS technology 14GHz oscillator, leading to a VCO start-up time better than 20ns, at par with the fastest start-up circuits in literature, with an extremely compact area of $0.003\mathrm{mm}^2$.**

***Index Terms*—Class-C, dynamic bias, oscillator, start-up, VCO.**

I. Introduction

Since their introduction, class-C oscillators have drawn interest for their ability to reach better phase noise than class-B topologies for comparable or lower power dissipation [1]. However, to guarantee robust start-up and high efficiency at steady state, additional circuitry is needed. Fig. 1 shows a current-biased implementation of a class-C oscillator, in which the transistors are alternately switched by the periodic oscillation; the large tail capacitance, C_{TAIL}, acts as a low-impedance source of current pulses delivered to the LC resonant tank. Conflicting requirements hold for the differential pair bias voltage, V_{BIAS}: on start-up, it should be high enough to quickly switch on the transistor pair; at steady state, it must be lowered to turn the transistors off for most of the oscillation period, thus increasing the DC to RF current conversion efficiency and, in turn, the oscillation amplitude for the same current consumption.

To this aim, several solutions have been proposed in literature. In [2], [3], the tank losses are overcome on start-up by adding a *cross-coupled pair in class-B operation*, but at the expense of efficiency and area. In [4]–[7] an *amplitude feedback* loop senses the oscillation amplitude, acting on V_{BIAS} to switch on the transistor pair on start-up and then pushing the devices in class-C at steady state. However, the amplitude peak detector loads the tank, thus reducing its quality factor. This limitation is circumvented by the *dynamic bias* approach [8], [9], where the class-C stage operation is indirectly sensed on the bias voltage across the tail generator with an *OTA*, without loading the tank, then acting on V_{BIAS}. The setup, though, needs an *OTA* and an external reference voltage. In this paper a simple yet effective *self-biasing dynamic* start-up circuit is presented, reaching start-up performance at par with the fastest start-up circuits in literature [8] and with minimal circuit overhead.

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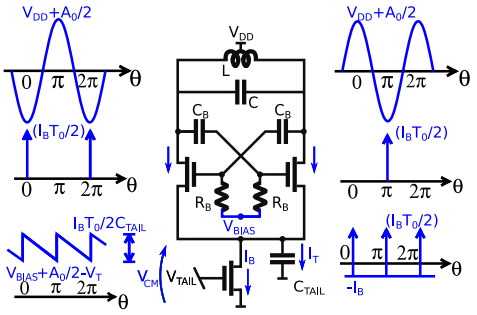


Fig. 1. Current-biased class-C oscillator. Waveforms in the ideal case of transistors acting as ideal switches.

II. Self-biasing Start-Up Circuit

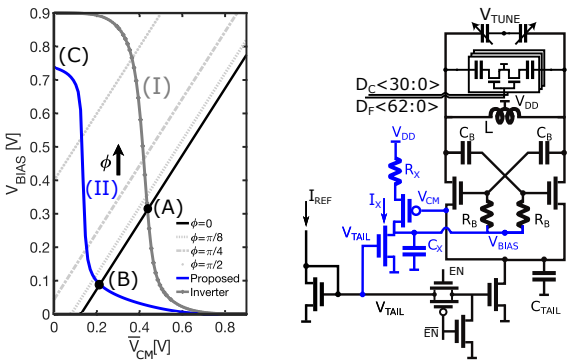
To appreciate the solution proposed here, let us first describe how a *dynamic bias* circuit sets the steady state operation of a class-C oscillator (Fig. 1). Assuming for simplicity that the transistors act as ideal switches, delta-like current pulses are delivered to the tank twice per each oscillation period, T_0. At the same time, these pulses refill the tail capacitance, C_{TAIL}. Each transistor turns on when its gate voltage reaches the positive peak value at $V_G = V_{BIAS}+A_0/2$, while the common source node potential, V_{CM}, is at $V_G - V_{T_n}$. It follows that V_{CM} has a sawtooth waveform, as reported in Fig. 1, starting from the value $V_{BIAS} + A_0/2 - V_{T_n}$ and with peak-to-peak amplitude q_P/C_{TAIL}, where $q_p = I_B T_0/2$ is the charge of each pulse. Denoting as R the lumped parallel losses of the tank, the differential zero-peak oscillation amplitude, A_0 is given by $I_B R$, since I_B is the first harmonic of the differential current generated by delta-like pulses with charge q_p. Based on these results, a link can be derived between the average common source voltage, $\overline{V_{CM}}$, and V_{BIAS}, namely

$$\overline{V_{CM}} = V_{BIAS} - V_{T_n} + \frac{A_0}{2} + \frac{I_B T_0}{4C_{TAIL}}. \tag{1}$$

Neglecting the voltage ripple (large C_{TAIL}) and using $A_0 = I_B R$, we get

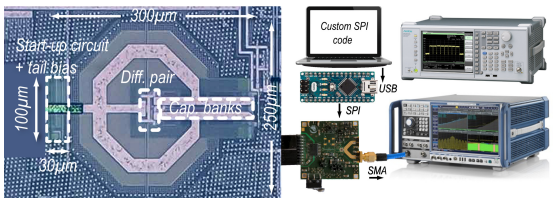
$$V_{BIAS} \approx \overline{V_{CM}} + V_{T_n} - \frac{I_B R}{2}. \tag{2}$$

Note that (2) appears as a load line over the $(V_{BIAS}, \overline{V_{CM}})$ plane in Fig. 2(a) (solid line). It follows that a simple way to set the steady state operating point of the class-C oscillator is to insert an inverting stage between V_{BIAS} and V_{CM}. This corresponds to superimposing the static characteristic line (I) over the load line in Fig. 2. In this way the steady state



(a) (b)

Fig. 2. (a) Inverter characteristics and load lines from (2) and (4) for different transistor conduction angles, 2ϕ; (b) Class-C oscillator with the proposed start-up circuit. The circuit bridges the nodes at V_{BIAS} and V_{CM} which are points of symmetry of the VCO.



(a) (b)

Fig. 3. (a) VCO micrograph with main blocks highlighted and (b) schematic measurement setup. The start-up circuit occupies 0.003mm^2 and was placed along the symmetry axis of the differential pair.

operating point goes to (A). This result can be extended to realistic circuit operation. Even if transistors work in saturation and current waveforms deviate from ideal delta-like pulses the link (2) is preserved with minimal formal variations. Denoting as 2ϕ the transistor conduction angle during each oscillation cycle, it is

$$\phi = \arccos\left(\frac{\overline{V_{CM}} + V_{T_n} - V_{BIAS}}{A_0/2}\right). \tag{3}$$

Assuming the classical square dependence for the transistor current, $I_{DS} = k_n(V_{GS} - V_T)^2$ and following [1], it can be shown that the link between V_{BIAS} and $\overline{V_{CM}}$ is given by

$$V_{BIAS} = \overline{V_{CM}} + V_{T_n} - \frac{I_B R}{2}\frac{\beta(\phi)}{\gamma(\phi)}\cos(\phi), \tag{4}$$

which is the extension of (2) to the case of finite ϕ, where $\gamma(\phi)$ and $\beta(\phi)$ are transcendental functions[1]. The resulting load lines are reported as dotted-lines in Fig. 2 for increasing ϕ, corresponding to decreasing transistors conductivity, k_n. On the other hand, to maximize A_0 and therefore phase noise, it is convenient to shift the steady state V_{BIAS} closer to ground, with $\overline{V_{CM}}$ as close as possible to the tail transistor overdrive (point (B) in Fig. 2(a)). To this aim, a better solution corresponds to the solid curve (II), which can be obtained using the *OTA*-based topology of [8]. The solution proposed here implements the same concept with a *self-biased*, *more compact inverting stage* (Fig. 2(b)). In this circuit, the nMOS sets the bias current, I_X, while the pMOS conductivity, k_p, and the resistor R_X shift the transition of (II) to a suitably low $\overline{V_{CM}}$ value (Fig. 2(a)), the corresponding sizing equation being

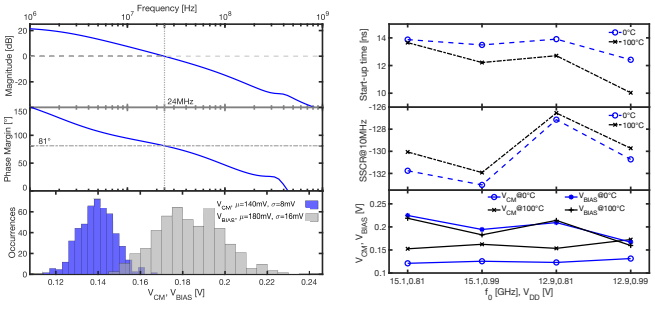
$$\overline{V_{CM}} \approx V_{DD} - R_X I_X - |V_{T_p}| - \sqrt{\frac{I_X}{k_p}}. \tag{5}$$

In conclusion, when at start-up V_{CM} is close to GND and the pMOS is ohmic, V_{BIAS} is pulled close to the supply to point (C) in Fig. 2(a), $\approx V_{DD} - R_X I_X$, ensuring fast turn-on transient. At steady state, the operating point shifts to class-C, lowering V_{BIAS} to (4) as $\overline{V_{CM}}$ settles to (5).

III. Implementation and Results

The self-biasing start-up circuit was implemented in a 28nm bulk CMOS technology and embedded in a 14GHz oscillator with 31 coarse and 63 fine segmented digital capacitor banks and an analog tuning varactor, covering the 12.9GHz-15.1GHz frequency range [10], [11] (Fig. 3(a)). To limit current consumption I_X was set to 0.35mA, which is only 5% of I_B. To maximize the output voltage swing, the nMOS tail current generator was sized with an overdrive $V_{OV} \approx 0.1$V. Based on (5), the resistance R_X and the pMOS conductivity k_p, were chosen as $R_X = 250\Omega$ and $k_p \approx 20$mA/V^2, respectively, to have $\overline{V_{CM}} \approx 0.14$V, and $V_{BIAS} \approx 0.18$V at steady state. The resulting V_{BIAS} value on start-up is $(V_{DD} - R_X I_X) \approx 0.75$V, enough for fast oscillation turn-on. To prevent *squegging*, a capacitance, C_X, is attached to V_{BIAS}. On this matter, note that a disturbance on V_{CM}, after being transferred to V_{BIAS}

[1] $\beta(\phi) = [2\sin(\phi) + \sin(\phi)\cos^2(\phi) - 3\phi\cos(\phi)]/6\pi$;
$\gamma(\phi) = [2\phi - \frac{3\sin(2\phi)}{2} + \phi\cos(2\phi)]/4\pi$.



(a) (b)

Fig. 4. Stability and PVT: (a) magnitude and phase margin (PSTB) and Monte Carlo at 100°C on (5); (b) start-up time, noise and bias *vs* f_0, T and V_{DD}.

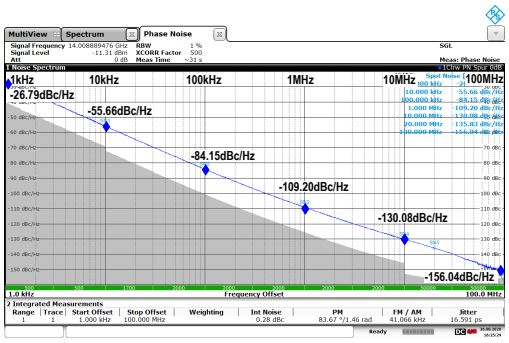


Fig. 5. Measured VCO phase noise at 14GHz.

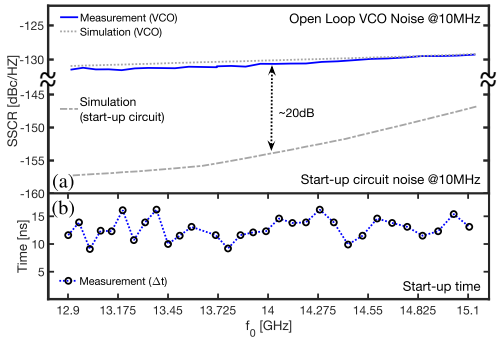


Fig. 6. Circuit performance *vs.* tuning range: (a) VCO phase noise at 10MHz offset and contribution of the start-up circuit; (b) measured start-up time.

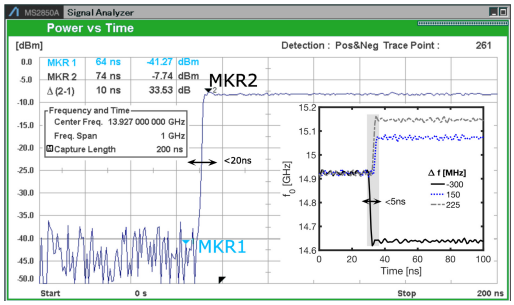


Fig. 7. Measured start-up transient and frequency hops (inset).

by the inverting stage, has two ways to move back to its injection point [8]: (i) a low-frequency path, causing the source terminals to follow the gate variation as in (4); (ii) a RF path through the up-conversion of the perturbation on V_{BIAS} around f_0, due to the mixing action of the switching pair. The $R_B C_B$ coupling network brings back the amplitude modulated carrier to the nMOS gates, where it is down-converted to baseband and transferred to V_{CM}. It follows that, to check amplitude stability, a series probe must be placed on the pMOS gate (node at V_{CM} in Fig. 2(b)), thus accounting for both paths. Fig. 4(a) shows the resulting amplitude and phase of the loop gain derived by Spectre®RF Periodic Stability Analysis (PSTB). The adoption of $C_X = 1$pF is enough to shift the unity gain loop bandwidth at ≈ 24MHz, leading to unconditional stability against amplitude disturbances with a 81° phase margin.

The sizing was then tested against phase noise performance. With a bias current I_B of 7mA from a 0.9V supply, the differential oscillation amplitude is $A_0 = 0.86$V, leading to $\phi \approx \pi/4$, similar to the values in [1], [2]. Fig. 5 shows the output phase noise measured at 14GHz with the R&S®FSWP26 Phase Noise Analyzer of Fig. 3(b). The measurements match the Spectre®RF post-layout simulation results over the tuning range (Fig. 6(a)). The worst-case noise contribution of the start-up circuit is at 10MHz frequency offset, 18-26dB below the overall phase noise. The transient performance displayed in Fig. 6(b) and Fig. 7 were characterized with the *Power/Frequency vs time* tools of the *MS2850A* Anritsu Signal Analyzer of Fig. 3(b), measuring the output signal after on-chip buffering to drive the wire-bond, coplanar waveguide and SMA connection to the instrument. In the start-up measurements, the output power settles to its steady state value (MKR2) in less than 20ns from the wake-up signal (MKR1) controlling the tail transmission gate of Fig. 2(b). The same setup was adopted to test the performance of the bias circuit across the tuning range: the inset of Fig. 7 shows the superposition of several measurements corresponding to different steps of the coarse capacitor banks. In this case the transient is much faster than the start-up time, therefore not limiting the VCO frequency hops. The results confirm the circuit robustness to amplitude variations.

The impact of PVT variations on nominal performance, shown in Fig. 4, was analyzed by: (a) Monte Carlo simulations at 100°C of the parameters of (4) and (5), with fixed current and tank; (b) simulations at 0°C and 100°C, $V_{DD} \pm 10\%$ at the edges of the tuning range. The standard deviation values less than 10mV and 20mV for V_{CM} and V_{BIAS}, respectively, pose no issues. The VCO operates properly in most adverse conditions, with a worst-case 3dB penalty of phase noise when the combination of highest tank Q and lowest voltage headroom briefly pushes the pair out of saturation. In this case proper performance can be recovered by slightly changing the bias current.

Tab. I compares the measured results with prior art. Since most of the papers in literature do not provide the area of the start-up circuit, complexity and area of the different solutions are quoted by reporting in the last column the number of active devices, and the presence of a voltage reference and/or auxiliary control signals, marked by asterisks. The simple start-up circuit presented here clearly matches the best start-up performance shown so far in literature with minimal complexity and area occupation.

TABLE I
START-UP CIRCUITS FOR CLASS-C VCOS.

Start-up/ bias	Work, year	Tech [nm]	f_0 [GHz]	T_{start} [ns]	MOS count
Dual pair	Okada 2009 [2]	180	4.5	class-B	2*
	Song 2016 [3]	65	2.46	10	9*
Amplitude feedback	Chen 2011 [6]	180	3.1	100	20*
	Zhu 2015 [7]	180	5	1500	7*
	Xu 2017 [4]	56†	18.7	30	8*
	Fang 2018 [5]	40†	16	30	2
OTA feedb.	Fanori 2013 [8]	90	3.9	20	6*
	Perticaroli 2014 [9]	55	7.15	> 1000	5*
pMOS	**This work**	**28**	**14**	$\mathbf{< 20}$	**2**

†:SOI,∗: extra reference voltage needed.

IV. CONCLUSIONS

A simple self-biasing start-up circuit is proposed for current-biased class-C LC-VCOs. The circuit occupies only 0.003mm^2, and is reference-less, fast and low-noise. The sizing requires minimal effort. The circuit was included in a 14GHz class-C oscillator implemented in a 28nm bulk CMOS technology, with a 12.9GHz-15.1GHz tuning range. Measurements of start-up transients within 20ns are reported, together with ns frequency transient after switching of the coarse capacitive banks, at par with the state-of-the-art.

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