# Surface evolution of 4H-SiC(0001) during in-situ surface preparation and its influence on graphene properties

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**Abstract.** The evolution of SiC surface morphology during graphene growth process has been studied through the comparison of substrate surface step structure after in-situ etching and graphene growth in vacuum. Influence of in-situ substrate surface preparation on the properties of graphene was studied through the comparison of graphene layers on etched and un-etched substrates grown under same conditions.

## Introduction

Semi-insulating (SI) SiC is a natural choice of substrate for graphene-based high-frequency fieldeffect transistors. A few layer graphene can be obtained on the Si-face of SiC substrate through thermal decomposition of the surface. However, high temperature growth processes leads to surface step-bunching and defect-selective etching native to the Si-face of SiC. These phenomenon severely degrade the surface and result in very large steps and pits on the surface. Thermal evaporation rate of Si at surface damages is higher and leads to multiple layers of graphene on steps and defect related etch pits and limits the graphene thickness uniformity to a very small area. Native properties of graphene are directly related to its total thickness and uniformity therefore, a better control of graphene thickness uniformity is important to realize its potential in electronic devices. Large steps on the surface also influence the charge carrier mobility [1], an important parameter for high frequency devices. A better control of surface morphology prior to and during graphene growth is highly required to control surface non-uniformities and thickness uniformity on a large scale.

In this study we focus on the surface step evolution of Si-face of semi-insulating (SI) on-axis 4H-SiC substrates during in-situ surface preparation and graphene growth, and properties of graphene grown on etched and un-etched substrates. A process of in-situ surface preparation and a-few-layer graphene growth is developed at relatively low temperature to minimize the surface degradation and non-uniformities in thickness over large areas.

# Experimental

Chemo-mechanically polished (CMP) SI on-axis 4H-SiC cut into 20 x 20 mm<sup>2</sup> chips were used as substrate. A horizontal hot-wall CVD reactor equipped with a SiC coated graphite susceptor was used for graphene growth along with pre- and post-growth processes. Two set of experiments were conducted to compare the influence of in-situ substrate surface preparation on graphene properties. Each set of experiments was further divided into two growth processes to compare the influence of hydrogen intercalation on charge carrier mobility. In first set of experiments the first growth process

was started with in-situ surface preparation of substrate followed by graphene growth while in second growth process hydrogen intercalation was also performed after in-situ etching and graphene growth. In second set of experiments, in first growth process, graphene was grown on as-received substrate without any in-situ surface preparation while in second growth process samples were also intercalated with hydrogen. Each growth process was done in a single sequence without exposing the samples to air. Same growth temperature, pressure and hydrogen intercalation conditions were used during each set of experiments. In order to remove substrate surface damages in-situ surface preparation [2] was made in a mixture of hydrogen and silane (0.06%) for 10 minutes at 1400 °C. Graphene was grown at relatively low temperature of 1400 °C in vacuum (1 x 10<sup>-5</sup> mbar) for one hour. Hydrogen intercalation was made in the temperature range of 700-800 °C at 500 mbar for one hour. Optical microscope with Nomarski diffractional interference contrast and atomic force microscopy (AFM) in tapping mode was used to study surface morphology and surface step structure. Numbers of graphene layers were observed with low energy electron microscopy (LEEM). Contactless measurement of charge carrier mobility was made with Leighton's microwave reflectivity equipment. Van der Pauw device structures were also made through lithography ohmic contacts of Ti/Au 300/700 Å. We have designed and fabricated a photomask with electron beam lithography in order to perform each fabrication step of Van der Pauw devices with optical lithography. Ohmic contacts were fabricated with reverse lithography technique. After development, 20 nm Ti and 100 nm Au were deposited by electron beam evaporator followed by standard lift-off process. Mesa lithography step was performed in order to preserve the active graphene region, while etching the rest of the graphene on the sample surface with O<sub>2</sub> plasma. Interconnect metal lithography was performed by using 30 nm/220 nm Ti/Au metal pair.

#### **Results and discussion**

Surface evolution during in-situ etching. CMP SiC wafers usually have smooth surface but may have surface damages in the form of scratches and pits. Polishing related damages were significantly removed after in-situ surface treatment of substrates at 1400 °C. Two kinds of surface morphologies can be identified on the same sample, low step-bunched with large smooth areas between elongated features (Fig. 1a) and heavily step-bunched with high density straight steps (Fig. 1b) visible in optical images. Elongated features and big steps are related to surface step-bunching native to Siface of SiC. The height of elongated features in low step-bunched regions is 10-20 nm (Fig. 1c), large areas of several hundred  $\mu$ m between elongated features are covered with micro-step structure



Fig. 1 Optical image taken after in-situ surface preparation a) low magnification b) high magnification. AFM image c) from a region marked in (a), d) marked in (c), e) marked in (b) and f) marked in (e).



Fig. 2 Optical image taken after graphene growth a) from region similar to that in Fig.1a, b) high magnification image, and (c) AFM image from the area between big steps in (b).

of 1 nm height (Fig.1d). The un-intentional off-cut of the wafer, as measured in the middle of the wafer with high resolution X-ray diffraction, was 0.08 ° however this can vary across the wafer due to basal plane bending related to basal plane dislocations. The local off-cut, as measured using terrace height and width in the region given in Fig. 1a, is between 0.12-0.14°. In heavily stepbunched regions (Fig. 1b) the height of large steps is 20-30 nm (Fig. 1e) however, the regions between large steps is covered with 1 nm height steps (Fig. 1f). The local off-cut measure similarly in this region is 0.02-0.04°. A clear difference in local off-cut in two kinds of regions is also obvious from the step density where large terrace width in Fig. 1f corresponds to small off-cut.

**Surface evolution during graphene growth.** The fine micro-step structure between large steps in both kinds of regions completely vanished during graphene growth at 1400 °C under vacuum  $(1 \times 10^{-5} \text{ mbar})$  and the surface evolved with relatively large but sharp steps of 5-10 nm (Fig. 2a-c). Big step formed during in-situ surface preparation (marked with white arrows in Fig. 2a and b) still persist on the surface and the overall surface morphology further degraded due to additional step-bunching during graphene growth. A very few defect selective etch pits, marked with white arrow in Fig. 2c, are also observed on the surface after graphene growth.

**Surface evolution during graphene growth on un-etched substrates.** A relatively smooth surface with less step-bunching is observed after graphene growth under the same growth conditions directly on as-received substrate without any in-situ substrate surface preparation prior to the growth (Fig. 3a). AFM shows relatively small steps of 5-10 nm (Fig. 3b) however, the steps not very sharp. The polishing related substrate surface damages, marked with white arrows in Fig. 3a and b, still present on the surface after graphene growth. This is mainly due to very low thermal decomposition rate of SiC surface in vacuum at such low temperature of 1400 °C compared to in a mixture of hydrogen and silane which affectively etch away the surface and removes surface damages.

**Comparison of graphene properties.** Graphene growth on etched substrates showed mainly 2 graphene layer coverage on entire sample with 3-4 layers on big step edges (Fig. 4a). Graphene thickness is quite uniform over large terraces and a well defined pattern corresponding to the surface step structure is observed on the surface. Graphene growth on un-etched substrates showed 0-2



Fig. 3 (a) Optical image after graphene growth and (b) AFM image. Surface damages are highlighted with white arrows in both images.



Fig. 4 LEEM image (field of view=30  $\mu$ m) of as-grown graphene on a) etched, and b) un-etched substrate.

layers of graphene, however the thickness in not uniform and graphene grains are very small and irregular in shape. A better graphene morphology observed on etched substrate could be related to well define surface step structure formed during in-situ surface preparation.

**Influence of hydrogen intercalation.** In-order to transform the carbon buffer layer at the interface of substrate and graphene, hydrogen was introduced to the growth cell after the graphene growth. Contactless microwave reflectivity measurements showed a relatively low charge carrier mobility of 250-300 cm<sup>2</sup>/Vs in as-grown graphene on un-etched substrates compared to 600-700 cm<sup>2</sup>/Vs in graphene grown on etched substrates. Hydrogen intercalation significantly improved charge carrier mobility in graphene grown on un-etched and etched substrate to 1500 cm<sup>2</sup>/Vs and 2500 cm<sup>2</sup>/Vs, respectively. Higher charge carrier mobility in graphene grown on etched substrates could be due to large area coverage with uniform thickness of graphene. Hall mobility values as measured from Van Der Pauw device structures made in different graphene layers but under the same growth conditions on etched and un-etched substrates and with hydrogen intercalation showed similar values of about 1500-2000 cm<sup>2</sup>/Vs. This difference could be due to graphene damages during device processing, however more statistical data is required to understand the difference.

#### Summery

Surface evolution of SiC was studied and compared after in-situ surface preparation and graphene growth in vacuum. Fine surface step structure formed during in-situ etching was replaced with large steps due to step-bunching during graphene growth. Morphology and properties of graphene on etched and un-etched substrates was also compared. A relatively smooth surface is obtained on un-etched substrate however, with polishing related damages. The polishing related damages were efficiently removed on etched substrate. A high charge carrier mobility observed graphene layers on etched substrates is attributed to uniform thickness of graphene over large areas.

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